STUDY OF ELECTRICAL PROPERTIES IN BORON-DOPED P-TYPE ULTRANANOCRYSTALLINE DIAMOND/N-TYPE SILICON HETEROJUNCTIONS

RAWIWAN CHALEAWPONG

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENT FOR THE
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DEPARTMENT OF PHYSICS
FACULTY OF SCIENCE
KING MONGKUT'S INSTITUTE OF TECHNOLOGY LADKRABANG
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Thesis Certification

Thesis Title	Study of electrical properties in boron-doped p-type ultrananocrystalline diamond/n-type silicon heterojunctions
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Department	Physics
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Date 31th July 2018

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Abstract

Heterostructure diodes comprising B-doped UNCD/a-C:H films and Si wafer were constructed utilizing pulsed laser deposition. In the first part, their dark current density-voltage (*J* - *V*) characteristics were measured at low temperatures. Based on the *J* - *V* characteristics, the estimation of junction parameters was performed via TE theory, Cheung and Norde models. Via TE theory, the values of the barrier height were 0.78 eV at 300 K and 0.18 eV at 60 K, while the values of the ideality factor were 2.70 at 300 K and 8.66 at 60 K. Both parameters were equivalent with those estimated through both Cheung and Norde models. The values of the series resistance (R_s) calculated via Cheung model were 271.41 Ω at 300 K and 72.38 kΩ at 60 K. These values of R_s are consistent with those calculated via Norde model. In the second part, by means of impedance spectroscopy, the real part (Z') and imaginary part (Z'') characteristics were measured as a function of V values ranging from 0 V - 2 V. The curves of Z''-Z' presented a single semicircle for all bias voltages. The center of semicircles lies below the Z'' axis. The diameter of the semicircle decreased with increasing V values. The idiosyncrasy of the semicircular curve indicated that the junction behavior should be appropriate with the parallel resistance (R_p) and constant phase element (CPE) in parallel combined with R_s. From the simulation by EC-lab software, the values of R_s were 171.55 Ω at 0 V and 52.97 Ω at 2 V. At 0 V, the value of R_p was 1.88×10^6 Ω and it decreased to 4.67×10^5 Ω at 2 V. The value of CPE was 2.14×10^{-9} F together with α value of 0.90 at 0 V. At the V value of 2 V, the CPE value dropped slightly to 1.13×10^{-9} F, while α value was 0.91.

Keywords : Heterostructure diodes, Diode parameters, Circuit Parameters

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Miss Rawiwan Chaleawpong

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Chapter 1

Introduction

1.1 Background

The composite film of ultrananocrystalline diamond (UNCD)/hydrogenated amorphous carbon (a-C:H) consists of a large number of diamonds in nanograins with the diameter of crystalline approximately 5-10 nm which are embedded in an a-C:H matrix [1-4]. Currently, the films of UNCD/a-CH have acquired substantial attention for the utilization in the optoelectronic devices [5], micro-electro-mechanical systems [6-7], electron-field emission sources [8], and hard coating [9] as the result of their features owing to a lot of grain boundaries. UNCD/a-C:H film has been reported that held the peculiarities as follows: (i) very smooth film surface [1,5,10], (ii) high hardness and modulus [11], (iii) specific characteristic of electrical and optical properties because of a lot of grain boundaries [10,12], (iv) more stability in temperature than diamond-like carbon (DLC) [1,10]. Furthermore, UNCD/a-C:H film can be constructed on many types of the solid substrate [1,10]. By the usage of pulse laser deposition (PLD), the constructed films of UNCD/a-C:H hold high optical absorption coefficients beyond 10^5 cm^{-1} in the photon energy ranging from 3 eV to 6 eV [1,5]. The construction of p-type and n-type conductions can be achieved by impletion of boron (B) and nitrogen (N) substances, respectively [13,14].

Previously, the layer of UNCD/a-C:H has been grown on Si wafer by the usage of PLD. The UNCD/a-C:H layer was investigated to explore the basis of physical features [5,15]. Afterward, the construction of the heterostructure diode comprising B-doped UNCD/a-C:H films and Si wafers was accomplished by using PLD apparatus. The the heterostructure diode comprising B-doped UNCD/a-C:H films and Si wafers were examined at the temperature of 300 K to corroborate the rectifying characteristic and the detection of deep-ultraviolet (DUV) Light [16,17]. Besides, the enhancement of current rectification and DUV detection for the heterostructure diode comprising B-doped UNCD/a-C:H films and Si wafers was attested at low temperature [17]. Nevertheless, the performance of detecting DUV light was unexpectedly low. Therefore, the considerable diode parameters such as ideality factor (n), barrier height (ϕ_b), and series resistance (R_s) for the heterostructure diode comprising B-doped UNCD/a-C:H films and Si wafers were estimated to understand the cause of degradation. However, the investigation regarding the electrical properties of the heterostructure diode comprising B-doped UNCD/a-C:H films and Si wafers require more study to understand their behavior.

In general, the impedance spectroscopy is a proper measurement for studying the electrical features by monitoring the response of devices to an AC signal [18-20]. This approach has been broadly applied to investigate the electrical features in solar cell and heterojunction diodes [18-20]. Tough, the investigation of impedance characteristics based on devices consisting of UNCD/a-C:H films has been reported by a few research groups. Consequently, the study about the impedance spectroscopy was applied in the current work to understand more about the behavior of the heterostructure diode comprising B-doped UNCD/a-C:H films and Si wafers. Via impedance spectroscopy, the real part (Z') and imaginary part (Z'') of complex impedance were extracted. Based on the characteristics of Z''-Z', the equivalent electric circuit model and circuit parameters such as R_s, parallel resistance (R_p) and constant phase element (CPE) were examined.

1.2 Research goals

1. Investigate the surface, thickness, and roughness for the film of B-doped UNCD/a-C-H films formed on Si wafer substrate.
2. Assess the considerable diode parameters such as n , R_s, and ϕ_b for the heterostructure diode comprising B-doped UNCD/a-C:H films and Si wafers from the measurement of current-voltage (I-V) at different temperatures.
3. Provide impedance characteristics and the equivalent circuit under various voltages for the heterostructure diode comprising B-doped UNCD/a-C:H films and Si wafers.
4. Extract the circuit parameters such as R_s, R_p and CPE for the heterostructure diode comprising B-doped UNCD/a-C:H films and Si wafers from the simulation by employing EC-Lab software.

1.3 Research scopes

1. The investigation of the film surface, thickness and roughness were performed utilizing Field Emission Scanning Electron Microscopy (FESEM) and Atomic force microscope (AFM).
2. Using the characteristics of I-V, the values of n, R_s and ϕ_b were extracted on the basis of thermionic emission (TE) theory, Cheung's model and function of Norde.
3. By usage of the characteristics of the real part (Z') and imaginary part (Z'') of complex impedance, the equivalent circuit model was provided.

4. Based on the equivalent circuit model, the circuit parameters were simulated using EC-Lab software.

1.4 Research organization

Table 1.1 Schedule of the operation procedures

Procedures	Aug-Oct	Nov-Jan	Feb-Apr	May-Jul
Study the related principles and literature concerning the current research.	↔	↔		
Investigate the surface morphology and the roughness of the films.	↔			
Measure the curves of *I-V* and *Z"-Z'*.		↔		
Evaluate and simulate the vital diode parameters and circuit parameters using the idiosyncrasy of *I-V* and *Z"-Z'* curves, respectively.			↔	
Analyse the data and prepare the master's thesis.				↔

1.5 Expectation

1. Reveal the features of surface, thickness, and roughness for the film.
2. Expose the considerable diode parameters for the heterostructure diode comprising B-doped UNCD/a-C:H films and Si wafers.

   Provide the impedance characteristics, equivalent electric circuit model and circuit parameters for the heterostructure diode comprising B-doped UNCD/a-C:H films and Si wafers.

Chapter 2

Related Literatures

2.1 Chapter overview

In this chapter, the author will explain the details of the principle and the brief descriptions of the related literature regarding the present thesis. In the beginning, the characteristics of UNCD will be manifested. Subsequently, the feature, construction, and energy band diagram of heterostructure diodes comprising B-doped UNCD/a-C:H films and Si substrates will be illuminated. Afterward, the operation principle of PLD technique will be delineated. Ultimately, the implication of the considerable diode parameters and equation for evaluating the parameters will be elucidated.

2.2 Feature of ultrananocrystalline Diamond

The film of ultranacrystalline diamond (UNCD), which possessed the diameter of crystalline size around 10 nm, is one kind of diamond films [1-4]. Nowadays, the film of UNCD has been appealing considerable attention for the research concerning diamond aspect due to the gripping characteristics compared with the diamond in single-crystalline or poly-crystalline [2]. The gripping particularities of UNCD can be delineated hereinafter: (i) the films of UNCD are uncomplicated for creation on many types of foreign substrate [1,10], (ii) surfaces of UNCD film are utterly smooth [1,5,10], (iii) these films own high hardness and modulus [], (iv) UNCD films have high stability in temperature [1,10], and (v) they have the unique characteristic of electrical and optical features owing to having a lot of grain boundaries [10,12].

In previous research, the absorption coefficient and the energy band gap for the films UNCD/a-C, which constructed in the surroundings of hydrogen gas by the usage of PLD, have been revealed by T. Yoshitake et. al. [1] They reported that the UNCD/a-C:H films owned a high coefficient absorption of the optical spectrum (approximately 1×10^{6} cm^{-1}) in the range of photon energy between 3 eV and 5 eV as manifested in Fig 2.1. The optical band gaps of the film were evaluated from the plot of the optical absorption spectra as illustrated in the inset of Fig 2.1, which the values of the direct and indirect band gap of the optical spectrum were 2.2 eV and 1.0 eV, respectively.

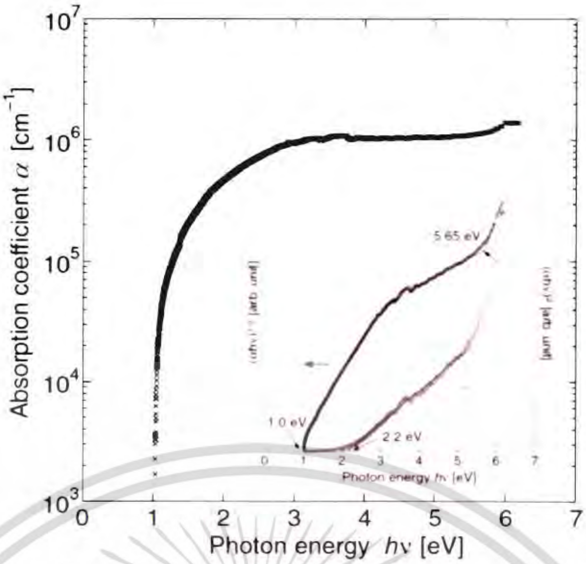


Figure 2.1 Relationship of the absorption coefficient and the photon energy for the film of UNCD/a-C:H. The inset illustration revealed the relation between $(\alpha h\upsilon)^{1/2}$ and $(\alpha h\upsilon)^2$ against the photon energy for evaluating the band gap [1].

Previously, S. Ohmagari et. al [21] have revealed about the discontinuities of the valence band (ΔE_{VB}) and conduction band (ΔE_{CB}) of the heterostructure photodiodes comprising B-doped UNCD/a-C:H films and Si wafers built by PLD. From the estimation, ΔE_{VB} was -0.03 eV and ΔE_{CB} was -0.15 eV, in the case of the energy band gap of Si and a-C:H were 1.12 eV and 1.0 EV, respectively. The small discontinuities of ΔE_{VB} and ΔE_{CB} are beneficial for the carrier diffusion and the collection of photogenerated carriers.

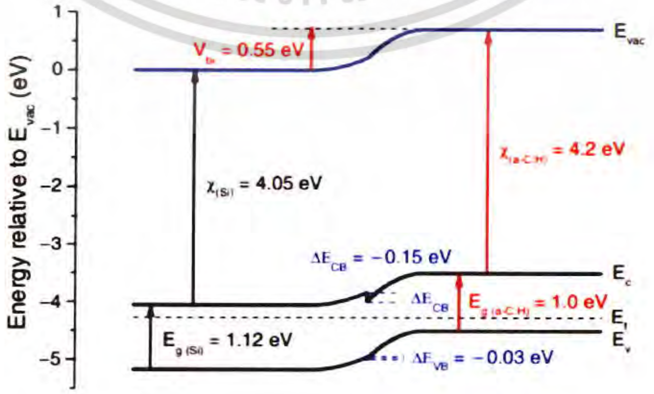


Figure 2.1 Energy band diagram of the heterostructure diodes comprising B-doped UNCD/a-C:H and Si built by PLD [21].

Additionally, T. Hanada et al. [22] have reported regarding the examination of the electrical characteristics of the heterostructure diodes comprising B-doped UNCD/a-C:H films and Si substrates produced through PLD. The rectifying action in the dark at different temperatures was confirmed by the experimental results. According to Fig. 2.3, the characteristics of *I-V* demonstrated a large leakage current at a temperature of 300 K, whereas the leakage current was reduced when the temperature was diminished. At a temperature of 60 K, the decrease of the leakage current was distinguished. This is likely owing to the reduction of the density of carrier in UNCD/a-C:H layer and Si layer when the temperature was reduced. Furthermore, UV light detection at various temperatures was observed. From the observation of UV detection in Fig 2.4, it revealed a minimal photocurrent at 300 K while the photocurrent was slightly increased when the temperature was decreased to be 60 K. The small increase of photocurrent was attributed to a spike in the band offset of the heterostructure diodes comprising B-doped UNCD/a-C:H films and Si substrates, which was higher at low temperatures.

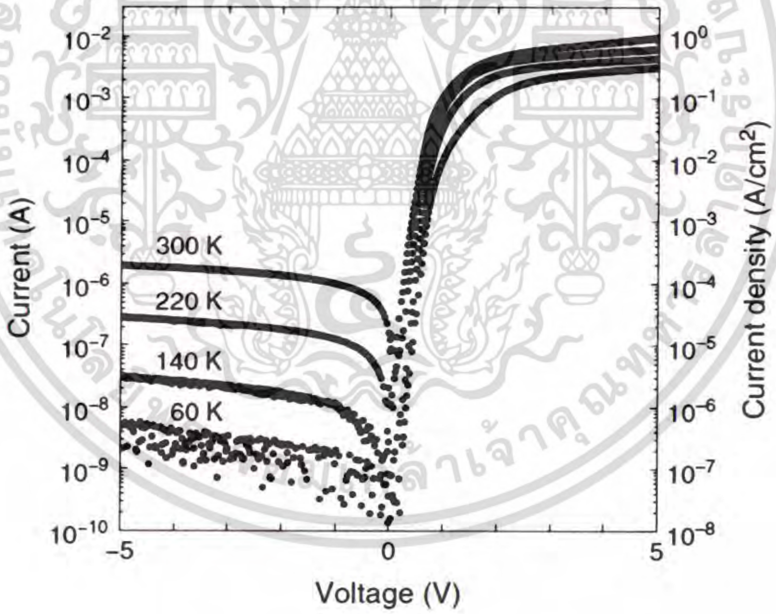


Figure 2.3 Relation between *I* versus *V* of the heterostructure diodes comprising B-doped UNCD/a-C:H films and Si substrates in the dark at several temperatures [22].

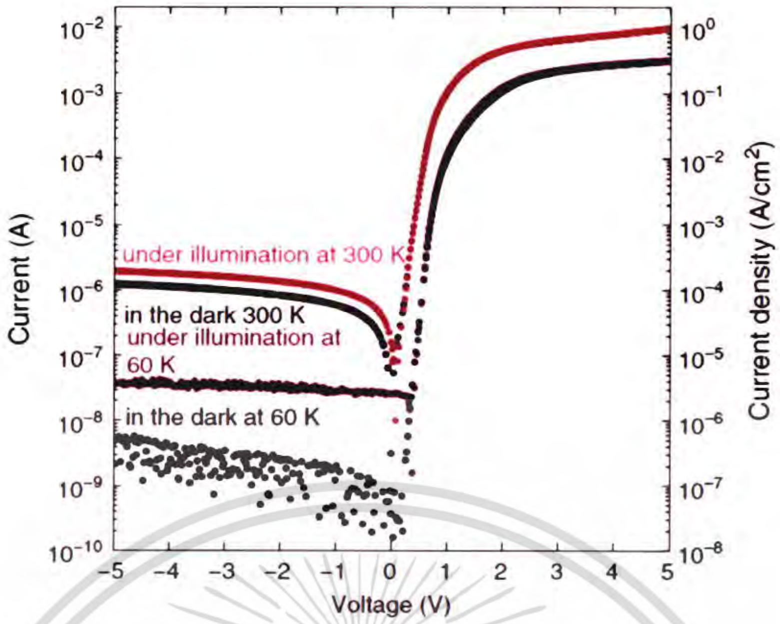


Figure 2.4 *I-V* characteristics measured in the dark and under illumination at 300 and 60 K for the heterostructure diodes comprising B-doped UNCD/a-C:H films and Si substrates [22].

2.3 Semiconductor [23]

A semiconductor is the material that hold an electrical conductivity value between a conductor and an insulator, which depends on the surrounding temperature, the concentration of doping atom or the incident light. Following its features, the semiconductor is proper for application in electronic and optoelectronic devices such as solar cells, p-n diodes including transistors. The semiconductor can be separated as intrinsic semiconductors and extrinsic semiconductors. An intrinsic semiconductor is semiconductor material without doping and nucleus of atom is surrounded by four valence electrons, which the carrier population of holes in the band of valence is equivalent to the electron populations in the band of conduction such as Silicon and Germanium. The structures of an atom of silicon and germanium are depicted in Fig. 2.2. Following its feature, the electric charge of the intrinsic semiconductor atom is unprejudiced. In the other hands, the extrinsic semiconductor is semiconductor material, which is comprised of elements more than two types. Types of extrinsic semiconductor can be divided as p-type and n-type semiconducting materials.

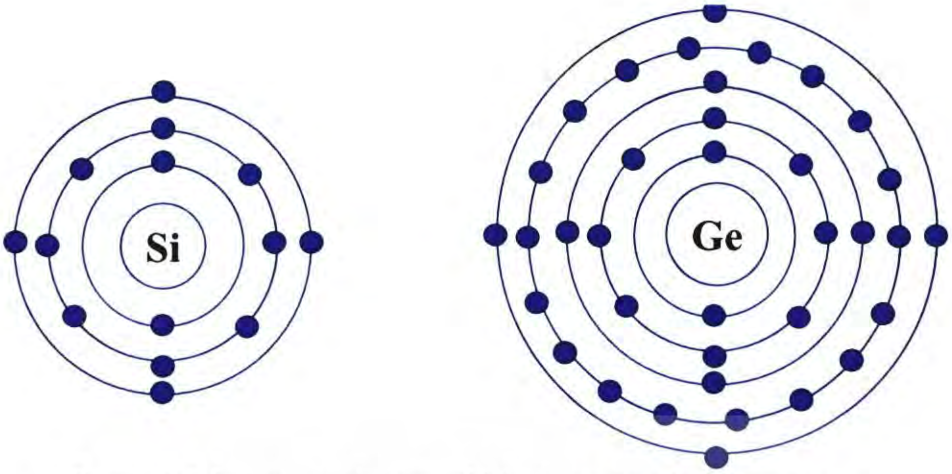
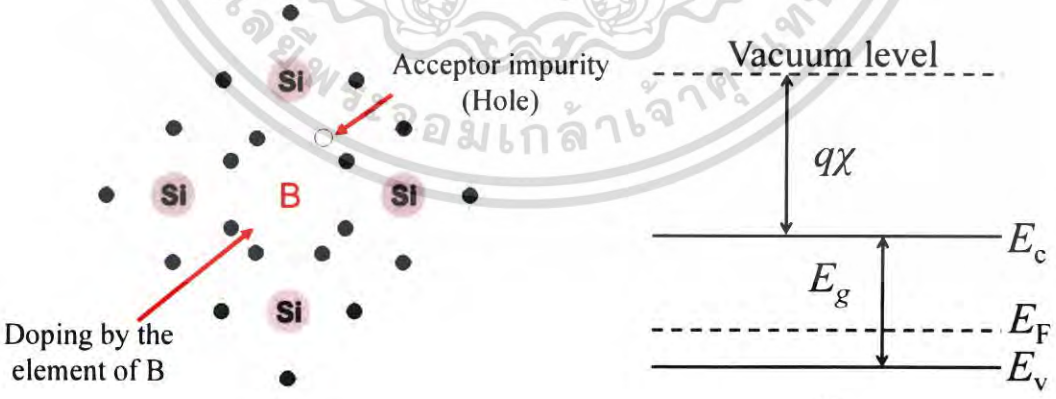


Figure 2.5 Structure of atom of (a) silicon and (b) germanium.

2.3.1 p-Type semiconducting material [23]

A p-type material is semiconductor that the atom in lattice of semiconductor is supplanted via an element with three valence electrons, which influence the change of the electron-hole equilibrium. The elements that have three valence electrons such as boron (B) and aluminum (Al). Replacement of element with three valence electrons in the semiconductor lattice is the cause of one excess hole as seen in Fig. 2.3. The excess holes are called the acceptor impurities because there will take the free electrons. The semiconductor of p-type possesses a larger number of the concentration of hole, which contribute to the positive charge. Besides, p-type semiconducting material has Fermi level less than Fermi level of intrinsic, which is nearly the valence band as demonstrated in Fig. 2.6 (b).

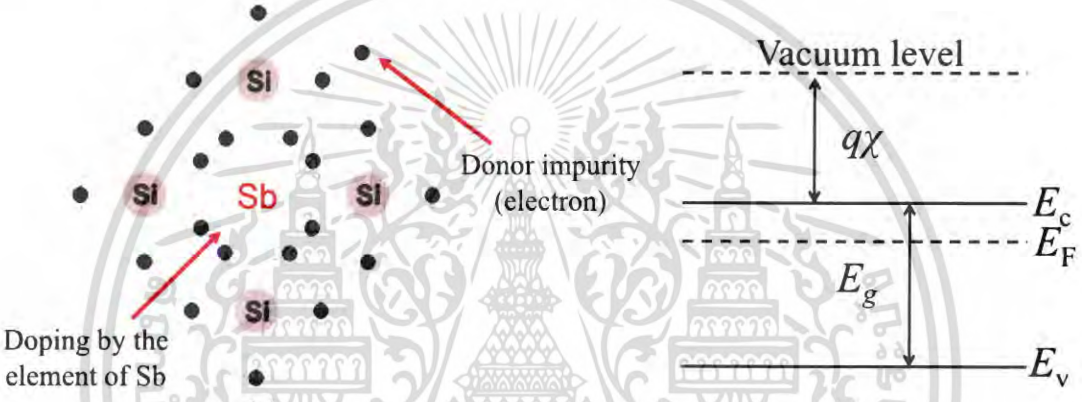


(a) (b)

Figure 2.6 (a) Structure of silicon added boron element to create p-type semiconducting material [24] and (b) band diagram of p-type semiconductor.

2.3.2 n-Type semiconducting material

In n-type semiconducting material, the semiconductor lattice of atom is substituted by an element with five valence electrons, such as nitrogen (N) and phosphorus (P). Substitution of the lattice atom by five valence electrons, while the lattice can only catch four electrons, contributes to occur one excess electron as shown in Fig. 2.4. The excess electron will donate an electron when there is driven by high energy in the heterojunctions. The excess electron is called donor impurity. Additionally, the semiconductor of n-type has a larger electron concentration, which conduces to a negative charge. n-Type semiconductor has higher Fermi level than purity semiconductor, which is about the conduction band.

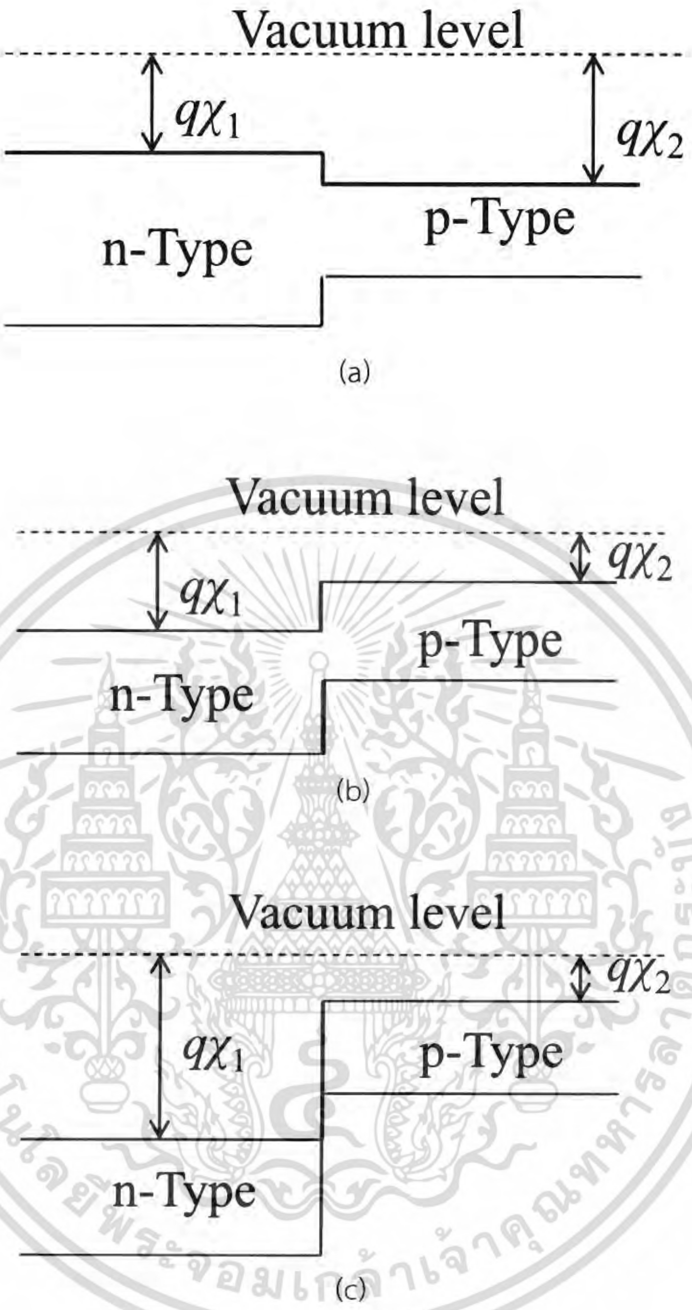


(a) (b)

Figure 2.7 (a) Structure of silicon added antimony element to produce n-type semiconducting material [25] and (b) band diagram of n-type semiconductor.

2.4 Heterostructure diode [23,26]

Commonly, a heterostructure diode is determined by the interface between two layers of different semiconductors. These different semiconductors have similar lattice constants, but the energy band gaps and different electron affinities are dissimilar as differed with a homojunction. Following these results, the band diagram of energy band gap for heterostructure diode is discontinuity and band bending is not smooth, when it compared with band bending of a homojunction. The heterostructure diodes can be divided as three types as demonstrated in Fig. 2.8. The vacuum level mentions to the energy of a free electron outside the semiconductor. The electron affinity (χ) refers to the energy that is requested for inducing an electron from the bottom of the conduction band toward the vacuum level.



(a)

(b)

(c)

Figure 2.8 Three types of heterostructure diodes following alignment of band gap comprising (a) Type 1 (Straddling), (b) Type 2 (Staggered gaps) and (c) Type 3 (Broken gaps) [23].

Following Anderson's rule (electron affinity rule), the band bending of the heterostructure diode of type 1, which qχ of different semiconductors are constant, the vacuum levels are continue and parallel with E_C and E_V including lattice constants of semiconductors are equal, can be illustrated as Fig. 2.9. As shown in Fig. 2.9, the conduction band and valance band are discontinued. Based on Anderson's rule, the band offset of the conduction band can be computed by using the following equation:

$$\Delta E_c = q\chi_2 - q\chi_1 \tag{2.1}$$

And the band offset of the valance band is given as

$$\Delta E_V = (Eg_1 - Eg_2) - \Delta E_C = \Delta E_g - \Delta E_C \tag{2.2}$$

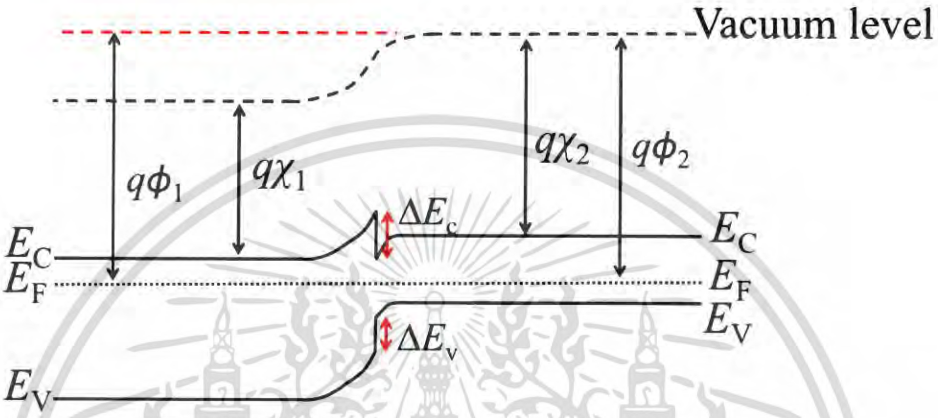


Figure 2.9 Band diagram of heterojunction diode (Type 1) at thermal equilibrium.

2.5 Thermionic emission (TE) theory [26-30]

Thermionic emission (TE) is emission of electrons since them temperature are high. The electrons in valence band are responsible for conducting the electric current. If the temperature is increased, the electrons in valence band will be driven to higher energy band. The temperature that induced the flow of electrons is called thermionic emission.

For consideration in the case of a diode, the peculiarity of *J-V* can be expressed as a single exponential via the model of equivalent circuit in Fig. 2.10. The current flow for a diode in arithmetic parts can be expressed via the following equation:

$$I = I_0\left(\exp\left(\frac{qV}{nkT}\right) - 1\right) \tag{2.3}$$

where, I, I_0, q, V, n, k, and T are the current, saturation current, charge of an electron, voltage across a diode, Boltzmann's constant and temperature, respectively.

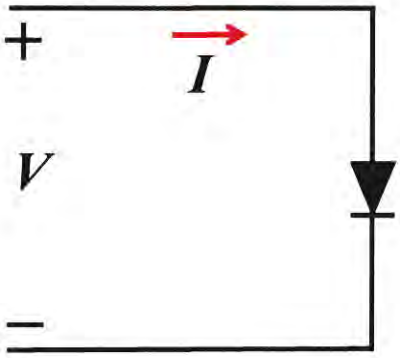


Figure 2.10 Model of an equivalent circuit comprising a diode.

By dividing the parameter of area (*A*) into both sides of Eq 2.3, the relationship of the current density (J_0) can be written as follows:

$$J = J_0\left(\exp\left(\frac{qV}{nkT}\right) - 1\right) \tag{2.4}$$

Here, J and J_0 are the current density and saturation current density, respectively.

By taking the natural logarithm into both sides of Eq. 2.4 and neglecting the term of -1 in Eq. 2.4 in the case of the assumption that $J >> J_0$. Therefore, Eq. 2.4 can be written as follows:

$$\ln(J) = \ln(J_0) + \frac{qV}{nkT} \tag{2.5}$$

Based on Eq. 2.5, if the value of V value is higher than $3kT/q$, the value of n can be evaluated through the slope of the linear part of ln$J$-V characteristic in the initial of forward bias according to the following equation:

$$n = \left(\frac{q}{kT}\right)\left(\frac{\mathrm{d}V}{\mathrm{d}(\ln J)}\right) = \left(\frac{q}{kT}\right)\left(\frac{1}{\text{slope}}\right) \tag{2.6}$$

The value of n, there can describe the behavior of flow mechanism of carrier within the junction of heterostructure diode.

According to Eq. (2.5), the value of J_0 can extract from the intercept of the straight line of ln$J$ - V plot at 0 V. The value of J_0 is utilized for estimation of the value of $\varnothing_b$ through the following relationship:

$$J_0 = A^* T^2 \exp\left(\frac{-q\phi_b}{kT}\right) \tag{2.7}$$

where A^* and ϕ_b are Richardson's constant and the value of barrier height, respectively.

2.6 Model of Cheung [29-31]

For Cheung model, consideration was executed in the case of the combination of a diode and a resistance, which the current throughs the equivalent circuit as shown in Fig. 2.11. The voltage (V_D) across the diode can be described as the total voltage, which dropped across a diode and a resistance. The relation of voltage can be written as: $V_D = V - IR_s$ in the case of V_D greater than $3kT/q$, Eq. 2.4 can be written as shown in the following relation:

$$J = J_0\left(\exp\left(\frac{q(V - JAR_s)}{nkT}\right) - 1\right) \tag{2.8}$$

Here, J, J_0, q, V, n, k, R_s, and T are the current, saturation current, charge of an electron, applied bias voltage, Boltzmann's constant, series resistance and temperature, respectively.

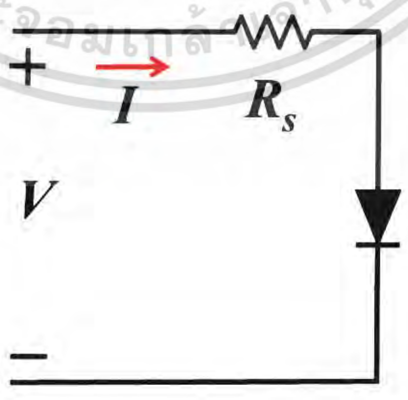


Figure 2.11 Model of an equivalent circuit comprising a diode and a resistance.

By taking the natural logarithm into Eq. 2.8 with neglecting minor effect in term of -1 in and under assumption that $J >> J_0$, the formula in Eq. 2.8 can be written as follows:

$$\ln\left(\frac{J}{J_0}\right) = \frac{q\left(V - JAR_s\right)}{nkT} \tag{2.9}$$

Following Eq. 2.9, it can be rearranged as expressed below:

$$V = JAR_s + \frac{nkT}{q}\ln\left(\frac{J}{J_0}\right) \tag{2.10}$$

According Eq. 2.10, when the term of J_0 is replaced by Eq. 2.7, it can be written as shown below:

$$V = JAR_s + \frac{nkT}{q}\left(\ln J - \ln\left(A^{*}T^{2}\exp\left(\frac{-q\phi_b}{kT}\right)\right)\right) \tag{2.11}$$

Based on Eq. 2.11, it can be rearranged as indicated below:

$$V = JAR_s + n\phi_b + \frac{nkT}{q}\ln\left(\frac{J}{A^{*}T^{2}}\right) \tag{2.12}$$

Based on Eq 2.12, the existence of n and R_s can be estimated by pointing to term of J. The equation can be expressed as a given formula:

$$\frac{\mathrm{d}V}{\mathrm{d}\left(\ln J\right)} = AJR_s + \frac{nkT}{q} \tag{2.13}$$

According to a relation between $\mathrm{d}V/\mathrm{d}(\ln J)$ and J, a term of AR_s and nkT/q can be obtained from a slope and an intersection of y-axis, respectively. Additionally, the function of $H(J)$ was utilized in order to assess R_s and ϕ_b. By determination the function of $H(J)$ into Eq. 2.12, therefore, the function of $H(J)$ can be written as follows:

$$H\left(J\right) = V - \left(\frac{nkT}{q}\right)\ln\left(\frac{J}{T^{2}A^{*}}\right) \tag{2.14}$$

where term of *H*(*J*) was determined as follows:

$$H(J) = JAR_s + n\phi_b \tag{2.15}$$

Here, *V*, *J*, R_s, *n*, *k*, *T*, *q*, *A* and *A** are the bias voltage, current density, series resistance, ideality factor, Boltzmann's constant, temperature, electron charge, junction area and Richardson's constant, respectively. Furthermore, the value of *n* in Eq. 2.5 is obtained from the estimated value of *n* via Eq. 2.4.

2.7 Norde's Function [29,30,32-35]

Based on the equation of ideal Schottky diode, if the existence of a series resistance to diode displays in the base material, the linear line from plotting of ln*I*-*V* will be governed by the bias voltage in range of $kT/q \ll V \ll IR$. If the series resistance is high, the range of bias voltage for giving a reliable value of I_0 will be very minute. Additionally, on conventional equation, it confines us for selecting the range of bias voltage at the minimal value of *V*. This results in that the recombination mechanism in the heterostructure diode should be a vital part of the entire current, leading to the value of I_0 value low authentic. For consideration in case of a diode with a series resistance, the problem with a series resistance was eluded by the usage of relationship developed by Norde and others as indicated in the following equation □:

$$F(V) = \frac{V}{\gamma} - \left(\frac{kT}{q}\right)\ln\left(\frac{J}{T^2 A^*}\right) \tag{2.16}$$

where *V*, *k*, *T*, *q*, *J*, *A** and γ are the bias voltage, Boltzmann's constant, temperature, charge of electron, current density, Richardson's constant and first integer high than the value of *n*, which *n* acquired from TE theory, respectively.

The value of ϕ_b and R_s value can be estimated though the minimum point of the *F(V)*-*V* plot. The equation for calculating the value of ϕ_b is expressed following the relation as follows:

$$\phi_b = F(V_0) + \frac{V_0}{\gamma} - \frac{kT}{q} \tag{2.17}$$

where $F(V_0)$ and V_0 are the minimum point of $F(V)$ and the voltage, which corresponded the value of $F(V)$ at minimum point, respectively. The formula for the estimation of R_s is explained as follows:

$$R_s = \frac{kT}{qAJ_{min}}(\gamma - n) \tag{2.18}$$

Here, J_{min} is the current density, which corresponded the minimum point of $F(V)$.

Recently, P. Sittimart et. al [30] have reported regarding calculating diode parameters of n-Type β-FeSi2/ p-Type Si heterostructure diodes by at different temperature. The heterostructure diodes were confirmed the rectifying action at different temperatures. From *I-V* measurement, the diode parameters were examined based on TE theory, Cheung approach and Norde model. By the calculation from TE theory, the value of *n* was increased with decreasing temperature, whereas the value of ϕ_b was reduced by the decrease of temperature. Both *n* and ϕ_b estimated via TE theory accorded with those evaluated by Cheung's and Norde's approaches. At low temperature, the n-Type β-FeSi2/ p-Type Si heterostructure diodes owned a large *n*. This behavior should be attributable to the presence inhomogeneity and tunneling. Via Cheung and Norde approaches, the computed R_s values were raised when the temperatures were diminished. The increase of R_s value at low temperatures might be likely due to the increase of *n* at low temperatures.

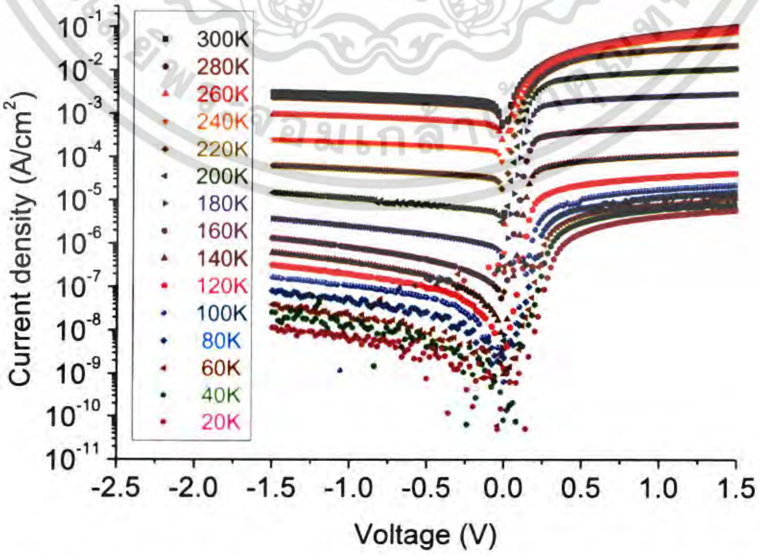


Figure 2.12 *I-V* curve at low temperatures of n-Type β-FeSi$_2$/ p-Type Si heterostructure diodes [30].

2.8 Impedance spectroscopy [18-20,36,37]

Impedance spectroscopy is a major measurement for the investigation of the electrical properties of materials and devices such as solar cell and heterojunction diodes. The investigation of impedance spectroscopy can be executed though the measurement of the response of device with applying AC signal. On the basis of an ideal resistance with a resistance, the current flow through the resistor and voltage across of the resistor following relation following Ohm's rule can be described by the following equation:

$$V = IR \tag{2.19}$$

where V, I and R are the voltage across the resistor, current and resistance, respectively.

Nevertheless, the concept of impedance is complicated than common concept of the resistance because of the complexity that is attributable to regarding phase difference. The impedance $Z(\omega,t)$ of the system can be calculated by the following relation:

$$Z(\omega) = \frac{V(\omega,t)}{I(\omega,t)} \tag{2.20}$$

where $V(\omega,t)$ is a minimal amplitude of voltage that is biased in the range of frequency ($f = \omega/2\pi$) and $I(\omega,t)$ is the corresponding current $I(\omega,t)$.

In the term of complex number, a minimal amplitude of voltage can be expressed by the following function:

$$V(\omega,t) = V_0 \exp(j\omega t) \tag{2.21}$$

and the corresponding AC current is given by as follows:

$$I(\omega,t) = I_0 \exp(j\omega t - j\theta) \tag{2.22}$$

where $\boldsymbol{\theta}$ is denoted that is the different phase of $V(\omega,t)$ and $I(\omega,t)$, besides j is $(-1)^{1/2}$. When Eq. (2.21) is substituted by (2.22) and (2.23), it can be described as follows:

$$Z(j\omega)=\frac{V_0}{I_0}\exp(j\theta)=Z_0\exp(j\theta) \tag{2.23}$$

By utilization of relative of Euler and substitution of Z_0 by $|Z|$, Eq. 2.24 can be written as follows:

$$Z(j\omega)=|Z|(j\sin\theta+\cos\theta) \tag{2.24}$$

Commonly, the function of impedance can be explained by the following relation:

$$Z=Z'-\mathrm{j}Z'' \tag{2.25}$$

where Z' is term of real part of impedance when $Z'=|Z|\cos\theta$ and Z'' is term of imaginary part of impedance when $Z''=j|Z|\sin\theta$. Via the impedance spectroscopy, we can extract the real part (Z') and imaginary part (Z'') of complex impedance.

In the case of the impedance for a resistor, the voltage across the resistance is $V(\omega,t)=V_0\sin(\omega t)$ and the current flow is $I(\omega,t)=I_0\sin(\omega t)$, it can be explained by given equation:

$$Z_R(\omega)=\frac{V(\omega,t)}{I(\omega,t)}=R \tag{2.26}$$

For the impedance of a constant phase element (CPE), it can be explained in term of frequency based on the impedance for capacitor by given equation:

$$Z_{\mathrm{CPE}}(\omega)=\frac{1}{(j\omega)^a\,\mathrm{CPE}} \tag{2.27}$$

2.8.1 Impedance for equivalent circuit comprising R_s, R_p and CPE [18-20,36,37]

Fig. 2.12 presents the equivalent circuit comprising R_p and CPE in parallel combined with the series resistance (R_s) on the basis of the simple circuit of Randle. The electrical impedance corresponding to Randle model with CPE can be expressed though the following relation:

$$Z(\omega) = R_s + \frac{R_p}{1 + R_p (j\omega)^a \mathrm{CPE}} \tag{2.28}$$

where ω displays angular frequency, CPE is the magnitude of constant phase element and a is a deviation of the magnitude of CPE from the ideal dependent capacitor in ranging from 0 to 1. If a is equal to 1, CPE can be considered an ideal capacitor.

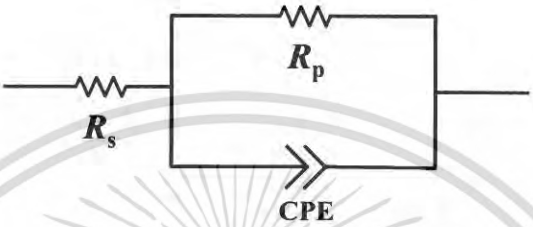


Figure 2.13 Model of an equivalent circuit comprising R_p and CPE in parallel combined with R_s.

Recently, B. Arredondo et. al [48] have reported about the impedance spectra of photovoltaic cell at different voltages in the dark. Z''-Z' characteristics displayed a semicircle for each voltage, as revealed in Fig. 2.13, which the center of semicircle was depressed. It indicated that the circuit model for this photovoltaic cell is appropriate for the combination of R_p and CPE in parallel combined with the series resistance (R_s). For CPE together with a value in the range of 0.9 – 1.0, CPE can be considered in term of the capacitance value (C).

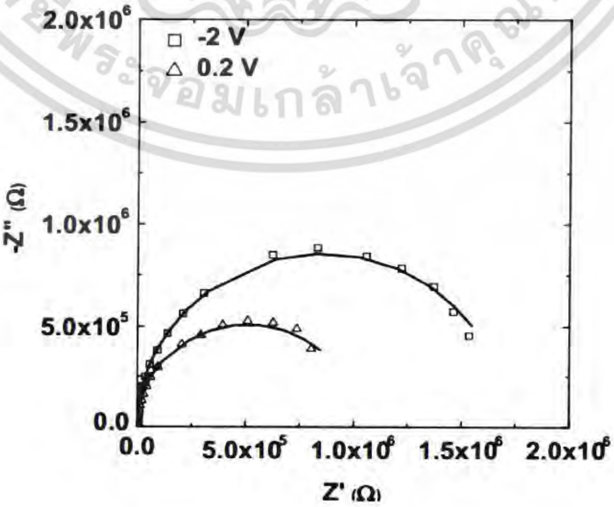


Figure 2.14 Characteristics of Z''-Z' in the dark at different V values of circuit model consisting of with R_p and CPE in parallel combined with R_s.

2.9 Diode and circuit parameters

2.9.1 Ideality factor (n) [39-42]

The parameter of n can indicate the possible of mechanism for carrier transportation across a junction. The denotation of n values can be described by three transportation mechanisms such as diffusion, generation-recombination, and tunneling. If the value of n is equal to one, the transportation mechanism of the carrier across the junction is particularly governed from the process of a thermal diffusion. If the value of n is higher than one and nearly two, generation-recombination will be the remarkable transportation mechanism that control the flow of carrier within the junction. In addition, if n value is higher than two, the process of tunneling will notably dominate the transportation mechanism of the carrier.

2.9.2 Barrier height (ϕ_b) [39-41]

Based on metal-semiconductor device, ϕ_b at steady state relies on the association of the metal and semiconductor. ϕ_b is a barrier of the potential energy for charges induced at a heterojunction. The barriers, which own the characteristics of rectifying action, are proper for application in the heterojunction diodes.

2.9.3 Series resistance (R_s) [39-42]

Generally, the considerable parameter of the heterostructure diode, which influence the electrical properties of diodes. R_s is the current-limiting factor, which the lowest possible value of R_s should be preserved in the junctions. R_s can occur from the different causes such as the contact occurring from the layer of film, the electrodes and the probes or the resistance of the neutral bulk in semiconductor and non-homogenous of film due to doping.

2.9.4 Interface state density (N_{ss}) [43]

On the basis of metal-semiconductor device, the interface states are atomic dimensions that arranged between the junction interface of the metal and semiconductor. The interface states can build the interacting quantum dipoles at the junction interface, which generate a broad electric field at the junction and can modify a vital amount of potential in interval of atomic distance. In the case of the heterostructure diodes, the interface states within junction behave as the recombination centers and raise the leakage currents [41]. Consequently, the density of Interface state should be minimal as possible. Figure 2.14 depicts the presence of interface state in the heterostructure diodes.

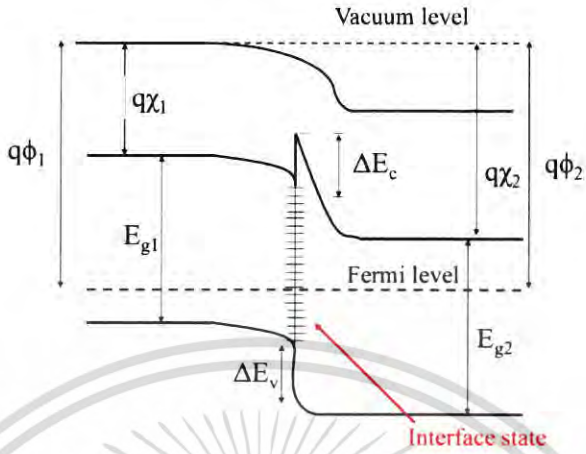


Figure 2.15 The presence of interface state at the junction interface for heterostructure diode.

2.9.5 Parallel resistance (R_p) [18-20,41]

R_p is associated with the interface charge transport process, defined by the charge transfer resistance. R_p can occur from the different causes the transportation of charge across the heterogeneous between the layers of interface, which might be dependent on surface roughness.

2.9.6 Constant Phase element (CPE) [18-20,41]

CPE conveys the non-ideality, including an adjustable parameter in order to recompense for non-homogeneity in the blocking interfaces because of the surface states, surface roughness, defects or grain boundaries. Ordinarily, the deviation of CPE from the ideal dependent capacitor can be describe by the value of a, which is in ranging from -1 to 1. For $a = 1$, CPE can be deemed a capacitance, while $a = 0$, it is a reciprocal of resistance (R^{-1}). If a is equal to -1, the value of CPE means an inductance. In the case of the experimental results from fitting, CPE can be approximated to a capacitance when the value of a is in the range of 0.9 – 1.

Chapter 3

Experimental details

3.1 Chapter overview

The construction of heterostructure diodes comprising B-doped UNCD/a-C:H films and Si wafers though PLD technique will be firstly delineated in this chapter. Afterward, the measurements of the physical and electrical characteristics of the heterostructure diodes comprising B-doped UNCD/a-C:H films and Si wafers will be described. Ultimately, the approaches for estimating the considerable diode parameters will be indicated.

3.2 Production of the heterostructure diodes comprising B-doped UNCD/a-C:H films and Si wafers

3.2.1 Construction of layer of B-doped UNCD/a-C:H

The construction of B-doped UNCD/a-C:H film with a film thickness of 230 nm was performed on Si wafer by the employment of PLD apparatus, which was manifested in Fig. 3.1. The target, which employed for producing the film, was graphite comprising 0.1 at.% of boron element. The source of irradiation for PLD apparatus was an ArF excimer laser, which its wavelength was 193 nm. The schematic illustration of PLD system was displayed in Fig 3.2.

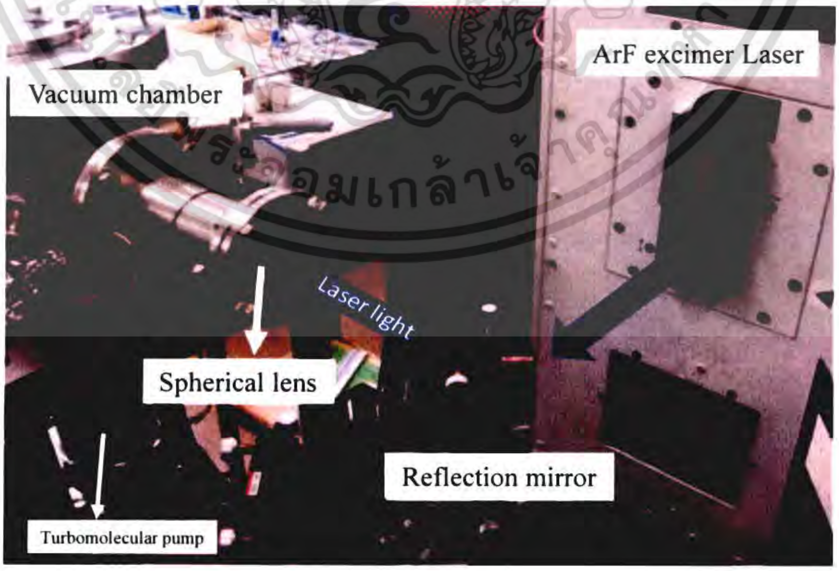


Figure 3.1 PLD system at Yoshitake Sensei's laboratory.

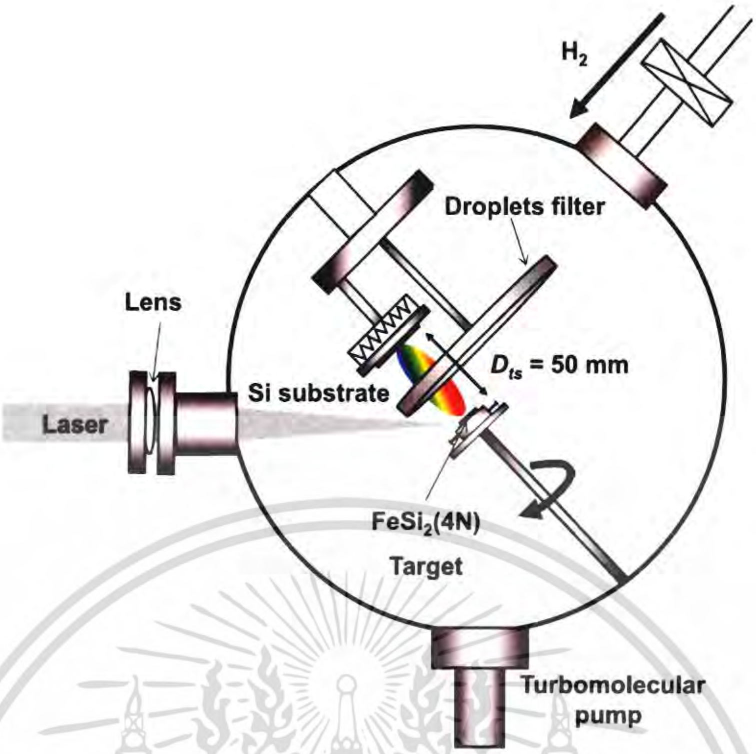


Figure 3.2 Illustration of the schematic of a PLD system.

Prior to the building procedure of the film, the surface of Si wafer substrate was cleaned to eradicate the dust, oils including residues by the solvents. Firstly, the Si wafer was rinsed with acetone solvent. Afterward, to eliminate the acetone, the methanol was utilized. In the next step, the deionized water was used for removing the methanol. For each step, the period for cleaning was performed for 5 minutes in an ultrasonic cleaner. Next step, the Si wafer substrate was dipped in a solution of hydrofluoric acid to eradicate the native oxide on the surface layer. Ultimately, by flowing nitrogen gas, the Si wafer was dried.

After the cleaning process, the Si wafer substrate was mounted on a substrate holder inside of the PLD chamber as shown in Fig 3.3. The substrate holder was spaced from the target at 15 mm. After that, the base pressure inside the chamber was evacuated to 7.5 × 10^{-6} Torr via a turbomolecular pump and a rotary pump. Next, the temperature of the substrate was heated to 550 °C and sustained until the finish of film production. During the process of building the film, the gas of H2 was fed into the chamber at a flow rate of 5 sccm and the pressure inside the chamber was kept at 0.4 Torr. The ArF excimer laser was energized with 100 mJ, and the focus point of the laser beam was indicated on a target, which can be rotated. For the pulse of the laser, the frequency of repletion was 50 Hz. For building the film, the conditions were performed following Table. 3.1.

Table 3.1 Condition for depositing the B-doped UNCD/a-C:H layer.

Process	Condition
Target	Graphite target with 0.1 at% of B
Source	ArF excimer laser
Substrate	n-type Si(100)
Substrate resistivity	1-5 Ω cm
Substrate temperature	550 °C
Substrate thickness	260 μm
Space between holder and target	15 mm
Base pressure	around 7.5×10^{-6} Torr
Flow speed of H_2 gas	5 sccm
Operating pressure	0.4 Torr
Energy of laser pulses	100 mJ
Repletion frequency of laser pulses	50 Hz
Film thickness	230 nm

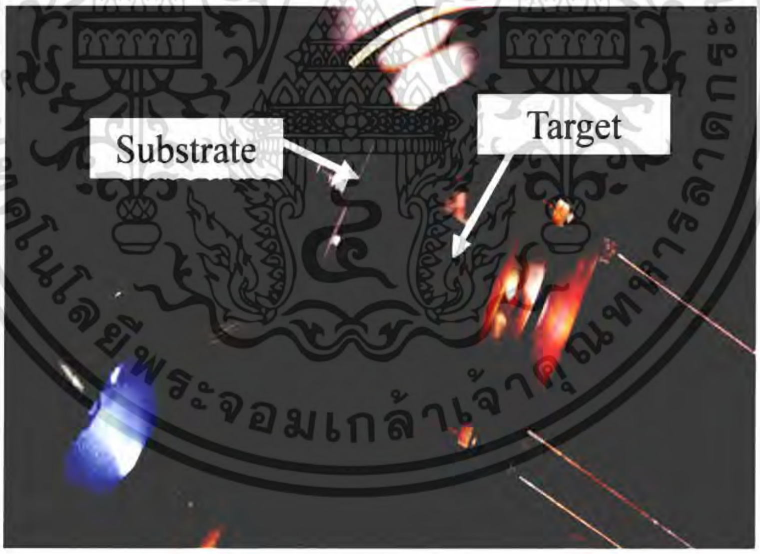


Figure 3.3 Instrument inside the system of PLD.

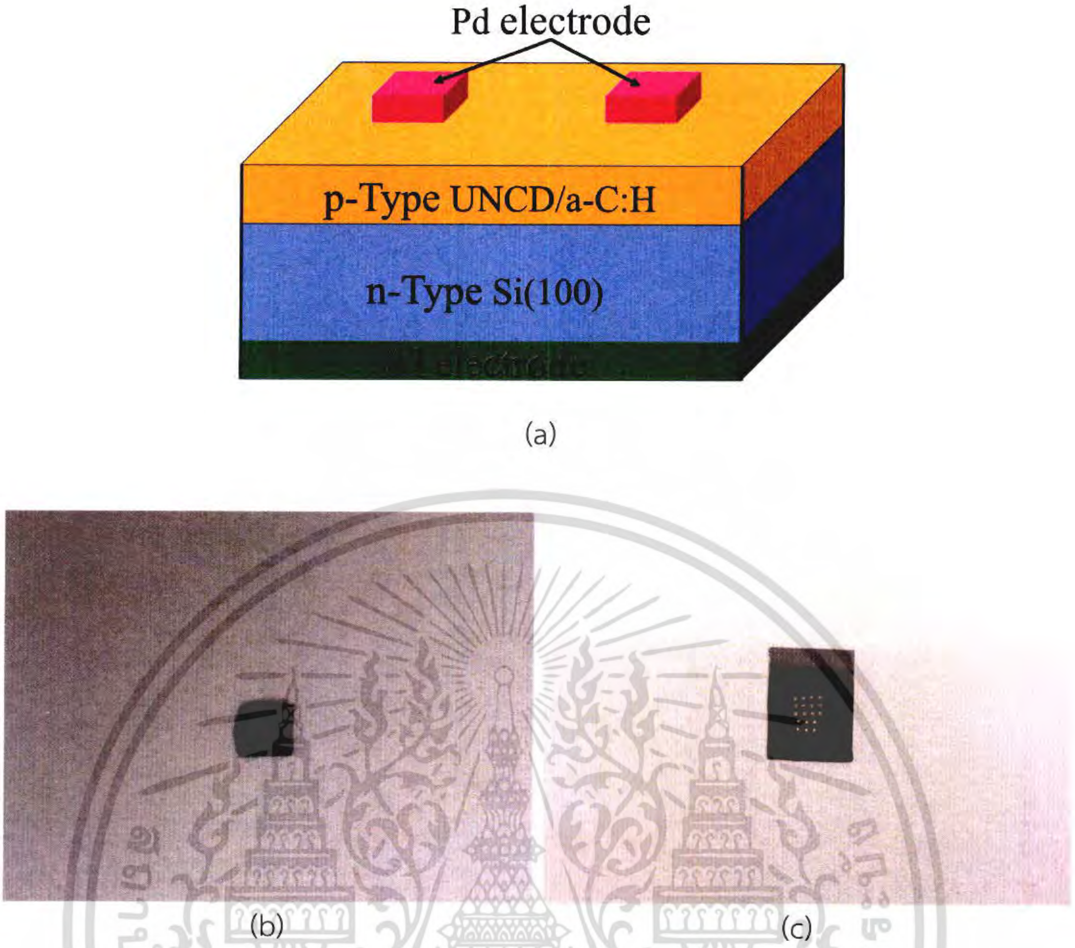
3.2.2 Construction of aluminum (Al) and palladium (Pd) electrodes

The electrodes of Al and Pd were constructed by radio frequency magnetron sputtering (RFMS) deposition as depicted in Fig 3.4. After the production of B-doped UNCD/a-C:H film, the electrode of Al was formed on the entire surface of Si substrate by using Al target with a purity of 4N. By the employment of Pd target with a purity of 4N, the Pd electrode was built on the surface of the constructed film. The production of both Al and Pd electrodes was executed according to the condition in Table 3.2. The images of the schematic diagram and samples of the constructed heterostructure diodes comprising B-doped UNCD/a-C:H films and Si substrates were shown in Fig. 3.5(a) (b) and (c), respectively.

Figure 3.4 RFMS system to construct the electrodes.

Table 3.2 Condition for fabricating the electrodes of Al and Pd.

Electrode material	Al	Pd
Sputtering target	Al (purity: 4N)	Pd (purity: 4N)
Base pressure	1×10^{-5} Pa	1×10^{-5} Pa
Substrate temperature	Room temperature	Room temperature
Operating pressure	2.66×10^{-1} Pa	1.33×10^{-1} Pa
Ar gas	10 sccm	10 sccm
Power for sputtering	200 W	200 W
Deposition rate	4.2 nm/min	8.3 nm/min
Film thickness	500 nm	500 nm



(a)

(b) (c)

Figure 3.5 (a) Illustration of the schematic diagram, as well as the image of the built heterostructure diodes comprising B-doped UNCD/a-C:H films and Si wafers with an electrode area of (b) 0.04 mm^2 and (c) 0.008 mm^2.

3.3 Investigation of the constructed B-doped UNCD/a-C:H films

The constructed film of B-doped UNCD/a-C:H will be examined to observe the characteristics of the film. Firstly, the feature of the film surface was monitored by the employment of a Field emission scanning electron microscope (FESEM) with a model of Carl Zeiss Auriga. Fig. 3.6 presented the equipment of a Carl Zeiss Auriga FESEM at Suranaree University of Technology. After that, the thickness of B-doped UNCD/a-C:H layer was explored utilizing a Hitachi S-4700 SEM at Thai Microelectronics Center, which was depicted in Fig. 3.7. Finally, the film roughness was inspected through the measurement of Atomic Force Microscope (AFM) with Park Systems XE-120 at Suranaree University of Technology. AFM apparatus was shown in Fig 3.8.

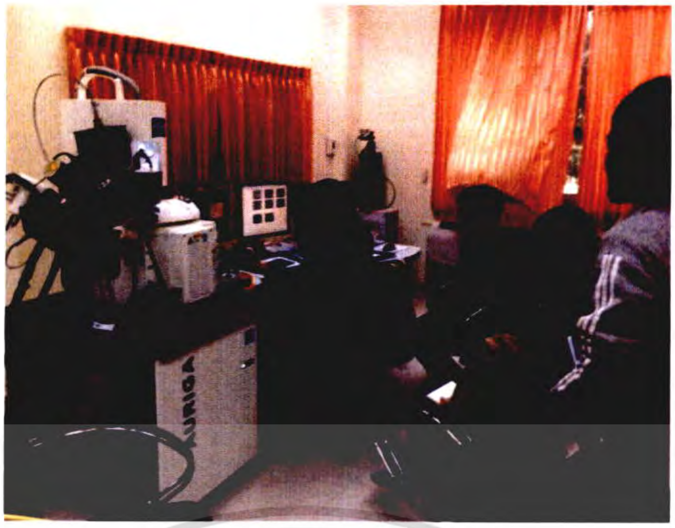


Figure 3.6 FESEM (Carl Zeiss Auriga) for surface investigation.

Figure 3.7 Hitashi S-4700 SEM at Thai Microelectronics Center.

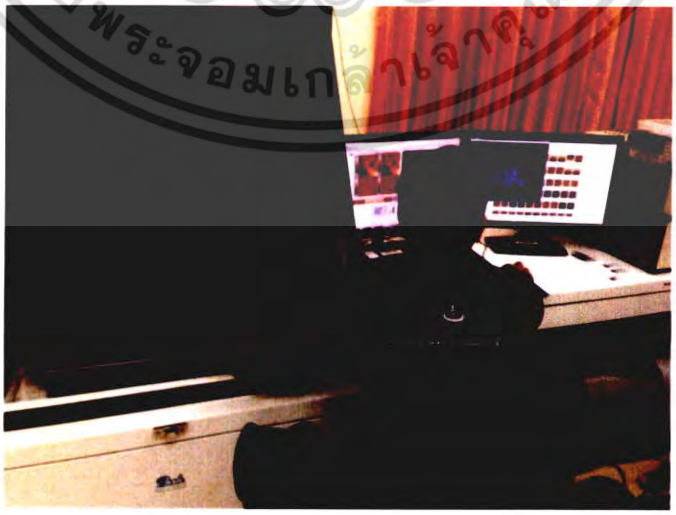


Figure 3.8 AFM with Park system (XE-120 model).

3.4 Examining *I-V* characteristics of the heterostructure diodes comprising B-doped UNCD/a-C:H films and Si wafers

The measurement of *I-V* was executed under various temperatures in the range between 60 K and 300 K in the dark. A source meter for monitoring the peculiarity of *I-V* was Keithley 2400 as presented in Fig. 3.9.

Figure 3.9 A source meter for Keithley 2400 model.

Step for measurement of *I-V* at different temperatures

1. Turn on the water chiller and wait until the temperature of the water were below 10 °C. The image of water chiller was depicted in Fig. 3.10.

Figure 3.10 Water chiller.

2. During reducing the temperature, we set a sample into the cryostat chamber. To set the sample, we used the screwdriver to remove the nuts from the black cover of the sample holder. The cryostat chamber together with a sample holder was demonstrated in Fig. 3.11.

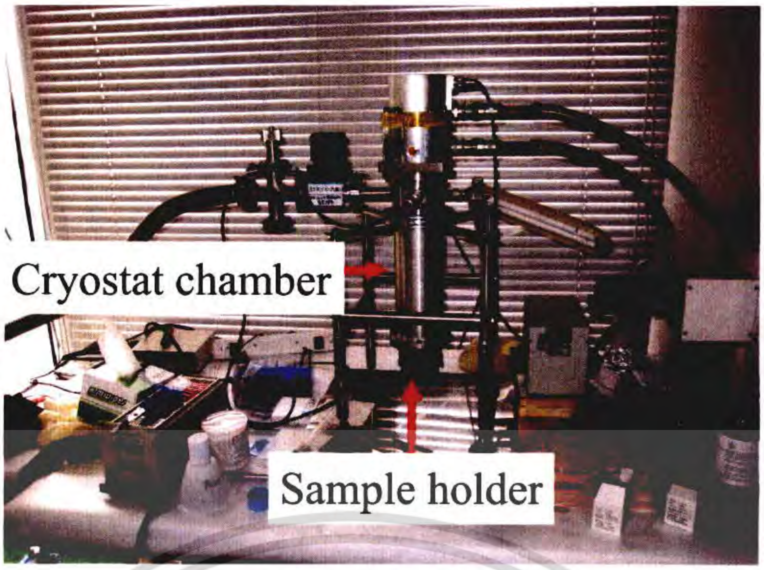


Figure 3.11 Images of cryostat chamber together with a sample holder.

3. The silver paste was used to mount the gold wires with the front and back of electrodes to contact the front and back of electrodes of the heterostructure diodes comprising B-doped UNCD/a-C:H films and Si wafers. The silver paste was liquefied by isopropyl alcohol. Then, we mounted the gold wire and Al electrode (Backside) by silver paste solder. After silver paste solder dried, we mounted the gold wire and Pd electrode (front side). After silver paste solder at the side of Pd electrode dried, we locked sample by using sample holder. Finally, we locked the cover of the sample holder by the nuts. The wires are connected to a source meter (Keithley 2400). Fig. 3.12 exhibited both of gold wires inside the sample holder of cryostat chamber.

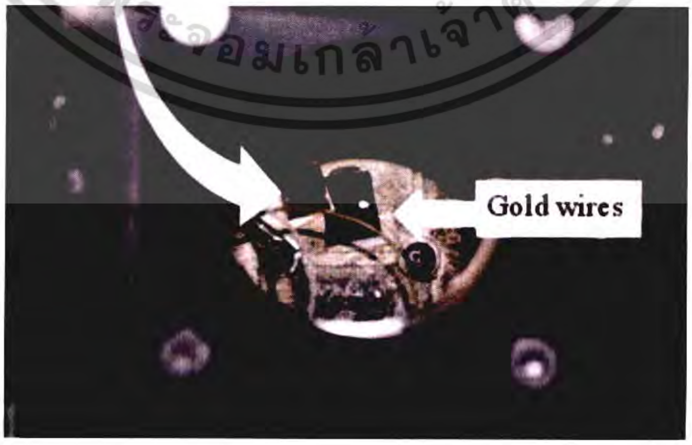
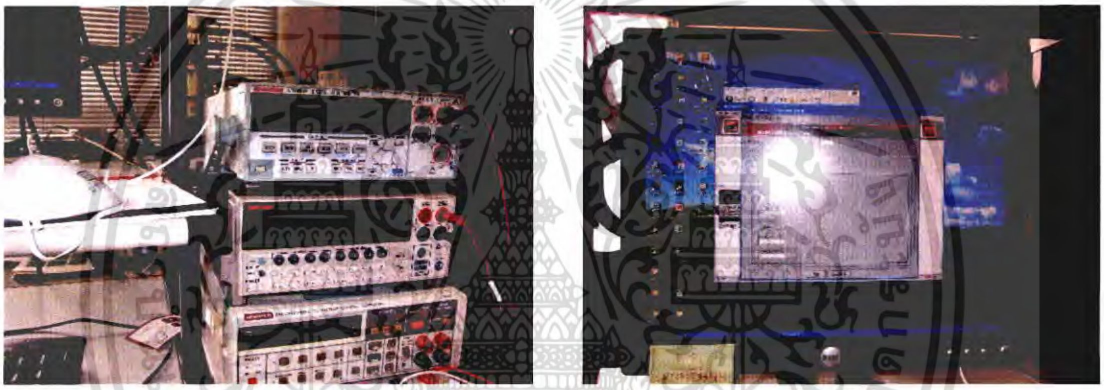


Figure 3.12 Both gold wires inside the sampler holder.

4. To evacuate the inside of cryostat chamber, we switched on the rotary pump and open gate value, respectively. The time for evacuating the pressure to vacuum is around 30 minutes.
5. After that, we turned on the computer, which connected to a source meter (Keithley 2400) as manifested in Fig. 3.13 (a), and open Lab test software for measuring *I-V* as depicted in Fig. 3.13 (b). In this software, we can set the variables for the measurement such as a range for applying the bias voltage, step for *I-V* measurement and measurement time. If we would like to measure *I-V* at 300 K, we can perform by selecting the command of "RUN". After finishing the measurement, the graph of measured *I-V* was shown on the display of this software. Then, the data of measurement was saved as text. file.



(a) (b)

Figure 3.13 (a) A source meter connected with a computer, and (b) the program for setting the variables for measurement of *I-V* curve.

6. For the measurement of *I-V* at different temperatures, we can perform by reducing the temperature inside the cryostat chamber. For reducing the temperature, the cryogenic machine was turned on by pushing the green-light button at the upper right corner of a cryogenic machine as presented in Fig. 3.14, and we used the temperature controller to set and control the temperature inside the cryostat chamber.

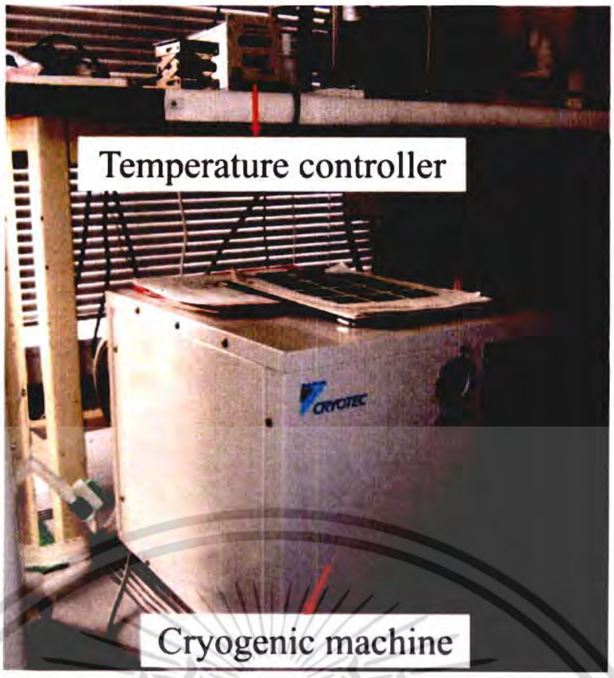


Figure 3.14 A temperature controller with the cryogenic machine.

7. To monitor *I-V* characteristic at 280 K, we turn on the cryogenic machine and set the temperature at 280 K. When the temperature controller displayed the temperature of 280 K, we can monitor the characteristic of *I-V* by using software "Lab test". We can perform to measure by selecting the command of "RUN". After finishing the measurement, the graph of measured *I-V* was shown on the display of this software. Then, the data of measurement was saved as text. file.
8. To monitor *I-V* characteristic for lower temperatures, we perform by repeating the step of 5.

3.5 Measurement of *Z"-Z'* characteristics of the heterostructure diodes comprising B-doped UNCD/a-C:H films and Si wafers

The impedance spectroscopy was performed to obtain *Z'* and *Z"* at different voltages in the range of 0 V - 2 V. Fig. 3.15 shows LCR meter (Agilent E4980A) for the measurement of *Z'-Z"*.

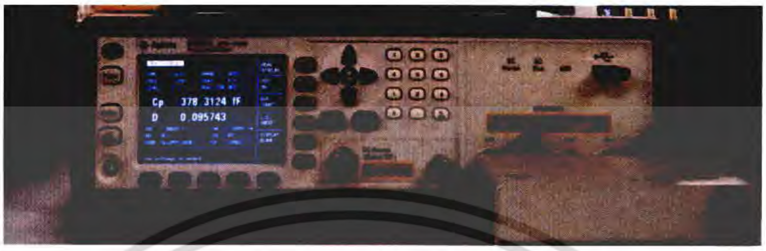


Figure 3.15 LCR meter (Agilent E4980A) at Yoshitake Sensei's laboratory.

For measuring the characteristics of *Z"-Z'*, *I-V* measurement should be firstly performed to verify the rectification characteristic of the diode. Fig. 3.16 illustrated the equipment for measuring the impedance and *I-V* characteristic, which was comprised of the computer, a temperature controller, a Keithley 2400 source meter, an Agilent E4980A LCR meter, an uninterruptible power supply and a cabinet with cover for opening and closing. For the experiment in the condition of the dark, the cover of the cabinet was closed to prevent the noise of the surrounding light.

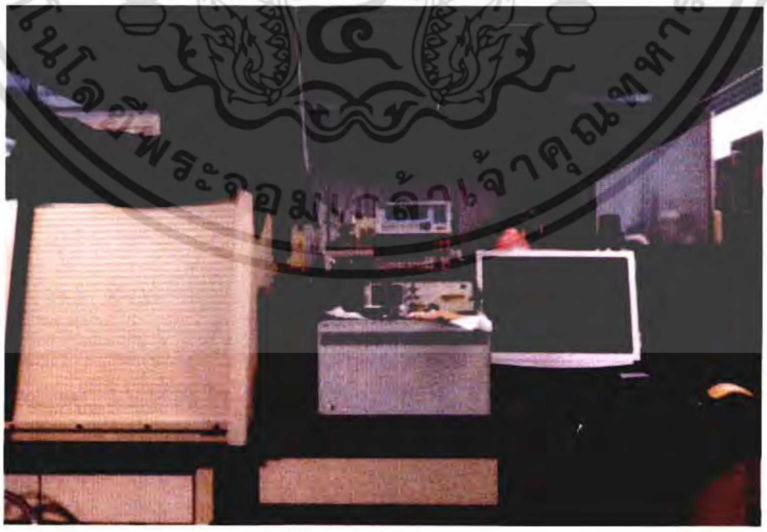


Figure 3.16 Equipment for measuring the impedance characteristic.

Step for measuring *Z"-Z'* curve under various voltages

1. Set up the sample into the chamber. Firstly, the chamber cover was uncovered to insert the sample into the inside of the chamber. Then, the sample was placed on the copper electrode inside the chamber. After that, the probes were adjusted to contact on a sample electrode and copper electrode. Fig. 3.17 revealed setting the sample inside the chamber for measuring the *Z"-Z'* characteristic.

Figure 3.17 Chamber for measuring *Z"-Z'*.

2. After arranging the sample, an LCR meter (Agilent E4980A) was switched on by pushing the button of "Power switch". Subsequently, USB flash drive was inserted into the USB port. The illustration and the image of Agilent E4980A control panel were revealed in Fig. 3.18.

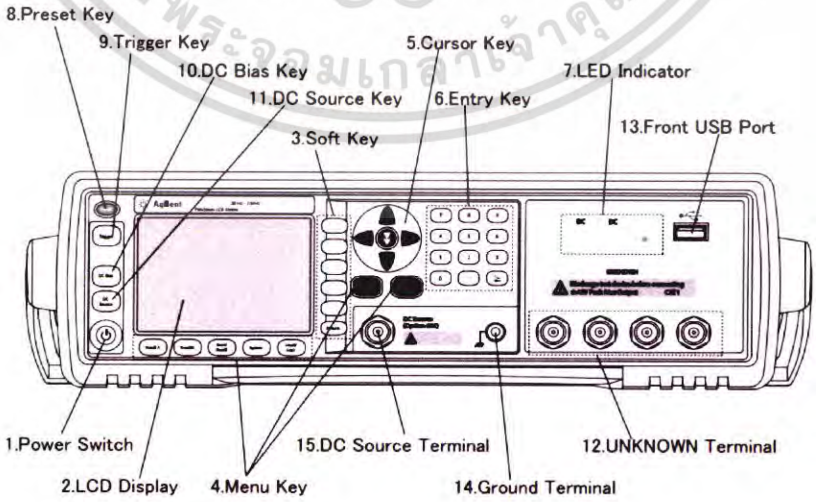
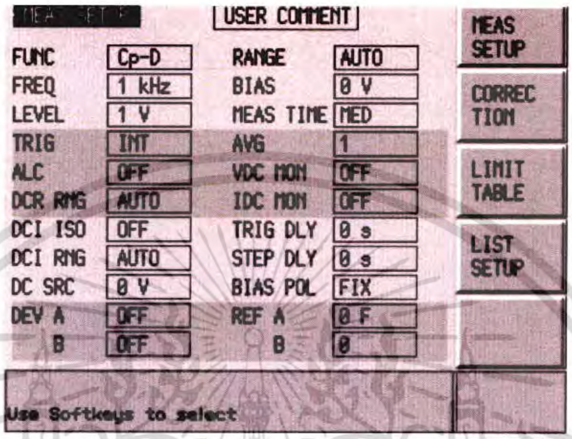


Fig. 3.18 Schematic of the control panel for an Agilent E4980A.

3. After that, the button of "Local/ log" and "System" were pushed, respectively.
4. For setting the condition for measurement the *Z"*-*Z'*, the button of "MEAS SETUP" was pressed. After press, the display of LCR meter showed the display as indicated in Fig 3.19. For setup, the cursor keys were used for shifting the highlighted menu to the purpose menu.



USER COMMENT

FUNC	Cp-D	RANGE	AUTO
FREQ	1 kHz	BIAS	0 V
LEVEL	1 V	MEAS TIME	MED
TRIG	INT	AVG	1
ALC	OFF	VDC MON	OFF
DCR RNG	AUTO	IDC MON	OFF
DCI ISO	OFF	TRIG DLY	0 s
DCI RNG	AUTO	STEP DLY	0 s
DC SRC	0 V	BIAS POL	FIX
DEV A	OFF	REF A	0 F
B	OFF	B	0

Use Softkeys to select

Figure 3.19 Display of LCR meter after pushing the MEAS SETUP button.

5. To set up the function for measuring *Z'* and *Z"*, the menu of function "FUNC" was adjusted to "R-X" (*Z'*-*Z"* function) as presented in Fig. 3.20. Next, the trigger menu "TRIG" menu was adjusted to manual mode "MAN". Then, to define the range of time for measuring, the medium range "MED" was set. Finally, the desirable voltage was adjusted via entering the key "Entry key" as displayed in Fig. 3.21.

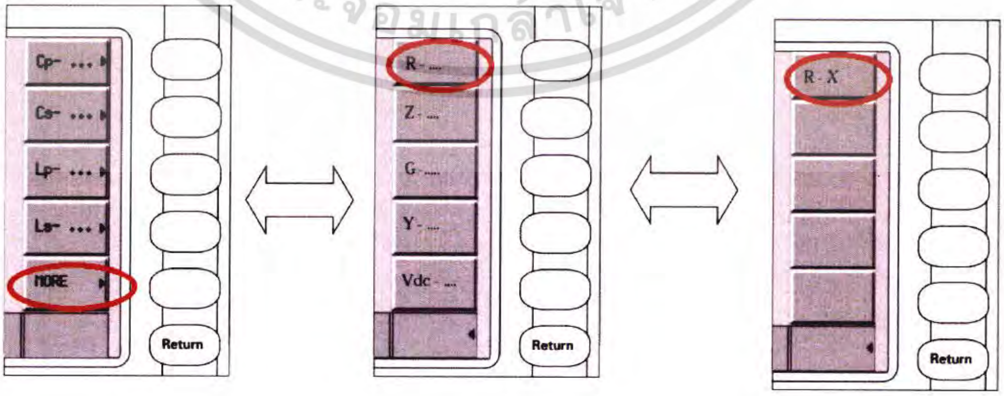
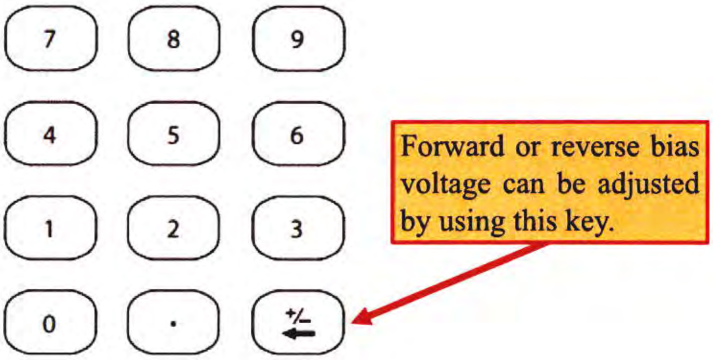


Figure 3.20 Step for setting the function of *Z"*-*Z'* measurement.



Forward or reverse bias voltage can be adjusted by using this key.

Figure 3.21 Entry key for adjusting the number for *Z"-Z'* measurement.

6. To define the values of frequency, "MEAS SETUP" button and "LIST SETUP" menu were pressed, respectively. After that, the display of LCR meter exhibited as Fig. 3.22. The frequency was set to 20 kHz at the first frequency and 2 MHz at the hindmost frequency. Next, the menu of "FILL LOG" was chosen to auto-run the frequency as shown in Fig. 3.23.

Figure 3.22 Display of LCR meter for valuation of the frequency.

Figure 3.23 Display of LCR meter during pressing FILL LOG menu.

7. Backward to the main menu by employing “Display Format” button. Then, “Save/Recall” button, “SAVE DATA” and “START LOG” menu were selected, respectively, to record the set frequency as exhibited in Fig. 3.24.

Figure 3.24 Image during selecting START LOG menu.

8. Back to the main menu by using Display Format button and press the button of LIST SWEEP as depicted in Fig. 3.25.

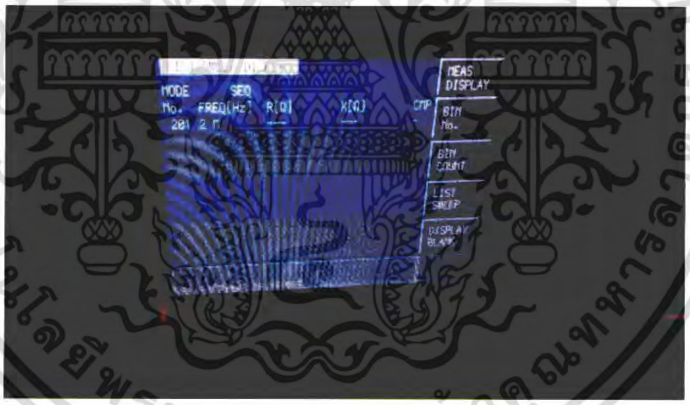


Figure 3.25 Image pushing LIST SWEEP menu.

9. Push DC Bias button to apply the voltage, which the appearance of LED status of DC bias presented in Fig. 3.26. After that, Trigger button was pushed. Then, the LCR meter was performed to measure the data of *Z”* and *Z’* at different frequencies following the defined condition as manifested in Fig. 3.27.

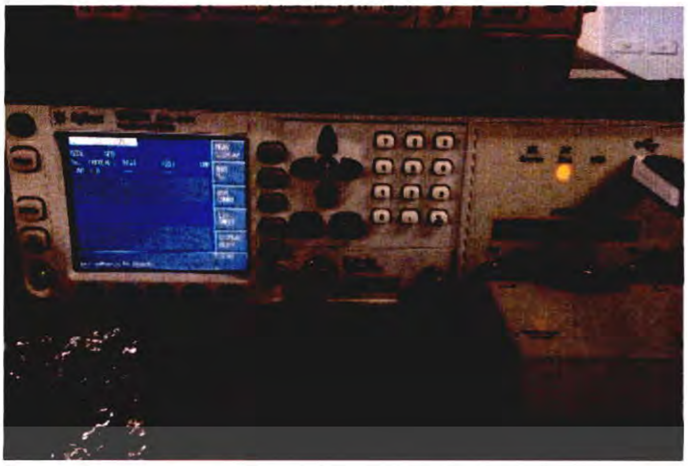


Figure 3.26 Manifestation for LED status of DC bias.

Figure 3.27 Demonstration for the display of LCR meter during operating.

10. After the measurement was finished, Save/Recall button, SAVE DATA and SAVE & STOP menu were selected, respectively, to record the data of *Z”-Z’*. The display will notify “PROCESSING...” and disappear after the completion of the recording process. After the recording process, the file name will show as E498xXXX.csv (001 to 999) and the LED status of USB will turn off.

3.6 Approach for evaluating the diode parameters through TE theory

1. Following the data of *I-V* from the measurement, *I* was change to *J* by dividing with the area. By using the Origin Pro 8.5, the data of *J-V* was plotted. The x-axis was stipulated as *V* and y-axis was determined as a natural logarithm of *J*. Sample for plotting between ln(*J*) and *V* was demonstrated in Fig. 3.28.

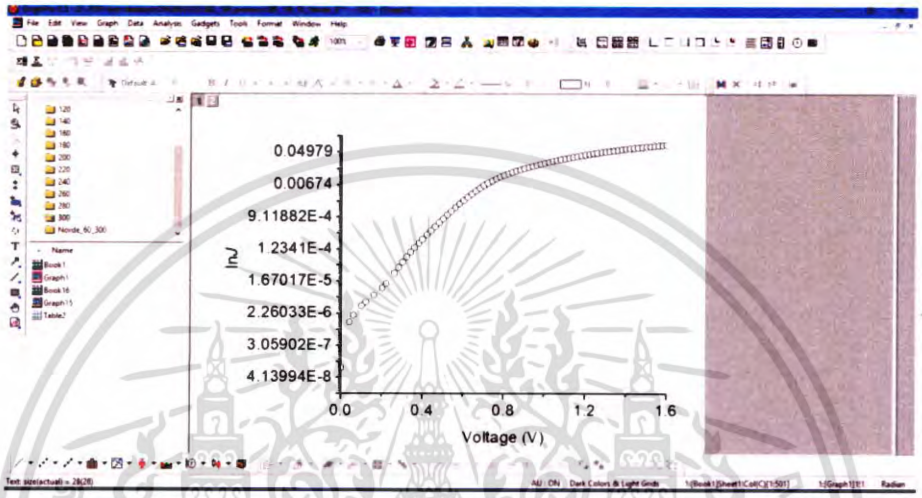
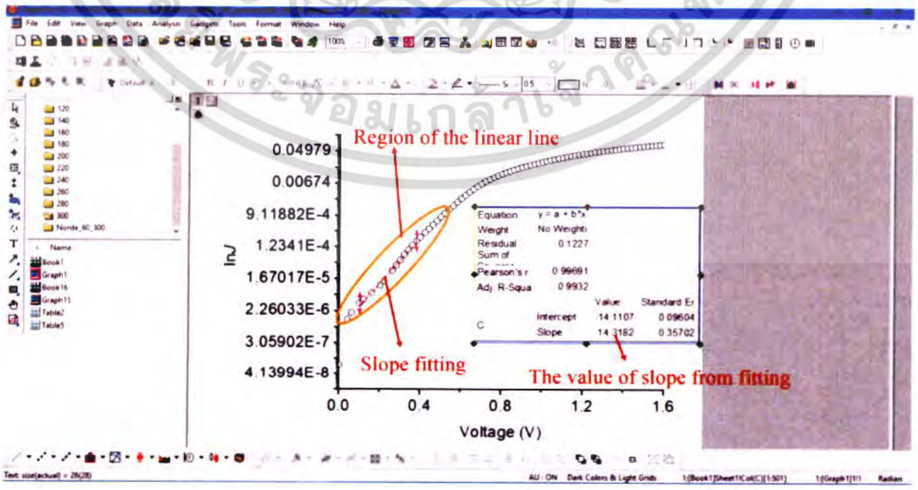


Figure 3.28 Curve of ln(*J*) and *V* plotted via Origin Pro 8.5.

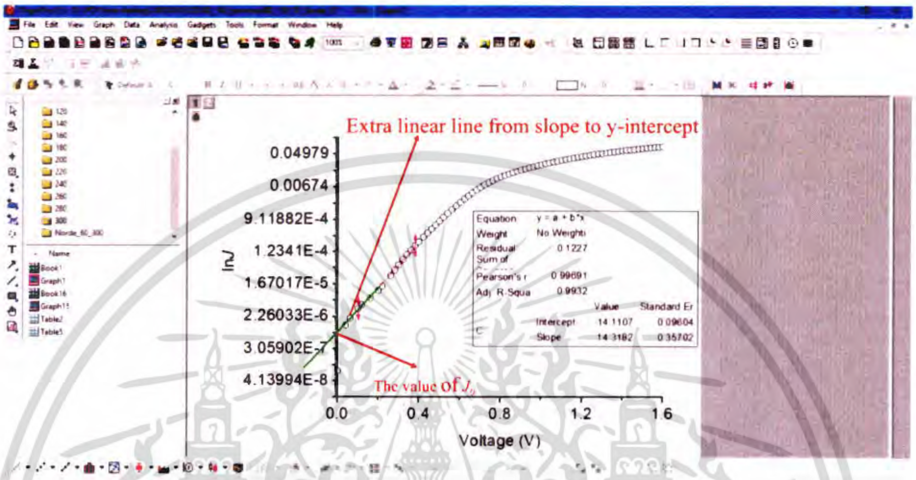
2. Base on the relation of *J-V*, at *V* less than 0.5 V, the *J-V* plot show the linear characteristic in the initial of *J-V* curve. Via fitting the function of the program, we can obtain the slope from the straight line as displayed in Fig. 3.29.



Equation	y = a + b*x		
Weight	No Weighting		
Residual Sum of Squares	0.1227		
Pearson's r	0.99691		
Adj. R-Square	0.9932		
		Value	Standard Error
C	Intercept	14.1107	0.09604
	Slope	14.3182	0.35702

Figure 3.29 Fitting the curve of ln(*J*)-*V* to find the slope using Origin Pro 8.5.

3. In order to estimate the n value of diode parameter, the slope value was substituted into Eq. 2.6.
4. According to the linear line of J-V plot, to obtain the value of J_0, the extra linear line was drawn from the slope line to intercept in y-axis as presented in Fig. 3.30. After that, we employed the screen reader function in Origin Pro 8.5 to point and read the value of J_0 at y-axis intercept.



Equation y = a + b*x
Weight No Weighti
Residual Sum of 0.1227
Pearson's r 0.99691
Adj. R-Squa 0.9932

		Value	Standard Er
C	Intercept	14.1107	0.09604
	Slope	14.3182	0.35702

Figure 3.30 Drawing the extra linear line from ln(J)-V curve to find J_0 value.

5. To calculate the value of ϕ_b, the obtained value of J_0 was substituted into Eq. 2.7.

3.7 Method for calculating the diode parameters via Cheung's model

1. To plot the functions of dV/d(ln$J$) and H(J) against J, Eq. 2.13 and 2.14 were used to compute the values of dV/d(ln$J$) and H(J) functions, respectively.
2. After the calculation of dV/d(ln$J$) and H(J) values, the relation of both values and J was plotted as displayed in Fig. 3.31. Here, the black line was the plot of dV/d(ln$J$)-J and the red line was H(J)-J.

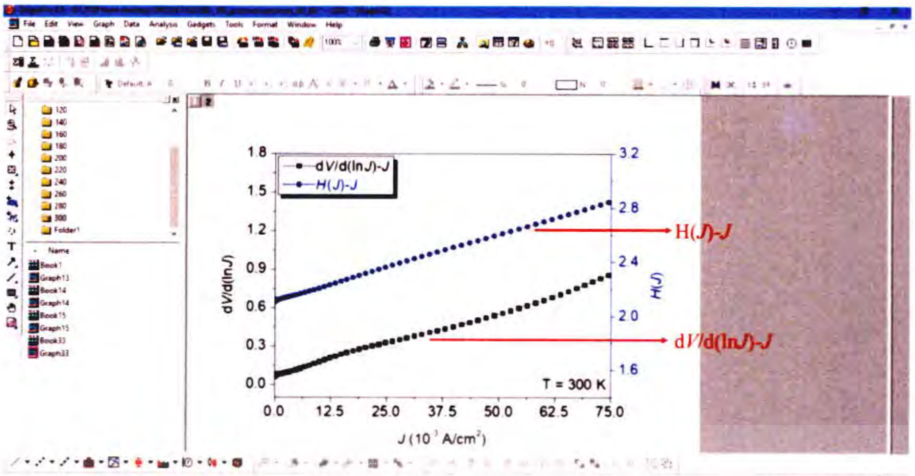
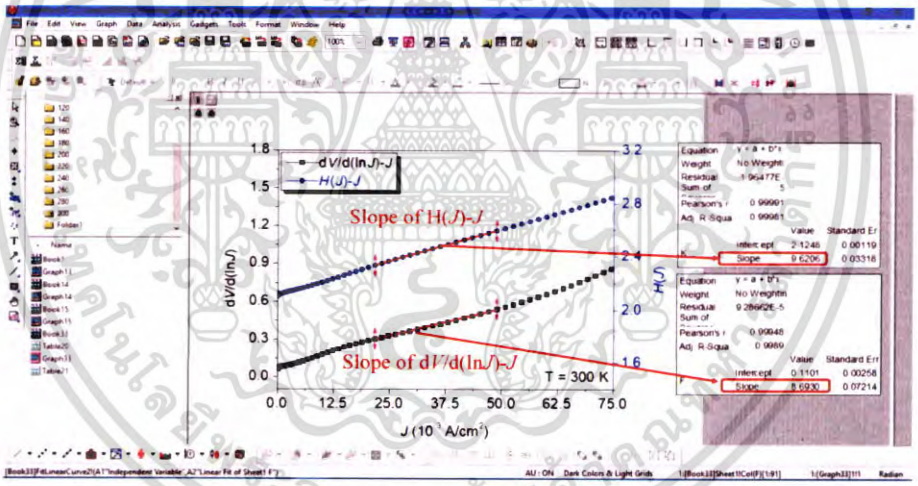


Figure 3.31 Relationship of dV/dln*J* and *H(J)* against *J*. by Origin Pro 8.5.

3. According to the plot in Fig 3.31, the straight lines were observed. By employing function for linear fitting in Origin Pro 8.5, the slopes of both lines were found as shown in Fig. 3.32.



```
Equation      y = a + b*x
Weight        No Weightin
Residual      1.96477E-
Sum of               5
Pearson's r     0.99991
Adj. R-Squa     0.99961
                        Value     Standard Er
K          Intercept    2.1248    0.00119
           Slope        9.6206    0.03318
```

```
Equation      y = a + b*x
Weight        No Weightin
Residual      9.28662E-5
Sum of
Pearson's r     0.99948
Adj. R-Squa      0.9989
                        Value     Standard Err
F          Intercept    0.1101    0.00258
           Slope        8.6930    0.07214
```

Figure 3.32 Estimating the slopes of dV/dln*J*-*J* and *H(J)*-*J* functions in Origin Pro 8.5.

4. The values of slope for dV/dln*J*-*J* or *H(J)*-*J* functions could give the values of R_s via Eq. 2.13 and 2.14, respectively.
5. Additionally, the intercepts from drawing the extra straight line from slopes of both plots to y-axis were used to estimate the values of *n* and ϕ_b via Eq. 2.13 and 2.15, respectively. Where *n* value in Eq. 2.15 was determined by Eq. 2.13.

3.8 Procedure for assessing the diode parameters by model of Norde

1. In the first step, the values of *F(V)* function were estimated from the data of *J-V* by the employment of Eq. 2.16.
2. After calculating the values of *F(V)*, there were plotted versus *V* values as shown in Fig. 3.33. The plots of *F(V)-V* displayed the parabola functions, which each line of *F(V)-V* function gave a minimum point.
3. To obtain the minimum point of *F(V)-V* function, a tool of data reader in Origin Pro 8.5 was used to point and read. The value at a minimum point is called "$F(V_0)$". When V_0 is the bias voltage, which corresponds to *F(V)* at a minimum point.

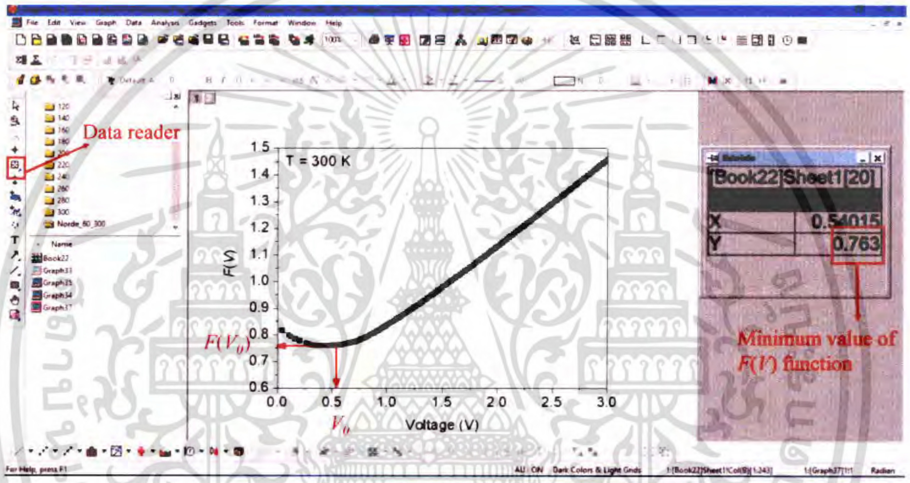
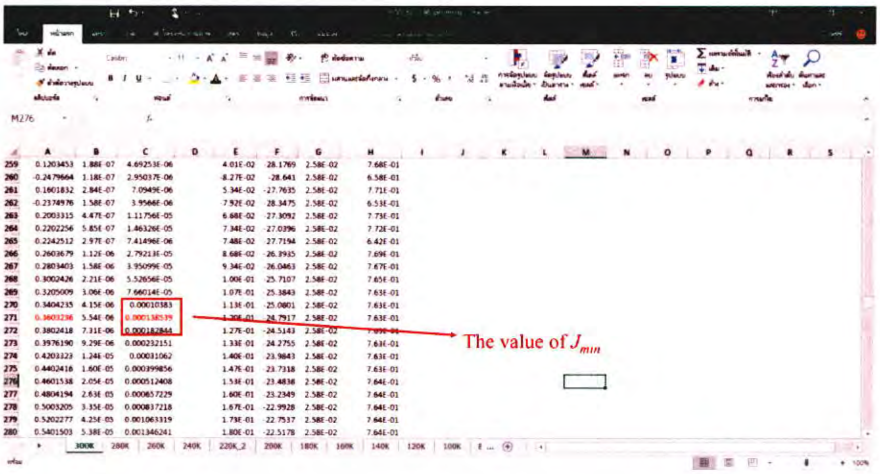


Figure 3.33 The plot of *F(V)* versus *V* value in Origin Pro 8.5.

4. By the utilization of Eq. 2.17, the value of ϕ_b was estimated from the value of $F(V_0)$ and V_0.
5. Following the value of V_0, we can find the corresponding value of *J* from the data of the measured *J-V* as exhibited in Fig 3.34. The corresponding value of current density is called "J_{min}".



M276

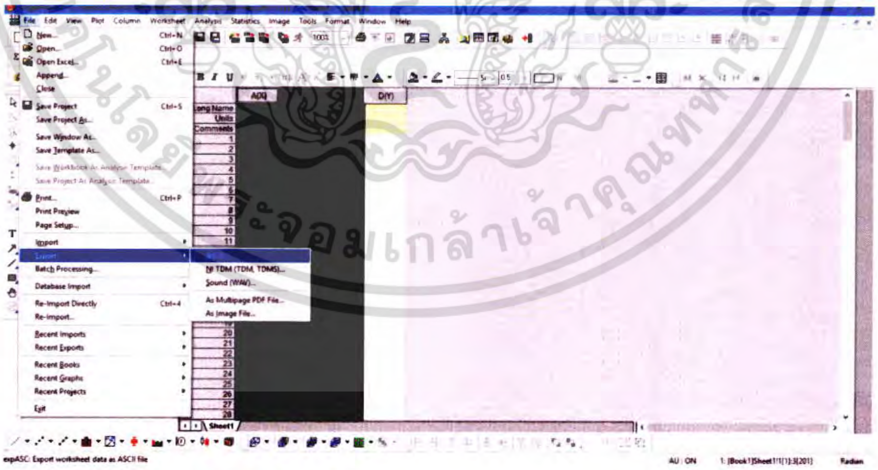
	A	B	C	D	E	F	G	H
259	0.1203453	1.88E-07	4.69253E-06		4.01E-02	-28.1769	2.58E-02	7.68E-01
260	-0.2479664	1.18E-07	2.95037E-06		-8.27E-02	-28.641	2.58E-02	6.58E-01
261	0.1601832	2.84E-07	7.0949E-06		5.34E-02	-27.7635	2.58E-02	7.71E-01
262	-0.2374976	1.58E-07	3.9566E-06		-7.92E-02	-28.3475	2.58E-02	6.53E-01
263	0.2003315	4.47E-07	1.11756E-05		6.68E-02	-27.3092	2.58E-02	7.73E-01
264	0.2202256	5.85E-07	1.46326E-05		7.34E-02	-27.0396	2.58E-02	7.72E-01
265	0.2242512	2.97E-07	7.41496E-06		7.48E-02	-27.7194	2.58E-02	6.42E-01
266	0.2603679	1.12E-06	2.79213E-05		8.68E-02	-26.3935	2.58E-02	7.69E-01
267	0.2803403	1.58E-06	3.95099E-05		9.34E-02	-26.0463	2.58E-02	7.67E-01
268	0.3002426	2.21E-06	5.52656E-05		1.00E-01	-25.7107	2.58E-02	7.65E-01
269	0.3205009	3.06E-06	7.66014E-05		1.07E-01	-25.3843	2.58E-02	7.63E-01
270	0.3404235	4.15E-06	0.00010383		1.13E-01	-25.0801	2.58E-02	7.63E-01
271	0.3603236	5.54E-06	0.000138539		[illegible]	-24.7917	2.58E-02	7.63E-01
272	0.3802418	7.31E-06	0.000182844		1.27E-01	-24.5143	2.58E-02	[illegible]
273	0.3976190	9.29E-06	0.000232151		1.33E-01	-24.2755	2.58E-02	7.63E-01
274	0.4203323	1.24E-05	0.00031062		1.40E-01	-23.9843	2.58E-02	7.63E-01
275	0.4402416	1.60E-05	0.000399856		1.47E-01	-23.7318	2.58E-02	7.63E-01
276	0.4601538	2.05E-05	0.000512408		1.53E-01	-23.4838	2.58E-02	7.64E-01
277	0.4804194	2.63E-05	0.000657229		1.60E-01	-23.2349	2.58E-02	7.64E-01
278	0.5003205	3.35E-05	0.000837218		1.67E-01	-22.9928	2.58E-02	7.64E-01
279	0.5202277	4.25E-05	0.001063319		1.73E-01	-22.7537	2.58E-02	7.64E-01
280	0.5401503	5.38E-05	0.001346241		1.80E-01	-22.5178	2.58E-02	7.64E-01

Figure 3.34 Estimation of J_{min} via the value of V_0 in Excel data.

6. Utilizing Eq. 2.18, the value of R_s can be evaluated from the value of J_{min}.

3.9 Approach for simulating the circuit parameters from *Z"-Z'* curve

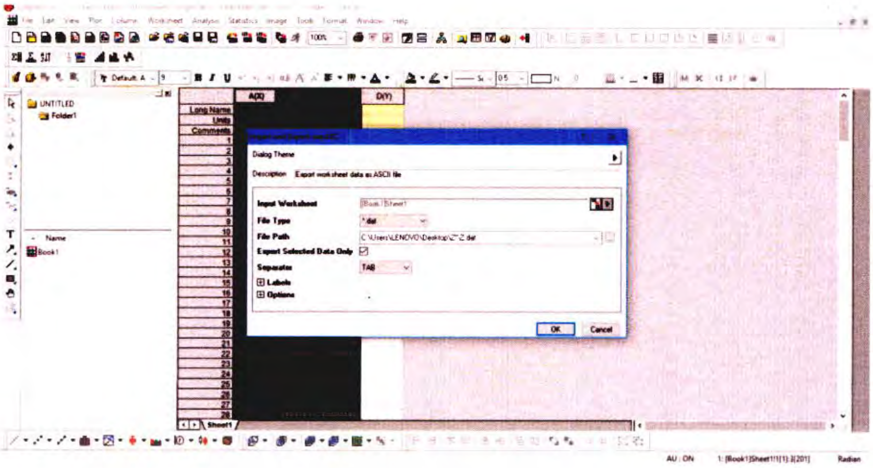
1. According to the data of *Z"-Z'-f*, we can simulate to find the circuit parameters such as R_s, R_p, including CPE by using EC-Lab software.
2. In order to use EC-Lab software, the data of *Z"-Z'-f* must be in .dat file. We can change the data of *Z"-Z'-f* to .dat file by using Origin Pro 8.5 as seen in Fig. 3.35.



expASC: Export worksheet data as ASCII file

Figure 3.35 Changing the *Z"-Z'-f* data to .dat file by using Origin Pro 8.5.

3. We can select the location for saving file as seen in Fig. 3.36.


Dialog Theme

Description Export worksheet data as ASCII file

Input Worksheet [Book1]Sheet1

File Type *.dat

File Path C:\Users\LENOVO\Desktop\Z''Z.dat

Export Selected Data Only ☑

Separator TAB

Figure 3.36 Selecting the location and saving the data by using Origin Pro 8.5.

4. By using EC-Lab software, we can import the data of *Z”-Z’-f* by choosing the menu of Import From Text as shown in Fig. 3.37.

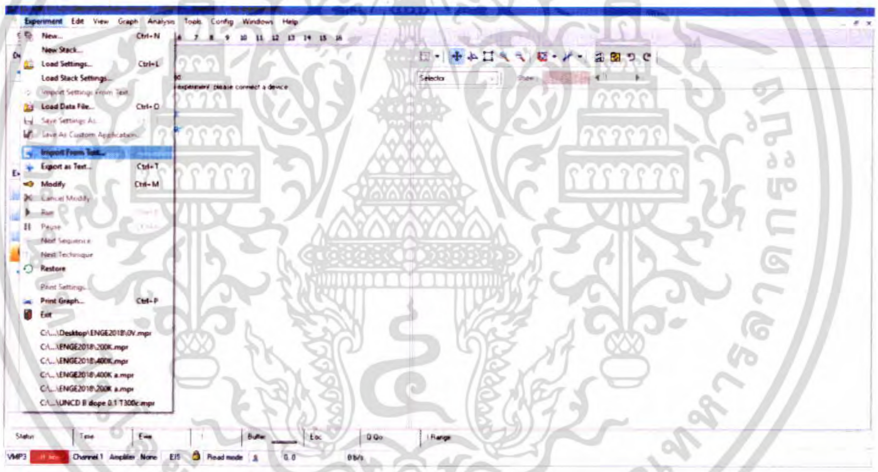
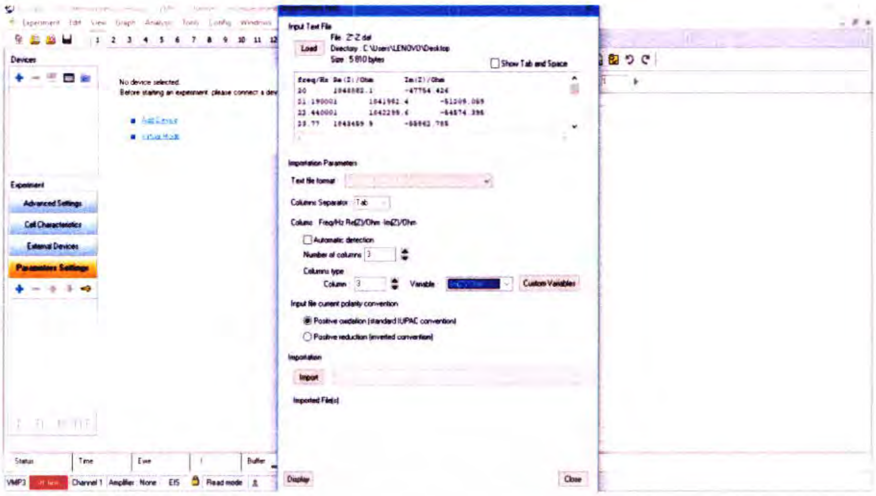


Figure 3.37 Selecting the menu of Import From Text in EC-lab software.

5. After that, the icon of Import From Text will be display as seen in Fig. 3.38. In this icon display, we can set the variations at Column type menu.



Input Text File

File: Z"-Z.dat

Directory: C:\Users\LENOVO\Desktop

Size: 5 810 bytes

Importation Parameters

Columns Separator: Tab

Column: Freq/Hz Re(Z)/Ohm -Im(Z)/Ohm

☐ Automatic detection

Number of columns: 3

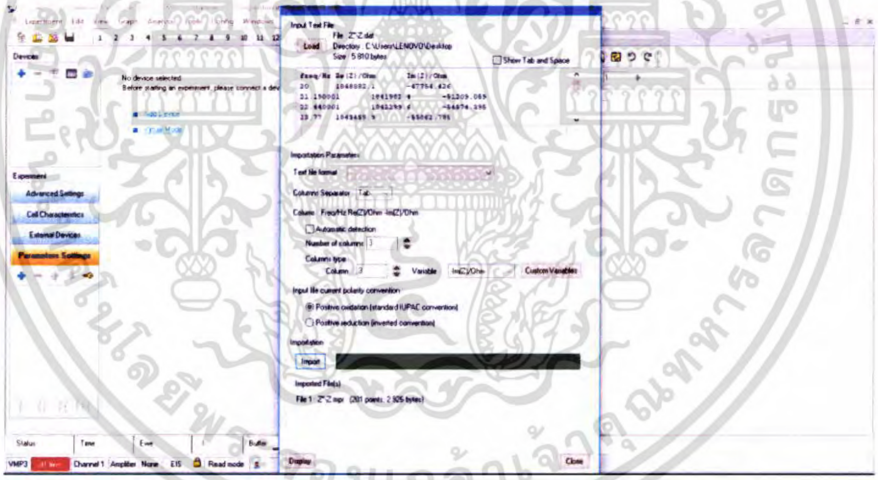
Columns type: Column 3

● Positive oxidation (standard IUPAC convention)

○ Positive reduction (inverted convention)

Figure 3.38 Menu for importing the data in EC-lab software.

6. After setting the variations, we can load the menu of Import as depicted in Fig. 3.39. To display the data, we can select Display menu. Fig. 3.40 exhibited the data of *Z"*-*Z'* curve.



Input Text File

File: Z"-Z.dat

Directory: C:\Users\LENOVO\Desktop

Size: 5 810 bytes

Importation Parameters

Columns Separator: Tab

Column: Freq/Hz Re(Z)/Ohm -Im(Z)/Ohm

☐ Automatic detection

Number of columns: 3

Columns type: Column 3

● Positive oxidation (standard IUPAC convention)

○ Positive reduction (inverted convention)

Imported File(s)

Figure 3.39 Menu for importing the data to simulate the circuit parameters.

7. In order to simulate the circuit parameter, the function of *Z* Fit will be used as seen in Fig. 3.40.

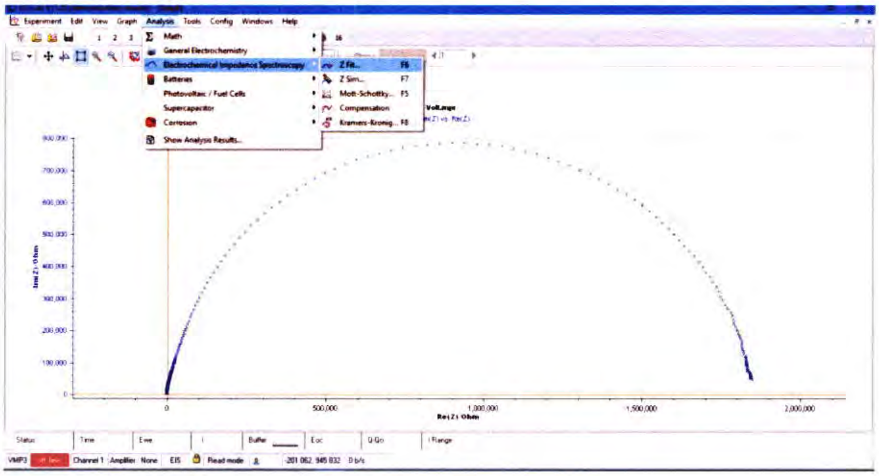


Figure 3.40 Function of *Z* Fit in EC-lab software.

8. After selecting function of *Z* Fit, the program will manifest the *Z* Fit menu as demonstrated in Fig. 3.41.

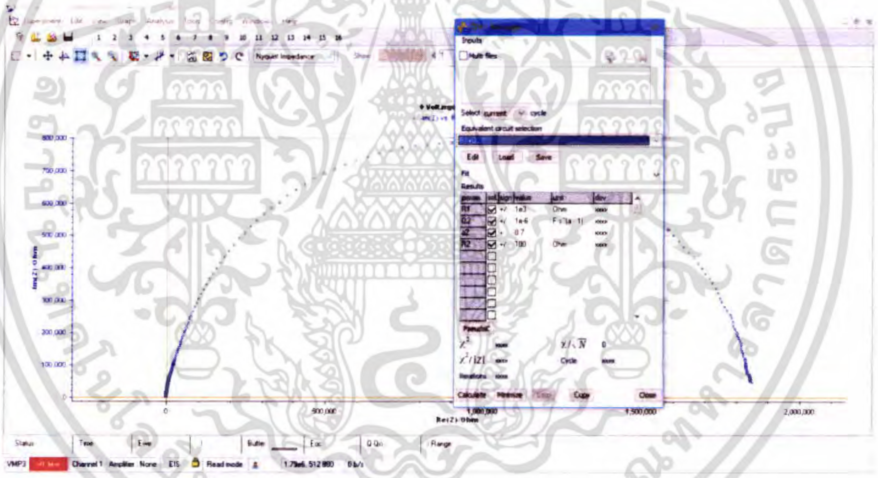
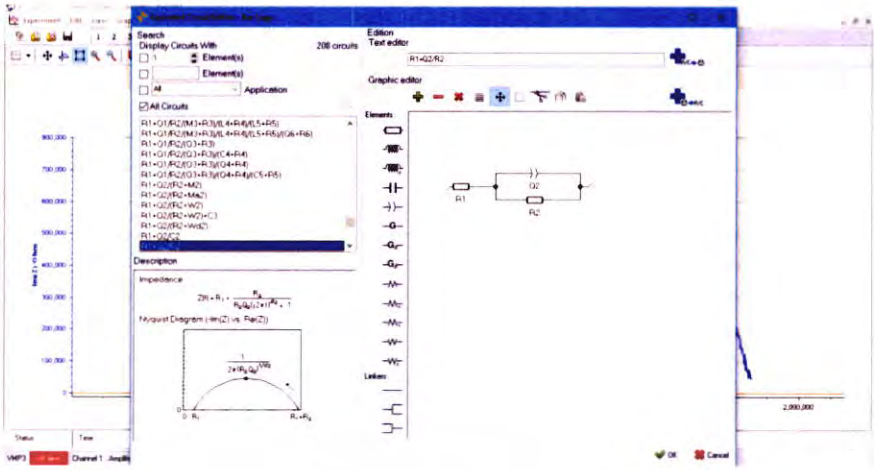


Figure 3.41 *Z* Fit menu for simulating the circuit parameters.

9. For analysis of the characteristics of *Z”-Z’*, we can execute by determining the equivalent circuit, which is appropriate with the heterostructure diodes comprising B-doped UNCD/a-C:H films and Si wafers. In this case, we selected the equivalent circuit, which comprising R_s, R_p and CPE to simulate the magnitudes of these parameters, as indicated in Fig. 3.42.

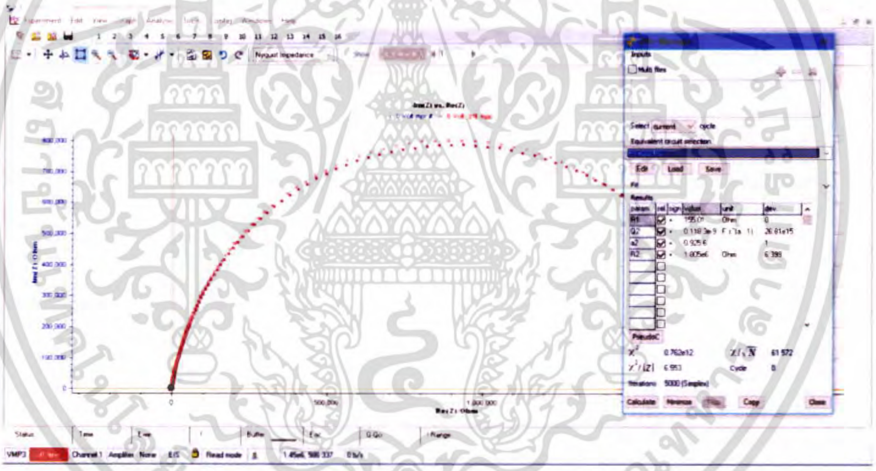


Text editor: R1+Q2/R2

R1+Q1/R2/(M3+R3)/(L4+R4)/(L5+R5)
R1+Q1/R2/(M3+R3)/(L4+R4)/(L5+R5)/(Q6+R6)
R1+Q1/R2/(Q3+R3)
R1+Q1/R2/(Q3+R3)/(C4+R4)
R1+Q1/R2/(Q3+R3)/(Q4+R4)
R1+Q1/R2/(Q3+R3)/(Q4+R4)/(C5+R5)
R1+Q2/(R2+M2)
R1+Q2/(R2+Ma2)
R1+Q2/(R2+W2)
R1+Q2/(R2+W2)+C3
R1+Q2/(R2+Wd2)
R1+Q2/C2

Figure 3.42 Determining the equivalent circuit for fitting the circuit parameters.

10. After determining the equivalent circuit, we can select the menu of Minimize and Calculate to simulate the circuit parameters as presented in Fig. 3.43.



param	sel	sign	value	unit	dev
R1	☑	+	195.07	Ohm	0
Q2	☑	+	0.118 3e-9	F.s^(a-1)	26.81e15
a2	☑	+	0.925 6		1
R2	☑	+	1.605e6	Ohm	6.398

χ^2 0.762e12 $\chi/\sqrt{N}$ 61.572

$\chi^2/|Z|$ 6.953 Cycle 0

Iterations 5000 (Simplex)

Figure 3.43 Simulating the values of the circuit parameters by EC-lab software.

Chapter 4

Results and discussion

4.1 Chapter overview

In this chapter, the author will explore the experimental results of the heterostructure diodes comprising B-doped UNCD/a-C:H films and Si substrates constructed though PLD. In the first section, the surface morphology of the built B-doped UNCD/a-C:H films will be shown and described. After that, the results from *I-V* curves and *Z"-Z'* will be explored and delineated.

4.2 Surface morphology of B-doped UNCD/a-C:H films

4.2.1 Surface of B-doped UNCD/a-C:H films

The observation of B-doped UNCD/a-C:H films surface built employing the PLD was performed by the measurement of FESEM. An illustration of FESEM in flat view with a magnitude of 200,000 was manifested in Fig. 4.1. Following FESEM surface image, it could be revealed that the built film was distinctly smooth surface and the film cracking was not observed. Moreover, the film was composed of a considerable number of B-doped UNCD grains with the diameter less than 10 nm, which were encompassed with an a-C:H matrix. Following this result, it is consistent with the previous report from T. Yoshitake. et. al [1].

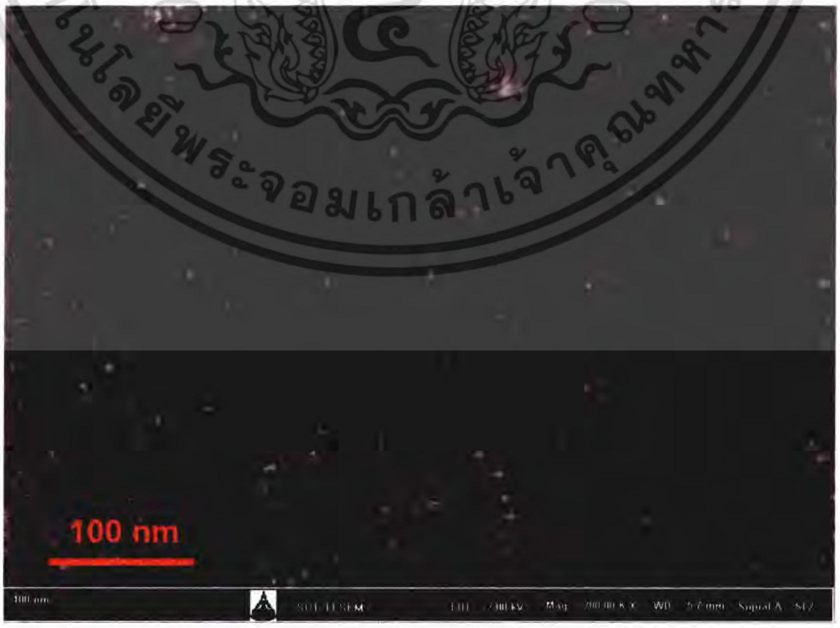


Figure 4.1 Manifestation of FESEM for the built B-doped UNCD/ a-C:H film surface.

4.2.2 Cross-section of B-doped UNCD/a-C:H films

The cross-sectional vision was executed through SEM to survey the constructed heterostructure diode comprising B-doped UNCD/a-C:H film and Si substrate. The presentation of the view of the cross-section of B-doped UNCD/a-C:H film was indicated in Fig. 4.2. According to the cross-sectional view, B-doped UNCD/ a-C:H film on Si substrate was uniform absent film cracking including the interface between the film and substrate can be observed as indicated in Fig. 4.2.

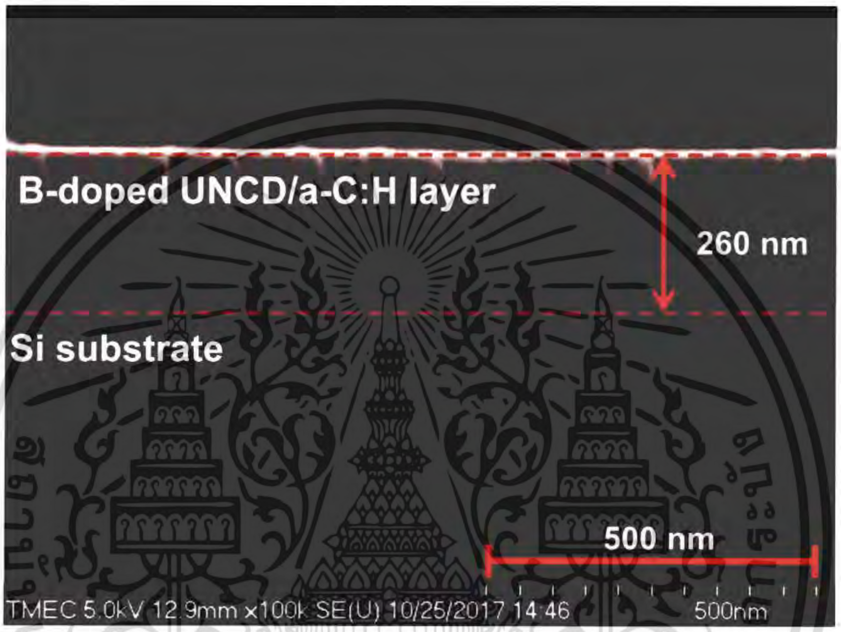


Figure 4.2 Micrograph of SEM of the cross-section for B-doped UNCD/a-C:H films.

4.2.3 Roughness of B-doped UNCD/a-C:H films

The roughness of the produced B-doped UNCD/a-C:H films was executed though measuring AFM. Fig. 4.3 revealed the illustration of the three-dimensional AFM for the produced films with the scanning film area of 500 × 500 nm. The result from scanning the produced film revealed that the film surface was quite smooth with RMS roughness of 4.562 nm.

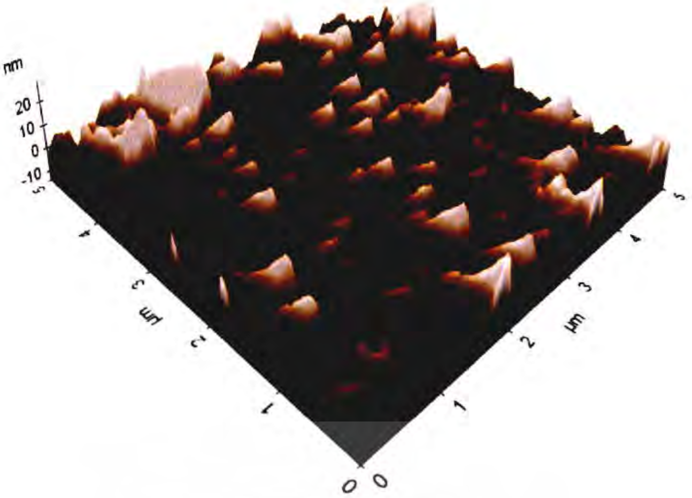


Figure 4.3 AFM image for B-doped UNCD/a-C:H films.

4.3 *J-V* curves of heterostructure diodes comprising B-doped UNCD/a-C:H films and Si wafers

The data from the curve of *J-V* can be employed for estimating turn-on voltage, n, ϕ_b, and R_s. Fig. 4.4 shows the illustration of *J-V* characteristic in linear scale for the heterostructure diodes comprising B-doped p-type UNCD/a-C:H films and n-type Si wafer substrates. The measurement of *J-V* was performed in the dark at the temperature of 300 K, under reverse and forward bias voltage with the junction area of 0.04 mm^2. The built heterostructure diode revealed the rectifying action similar to the common p-n junctions. Additionally, we can obtain the turn-on voltage of 0.56 V from the curve.

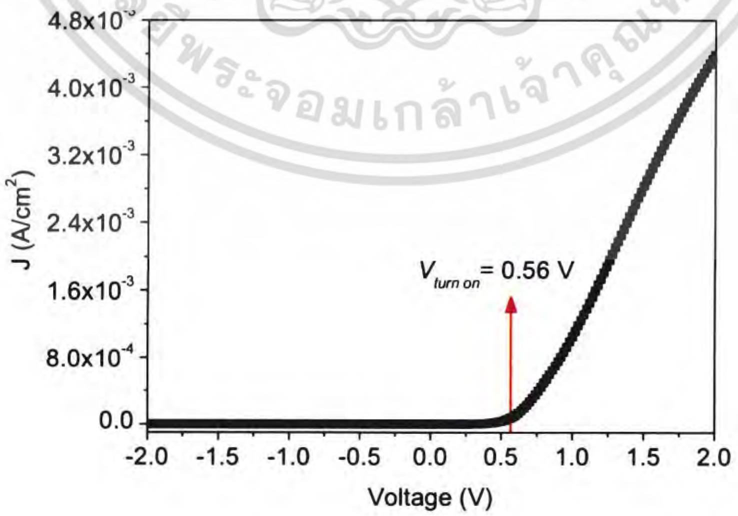


Figure 4.4 Curve of *J-V* in the linear scale of the heterostructure diode measured in the dark condition at 300 K.

Figure 4.5 displays log*J*-*V* plots for the constructed heterostructure diodes comprising B-doped UNCD/a-C:H films and Si substrates at different temperatures in the range of 300 K - 60 K under reverse and forward voltages. The rectifying action of the built heterostructure diode was revealed from *J*-*V* plots. Following the curve of *J*-*V*, the magnitude of the ratio for rectification was approximately four orders at applied voltages of ± 5 V. We can investigate that the ratio of rectification was enhanced at low temperatures. In contrast, the leakage current was high at the temperature of 300 K. A large leakage current occurred from a structural defect in the heterostructure diodes comprising B-doped UNCD/a-C:H films and Si substrates. The leakage current was explicitly decreased at low temperatures.

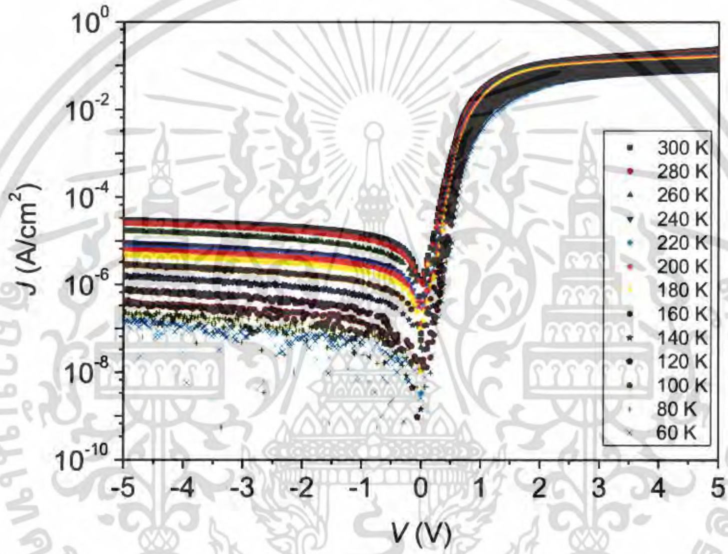
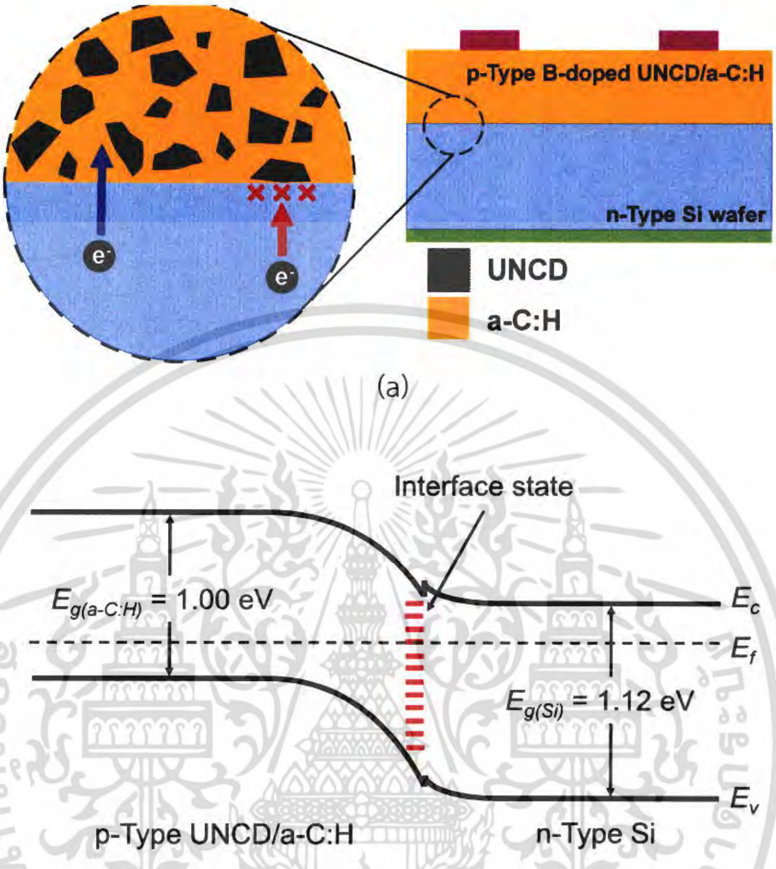


Figure 4.5 Relation between log*J* and *V* curves measured in the dark at different temperatures ranging from 300 K to 60 K.

Fig. 4.6 (a) demonstrated a large number of UNCD grains, which were expected to be partially agglutinated at the interface of the heterostructure diode [21]. The agglutinated grains of UNCD might conduct as the center of carrier trap under reverse bias voltage, which it conformed to the increase of leakage current [21,44]. At the temperature of 300 K, the mechanism of generation-recombination presented particularly, which it revealed having the defect of recombination centers in the heterostructure diode [39,44,45]. The defect might occur from the interface state between the layer of UNCD and Si as depicted in Fig. 4.6 (b) [21,44,45]. The recombination center resulted in the increase of leakage currents. At the temperature of 60 K, the magnitude of leakage current was decreased approximately three orders when there was compared with the leakage currents at 300 K. Abatement of leakage currents at low temperature might be due to the decrease of carrier density.



(a)

(b)

Figure 4.6 (a) Image of the interface between the layer of UNCD and Si and (b) schematic of the band diagram for heterostructure diode created via PLD.

According to *J-V* characteristics under forward bias voltage, *J-V* plot displayed the linear line when *V* was lower than 0.56 V. The current flow across the junction of the conventional diode can be expressed as the below equation [39,44-47]:

$$J = J_0\left(\exp\left(\frac{qV}{nkT}\right)-1\right)$$

Where, J, J_0, q, V, n, k, and T are the current density, saturation current density, charge of an electron, bias voltage, Boltzmann's constant and temperature, respectively.

Following above equation, in the case of the value of V value is higher than $3kT/q$, the value of n can be evaluated through the slope of the linear part of lnJ-V characteristic according to the following formula [39,44-47]:

$$n = \left(\frac{q}{kT}\right)\left(\frac{\mathrm{d}V}{\mathrm{d}(\ln J)}\right) = \left(\frac{q}{kT}\right)\left(\frac{1}{\mathrm{slope}}\right)$$

The value of J_0 can extract from the intercept of the straight line of ln$J$-V function at 0 V. The value of J_0 is used to estimate $\varnothing_\mathrm{b}$ value by using the following equation [45]:

$$J_0 = A^{*}T^{2}\exp\left(\frac{-q\phi_b}{kT}\right)$$

where A^{*} and ϕ_b are Richardson's constant and the value of barrier height, respectively.

The relation of the calculated value of n and T was manifested in Fig. 4.7. At room temperature, the value of n was about 2.70. Following the value of n, there exhibited that the mechanism of heavy recombination and tunneling occurred in the layer of B-doped UNCD/a-C:H and at junction interface [14,48]. The grain boundaries in the layer of B-doped UNCD/a-C:H might construct the deep of energy levels in the energy bandgap, which there produce the recombination centers [49]. The minimal response of DUV light was attributed to recombination of carriers at the interface of junction [50]. Furthermore, the transportation mechanism of tunneling might be owing to existing the interface states at interface between B-doped UNCD/a-C:H layer and Si substrate [49]. The interface states could act as a center of trap for photogenerated carriers, which cause for reducing photocurrent [49,51]. At the temperature of 60, the value of n reached to 8.66. The increase of n, when the temperature was diminished, was likely due to the dependence of interface state density with the temperature [40]. A considerable n value resulted from non-ideality of contact, inhomogeneity and tunneling process [40]. According to a large number of n, the outstanding mechanism for transporting carrier was tunneling process, which occurred from the presence of interface states at heterostructure interface. At low temperatures, the interface states could behave as a center for trapping the photogenerated carriers, which cause for decreasing photocurrent. Additionally, the increase of *n* value at low temperatures was consistent with the value of *n* computed in previous report of P. Sittimart et. al [30].

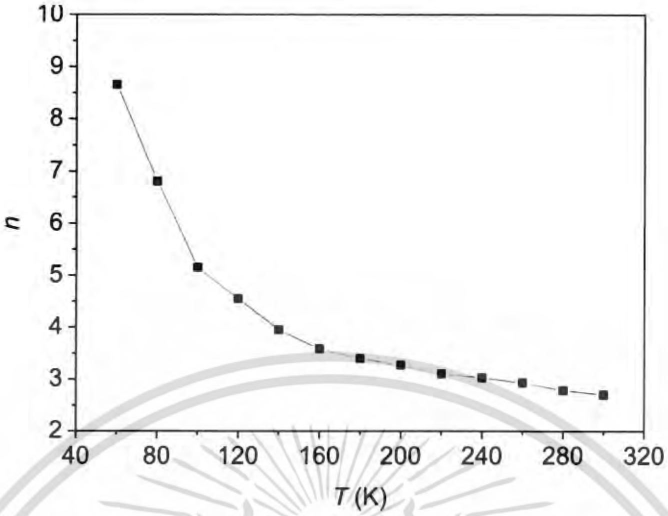


Figure 4.7 Plot of *n* computed via TE theory and *T* for the heterostructure diode.

The plot of the calculated values of ϕ_b against temperature is shown in Fig. 4.8. At the temperature of 300 K, the value of ϕ_b was 0.78 eV, as well as, at the temperature of 60 K, ϕ_b decreased to 0.18 eV. According to the results, it can be observed that the value of ϕ_b decreased and *n* raised when the temperature was reduced. This is attributable to non-uniformity of the charges at the interface of junction and inhomogeneity in the barrier of material [52,53]. The decrease of the calculated ϕ_b conformed with the report of ϕ_b by P. Sittimart et. al [30].

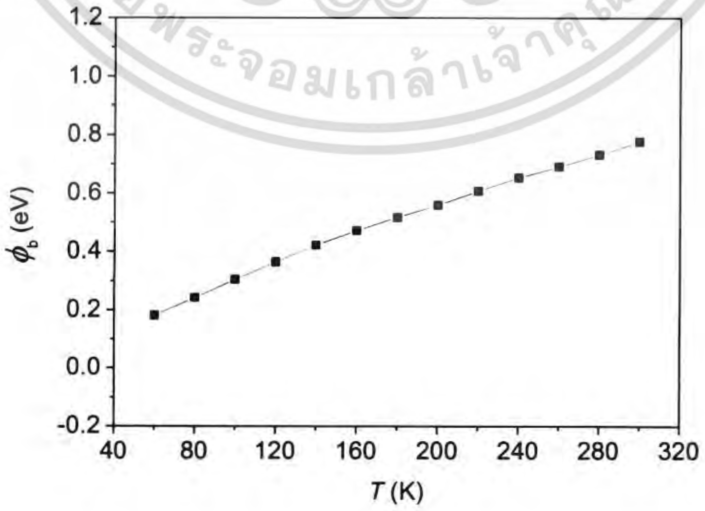


Figure 4.8 Plot of ϕ_b computed from TE theory as a function of temperature.

Following the values of J_0, the values of activation energies (E_a) can be estimated via the following relation [30]:

$$J_0 \propto \exp\left(\frac{\Delta E_a}{kT}\right)$$

Fig. 4.9 exhibited the Arrhenius plot of lnJ_0 versus 1000/T for the heterostructure diodes. The value of J_0 from the intercept of ln$J$-V plot was 7.36×10^{-7} A/cm^2 at the temperature of 300 K and it diminished to the minimum value of 1.82×10^{-10} A/cm^2 at the temperature of 60 K. As seen in Fig. 4.9, the Arrhenius plot showed the two regions, which it demonstrated providing two values of the activation energies. The computed activation energies were found to be 0.15 eV when the temperature raised beyond 140 K and 15.87 meV, when the temperature was below 140 K. Following the activation energies, they revealed the different mechanism of the current of the heterostructure diode at low and high temperature [40,50,54]. When the temperature is more than 140 K, the distinguished mechanism for current flow is recombination. At lower temperature, the tunneling process is the outstanding mechanism for carrier transportation.

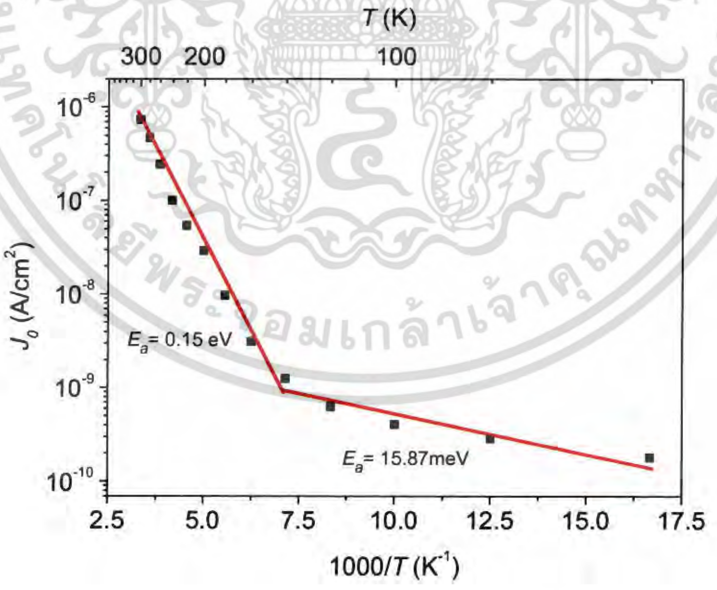


Figure 4.9 Arrhenius plot of lnJ_0 against 1000/T for the heterostructure diodes comprising B-doped UNCD/a-C:H films and Si substrates.

Cheung's model is an approach to extract the value of n, ϕ_b, and R_s from the characteristic of I-V at forward bias. Basically, the values of n and R_s are the considerable parameters, which influence the electrical properties of diodes. The values of n and R_s can be estimated by mean of Cheung' model as described by a given formula [30,31]:

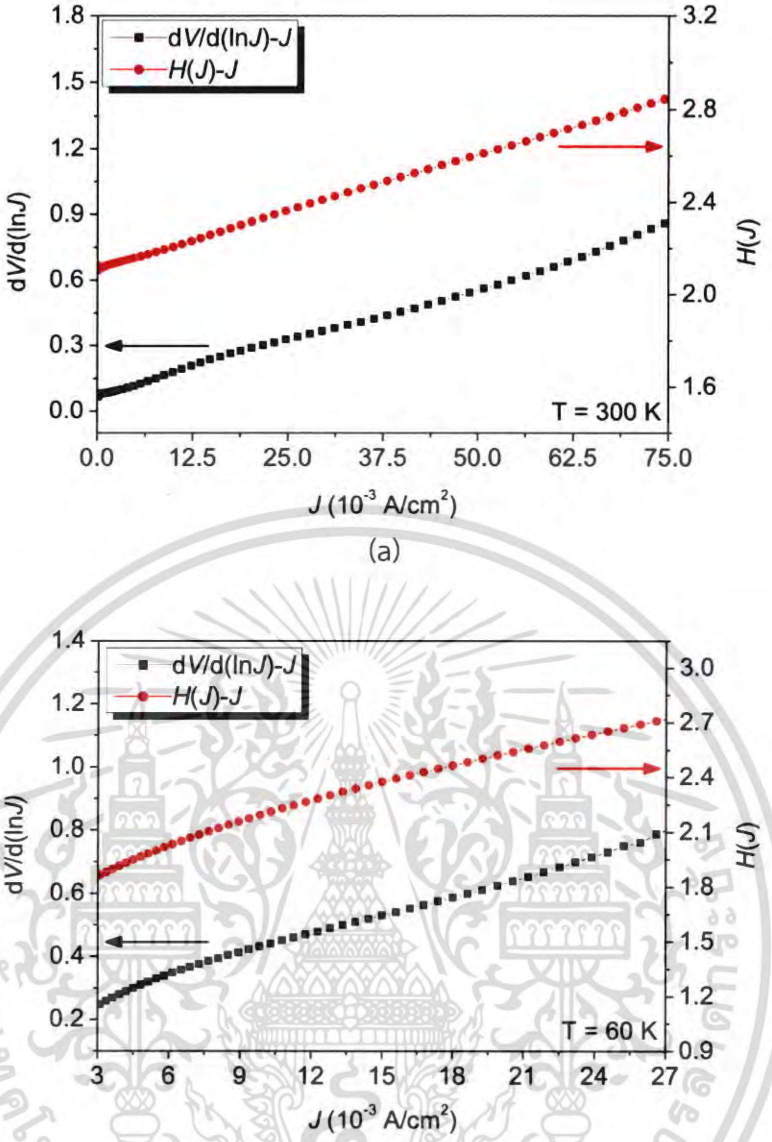
$$\frac{\mathrm{d}V}{\mathrm{d}(\ln J)} = R_s AJ + \frac{nkT}{q}$$

The values of ϕ_b and R_s can be accessed via mean of Cheung' model following relation [30,31]:

$$H(J) = V - \left(\frac{nkT}{q}\right)\ln\left(\frac{J}{T^2 A^*}\right) = R_s AJ + n\phi_b$$

Where V, J, R_s, n, k, T, q, A and A^* are the bias voltage, current density, series resistance, ideality factor, Boltzmann's constant, temperature, electron charge, junction area and Richardson's constant, respectively. Furthermore, the value of n for $H(J)$ function is obtained from the estimated value of n via the calculation from dV/d(ln$J$) plot.

The illustrations of plots of dV/d(ln$J$)-J in the black line and $H(J)$–J in the blue line at the temperature of 300 K and 60 K were indicated in Fig. 4.10 (a) and (b), respectively. From the particularities of dV/d(ln$J$) versus J and $H(J)$ versus J, these plots displayed the linear straight lines, which we can obtain the slope and y-intersection from these plots. The relation between dV/d(ln$J$) and J was plotted for evaluation of the values of R_sA and nkT/q by utilization of the slope of dV/d(ln$J$) characteristic and the intersection of the y-axis, respectively. The trend of R_s and ϕ_b was confirmed from the plot of $H(J)$–J. According to $H(J)$–J characteristic, the value of AR_s was assessed by the usage of the slope of the characteristic of $H(J)$–J, and $n\phi_b$ value was evaluated via the intersection of the y-axis.



(a)

(b)

Figure 4.10 Plot of dV/d(ln*J*) (left vertical axis) - *J* in the black line and the plot of *H*(*J*) (right vertical axis) - *J* in the blue line at (a) 300 K and (b) 60 K.

According to the intercept of y-axis of *dV/d*(ln*J*)-*J* plot, the calculated value of *n* was 2.73 at the temperature of 300 K. It increased to 8.65 at 60 K. The values of *n* versus temperatures were plotted in Fig. 4.11. The trend of *n* from the calculation of *dV/d*(ln*J*)-*J* plot accorded with the value of *n* assessed from TE theory.

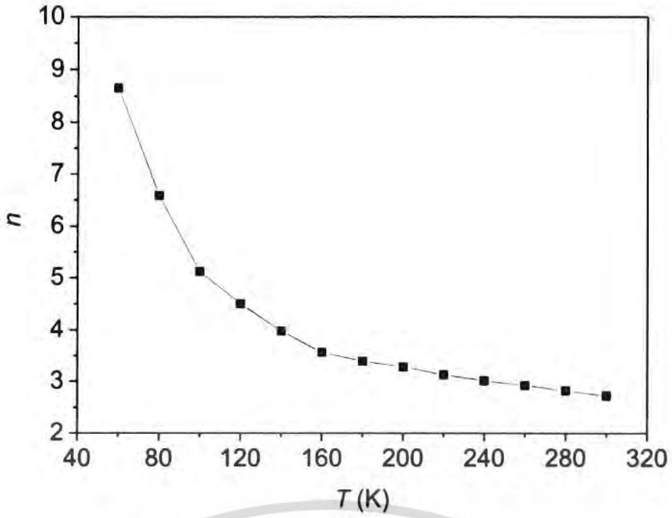


Figure 4.11 Plot of *n* computed from *dV/d(lnJ)-J* characteristics at different temperature for the heterostructure diodes.

The values of ϕ_b via the estimation of *H(J)-J* plots were 0.77 eV at room temperature and 0.18 eV at 60 K. The plot of ϕ_b versus temperature for the heterostructure diodes is shown in Fig. 4.12. The value of ϕ_b was decreased when the temperature was reduced. It demonstrated that ϕ_b computed from the plot of *H(J)-J* conformed to the ϕ_b from the assessment of TE theory.

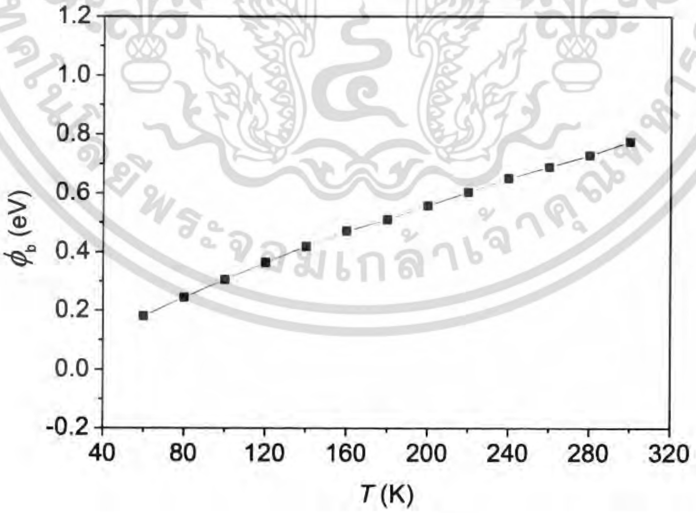


Figure 4.12 Plot of ϕ_b computed from *H(J)-J* plot at different temperatures.

The values of R_s evaluated from $dV/d(\ln J)$-J plot were 271.09 Ω at 300 K and 70.77 kΩ at the temperature of 60 K. This indicated that R_s increased with decreasing temperature. Based on the plot of $H(J)$-J, the values of R_s was found to be 271.72 Ω at the temperature of 300 K and increased to 73.99 kΩ at 60 K. Following these results, it can be described that the trend of R_s by the evaluation from $dV/d(\ln J)$-J plot was consistent with the calculated value of R_s by $H(J)$-J plot. Fig. 4.13 indicated the relation between R_s and temperature by the calculation from $dV/d(\ln J)$-J and $H(J)$-J for the heterostructure diode. The existence of R_s at room temperature was attributable to R_s at the neutral regions including ohmic contact. This is the factor of the current limitation of the heterostructure diode [31]. Moreover, the value of R_s was found that increased distinctly with the decrease in temperature [52]. The increase of R_s might be owing to the similar factors that increase the value of n [39,52], as well as the reduction of carrier concentration in the layer of B-doped UNCD/a-C:H [52,55,56]. The reduction of carrier concentration can decrease the electrical conductivity (σ) and increases R_s value [56]. Following previous work, S. Ohmagari et. al have reported that the value of σ of 0.1 at% B-doped UNCD/a-C:H films via the measurement of van der Pauw method was 3.0 x 10^{-2} S/cm at the temperature of 500 K and decreased to 7.5 x 10^{-3} S/cm at the temperature of 375 K [10]. The increment of the calculated R_s accorded with the previous report by P. Sittimart et. al [30].

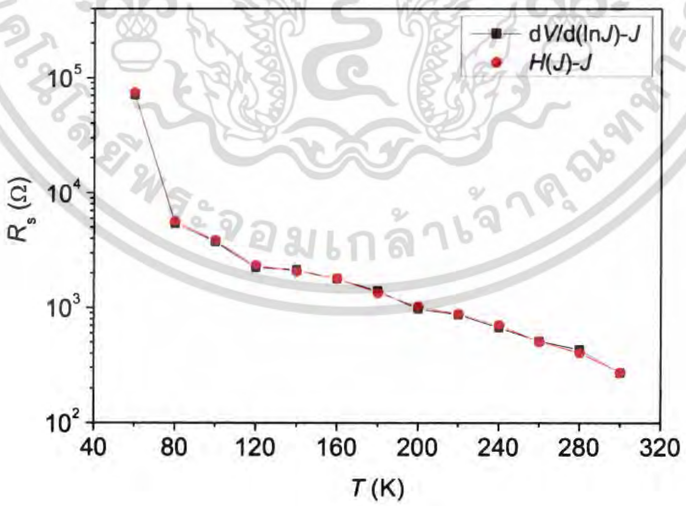


Figure 4.13 Relation of R_s and temperature by the calculation from $dV/d(\ln J)$-J and $H(J)$-J for the heterostructure diode.

In order to confirm the accuracy of the values of R_s and $\varnothing_b$ from TE theory and Cheung's model, Norde's function was applied to extract the considerable parameter of R_s and ϕ_b for the heterostructure diodes. The relation developed by Norde is explained by the following equation [32,33,46]:

$$F(V) = \frac{V}{\gamma} - \left(\frac{kT}{q}\right)\ln\left(\frac{J}{T^2 A^*}\right)$$

where V, k, T, q, J, A^* and γ are the bias voltage, Boltzmann's constant, temperature, charge of electron, current density, Richardson's constant and first integer high than the value of n, which n acquired from TE theory, respectively.

The presence of ϕ_b and R_s value can be estimated through the minimum point of the $F(V)$-V plot. The equation for calculating the value of ϕ_b is expressed following the relation as follows [32,33,46]:

$$\phi_b = F(V_0) + \frac{V_0}{\gamma} - \frac{kT}{q}$$

where $F(V_0)$ and V_0 are the minimum point of $F(V)$ and the voltage, which corresponded to the value of $F(V)$ at minimum point, respectively.

The formula for the estimation of R_s via Norde model is explained as follows [32,33,46]:

$$R_s = \frac{kT}{qAJ_{min}}(\gamma - n)$$

Here, J_{min} is the current density, which corresponded to the minimum point of $F(V)$.

The function of $F(V)$ versus V at the temperature of 300 K in the black line and 60 K in the blue line was manifested in Fig. 4.14. The characteristics of $F(V)$ versus V indicated exponential curves that give a minimum value for each temperature. The presence of ϕ_b can be estimated by using $F(V_0)$ and V_0, which are the minimum point of $F(V)$ and the corresponding voltage. The existence of R_s can be assessed from the current density (J_{min}), which corresponds to the minimum point of $F(V)$.

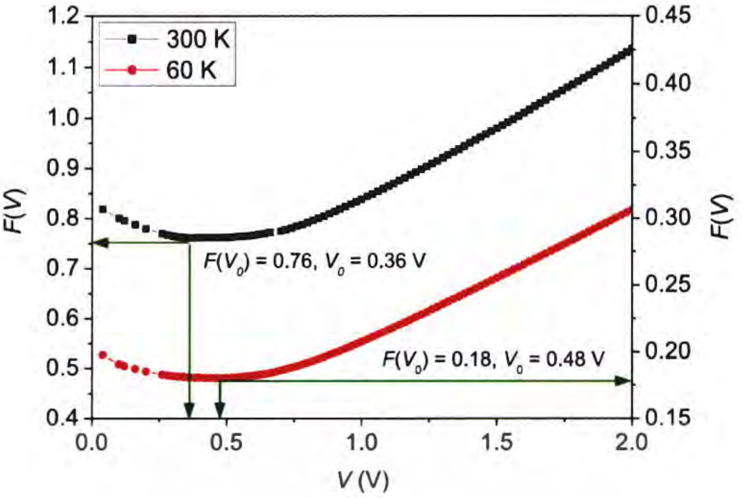


Figure 4.14 Curve of *F*(*V*) versus *V* at 300 K in the black line and 60 K in the blue line.

Following the assessment based on Norde's model, the value of ϕ_b was 0.89 eV at 300 K and it decreased to 0.21 eV at 60 K. The plot of ϕ_b calculated via Norde's model as a function of temperature was shown in Fig. 4.15. The estimated values of ϕ_b by mean of Norde raised when the temperature was increased. These results from Norde's Model conformed to the estimation by TE theory.

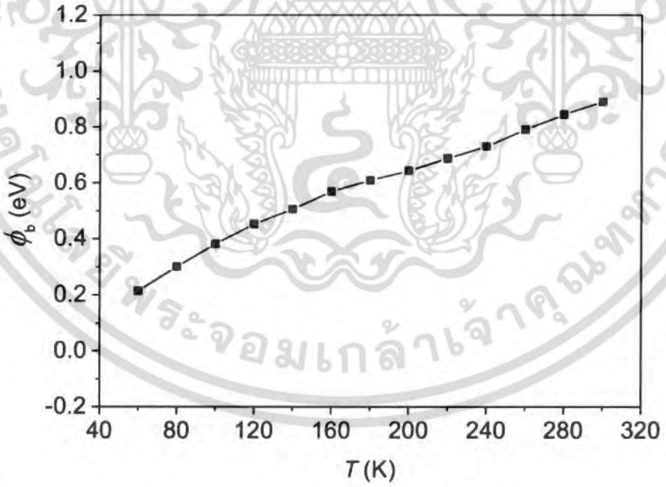


Figure 4.15 ϕ_b calculated via Norde model against temperature for the heterostructure diodes.

Furthermore, R_s calculated by mean of Norde was 275.24 Ω at 300 K and increased to 78.66 kΩ at 60 K. The relation between R_s and temperature was illustrated in Fig. 4.16. As manifested in Fig. 4.16, the value of R_s reduced obviously, when the temperature was decreased. The assessment of R_s from Norde's function are consistent with R_s evaluated by the plots of $dV/d(\ln J)$-J and $H(J)$.

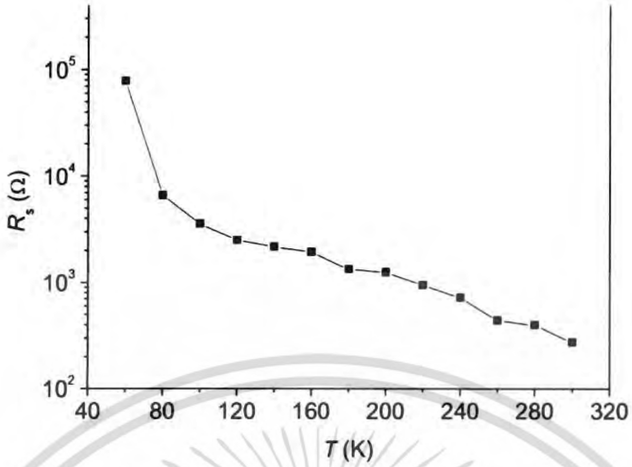


Figure 4.16 Variation of R_s calculated by mean of Norde against temperature for the heterostructure diodes.

4.4 Z''-Z' curves of the heterostructure diode comprising B-doped UNCD/a-C:H films and Si substrates

By utilization of the impedance spectroscopy measurement, the values of Z' and Z'' at different V values were extracted. The relation between Z' and f in the range of V between 0 V and 2 V was displayed in Fig. 4.11. Following the plot of Z'-f, it can be revealed that Z' value was decreased with the increment of bias voltage at low frequencies. The value of Z' slightly changed when the frequency is more than 50 kHz.

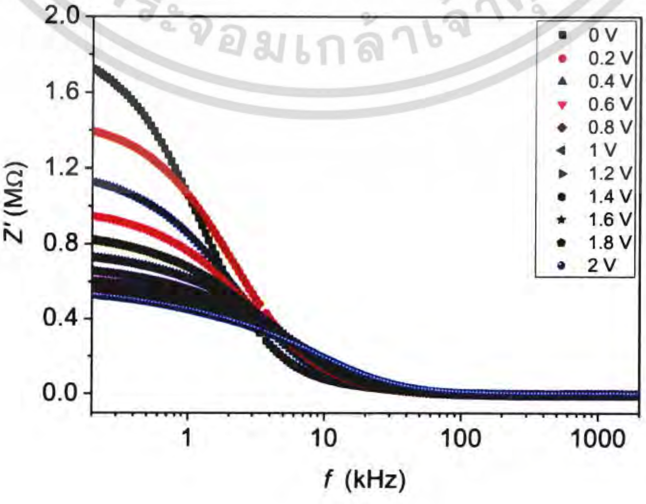


Figure 4.17 Plot of Z' versus f at various V values between 0 V and 2 V.

Fig. 4.18. presented the curve of *Z”* versus *f* under the change of the bias voltage in the range of 0 V – 2 V. At *f* lower than 100 kHz, the peculiarities of *Z”*- *f* plots revealed that the values of *Z”* were distinctly decreased when the bias voltage was raised. At *f* greater than 100 kHz, the value of *Z”* was almost constant with increasing bias voltage. From the curves of *Z”*- *f*, the maximum value of *Z”* at all bias voltage were observed. The peak value of *Z”* at bias voltage of 0 V was 7.87 × 10^5 Ω. The peak value of *Z”* at bias voltage of 2 V was around 1.94 × 10^5 Ω. Additionally, the highest value of *Z”* was slightly shifted to the higher *f* value with elevating bias voltage.

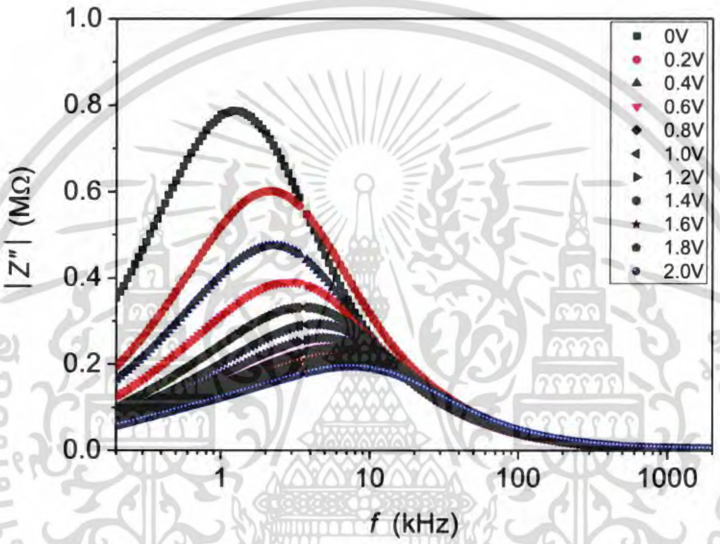


Figure 4.18 Frequency dependence of the *Z”* at different *V* values in the range from 0 V to 2 V.

The observation of *Z”*-*Z’* characteristics at different bias voltage in the range of 0 V - 2 V. Following the characteristics of *Z”*-*Z’*, the values of *f* were diminished from the side of left-hand toward right-hand. The appearance of *Z”*-*Z’* plot presented a single semicircle for all bias voltages. The magnitude of the semicircle was decreased by the increase of bias voltage. The central point of the single semicircle owned the value of *Z”*, which was below than *Z’*.

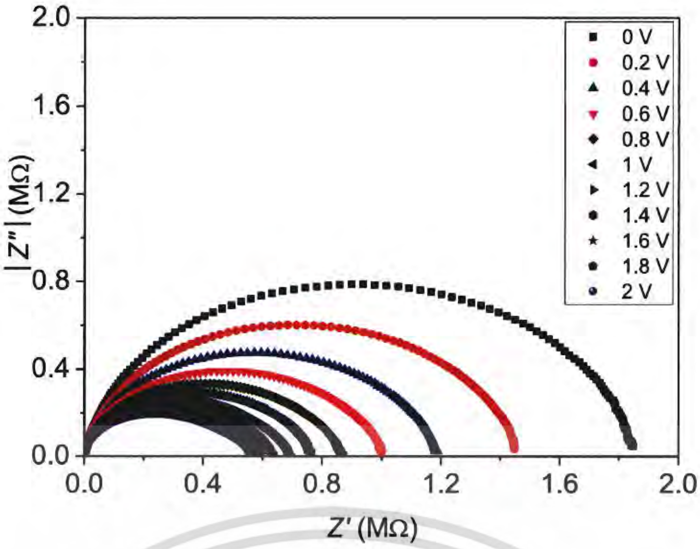


Figure 4.19 Characteristics of *Z"*-*Z'* at different *V* values for the heterostructure diode comprising B-doped UNCD/a-C:H films and Si substrates.

Following the characteristic of the semicircular curve, it indicated that the behavior of the heterostructure diode comprising B-doped UNCD/a-C:H films and Si substrates should be appropriate with an equivalent circuit as manifested in Fig. 4.20 [18,20,38,57-59]. The equivalent circuit was composed of the association of CPE and R_p in parallel, which connected with R_s [18,20,38,57-59]. R_s expressed the resistance within Ohmic contact and bulk in the active layer [38,58,59]. R_p determined by the resistance of charge transfer [38,58,59]. CPE is the non-ideality, including an adjustable parameter in order to recompense for non-homogeneity in the blocking interfaces because of the surface states [18,20,38,58,59].

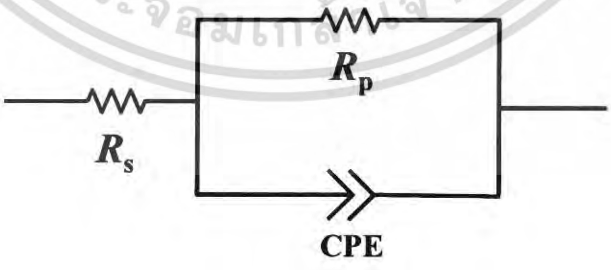


Figure 4.20 Model of equivalent circuit corresponding the curve of *Z"*-*Z'* for the heterostructure diode comprising B-doped UNCD/a-C:H films and Si substrates.

The values of R_s, R_p and CPE parameters were simulated via the usage of EC-Lab Software. Following the result of simulation, the existence of R_s was found to be 171.55 Ω at bias voltage of 0 V. At higher bias voltage, R_s was found that decreased and it reduced to 52.97 Ω at the bias voltage of 2 V. Figure 4.21 exhibited R_s as a function of bias voltage at various *f*. From the obtained R_s, it presented the reduction of R_s when the bias voltage was raised. The obtained values of R_s is likely owing to the presence of R_s in the Ohmic contact and neutral regions [60,61].

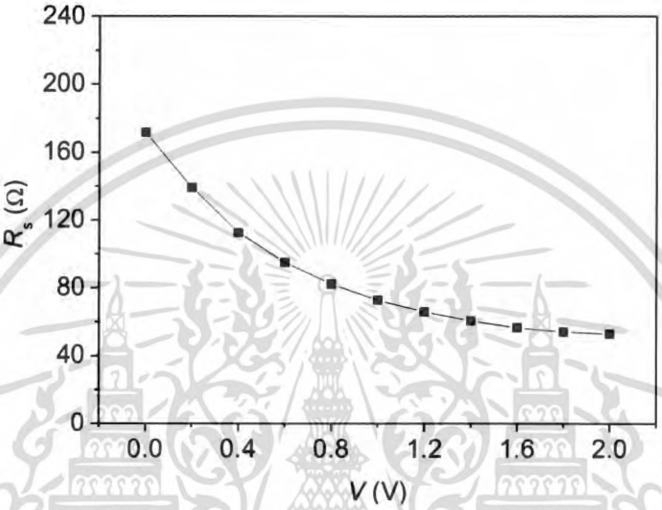


Figure 4.21 Variation of simulated values of R_s as a function of *V*.

At the bias of 0 V, R_p value from the simulation by EC-Lab Software was 1.88 × 10^6 Ω and it dropped to 4.67 × 10^5 Ω at bias voltage of 2 V. From these results, R_p decreased with the increment of bias voltage, which it should be likely due to the leakage paths following the resultant of currents from generation-recombination in depletion area [18,62].

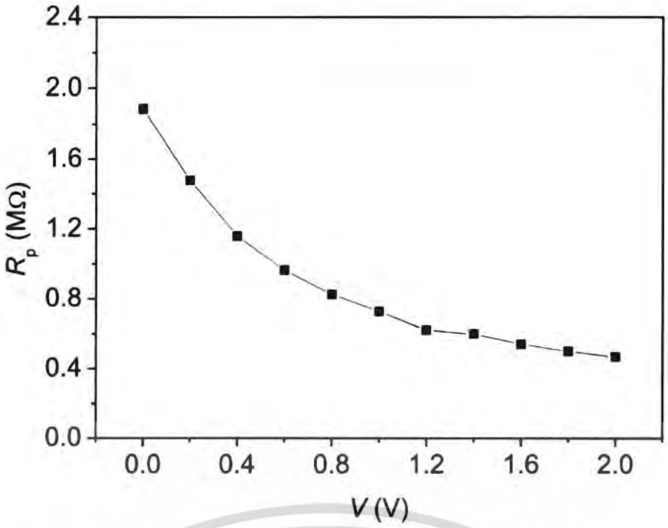


Figure 4.22 The simulated value of R_p as as a function of V.

Based on the simulation from EC-Lab Software, the value of CPE was found to be 2.14×10^{-9} F with the deviation from standard (*a*) value of 0.90 at the bias voltage of 0 V. At higher bias violtage, CPE was dropped, and it was diminied to 1.13×10^{-9} F with *a* value of 0.91 at the bias voltage of 2 V. The diminution of CPE at higher bias voltage might be ascribe to the increment of current across the device [63].

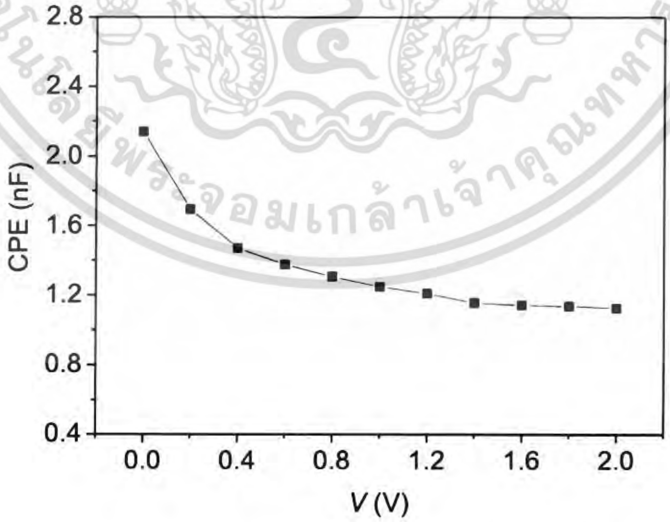


Figure 4.23 Relation of the values of CPE from simulation and V.

Chapter 5

Conclusion and suggestions

5.1 Conclusion

The heterostructure diodes consisting B-doped UNCD/a-C:H film and Si layer was produced by utilization of PLD with the substrate temperature of 550 °C. The examination of the surface morphology and the electrical features regarding *I-V* and *Z"-Z'* characteristics of the heterostructure diode was performed in this study.

From the observation of FESEM surface illustration, the film was composed of a considerable number of B-doped UNCD grains with diameter less than 10 nm surrounded by an a-C:H matrix. In addition, the film cracking was not observed, and the film revealed distinctly smooth surface. The cross-sectional vision from SEM presented that the interface between B-doped UNCD/a-C:H films and Si substrate was uniform. By utilization of AFM, an AFM illustration of the produced film revealed the rms roughness of 4.562 nm.

The measurement of *I-V* characteristics was executed under dark condition at various temperatures in the range of 300 K – 60 K. TE theory, Cheung approach, and Norde model were utilized to assess their diode parameters such as n, ϕ_b and R_s. The values of n assessed by TE theory were 2.70 and 8.66 at 300 K and 60 K, respectively. These values of n are in agreement with those estimated by Cheung model. It indicated that the carrier transport mechanism is controlled by the recombination process accompanied with tunneling process at 300 K, while the tunneling mechanism is outstanding at 60 K. The increment of n at lower temperatures might be due to the interface states which behave as a center for trapping the photogenerated carriers. The minimal response of DUV light was attributed to recombination of carriers at the interface of junction. Based on TE theory, the estimated barrier height values at 300 K and 60 K were 0.78 and 0.18, respectively. The estimated barrier height values from approaches of Cheung and Norde conformed with TE theory. The decrease of ϕ_b with the reduction of temperature is attributable to non-uniformity of the charges at the interface of junction and inhomogeneity in the barrier of material. The evaluated magnitudes of R_s from the functions of d*V*/dln*J*-*J* and *H*(*J*)-*J* were consistence with those of Norde model. Via d*V*/dln*J*-*J* characteristics, R_s was 271.09 Ω at 300 K and 70.77 k Ω at temperature of 60 K. At low temperatures, the increase of R_s was likely due to the decrease of carrier concentration · in the B-doped UNCD/a-C:H films.

At temperature of 300 K, the measurement of impedance spectroscopy was executed under dark condition at different voltages ranging from 0 V – 2 V and a frequency range of 20 Hz - 2 MHz to extract *Z'* and *Z"* magnitudes. The curves of *Z"-Z'* presented a single semicircle for all bias voltages. The magnitudes of the semicircle were dropped by the increment of bias voltage. The central point of the single semicircle was depressed below *Z'*. This can be identified that the heterostructure diodes conformed with the model of R_p with CPE in parallel combined with R_s. R_s expressed the resistance within Ohmic contact and bulk in the active layer. R_p determined by the resistance of charge transfer. CPE is the non-ideality, including an adjustable parameter to recompense for non-homogeneity in the blocking interfaces because of the surface states. The simulation of R_s, R_s and CPE were performed by the employment of EC-lab software. The existence of R_s were 171.55 Ω at 0 V and 52.97 Ω at 2 V. The reduction of R_s, when the bias voltage was raised, is likely owing to the presence of R_s in the Ohmic contact and neutral regions. At 0 V, the magnitude of R_p was 1.88×10^6 Ω and it dropped to 4.67×10^5 Ω at 2 V. The depression of R_p with the increment of bias voltage ascribed to the leakage paths following the resultant of currents from generation-recombination in depletion area. The manitude of CPE at 0 V and 2 V were 2.14×10^{-9} F with *a* of 0.90 and 1.13×10^{-9} F with *a* value of 0.91, respectively.

5.2 Suggestions

1. The impedance characteristics for heterostructure diodes comprising B-doped UNCD/a-C:H films and Si wafers should be measured under illumination of UV light.
2. The impedance characteristics for heterostructure diodes comprising B-doped UNCD/a-C:H films and Si wafers should be measured under various B-doped concentrations.
3. The impedance characteristics for heterostructure diodes comprising B-doped UNCD/a-C:H films and Si wafers should be measured at low temperatures.
4. The impedance characteristics for heterostructure diodes comprising N-doped UNCD/a-C:H films and Si wafers should be measured.
5. The impedance characteristics for heterostructure diodes comprising B-doped UNCD/a-C:H films and Si wafers constructed by coaxial arc plasma deposition (CAPD) should be measured.

6. The capacitance-voltage (C-V) and conductance-voltage (G-V) characteristics for heterostructure diodes comprising B-doped UNCD/a-C:H films and Si wafers should be measured in order to estimate the interface state density by mean of Hill-Coleman.

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Academic Publications

1. Rawiwan Chaleawpong, Nathaporn Promros, Peerasil Charoenyuenyao, Takanori Hanada, Shinya Ohmagari, Abdelrahman Zkria, and Tsuyoshi Yoshitake, Junction parameters of boron-doped p-type ultrananocrystalline diamond/hydrogenated amorphous carbon composite/n-type silicon heterojunctions formed by pulsed laser deposition, Journal of Nanoscience and Nanotechnology, (accepted). (Impact factor 1.483, Indexed in ISI).
2. Peerasil Charoenyuenyao, Nathaporn Promros, Rawiwan Chaleawpong, and Tsuyoshi Yoshitake, Surface morphology and wettability for thin films of beta-iron disilicide produced through direct-current sputtering utilizing a pair of facing targets, The 4th International Conference on Engineering, Applied Sciences and Technology, 1091-1094.
3. Nathaporn Promros, Pitoon Noymaliwan, Peerasil Charoenyuenyao, Rawiwan Chaleawpong, Supanit Porntheeraphat, Bunpot Saekow, Tanapoj Chaikeeree, Benjarong Samransuksamer, Peerapong Nuchuay, Chanunthorn Chananonnawathorn, Saksorn Limwichean, Mati Horprathum, Pitak Eiamchai, and Viyapol Patthanasettakul, Study of Annealing Influence on Basic Properties of Indium Tin Oxide Nanorod Films Deposited Using Glancing Angle Ion-Assisted Electron Beam Evaporation, Journal of Nanoscience and Nanotechnology, (accepted). (Impact factor 1.483, Indexed in ISI).

Author Biography (cont.)

Academic Publication(s)

4. Weerasaruth Kaenrai, Nathaporn Promros, Phongsaphak Sittimart, Rawiwan Chaleawpong, Peerasil Charoenyuenyao, Thanachai Changcharoen, Adison Nopparuchikun, Tomohiro Nogami, and Tsuyoshi Yoshitake, Photovoltaic Properties and Series Resistance of p-Type Si/Intrinsic Si/n-Type Nanocrystalline FeSi2 Heterojunctions Created by Utilizing Facing-Targets Direct-Current Sputtering, Journal of Nanoscience and Nanotechnology, (accepted). (Impact factor 1.483, Indexed in ISI).
5. Nathaporn Promros, Pitoon Noymaliwan, Peerasil Charoenyuenyao, Rawiwan Chaleawpong, Supanit Porntheeraphat, Bunpot Saekow, Tanapoj Chaikeeree, Benjarong Samransuksamer, Peerapong Nuchuay, Chanunthorn Chananonnawathorn, Saksorn Limwichean, Mati Horprathum, Pitak Eiamchai, and Viyapol Patthanasettakul, Impact of Annealing Temperature on the Physical Properties of Indium Tin Oxide Nanorod Films Grown by Glancing-Angle Ion-Assisted Electron-Beam Evaporation, E-MRS Proceedings, (accepted).