TECHNIQUES FOR TEMPERATURE-COMPENSATED AND LOW-NOISE CMOS RC OSCILLATORS

SIRAPORN SAKPHROM

A THESIS SUBMITTED IN FULLFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF DOCTOR OF ENGINEERING IN ELECTRICAL ENGINEERING
FACULTY OF ENGINEERING
KING MONGKUT'S INSTITUTE OF TECHNOLOGY LADKRABANG
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หัวข้อวิทยานิพนธ์ เทคนิคการชดเชยอุณหภูมิและการลดสัญญาณรบกวนสำหรับวงจรซีมอสออสซิลเลเตอร์ที่ใช้ตัวต้านทานและตัวเก็บประจุ

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พ.ศ. 2558

อาจารย์ที่ปรึกษาวิทยานิพนธ์ รศ. ดร. อภินันท์ ธนชยานนท์

บทคัดย่อ

วิทยานิพนธ์นี้อธิบายเทคนิคสำหรับการชดเชยอุณหภูมิสำหรับวงจรซีมอสออสซิลเลเตอร์แบบรีแลกซ์และการลดสัญญาณรบกวนในวงจรซีมอสออสซิลเลเตอร์แบบวงแหวน การนำเสนอเทคนิคการชดเชยอุณหภูมิ ใช้องค์ประกอบของวงจรในวงจรออสซิลเลเตอร์แบบรีแลกซ์ ซึ่งขึ้นกับอุณหภูมิ เพื่อชดเชยในการเลื่อนของความถี่เนื่องจากการเปลี่ยนแปลงอุณหภูมิโดยรอบ การนำเสนอการชดเชยอุณหภูมิในวงจรออสซิลเลเตอร์แบบรีแลกซ์ใช้โครงสร้างการควบคุมของกระแสด้วยค่าต้านทานจากทรานส์คอนดักเตอร์ที่ใช้การถดถอยซอร์ส และใช้วงจรเปรียบเทียบกระแสเพื่อทำให้ได้ที่ความถี่ออสซิเลชันสูงและกินกำลังงานต่ำ วงจรออสซิลเลเตอร์แบบรีแลกซ์ถูกออกแบบและเพิ่มประสิทธิภาพโดยใช้เทคโนโลยีซีมอสขนาด 0.35 ไมโครเมตร ด้วยแรงดันไฟเลี้ยง 2.5 โวลต์ ผลการจำลองการเลย์เอาท์แสดงให้เห็นการทำงานของวงจร ซึ่งสามาถทำงานได้ที่ความถี่ ระดับหลักสิบเมกกะเฮิร์ตภายใต้สัมประสิทธ์ทางอุณหภูมิ 100 ส่วนในล้านส่วน ต่อ องศาเซลเซียส (ppm/°C) ของการเปลี่ยนแปลงความถี่ช่วงอุณหภูมิ -40 ถึง 120 องศาเซลเซียส

ในการออกแบบวงจรออสซิลเลเตอร์แบบวงแหวนที่มีสัญญาณรบกวนต่ำ ใช้เทคนิคการไบอัสด้วยตัวเองบนโครงสร้างของอินเวอร์เตอร์แบบกระแสนิ่ง เพื่อลดสัญญาณรบกวนเชิงเฟส เนื่องจากสัญญาญรบกวน 1/f ร่วมกับเทคนิคสวิตซ์ไบอัส เพื่อลดสัญญาณรบกวน 1/f ในมอสเฟต วงจรออส

ซิลลเตอร์แบบวงแหวนถูกออกแบบโดยใช้ซีมอสเทคโนโลยีขนาด 0.35 ไมโครเมตร และใช้แรงดันไฟเลี้ยง 3.3 โวลต์ ผลการทดลองแสดงให้เห็นว่า วงจรออสซิลเลเตอร์แบบวงแหวนมีสัญญาณรบกวนเชิงเฟสต่ำเมื่อเทียบกับวงจรออสซิลเลเตอร์แบบวงจรแหวนแบบกระแสนิ่งทั่วไป

Thesis Techniques for Temperature-compensated and Low-noise CMOS RC Oscillators

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Thesis Ad-visor Assoc. Prof. Dr. Apinunt Thanachayanont

ABSTRACT

This dissertation describes circuit design techniques for CMOS temperature-compensated relaxation oscillator and low-noise ring oscillator. The proposed temperature compensation technique employs temperature-dependent circuit elements in a relaxation oscillator to compensate for frequency shifts due to changes in ambient temperature. The proposed temperature-compensated relaxation oscillator employs the current controlled topology with a resistive source-degenerated transconductor and a current comparator to achieve high oscillation frequency and low power dissipation. The relaxation oscillator was designed and optimized with process parameters from a standard 0.35-μm CMOS technology and a 2.5-V single power supply voltage. Post-layout simulation verified that the circuit achieved the oscillation frequency in the order of tens of MHz with Sub-100 $ppm/^oC$ frequency variation over a temperature range of -40 to $+120^oC$.

In the design of low-noise ring oscillator, a new self-biased current-starved inverter delay cell is proposed to reduce phase noise due to the up-converted $1/f$ noise. The self-biased delay cell incorporate the switched biasing technique to reduce MOSFET's $1/f$ noise. The proposed ring oscillator was designed by using process parameters from a standard 0.35-μm CMOS technology and a 3.3-V single power supply voltage. Simulation results showed that the proposed ring oscillator exhibited lower phase noise comparing to the conventional current-starved ring oscillator.

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Chapter 1

Introduction

1.1 Motivation

This dissertation is concerned with the design of CMOS temperature-compensated relaxation oscillator and low-noise ring oscillator. Emerging short-range, low-cost, and low-power wireless communication systems, such as wireless sensor and body area networks [1, 2], have relaxed performance requirements for radio transceivers. These systems have recently prompted research and development of highly stable and accurate integrated oscillators as a replacement of the reliable quartz crystal oscillators. For a reference frequency of less than 100 MHz, relaxation oscillators, ring oscillators, and the Wien bridge oscillators can be employed to achieve high frequency stability and low power dissipation.

The oscillation frequency practically varies with process parameters, power supply voltage, and temperature. The frequency variations due to power supply voltage can be minimized by using a voltage regulator, while the variations due to process parameters can be compensated by trimming of resistors and capacitors. Thus, the temperature stability of oscillation frequency is very critical during operation in order to minimize timing uncertainty. The temperature stability of f_{osc} of the relaxation oscillator is typically due to the temperature dependence of RC time constant and the delay times of comparator and flip-flops.

Oscillators are key building blocks in integrated transceivers, which consist of the receiver and transmitter. The receiver front-end selects, amplifies and converts the desired high-frequency signal to baseband. At baseband the signal can then be converted into the digital domain for further data processing and demodulation. The transmitter front-end converts an analog baseband signal to a suitable high-frequency signal that can be transmitted over the wired or wireless channel. Given the wide range of applications of wireless transceivers, oscillator specifications differ greatly for each transceiver. The challenge for the oscillator designer is to find the right oscillator topology and to define its dimensions in a limited time, so that the oscillator meets the requirements imposed by the transceiver in which it is embedded.

This research work investigates the circuit design techniques for CMOS temperature-compensated relaxation oscillator and low-noise ring oscillator.

1.2 Scope

This dissertation is involved with the theory, analysis and design of CMOS temperature-compensated relaxation oscillator and low-phase noise CMOS ring oscillator.

The first part of this research is concerned with the design of a CMOS relaxation oscillator with oscillation frequency above 20MHz and low power dissipation. A method of temperature-compensated biasing is adopted to achieve very low frequency variation over a wide range of temperature. For many applications, such as implantable biomedical electronics or wireless body area networks, the accuracy requirements of the frequency reference are much less stringent and, in the order of a few hundred $ppm/^oC$. Thus it is feasible to use a well-designed relaxation oscillator to replace crystal oscillator for frequency reference generation.

Ring oscillators are key building blocks in integrated transceivers and can be used as a voltage controlled oscillator (VCO) in low-power frequency synthesizer . The second part of this research is focused on the design of a low noise CMOS ring oscillator.

1.3 Outline of the dissertation

This dissertation is a compilation of several experimental investigations. Each major investigation is designed to refine techniques for low phase noise and high frequency stability of oscillators. The dissertation is organized into five chapters.

Chapter 1 presents the motivation, scope and outline of the dissertation.

Chapter 2 covers some of the basic and background theories related to this dissertation .

Chapter 3 describes the design and simulation results of the proposed temperature-compensated CMOS relaxation oscillator. It also points out the design optimization issues for low frequency variation relaxation oscillator.

Chapter 4 describes the design and simulation of a low-phase noise CMOS ring oscillator. The ring oscillator was fabricated in a $0.35\mu m$ CMOS technology and measurement results are reported.

Chapter 5 describes the conclusion of the dissertation.

Chapter 2

Integrated RC Oscillators

This chapter describes with the general principles for analysis and design of oscillator circuits. The chapter is organized as follows. The basic theory and principle of oscillators are described in section 2.1 Section 2.2 and 2.3 describe the types and the characteristics of oscillator circuits, respectively. Conclusion is given in section .

2.1 Basic theory of oscillators

Oscillators can basically be characterized and modeled by using a linear feedback system. Figure 2.1 depicts a linear feedback model of a oscillator circuit, which consists of an amplifier $H(j\omega)$ and a frequency-selective network $\beta(j\omega)$ connected in a positive feedback loop. A simple analysis shows that the transfer function of the feedback system can be written as

$$\frac{Y_{out}(j\omega)}{X_{in}(j\omega)} = \frac{H(j\omega)}{1 - H(j\omega)\beta(j\omega)} \tag{2.1}$$

where $H(j\omega)$ is transfer function of the amplifier and $\beta(j\omega)$ is the transfer function of the frequency selective network. Let us define the loop gain $L(j\omega)$ as

$$L(j\omega) = H(j\omega)\beta(j\omega) \tag{2.2}$$

According to the standard oscillator definition, this system must have a finite output even in the absence of an input signal. From the above equations, it is easily seen that this condition occurs if the transfer function in (2.1) converges to infinity at a specific frequency, implying that the loop gain $L(j\omega)$ should be equal to one at this frequency. Thus the magnitude of the loop gain should be equal to unity and the phase of the loop gain should be an integer multiple of 2π for the feedback loop to provide stable oscillation. The necessary conditions for steady-state oscillation are known as the "Barkhausen conditions". The first condition is known as the "gain condition" and specifies that the loop gain must be unity. The gain condition for steady state oscillation states can be written as

$$|H(j\omega)\beta(j\omega)| = 1 \tag{2.3}$$

The second condition is known as the "phase condition", which is expressed as

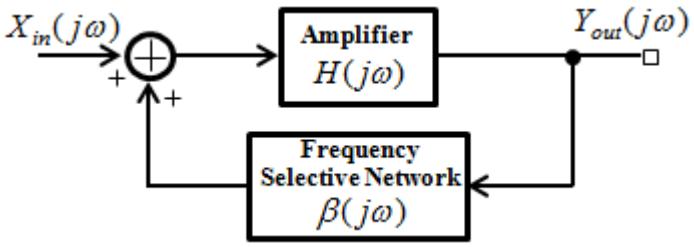


Figure 2.1: Block diagram of the feedback model for analyzing oscillation conditions.

$$\angle H(j\omega)\beta(j\omega) = (2m+1)\cdot 180^{\circ} \tag{2.4}$$

which states that the total open-loop phase shift must be $(2m+1)$ times 180 degrees where m is an integer value including zero. This leads one to the conclusion that the frequency stability of an oscillator depends on how the phase characteristic of the loop varies with frequency as described in Section 2.3.

2.2 Type of RC oscillators

Integrated RC oscillator can be classified into two categories: 1) relaxation oscillators and 2) ring oscillators. The principles and operations of the two types of oscillators will be described in this section.

2.2.1 Relaxation Oscillators

CMOS relaxation oscillators can be classified into two categories: 1) RC relaxation oscillators and 2) constant-current oscillators. This section describes the architecture and circuit operation of both types of relaxation oscillators.

RC relaxation oscillators

A simplified circuit of an RC relaxation oscillator is illustrated in Fig. 2.2. It consists of two resistors (R_1, R_2), a capacitor (C_1), a comparator, and a switch (S_1). The operation of the RC relaxation oscillator is based on charging and discharging the capacitor by using the resistors. The resistors and capacitor set the timing of charging and discharging processes. The switch S_1 can be realized with a MOSFET. The comparator is usually realized with a level-detecting circuit with hysteresis (i.e. a Schemitt trigger). The symbol and the characteristic of the Schmitt trigger are shown in Fig. 2.3. The output voltage of the Schmitt trigger changes from low to high when the input voltage exceeds the upper switching threshold voltage (V_B). The output voltage of the of the Schmitt trigger changes from high to low when the input voltage decreases below the lower switching threshold voltage (V_A), where $V_A < V_B$. The hysteresis voltage of the comparator is equal to $V_B - V_A$.

The operation of the RC relaxation oscillator can be described as follows: Consider when V_{out} is low and the switch S_1 is open, the capacitor C_1 is charged via R_1 and the voltage across the capacitor V_{o1} rises exponentially toward V_{DD} with a time constant of the charging period is the time constant τ_1, where

$$\tau_1 = R_1 C_1 \tag{2.5}$$

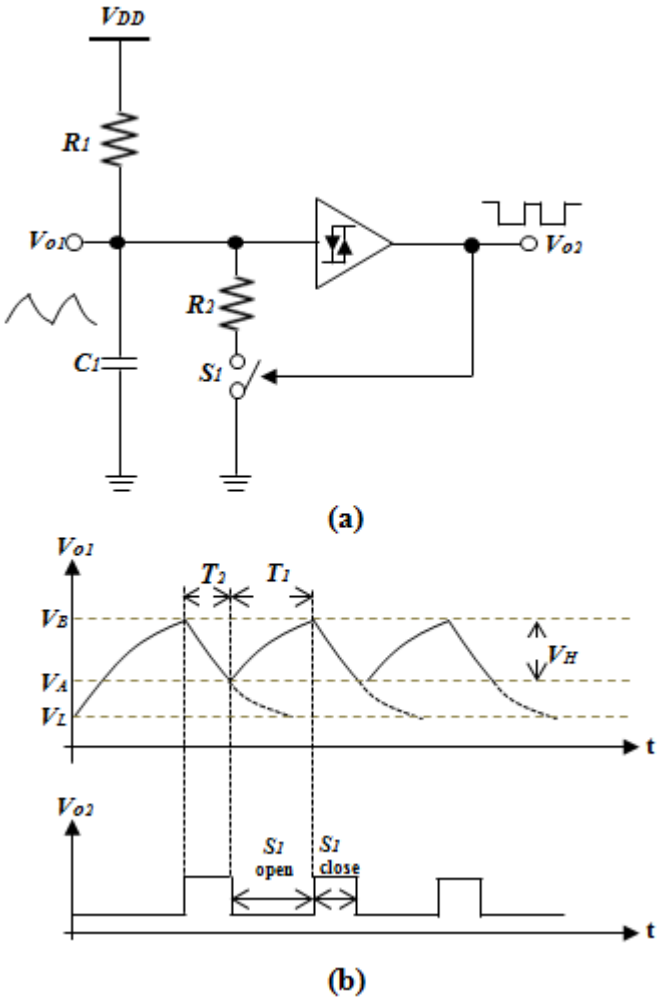


Figure 2.2: A simplified circuit of an RC relaxation oscillator. (a) generalized circuit configuration, and (b) output wave forms.

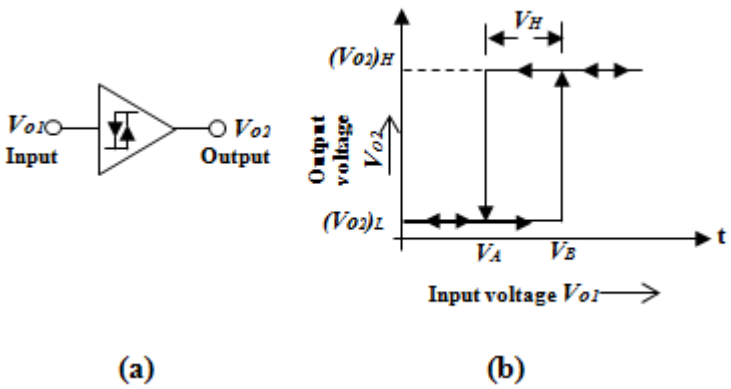


Figure 2.3: Circuit symbol and voltage transfer characteristics of a Schmitt trigger: (a) Circuit symbol; (b) Transfer characteristics.

When V_{o1} reaches the upper threshold voltage V_B of the comparator, the output voltage changes from low to high and the switch S_1 is closed. The voltage across the capacitor now decays toward

a lower voltage level V_L, where

$$V_L = V_{DD}\frac{R_2}{R_1+R_2} \tag{2.6}$$

with a time constant, τ_2, where

$$\tau_2 = (R_1||R_2)C_1 \tag{2.7}$$

If the resistor values R_1 and R_2 are chosen such that $V_L < V_A$, then when V_{o1} reaches V_A the comparator output voltage will change from high to low and the switch S_1 will open. The capacitor C_1 is then charged up toward V_{DD} again and the cycle is repeated. Figure 2.2(b) demonstrates the periodic output waveforms of the RC relaxation oscillator, assuming that S_1 is closed when the output of comparator is high. The time T_1 for V_{o1} to change from the lower threshold V_A to the upper threshold V_B can be expressed as

$$T_1 = \tau_1 ln\left(\frac{V_{DD}-V_A}{V_{DD}-V_B}\right) \tag{2.8}$$

Similarly, the time T_2 for V_{o1} to decay from V_B to V_A can be given as

$$T_2 = \tau_2 ln\left(\frac{V_B-V_L}{V_A-V_L}\right) \tag{2.9}$$

Thus, the total period of oscillation T is equal to T_1+T_2, and the frequency of oscillation f can be given as

$$f = \frac{1}{T} = \frac{1}{T_1+T_2} \tag{2.10}$$

or

$$f = \frac{1}{R_1C_1}\left[ln\left(\frac{V_{DD}-V_A}{V_{DD}-V_B}\right)+\frac{R_2}{R_1+R_2}ln\left(\frac{V_B-V_L}{V_A-V_L}\right)\right]^{-1} \tag{2.11}$$

In the design of the RC relaxation oscillator, the performance of the comparator is very critical since the accuracy and stability of the threshold levels of the comparator are directly related to the frequency stability and accuracy of the oscillator. Two commonly used comparator configurations in CMOS relaxation oscillator designs are the single-comparator and the dual-comparator Schmitt trigger circuits.

Figure 2.4 shows the simplified circuit diagram of the RC relaxation oscillator using the single comparator Schmitt trigger . The operation of the oscillator can be explained as follows. Assuming that S_1 and S_2 are open initially, the capacitor C_1 are charged exponentially toward V_{DD} and when the capacitor voltage V_{o1}reaches the upper threshold voltage V_B, the comparator output voltage will change from low to high, thus setting the flip-flop and causing the switches S_1 and S_2 to close. The upper threshold voltage V_B of the comparator is set by the ratio of resistors, given by

$$V_B = V_{DD}\frac{R_B+R_C}{R_A+R_B+R_C} \tag{2.12}$$

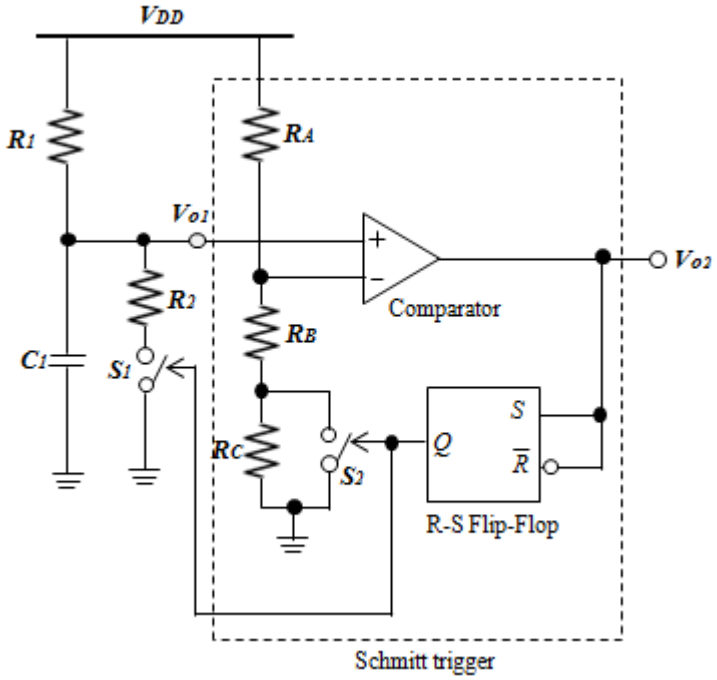


Figure 2.4: RC relaxation oscillator using single-comparator-type Schmitt trigger.

When S_2 is closed, the threshold setting resistor R_C is short circuited and the new threshold level V_A is generated as

$$V_A = V_{DD}\frac{R_B}{R_A + R_B} \tag{2.13}$$

where V_A is set to be lower than V_B. When S_1 is closed, the voltage across the capacitor C_1 decays exponentially until it reaches the lower threshold level V_A. The comparator output voltage then changes from high to low, thus causing the flip-flop to reset and S_1 and S_2 to open. The charging and discharging cycles are then repeated. The circuit oscillates by generating exponential ramp voltages across C_1, between two threshold levels V_A and V_B, as shown in Fig. 2.2(b). The hysteresis voltage V_H of the Schmitt trigger is primarily determined by the value of R_C, given by

$$V_H = V_B - V_A = V_{DD}\frac{R_A R_C}{(R_A + R_B + R_C)(R_A + R_B)} \tag{2.14}$$

The threshold voltages V_B and V_A as well as the hysteresis voltage V_H are proportional to the supply voltage V_{DD}. The charging currents available to C_1 are proportional to V_{DD} as long as R_1 is connected to V_{DD}. Thus as V_{DD} is increased, the hysteresis voltage V_H, which determines the amplitude of V_{o1} , also increases, and the slope of exponential waveforms increases proportionally. Thus, the V_{DD} dependence cancels out and the frequency of oscillation is, to the first order, independent of the supply voltage as given by (2.11). However, the output amplitude is proportional to V_{DD}.

The drawback of the single-comparator configuration, as shown in Fig. 2.4, is that the switching of voltage levels across the bias setting resistor string, when the voltage swing reaches the threshold levels. The parasitic node capacitance across R_A, R_B and particularly R_C slow down the switching time of the circuit at high oscillation frequencies. This issue can be partially addressed with a dual-comparator Schmitt trigger configuration.

Figure 2.5 shows the simplified circuit diagram of the relaxation oscillator using a dual-comparator Schmitt trigger. The comparator 1 changes its output state when the voltage swing across the capacitor C_1 reaches

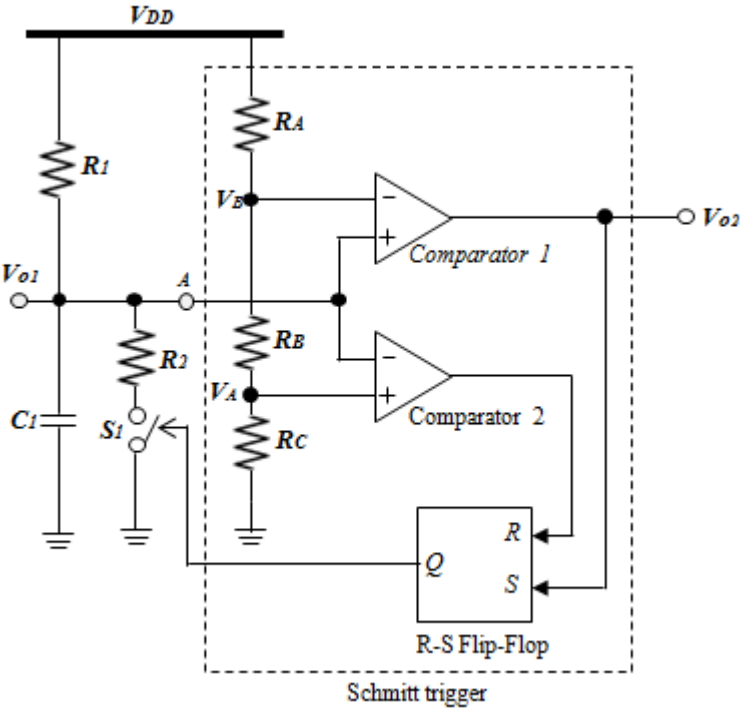


Figure 2.5: RC relaxation oscillator with dual-comparator-type Schmitt trigger.

the upper threshold voltage V_B, and the comparator 2 changes its output voltage when V_{o1} reaches the lower threshold voltage V_A. These threshold voltages are given by the resistor ratios as

$$V_B = V_{DD}\frac{R_B + R_C}{R_A + R_B + R_C} \tag{2.15}$$

When S_2 is closed, the threshold setting resistor R_C is short circuited and the new threshold level V_A is generated as

$$V_A = V_{DD}\frac{R_B}{R_A + R_B} \tag{2.16}$$

Thus the total hysteresis voltage V_H is given by

$$V_H = V_B - V_A = V_{DD}\frac{R_B}{(R_A + R_B + R_C)(R_A + R_B)} \tag{2.17}$$

When S_1 opens, V_{o1} rises exponentially toward V_{DD} and when it reaches V_B, the comparator 1 changes its output voltage from low to high. This sets the flip-flop which causes S_1 to close, and initiates the discharge cycle. When V_{o1} is reduced below the lower threshold voltage V_A , the comparator 2 changes its output voltage from low to high. This resets the flip-flop and opens S_1. The cycles are then repeated As described earlier, although V_A and V_B are dependent on V_{DD} this dependence is canceled out since the charging and discharging currents associated with C_1 are also proportional to V_{DD}. Thus, the frequency of oscillation is, to the first order, independent of the supply voltage and is given by (2.11).

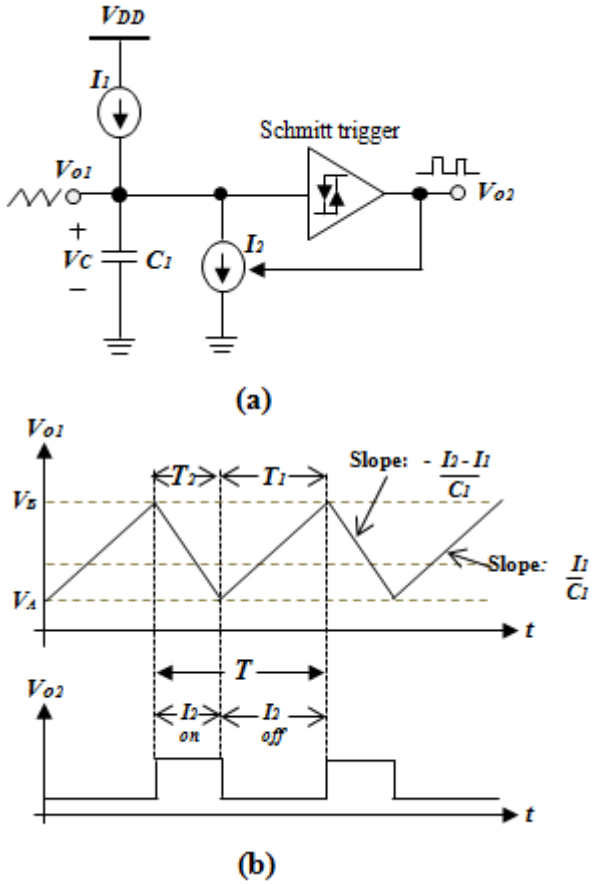


Figure 2.6: Constant-current charge and discharge oscillator (a) basic circuit configuration, and, (b) output waveform.

Constant-current relaxation oscillators

Figure 2.6 shows the basic circuit configuration of a constant-current relaxation oscillator. The circuit rely on current sources, rather than resistors, to charge and discharge a timing capacitor. The constant-current oscillator normally consists of two current sources. One current source, I_1, is always on, while the other current source, I_2, is turned on and off intermittently. When I_2 is turned off, the capacitor C_1 is charged with the constant current I_1 until the capacitor voltage V_{o1} reaches the upper threshold voltage V_B of the Schmitt trigger . The Schmitt trigger then changes its output from low to high, which turns the current source I_2 on. Assuming that $|I_2| > |I_1|$, the capacitor C_1 is then discharged with a net current of $I_2 - I_1$ until V_{o1} reaches the lower threshold voltage V_A. The Schmitt trigger then again changes sits output voltage from high to low, which turns the current source I_2 off. Therefore the circuit oscillates with the linear ramp waveforms as shown in Fig. 2.6(b).

The total time T_1 for the charging cycle is

$$T_1 = \frac{(V_B - V_A)C_1}{I_1} \tag{2.18}$$

Similarly, the total time T_2 for the discharge cycle is

$$T_2 = \frac{(V_B - V_A)C_1}{I_2 - I_1} \tag{2.19}$$

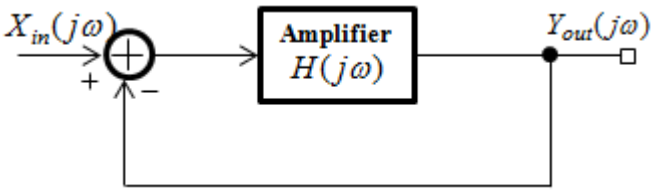


Figure 2.7: Ring oscillator block model.

The frequency of oscillation f is written as

$$f = \frac{1}{T} = \frac{1}{T_1 + T_2} = \frac{I_1}{(V_B - V_A)C_1}\left(1 - \frac{I_1}{I_2}\right) \tag{2.20}$$

Usually, such an oscillator sets $I_2 = 2I_1$, then both the charge and discharge currents for the timing capacitor would be equal, and the output waveform V_{o1} becomes a triangle wave with frequency f,

$$f = \frac{I_1}{2(V_B - V_A)C_1} \tag{2.21}$$

where $V_B - V_A = V_H$ which is the hysteresis voltage of the Schmitt trigger. Then, the frequency, f can be expressed as

$$f = \frac{I_1}{2V_H C_1} \tag{2.22}$$

Note that the Schmitt trigger output V_{o2} is a symmetrical (i.e., 50% duty cycle) square wave.

In [3] and [4], the authors experimented with the constant-current relaxation oscillators. These oscillators are performed by iteration of charging and discharging the capacitor C as applied negative feedback using a frequency-to-voltage converter or a feedback mechanism that monitors the capacitor voltage swing and dynamically adjusts the threshold levels such that the voltage swing and thus the period of oscillation remains constant. The constant-current relaxation oscillators are the focus of this dissertation because of their simple circuit, low current consumption, and, small silicon area. These features thus make the constant-current relaxation oscillators suitable for embedding in a battery-operated low power system.

2.2.2 Ring Oscillators

A ring oscillator consists of a number of amplifier stages connecting in a negative feedback loop as shown in Fig. 2.7 The ring oscillator does not contain any frequency selective network. The lack of a high-Q selective network generally makes the ring oscillator harder to achieve the lowest noise and highly stable frequency performance However, the design of ring oscillators is straightforward by using integrated circuit design techniques. Other properties of ring oscillators, such as the availability of multiple phases at the output and the wide tuning range can be useful for some specific applications including frequency synthesizers and oversampling circuits. These characteristics of ring oscillators lead to the conclusion that they are still important in modern integrated communications systems.

A behavioral model of an N-stage ring oscillator is shown in Fig. 2.8. The gain of an N-stage ring oscillator is determined as

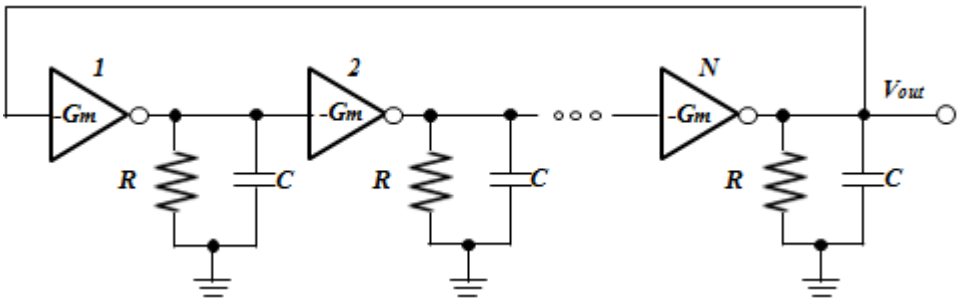


Figure 2.8: Linearized model of a N-stage ring oscillator.

$$H(j\omega) = [\frac{-G_m R}{1+RCj\omega}]^N \tag{2.23}$$

According to Barkhausen criteria the ring oscillator is operative when the following conditions are satisfied $|H(j\omega)| = 1$. The oscillation frequency of an N-stage ring oscillator is determined by the phase condition for oscillation as given by

$$\angle H(j\omega) = -N \cdot (arctan(\omega RC)) = \theta \tag{2.24}$$

Solving $\angle H(j\omega) = -\pi$, lead to the oscillation frequency for an N-stage ring oscillator

$$\omega = \frac{tan\theta}{RC} \tag{2.25}$$

and the minimal single stage gain is

$$G_m R \geq \frac{1}{cos\theta} \tag{2.26}$$

Then, for the three-stage ring oscillator can be shown in Fig. 2.8 (when $N = 3$). The inverters are modeled by a transconductor and an RC circuit. With a simple circuit analysis, the open-loop transfer function of the linearized model for the three-stage ring oscillator is found to be

$$H(j\omega) = [\frac{-G_m R}{1+RCj\omega}]^3 \tag{2.27}$$

In the oscillatory system, $|H(j\omega)| = 1$, which results in

$$\omega = \frac{\sqrt{3}}{RC} \tag{2.28}$$

$$G_m R = 2 \tag{2.29}$$

This system will oscillate if (2.29) is satisfied and the oscillation frequency is dictated by (2.28). To achieve oscillation, the ring oscillator must provide a phase shift of 2π and have unity voltage gain at the oscillation

frequency. Each delay stage must provide a phase shift of π/N, where N is the number of delay stages. The remaining π phase shift is provided by a DC inversion. This means that for an oscillator with single-ended delay stages, an odd number of stages are necessary for the DC inversion. If differential delay stages are used, the ring can have an even number of stages if the feedback lines are swapped.

A basic ring oscillator consists of an odd number N of inverter stages connected in a negative feedback loop. Therefore, if one of the nodes is excited, the pulse will propagate through all stages and will reverse the polarity of the initially excited node. The most common way to determine the frequency of oscillation of the ring oscillator is to assume each stage provides a time delay of t_d. The difficulty in obtaining a value for the frequency arises when trying to determine t_d, mainly due to the non-linearity and parasitic of the circuit. Moreover, the value of the frequency also depends on the topology used for the delay stage. Even with a circuit that appears as simple as this one, many assumptions and simplifications are necessary to obtain a value for t_d. Therefore, numerous equations exist for determining the oscillation frequency of a VCO, each derived with a separate set of assumptions and simplifications. Most of these derivations use a common set of parameters to find a relationship of the time delay, t_d. Due to the signal goes through each of the N delay stages once to provide the first π phase shift in a time of $N \cdot t_d$. Then, the signal must goes through each stage a second time to obtain the remaining π phase shift, resulting in a total period of $2 \cdot N \cdot t_d$. Therefore, the frequency can then be solved for in (2.30) and (2.31) , resulting in an analytical expression for improving the frequency stability.

$$f_{osc} = \frac{1}{2 \cdot N \cdot t_d} \tag{2.30}$$

In general, the time delay of amplifier stage is related to its current-driving ability, its output voltage swing and the load capacitance. A simple analysis can show that the time delay is given by

$$t_d = C_L V_{osc} / I_c.$$

where V_{osc} is the output voltage swing, I_c is the output current provided by the amplifier stage, and C_L is the load capacitance. Thus the oscillation frequency is given by (2.31)

$$f_{osc} = \frac{I_c}{2 \cdot N \cdot V_{osc} \cdot C_L} \tag{2.31}$$

A classification of CMOS ring oscillators can be identified by the type of signal in the ring delay stage into two general types: 1) single-ended, 2) true differential. This section describes the architecture and circuit operation can be explained as follows. .

Single-ended ring oscillators

A single-ended ring oscillator is shown in Fig. 2.9, which composes of an odd number of inverter delay stages

The ring oscillator in Fig 2.9 does not include any means to control the oscillation frequency. A control method can be added in various ways, such as by changing the strength of inverters in the loop, by changing the loads, or by varying V_{DD}. Fig. 2.10 shows an implementation where the strength of inverters is changed by adding two more transistors, M_3 and M_4, to the inverter structure , which is called the current-starved inverter. The load tuning of M_3 and M_4 need to implement the bias circuit to control the drain current, I_c in CMOS inverters. Single-ended structures are usually preferred over the differential architectures whenever simplicity is essential. They are also desirable when power dissipation is the most important consideration since they include less number of active elements that dissipate power. Although power supply control can be used for both single-ended and differential ring oscillator architectures, use of low power supply voltages results in

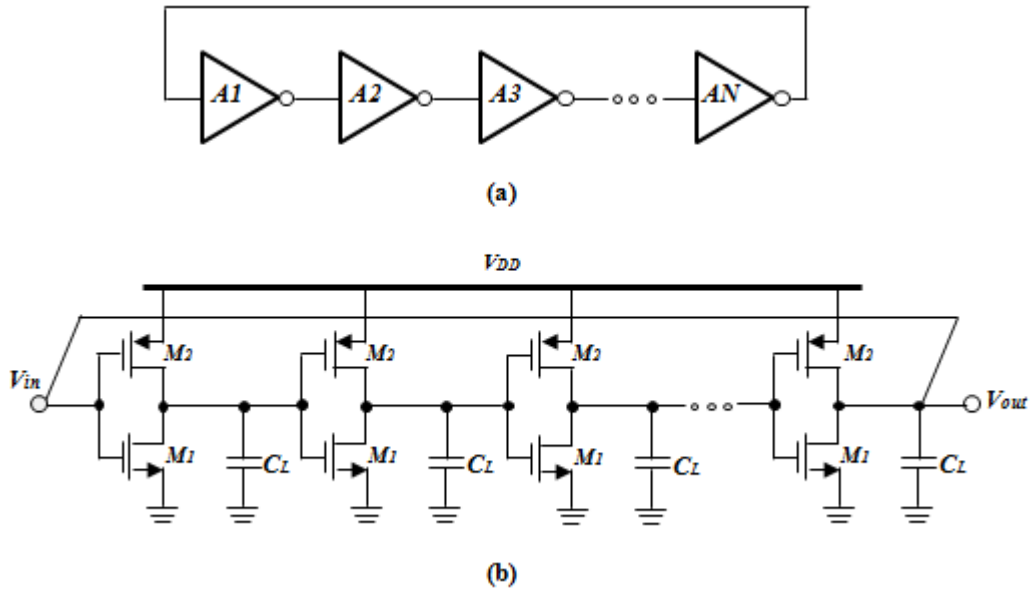


Figure 2.9: (a) Single-ended ring oscillator structure, (b) Inverter stages.

smaller output swings. This results in a reduction in the phase noise performance and the oscillators get more susceptible to supply and ground disturbances.

The advantage of a single-ended ring oscillator that is the power efficiency due to the delay stage only draws power when there is a signal transition, in contrast to true differential stages which require a bias current that is always owing whether or not the signal is in transition. Therefore, it is the best choice for the design of low power ring oscillator. Susceptibility to supply, substrate interference and constraint on number of stages are the disadvantages of single-ended ring oscillator, which resulted in phase noise of ring oscillator as explained in Chapter 3.

True differential ring oscillators

Figure 2.11 (a) shows an example of a ring oscillator with a true differential signal in the ring, which is the differential ring oscillator structure and the simplest differential pair structure with resistor, R_L loads (Fig. 2.11 (b)). Here the distinguishing factor is that the signal in the ring is defined differentially. “True" refers to a differential gate circuit that provides some measure of common mode rejection, such as the differential pair with current source bias, I_{TAIL}.Figure 2.11 (c), the differential ring oscillator with active loads biased in the saturation region, which the differential ring oscillator with symmetrical active loads, which consists of a PMOS transistor pair. One PMOS device is biased in the triode region with an additional bias circuitry, while the other is a diode-connected transistor biased in the saturation region. This load provides symmetrical I-V characteristics and an amplitude control option through V_{bias}, which is used to change the resistance of the triode-region transistors. This way, the output swing is kept between V_{dd} and V_{bias}.

Differential ring oscillators can be constructed with an even number of stages, unlike their single-ended counterparts. The delay of the differential stage in Fig. 2.11 can be written as

$$T_d = \frac{C_L V_{sw}}{I_{cotrl}} \tag{2.32}$$

where C_L is the total load capacitance at each output node, V_{sw}, is the voltage swing at the output, and I_{contrl} is the mirrored current or a tail current. Therefore, the oscillation frequency of an N-stage ring oscillator

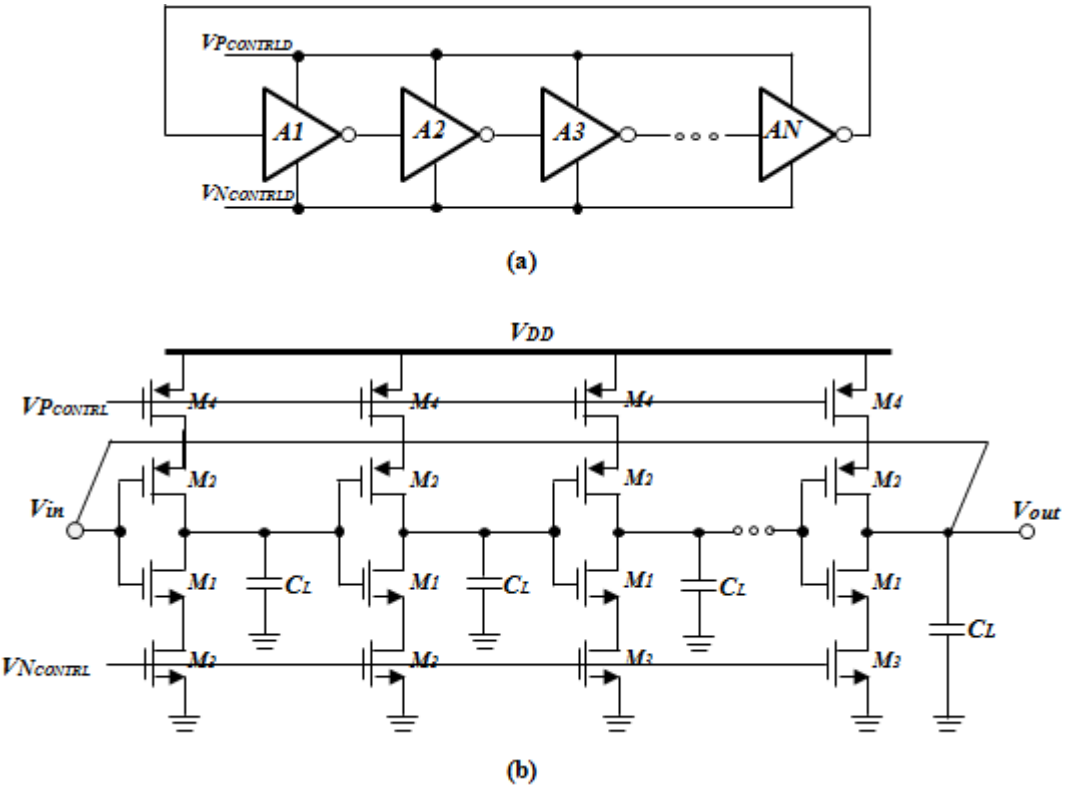


Figure 2.10: (a) Single-ended structure, (b) Current starved inverter stages.

employing this stage is

$$f_{osc} = \frac{I_{cotrl}}{2 \cdot N \cdot C_L V_{sw}} \tag{2.33}$$

Equation (2.32) and (2.33), one can see that the oscillation frequency of the oscillator can be controlled linearly by varying the mirrored current.

The advantages of the true differential approach that is a number of stages due to both phases of the signal are available, the number of stages in the ring is not restricted to be odd. A wire inversion can be used to meet the oscillation criterion and an even or odd number of stages can be used. In addition to the differential circuitry offers the possibility of good common mode rejection. If symmetric layout and good circuit design practices are observed, the amplitude coupling interference mechanism, which is a common mode signal and does not act the differential signal. This can be seen from considering the simplified waveforms in Fig. 2.12. The switching threshold time t_{SW} for the case with no noise (dashed lines in the grue) occurs when the differential signal crosses zero. With interference from the supply voltage variation V_{DD}, an output voltage change v_o is coupled to both outputs. Since the switching threshold time t_{SW} is defined when the differential signal crosses zero, the common mode interference signal does not affect t_{SW} . To realize the benefits of fully differential signals, it is necessary to minimize delay modulation due to supply and substrate coupling to the differential signal delay.

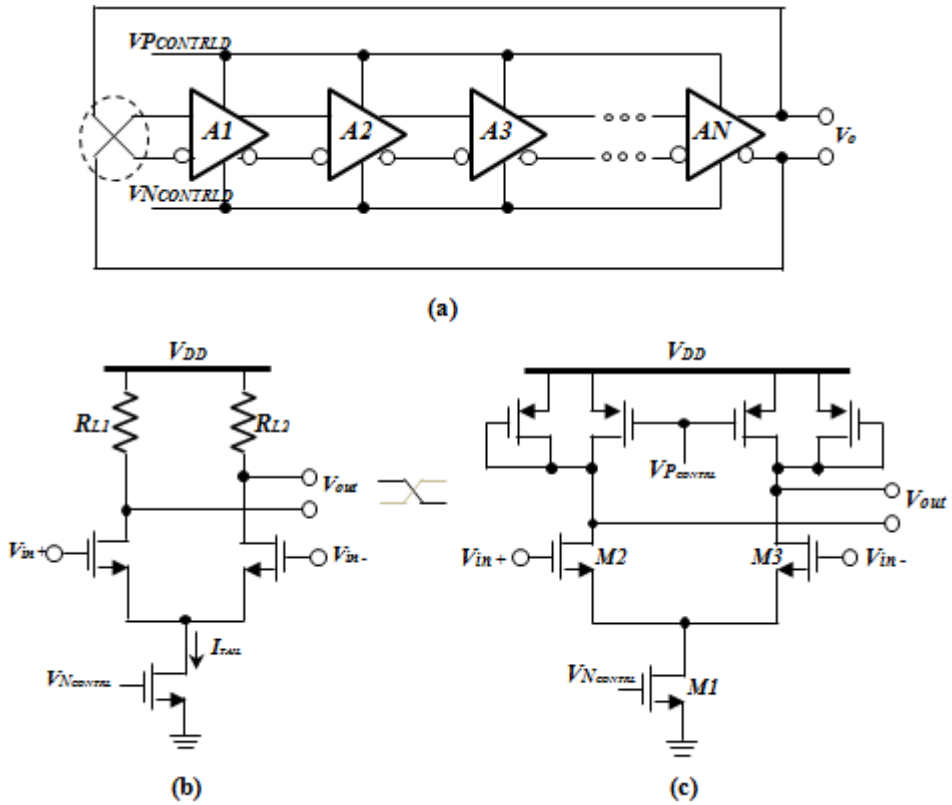


Figure 2.11: (a) Differential ring oscillator structure, (b) Simple differential pair stages, (c) Differential pair with symmetrical loads.

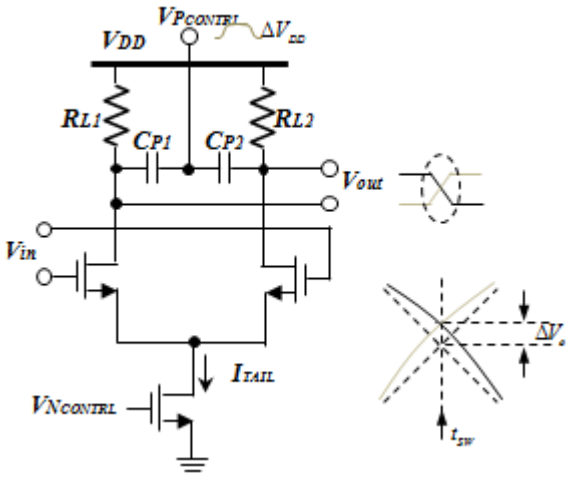


Figure 2.12: Amplitude coupling interference to true differential signal.

2.3 Characteristics of Oscillators

The basic function of an oscillator is to generate a periodic signal with certain properties. All oscillators in the classification are feedback systems and in most instances feedback modeling is used to assess the oscillation conditions. The feedback model is used throughout this work and is discussed extensively in the next subsection.

2.3.1 Characterization and Frequency Stability of an Oscillator

The output signal of an sinusoidal oscillator can be expressed as

$$v_{out}(t) = A(t) \cdot cos\left(\omega_o t + \phi\left(t\right)\right) \tag{2.34}$$

where v_{out} represented a output voltage, $A(t)$ and $\phi(t)$ are the instantaneous amplitude and phase, respectively. The time derivative of the instantaneous phase can be described in term of the instantaneous angular frequency as given by

$$\omega(t) = \omega_o + \frac{d\phi(t)}{dt} \tag{2.35}$$

In an ideal oscillator, the angular frequency is a constant, ω_o while the phase is an ideal ramp given by $\omega_o t$, due to the integration. Consider, for frequency derived from the nominal frequency of oscillation in a voltage controlled oscillator (VCO), is linearity proportional to the control voltage. Thus, its phase derivation is proportional to the integral of the input control voltage.

For the instantaneous angular frequency of (2.35) can be re-written as

$$\omega(t) = \omega_o + \frac{d\phi(t)}{dt} = \omega_o + \Delta\omega(t) \tag{2.36}$$

where $\Delta\omega(t)$ represents the random instantaneous angular frequency fluctuations. Of course, for high-quality oscillator:

$$|\Delta\omega(t)| \ll \omega_o \tag{2.37}$$

A useful parameter is the instantaneous fractional frequency fluctuation $y(t)$ defined (2.38) which is divided the phase by ω_o.

$$y(t) = \frac{\frac{d\phi(t)}{dt}}{\omega_o} = \frac{\Delta\omega(t)}{\omega_o} = \frac{\Delta f(t)}{f_o} \tag{2.38}$$

The fractional frequency fluctuation $y(t)$ is a random quantity. Also, it allows for easier comparison of frequency stability among oscillators having different nominal frequencies. Therefore, this dissertation is concerned with the random fractional frequency fluctuation $y(t)$ of oscillators. The Fast Fourier Transforms (FFTs) is used to analyze power spreading in the frequency domain of statistical parameter of $y(t)$ to obtain the frequency stability characteristics.

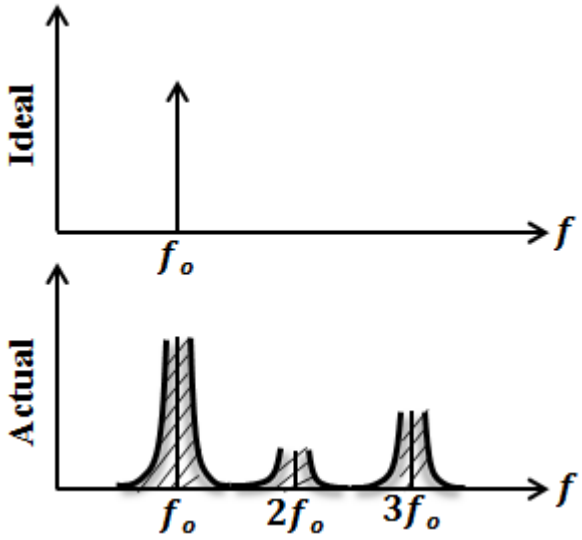


Figure 2.13: The spectrum of an ideal and a practical oscillator.

2.3.2 Phase Noise

In an ideal oscillator, an oscillator signal can be expressed as

$$v_{out}(t) = A_0 cos(2\pi f_o t + \phi(t) + \varphi(t)) \tag{2.39}$$

where the amplitude A_0, the frequency f_o, the instantaneous phase $\phi(t)$ and the random instantaneous phase fluctuations $\varphi(t)$, are all constants. The one-side spectrum of an ideal oscillator with no random fluctuations consists of an impulse at f_o as shown in Fig.2.13. In practical oscillator, the spectrum exhibits "skirt" around the center or "carrier" frequency (Fig.2.13). [5]

Phase noise is usually characterized in frequency domain. The random fluctuations in a signal manifests itself as phase noise is presented in the frequency domain . To quantify phase noise, we consider a unit bandwidth at an offset $\Delta f(t)$ with respect to f_o and calculate the noise power within this unit bandwidth, and divide the result by the carrier power. However, the fluctuations that result to phase noise are considered in a periodic function with period 2π. As there are many ways of quantifying these fluctuations (e.g. a comprehensive review of different standards and measurement methods is given in [5]). An oscillator's short-term instabilities are usually characterized in term of the single sideband noise spectral density. It has a unit of decibel below the carrier per hertz (dBc/Hz) and is defined as

$$\mathscr{L}_{\text{total}}\{\Delta f\} = 10log\left[\frac{P_{sideband}(f_o + \triangle f, 1Hz)}{P_{carrier}}\right] \tag{2.40}$$

where $P_{sideband}(f_o + \triangle f, 1Hz)$ represents the single sideband power at a frequency offset Δf from the carrier in a measurement bandwidth of $1 - Hz$, and $P_{carrier}$ is the total power under the power spectrum. Note that the definition of (2.38) includes the effect of phase fluctuations $\varphi(t)$ as shown in Fig.2.14(a). Generally, if the $P_{carrier}$ is greatly larger than $P_{sideband}(f_o + \triangle f, 1Hz)$, the phase noise would get better. However, it has many methods that can increase the $P_{carrier}$, e.g. increasing the power supply level (or power supply voltage) which increases the power consumption.

Figure 2.14(b) presents the phase noise spreads some of the power of the oscillator to neighboring frequencies, creating phase noise sidebands. The sidebands are shown falling off as $1/\Delta f^2$ for frequencies far enough away

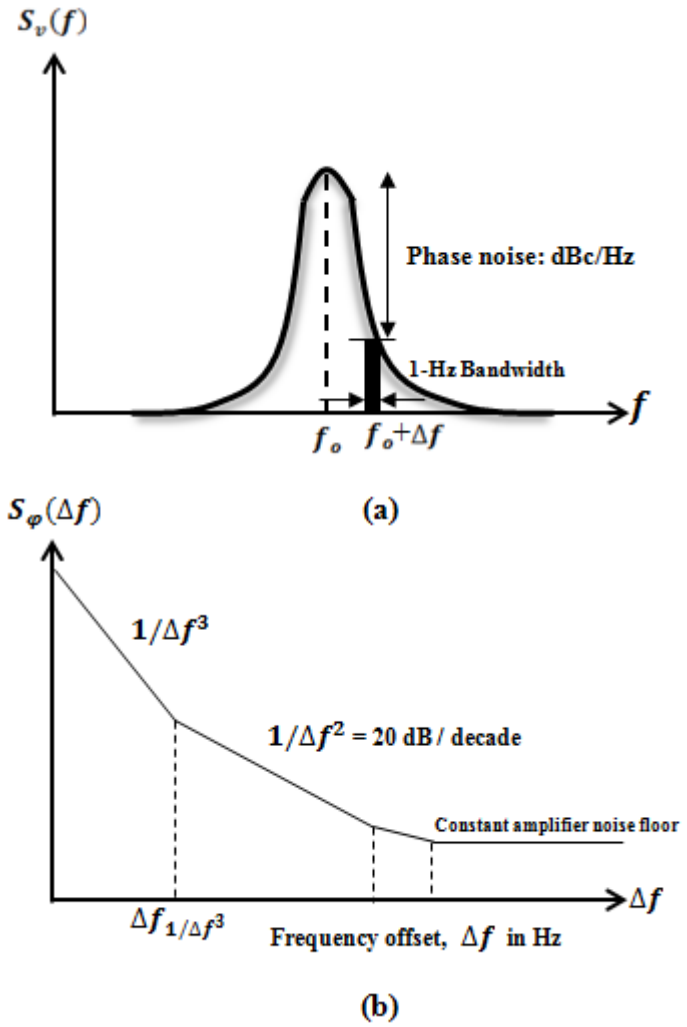


Figure 2.14: The phase noise per unit bandwidth in an oscillator (a) power spectrum of oscillator (b) phase fluctuation power spectral density.

from the carrier. The frequency, Δf is the offset frequency from the center. Phase noise of an oscillator at a given offset, is calculated from the ratio of the power in a 1-Hz bandwidth at the offset frequency, to the total power of the carrier. Figure 2.14(a) this would be the ratio of the area of the rectangle with 1-Hz bandwidth at offset Δf, to the total area under the power spectrum curve. The spectrum in Fig. 2.14(a) is the power spectrum of an oscillator with a noisy phase angle. The spectrum of the phase fluctuations themselves can also be shown, as in Fig. 2.14(b). The spectrum in 2.14(b), is that of the noisy phase angle term, $\varphi(t)$, and is called the spectral density of phase fluctuations. For offsets sufficiently far from carrier, the phase noise in dBc/Hz measured from the power spectrum in Fig. 2.14(a) is equal to the value of the spectral density of phase fluctuations in Fig. 2.14(b). The spectrum in Fig. 2.14(b) is shown on a log-log scale, with phase noise sidebands that fall as $1/\Delta f^2$, or 20-dB/decade. The $1/\Delta f^2$ region is referred to as the "white frequency" variation region, since it is due to white, or uncorrelated, fluctuations in the period of the oscillator. The behavior in this region is dominated by the thermal noise in the devices of the oscillator circuit. For low enough offset frequencies the flicker noise of devices generally comes into play and the spectrum in this region falls as $1/\Delta f^3$.

Also worth noting, the sidebands in Fig. 2.14(b) grow towards infinity as the offset frequency approaches zero. This is consistent with the behavior expected for timing jitter in free-running oscillators, and will be described shortly.

Phase Noise with FOMs

Design figure-of-merits ($FOMs$) compare an estimation of a performance aspect of an oscillator with its functional specification. The design margin is indicated by the value of the FOM. At the cost of reduced accuracy, relatively simple first-order calculations can be used to formulate design $FOMs$. In other words, the complexity of the design FOM is reduced at the cost of some accuracy. Once all important design FOM are defined and evaluated for several oscillator topologies, for example the design FOM concerning frequency, temperature coefficient and the phase noise, $\mathscr{L}(f)$, these topologies can be ranked on the basis of the design FOM values. Design FOM of oscillator topologies provide qualitative insight concerning the relations between the design parameters, and quantitative insight when evaluated.

Equation (2.39), the random phase fluctuations, $\varphi(t)$ is a stochastic variable and it one side power spectrum density of phase fluctuations is $S_\varphi(f)$ which it is difficult to measure directly. Normally, $S_{v_{out}}(f)$ is measured, being the power spectrum density of v_{out}. The power density $S_{v_{out}}(f)$ versus frequency can be directly read form the analyzer display. Base on this measurement, $S_\varphi(f)$ of an oscillator is characterized by the single-sideband (SSB) phase noise to carrier ratio at offset frequency from the carrier frequency f_{osc}. The phase noise measurement is defined in equation of

$$\mathscr{L}(f) = 10log\left[\frac{P_{\varphi-sideband}(f_{osc}+\triangle f, 1Hz)}{P_{signal}}\right]. \tag{2.41}$$

The design margin is indicated by the value of the Figure of Merit (FOM) to compare an estimation of a performance aspect of an oscillator with its functional specification. Once all important design $FOMs$ are defined and evaluated for several oscillator topologies, for example the design $FOMs$ concerning frequency and phase noise can be indicated the performance of $1/f^2$ phase noise in an oscillator by

$$FOM_3 = \mathscr{L}(f) + 10log\left(\left(\frac{\Delta f}{f_o}\right)^2 \cdot \frac{P_{diss}}{1mW}\right). \tag{2.42}$$

where P_{diss} is the power consumed by the oscillator core. Design $FOMs$ of oscillator topologies provide qualitative insight concerning the relation between the design parameters, and qualitative insight when evaluated.

2.3.3 Frequency Tuning and Controlled Linearity

Frequency tuning are important specifications that can achieve a significant impact on designing of an oscillator. In general, the most oscillators need to specify to cover a band of interest around a center frequency. Several applications are usually show the center frequency, absolute tuning range which it means the minimum and maximum frequency that these applications can operate frequency in this range. As for any specification, the tuning range specification must be met under worst case conditions. Therefore frequency deviations due to temperature changes, process spread and power supply variations should be added to the tuning range.

Considering a very simplified model of ring frequency as shown in Fig. 2.15, which is the scheme for classification by tuning method. For an N-stage ring, the frequency is given by 2.30, can be rewritten by

$$f_{osc} = \frac{1}{2 \cdot N \cdot T_d} \tag{2.43}$$

Note that, the frequency is tuned by changing either the number of stages. In either case, the tuning can be discrete or continuous. For the stage delay, the gate input transition time approach zero, so that the output waveform begins its transition immediately. With this idealization, the output delay time T_d is given by

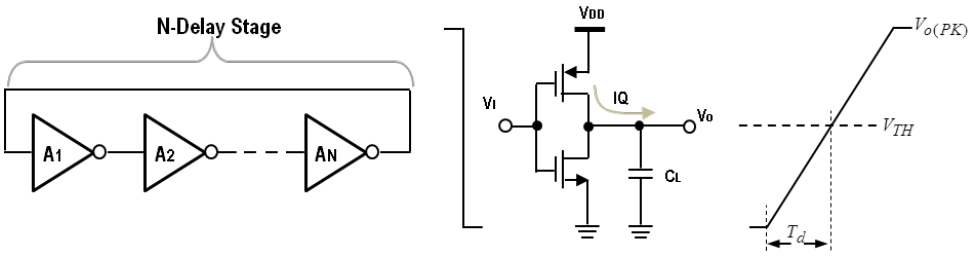


Figure 2.15: Simple model of ring frequency, stage delay.

$$\frac{I_0}{C_L} = \frac{V_{TH}}{T_d} \Rightarrow T_d = \frac{C_L V_{TH}}{I_0} \tag{2.44}$$

The frequency tuning can be changed the loading C_L, the drive strength I_0, or voltage V_{TH}. Moreover, the frequency tuning, respectively, ring oscillator can be varied a number of stages, loading, and drive strength voltage.

Suppose a ring oscillators are used for the voltage-controlled oscillators (VCOs)or the current-controlled oscillators (CCOs) so that they have a tuning constant K_{VCO} that is specified in Hz/V (or K_{CCO} in Hz/A). This constant will become larger if the tuning range is increased, to cover process spread for example. If the supply voltage decreases, in the case of a redesign using a newer CMOS technology for example, the tuning-voltage range will also decrease and thus K_{VCO} will increase. In practice, the tuning characteristic of an oscillator is a nonlinear function. Fig. 2.16(a) shows the typical tuning curve of VCO which a large part of the tuning range, K_{VCO} is equal to $\Delta f_1/\Delta V_1$. However, at the end of the tuning range, where parasitic start to dominate, K_{VCO} decreases ($\Delta f_2/\Delta V_2 < \Delta f_1/\Delta V_1$). Similarly, at the end the tuning range in Fig. 2.16(b), where parasitic start to dominate, K_{CCO} decreases ($\Delta f_2/\Delta I_2 < \Delta f_1/\Delta I_1$). In addition in Fig. 2.16(b), we can describe the controlled linearity by considering in the first order of oscillator analysis that the delay which is added to the period of oscillation, is dependent of the oscillator's control current, I_{charge}. In practice, this delay decreases somewhat with increasing frequencies of oscillation, due to the larger slope of the comparator input at higher frequencies of oscillation, resulting in a larger excitation of the comparator. The delay t_{delay}, results in a non-linear relationship between the control current and the frequency of oscillation. Assuming that the delay is independent of I_{charge}, the expression for f_{osc} becomes:

$$f_{osc} = \frac{1}{T_{osc} + t_{delay,tot}} = \frac{1}{\frac{1}{K_{CCO} \cdot I_{charge}} + t_{delay,tot}} \tag{2.45}$$

where:

$$K_{CCO} = \frac{1}{2 \cdot C \cdot V_{REF}} \tag{2.46}$$

Fig. 2.16(b) gives an illustration of the non-linear dependency between f_{osc} and I_{charge}. For increasing values of $I_{charge}$the frequency asymptotically approaches its maximum value $1/t_{delay,tot}$. The non-linearity in the control characteristic of the oscillator results in distortion when the oscillator is used in a frequency (de)modulation application. In order to derive expressions for the harmonic distortion, a Taylor expansion around the center frequency (f_o, I_o see in Fig. 2.16(b)) must be made. Depending on whether the oscillator is used for modulation or demodulation, equation (2.45) or its inverse should be used for calculating the Taylor expansion. For instance, when the oscillator is used for FM-demodulation (input: frequency; output: current), the control non-linearity yields second order distortion [6]:

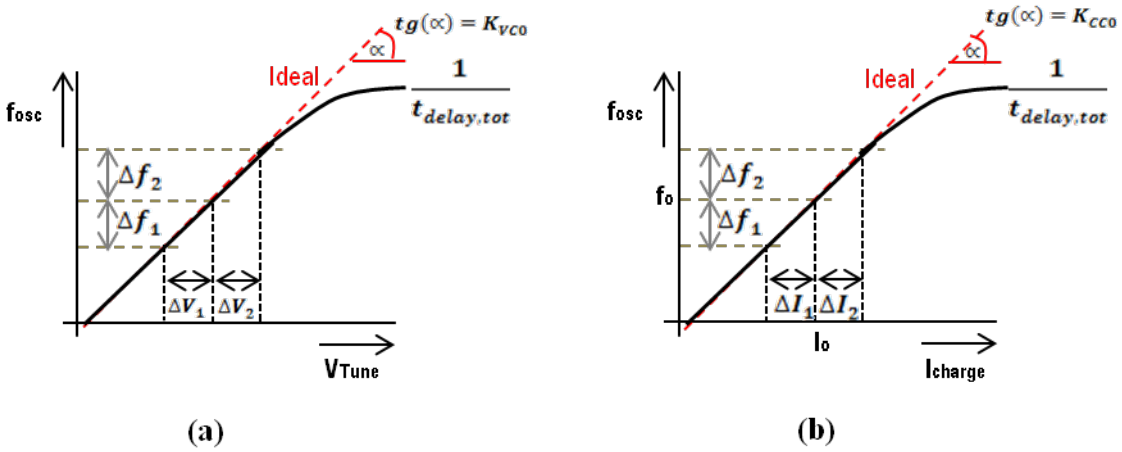


Figure 2.16: Typical tuning curve of (a) voltage controlled oscillator (VCO) and (b) current controlled oscillator (CCO).

$$HD_2 = \frac{t_{delay,tot} \cdot \Delta f}{2} if \frac{t_{delay,tot}}{T_{osc}} \ll 1 \tag{2.47}$$

Notice that the amount of distortion does not depend on the center-frequency f_o (see Fig. (2.16)(b)), but only on the frequency-sweep Δf and the total delay [7]. In order to minimize the distortion, the delay of the level detection circuitry should be minimized. Unfortunately, this increases the noise bandwidth of the equivalent noise at the input of the detection circuit, resulting in an increase of the variance of this noise. As a consequence, the jitter of the oscillator increases.

2.4 Summary

In this chapter, integrated RC oscillators are introduced with a brief discussion of the oscillator fundamentals. Relaxation oscillators, both RC relaxation oscillators and constant-current oscillators are described. Single-ended or differential ring oscillators are discussed . The first-order frequency domain analysis of oscillators and the relevant frequency-domain measures of frequency stability and their particularities are presented. In addition to the important characteristics, such as the phase noise, frequency tuning range and the stability under parameter variations, are also analyzed in the chapter. Finally, the use of figure-of-merit (FOM) is discussed to allow phase noise performance comparison of different oscillators.

Chapter 3

Temperature-compensated relaxation oscillator

3.1 Introduction

A highly stable frequency reference generator is one of the most critical building blocks in many electronic circuits and systems. An external crystal oscillator (XO) is usually employed to generate highly stable frequency reference with excellent accuracy in the order of a few $ppm/^oC$. However, XOs are bulky, power-hungry and cannot be integrated on-chip. For many applications, such as implantable biomedical electronics or wireless body area networks, the accuracy requirements of the frequency reference are much less stringent and, in the order of a few hundred $ppm/^oC$. Thus it is feasible to use a well-designed fully-integrated oscillator to replace XO for frequency reference generation. There have been several works on the implementation of fully-integrated frequency reference in CMOS process technology [1, 3, 8, 9, 10, 11, 12, 13, 14]. LC oscillators can achieve high frequency accuracy and low phase noise, however they consume large chip area and high power consumption. Ring oscillators and relaxation oscillators usually achieve lower frequency accuracy and higher phase noise, but they consume significantly less chip area and have less power dissipation. Therefore, ring and relaxation oscillators are strong candidates for realization of low-cost low-power fully-integrated frequency reference. Nevertheless, clever circuit design techniques are required to ensure that ring and relaxation oscillators can meet the frequency accuracy requirement.

This chapter describes the design of a CMOS fully-integrated temperature-compensated relaxation oscillator. The oscillator is targeted as a replacement of external XO for some applications, where the frequency accuracy requirements are in the order of a few hundreds $ppm/^oC$. This chapter is organized as follows. Section 3.2 describes the literature review of previous works on CMOS relaxation oscillators. Section 3.3 describes the proposed low-power CMOS temperature-compensated relaxation oscillator. Section 3.4 describes the simulation results and conclusion is given in section 4.3.

3.2 Temperature stability and compensation

Recently, there is a growing interest to develop low power CMOS relaxation oscillators with high frequency stability[3, 15, 9, 16, 17, 18, 19] . The oscillation frequency (f_{osc}) practically varies with process parameters, power supply voltage, and temperature. The frequency variations due to power supply voltage can be minimized by using a voltage regulator [20], while the variations due to process parameters can be compensated by trimming of resistors and capacitors. Thus, the temperature stability of f_{osc} is very critical during operation in order to minimize timing uncertainty. The temperature stability of f_{osc} of the relaxation oscillator is typically

due to the temperature dependence of RC time constant and the delay times of comparator and flip-flops.

Temperature compensation entails using temperature dependent circuit elements to compensate for shifts in frequency due to changes in ambient temperature. An oscillator that uses for frequency stabilization technique is referred to as a temperature-compensated oscillator. Temperature compensated oscillators typically employ to generate reduce a frequency variation over temperature. Many factors affect the frequency stability of an oscillator. These include variations in voltage, time, and temperature. Specifications for frequency stability are expressed as the amount of the divergence from the nominal operating frequency, usually in terms of a percentage or in parts per million (ppm). The frequency-variation from temperature behavior can be expressed in term of its temperature coefficient, which is derived from the 1^{st} order temperature coefficient of an expansion around the nominal temperature of T_{osc}. The definitions of the temperature coefficient, TC can be given by (3.1), where x is any functions.

$$TC_x = \frac{1}{x} \cdot \frac{\partial x}{\partial T} \tag{3.1}$$

Note that the temperature stability of f_{osc} can be given by

$$TC(f_{osc}) = \frac{1}{f_{osc}} \cdot \frac{\partial f_{osc}}{\partial T} \tag{3.2}$$

Temperature compensation of f_{osc} can be achieved by employing temperature stable biasing [9, 3] offset cancellation structure [17], voltage-averaging or error feedback loop [15], [19], or feed forward period control scheme [18]. The offset cancellation structure, described in [17], can achieve $\pm 0.25\%$ frequency variations at 18.5 kHz over temperature range of $-40^{\circ}C$ to $+90^{\circ}C$, however it requires two clock phases for operation thus another timing circuit is needed. In [9], a 1.1-MHz relaxation oscillator with $\pm 0.5\%$ over temperature range of $-20^{\circ}C$ to $+80^{\circ}C$ is obtained by using temperature-compensated biasing. The relaxation oscillator in [15] employs switched capacitor error feedback loop and it achieves 12.6-MHz with $\pm 0.82\%$ variation over temperature range of $0^{\circ}C$ to $+80^{\circ}C$. In [19], the voltage-averaging feedback is employed to realize a 14-MHz relaxation oscillator with $\pm 0.19\%$ variation over temperature range of $-40^{\circ}C$ to $+125^{\circ}C$.

As mentioned above, the frequency variations of the relaxation oscillator can be improved by employing into three techniques for the temperature-compensation: 1) the temperature stable biasing techniques, 2) the offset-cancellation techniques and 3) the voltage-averaging or error feedback loop or feed forward period control scheme techniques. This section describes the circuit operation to improving the temperature stability of f_{osc}.

3.2.1 The temperature stable biasing technique

This section describes the main causes of of temperature stability of f_{osc} of a relaxation oscillator.

The RC relaxation oscillator is shown in Fig. 3.1. The frequency of oscillation in Fig. 3.1 can be given by

$$f_{osc} \approx \frac{1}{R_1 C_1} \tag{3.3}$$

The frequency variations of the RC relaxation oscillator is mainly caused by the resistors, R_1, and hysteresis voltage of the Schmitt trigger, $V_H = V_B - V_A$. The RC relaxation oscillator are inversely proportional to the hysteresis voltage of the Schmitt trigger, $V_H = V_B - V_A$. It means that the temperature stability of f_{osc} of the relaxation oscillators typically due to the temperature dependence of the voltage levels of V_H. A temperature-independent of the hysteresis voltage, V_H, is possible by designing V_B track proportional to V_A. Furthermore,

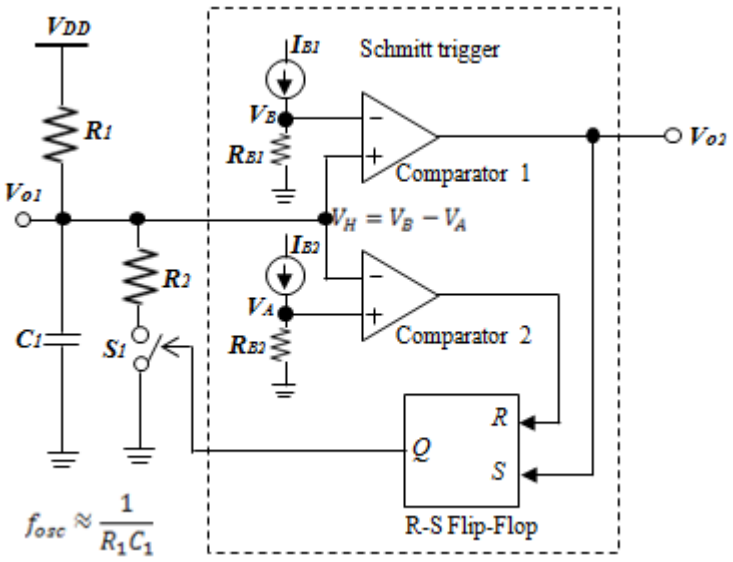


Figure 3.1: RC oscillators intensive temperature.

the bias setting resistors are implemented two voltage source, V_A and V_B as shown in Fig. 3.1. The temperature-independence of the hysteresis voltage, V_H, depends on the current source, I_{B1} and I_{B2} that flow through resistors R_{B1} and R_{B2}, respectively. The frequency drift is mainly caused by the variations of bias currents and resistors due to process, voltage and temperature. The temperature variation of the current source and resistors can be controlled by implementing the zero/low-temperature coefficient (TC) in bias currents and resistors to reduce frequency variations. The zero/low-TC in bias currents can be employed the combined PTAT and CTAT current sources and the composite resistors are used to adjust the temperature coefficient of the current references. For example, the PTAT current reference is shown in Fig. 3.2(a) [9]. The voltage dropped across the resistors $R+$ and $R-$ is given by $V_R = V_{GS1} - V_{GS2}$, where V_{GS1} and V_{GS2} represent the gate-to-source voltages of transistors M_1 and M_2, respectively. Assuming the drain current of an NMOS transistor working in the subthreshold region and the drain current of M_1 and M_2 are equal, the current I_P is given by [9]

$$I_P = \frac{\eta V_T}{R_+ + R_-} \cdot ln\left(\frac{W_2/L_2}{W_1/L_1}\right) \tag{3.4}$$

where V_T is the thermal voltage, η is the subthreshold slope factor and the resistors $R+$ and $R-$ have the positive and negative temperature coefficients, respectively. According to (3.4), if the temperature coefficients of $R+$ and $R-$ are canceled, the PTAT current I_P is realized.

The CTAT current reference in Fig. 3.2(b) [9]. When M_5 works in the subthreshold region, the current I_A, is mirrored by a zero/low-TC current source I_P with a current ratio $m < 1$. Since, the the temperature coefficient of the gate-to-source of M_5 transistor is negative, the CTAT current I_C can be canceled by using the temperature coefficients of $R+$ and $R-$.

The cancellation of the temperature coefficients of $R+$ and $R-$ are usually realized by the composite resistors. In [21] presented simple composite resistor topologies as shown in Fig. 3.3. The simple series and parallel resistors are shown in Fig. 3.3(a) and Fig. 3.3(b), respectively. The temperature coefficient in Fig. 3.3(a) and Fig. 3.3(b) can be given by

$$TC_s = TC_A \cdot \frac{\beta}{1+\beta} + TC_B \cdot \frac{1}{1+\beta} \tag{3.5}$$

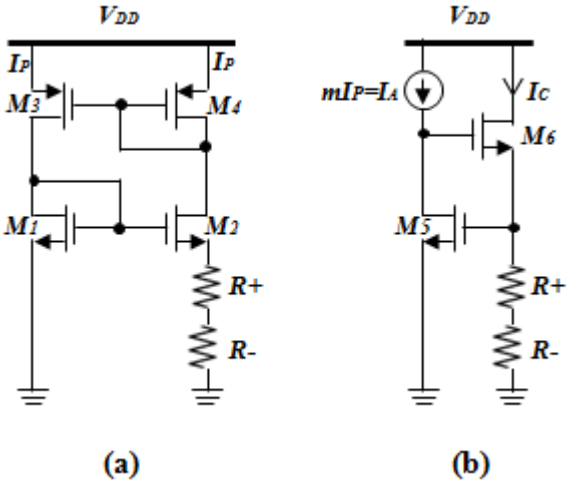


Figure 3.2: PTAT current references.

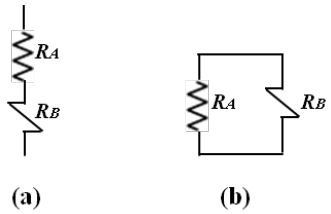


Figure 3.3: Composite resistor topologies (a) series (b) parallel.

$$TC_p = TC_A \cdot \frac{1}{1+\beta} + TC_B \cdot \frac{\beta}{1+\beta} \tag{3.6}$$

The composite resistor temperature coefficient is determined by the relative size of R_A and R_B where $\beta = R_A/R_B$ at T_0.

The constant-current relaxation oscillator architecture is shown in Fig. 3.4. Assuming the current $I_2 = 2I_1$, then, the frequency of oscillation, f_{osc} can be expressed as

$$f_{osc} = \frac{I_1}{2V_H C_1} \tag{3.7}$$

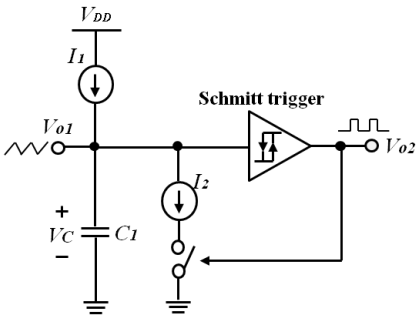


Figure 3.4: The constant-current relaxation oscillator intensive temperature.

Equation (3.7), implies that the main contributions to the frequency drift are caused by two current sources I_1 and I_2, which affect to the drift of the charge and discharge bias current. Moreover, a temperature stability of f_{osc} in the constant-current relaxation oscillators depend on the drift of the total hysteresis voltage V_H, any temperature drift of V_H results in an equal amount of relative frequency drift. Therefore, the temperature-independent current source, I_1 and I_2 can be implemented the zero/low-TC in bias currents by employing the combined PTAT and CTAT current sources and the composite resistors. In the same case of the hysteresis voltage, V_H , are designed by the bias setting resistors to implement two voltage source, V_A and V_B as shown in Fig. 3.1.

In addition to a positive temperature coefficient of V_H in Fig. 3.4 results in a negative contribution to temperature coefficient of the oscillation frequency. Therefore, designing a bias current circuitry with a positive temperature coefficient it is possible to compensate the drift of the hysteresis window V_H, minimizing the overall variation of the oscillation frequency due to the temperature changes. Several works have been reported [22, 9, 23] to demonstrate a positive temperature coefficient in the temperature compensation of the current and voltage references.

The frequency deviation over a wide temperature range is one of the primary performance metrics evaluated in the design and manufacturing of a temperature compensated oscillator. Therefore, this dissertation focuses on the temperature stable biasing techniques, which is the best choice for designing in the temperature compensation of the constant-current relaxation oscillator architecture as will be described in Section 3.3.

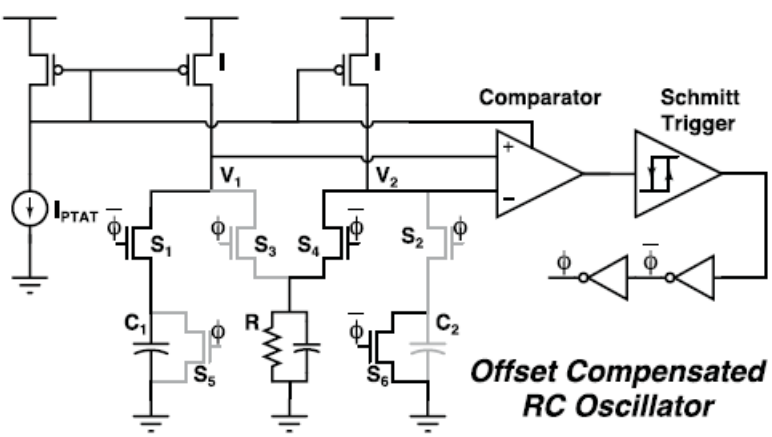
3.2.2 The offset-cancellation techniques

The offset-canceling oscillator can achieve good frequency and temperature stability with low power consumption. In [17], an offset-cancellation scheme which allows significant power reduction in the oscillator was proposed. The architecture of the offset compensated RC oscillator is shown in Fig. 3.5. A current I passes through resistor R to generate a voltage $I \cdot R$ on node V_2, when phase $\phi = 0$. At the same time, a matched current source charges capacitor C_1, such that node V_1 crosses V_2 at time RC. After t_{delay} corresponding to the delay of the comparator and subsequent buffers, ϕ changes to 1, which then resets the capacitor voltage. The two comparator inputs is reversed, with V_1 being the resistor voltage and V_2 the voltage across capacitor C_2. The period of the oscillator is thus nominally $2RC + 2t_{delay}$. Two separate capacitors are used in the two phases so that the delay of capacitor discharge is not included in the period. This switching scheme also cancels comparator offset. For example, if the comparator has an offset V_{os}, as shown in Fig. 3.5(b), the duration of phase $\phi = 0$ increases by CV_{os}/I, however the opposite phase $\phi = 1$ decreases by the same amount, thus the total period of oscillation is constant.

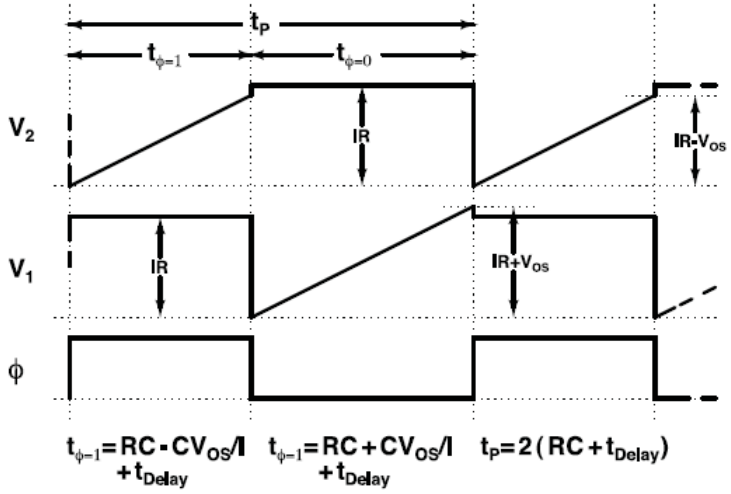
The offset cancellation scheme achieved a temperature stability of $\pm 0.25\%$, ultra-low power operation at $120nW$ and long-term stability of better than 20ppm. The main causes that improves temperature stability in [17] are: (a) permitting low-swing oscillations since offset and temperature variations of the offsets do not proportionally affect frequency stability, (b) requiring only one comparator as opposed to two in traditional architectures, and (c) relaxing the specifications on the comparator offset, and allowing optimization of gain and bandwidth. The offset cancellation also attenuates the effect of flicker noise, improving long-term stability of the oscillator.

3.2.3 The voltage averaging feedback techniques

The oscillation frequency of a conventional relaxation oscillator typically varies with variations of the comparator's delay time, aging of current sources, and flicker noise of current sources. Typically, for a stable and accurate oscillation, the comparator delay time is required to be shorten such that it is negligible. However, this



(a)



(b)

Figure 3.5: Architecture of the offset compensated RC oscillator. The switch state for phase $\phi = 0$ is shown with off switches grayed out.

approach is power-consuming and is not suitable for low power applications. A voltage-averaging feedback (VAF) method can overcomes these issues while achieving good accuracy with low power dissipation. An advantage for applying VAF to a oscillation is achieving oscillation independent of the comparator's delay t_d. A complementary relaxation oscillator and an active filter for VAF is shown in Fig. 3.6. The relaxation oscillator is considered as a voltage-controlled oscillator with a control signal V_c.

Oscillation waveforms V_{osc1} and V_{osc2} are summed up to V_{osc} and transferred to the active filter part. At this condition, the active filter maintains DC voltage of whole oscillation at the reference voltage as shown in Fig. 3.6(b). The VAF loop equalizes DC of the oscillation waveform with V_{ref} as

$$\frac{1}{T}\int_0^T V_{osc1,2}(t)dt = V_{ref} \tag{3.8}$$

V_{osc} and V_{ref} are virtually shorted in a low-frequency domain defined by a time constant of R_1C_1. V_{ref} is generated by a voltage divider of rail-to-rail voltages. Therefore, the following simplified equation is obtained by

$$\frac{(1-\alpha)\,T}{RC} = 1 - e^{-T/RC} \tag{3.9}$$

where $\alpha = \left(V_{ref}/V_{dd}\right)$, the oscillation frequency is just defined by a time constant RC and α. The variation of t_d has little effect on T because VAF automatically adjusts V_C to keep the equilibrium condition of (3.8), which results in a stable desired frequency.[19]

3.3 Proposed Relaxation Oscillator Design

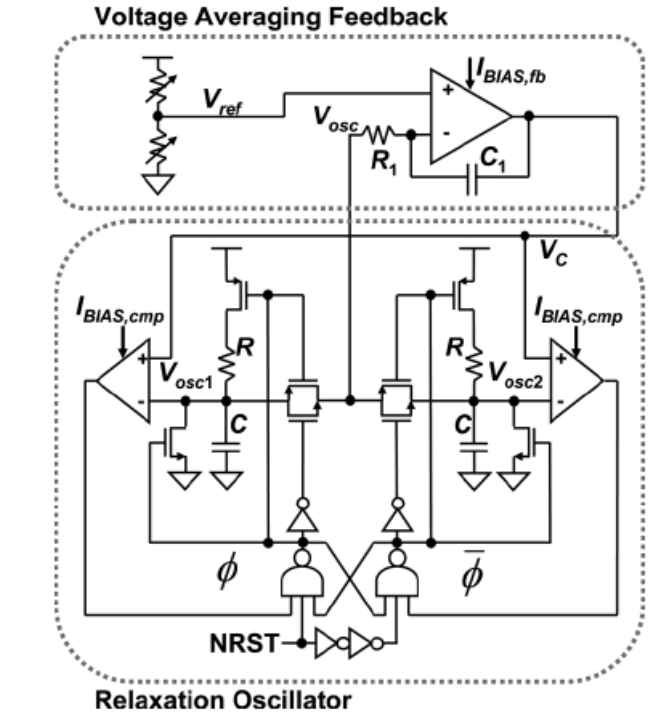
This section describes the design and realization of a high-frequency relaxation oscillator with low power dissipation and low frequency variation. A method of temperature-compensated biasing is proposed to achieve very low frequency variation over a wide range of temperature.

3.3.1 Circuit architecture

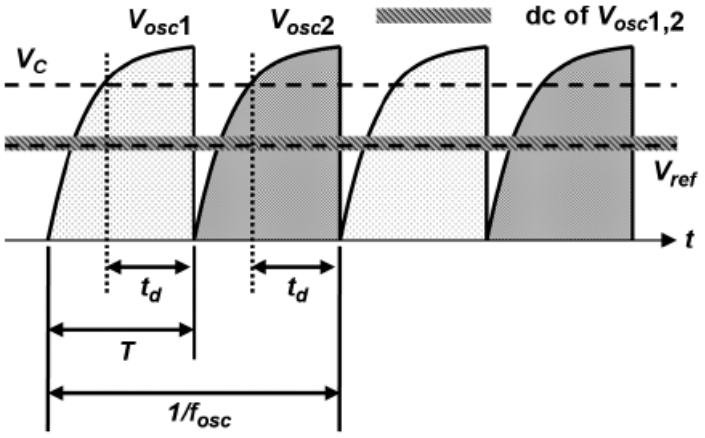
Figure 3.7(a) illustrates a conceptual block diagram of a typical constant-current relaxation oscillator. Assuming that the voltage across the capacitor V_C is initially zero and the MOSFET switch (M_X) is off, the constant current will charge the capacitor and V_C will increases. The capacitor voltage V_C is compared with a constant reference voltage $V_R = I_R R$, which is generated by another constant current I_R and a passive resistor R. When V_C is less than V_R, the output voltage (V_{out}) of the comparator is low or 0 V and M_X remains off. When V_C exceeds V_R, the comparator trips and V_{out} is HIGH or V_{DD} after a delay time t_p and M_X is turned on to discharge the capacitor and reset V_C to 0 V. Thus the capacitor is charged and discharged periodically by the I_C and M_2, respectively. Fig. 3.7(b) shows the time-domain waveforms of V_C and V_{out}. The period of oscillation (T_{OSC}), is given by (3.10), where t_c is the charging time by I_C, t_p is the delay time of the comparator and t_d is the discharging time by the MOSFET switch M_X.

$$T_{osc} = t_c + t_p + t_d \tag{3.10}$$

where t_c is the delay introduced by controlling charging cycle as the level detection circuitry. The t_p is delay time of the current comparator which several public papers [13], [3], [9] are usually ignore in term of t_p by



(a)



(b)

Figure 3.6: Voltage-averaging feedback relaxation oscillator (a) its schematic and (b) its waveform.

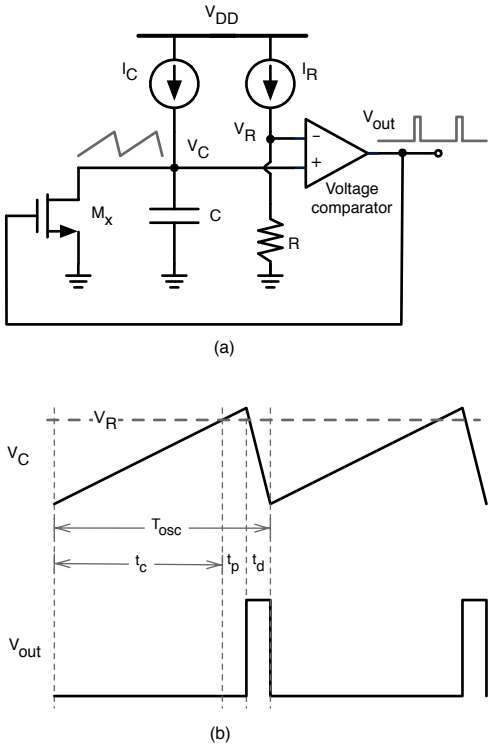


Figure 3.7: A typical current-controlled relaxation oscillator (a) the schematic (b) the waveform.

designing to be as short as the hold time required; therefore, the frequency-variation of a switched-capacitor relaxation oscillator is mainly due to the t_c. The discharging time (t_d) is proportional to $(C+C_p)R_{on}$, where R_{on} is the average on-resistance of M_x and C_p is the drain parasitic capacitance of M_x. Since R_{on} is inversely proportional to $(W/L)_x$ but C_p is proportional to $(WL)_x$, thus increasing $(W/L)_x$ reduces R_{on} but increasing C_p. Therefore, increasing $(W/L)_x$ to reduce t_d will have a diminishing influence beyond certain values and t_d will asymptotically reach a minimum value. In this dissertation, the integrating capacitor C is chosen to be much larger than C_p and an optimal value of $(W/L)_x$ is selected to achieve $t_d \ll t_c$. To minimize t_d, a high-speed comparator is required and it is usually quite power-hungry when realized in voltage-mode. On the other hand, current-mode comparators can achieve high speed with low power consumption thus it is beneficial for low power applications. Current-mode comparators have been used to realize low-power relaxation oscillators in [3, 9]. However, the frequency of oscillation is limited to a few MHzs in order to achieve low power consumption and low frequency variations. This dissertation presents the design and optimization of a temperature-compensated high-frequency relaxation oscillation, in the order to tens of MHzs, with low frequency variations.

Fig. 3.8 shows the simplified circuit diagram of the proposed relaxation oscillator using a current-mode comparator. The proposed circuit is based on the current-controlled topology with the use of a current comparator. The capacitor voltage (V_C) is converted to a current (I_1) by a resistive source-degeneration transconductor, realized by M_1 and R. The simple source-degeneration transconductor, instead of a more complex circuit, is employed in order to achieve high oscillation frequency and low power consumption. The transconductor's output current (I_1) is compared with a constant reference current I_R and the resultant current ($I_x = I_R - I_1$) is applied to the current comparator.

Assuming that V_C is initially zero, the constant current I_C will charge up the capacitor then V_C and I_1 increase. When $I_1 < I_R$ (i.e. $I_x > 0$), the comparator output voltage (V_{out}) will be LOW or 0 V, then M_2 is turned off and V_C and I_1 continue to rise. When I_1 exceeds I_R or $I_1 > I_R$ (i.e. $I_x < 0$), V_{out} is HIGH or V_{DD} and M_2 is turned on to discharge V_C to ground and I_1 is reset to 0. Next, V_C is charged again and the above process is repeated. Thus the capacitor is charged and discharged periodically by I_C and M_2, respectively.

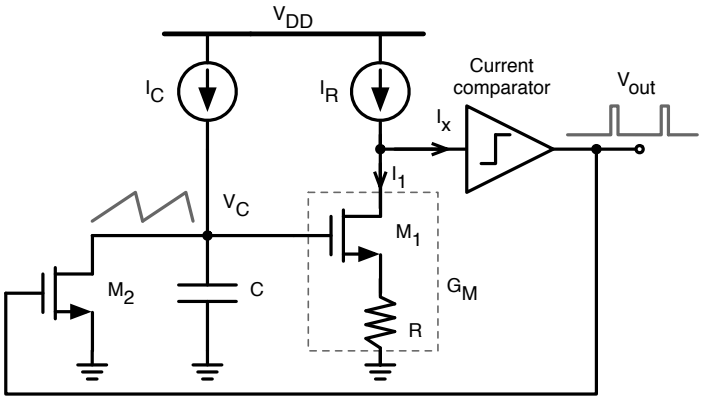


Figure 3.8: Simplified circuit diagram of the proposed relaxation oscillator with current-mode comparator

Equation (3.10) is the period of oscillation which it can usually assumed that t_p and t_d are much less than t_c, thus $T_{osc} \approx t_c$. Thus, T_{osc}can be described by (3.11). Therefore, the main reasons of the period of oscillation in relaxation oscillator is the delay of the t_c as:

$$T_{osc} \approx t_c = \frac{C \cdot V_R}{I_C} \tag{3.11}$$

where C, V_R and I_C are the reference capacitor, reference voltage and bias current, respectively. The voltage waveforms of V_C and V_{out} are the same as in Fig. 3.7(b) with the equivalent $V_R = {}^{I_R}/_{G_M}$, where G_M is the transconductance of the transconductor as described by (3.12). The period of oscillation (T_{osc}) can also be described by (3.10). Typically, a current comparator can easily achieve the delay time (t_p) in the order of a few nanoseconds [24], thus t_p can be neglected for T_{osc} larger than tens of nanoseconds. The discharging time (t_d) is directly proportional to the on-resistance of M_2, which can be made negligibly small by using a sufficiently large $({}^{W}/_{L})_2$. Therefore, for oscillation frequencies in the range of tens of MHz, it can be assumed that t_p and t_d are much less than t_c and $T_{osc} \approx t_c$, which can be described by (3.11). In the proposed oscillator, $V_R = {}^{I_R}/_{G_M}$ thus T_{osc} is given by (3.13), assuming that I_R is a scaled-copy of I_C or $I_R = mI_C$.

$$G_M = \frac{1}{R + \frac{1}{g_{m1}}} \tag{3.12}$$

$$T_{osc} = \frac{C}{G_M} \cdot \frac{I_R}{I_C} = \frac{C}{G_M} \cdot m \tag{3.13}$$

3.3.2 Temperature compensation approach

The temperature dependence of a parameter can be characterized by the fractional temperature coefficient (TC). The TC of T_{osc} ($TC(T_{osc})$) can be calculated by (3.14) and the result is given by (3.16), where $\alpha_c = {}^{t_c}/_{T_{osc}}$, $\alpha_p = {}^{t_p}/_{T_{osc}}$, $\alpha_d = {}^{t_d}/_{T_{osc}}$ and $TC(t_c)$, $TC(t_c)$, $TC(t_c)$ are the fractional temperature coefficients of t_c, t_p, and t_d, respectively. Assume that $\alpha_c \approx 1$, $\alpha_p \ll 1$, and $\alpha_d \ll 1$, thus $TC(T_{osc}) \approx TC(t_c)$.

$$TC(T_{osc}) = \frac{1}{T_{osc}} \frac{\partial T_{osc}}{\partial T} \tag{3.14}$$

$$= \left(\frac{t_c}{T_{osc}}\right) \cdot \frac{1}{t_c} \frac{\partial t_c}{\partial T} + \left(\frac{t_p}{T_{osc}}\right) \cdot \frac{1}{t_p} \frac{\partial t_p}{\partial T} + \left(\frac{t_c}{T_{osc}}\right) \cdot \frac{1}{t_d} \frac{\partial t_d}{\partial T} \tag{3.15}$$

$$= \quad \alpha_c TC(t_c) + \alpha_p TC(t_p) + \alpha_d TC(t_d) \tag{3.16}$$

For the circuit in Fig. 3.7(a), the $TC(T_{osc})$ can be derived from (3.13) as given by (3.18), which equals the sum of the temperature coefficients of R and C. In theory, the period and frequency of oscillation can be insensitive to temperature variations by ensuring $TC(T_{osc}) = 0$. Typically, on-chip capacitors (e.g. metal-insulator-metal or polysilicon-polysilicon capacitors) have very small TCs, compared with those of on-chip resistors (e.g. see Table 3.1 $TC\left(C_{poly1}\right) = +0.03 \times 10^{-3}/^{o}\text{C}$). Thus, it can be assumed that $TC(T_{osc}) \approx TC(R)$ and the design goal is to minimize $TC(R)$. One method of minimizing $TC(R)$ is to use a composite resistor, which is either a series or parallel combination of positiveTC and negativeTC resistors [13, 18].

$$TC(T_{osc}) = \frac{1}{T_{osc}} \frac{\partial T_{osc}}{\partial T} = \frac{1}{R} \frac{\partial R}{\partial T} + \frac{1}{C} \frac{\partial C}{\partial T} \tag{3.17}$$

$$= TC(R) + TC(C) \tag{3.18}$$

For the proposed circuit in Fig. 3.8, the $TC(f_{osc})$ can be derived from (3.13) as given by (3.19). Assume that $TC(C)$ is negligible, thus $TC(f_{osc}) \approx TC(G_M)$. Since G_M is described by (3.12), the $TC(G_M)$, and thus $TC(f_{osc})$, can be derived as given by (3.22). Therefore $TC(f_{osc})$ can be minimized by canceling the two terms of $TC(R)$ and $TC(g_{m1})$ in (3.22).

$$TC(f_{osc}) = \frac{1}{f_{osc}} \frac{\partial f_{osc}}{\partial T} = \frac{1}{G_M} \frac{\partial G_M}{\partial T} - \frac{1}{C} \frac{\partial C}{\partial T} \tag{3.19}$$

$$= TC(G_M) - TC(C) \tag{3.20}$$

$$TC(f_{osc}) \approx TC(G_M) = \frac{1}{G_M} \frac{\partial G_M}{\partial T} \tag{3.21}$$

$$= -\left(\frac{g_{m1}R}{1+g_{m1}R}\right) TC(R) + \left(\frac{1}{1+g_{m1}R}\right) TC(g_{m1}) \tag{3.22}$$

In Fig. 3.8, M_1 will operate mostly in the saturation region as V_C increases. Thus, assuming the MOSFET's square-law relationship, $TC(g_{m1})$ can be derived as given by (3.24). Since both $TC(\mu_n)$ and $TC(V_{TH})$ are negative [25], $TC(g_{m1})$ can be either positive or negative depending on the value of V_{GS}. Note that there is a specific value of V_{GS} which can give $TC(g_{m1}) = 0$ and this is usually known as the zero temperature coefficient (ZTC) point of MOSFET [25]. In this work, M_1 is biased in the region below the ZTC point, thus second term in (3.24) dominates and g_{m1} increase with temperature or $TC(g_{m1}) > 0$. Therefore, from (3.22), a positive-TC resistor should be used to compensate with $TC(g_{m1})$ in order to achieve low $TC(f_{osc})$.

$$TC(g_{m1}) = \frac{1}{g_{m1}} \frac{\partial g_{m1}}{\partial T} = \frac{1}{\mu_n} \frac{\partial \mu_n}{\partial T} - \left(\frac{V_{TH}}{V_{GS}-V_{TH}}\right) \frac{1}{V_{TH}} \frac{\partial V_{TH}}{\partial T} \tag{3.23}$$

$$= TC(\mu_n) - \left(\frac{V_{TH}}{V_{GS}-V_{TH}}\right) TC(V_{TH}) \tag{3.24}$$

Fig. 3.9 shows the effect of temperature variations on V_C, which were obtained by using ideal I_C and I_R with zero TCs and ideal resistor R with $TC(R) = 0$. According to (3.22) and (3.24), g_{m1} and G_M increase with temperature thus the effective V_R is reduced (i.e. the peak voltage of the sawtooth waveform in Fig. 3.9 decreases as temperature increases), and thus f_{osc} is increased as temperature increases. Temperature

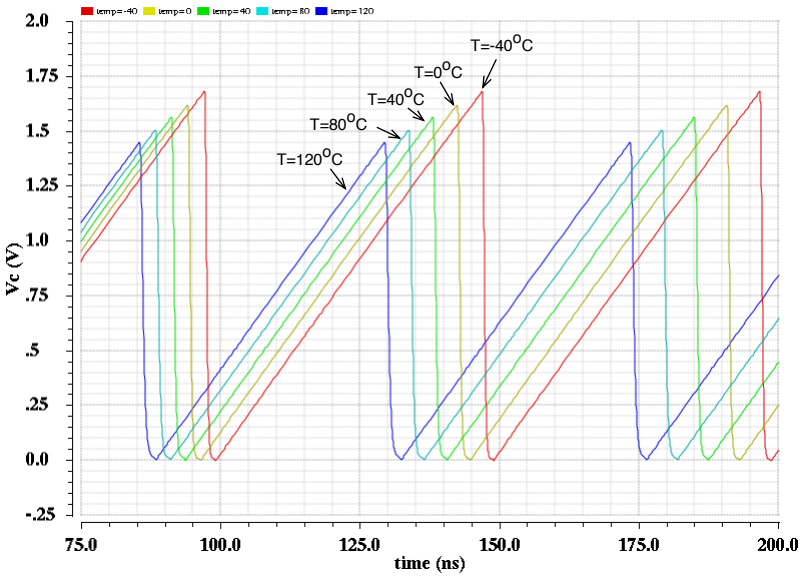
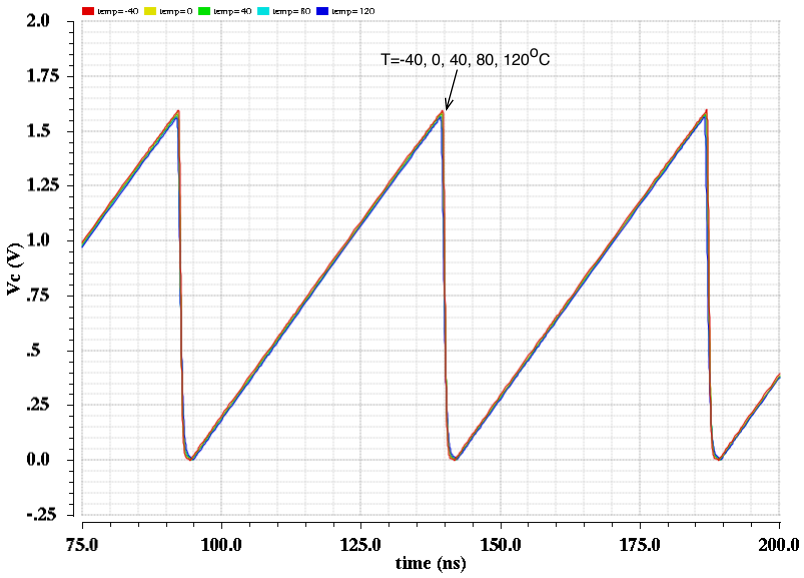


Figure 3.9: Effect of temperature variations on V_C and f_{osc} with $TC(I_C) = TC(I_R) = TC(R) = 0$.

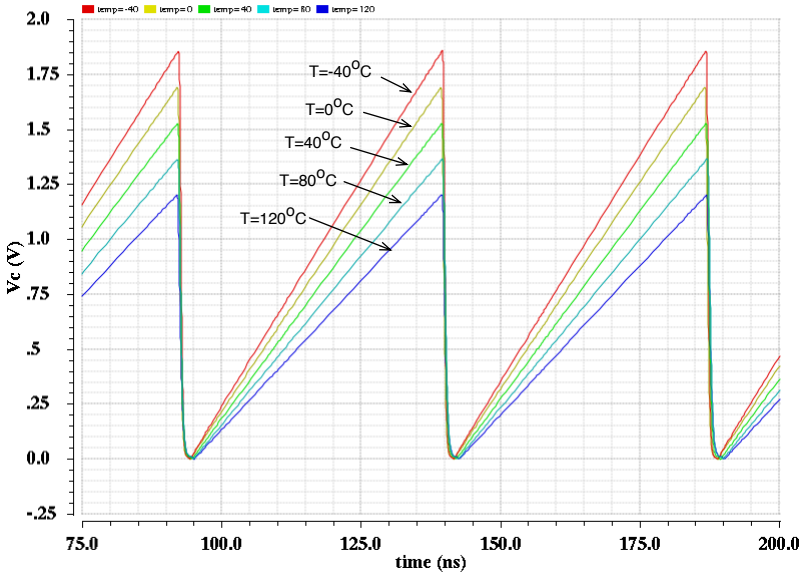
compensation of f_{osc} can be achieved by either reducing I_C (and I_R) or increasing R as temperature increases. The two approaches are demonstrated in Fig. 3.10.

In Fig. 3.10(a), $TC(I_C) = 0$ and $TC(R) = +1.4 \times 10^{-3}/^{\circ}\text{C}$, the charging rate of V_C ($\partial V_C/\partial T$) is unaffected by temperature variations and R is increased with temperature to compensate for the increase of g_{m1}. This keeps G_M and the effective V_R relatively constant with temperature, and thus f_{osc} can be insensitive with temperature. In Fig. 3.10(b), $TC(I_C) = TC(I_R) = -2.5 \times 10^{-3}/^{\circ}\text{C}$ and $TC(R) = 0$, the charging rate $\partial V_C/\partial T$ (due to reduced I_C) and V_R (due to reduced I_R) are decreased proportionally as temperature increases, and thus f_{osc} is insensitive with temperature. Fig. 3.11 shows the simulated frequency variations of f_{osc}, over a temperature range of $-40\,^{\circ}\text{C}$ to $+120\,^{\circ}\text{C}$, without compensation (in grey with $TC(I_C) = TC(R) = 0$) and with ideal compensation (in green with $TC(I_C) = 0$ & $TC(R) = +1.4 \times 10^{-3}/^{\circ}\text{C}$). The average $TC(f_{osc})$ can be reduced from 783.33 $^{\text{ppm}}/^{\circ}\text{C}$ (without compensation) to about 10.05 $^{\text{ppm}}/^{\circ}\text{C}$ (with optimum compensation). Therefore, the optimum compensation can be achieved with either $TC(I_C) = 0$ & $TC(R) = +1.4 \times 10^{-3}/^{\circ}\text{C}$ or $TC(I_C) = -2.5 \times 10^{-3}/^{\circ}\text{C}$ and $TC(R) = 0$. However, in practice, either $TC(I_C) = 0$ or $TC(R) = 0$ cannot be obtained, and thus a more practical design approach is to choose a value of $TC(R)$ and find the optimum value of $TC(I_C)$ to achieve the best temperature compensation.

Table 3.1 shows the fractional temperature coefficients of the on-chip resistors and capacitors available in our 0.35-μm CMOS technology. Note that the TC of polysilicon capacitor (C-poly) is very small ($+0.03 \times 10^{-3}/^{\circ}\text{C}$) and thus it is neglected. It can be seen that the TCs of the diffusion resistors (Rdiffn or Rdiffp) are quite close to the required TC, however the resistance of diffusion resistors, especially at large resistance, are practically voltage-dependent and non-linear. The TC of the diffusion resistors varies substantially with its resistance and voltage, thus they are not suitable for our design. The polysilicon resistors (R-poly1 or R-poly2) are preferred because of their excellent linearity, which make their TCs virtually independent with resistance and voltage. However, the drawback of polysilicon resistors is small sheet resistance, thus relatively large silicon area is required. It may be argued that a composite resistor, realized by combining polysilicon and n-well resistors (R-nwell) in series or parallel, can be used to obtain the required TC and save the chip area. However, the required TC is much closer to the TC of polysilicon resistor, thus the suitable composite resistance need to use polysilicon resistance much larger than the n-well resistance. For example, a 150-kΩ series-composite resistance requires about 140-kΩ of R-poly1 and 10-kΩ of R-nwell to obtain the desired $TC(R) = +1.4 \times 10^{-3}/^{\circ}\text{C}$. In this case, the area saving of a composite resistor is insignificant, and thus R is implemented with R-poly1. Since the TC of R-poly1 is $+0.9 \times 10^{-3}/^{\circ}\text{C}$, the temperature compensation is not optimum, and the achievable $TC(f_{osc})$ with $TC(I_C) = 0$ is about 282.05 $^{\text{ppm}}/^{\circ}\text{C}$ over a temperature range of $-40\,^{\circ}\text{C}$ to $+120\,^{\circ}\text{C}$,



(a)



(b)

Figure 3.10: Effect of temperature variations on V_C and f_{osc} with (a) $TC(I_C) = TC(I_R) = 0$ & $TC(R) = +1.4 \times 10^{-3}/^{o}\text{C}$ and (b) $TC(I_C) = TC(I_R) = -2.5 \times 10^{-3}/^{o}\text{C}$ & $TC(R) = 0$

Table 3.1: Fractional temperature coefficients of on-chip resistors and capacitor.

Component	Sheet resistance ($\Omega/\square$)	1st-order TC (10^3/ºC)
R-Poly1	8	0.9
R-Poly2	50	0.59
R-nwell	1,000	6.2
R-diffn	75	1.5
R-diffp	140	1.5
C-poly	n/a	0.03

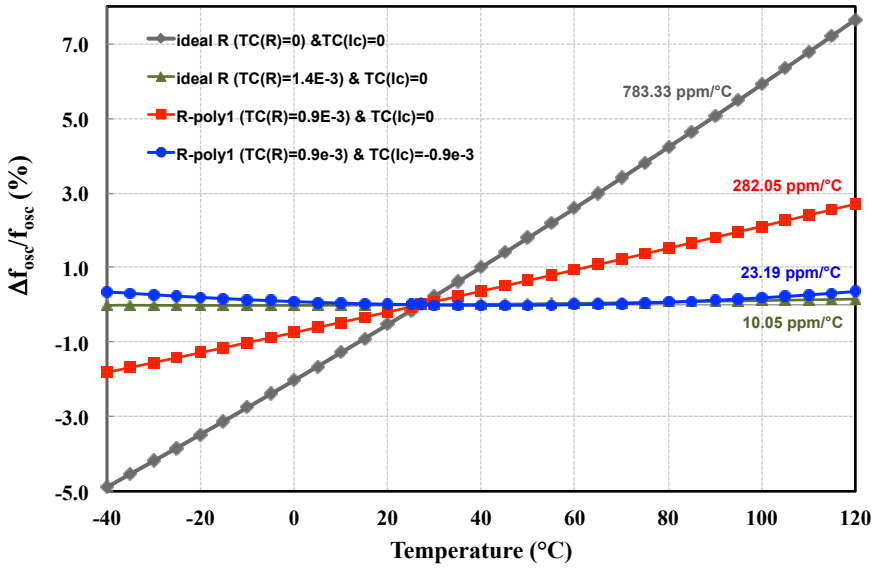


Figure 3.11: Simulated temperature variations of f_{osc}.

as depicted in Fig. 3.11 (in red). The optimum temperature compensation of f_{osc} can be achieved by using I_C and I_R with an optimum negative TC, as demonstrated in Fig. 3.11 (in blue). In this design with R realized by 150-kΩ R-poly1, the optimum temperature compensation was obtained with $TC(I_C) = -0.9\times10^{-3}/^{o}C$ and the minimum achievable $TC(f_{osc})$ was about 23.19 $ppm/^{o}C$. Thus, the next design task is to design a bias current generator circuit that can provide the optimum $TC(I_C) = -0.9\times10^{-3}/^{o}C$.

3.3.3 Complete circuit implementation

Fig. 3.12 shows the complete schematic diagram of the proposed oscillator. The conventional constant-g_m bias current generator, realized by $M_{10}-M_{15}$, R_{B1} and R_{B2}, is used to provide the currents I_C and I_R via M_3 and M_4, respectively.

A high-speed capacitive-input current comparator [26, 24], realized by M_6–M_9, is adopted because the circuit can achieve input current offset and resolution of less than 10 pA. The circuit operation of the current comparator can be explained as follow. The input current I_x, which is the difference between I_R and I_1, is applied to a CMOS inverting amplifier formed by M_8 and M_9. The output voltage of the amplifier, v_a is fed back non-linearly to the input node via M_6 and M_7, in order to achieve non-linear input impedance. For small I_x around the quiescent point, both M_6 and M_7 are OFF and the input impedance is large and mostly capacitive. The large input impedance greatly facilitates the detection of small input current levels and thus high current resolution is achieved. For positive I_x, the voltage at the input node increases and v_a decreases; this turns M_6 ON and a positive feedback loop is created to fix the voltage and obtain a virtual ground at the input node. For negative I_x,

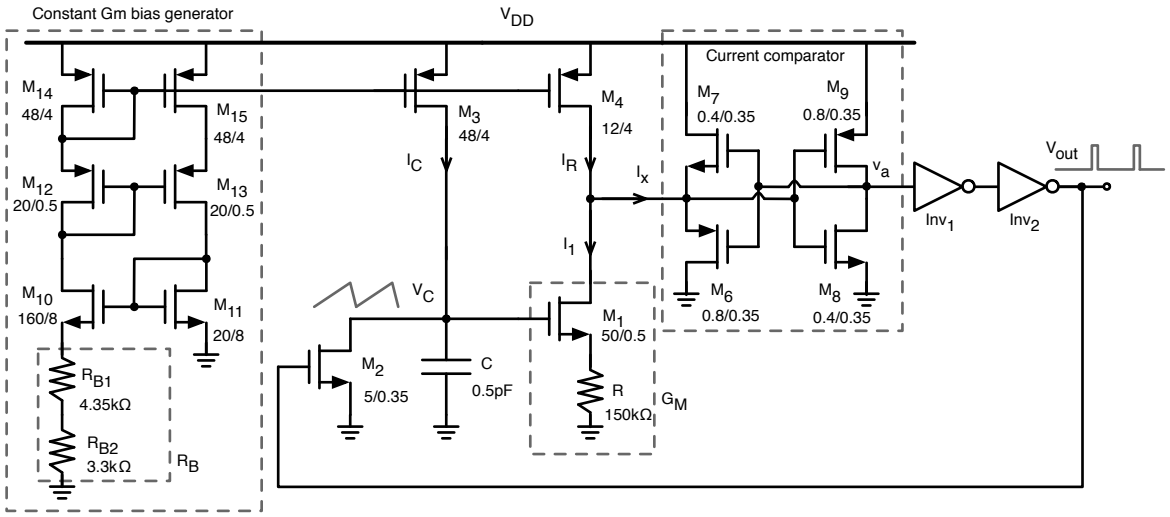


Figure 3.12: Complete schematic diagram of the proposed relaxation oscillator

M_7 is turned ON and a similar circuit operation occurs. For large input currents, the voltage excursions at the input node are kept small because of the feedback loop. Rail-to-rail output voltage swing and short transition time are achieved by using an output CMOS inverters, Inv_1 and Inv_2. For good temperature compensation of the oscillation frequency, the propagation time delay (t_p) of the comparator is required to be small compared with the period of oscillation. The propagation time delay is dependent of the size of transistors and power supply voltage. Minimum-sized transistors were employed to obtain very small t_p. Fig. 3.13 shows the simulated t_p as a function of power supply voltage (V_{DD}), over a temperature range of −40°C to +120°C. In our CMOS technology, the simulated t_p is less than 2 nS and is almost insensitive to temperature variations when V_{DD} is greater than 2 V. For accurate temperature compensation, the period of oscillation (T_{osc}) should be greater than $10t_p$ (i.e. 20 nS) and thus f_{osc} should be limited to below 50 MHz. Simulation results with $V_{DD} = 2.5$ V showed that the fractional temperature coefficient of t_p was about -0.69×10^{-3}/°C. Figure 3.13 found that the proposed current comparator requires supply voltage too much which is the optimum supply voltage that results in temperature insensitive. Therefore, the supply voltage was selected to be 2.5-V. Fig. 3.14 is plotted the time delay of the proposed current comparator versus temperature at 2.5-V of supply voltage.

To achieve the required $TC(I_C)$ = -0.9×10^{-3}/°C for the optimum compensation, the bias resistor R_B with $TC = +3 \times 10^{-3}$/°C has to be employed. In this work, R_B is implemented by a series composite resistor, R_{B1} and R_{B2}, which are realized with R-poly1 and R-nwell, respectively. For a nominal I_C of 20 μA, $R_B = 7.65\,\text{k}\Omega$ is required and it is realized with $R_{B1} = 4.35\,\text{k}\Omega$ and $R_{B2} = 3.3\,\text{k}\Omega$ in order to achieve the required $TC(I_C)$. Fig. 3.15 shows the simulated I_C, over a temperature range of $-40\,^{\circ}$C to $+120\,^{\circ}$C, obtained with the series composite resistor (in blue). It can be seen that the achievable TC is very close to the required value of $TC(I_C)$ = -0.9×10^{-3}/°C (in red).

3.4 Simulation Results

The proposed relaxation oscillator was designed and simulated by using Cadence Spectre with process parameters from a standard 0.35-μm CMOS technology. The circuit was designed to operate with a 2.5-V power supply voltage and a nominal oscillation frequency of about 20 MHz at room temperature of 27 °C. The nominal values of C, I_C and m were chosen to be 0.5 pF, 20 μA and 4, respectively. The resistors R, R_{B1} and R_{B2} were realized with 150-kΩ R-poly1, 4.35-kΩ R-poly1 and 3.3-kΩ R-nwell. Using the above parameters and biasing conditions, the oscillation frequency of 21.14 MHz was obtained with an average $TC(f_{osc})$ of 20.59 ppm/°C over a temperature range of $-40\,^{\circ}$C to $+120\,^{\circ}$C, as depicted in Fig. 3.16 (in blue). The frequency variations of the proposed oscillator was also examined at other oscillation frequencies by changing only the values of C to 0.25 pF, 0.75 pF, and 1.0 pF, and thus the oscillation frequency was changed to 34.26 MHz, 15.43 MHz,

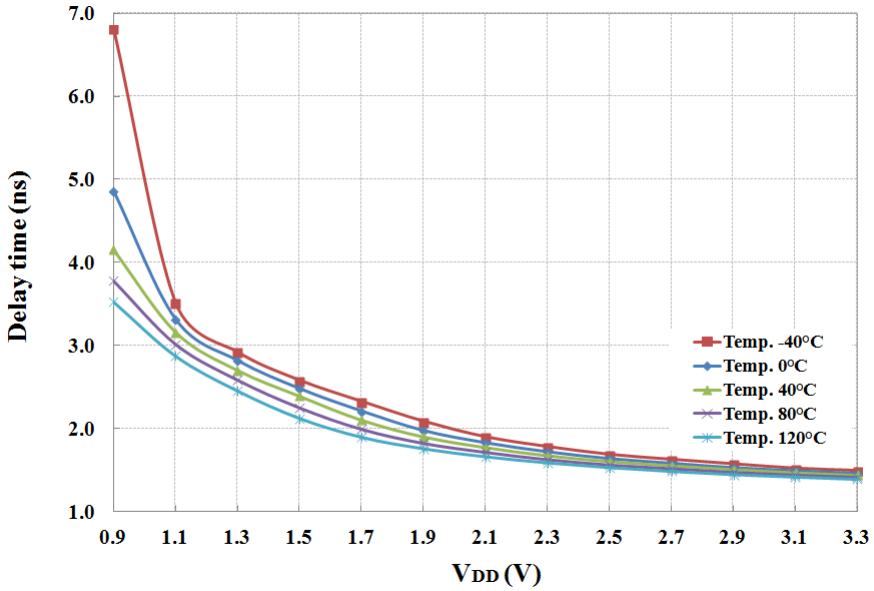


Figure 3.13: The optimum V_{DD} for resulting to the delay time insensitive temperature.

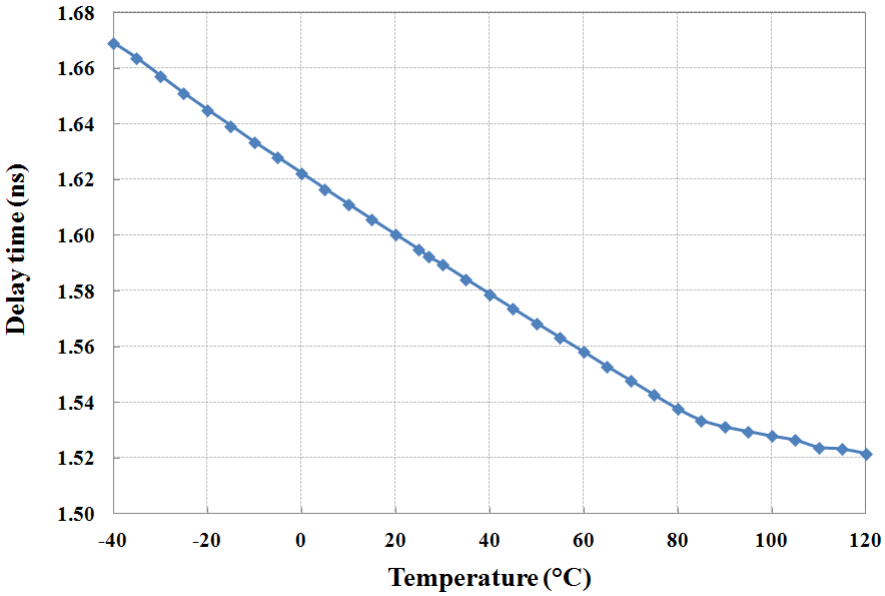


Figure 3.14: Temperature curve of the time delay at power supply voltage of 2.5-V.

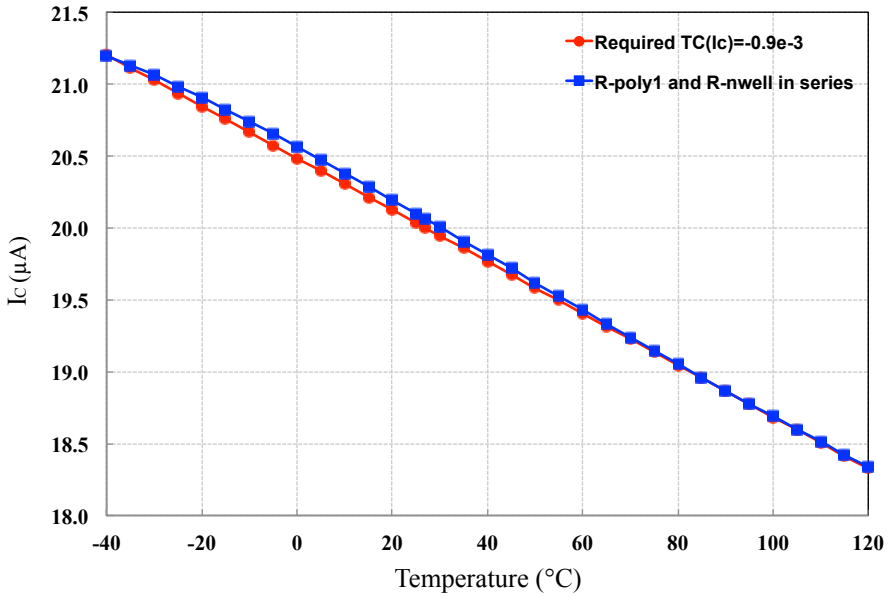


Figure 3.15: Simulated temperature variations of I_C generated by the constant-g_m biasing circuit with R_{B1} and R_{B2} realized by R-poly1 and R-nwell, respectively.

and 12.19 MHz, respectively. Simulations were performed without re-optimization and the resultant frequency variations were plotted in Fig. 3.16. The average $TC(f_{osc})$ of the three cases are less than 65 $^{ppm}/^{o}C$ over the temperature range of $-40^{o}C$ to $+120^{o}C$. Note that the frequency variation is increased when C is increased because the discharging time t_d is increased and becomes a larger proportion of T_{osc} and thus it's variation cannot be ignored. On the other hand, the frequency variation is also increased when C is decreased because the charging time t_c is decreased and thus t_d and t_p become significant proportions of T_{osc} and their variations cannot be ignored.

Figure 3.17 shows the physical layout of the proposed oscillator with $C = 0.5$ pF and it occupies an active area of 0.016 mm^2. Post-layout simulation showed that the average $TC(f_{osc})$ increased to 34.16 $^{ppm}/^{o}C$, as shown in Fig. 3.16. The effects of mismatch and process variations on the variations of f_{osc} were evaluated by performing Monte-carlo simulations. Figures 3.18(a) and (b) plot the simulated 100-sample histograms of f_{osc} at 21.14 MHz under mismatch and process variations, respectively. The resultant frequency deviations are 1.17% (0.247 MHz) and 21.4% (3.947 MHz) under mismatch and process variations, respectively. Thus, the oscillation frequency is very robust under parameter mismatches.

One drawback of the oscillator in Fig. 3.12 is that the output voltage has a very small duty cycle, however this can be overcome easily by replacing the discharging MOSFET switch with a constant discharging current source. The modified oscillator is depicted in Fig. 3.20, where M_2 (in Fig. 3.12) now realizes a constant discharging current source (I_D) which is a replica of the reference current. The charging (I_C) and discharging currents are turned on and off alternately by MOSFET switches, M_{16} and M_{17}. The duty cycle is simply determined by the ratio of $I_C/(I_C+I_D)$. Since both I_C and I_D are replicas of the reference current, their temperature variations will be closely matched and their effects to the oscillation time period and duty cycle will be canceled out.

The modified current-controlled relaxation oscillator circuit to adjusting a larger of the duty cycle, consists of an integrating capacitor (C), a charging current source (I_C), a discharging current source (I_D), a reference current (I_R), a resistive source-degeneration transconductor (formed by M_1 and R), controlled switches (S_1 and S_2) and a current-mode comparator as shown in Fig. 3.19(a). The transconductor is used to convert the capacitor voltage (V_C) to a current (I_1) in order to compare with the constant reference current I_R. The resultant current ($I_x = I_R - I_1$) is applied to the current-mode comparator. The simple source-degeneration transconductor is employed in order to achieve high oscillation frequency and low power consumption. The operation of the

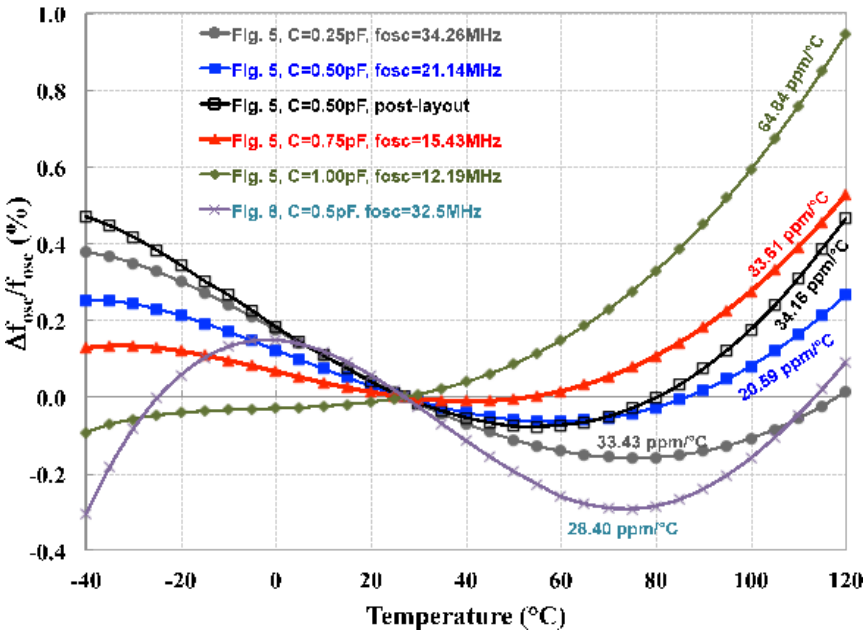


Figure 3.16: Simulated temperature variations of the oscillation frequencies.

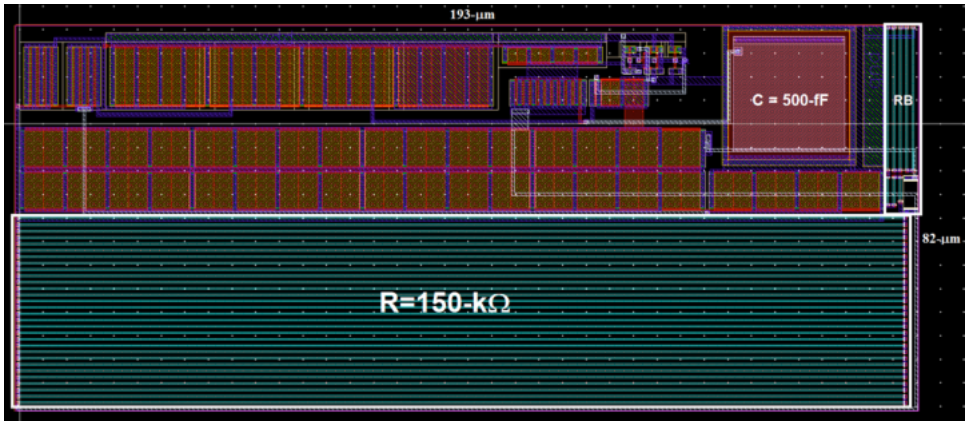
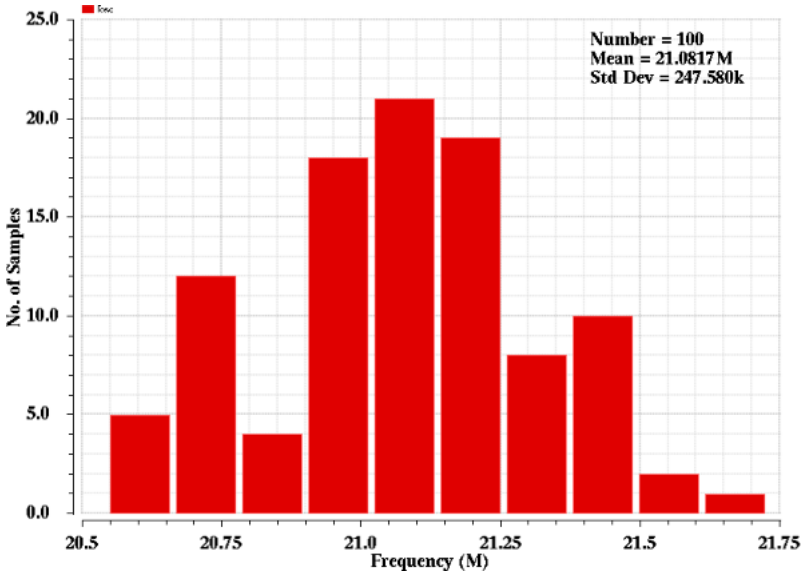
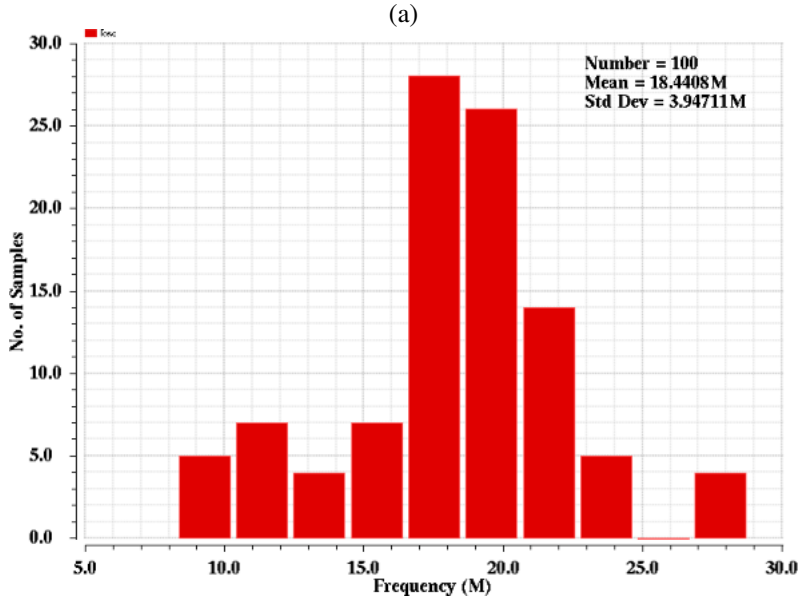


Figure 3.17: Layout of the proposed oscillator



(a)



(b)

Figure 3.18: Monte-carlo simulation results of f_{osc} with (a) mismatch and (b) process variations.

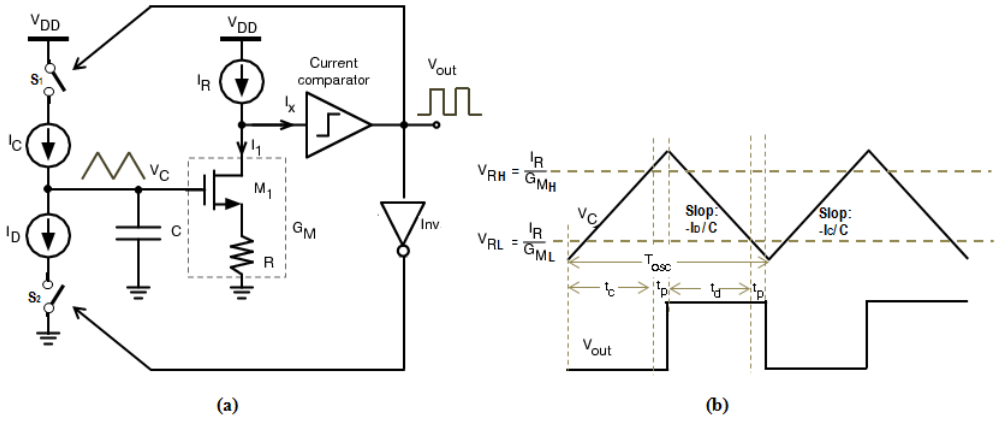


Figure 3.19: (a) Simplified circuit diagram of the proposed relaxation oscillator and (b) its voltage waveforms.

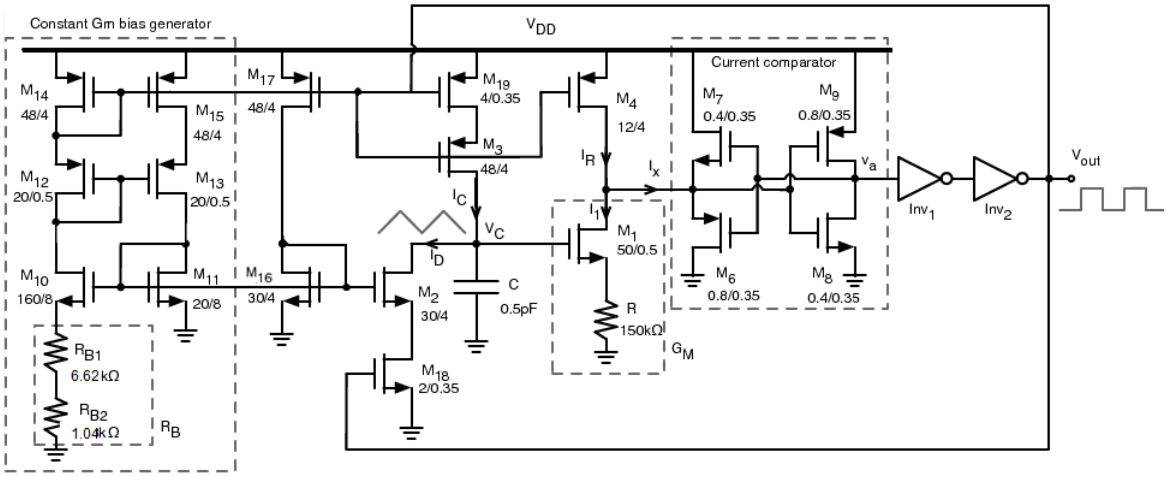


Figure 3.20: The proposed relaxation oscillator.

proposed oscillator can be explained as follows.

Suppose initially that switch S_1 is OFF and switch S_2 is ON , I_C will charge the integrating capacitor to raise V_C and I_1 When I_1 exceeds I_R or $I_1 > I_R$ (i.e. $I_x < 0$) then V_{out} is HIGH and S_1 is turned on and S_2 is turned off , then I_D will discharge the capacitor to lower V_C and I_1. When $I_1 < I_R$, V_{out} goes LOW and turns off S_1 and turns on S_2, and the cycle is repeated. Thus the capacitor is charged and discharged periodically by I_C and I_D, respectively. The waveforms of the capacitor (V_C) and output voltages (V_{out}) are depicted in Fig. 3.19(b), which shows that V_C swings between the equivalent upper and lower threshold voltages of V_{RH} and V_{RL}, respectively. The values of V_{RH} and V_{RL} are approximately given by

$$V_{RH(L)} = \frac{I_R}{G_{MH(L)}} = I_R \left(R + \frac{1}{g_{m1H(L)}} \right) \tag{3.25}$$

where $G_{MH(L)}$ and $g_{m1H(L)}$ are the transconductances of the transconductor and M_1 during the charging (with subscript H) and discharging periods (with subscript L). Due to the body effects of M_1, the values of g_{m1} during the charging and discharging periods are different, which leads to different values of V_{RH} and V_{RL}.

The period of oscillation (T_{osc}) is still given by (3.10), where t_c is the charging time due to I_C, t_p is the propagation delay time of the comparator and t_d is the discharging time due to I_D. For oscillation frequencies in the range of tens of MHz, it can be assumed that t_p is much less than t_c and t_d, and $T_{osc} \approx t_c + t_d$.

Considering the time-domain waveforms of V_C and V_{out} in Fig. (3.19), the period of oscillation (T_{OSC}) is changed from (3.10) to (3.26) as

$$T_{osc} = t_c + 2t_p + t_d \approx t_c + t_d. \tag{3.26}$$

From (3.25), the voltage swing of V_C is approximately given by

$$\triangle V_C = V_{RH} - V_{RL} = I_R \left(\frac{1}{G_{MH}} - \frac{1}{G_{ML}} \right) \tag{3.27}$$

Thus assuming that $I_R = mI_C$, T_{osc} can be easily derived as given by

$$T_{osc} \approx t_c + t_d = \frac{C\triangle V_C}{I_C} + \frac{C\triangle V_C}{I_D} \tag{3.28}$$

$$= \left(\frac{1}{G_{MH}} - \frac{1}{G_{ML}} \right) Cm \left(1 + \frac{I_C}{I_D} \right) \tag{3.29}$$

From (3.29), when $I_C = I_D$ we have $t_c = t_d$ and V_{out} will have 50% duty cycle. The duty cycle is simply determined by the ratio of $I_C/(I_C+I_D)$.

The temperature dependence of a parameter can be characterized by the fractional temperature coefficient (TC). The TC of T_{osc} ($TC(T_{osc})$) can be calculated by (3.30).

$$TC(T_{osc}) = \frac{1}{T_{osc}} \frac{\partial T_{osc}}{\partial T} \tag{3.30}$$

For the proposed circuit in Fig. 3.19(a), the $TC(T_{osc})$ can be derived from (3.29) as given by (3.31).

$$TC(T_{osc}) = -\frac{1}{G_{MH}} \frac{\partial G_{MH}}{\partial T} + \frac{1}{G_{ML}} \frac{\partial G_{ML}}{\partial T} + \frac{1}{C} \frac{\partial C}{\partial T} + \frac{1}{I_C} \frac{\partial I_C}{\partial T} - \frac{1}{I_d} \frac{\partial I_D}{\partial T} \tag{3.31}$$

$$= -TC(G_{MH}) + TC(G_{ML}) + TC(C) + TC(I_C) - TC(I_D) \tag{3.32}$$

In the same case the $TC(C)$ is negligible, and when both I_C and I_D are replicas of the same reference current, their temperature variations will be closely matched and their effects to the oscillation time period and duty cycle will be canceled out, e.g. $TC(I_C) \approx TC(I_D)$. Therefore,

$$TC(T_{osc}) \approx -TC(G_{MH}) + TC(G_{ML}) \tag{3.33}$$

Ideally, the temperature coefficients $TC(G_{MH})$ and $TC(G_{ML})$ are equaled since they are derived from the same transconductor circuit so they will cancel out in (3.33) and $TC(T_{osc})$ will be approximately zero. However, in practice, $TC(G_{MH})$ and $TC(G_{ML})$ will be slightly different due to higher-order effects thus $TC(T_{osc})$ will be somewhat larger.

Fig. 3.20 shows the schematic diagram of the proposed oscillator. The conventional constant-g_m bias current generator, realized by $M_{10} - M_{17}$, R_{B1} and R_{B2}, is used to provide the currents I_C and I_R via M_3 and M_4, respectively. The discharging MOSFET switch S_1 with a constant discharging current source (I_D) is used a replica of the reference current. The charging (I_C) and discharging currents are turned on and off alternately by MOSFET switches, M_{18} and M_{19}. The duty cycle is simply determined by the ratio of $I_C/(I_C+I_D)$. Since both

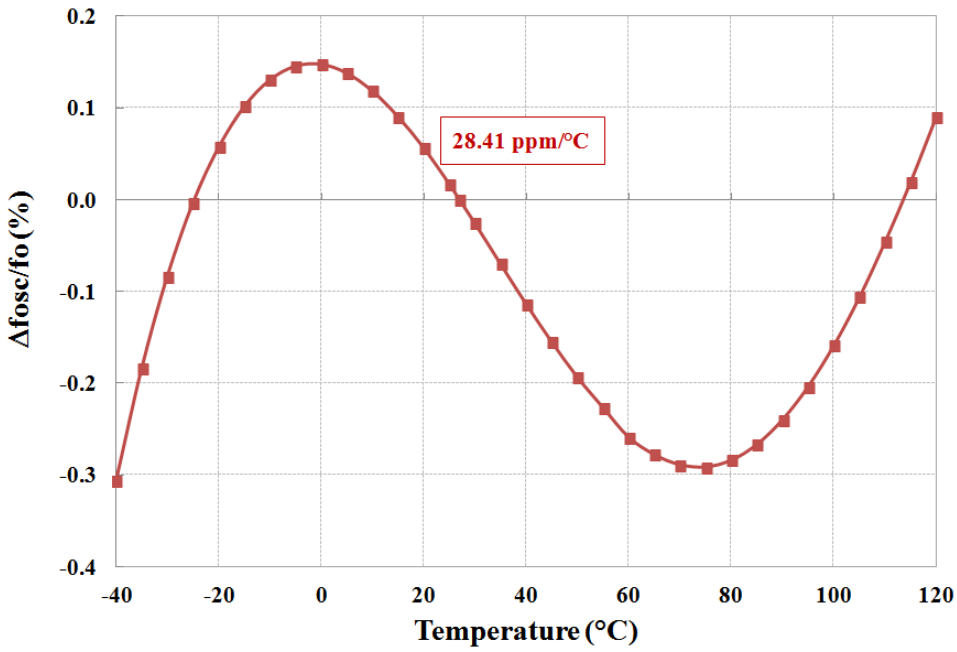


Figure 3.21: Simulated temperature variations of the oscillation frequencies.

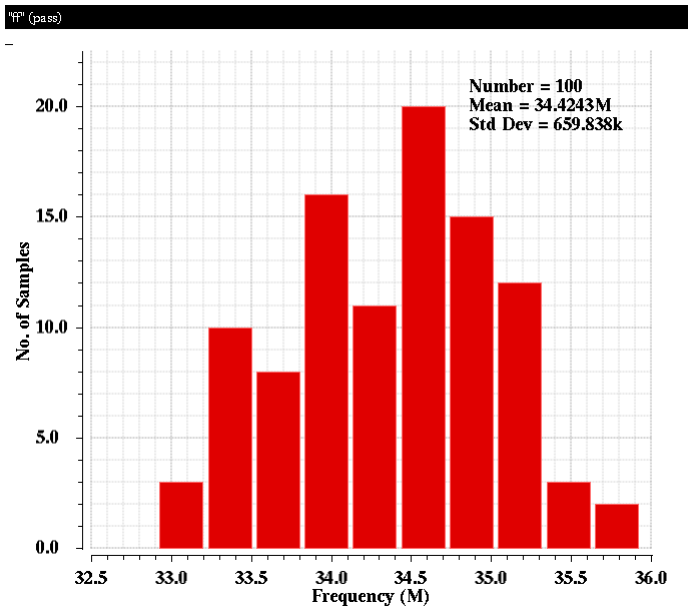
I_C and I_D are replicas of the reference current, their temperature variations will be closely matched and their effects to the oscillation time period and duty cycle will be canceled out. A high-speed capacitive-input current comparator [24], realized by M_6_M_9, is adopted. Rail-to-rail output voltage swing and short transition time are achieved by using an output CMOS inverters, Inv_1 and Inv_2.

The simulation results of the modified relaxation oscillator by using process parameters from a standard 0.35-μm CMOS technology. The circuit is designed to operate with a 2.5-V power supply voltage. A current comparator is remained to easily achieve the delay time (t_p) in the order of a few nanoseconds, thus t_p can be neglected for T_{osc} larger than tens of nanoseconds. For accurate temperature compensation, the period of oscillation (T_{osc}) should be greater than $10t_p$ (i.e. 20 nS) and thus f_{osc} should be limited to below 50 MHz. Simulation results with $V_{DD} = 2.5$ V showed that the fractional temperature coefficient of t_p was about -0.69$\times 10^{-3}$/°C.

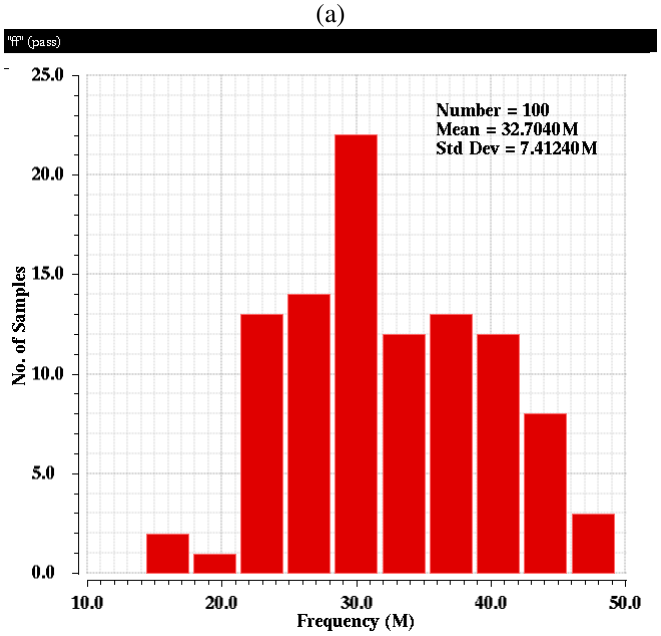
A nominal oscillation frequency of the proposed circuit can be operated about 30 MHz at room temperature of 27 °C. The nominal values of C, I_C and m are chosen to be 0.5 pF, 20 μA and 4, respectively. The resistors R, R_{B1} and R_{B2} are realized with 150-kΩ R-poly1, 6.62-kΩ R-poly1 and 1.04-kΩ R-nwell. Using the above parameters and biasing conditions, the oscillation frequency of 32.48 MHz is obtained with an average $TC(f_{osc})$ of 28.41 ppm/°C over a temperature range of -40 °C to $+120$ °C, as depicted in Fig. 3.21. The effects of mismatch and process variations on the variations of f_{osc} are evaluated by performing Monte-carlo simulations. Figures 3.22(a) and (b) plot the simulated 100-sample histograms of f_{osc} at 32.48 MHz under mismatch and process variations, respectively. Thus, the oscillation frequency is very robust under parameter mismatches.

The duty cycle of the output voltage of the circuit in Fig. 3.12 is about 5%. The modified oscillator in Fig. 3.20 was designed and simulated with $I_C = I_D = 20$ μA to achieve a duty cycle of 50%. The circuit oscillates at 32.5 MHz with an average $TC(f_{osc})$ of 28.4 ppm/°C over a temperature range of -40 °C to $+120$ °C, as also depicted in Fig. 3.16.

In principle, the proposed temperature-compensated oscillator can be realized using a state-of-the-art ultra deep submicron CMOS process because temperature coefficients of resistors and capacitors are not drastically different over process nodes. In practice, the circuit will generally face two main design issues including smaller power supply voltage and larger transistor mismatch. Smaller power supply voltages will increase



(a)



(b)

Figure 3.22: Monte-carlo simulation results of f_{osc} with (a) mismatch and (b) process variations.

Parameters	Fig. 3.12[s]	Fig. 3.20	[27][m]	[9][m]	[15][m]	[19][m]	[28]
Process (nm)	350	350	130	180	65	180	0.35
Supply (V)	2.5	2.5	1.0	1.8	1.2	1.8	1.2
Freq. (MHz)	21	32.48	1.24	1.1	12.6	14	10
Power (μW)	201	241.5	5.8	0.859	98.4	45	80
Temp (^oC)	-40 to 120	-40 to 120	-40 to 80	-20 to 80	0 to 80	-40 to 125	-20 to 100
TC ($^{ppm}/_{^oC}$)	34.16	28.41	-296	64.3	205	23.03	66.7
Area (mm^2)	0.016	-	0.016	0.075	0.01	0.04	-
FOM_1	168.1	171.9	149.5	163.4	159	172.8	162.7
FOM_2	186	-	167.5	174.7	178.9	186.7	-

Table 3.2: Performance summary and comparison.

the propagation delay time of the current-mode comparator and its contribution to the oscillation time period, however this effect can be counterbalanced by using minimum-length transistors. More importantly, the current generator circuit will suffer from reduced headroom voltage under small supply voltages. Transistors employed for the current generator and current mirrors should have large channel width and length to reduce mismatch and variation.

Table 3.2 shows the performance summary and comparison with other high-frequency relaxation oscillators by using FOM defined by (4.41) and (3.35). The calculated FOM of the proposed oscillators are 186 (the proposed oscillator) and 171.9 (the modified of the proposed oscillator), which is competitive with other oscillators. The proposed circuit achieves the lowest temperature coefficient with the highest oscillation frequency.

$$FOM_1 = 10\log\left(\frac{f_{osc}^2}{P_{diss}} \cdot \frac{1}{TC\,(f_{osc})}\right) \tag{3.34}$$

$$FOM_2 = 10\log\left(\frac{f_{osc}^2}{P_{diss} \cdot Area \cdot TC\,(f_{osc})}\right) \tag{3.35}$$

3.5 Summary

A temperature-compensated high-frequency current-controlled relaxation oscillator has been described. Source-degenerated transconductor and current-mode comparator are used to achieve high speed and low power dissipation. Temperature compensation is achieved by using suitable composite resistors and temperature compensated current sources. Simulation results showed that the proposed circuit could operate at 21-MHz oscillation frequency with an average TC of 20.59 $^{ppm}/_{^oC}$ over a temperature range of -40^oC to $+120^oC$, while dissipating 201 μW from a single 2.5-V power supply voltage. Due to the output voltage of the proposed relaxation oscillator has a very small duty cycle, but this can be overcome easily by replacing the discharging MOSFET switch with a constant discharging current source. The modified relaxation oscillator can be operated at 32.48-MHz oscillation frequency, while dissipating 241.5 μW from a single 2.5-V power supply voltage. The modified relaxation oscillator exhibits good frequency stability over a wide temperature range of -40^oC to $+120^oC$ with an average TC of 28.41 $^{ppm}/_{^oC}$. Therefore the proposed and the modified oscillator exhibits good frequency stability over a wide temperature range, which renders it viable as a frequency reference for short-range low-cost wireless communication systems.

Chapter 4

Low-phase noise CMOS ring oscillator

This chapter is concerned with the design and implementation of CMOS ring oscillators with low phase noise and is is organized as follows. Section 4.1 describes a brief review of previous works on low-phase noise ring oscillators and the analysis of phase noise of single-ended and differential ring oscillators. Section 4.2 describes the proposed low-power, low-phase noise CMOS ring oscillators. Finally, conclusion is given in section 4.3.

4.1 Analysis of Jitter and Phase Noise in CMOS Ring Oscillators

This section describes and review the analysis of jitter and phase noise in CMOS ring oscillators from the literature [29].

4.1.1 Relation between jitter and phase noise

Jitter and phase noise are fundamentally different, and the relationship is not obvious. The jitter is motivated by the issue that baseband communication systems specify clock purity in the time domain, either as the jitter in a single period of the clock, which is known as *period jitter*, or by *accumulated jitter* over N cycles of the clock. While phase noise of an oscillator specifies an oscillator's frequency instability in the frequency domain to indicate random accelerations and decelerations in phase (ϕ) as an oscillator orbiting at a nominally constant frequency (f_o) in steady-state. Fig. 4.1 shows an example of a noisy oscillatory waveform that is nominally free of DC and the period (τ) may be defined as the interval between successive zero crossings of the waveform with positive slope. A set of *discrete* random variables is the presence of phase noise $\{\tau\}$ and the standard deviation σ_τ is defined by the discrete sequence around the mean value of the *period jitter*. By contrast, the power spectrum density (PSD), $S_\phi(f)$ is used to specify a continuous random variable of the phase noise. We can derive the relation between the jitter and phase noise as follows [29].

The time period of an oscillatory waveform can be derived as

$$\tau_i = \frac{1}{2\pi f_o}\left(\phi\left(t_{i+1}\right) - \phi\left(t_i\right)\right) = \frac{1}{2\pi f_o}\Delta\phi_i \tag{4.1}$$

where ϕ is a continuously evolving variable and $\Delta\phi$ is calculated by the first-difference operation, which is, by subtracting it after a delay equal to the nominal period $1/f_o$. Thus, the spectral density $S_{\Delta\phi}(f)$ can be derived as

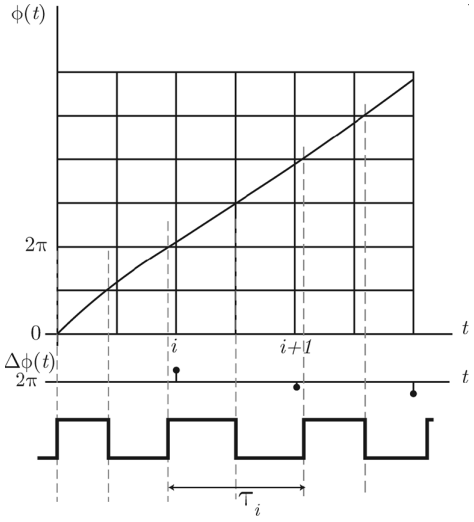


Figure 4.1: The relationship between phase noise and period jitter of the connection between phase of an oscillation [29]

$$S_{\Delta\phi}(f) = S_{\phi}(f)\,|1 - e^{-j2\pi f/f_o}|^2 = 4S_{\phi}(f)\,sin^2(\pi f/f_o)\,. \tag{4.2}$$

From (4.2) and (4.1), the *spectral density of jitter* can be expressed as

$$S_{\tau}(f) = S_{\phi}(f)\,\frac{sin^2(\pi f/f_o)}{(\pi f_o)^2}. \tag{4.3}$$

Equation (4.3) is the spectrum of the quantity τ sampled at f_o, and is defined only over the frequency range (0, $f_o/2$). In practice, the spectral density of jitter is usually indicated by its mean-square value σ_{τ}^2, as would be measured by a time-domain instrument such as a digital oscilloscope. Using the Wiener–Khinchine theorem, σ_{τ}^2 can be as expressed as

$$\sigma_{\tau}^2 = \int_0^{\infty} S_{\tau}(f)\,df = \int_0^{\infty} S_{\phi}(f)\,\frac{sin^2(\pi f/f_o)}{(\pi f_o)^2}df. \tag{4.4}$$

Equation (4.4) describes the general form of the relation between jitter and phase noise Consider a special case of (4.4) when all phase noise arises from white noise sources, the relationship between the single side band (SSB) phase noise PSD $\mathscr{L}(f)$ at moderate frequency offsets is given by

$$\mathscr{L}(f) = \frac{S_{\phi}(f)}{2} = \frac{S_w}{f^2} \tag{4.5}$$

where S_w is a coefficient specific to an oscillator and its noise sources. From (4.4) σ_{τ}^2 can be evaluated exactly as:

$$\sigma_{\tau}^2 = \frac{2}{\pi f_o^3} S_w \int_0^{\infty} \frac{sin^2 x}{x^2}dx = \frac{S_w}{f_o^3}. \tag{4.6}$$

Thus

$$\mathscr{L}(f) = \sigma_\tau^2 \frac{f_o^3}{f^2} \tag{4.7}$$

Equation (4.7) expresses the relationship between jitter and phase noise by analyzing only white noise sources. This equation will be used to analyze the phase noise of ring oscillators in the following sections.

4.1.2 Type of noise in ring oscillators

This section describes an analysis of phase noise of CMOS inverter-based single-ended ring oscillators. The following analysis describes an accurate estimation of the time delay of CMOS inverter and jitter or phase noise in ring oscillators. The propagation delay (t_d) of a CMOS inverter is defined as the time between when the input crosses the switching threshold or toggle point (V_M) of the inverter to when its output crosses the toggle point of the next inverter [29]. Figure 4.2 (a) shows the time-domain output waveform of a CMOS inverter, where the propagation delay is estimated by the gate delay of the CMOS inverter driving the input capacitance of the next stage to cross the trip point in response to an input step. In a practice, the input waveforms have a finite slope that are not ideal steps, which results in the case of balanced CMOS inverters with equal pull-up and pull-down. Therefore, a refinement of the calculation based on step response delay has to be performed to take into account the finite slope of the input ramp, as shown in Fig. 4.2(b). The delay in the first step of Fig 4.2 (b) is the time that it takes the ramp to reach the inverter toggle point, and the delay in the second step depends on the load capacitance and the ramp rate at the input. The delay between the first and second steps, τ_f, is roughly half of the remaining time for the input ramp to reach its final value. If $\tau_f \to 0$, then the delay with a step input [Fig. 4.2(b)] will be equaled to the estimation again. The input step is correctly located in time, because is measured from the time that the input crosses the toggle point. We will use this simplification in subsequent analysis.

A CMOS inverter that produces a voltage ramp at its output in response to a correctly positioned step input is modeled in this section for the analysis of phase noise in a ring oscillator. Jitter and phase noise due to white noise, control noise and flicker noise will be described. We will start by describing a basic CMOS inverter which is one delay stage of a ring oscillator. Then, we will describe a N-stage of inverter-based ring oscillator. Next, we will discuss the jitter and phase noise when a ring oscillator is used as a voltage-controlled oscillator (VCO) and we will discuss the phase noise due to VCO control signal or we call that the control noise. Finally, a ring oscillator phase noise due to flicker noise will be described.

Jitter and phase noise analysis due to white noise

The analysis of phase noise due to white noise sources of an inverter delay stage can be performed by considering signal and noise current as shown in Fig. 4.3. In case of a positive input step, the PMOS is shut off and the NMOS is biased in the saturation region. The NMOS pulls down the voltage on C from V_{DD} to 0. Then, the propagation delay t_d of the inverter delay stage is determined by the time from the input step to when the output ramp crosses the next inverter's toggle point, which is located at $V_{DD}/2$. Note that, an inverter with symmetrical toggle point results in unequal rise and fall times. The NMOS enters triode region when v_{out} crosses $(V_{DD} - V_{tN})$. If $(V_{DD} - V_{tN}) > (1/2)V_{DD}$, the NMOS will enter the triode region during the propagation delay, otherwise not. While the NMOS is in saturation, the discharge current is equaled to

$$I_{NMOS} = I_{DN_{sat}} = I_N = (1/2)\,\mu C_{ox}^{'}\,(W/L)\,(V_{DD} - V_{tN})^2 . \tag{4.8}$$

The discharging current in (4.8) will fall gradually in the triode region. Assuming that the drain current of the NMOS does not change significantly when it enters the triode region during t_{dN}. Thus, the output voltage crosses the toggle point with a slope given by

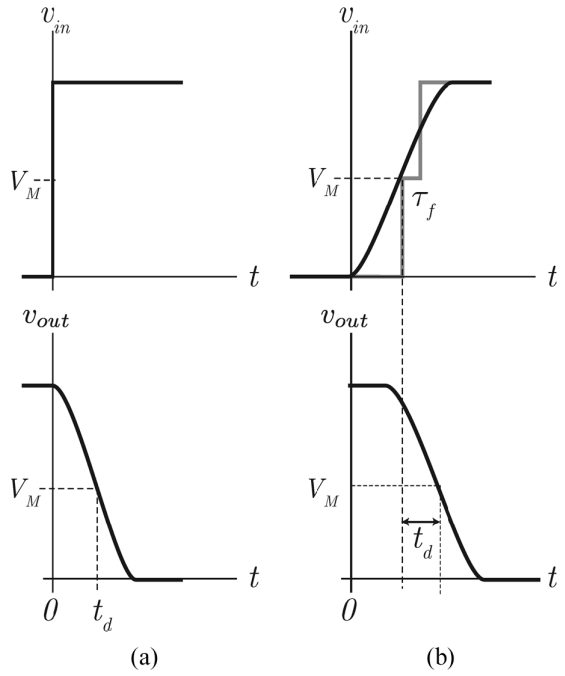


Figure 4.2: (a) Propagation delay defined in response to a step voltage input. (b) Realistic ramp input, which can be approximated by a two-step input for any fanout.

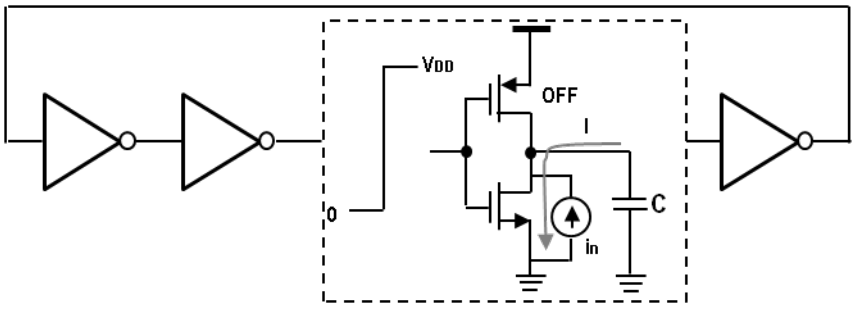


Figure 4.3: The analytical phase noise with inverter, is shown signal and noise current.

$$dv_{out}/dt = I_{DN_{sat}}/C. \tag{4.9}$$

The current in Fig. 4.3 is accompanied by noise i_n from the NMOS. Then, the spectral density of the noise can be given by

$$S_{i_nN} = 4kT\gamma_N g_{DS0} = 4kT\gamma_N g_m = 8kT\gamma_N \frac{I_{DN_{sat}}}{V_{DD} - V_{tN}}. \tag{4.10}$$

where g_{DS0} is the zero-bias drain source conductance and γ_N is the coefficient of NMOS for long-channel devices in the saturation region. i_n is a noise current that integrates on a capacitor C over an interval t_d. The resulting voltage v_n is given by

$$v_n = \frac{1}{C}\int_0^{t_d} i_n dt \tag{4.11}$$

The capacitor C integrates noise into voltage over the window $t_d = t_{dN}$. This voltage varies randomly at a rate that is inversely proportional to t_{dN}, advancing or delaying the instant of threshold crossing. The dynamics of the threshold crossing are described by

$$\int_0^{t_{dN}} \frac{I_N + i_{nN}}{C} dt = \frac{V_{DD}}{2} \tag{4.12}$$

where t_{dN} is a random variable that arises from noise current. The statistics of t_{dN} follow:

$$t_{dN} \equiv \langle t_{dN} \rangle = \frac{CV_{DD}}{2I_N} \tag{4.13}$$

and

$$\sigma^2_{t_{dN}} = \frac{1}{I_N^2}\left\langle \left(\int_0^{t_{dN}} i_{nN} dt \right)^2 \right\rangle. \tag{4.14}$$

The spectral density of t_{dN} can be calculated as

$$S_{t_{dN}} = \frac{t_{dN}^2}{I_N^2} sinc^2 (f t_{dN}) S_{iN} \tag{4.15}$$

and the Wiener–Khinchine theorem is used to find the mean-square value

$$\sigma^2_{t_{dN}} = \int_0^{\infty} S_{t_{dN}} df = \frac{t_{dN}}{\pi I_N^2} S_{i_nN} \int_0^{\infty} \frac{sin^2 x}{x^2} dx \tag{4.16}$$

Using (4.10) this simplifies to

$$\sigma_{t_{dN}}^2 = \frac{4kT\gamma_N t_{dN}}{I_N\left(V_{DD}-V_{tN}\right)}. \tag{4.17}$$

Equation (4.17) expresses the uncertainty in the propagation delay caused by current noise integrating on the capacitor C uncertainty in.

Prior to the switching event the channel resistance of the PMOS pull-up deposits an initial noise on the capacitor. The mean square noise and the associated jitter are

$$\left\langle v_n^2 \right\rangle = kT/C \tag{4.18}$$

Then, (4.17) can be rewritten by

$$\sigma_{t_{dP}}^2 = \frac{\left\langle v_n^2 \right\rangle}{\left(I_P/C\right)^2} = \frac{kTC}{I_P^2}. \tag{4.19}$$

Assuming $I_P = I_N$, thus, the total jitter due to these two uncorrelated white noise sources is

$$\sigma_{t_d}^2 = \frac{4kT\gamma_N t_{dN}}{I_N\left(V_{DD}-V_{tN}\right)} + \frac{kTC}{I_N^2}. \tag{4.20}$$

Suppose Fig. 4.3 is considered to be a ring oscillator by comprising N inverter delay stages. Therefore, the period of oscillation τ will be defined by the time it takes for a transition to propagate twice around the ring (t_{dN} and t_{dP}). The nominal frequency of oscillation f_o is given by

$$f_o = \frac{1}{N\left(t_{dN}+t_{dP}\right)} \simeq \frac{2}{NCV_{DD}}\left(\frac{1}{I_N}+\frac{1}{I_P}\right)^{-1} \simeq \frac{I/C}{NV_{DD}}. \tag{4.21}$$

We assume that the pull-up and pull-down currents are equal, whereas when the toggle point is symmetric at $(1/2)V_{DD}$, they are actually different.

Every propagation delay is jittered by noise in the pull-up or pull-down processes. These noise events are uncorrelated and add in the total mean-square jitter. Therefore, the variance of period jitter is given by

$$\sigma_\tau^2 = N\left(\sigma_{t_{dN}}^2 + \sigma_{t_{dP}}^2\right). \tag{4.22}$$

Using (4.20) and (4.21), and assuming that $V_{tN} = V_{tP} = V_t$, then σ_τ^2 can be written as

$$\sigma_\tau^2 = \frac{kT}{If_o}\left(\frac{2}{V_{DD}-V_t}\left(\gamma_N+\gamma_P\right)+\frac{1}{V_{DD}}\right)\left(\frac{f_o}{f}\right)^2 \tag{4.23}$$

Inverter stages toggle in sequence and the pull-up and pull-down processes are alternating. The pull-up current I charges an inverter's load C to V_{DD}, then the following inverter stage discharges its pre-charged C to ground. Thus, the average current that flows from the supply to ground is I . Thus the following conclusions can be drawn.

1) The phase noise is independent of the number, N, of delay stages, and depends only on the frequency of oscillation f_o.

2) The technology-dependent parameters are V_t and γ. Therefore the main design guideline is that large power supply voltage and current should be used to lower the phase noise. The desired oscillation frequency determines the number of stages.

Jitter and phase noise analysis due to control noise

A CMOS ring oscillator is widely used as the voltage-controlled oscillator (VCO), which is the critical building block in phase-locked loops (PLLs). Therefore, noise on the frequency tuning voltage or current is an important factor for phase noise of a ring oscillators. In case of a current-starved inverter, the control voltage V_C imposes a sensitivity κ_V on the nominal frequency f_o, then the resulting phase noise can be expressed by [29]

$$\frac{\partial f_o}{\partial V_C} = \kappa_V \Rightarrow S_{f_o}(f) = \kappa_V^2 S_{V_C}(f) \Rightarrow \mathscr{L}(f) = \frac{\kappa_V^2}{4f^2} S_{V_C}(f). \tag{4.24}$$

The supply voltage V_{DD} has a significant impact on the inverter delay. The switching of nearby digital circuits can cause disturbances to an oscillator, which can modulate the delay in all the inverters connected to the perturbed supply voltage. The delay modulation is correlated between the inverters. Even if the power supply voltage to the oscillator is well-regulated and filtered, flicker noise will probably be present at the regulator output. Its effect can be estimated by finding the κ_V and applying (4.24).

Equation (4.21) shows that the oscillation frequency of a ring oscillator depends on V_{DD}, and this dependence can be made clear assuming that C is only due to the gate capacitance:

$$f_o = \frac{\mu}{2L^2N} \frac{(V_{DD} - V_t)^2}{V_{DD}} \tag{4.25}$$

so that

$$\kappa_{V_{DD}} = \frac{\partial f_o}{\partial V_{DD}} = \frac{\mu}{2L^2N} \left(1 - \frac{V_t^2}{V_{DD}^2}\right) \simeq \frac{\mu}{2L^2N} \tag{4.26}$$

Clearly, MOSFETs with long channel length should be employed to desensitize the inverter-based voltage-controlled oscillator (VCO) against supply voltage noise.

At high frequencies, MOSFET capacitance will further raise the supply sensitivity. This is the main weakness CMOS inverter that it cannot usually be a precise delay element.

Jitter or phase noise analysis due to flicker noise

Flicker $(1/f)$ noise in MOSFET's is becoming an ever more important problem with shrinking transistor sizes. The $1/f$ noise should be analyzed from first principles because it is qualitatively different, and invokes different mechanisms of jitter and phase noise. Pull-up and pull-down currents contain flicker noise which may not fluctuate over a single transition, but varies slowly over many transitions. The noise arising in every MOSFET is, of course, uncorrelated.

Assuming I_{nk} and I_{pk} are the pull-down and pull-up currents supplied, respectively, by the NMOS and PMOS in the k-th stage of an N-stage ring oscillator. Then the period of oscillation and frequency f_o can be derived as

$$\tau = \frac{CV_{DD}}{2}\left(\frac{1}{I_{n1}}+\frac{1}{I_{p2}}+\ldots+\frac{1}{I_{pN}}+\frac{1}{I_{p1}}+\frac{1}{I_{n2}}+\ldots+\frac{1}{I_{nN}}\right) \tag{4.27}$$

$$f_o = \frac{2}{CV_{DD}}\left(\sum_{j=1}^{N}\frac{1}{I_{nj}}+\frac{1}{I_{Pj}}\right)^{-1} \tag{4.28}$$

In case of the symmetrically designed inverter, that is the pull-up and pull-down currents are equal to I, the expression for frequency is identical to (4.21). The sensitivity of f_o to the pull-down current in the k-th inverter is

$$\frac{\partial f_o}{\partial I_{nk}} = \frac{2}{CV_{DD}}\left(\sum_{j=1}^{N}\frac{1}{I_{nj}}+\frac{1}{I_{pj}}\right)^{-2}\frac{1}{I_{nk}^2} \tag{4.29}$$

$$= \frac{CV_{DD}f_o^2}{2I_{nk}^2} = \frac{f_o}{2NI}. \tag{4.30}$$

A VCO gain is expressed in (4.29), then, using (4.24), the SSB phase noise resulting from flicker noise of spectral density $S_{I_{nk}^2}^{1/f}$ in the k-th pull-down current is

$$\mathscr{L}(f) = \frac{1}{4f^2}\left(\frac{f_o}{2NI}\right)^2 S_{I_{nk}^2}^{1/f}(f) \tag{4.31}$$

and due to the uncorrelated contributions of the N NMOSs and PMOSs in the oscillator it is

$$\mathscr{L}(f) = \frac{1}{4f^2}\left(\frac{f_o}{2NI}\right)^2 \times N\left(S_{I_{nk}^2}^{1/f}+S_{I_{pk}^2}^{1/f}\right) \tag{4.32}$$

$$= \frac{1}{16NI^2}\left(S_{i_n}^{1/f}+S_{i_p}^{1/f}\right)\left(\frac{f_o}{f}\right)^2. \tag{4.33}$$

The spectral density of flicker noise in terms of MOSFET geometry and bias will be specified to obtain design insight. According to the flicker noise PSD in NMOS referred to the MOSFET gate as a voltage $v_n^{1/f}$ is given by the expression

$$S_{v_n}^{1/f} = \frac{K_{fn}}{WLC_{ox}^{'}f} \tag{4.34}$$

where K_{fp} and$K_{fn} \simeq 10^{-24}$ are the empirical coefficient of the expression holds for PMOS and NMOS, which are essentially independent of bias and technology, respectively. One can estimate an upper limit on the effects of flicker noise by setting $K_{fn} = K_{fp}$. To find the noise in the drain current we use (4.8) then,

$$S_{i_n}^{1/f} = g_m^2 S_{v_n}^{1/f} = \left(\frac{2I}{V_{DD}-V_t}\right)\frac{K_f}{WLC_{ox}^{'}f}. \tag{4.35}$$

The final expression for SSB phase noise induced by flicker noise is

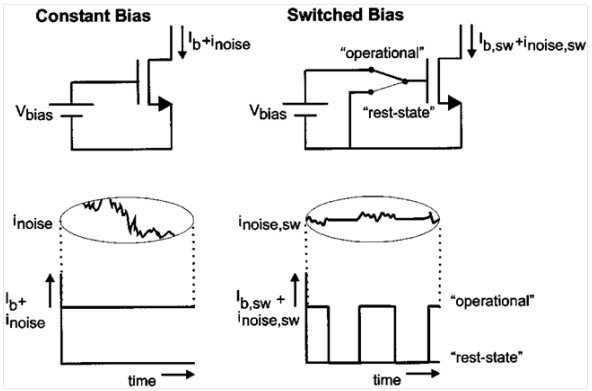


Figure 4.4: Concept of switched biasing ($V_T > 0$).

$$\mathscr{L}(f) = \frac{1}{4N(V_{DD}-V_t)^2}\left(\frac{K_{fn}}{W_nL_n}+\frac{K_{fp}}{W_pL_p}\right)\left(\frac{f_o^2}{f^3}\right) \tag{4.36}$$

$$= \frac{C_{ox}^{'}}{8NI}\left(\frac{\mu_nK_{fn}}{L_n^2}+\frac{\mu_pK_{fp}}{L_p^2}\right)\left(\frac{f_o^2}{f^3}\right). \tag{4.37}$$

Note that the lower flicker noise up conversion into phase noise can be designed by choosing large W/L to burn as much current in the oscillator as the budget allows, and use MOSFETs with the longest practical channel . As the ring oscillator's average bias current does not depend on the number of stages N, use the largest number of stages. These guidelines will also lower phase noise due to white noise sources.

$1/f$ noise in MOSFET's is becoming an ever more important problem at shrinking transistor sizes. It is one of the factors limiting the achievable dynamic range of electronic MOS circuits. The problem of noise in MOSFET's is introduced by Bram Nauta and members that noise reduction by increasing device dimensions comes at the cost of speed or power consumption. The techniques to reduce noise is presented by cycling a transistor between strong inversion and accumulation for an NMOS to clarify the difference with the switched biasing technique. Figure 4.4 shows the principle of switched biasing and compares it to constant biasing. Note that an active state in strong inversion which it contributes to the functional operation of a circuit. While an inactive state, the MOS transistor is not operational which is introduced reducing the noise of the MOS transistor during its operational state.

Thus, the basic idea of ring oscillator that can reduce $1/f$ noise by using a current-starved CMOS ring oscillator delay stage is proposed in this section.

4.2 Low Phase Noise Ring Oscillator Design

In this section demonstrates the technique for low noise of ring oscillator. A current-starved CMOS ring oscillator which highlights the switched biasing technique of control voltage, V_{CTL} dependence of phase noise. The current-starved with the switched biasing technique of control voltage. Next the circuit is improved a voltage swing by using latch-inverter technique to minimizing phase noise.

To minimize phase noise from fundamental sources such as thermal noise, the oscillation's amplitude should be maximized, which is more easily achieved with a single-ended delay stage. A CMOS single-ended ring oscillator in Fig. 4.8 does not allow easy frequency tuning method so we opt for a current-starved delay stage as shown in Fig. 4.5.

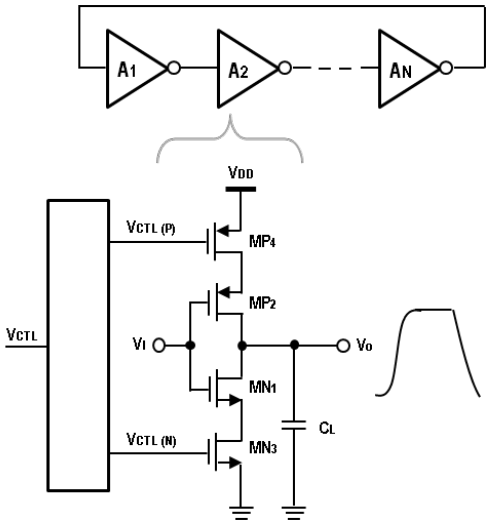


Figure 4.5: A current-starved ring delay stage.

4.2.1 The concept of the proposed of low noise ring oscillators design

The stage delay and oscillator frequency can be controlled by the bias current of the starved inverter, which is governed by the series PMOS and NMOS transistors operating either in saturation or triode regime as in Fig. 4.5. the transistors MN_3 and MP_4, limit the current available for charging and discharging the load capacitance C_L. The oscillator control voltage V_{CTL} may be separated into two control voltages $V_{CTL(N)}$ and $V_{CTL(P)}$. In practice, there will be some mismatches so rising and falling propagation delays will be unequal. An advantage of this technique is the wide tuning range, since the charging/discharging current can be varied over a wide range. The frequency of operation is determined by the delay of each element and the number of delay elements.

The single-ended ring oscillator is designed for the maximum operating frequency The minimum delay of single stage is determined by the current sourced/sunk by the active devices and the parasitics capacitance. When the current starving transistors, MP_4 and MN_3, Fig. 4.5, are operating in saturation the delay of each element can be approximated as

$$T_d \approx \frac{C_L}{2I_{PN}} V_{sw} \tag{4.38}$$

where C_L is load output capacitance, I_{PN} is the current provided by MP_4 or MN_3, which corresponds to charging/discharging current of C, and V_{sw} is a clock buffer (inverter) swing voltage (for MP_4 and MN_3 to stay in saturation, the voltage swing must be less than the supply voltage, V_{DD}). According to (4.38), linear delay variation, T_d, is possible to achieve if either C or V_{sw} varies linearly. In standard inverter's realization $V_{sw} = V_{DD}/2$. The signal goes through each of the M delay stages once to provide the first phase shift in a time of MT_d. Then, the signal must goes through each stage a second time to obtain the remaining phase shift, resulting in a total period of $2MT_d$. Therefore, the frequency of oscillation is

$$f_o = \frac{1}{2MT_d} \tag{4.39}$$

The delay of each inverter depends on its load capacitance as well as its biasing current from control voltage, V_{CTL}. Therefore, a control voltage source with a square wave signal switches the gate-source voltage of the NMOS and PMOS between two bias values. Figure 4.6 shows the proposed technique of a switched biasing control voltage to improve phase noise.

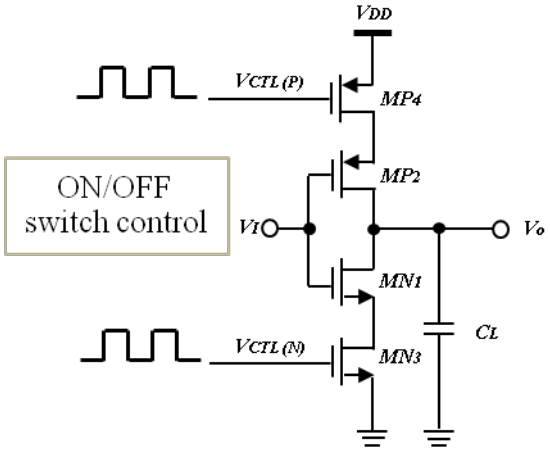


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Figure 4.6: The current-starved with the switched biasing technique of control voltage.

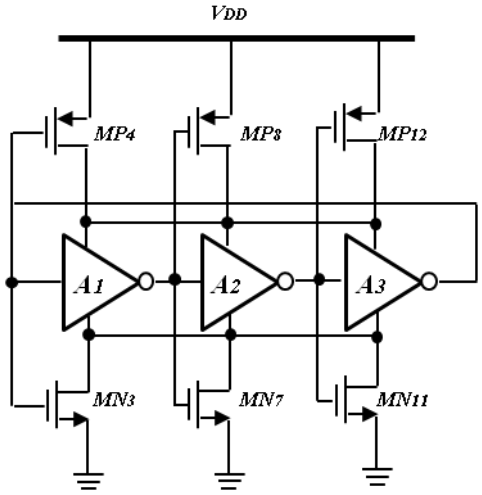


Figure 4.7: The current-starved with the switched biasing technique of control voltage.

One technique, that has been recently explored to make inverter based circuits less sensitive to process and temperature variations, is the self-biased method. This technique removes the biasing circuitry, thus, leading to a reduction in power and die area. Furthermore, as it will be proposed in this paper, self-biasing can further improve the phase noise of the ring oscillator by eliminating the unconverted low-frequency flicker noise caused by the traditional biasing circuitry. Moreover, variations in circuit performance due to deviations in biasing voltages can be reduced $1/f$ noise by using a switched biasing control voltage technique as shown in Fig.4.7.

Therefore, a low phase noise CMOS ring oscillator using a new self-biased inverter delay cell. The self-biased inverter delay cell is proposed to reduce phase noise of the oscillator. To validate the phase noise reduction of the proposed self-biased ring oscillator (SBRO), a conventional fixed bias current-starved three-stage ring oscillator (CBRO) was also designed and simulated for comparison. Both oscillators were designed with similar oscillation frequencies and current consumption, based on the current-starved with latch inverter structure. The self-biasing technique removes the biasing circuitry, thus, lead to a reduction in power and die area. Moreover, the self-biasing delay cell improves phase noise of the ring oscillator by eliminating the up-converted low-frequency flicker noise caused by the traditional fixed biasing circuitry [30]. A capacitor tuning technique was adopted in the ring oscillator to achieve frequency tuning.

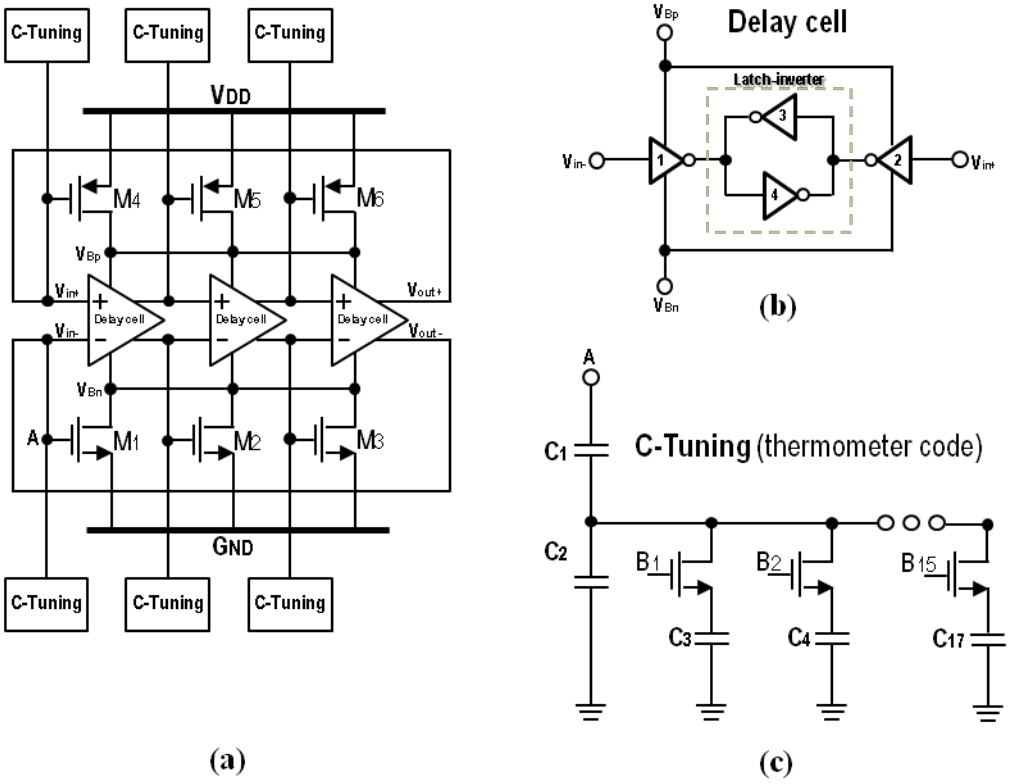


Figure 4.8: (a) Overall circuits of the proposed self-biased differential ring oscillator. (b) The latch-inverter delay cell. (c) Switched capacitor LSB implementation with thermometer code.

4.2.2 Low Phase Noise with self-biased inverter delay cell

Fig. 4.8 shows the schematic circuit diagram of the proposed differential ring oscillator. It consists of three identical differential inverter delay stages. Each stage is implemented with two CMOS inverters in Fig. 4.8(b), inv1 and inv2. A pair of cross-coupled inverters, inv3 and inv4, is used to achieve fast and full output voltage switching of the delay cell, which reduces the phase noise of the oscillator [30]. The CMOS inverters, inv1 and inv2, are realized by using the current-starved topology. Nodes V_{Bp} and V_{Bn}, which are the source terminals of PMOS and NMOS of the inverters, respectively, are connected to the biasing MOSFETs ($M_1 - M_6$). The gates of the biasing MOSFETs are connected to the output nodes of the inverters rather than a DC bias voltage as in the case of normal current-starved delay cell. Therefore the delay cell is self-biased. Since the gates of $M_1 - M_6$ are connected to the output nodes of the inverters, they are turned ON and OFF alternately and provide switching bias current to the inverters. Switching of biasing current can reduce the phase noise due to up-converted 1/f noise [31].

Since the delay cell is self-biased, the frequency of oscillation can be tuned and controlled by changing the inverters' load capacitance. This is achieved by using a switched capacitor array. The oscillation frequency of a ring oscillator is inversely proportional to the load capacitance. Increasing the capacitance reduces the oscillation frequency. In this work, the digitally-controlled switched capacitor tuning array in Fig. 4.8(c) is used to achieve fine frequency tuning. A 4-bit digital control word is used to switch the capacitor array, thus there are 15 MOSFET switches. The capacitors C_1 and C_2 are 10-fF and 200-fF, respectively. The capacitors $C_3 - C_{17}$ are equal to 30-fF. The change in capacitance when the nth MOSFET switch is turned ON is given by (4.40).

$$\Delta C = \frac{C_1 C_2 C_3 (C_1 + C_2)}{(C_1 + C_2 + kC_3)^2 - C_3 (C_1 - kC_3 + 1)} \tag{4.40}$$

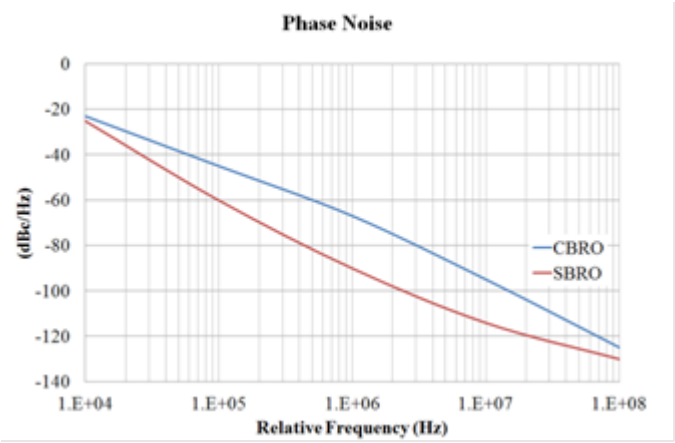


Figure 4.9: Simulated phase noise of the proposed ring oscillator vs. the conventional current-starved ring oscillator.

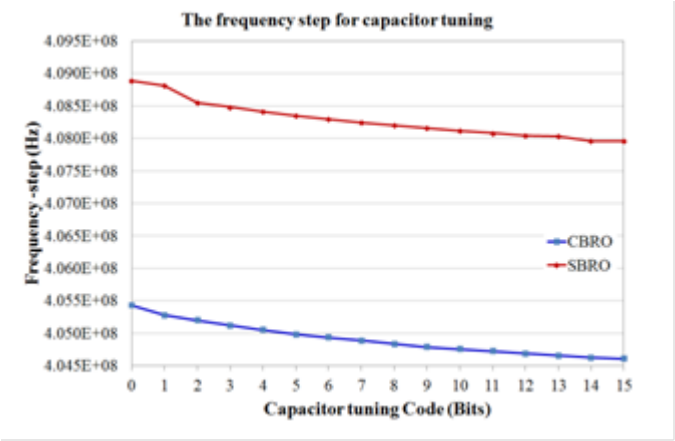


Figure 4.10: Fine frequency tuning characteristic of the proposed ring oscillator.

4.2.3 Simulation results

Fig. 4.9 plots the simulated phase noise of both ring oscillators. It can be seen that the phase noise of the proposed ring oscillator is about 20 dB lower than the conventional fixed bias current-starved ring oscillator. Note that the simulated phase noise at frequency offsets greater than 10MHz may be incorrect because the simulator model may be invalid as the frequency offsets is increased relative to the oscillation frequency (around 400 MHz). This validates the advantage of using the proposed self-biased inverter delay cell. Fig. 4.10 plots the fine frequency tuning characteristic of the proposed ring oscillator.

Table 4.1 summarizes and compares the simulated performance of the proposed oscillator. The conventional figure-of-merit (FOM) in (4.41) is used for comparison, where $\mathscr{L}(f)$ is the phase noise (dBc/Hz), Δf is the offset frequency, f is the oscillation frequency, and P_{DC} is the power dissipation. The proposed ring oscillator can achieve a FOM of -159.3.

$$FOM_4 = \mathscr{L}(f) + 10log\left(\left(\frac{\Delta f}{f}\right)^2 \frac{P_{DC}}{P_{REF}}\right) \tag{4.41}$$

Table 4.1: Performance summary.

Metrics	Proposed	CBRO	[32]
Technology (μm)	0.35	0.35	0.28
$V_{dd}(V)$	3.3	3.3	2.5
$\mathscr{L}(f)$@1MHz (dBc/Hz)	-113.62	-96.48	-96
$f_{osc}(MHz)$	409	405.5	2450
$P_{diss}(mW)$	4.44	3.11	19.2
FOM	-159.3	-143.7	-150.95

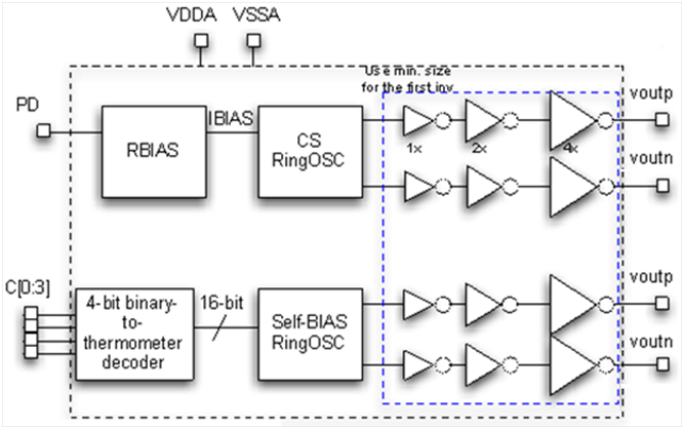


Figure 4.11: The overall circuit of the proposed transmitter.

4.2.4 Measurements

The proposed self-biased and current-biased oscillators were designed and fabricated by using process parameters from a 0.35-μm CMOS technology. Post-layout simulation of both ring oscillators showed that the circuits operate at 256-MHz and 252-MHz, respectively. Note that the oscillation frequency of both ring oscillators are lower than the designed values due to the layout parasitics capacitance. The block diagram of the proposed chip is shown in Fig. 4.11. A 4-bit binary-to-thermometer decoder circuit is used to control the frequency-tuning capacitor array. Both oscillators employ 4-stage buffer to drive the output off the chip. The chip micro photograph was shown in Fig. 4.12. The test board was shown in Fig. 4.13. With all bits of the capacitor tuning array shorted to ground, the maximum measured oscillation frequencies of the current-biased and the self-biased ring oscillator at the nominal temperature of 37C were about 250-MHz and 213-MHz, respectively. The measured fine frequency tuning characteristic of both ring oscillators were plotted in Fig. 4.14. Figures 4.15 show the measured phase noise of the self-biased and the current-bias ring oscillators at -104 dBc/Hz and -103 dBc/Hz, respectively.

Figures 4.15(a) and (b) show the measured power spectrums of the current-biased and the self-biased ring oscillators, which indicated the phase noise values at 1-MHz frequency offset of -104 dBc/Hz and -103 dBc/Hz, respectively. Note that, in fig. 4.15(a), the modulated sidebands located at +/-7.5 MHz away from the carrier frequency were caused by signal coupling from the output of the self-biased ring oscillator, which unfortunately could not be turned off due to mistakes in the prototype implementation.

4.3 Summary

This chapter presented a study and an analysis of low noise CMOS ring oscillators. We have successfully tied the design parameters for the optimization ring oscillators to the phase noise performance in such sys-

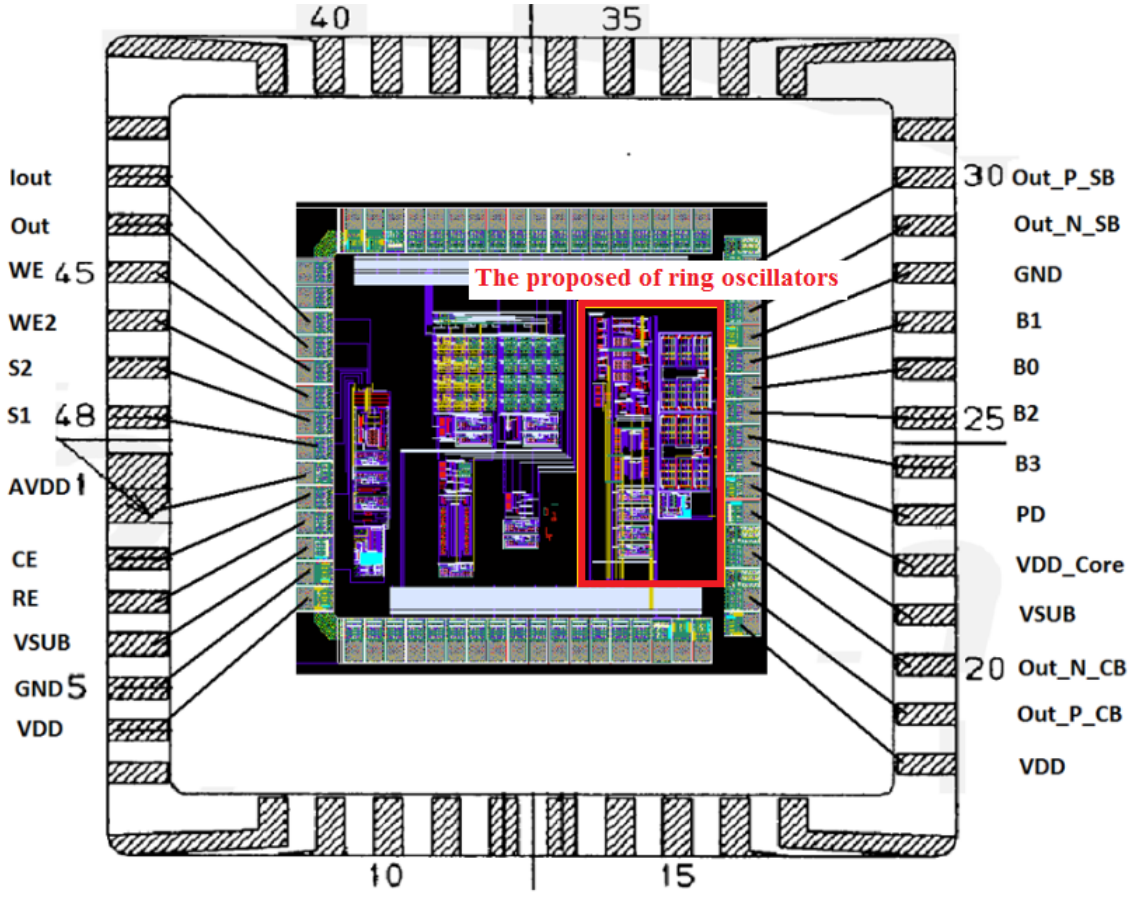


Figure 4.12: CMOS ring oscillator using the current-starved with latch inverter delay cell for MIC bands transmitter.

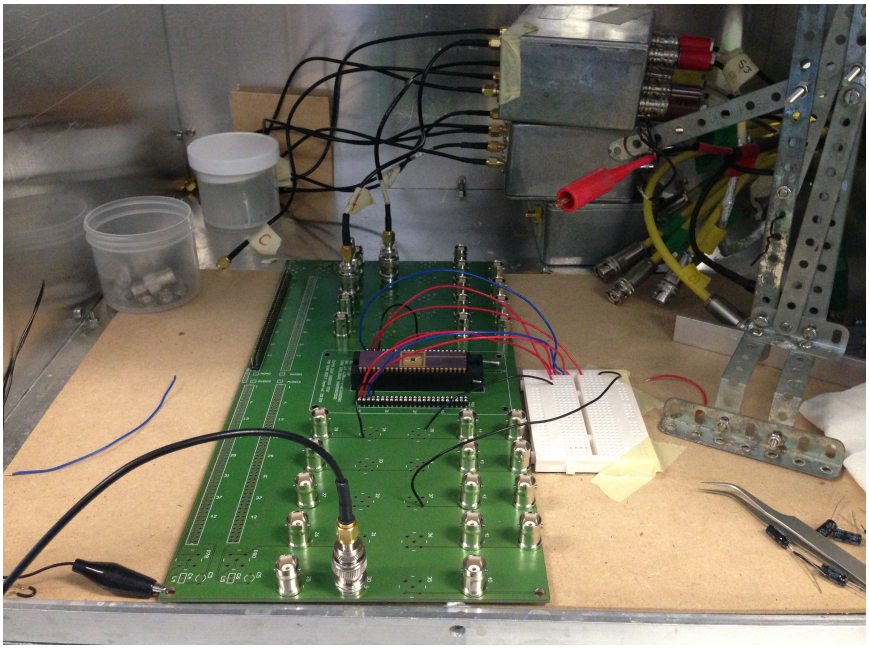


Figure 4.13: Test board.

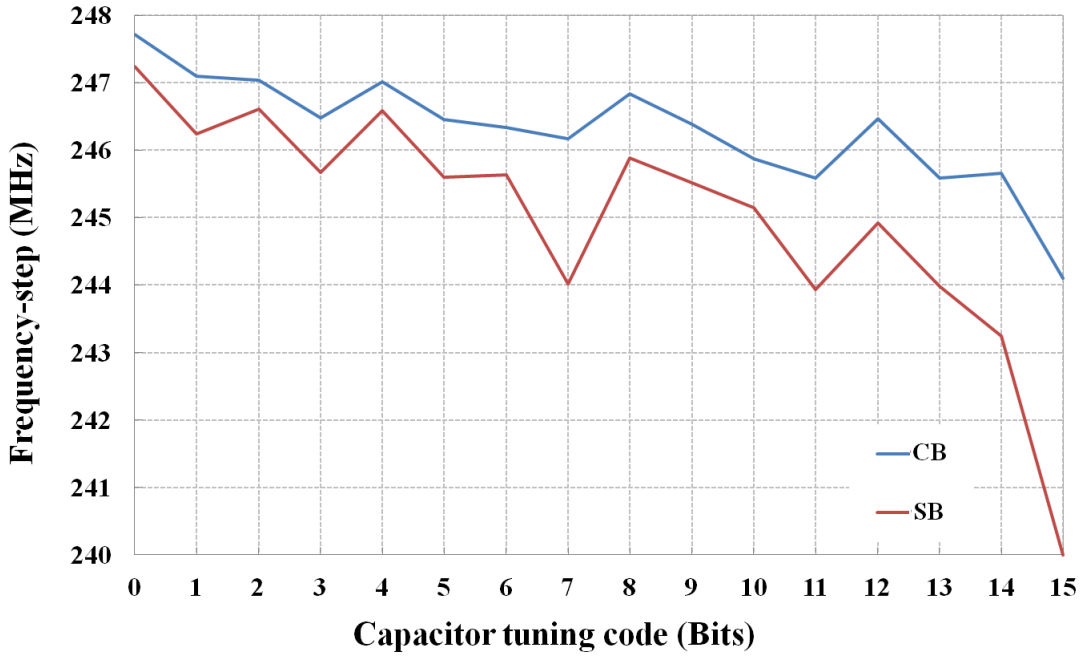
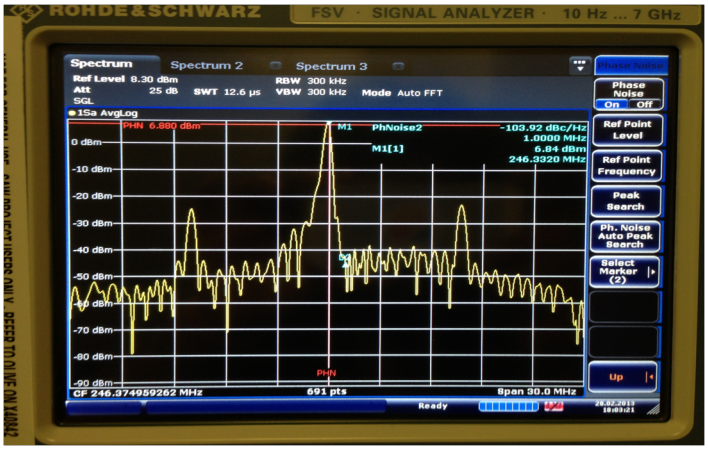
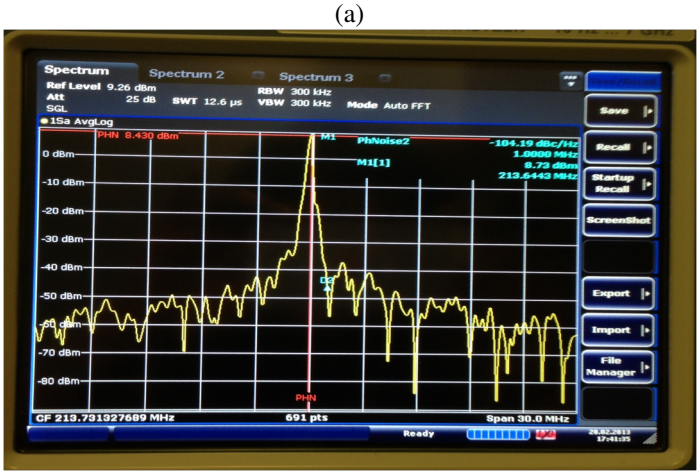


Figure 4.14: The measurement of the fine frequency tuning characteristic of the proposed ring oscillators.

tems. By illustrating the circuit designs that improve the phase noise characteristics of a single-ended ring oscillators. The proposed single-ended ring oscillator incorporates the switching biasing technique into the conventional current-starved topology, which results in a self-biased structure. The self-biased ring oscillator was designed and simulated by using process parameters from a standard 0.35-μm CMOS technology. The circuit is designed to operate with a 3.3-V power supply voltage and a nominal oscillation frequency of about 400 MHz at room temperature of 37 ^oC. Simulation results of the proposed ring oscillator achieved lower phase noise comparing to the conventional current-starved ring oscillator. The proposed self-biased and conventional current-starved ring oscillators were sent for fabrication. The performance of the prototype chip was measured. However, due to poor layout and under-estimated parasitics, there are large discrepancies between simulation and measurement results, in terms of oscillation frequency and phase noise.



(a)



(b)

Figure 4.15: The measured of the phase noise of the proposed ring oscillators (a) the current-bias and (b) the self-biased ring oscillators.

Chapter 5

Conclusion

This final chapter describes the conclusion drawn from the work carried out in this dissertation. The main research contributions of this dissertation have been on the study, analysis and design of CMOS temperature-compensated relaxation and low-noise ring oscillators, which were described in chapters 3 and 4, respectively.

In chapter 3, the analysis and design of a temperature-compensated high-frequency current-controlled relaxation oscillator was described. The structure of the proposed relaxation oscillator is based on the constant-current relaxation oscillator. A source-degenerated transconductor and a current-mode comparator are used to achieve high speed and low power dissipation. Temperature compensation is achieved by using suitable composite resistors and temperature compensated current sources. Simulation results showed that the proposed circuit could operate at 21-MHz oscillation frequency with an average TC of 20.59 $ppm/^oC$ over a temperature range of -40^oC to $+120^oC$, while dissipating 201 μW from a single 2.5-V power supply voltage. Therefore the proposed oscillator exhibits good frequency stability over a wide temperature range, which renders it viable as a frequency reference for short-range low-cost wireless communication systems.

In chapter 4, the analysis and design of a low noise CMOS ring oscillator were described. The proposed single-ended ring oscillator incorporates the switching biasing technique into the conventional current-starved topology, which results in a self-biased structure. The self-biased ring oscillator was designed and simulated by using Cadence Spectre with process parameters from a standard 0.35 um CMOS technology. The circuit was designed to operate with a 3.3-V power supply voltage and a nominal oscillation frequency of about 400 MHz at room temperature of 37 oC. Simulation results also suggested that the proposed ring oscillator was able to achieve lower phase noise comparing to the conventional current-starved ring oscillator, thanks to the switching biasing technique. The proposed self-biased and conventional current-starved ring oscillators were sent for fabrication. The performance of the prototype chip was measured. However, due to poor layout and under-estimated parasitics, there are large discrepancies between simulation and measurement results, in terms of oscillation frequency and phase noise.

Bibliography

[1] Asad A. Abidi. Phase noise and jitter in CMOS ring oscillators. *Solid-State Circuits, IEEE Journal of*, 41(8):1803–1816, 2006.

[2] Fabio Sebastiano, Lucien J. Breems, Kofi A. A. Makinwa, Salvatore Drago, Domine M. W. Leenaerts, and Bram Nauta. A 65-nm CMOS temperature-compensated mobility-based frequency reference for wireless sensor networks. *IEEE Journal of Solid-State Circuits*, 46(7):1544–1552, July 2011.

[3] Yi-Chun Shih and Brian Otis. An on-chip tunable frequency generator for crystal-less low-power WBAN radio. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 60(4):187–191, April 2013.

[4] Urs Denier. Analysis and design of an ultralow-power CMOS relaxation oscillator. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 57(8):1973–1982, August 2010.

[5] Si-Bo Huang, Jian-Guang Chen, Feng Yang, and Yu-Hua Cheng. Design of an ultralow-power CMOS relaxation oscillator for piezoresistive pressure sensor. In *2012 IEEE 11th International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, pages 1–3, October 2012.

[6] F. Herzel and B. Razavi. A study of oscillator jitter due to supply and substrate noise. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 46(1):56–62, January 1999.

[7] A Sempel and H. van Nieuwenburg. A fully-integrated HIFI PLL FM-demodulator. In *Solid-State Circuits Conference, 1990. Digest of Technical Papers. 37th ISSCC., 1990 IEEE International*, pages 102–103, February 1990.

[8] J. W. Smits, C. J M Verhoeven, and L. A D Van den Broeke. A 45mhz VCO Combining High Linearity With High Modulation Bandwidth. In *Solid-State Circuits Conference, 1991. ESSCIRC '91. Proceedings - Seventeenth European*, volume 1, pages 117–120, September 1991.

[9] A. Bellaouar, A. Fridi, M.I. Elmasry, and K. Itoh. Supply voltage scaling for temperature insensitive CMOS circuit operation. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 45(3):415–417, March 1998.

[10] Y.-H. Chiang and S.-I. Liu. A submicrowatt 1.1-MHz CMOS relaxation oscillator with temperature compensation. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 60(12):837–841, 2013.

[11] P.F.J. Geraedts, E. Van Tuijl, E.A.M. Klumperink, G.J.M. Wienk, and B. Nauta. A 90μW 12mhz Relaxation Oscillator with a –162db FOM. In *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pages 348–618, February 2008.

[12] S. L J Gierkink and E. van Tuij. A coupled sawtooth oscillator combining low jitter with high control linearity. *IEEE Journal of Solid-State Circuits*, 37(6):702–710, June 2002.

[13] K. Lasanen, Elvi Raisanen-Ruotsalainen, and J. Kostamovaara. A 1-V, self adjusting, 5-MHz CMOS RC-oscillator. In *IEEE International Symposium on Circuits and Systems, 2002. ISCAS 2002*, volume 4, pages IV–377–IV–380 vol.4, 2002.

[14] Yan Lu, Gang Yuan, L. Der, Wing-Hung Ki, and C.P. Yue. A 0.5% Precision On-Chip Frequency Reference With Programmable Switch Array for Crystal-Less Applications. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 60(10):642–646, October 2013.

[15] R. Navid, T.H. Lee, and R.W. Dutton. Minimum achievable phase noise of RC oscillators. *IEEE Journal of Solid-State Circuits*, 40(3):630–637, March 2005.

[16] Ying Cao, P. Leroux, W. De Cock, and M. Steyaert. A 63,000 Q-factor relaxation oscillator with switched-capacitor integrated error feedback. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, pages 186–187, February 2013.

[17] Paul F. J. Geraedts, Ed (A. J. M.) van Tuijl, Eric A. M. Klumperink, Gerard J. M. Wienk, and Bram Nauta. Towards minimum achievable phase noise of relaxation oscillators. *International Journal of Circuit Theory and Applications*, 42(3):238–257, March 2014.

[18] A. Paidimarri, D. Griffith, A. Wang, A.P. Chandrakasan, and G. Burra. A 120nW 18.5kHz RC oscillator with comparator offset cancellation for $\pm 0.25\%$ temperature stability. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, pages 184–185, February 2013.

[19] T. Tokairin, K. Nose, K. Takeda, K. Noguchi, T. Maeda, K. Kawai, and M. Mizuno. A 280nW, 100kHz, 1-cycle start-up time, on-chip CMOS relaxation oscillator employing a feedforward period control scheme. In *2012 Symposium on VLSI Circuits (VLSIC)*, pages 16–17, 2012.

[20] Y. Tokunaga, S. Sakiyama, A. Matsumoto, and S. Dosho. An on-chip CMOS relaxation oscillator with voltage averaging feedback. *IEEE Journal of Solid-State Circuits*, 45(6):1150–1158, 2010.

[21] K. Sundaresan, P.E. Allen, and F. Ayazi. Process and temperature compensation in a 7-MHz CMOS clock oscillator. *IEEE Journal of Solid-State Circuits*, 41(2):433 – 442, February 2006.

[22] B.R. Gregoire and Un-Ku Moon. Process-Independent Resistor Temperature-Coefficients using Series/Parallel and Parallel/Series Composite Resistors. In *IEEE International Symposium on Circuits and Systems, 2007. ISCAS 2007*, pages 2826–2829, May 2007.

[23] Yuchi Ni and Marvin Onabajo. A low-power temperature-compensated CMOS relaxation oscillator. *Analog Integrated Circuits and Signal Processing*, 79(2):309–317, May 2014.

[24] J. D B Soldera, M.T. Berens, and A. Olmos. A temperature compensated CMOS relaxation oscillator for low power applications. In *2012 25th Symposium on Integrated Circuits and Systems Design (SBCCI)*, pages 1–4, August 2012.

[25] H. Traff. Novel approach to high speed CMOS current comparators. *Electronics Letters*, 28(3):310 –312, January 1992.

[26] Yannis Tsividis and Colin McAndrew. *Operation and modeling of the MOS transistor*. Oxford University Press, New York, 2011.

[27] R. Dominguez-Castro, A. Rodriguez-Vazquez, F. Medeiro, and J.L. Huertas. High resolution CMOS current comparators. In *Solid-State Circuits Conference, 1992. ESSCIRC '92. Eighteenth European*, pages 242 –245, September 1992.

[28] A 1.2-MHz 5.8-uW Temperature-Compensated Relaxation Oscillator in 130-nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 61(5):334–338, May 2014.

[29] Junghyup Lee and SeongHwan Cho. A 10 MHz 80μW 67 ppm/^{o}C CMOS reference clock oscillator with a temperature compensated feedback loop in 0.18 μ m CMOS. In *2009 Symposium on VLSI Circuits*, pages 226–227, 2009.

[30] Liang Dai and R. Harjani. Design of low-phase-noise CMOS ring oscillators. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 49(5):328–338, May 2002.

[31] E.AM. Klumperink, S. L J Gierkink, AP. Van Der Wel, and B. Nauta. Reducing MOSFET 1/f noise and power consumption by switched biasing. *IEEE Journal of Solid-State Circuits*, 35(7):994–1001, July 2000.

[32] W. Rahajandraibe, L. Zai?d, V.C. de Beaupre, and G. Bas. Temperature Compensated 2.45 GHz Ring Oscillator with Double Frequency Control. In *2007 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pages 409–412, June 2007.

[33] Yan Lu, Gang Yuan, L. Der, Wing-Hung Ki, and C.P. Yue. A 0.5array for crystal-less applications. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 60(10):642–646, October 2013.

[34] V. De Smedt, P. De Wit, W. Vereecken, and M.S.J. Steyaert. A 66 μw 86 ppm/^{o}c fully-integrated 6 MHz wienbridge oscillator with a 172 dB phase noise FOM. *IEEE Journal of Solid-State Circuits*, 44(7):1990–2001, 2009.

[35] Joonsung Bae, Kiseok Song, Hyungwoo Lee, Hyunwoo Cho, and Hoi-Jun Yoo. A low-energy crystal-less double-FSK sensor node transceiver for wireless body-area network. *IEEE Journal of Solid-State Circuits*, 47(11):2678–2692, November 2012.

[36] Paul F. J. Geraedts, Ed (A. J. M.) van Tuijl, Eric A. M. Klumperink, Gerard J. M. Wienk, and Bram Nauta. Towards minimum achievable phase noise of relaxation oscillators. *International Journal of Circuit Theory and Applications*, pages 238–257, 2012.

[37] W.S.-T. Yan and H.C. Luong. A 900-MHz CMOS low-phase-noise voltage-controlled ring oscillator. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 48(2):216–221, February 2001.

APPENDICES

Appendix A : Publications

1. Siraporn Sakphrom, Pantelis Georgiou and Apinunt Thanachayanont, "A Sub-100 $ppm/^oC$ Temperature-Compensated High-Frequency CMOS Relaxation Oscillator," *Circuits Systems and Signal Processing,* ISSN 0278-081X Circuits Syst Signal Process DOI 10.1007/s00034-015-0057-x (2015)

2. Siraporn Sakphrom and Apinunt Thanachayanont, "Low Phase Noise CMOS Ring Oscillator Using Self-Biased Inveter Delay Cell," *2nd Asia-Pacific Conference on Antennas and Propagation (APCAP-2013)*, Page 203-204, Chiang Mai, Thailand, August 5-7, 2013

3. Siraporn Sakphrom and Apinunt Thanachayanont, "A Low-Power CMOS RF Power Detector," *19th The IEEE International Conference on Electronic, Circuit and Systems (ICECS 2012)*, Seville, Spain, 10-12 Dec. 2012.

I. A Sub-100 $ppm/^oC$ Temperature-Compensated High-Frequency CMOS Relaxation Oscillator : CSSP 2015

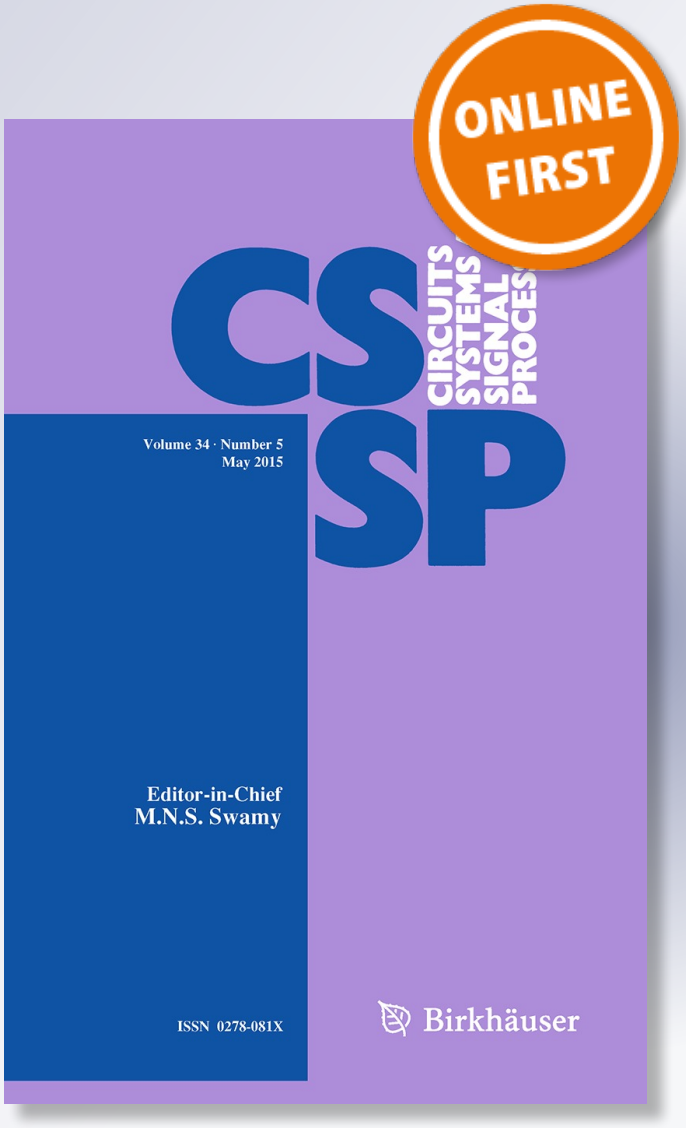
A Sub- $${100\,\hbox {ppm}/{^{\circ }\hbox {C}}}$$ 100 ppm / # C Temperature-Compensated High-Frequency CMOS Relaxation Oscillator

Siraporn Sakphrom, Pantelis Georgiou & Apinunt Thanachayanont

Circuits, Systems, and Signal Processing

ISSN 0278-081X

Circuits Syst Signal Process
DOI 10.1007/s00034-015-0057-x



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Circuits Syst Signal Process
DOI 10.1007/s00034-015-0057-x

A Sub-100 ppm/°C Temperature-Compensated High-Frequency CMOS Relaxation Oscillator

Siraporn Sakphrom[1] · **Pantelis Georgiou**[2] · **Apinunt Thanachayanont**[1]

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Abstract A temperature-compensated high-frequency CMOS integrated relaxation oscillator with low frequency variations is presented. A current-controlled oscillator topology is employed with a resistive source-degenerated transconductor and a current comparator to achieve high oscillation frequency and low power dissipation. The proposed oscillator was designed with process parameters from a standard 0.35-μm CMOS technology and a 2.5-V single power supply voltage. At a nominal oscillation frequency of 21 MHz, the total power dissipation of the circuit was 201 μW. Post-layout simulation results showed that the frequency variations were less than 34.16 ppm/°C over a temperature range of −40 to +120 °C.

Keywords Relaxation oscillators · Frequency stability · Temperature compensation · MOSFET

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1 Introduction

Emerging short-range, low-cost, and low-power wireless communication systems, such as wireless sensor and body area networks [1,10,11], have relaxed performance requirements for radio transceivers. These systems have recently prompted research and development of highly stable and accurate integrated oscillators as a replacement of the reliable quartz crystal oscillators. For a reference frequency of less than 100 MHz, relaxation oscillators [3], ring oscillators [12], and the Wien bridge oscillators [4] can be employed to achieve high frequency stability and low power dissipation.

Recently, there is a growing interest to develop low power CMOS relaxation oscillators with high frequency stability [2,3,5–8,13,14,17]. The oscillation frequency (f_{osc}) practically varies with process parameters, power supply voltage, and temperature. The frequency variations due to power supply voltage can be minimized by using a voltage regulator [12], while the variations due to process parameters can be compensated by trimming of resistors and capacitors. Thus, the temperature stability of f_{osc} is very critical during operation in order to minimize timing uncertainty. The temperature stability of f_{osc} of the relaxation oscillator is typically due to the temperature dependence of RC time constant and the delay times of comparator and flip-flops.

Temperature compensation of f_{osc} can be achieved by employing either temperature-stable biasing [3,5], offset cancelation structure [8], voltage-averaging or error feedback loop [2,14], or feedforward period control scheme [13]. The offset cancelation structure, described in [8], can achieve $\pm 0.25\,\%$ frequency variations at 18.5 kHz over temperature range of -40 to $+90\,^{\circ}\text{C}$; however, it requires two clock phases for operation, and thus, another timing circuit is needed. In [3], a 1.1-MHz relaxation oscillator with $\pm 0.5\,\%$ variation over temperature range of -20 to $+80\,^{\circ}\text{C}$ is obtained by using temperature-compensated biasing. The relaxation oscillator in [2] employs switched capacitor error feedback loop, and it achieves 12.6 MHz with $\pm 0.82\,\%$ variation over temperature range of 0 to $+80\,^{\circ}\text{C}$. In [14], the voltage-averaging feedback is employed to realize a 14-MHz relaxation oscillator with $\pm 0.19\,\%$ variation over temperature range of -40 to $+125\,^{\circ}\text{C}$.

In this work, we attempt to design a relaxation oscillator with oscillation frequency above 20 MHz and low power dissipation. A method of temperature-compensated biasing is adopted to achieve very low frequency variation over a wide range of temperature. This paper is organized as follows. Section 2 describes the circuit topology, temperature compensation method, and the transistor implementation of the proposed oscillator. Sections 3 and 4 describe the simulation results and conclusion, respectively.

2 Proposed Relaxation Oscillator

2.1 Circuit Topology

Figure 1a shows the simplified circuit diagram of the proposed current-controlled relaxation oscillator. The proposed circuits consist of an integrating capacitor (C), a charging current source (I_C), a reference current (I_R), a resistive source-degenerated

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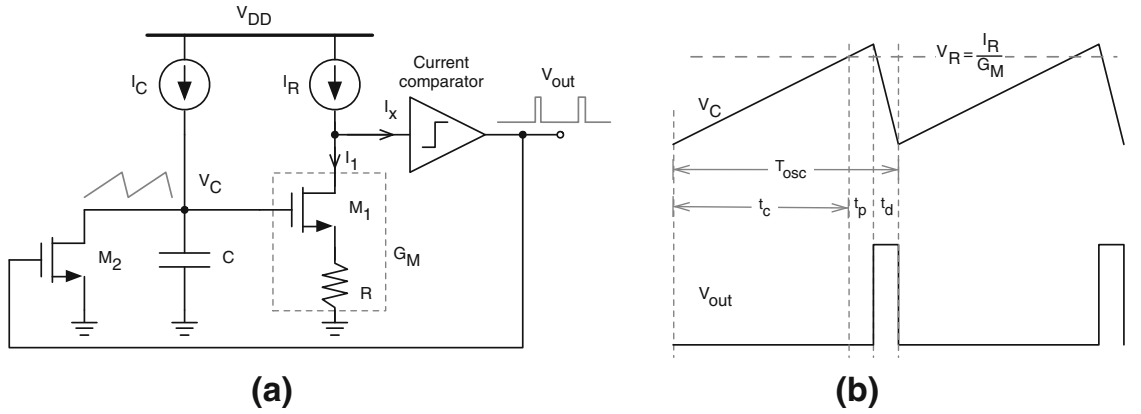

Fig. 1 **a** Simplified circuit diagram of the proposed relaxation oscillator and **b** its voltage waveforms

transconductor (formed by M_1 and R), a discharging MOSFET switch (M_2), and a current-mode comparator. The transconductor is used to convert the capacitor voltage (V_C) to a current (I_1), which is compared with the constant reference current I_R. The resultant current ($I_x = I_R - I_1$) is applied to the current-mode comparator. The simple source-degenerated transconductor, instead of a more complex circuit, is employed in order to achieve high oscillation frequency and low power consumption. The operation of the proposed oscillator can be explained as follows.

Assuming that the voltage across the capacitor (V_C) is initially zero and M_2 is OFF, the constant current I_C will charge the integrating capacitor and then V_C and I_1 increase. When $I_1 < I_R$ (i.e., $I_x > 0$), the comparator output voltage (V_{out}) will be LOW or 0 V, then M_2 is turned off, and V_C and I_1 continue to rise. When I_1 exceeds I_R or $I_1 > I_R$ (i.e., $I_x < 0$), V_{out} is HIGH or V_{DD} and M_2 is turned on to discharge V_C to ground, and I_1 is reset to 0. Next, V_C is charged again and the above process is repeated. Thus, the capacitor is charged and discharged periodically by I_C and M_2, respectively. The voltage waveforms of V_C and V_{out} are depicted in Fig. 1b with the equivalent reference voltage $V_R = {}^{I_R}/_{G_M}$, where $G_M = \left(R + g_{m1}^{-1}\right)^{-1}$ is the transconductance of the transconductor. The period of oscillation (T_{osc}) is given by (2), where t_c is the charging time of I_C, t_p is the propagation delay time of the comparator, and t_d is the discharging time of M_2. Typically, a current comparator can easily achieve the delay time (t_p) in the order of a few nanoseconds [9,15]; thus, t_p can be neglected for T_{osc} larger than tens of nanoseconds. The discharging time (t_d) is proportional to $\left(C + C_p\right) R_{\text{on}}$, where R_{on} is the average on-resistance of M_2 and C_p is the drain parasitic capacitance of M_2. Since R_{on} is inversely proportional to $({}^{W}/_{L})_2$ and C_p is proportional to $(WL)_2$; thus, increasing $({}^{W}/_{L})_2$ reduces R_{on} but increasing C_p. Therefore, increasing $({}^{W}/_{L})_2$ to reduce t_d will have a diminishing influence beyond certain values and t_d will asymptotically reach a minimum value. In this work, the integrating capacitor C is chosen to be much larger than C_p, and an optimal value of $({}^{W}/_{L})_2$ is selected to achieve $t_d \ll t_c$.

Therefore, for oscillation frequencies in the range of tens of MHz, it can be assumed that t_p and t_d are much less than t_c and $T_{\text{osc}} \approx t_c$. Assuming that $V_R = {}^{I_R}/_{G_M}$ and $I_R = mI_C$, T_{osc} can be easily derived as given by (3).

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$$G_M = \frac{1}{R + \frac{1}{g_{m1}}} \tag{1}$$

$$T_{\text{osc}} = t_c + t_p + t_d \approx t_c \tag{2}$$

$$T_{\text{osc}} \approx t_c = \frac{C}{G_M} \cdot \frac{I_R}{I_C} = \frac{C}{G_M} \cdot m \tag{3}$$

2.2 Temperature Compensation Approach

The temperature dependence of a parameter can be characterized by the fractional temperature coefficient (TC). The TC of T_{osc} ($TC\,(T_{\text{osc}})$) can be calculated by (4) and the result is given by (6), where $\alpha_c = {}^{t_c}/_{T_{\text{osc}}}$, $\alpha_p = {}^{t_p}/_{T_{\text{osc}}}$, $\alpha_d = {}^{t_d}/_{T_{\text{osc}}}$, and $TC\,(t_c)$, $TC\left(t_p\right)$, and $TC\,(t_d)$ are the fractional temperature coefficients of t_c, t_p, and t_d, respectively. Assume that $\alpha_c \approx 1, \alpha_p \ll 1$, and $\alpha_d \ll 1$, thus $TC\,(T_{osc}) \approx TC\,(t_c)$.

$$TC\,(T_{\text{osc}}) = \frac{1}{T_{\text{osc}}} \frac{\partial T_{\text{osc}}}{\partial T} \tag{4}$$

$$= \left(\frac{t_c}{T_{\text{osc}}}\right) \cdot \frac{1}{t_c} \frac{\partial t_c}{\partial T} + \left(\frac{t_p}{T_{\text{osc}}}\right) \cdot \frac{1}{t_p} \frac{\partial t_p}{\partial T} + \left(\frac{t_c}{T_{\text{osc}}}\right) \cdot \frac{1}{t_d} \frac{\partial t_d}{\partial T} \tag{5}$$

$$= \alpha_c TC\,(t_c) + \alpha_p TC\left(t_p\right) + \alpha_d TC\,(t_d) \tag{6}$$

For the proposed circuit in Fig. 1a, the $TC\,(f_{\text{osc}})$ can be derived from (3) as given by (7). Typically, on-chip capacitors (e.g., metal–insulator–metal or polysilicon–polysilicon capacitors) have very small TCs, compared with those of on-chip resistors (e.g., see Table 1 $TC\left(C_{poly1}\right) = +0.03 \times 10^{-3}/^{\circ}\text{C}$). Assume that $TC\,(C)$ is negligible, thus $TC\,(f_{\text{osc}}) \approx TC\,(G_M)$. Since G_M is described by (1), the $TC\,(G_M)$, and thus $TC\,(f_{\text{osc}})$, can be derived as given by (10). Therefore, $TC\,(f_{\text{osc}})$ can be minimized by canceling the two terms of $TC\,(R)$ and $TC\,(g_{m1})$ in (10).

$$TC\,(f_{\text{osc}}) = \frac{1}{f_{\text{osc}}} \frac{\partial f_{\text{osc}}}{\partial T} = \frac{1}{G_M} \frac{\partial G_M}{\partial T} - \frac{1}{C} \frac{\partial C}{\partial T} \tag{7}$$

$$= TC\,(G_M) - TC\,(C) \tag{8}$$

$$TC\,(f_{\text{osc}}) \approx TC\,(G_M) = \frac{1}{G_M} \frac{\partial G_M}{\partial T} \tag{9}$$

Table 1 Fractional temperature coefficients of on-chip resistors and capacitor

Component	Sheet resistance (Ω/□)	First-order TC ($10^{-3}/^{\circ}\text{C}$)
R-poly1	8	0.9
R-poly2	50	0.59
R-nwell	1000	6.2
R-diffn	75	1.5
R-diffp	140	1.5
C-poly	n/a	0.03

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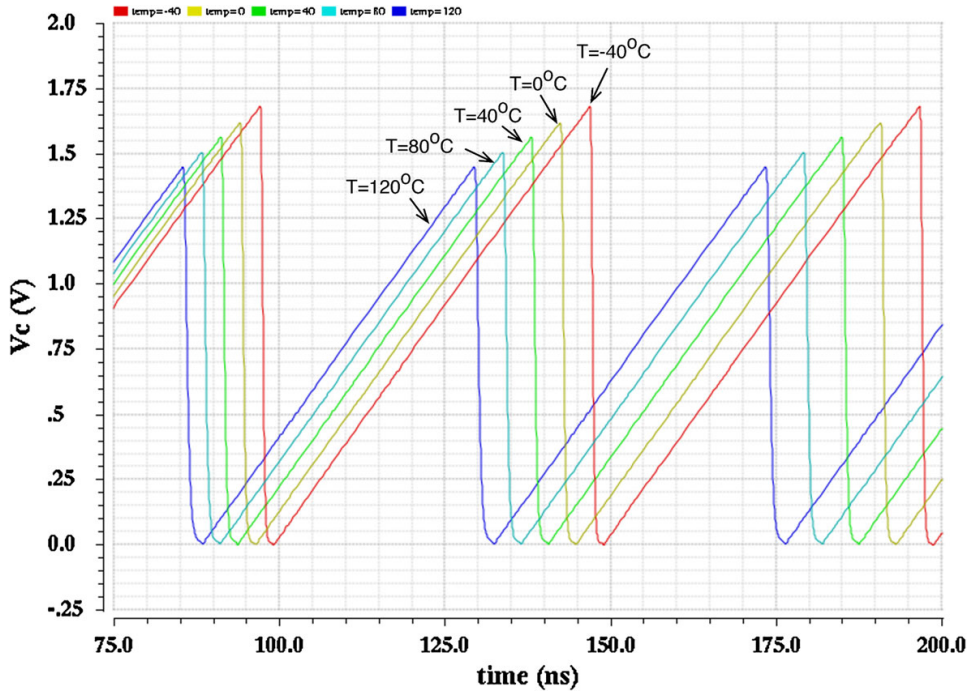

Fig. 2 Effect of temperature variation on V_C and f_{osc} with $TC\,(I_C) = TC\,(I_R) = TC\,(R) = 0$

$$= -\left(\frac{g_{m1}R}{1+g_{m1}R}\right) TC\,(R) + \left(\frac{1}{1+g_{m1}R}\right) TC\,(g_{m1}) \tag{10}$$

In Fig. 1a, M_1 will operate mostly in the saturation region as V_C increases. Thus, assuming the MOSFET's square-law relationship, $TC\,(g_{m1})$ can be derived as given by (12). Since both $TC\,(\mu_n)$ and $TC\,(V_{\text{TH}})$ are negative [16], $TC\,(g_{m1})$ can be either positive or negative depending on the value of V_{GS}. Note that there is a specific value of V_{GS} which can give $TC\,(g_{m1}) = 0$, and this is usually known as the zero temperature coefficient (ZTC) point of MOSFET [16]. In this work, M_1 is biased in the region below the ZTC point, thus second term in (12) dominates, and g_{m1} increases with temperature or $TC\,(g_{m1}) > 0$. Therefore, from (10), a positive-TC resistor should be used to compensate with $TC\,(g_{m1})$ in order to achieve low $TC\,(f_{\text{osc}})$.

$$TC\,(g_{m1}) = \frac{1}{g_{m1}}\frac{\partial g_{m1}}{\partial T} = \frac{1}{\mu_n}\frac{\partial \mu_n}{\partial T} - \left(\frac{V_{\text{TH}}}{V_{\text{GS}}-V_{\text{TH}}}\right)\frac{1}{V_{\text{TH}}}\frac{\partial V_{\text{TH}}}{\partial T} \tag{11}$$

$$= TC\,(\mu_n) - \left(\frac{V_{\text{TH}}}{V_{\text{GS}}-V_{\text{TH}}}\right) TC\,(V_{\text{TH}}) \tag{12}$$

Figure 2 shows the effect of temperature variations on V_C, which were obtained by using ideal I_C and I_R with zero TCs and ideal resistor R with $TC\,(R) = 0$. According to (10) and (12), g_{m1} and G_M increase with temperature, thus the effective V_R is reduced (i.e., the peak voltage of the sawtooth waveform in Fig. 2 decreases as temperature increases), and thus f_{osc} is increased as temperature increases. Temperature compensation of f_{osc} can be achieved by either reducing I_C (and I_R) or increasing R as temperature increases. The two approaches are demonstrated in Fig. 3.

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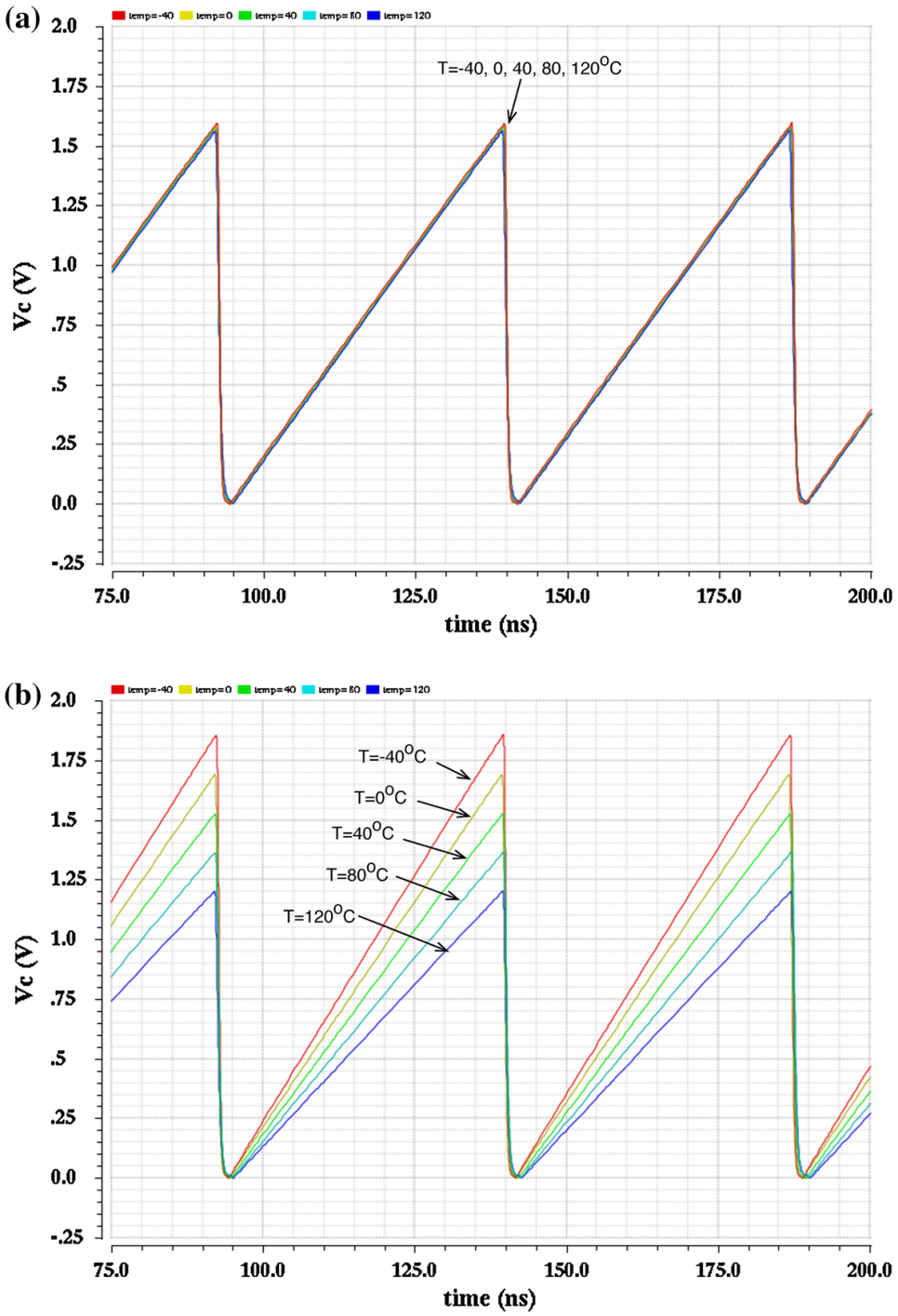

Fig. 3 Effect of temperature variations on V_C and f_{osc} with **a** $TC\,(I_C) = TC\,(I_R) = 0$ & $TC\,(R) = +1.4 \times 10^{-3}/°\text{C}$ and **b** $TC\,(I_C) = TC\,(I_R) = -2.5 \times 10^{-3}/°\text{C}$ & $TC\,(R) = 0$

In Fig. 3a, $TC\,(I_C) = 0$ and $TC\,(R) = +1.4 \times 10^{-3}/°\text{C}$, the charging rate of V_C $(\partial V_C/\partial T)$ is unaffected by temperature variations and R is increased with temperature to compensate for the increase of g_{m1}. This keeps G_M and the effective V_R relatively constant with temperature, and thus, f_{osc} can be insensitive with temperature. In Fig. 3b, $TC\,(I_C) = TC\,(I_R) = -2.5 \times 10^{-3}/°\text{C}$ and $TC\,(R) = 0$, the charging rate $\partial V_C/\partial T$ (due to reduced I_C) and V_R (due to reduced I_R) are decreased proportionally as temperature increases, and thus, f_{osc} is insensitive with temperature. Figure 4

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shows the simulated frequency variations of f_{osc}, over a temperature range of -40 to $+120\,^{\circ}\text{C}$, without compensation (in gray with $TC\,(I_C) = TC\,(R) = 0$) and with ideal compensation (in green with $TC\,(I_C) = 0 \& TC\,(R) = +1.4 \times 10^{-3}/^{\circ}\text{C}$). The average $TC\,(f_{\text{osc}})$ can be reduced from 783.33 ppm/°C (without compensation) to about 10.05 ppm/°C (with optimum compensation). Therefore, the optimum compensation can be achieved with either $TC\,(I_C) = 0 \& TC\,(R) = +1.4 \times 10^{-3}/^{\circ}\text{C}$ or $TC\,(I_C) = -2.5 \times 10^{-3}/^{\circ}\text{C}$ and $TC\,(R) = 0$. However, in practice, either $TC\,(I_C) = 0$ or $TC\,(R) = 0$ cannot be obtained, and thus, a more practical design approach is to choose a value of $TC\,(R)$ and find the optimum value of $TC\,(I_C)$ to achieve the best temperature compensation.

Table 1 shows the fractional temperature coefficients of the on-chip resistors and capacitors available in our 0.35-μm CMOS technology. Note that the TC of polysilicon capacitor (C-poly) is very small ($+0.03 \times 10^{-3}/^{\circ}\text{C}$) and thus it is neglected. It can be seen that the TCs of the diffusion resistors (Rdiffn or Rdiffp) are quite close to the required TC; however, the resistance of diffusion resistors, especially at large resistance, are practically voltage dependent and nonlinear. The TC of the diffusion resistors varies substantially with its resistance and voltage; thus, they are not suitable for our design. The polysilicon resistors (R-poly1 or R-poly2) are preferred because of their excellent linearity, which make their TCs virtually independent with resistance and voltage. However, the drawback of polysilicon resistors is small sheet resistance; thus, relatively large silicon area is required. It may be argued that a composite resistor, realized by combining polysilicon and n-well resistors (R-nwell) in series or parallel, can be used to obtain the required TC and save the chip area. However, the required TC is much closer to the TC of polysilicon resistor; thus, the suitable composite resistance needs to use polysilicon resistance much larger than the n-well resistance. For example, a 150-kΩ series composite resistance requires about 140-kΩ of R-poly1 and 10-$k\Omega$ of R-nwell to obtain the desired $TC\,(R) = +1.4 \times 10^{-3}/^{\circ}\text{C}$. In this case, the area saving of a composite resistor is insignificant, and thus, R is implemented with R-poly1. Since the TC of R-poly1 is $+0.9 \times 10^{-3}/^{\circ}\text{C}$, the temperature compensation is not optimum, and the achievable $TC\,(f_{\text{osc}})$ with $TC\,(I_C) = 0$ is about 282.05 ppm/°C over a temperature range of -40 to $+120\,^{\circ}\text{C}$, as depicted in Fig. 4 (in red). The optimum temperature compensation of f_{osc} can be achieved by using I_C and I_R with an optimum negative TC, as demonstrated in Fig. 4 (in blue). In this design with R realized by 150-kΩ R-poly1, the optimum temperature compensation was obtained with $TC\,(I_C) = -0.9 \times 10^{-3}/^{\circ}\text{C}$ and the minimum achievable $TC\,(f_{\text{osc}})$ was about 23.19 ppm/°C. Thus, the next design task is to design a bias current generator circuit that can provide the optimum $TC\,(I_C) = -0.9 \times 10^{-3}/^{\circ}\text{C}$.

2.3 Complete Circuit Implementation

Figure 5 shows the complete schematic diagram of the proposed oscillator. The conventional constant-g_m bias current generator, realized by $M_{10} - M_{15}$, R_{B1} and R_{B2}, is used to provide the currents I_C and I_R via M_3 and M_4, respectively. A high-speed capacitive-input current comparator [9,15], realized by $M_{6-}M_9$, is adopted. Rail-to-rail output voltage swing and short transition time are achieved by using an output

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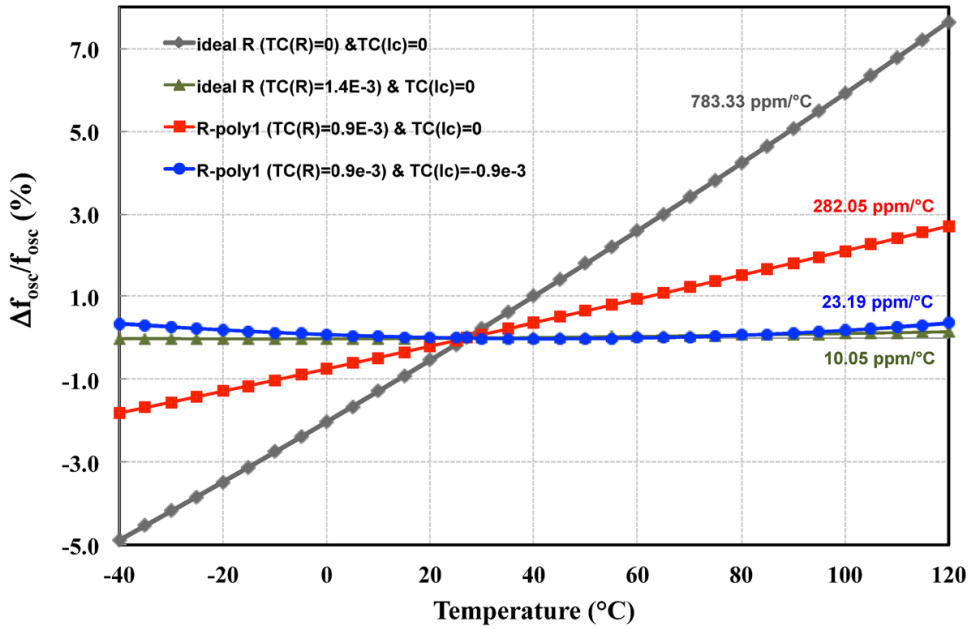

Fig. 4 Simulated temperature variations of f_{osc}

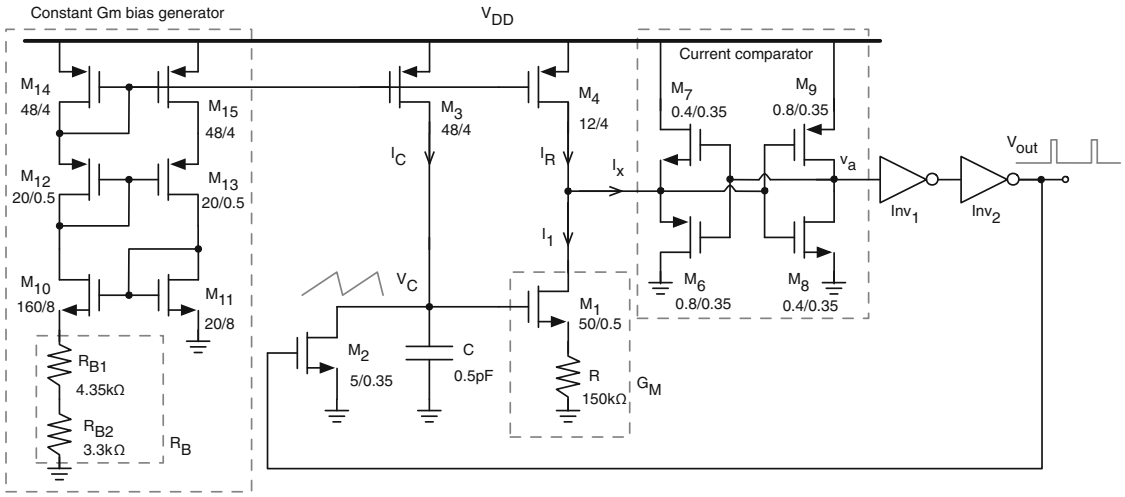

Fig. 5 Complete schematic diagram of the proposed relaxation oscillator

CMOS inverters, Inv_1 and Inv_2. For ease of compensation design, the time delay (t_p) of the comparator is required to be small compared with the period of oscillation. Figure 6 shows the simulated t_p as a function of power supply voltage (V_{DD}), over a temperature range of -40 to $+120$ °C. In our CMOS technology, the simulated t_p is less than 2 nS and is almost insensitive to temperature variations when V_{DD} is greater than 2 V. For accurate temperature compensation, the period of oscillation (T_{osc}) should be greater than $10t_p$ (i.e., 20 nS) and thus f_{osc} should be limited to below 50 MHz. Simulation results with $V_{\text{DD}} = 2.5$ V showed that the fractional temperature coefficient of t_p was about $-0.69 \times 10^{-3}/°\text{C}$.

To achieve the required $TC\,(I_C) = -0.9 \times 10^{-3}/°\text{C}$ for the optimum compensation, the bias resistor R_B with $TC = +3 \times 10^{-3}/°\text{C}$ has to be employed. In this work, R_B is implemented by a series composite resistor, R_{B1} and R_{B2}, which are realized with R-poly1 and R-nwell, respectively. For a nominal I_C of 20 μA, $R_B = 7.65$ kΩ is

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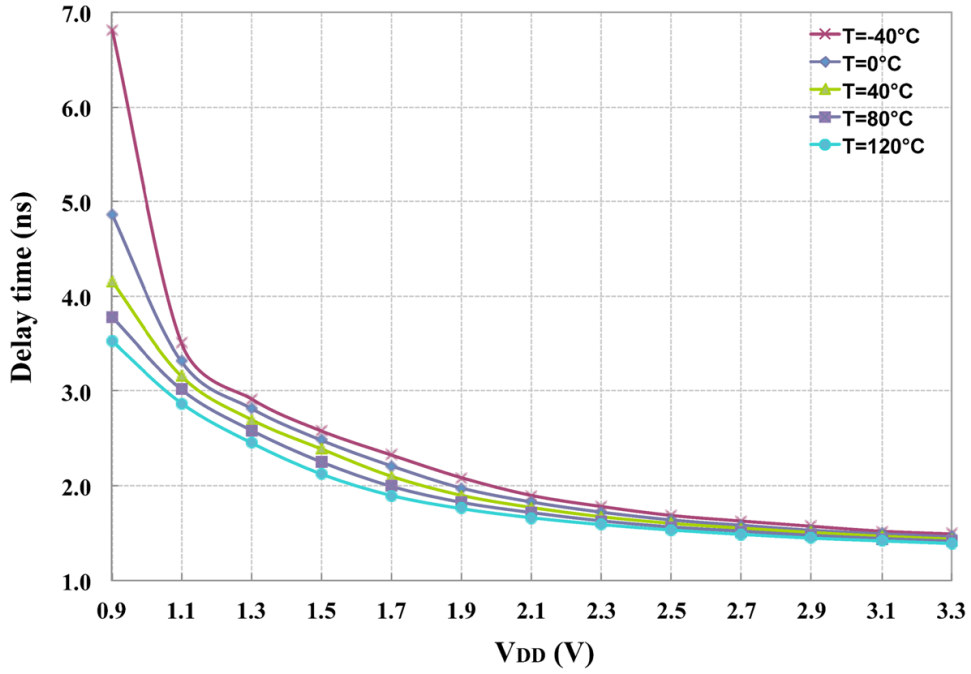

Fig. 6 Simulated delay time of the current comparator at different values of V_{DD} and temperature

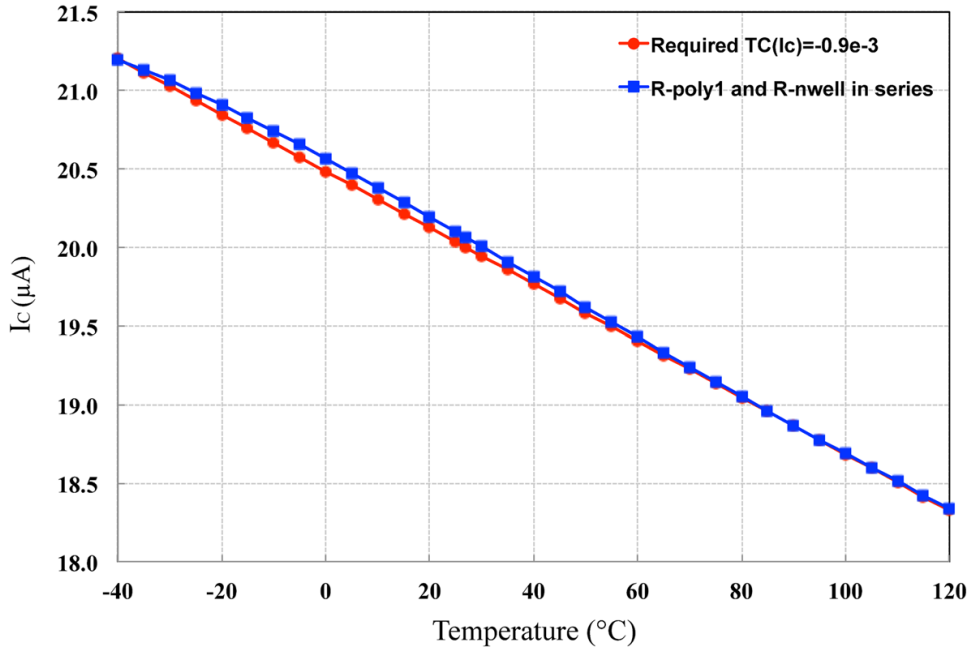

Fig. 7 Simulated temperature variations of I_C generated by the constant-g_m biasing circuit with R_{B1} and R_{B2} realized by R-poly1 and R-nwell, respectively

required and it is realized with $R_{B1} = 4.35\,\text{k}\Omega$ and $R_{B2} = 3.3\,\text{k}\Omega$ in order to achieve the required $TC\,(I_C)$. Figure 7 shows the simulated I_C, over a temperature range of -40 to $+120\,^{\circ}\text{C}$, obtained with the series composite resistor (in blue). It can be seen that the achievable TC is very close to the required value of $TC\,(I_C) = -0.9 \times 10^{-3}/^{\circ}\text{C}$ (in red).

One drawback of the oscillator in Fig. 5 is that the output voltage has a very small duty cycle; however, this can be overcome easily by replacing the discharging

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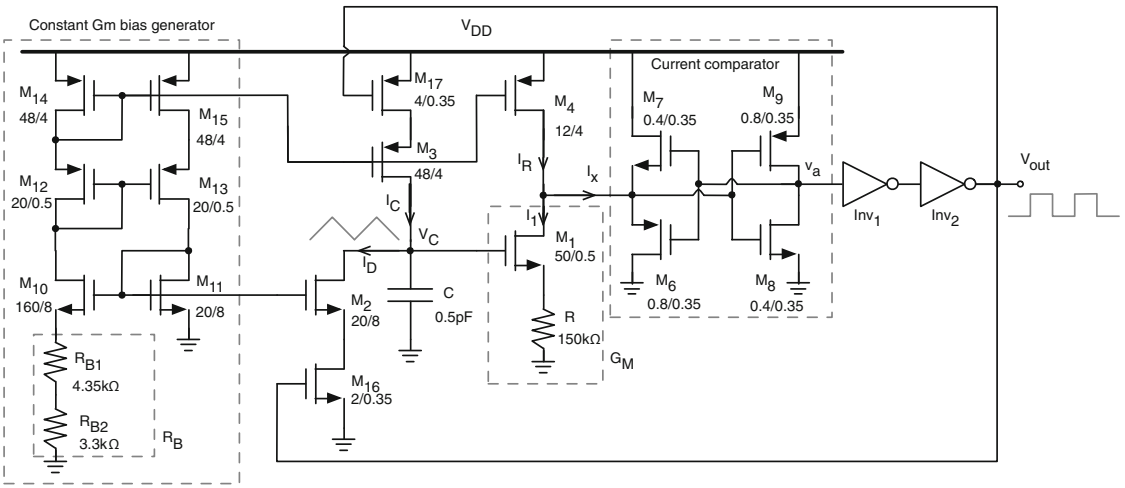

Fig. 8 Modification of the proposed relaxation oscillator for larger duty cycles

MOSFET switch with a constant discharging current source. The modified oscillator is depicted in Fig. 8, where M_2 now realizes a constant discharging current source (I_D) which is a replica of the reference current. The charging (I_C) and discharging currents are turned on and off alternately by MOSFET switches, M_{16} and M_{17}. The duty cycle is simply determined by the ratio of $I_C/(I_C+I_D)$. Since both I_C and I_D are replicas of the reference current, their temperature variations will be closely matched and their effects to the oscillation time period and duty cycle will be canceled out.

3 Simulation Results

The proposed relaxation oscillator was designed and simulated by using Cadence Spectre with process parameters from a standard 0.35 -μm CMOS technology. The circuit was designed to operate with a 2.5-V power supply voltage and a nominal oscillation frequency of about 20 MHz at room temperature of 27 °C. The nominal values of C, I_C, and m were chosen to be 0.5 pF, 20 μA, and 4, respectively. The resistors R, R_{B1}, and R_{B2} were realized with 150-kΩ R-poly1, 4.35-kΩ R-poly1, and 3.3-kΩ R-nwell. Using the above parameters and biasing conditions, the oscillation frequency of 21.14 MHz was obtained with an average $TC\,(f_{\text{osc}})$ of 20.59 ppm/°C over a temperature range of −40 to +120 °C, as depicted in Fig. 9 (in blue). The frequency variations of the proposed oscillator were also examined at other oscillation frequencies by changing only the values of C to 0.25, 0.75, and 1.0 pF, and thus, the oscillation frequency was changed to 34.26, 15.43, and 12.19 MHz, respectively. Simulations were performed without re-optimization, and the resultant frequency variations are plotted in Fig. 9. The average $TC\,(f_{\text{osc}})$ of the three cases is less than 65 ppm°C over the temperature range of −40 to +120 °C.

Figure 10 shows the physical layout of the proposed oscillator with $C = 0.5$ pF, and it occupies an active area of 0.016 mm^2. Post-layout simulation showed that the average $TC\,(f_{\text{osc}})$ increased to 34.16 ppm/°C, as shown in Fig. 9. The effects of mismatch and process variations on the variations of f_{osc} were evaluated by performing Monte Carlo simulations. Figure 11a, b plots the simulated 100-sample histograms of

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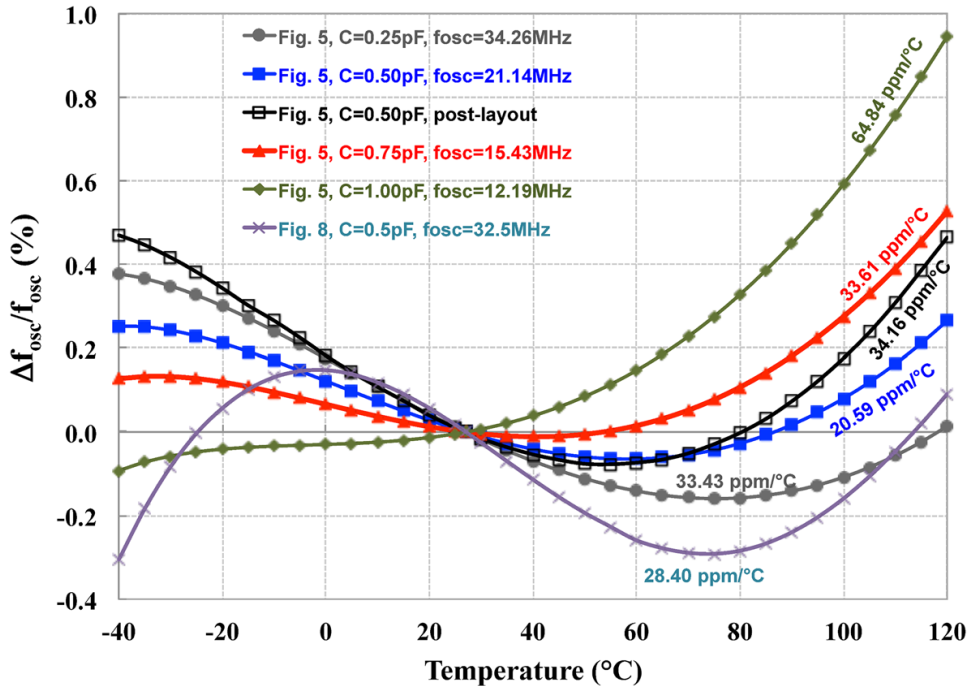

Fig. 9 Simulated temperature variations of the oscillation frequencies

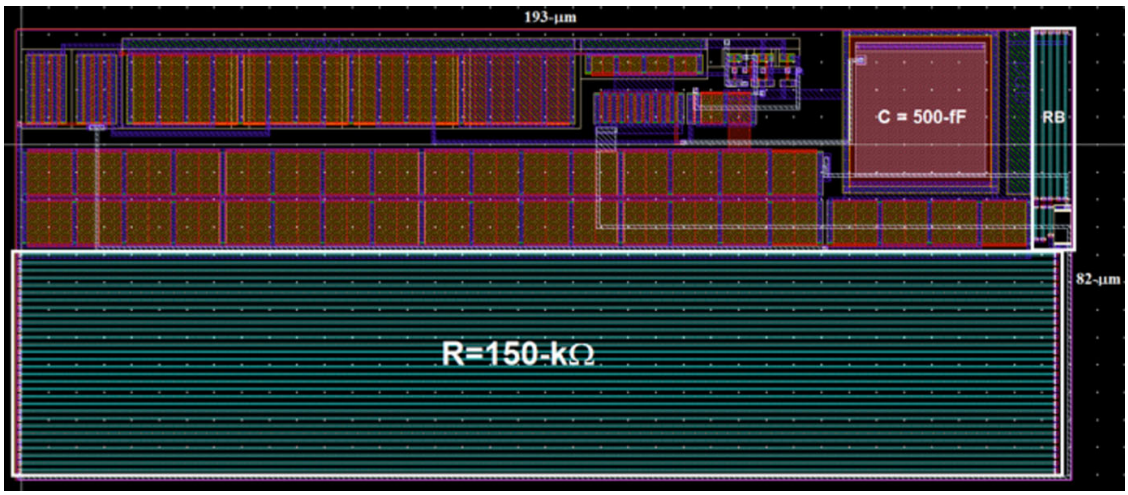

Fig. 10 Layout of the proposed oscillator

f_{osc} at 21.14 MHz under mismatch and process variations, respectively. The resultant frequency deviations are 1.17 % (0.247 MHz) and 21.4 % (3.947 MHz) under mismatch and process variations, respectively. Thus, the oscillation frequency is very robust under parameter mismatches.

The duty cycle of the output voltage of the circuit in Fig. 5 is about 5 %. The modified oscillator in Fig. 8 was designed and simulated with $I_C = I_D = 20\,\mu$ A to achieve a duty cycle of 50 %. The circuit oscillates at 32.5 MHz with an average TC (f_{osc}) of 28.4 ppm/°C over a temperature range of −40 to +120 °C, as also depicted in Fig. 9.

Table 2 shows the performance summary and comparison with other high-frequency relaxation oscillators. The figure of merit (FOM), defined by (13) [7], is used for a fair comparison. The FOM takes into account of the oscillation frequency (f_{osc}),

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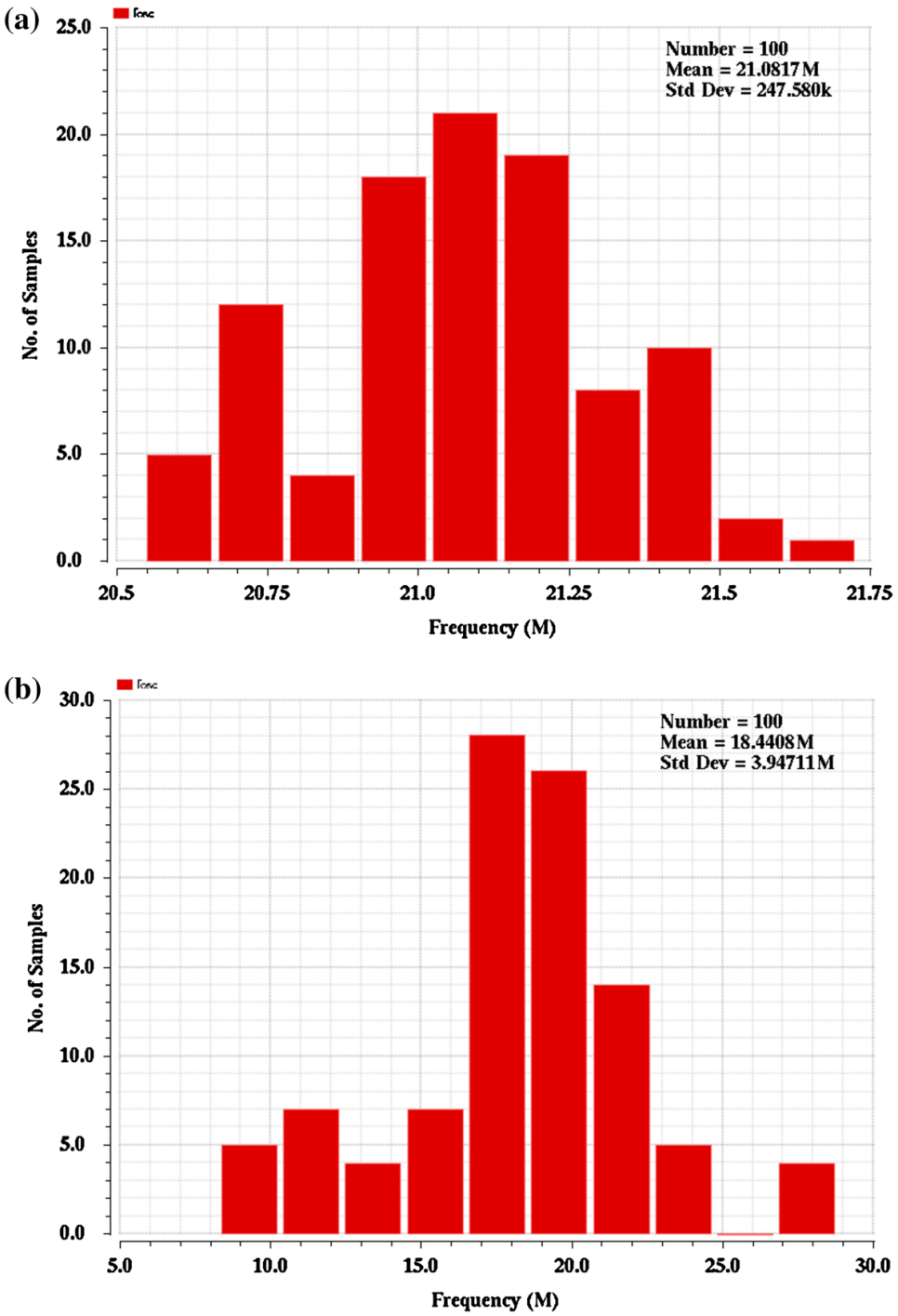

Fig. 11 Monte Carlo simulation results of f_{osc} with **a** mismatch and **b** process variations

power dissipation (P_{diss}), $TC\,(f_{\text{osc}})$, and active area. Using the $TC\,(f_{\text{osc}})$ obtained from post-layout simulation, the calculated *FOM* of the proposed oscillator is 186.

$$\text{FOM} = 10\log\left(\frac{f_{\text{osc}}^2}{P_{\text{diss}} \cdot \text{Area} \cdot TC\,(f_{\text{osc}})}\right) \tag{13}$$

In principle, the proposed temperature-compensated oscillator can be realized using a state-of-the-art ultra deep submicron CMOS process because temperature coeffi-

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Table 2 Performance summary and comparison

Parameters	This work^s	[7]^m	[3]^m	[2]^m	[14]^m
Process (nm)	350	130	180	65	180
Supply (V)	2.5	1.0	1.8	1.2	1.8
Frequency (MHz)	21	1.24	1.1	12.6	14
Power (μW)	201	5.8	0.859	98.4	45
Temperature (°C)	−40 to 120	−40 to 80	−20 to 80	0–80	−40 to 125
TC (ppm/°C)	34.16	−296	64.3	205	23.03
Area (mm^2)	0.016	0.016	0.075	0.01	0.04
FOM (dB)	186	167.5	174.7	178.9	186.7

s = post-layout simulation, m = measurement

cients of resistors and capacitors are not drastically different over process nodes. In practice, the circuit will generally face two main design issues including smaller power supply voltage and larger transistor mismatch. Smaller power supply voltages will increase the propagation delay time of the current-mode comparator and its contribution to the oscillation time period; however, this effect can be counterbalanced by using minimum-length transistors. More importantly, the current generator circuit will suffer from reduced headroom voltage under small supply voltages. Transistors employed for the current generator and current mirrors should have large channel width and length to reduce mismatch and variation.

4 Conclusion

A temperature-compensated high-frequency current-controlled relaxation oscillator has been described. Source-degenerated transconductor and current-mode comparator are used to achieve high speed and low power dissipation. Temperature compensation is achieved by using suitable composite resistors and temperature-compensated current sources. Post-layout simulation results showed that the proposed circuit could operate at 21-MHz oscillation frequency with an average *TC* of 34.16 ppm/°C over a temperature range of −40 to +120 °C, while dissipating 201 μW from a single 2.5-V power supply voltage. Therefore, the proposed oscillator exhibits good frequency stability over a wide temperature range, which renders it viable as a frequency reference for short-range low-cost wireless communication systems.

References

1. J. Bae, K. Song, H. Lee, H. Cho, H.-J. Yoo, A low-energy crystal-less double-FSK sensor node transceiver for wireless body-area network. IEEE J. Solid State Circuits **47**(11), 2678–2692 (2012)
2. Y. Cao, P. Leroux, W. De Cock, M. Steyaert, A 63,000 Q-factor relaxation oscillator with switched-capacitor integrated error feedback. In *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)* (2013), pp. 186–187
3. Y.-H. Chiang, S.-I. Liu, A submicrowatt 1.1-MHz CMOS relaxation oscillator with temperature compensation. IEEE Trans. Circuits Syst. II Express Briefs **60**(12), 837–841 (2013)

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4. V. De Smedt, P. De Wit, W. Vereecken, M.S.J. Steyaert, A 66 μw 86 ppm/°c fully-integrated 6 MHz Wienbridge oscillator with a 172 dB phase noise FOM. IEEE J. Solid State Circuits **44**(7), 1990–2001 (2009)
5. U. Denier, Analysis and design of an ultralow-power CMOS relaxation oscillator. IEEE Trans. Circuits Syst. I Reg. Pap. **57**(8), 1973–1982 (2010)
6. P.F.J. Geraedts, E.A.J.M. van Tuijl, E.A.M. Klumperink, G.J.M. Wienk, B. Nauta, Towards minimum achievable phase noise of relaxation oscillators. Int. J. Circuit Theory Appl. **42**, 238–257 (2012)
7. K.-K. Huang, D.D. Wentzloff, A 1.2-MHz 5.8-μW temperature-compensated relaxation oscillator in 130-nm CMOS. IEEE Trans. Circuits Syst. II Express Briefs **61**(5), 334–338 (2014)
8. A. Paidimarri, D. Griffith, A. Wang, A.P. Chandrakasan, G. Burra, A 120 nW 18.5 kHz RC oscillator with comparator offset cancellation for ±0.25 % temperature stability. In *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)* (2013), pp. 184–185
9. A. Rodriguez-Vazquez, R. Dominguez-Castro, F. Medeiro, M. Delgado-Restituto, High resolution CMOS current comparators: design and applications to current-mode function generation. Analog Integr. Circuits Signal Process. **7**(2), 149–165 (1995)
10. F. Sebastiano, L.J. Breems, K.A.A. Makinwa, S. Drago, D.M.W. Leenaerts, B. Nauta, A 65-nm CMOS temperature-compensated mobility-based frequency reference for wireless sensor networks. IEEE J. Solid State Circuits **46**(7), 1544–1552 (2011)
11. Y.-C. Shih, B. Otis, An on-chip tunable frequency generator for crystal-less low-power WBAN radio. IEEE Trans. Circuits Syst. II Express Briefs **60**(4), 187–191 (2013)
12. K. Sundaresan, P.E. Allen, F. Ayazi, Process and temperature compensation in a 7-MHz CMOS clock oscillator. IEEE J. Solid State Circuits **41**(2), 433–442 (2006)
13. T. Tokairin, K. Nose, K. Takeda, K. Noguchi, T. Maeda, K. Kawai, M. Mizuno, A 280 nW, 100 kHz, 1-cycle start-up time, on-chip CMOS relaxation oscillator employing a feedforward period control scheme. In *2012 Symposium on VLSI Circuits (VLSIC)* (2012), pp. 16–17
14. Y. Tokunaga, S. Sakiyama, A. Matsumoto, S. Dosho, An on-chip CMOS relaxation oscillator with voltage averaging feedback. IEEE J. Solid State Circuits **45**(6), 1150–1158 (2010)
15. H. Traff, Novel approach to high speed CMOS current comparators. Electron. Lett. **28**(3), 310–312 (1992)
16. Y. Tsividis, C. McAndrew, *Operation and Modeling of the MOS Transistor* (Oxford University Press, New York, 2011)
17. L. Yan, G. Yuan, L. Der, W.-H. Ki, C.P. Yue, A 0.5 % precision on-chip frequency reference with programmable switch array for crystal-less applications. IEEE Trans. Circuits Syst. II Express Briefs **60**(10), 642–646 (2013)

II. Low Phase Noise CMOS Ring Oscillator Using Self-Biased Inverter Delay Cell : APCAP 2013

Low Phase Noise CMOS Ring Oscillator Using Self-Biased Inverter Delay Cell.

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***Abstract*—This paper describes the design of a low phase noise CMOS ring oscillator using a new self-biased inverter delay cell. The proposed differential ring oscillator was designed for the Medical Implant Communications Service (MICS) frequency band. Using 0.35-µm CMOS process parameters and a 3.3-V power supply voltage, the simulation results showed that the proposed ring oscillator achieved a phase noise of -113.62 dBc/Hz at 1-MHz offset frequency while dissipating 4.4 mW.**

I. Introduction

Low phase noise oscillator is an important circuit for wireless communication system. For stringent phase noise requirement, the LC oscillator is usually the preferred choice over the ring oscillator. However, in several applications including the Medical Implant Communications Service (MICS) system, the phase noise requirement is much relaxed and therefore it is practically possible to use a ring oscillator [1]. This paper describes the design and simulation of a low phase noise CMOS differential ring oscillator for a MICS wireless transceiver. A new self-biased inverter delay cell is proposed to reduce the phase noise of the oscillator. Section II describes the circuit design and realization of the proposed oscillator. Sections III and IV describe the simulation results and conclusion, respectively.

II. Circuit Design and Implementation

Fig.1 shows the schematic circuit diagram of the proposed differential ring oscillator. It consists of three identical differential inverter delay stages. Each stage is implemented with two CMOS inverters, inv1 and inv2. A pair of cross-coupled inverters, inv3 and inv4, is used to achieve fast and full output voltage switching of the delay cell, which reduces the phase noise of the oscillator [2]. The CMOS inverters, inv1 and inv2, are realized by using the current-starved topology. Nodes Sp and Sn, which are the source terminals of PMOS and NMOS of the inverters, respectively, are connected to the biasing MOSFETs (M1-M6). The gates of the biasing MOSFETs are connected to the output nodes of the inverters rather than a DC bias voltage as in the case of normal current-starved delay cell. Therefore the delay cell is self-biased. Since the gates of M1-M6 are connected to the output nodes of the inverters, they are turned ON and OFF alternately and provide switching bias current to the inverters. Switching of biasing current can reduce the phase noise due to up-converted 1/f noise [3].

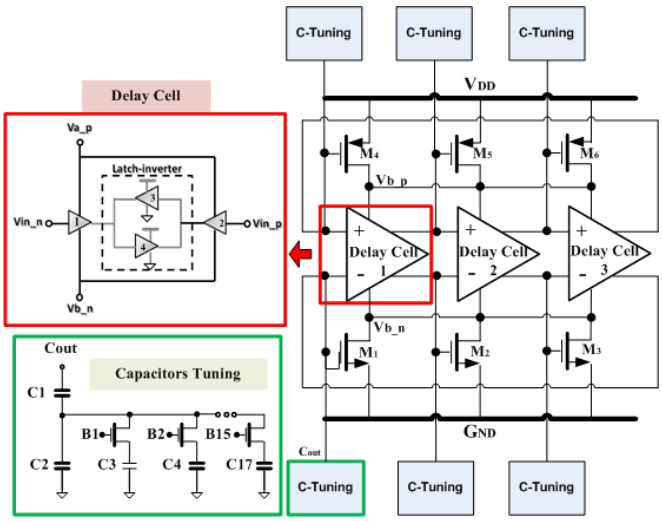

Fig. 1 The proposed self-biased differential ring oscillator.

Since the delay cell is self-biased, the frequency of oscillation can be tuned and controlled by changing the inverters' load capacitance. This is achieved by using a switched capacitor array. The oscillation frequency of a ring oscillator is inversely proportional to the load capacitance. Increasing the capacitance reduces the oscillation frequency. In this work, the digitally-controlled switched capacitor tuning array in Fig. 1 is used to achieve fine frequency tuning. A 4-bit digital control word is used to switch the capacitor array, thus there are 15 MOSFET switches. The capacitors C1 and C2 are 10 fF and 200 fF, respectively. The capacitors C3-C17 are equal to 30 fF. The change in capacitance when the nth MOSFET switch is turned ON is given by (1).

$$\Delta C = \frac{C_1 C_2 C_3 (C_1 + C_2)}{(C_1 + C_2 + kC_3)^2 - C_3(C_1 - kC_3 + 1)} \quad (1)$$

III. Simulation Results

The proposed ring oscillator was designed and simulated by using Spectre with process parameters from a 0.35-µm CMOS technology. The circuit was designed to operate with a 3.3-V power supply voltage. The nominal oscillator frequency was designed to be about 408 MHz. To validate the phase noise reduction of the proposed self-biased ring oscillator (SBRO), a conventional fixed bias current-starved 3-stage ring oscillator (CBRO) was also designed and simulated to achieve a comparison. Both oscillators were designed with similar oscillation frequency and current consumption.

Fig. 2 plots the simulated phase noise of both ring oscillators. It can be seen that the phase noise of the proposed ring oscillator is about 20 dB lower than the conventional fixed bias current-starved ring oscillator. This validates the advantage of using the proposed self-biased inverter delay cell. Fig. 3 plots the fine frequency tuning characteristic of the proposed ring oscillator.

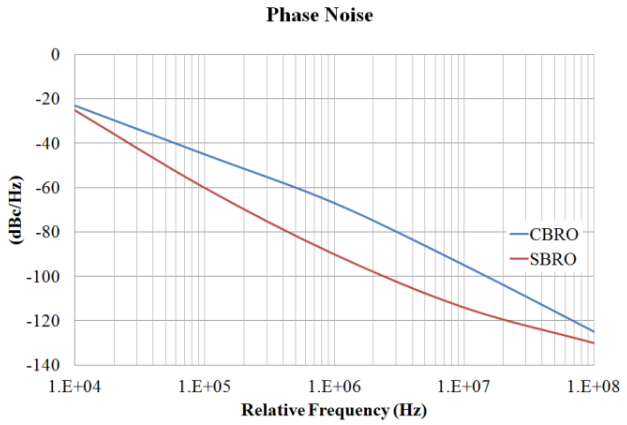

Fig. 2 Simulated phase noise of the proposed ring oscillator vs. the conventional current-starved ring oscillator.

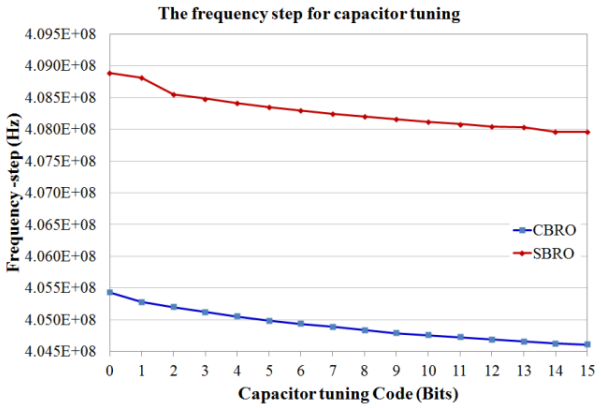

Fig. 3 Fine frequency tuning characteristic of the proposed ring oscillator.

Table I summarizes and compares the simulated performance of the proposed oscillator. The conventional figure-of-merit (FOM) in (2) is used for comparison, where L is the phase noise (dBc/Hz), Δf is the offset frequency, f is the oscillation frequency, and P_{DC} is the power dissipation. The proposed ring oscillator can achieve a FOM of -160.7.

$$FOM = L + 10\log\left(\left(\frac{\Delta f}{f}\right)^2 \frac{P_{DC}}{P_{REF}}\right) \quad (2)$$

IV. Conclusion

This paper describes the design of a low phase noise CMOS differential ring oscillator in a 0.35-µm CMOS technology. A new self-biased inverter delay cell is proposed to realize the ring oscillator. The self-biased inverter achieves switched current biasing which reduces the phase noise of the oscillator. Simulation results showed a 20-dB phase noise reduction when compared with the fixed biased oscillator.

TABLE I. Performance Summary.

Metrics	Proposed	CBRO	[4]
Technology (µm)	0.35	0.35	0.28
Vdd (V)	3.3	3.3	2.5
PN@1MHz (dBc/Hz)	-113.62	-96.48	-96
fosc (MHz)	409	405.5	2450
Pdiss (mW)	4.44	3.11	19.2
FOM	-159.3	-143.7	-150.95

Acknowledgement

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References

[1] W.-H. Chen, W.-F. Loke, and B. Jung, "A 0.5-V, 440- #x00B5;W Frequency Synthesizer for Implantable Medical Devices," *Ieee J. Solid-State Circuits*, vol. 47, no. 8, pp. 1896–1907, 2012.

[2] L. Dai and R. Harjani, "Design of low-phase-noise CMOS ring oscillators," *Ieee Trans. Circuits Syst. Ii Analog Digit. Signal Process.*, vol. 49, no. 5, pp. 328–338, 2002.

[3] E. A. M. Klumperink, S. L. J. Gierkink, A. P. Van Der Wel, and B. Nauta, "Reducing MOSFET 1/f noise and power consumption by switched biasing," *Ieee J. Solid-State Circuits*, vol. 35, no. 7, pp. 994–1001, 2000.

[4] W. Rahajandraibe, L. Zaïd, V. C. de Beaupre, and G. Bas, "Temperature Compensated 2.45 GHz Ring Oscillator with Double Frequency Control," in *2007 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2007, pp. 409–412.

III. A Low-Power CMOS RF Power Detector : ICICE 2012

A Low-Power CMOS RF Power Detector

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Abstract— **This paper describes the design and implementation of a low-power wide dynamic range radio-frequency (RF) power detector in a standard 0.18-μm CMOS process. The proposed circuit includes a root-mean-square (RMS) power detector and a logarithmic amplifier. The RMS power detector exploits the non-linear characteristic of MOSFET to realize the RMS conversion. A current-mirror active load is used in the RMS power detector to increase the RMS conversion gain. Since the output of the RMS power detector is a DC voltage, the following logarithmic amplifier does not require wide operating bandwidth, thus allowing simple circuit realization with minimum power dissipation. Simple differential amplifier is used to realize the limiting gain stage. Post-layout simulation results showed that the proposed circuit was able to detect input power from -70 dBm to -20 dBm with signal frequencies ranging from 0.5 GHz to 5 GHz, while dissipating only 0.9 mW under a 1.8-V power supply voltage.**

Keywords- Low-power, RF power detector, Limiting amplifier, Logarithmic amplifier, RMS power detector

I. INTRODUCTION

Power detection of radio frequency (RF) signals is required in many applications, ranging from wireless communication systems [1], [2] to integrated circuits test and measurement [3], [4]. In wireless communication systems, RF power detector is usually employed in a control loop in order to optimize power consumption, improve linearity of the power amplifier, or the control the gain of the transmitting and receiving chain.

The power level of a RF signal can be computed by using either the peak or root-mean-square (RMS) values. Peak detection is suitable for constant-envelope or low peak-to-average ratio modulated signals, however RMS detection is preferred for high peak-to-average ratio modulated signals due to better accuracy. Detection of the RMS value of a signal can be obtained by employing one of the following approaches: thermoelectric devices [5], the non-linear characteristics of diode [6] or bipolar junction transistor (BJT) [7] or metal-oxide-semiconductor field-effect transistor (MOSFET) [1], [8], [9], or current-mode computational circuits [3], [10], [11].

Current-mode computational circuits, including squarer, divider and filter, can be used to realize a RMS detector. These current-mode circuits can be realized by using transconductors [3], [10] or translinear circuits [11]. Power detectors based on the translinear principle exploit the exponential characteristic of BJT or subthreshold MOSFET to realize the mathematical functions required for RMS conversion [11]. Translinear-based power detector for RF signals has been demonstrated in [11], however the achievable bandwidth is relatively limited with respect to the other approaches.

In this paper, the RMS power detector in [1] is modified and improved further to increase the conversion gain and dynamic range. The conversion gain is enlarged by increasing the output resistance of the RMS power detector. The dynamic range is increased by using a successive-approximation logarithmic amplifier. The RF power detector is targeted to be employed in a microwave-based fruit maturity detection system [13], which exploits the reflection of microwave signal to determine the permittivity of the fruit-under-test and relates it to the maturity of the fruit. The system is intended to be deployed a wireless sensor network for fruit farming and the device must be able to operate for months without battery replacement, therefore requiring low power consumption. The RF signal power reflected from the fruit is usually small and in the order of the -50 dBm to -60 dBm, therefore requiring high sensitivity and wide dynamic range of the power detector. The proposed RF power detector is designed and simulated by using process parameters from a standard 0.18-□m CMOS technology. The paper is organized as follows. Section II describes the architecture of the proposed RF power detector. Detailed circuit designs are described in Section III. Simulation results and conclusion are given in Sections IV and V, respectively.

II. ARCHITECTURE OF THE PROPOSED RF POWER DETECTOR

Fig. 1 shows the architecture of the proposed RF power detector. It consists of a RMS power detector and a logarithmic amplifier. The input RF voltage signal is converted to a DC output voltage, which represents the RMS value of the input

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signal power, by exploiting the non- linearity of MOSFETs [1]. To achieve a linear-in-dB input-output characteristic, the DC output voltage is further amplified by a successive-approximation logarithmic amplifier, which is realized by cascading seven current limiting amplifiers. The cascaded limiting amplifiers produce a linear-in-dB output characteristic by using a piecewise linear approximation. All limiting amplifier stages are identical except for the first stage, which includes an extra input pair for DC offset cancellation. Each limiting amplifier produces both differential output voltage and current. The output voltage is passed to the following amplifying stage. The output currents of all limiting stages are summed and applied to a load resistor to produce the output voltage of the power detector. Since the input signal of the logarithmic amplifier is a DC voltage, the envelope detector or rectifier is not needed. This saves chip area and power dissipation. The resistor R_F and capacitor C_F realize a lowpass filter to perform DC offset cancellation feedback. The resistor R_F is realized by using a subthreshold MOSFET in order to obtain large resistance with minimum die area. The dynamic range and linearity error of the RF power detector are determined by the number of cascading limiting amplifier stages. Increasing the number of amplifying stages will improve the sensitivity and dynamic range of the detector, at the expense of increased power dissipation. In this paper, using seven stages of amplifiers was found to be an optimum solution, in terms of power dissipation, dynamic range and sensitivity of the power detector.

III. Circuit Description and Analysis

A. *RMS Power Detector*

Fig. 2 shows the RMS power detector realized by exploiting the square-law characteristic of MOSFET operating in the saturation region. The circuit is a modified version of the recently proposed RF power detector [1], in order to achieve higher conversion gain and sensitivity. The input RF signal is applied to transistor M_1, via an AC-coupling capacitor C_C. The transistors M_1 and M_2 are identical and operate in the saturation region with identical gate bias voltages. Transistor M_2 is used to reduce offset errors due to process, temperature and supply voltage variations. Thus the drain currents of M_1 and M_2 can be expressed as in (1) and (2), where $\beta_i = \mu_n C_{ox}(W/L)_i$ is the MOSFET transconductance parameter, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, V_T is the threshold voltage, W and L are the channel width and length of transistors, respectively.

$$I_{DS1} = \frac{\beta_1}{2}\left(V_{BIAS} + V_{RF} - V_{TN}\right)^2 \quad (1)$$

$$I_{DS2} = \frac{\beta_2}{2}\left(V_{BIAS} - V_{TN}\right)^2 \quad (2)$$

Assuming that $V_{RF} = V_i \cos(\omega t)$, the output voltages V_1 and V_2 are given by (3) and (4), respectively. The small-signal output resistance (r_{out}) of the circuit is equal to $r_{ds2}//r_{ds4}$, where r_{dsi} is the drain-source resistance of M_i.

$$V_1 = V_{DD} - V_{SG3} = V_{DD} - \sqrt{\beta_1/\beta_3}\left(V_i\cos(\omega t) + V_{BIAS} - V_{TN}\right) + V_{TP} \quad (3)$$

$$V_2 = V_{2,DC} + r_{out}\left(i_{DS1} - i_{DS2}\right) = V_{2,DC} + r_{out}\left\{\frac{\beta_1}{4}V_i^2 + \frac{\beta_1}{4}V_i^2\cos(2\omega t) + \frac{\beta_1}{4}\left(V_{BIAS} - V_{TN}\right)V_i\cos(\omega t)\right\} \quad (4)$$

The capacitors C_1 and C_2 form lowpass filters to filter out the RF signal and its harmonics. Since the circuit is fully-symmetrical, the DC voltage at V_2 ($V_{2,DC}$) is equal to the filtered voltage at V_1. Therefore the differential output voltage can be written as in (5), which is proportional to the square of the amplitude of the input RF signal.

$$V_2 - V_1 = r_{out}\frac{\beta_1}{4}V_i^2 \quad (5)$$

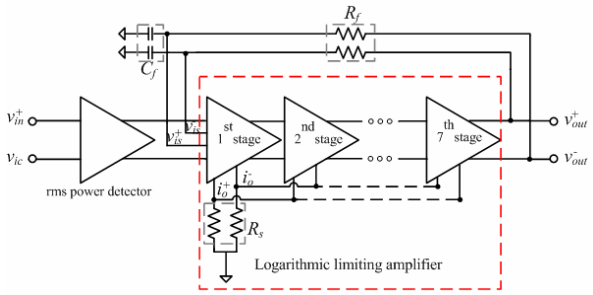


Figure 1. Architecture of the proposed RF power detector.

The simulated input-output characteristic of the proposed RMS power detector is demonstrated in Fig. 3, where the differential output voltage is plotted against the input signal power at 5 GHz. For comparison, the circuit in [1] was designed and simulated under the same circuit parameters and operating conditions and the results were plotted in Fig. 3. It can be seen that the proposed RMS power detector can achieve higher conversion gain due to larger output resistance. This improves the sensitivity of the power detector and eases the design of the following logarithmic amplifier. Furthermore, the proposed circuit has better linearity and wider input detectable range (i.e. -60 dBm to -10 dBm). Note that, the circuit can still detect the input signal power with the presence of offset errors and short-channel effects of MOSFETs, as explained in [1].

B. *Logarithmic Amplifier*

The output voltage of the RMS power detector is passed to the following 7-stage logarithmic amplifier as shown in Fig. 1. The logarithmic amplifier is realized with the limiting amplifier stage shown in Fig. 4. The limiting amplifier is realized by the simple source-coupled differential amplifier with current-mirror active loads (drawn in black). All amplifier stages are identical, except for the first stage which include an additional input source-coupled pair (drawn in grey) for DC offset cancellation feedback loop. Each amplifier provides both differential output voltage and current. The differential output voltage is passed to the input of the following amplifier stage. Since the input voltages of the limiting amplifiers are DC signals, the differential output currents of all amplifier stages, which exhibit the limiting current characteristic, can be summed at the output load resistors to produce the output voltage of the power detector. This saves the need for rectifiers and filters, which would normally be required in logarithmic amplifier. Furthermore, as the bandwidth of the amplifier can be very low, the amplifier can be optimized for the required input sensitivity and dynamic range with minimum power dissipation. The small-signal differential voltage gain of each amplifier stage is given by (6), where g_{mi} is

the small-signal transconductance of transistor M_i. Finally, the bias currents of the amplifiers are generated by a process, voltage and temperature insensitive current reference circuit [14], shown in Fig. 5.

$$A_v \approx -\frac{g_{m1}}{g_{m3}} = \sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_3}} \qquad (6)$$

IV. Simulation Results

The proposed RF power detector was designed and simulated by using Cadence Spectre with process parameters from a standard 0.18-µm CMOS technology. The circuit was designed to operate with a single 1.8-V power supply voltage and the total power dissipation is 0.9 mW. For the circuit in Fig. 2, the filtering capacitors (C_1 and C_2) are 100 fF, the AC-coupling capacitor (C_C) is 1 pF and the gate biasing resistor (R_G) is 1 kΩ.

Fig. 6 plots the differential output voltage (V_1-V_2) of the RF-to-DC converter in Fig. 2 against the input RF signal power at different input frequencies. The output voltage of 10 µV (-50 dBV) is generated with the input signal power of -65 dBm. The maximum output voltage of around 1 V (0 dBV) is generated when the input power is about -10 dBm. Therefore the input dynamic range is about -65 dBm to -10 dBm. Simulation results suggest that the circuit is able to detect the input power for frequencies up to 5 GHz. The authors are admittedly hesitant about the validity of the simulation results at very high input frequencies. However it is expected that the circuit should be able to operate at a few tens of GHz frequencies, as demonstrated in [1]. Fig. 7 shows the simulated transient output voltage of the power detector when applying different input powers of 2.5-GHz signal. The input signal power was swept from -80 to 0 dBm. The output voltage is plotted against the input signal power in Fig. 8. The output voltage range is roughly 0.4 V to 1.2 V and the input detectable range is approximately -70 dBm to -20 dBm. To verify the operation of the DC offset cancellation feedback, a DC input offset voltage source was added to the input of the first amplifier stage. A 2.5-GHz input RF voltage was applied to the power detector and the offset voltage was varied from 0 to 100 mV. The simulated transient output voltage were obtained and plotted in Figs. 9(a)-(b). It can be seen from Fig. 9(a) that the offset voltage only changes the output voltage level slightly and the circuit can still function correctly. Fig. 9(b) plots the output voltage variation as a function of the offset voltage when the input power is -50 dBm. The performance of the proposed RF power detector is summarized and compared with those of other reported detectors in Table II. It can be seen that the proposed circuit exhibits wide operating frequency, the largest input power detectable range and the best input sensitivity, with reasonably low power consumption. The proposed circuit has been sent for prototype chip fabrication.

V. Conclusion

A low-power wide dynamic range RF power detector has been described in this paper. The proposed circuit comprises a wideband RMS power detector and a successive logarithmic amplifier. The RMS power detector exploits the non-linear characteristic of MOSFET operating in the saturation region with an active load to achieve high RMS conversion gain with minimum power dissipation. The design of the logarithmic amplifier was simplified because wide operating bandwidth and the rectifier/filter circuit are not needed. Post-layout simulation results, in a 0.18-µm CMOS process, verified that the circuit was able to detect input power from -70 dBm to -20 dBm with signal frequencies ranging from 0.5 GHz to 5 GHz, while dissipating only 0.9 mW. Therefore the authors believe that the proposed RF power detector is suitable for wireless sensor network and telemetry applications.

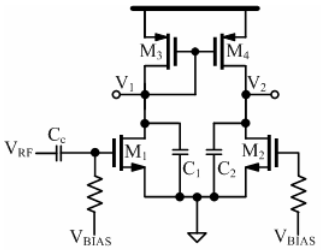


Figure 2. The proposed RMS power detector.

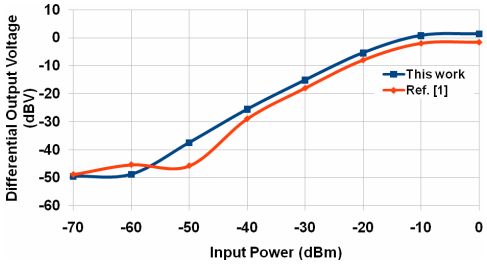


Figure 3. Output characteristic of the proposed RMS power detector with a 5-GHz input signal.

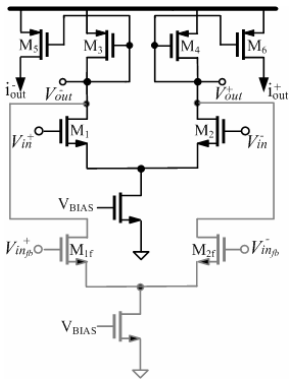


Figure 4. Limiting amplifier stage.

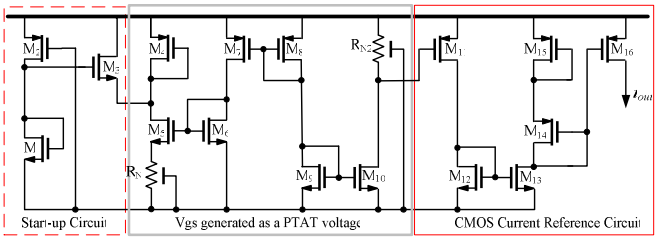


Figure 5. Process, voltage, temperature insensitive current reference.

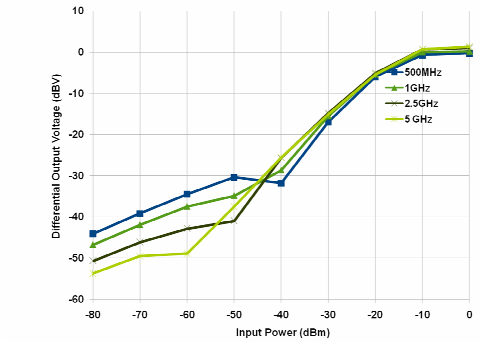


Figure 6. Output characteristic of the RF-to-DC converter at different input frequencies.

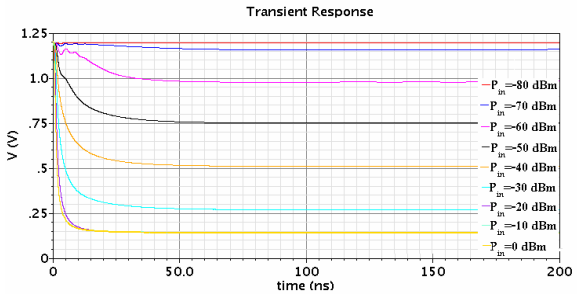


Figure 7. Transient output voltage of the power detector when applying different input signal power at 2.5 GHz.

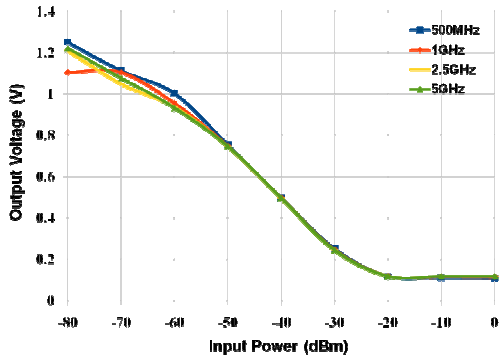
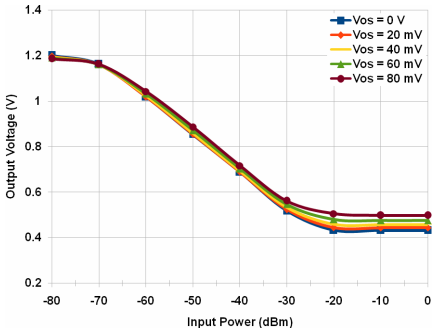


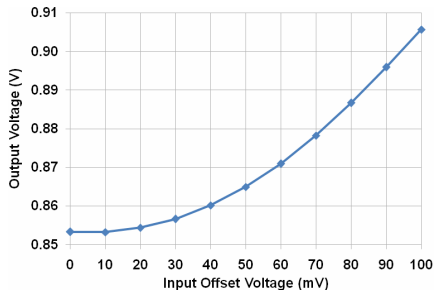
Figure 8. Input-output characteristic of the RF power detector.

Table I. Performance Summary and Comparison

Parameters	This work	[1]	[2]	[3]
CMOS Technology	0.18µm	0.13µm	0.18µm	0.35µm
Area (mm^2)	0.0078	0.0126	0.36	0.031
Conversion gain (mV/dB)	17	6	6	50
Dynamic range (dB)	50	20	20	30
Min. detectable signal (dBm)	-70	-35	-40	-25
Operating frequency range (GHz)	0.5 - 5	0.125-8.5	3.1-10.6	0.9-2.4
Supply voltage (V)	1.8	1.2	1.8	3.3
Power dissipation (mW)	0.9	0.18	10.8	8.6



(a)



(b)

Figure 9. Effect of the input offset voltage.

REFERENCES

[1] Y. Zhou and M. Y. Chia, "A Low-Power Ultra-Wideband CMOS True RMS Power Detector," IEEE Transactions on Microwave Theory and Techniques, vol. 56, 2008, pp. 1052-1058.

[2] K. A. Townsend and J. W. Haslett, "A Wideband Power Detection System Optimized for the UWB Spectrum," IEEE Journal of Solid-State Circuits, vol. 44, 2009, pp. 371-381.

[3] A. Valdes-garcia, R. Venkatasubramanian, J. Silva-martinez, and E. Sánchez-sinencio, "A Broadband CMOS Amplitude Detector for On-Chip RF Measurements," IEEE Trans. Instrumentation and Measurement, vol. 57, 2008, pp. 1470-1477.

[4] W. Eisenstadt and R. Fox, "A novel 5GHz RF power detector," 2004 IEEE International Symposium on Circuits and Systems, vol. I, 2004, pp. 897-900.

[5] V. Milanovic, M. Gaitan, E. Bowen, N. Tea, and M. Zaghloul, "Thermoelectric power sensor for microwave applications by commercial CMOS fabrication," IEEE Electron Device Letters, vol. 18, 1997, pp. 450-452.

[6] V. Milanovic, M. Gaitan, J. C. Marshall, and M. E. Zaghloul, "CMOS Foundry implementation of Schottky diodes for RF detection," IEEE Trans. Electron Devices, vol. 43, 1996, pp. 2210-2214.

[7] T. Zhang, W. Eisenstadt, R. Fox, and Q. Yin, "Bipolar Microwave RMS Power Detectors," IEEE Journal of Solid-State Circuits, vol. 41, 2006, pp. 2188-2192.

[8] R. A. Barrett, "Broadband RF power detector using FET," U.S. Patent 4647848, 1987.

[9] G. Ferrari, L. Fu, M.. Sampietro, E. Prati, and M. Fanciulli, "CMOS fully compatible microwave detector based on MOSFET operating in resistive regime," IEEE Microwave and Wireless Components Letters, vol. 15, 2005, pp. 445-447.

[10] J. Mulder, A. C. Woerd, W. A. Serdijn, and A. H. Roermund, "An RMS-DC Converter Based on the Dynamic Translinear Principle," IEEE J. Solid-State Circuits, vol. 32, 1997, pp. 1146-1150.

[11] Q. Yin, W. R. Eisenstadt, R. M. Fox, and T. Zhang, "A Translinear RMS Detector for Embedded Test Of RF ICs," IEEE Trans. Instrumentation and Measurement, vol. 54, 2005, pp. 1708-1714.

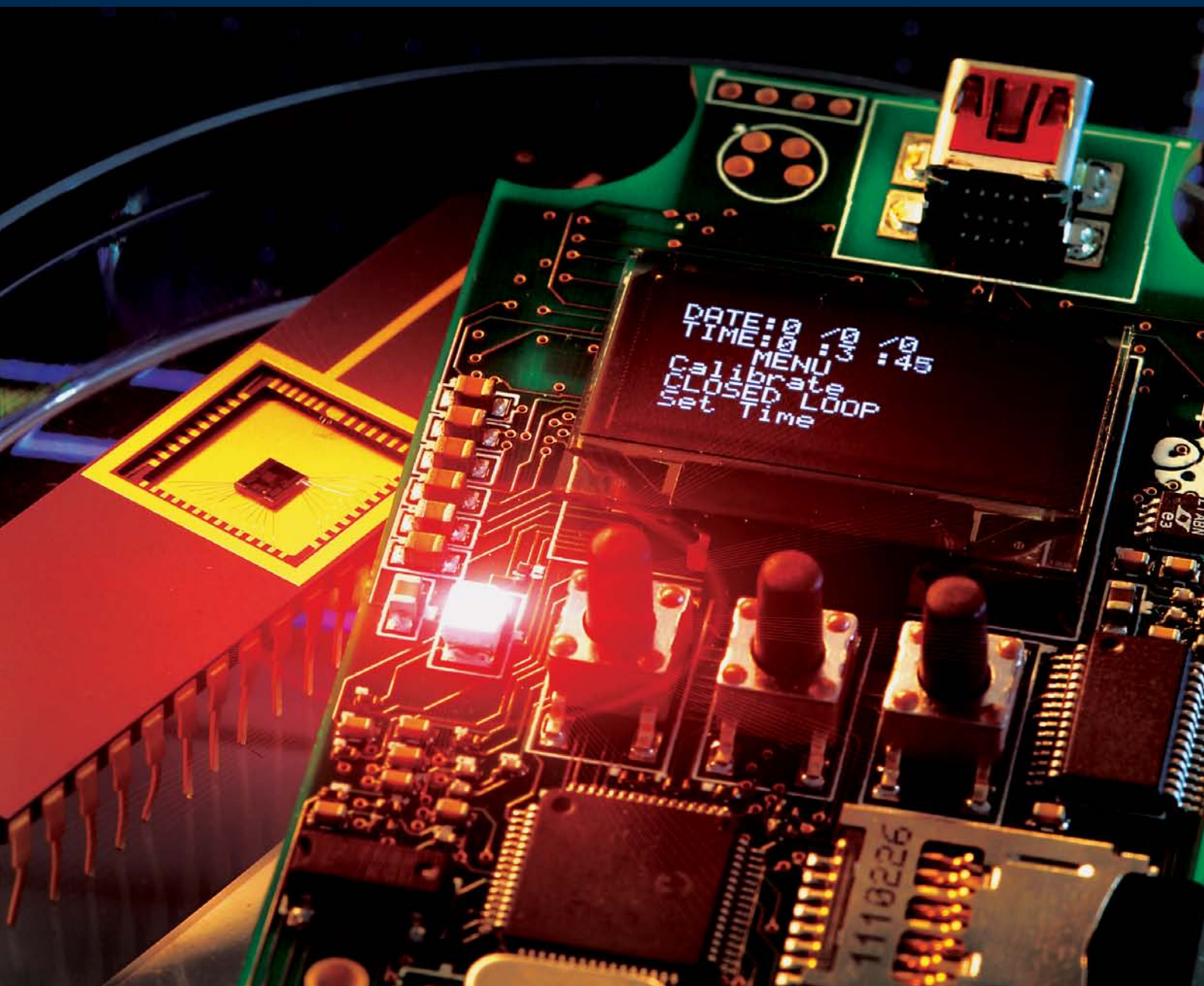
[12] S. Sengupta, K. Saurabh, and P. E. Allen, "Compensated CMOS constant current reference," 2004 IEEE International Symposium on Circuits and Systems, 2004, pp. 325-328.

Appendix B : Co-research with the Institute of Biomedical Engineering, Imperial College London

Imperial College
London

Centre for Bio-Inspired Technology

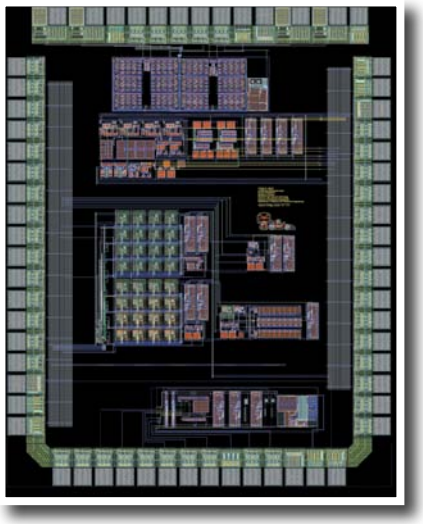
Annual Report 2012



Chip gallery

The Centre's focus is primarily the application of modern semiconductor technology to develop new bio-inspired systems and medical devices. This has in part been made possible through the EU-subsidised multi-project wafer (MPW) brokerage service provided by Europractice which provides our design tools via STFC (UK) and technology access via IMEC (Belgium) and Franhofer (Germany). Over the past seven years, we have fabricated a total of 26 integrated circuit designs in a variety of CMOS technologies.

The 'Chip Gallery' is also available online at: **www3.imperial.ac.uk/bioinspiredtechnology/research/chips**

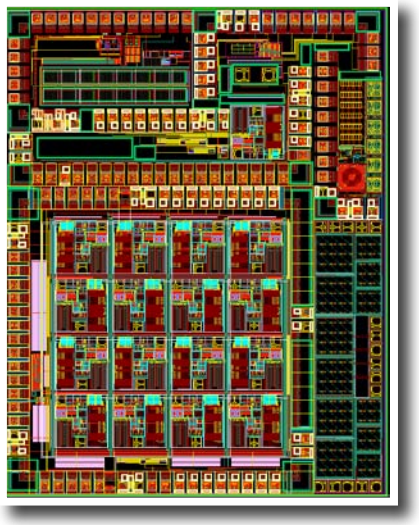


IBE12J01 (KIMI) – October 2012

Technology: Austriamicrosystems 0.35µm 2P4M CMOS

Purpose: ISFET sensing array, multi-channel glucose sensor instrumentation and oscillator

Designers: Yuanqi Hu, Siraporn Sakphrom, Mohamed El-Sharkawy, Yan Liu, Pantelis Georgiou

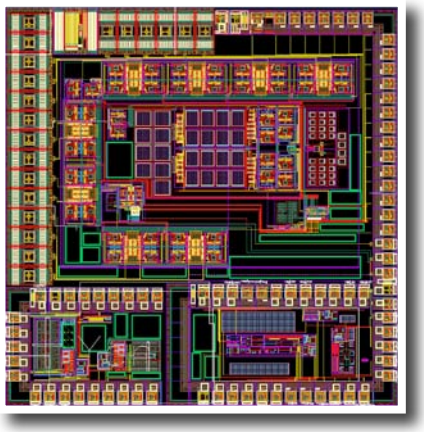


IBE12H01 (NGNI) – August 2012

Technology: Austriamicrosystems 0.18µm 1P4M HV CMOS

Purpose: Neural interface circuits and electro-optical modulator test structures

Designers: Yan Liu, Song Luan, Alexander Serb, Lieuwe Leene, Timothy Constandinou



IBE12D01 (Ian) – April 2012

Technology: Austriamicrosystems 0.18µm 1P4M HV CMOS

Purpose: Neural interface circuits

Designers: Ian Williams, Sivylla Paraskevopoulou, Yan Liu, Timothy Constandinou