DESIGN AND FABRICATION OF FIXED-PLATE STAIRCASE STRUCTURE USING OF THREE-DIMENSIONAL LITHOGRAPHY FOR CAPACITIVE SILICON MICROPHONE WITH MULTI-FILM THICKNESS MASK

JIRAWAT JANTAWONG

A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE RQUIREMENT FOR THE DEGREE OF
DOCTOR OF ENGINEERING IN ELECTRICAL ENGINEERING
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หัวข้อวิทยานิพนธ์	การออกแบบและสร้างโครงสร้างบันไดของแผ่นคงที่โดยใช้กระบวนการลิโธกราฟีสามมิติเพื่อไมโครโฟนซิลิกอนชนิดคาปาซิทีฟด้วยกระจกต้นแบบชนิดหลายความหนาชั้นฟิล์ม
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บทคัดย่อ

วิทยานิพนธ์ฉบับนี้ นำเสนอการออกแบบและสร้างโพรงอากาศที่มีลักษณะเฉพาะแบบขั้นบันไดสำหรับใช้เป็นเซ็นเซอร์ไฟฟ้าเครื่องกลจุลภาค (MEMS) สำหรับไมโครโฟนโดยใช้กระบวนการสร้างด้วยกระจกมาส์กต้นแบบชนิดพิเศษ (Multi-Film Thickness: MFT) ซึ่งโครงสร้างนี้โพรงอากาศแบบขั้นบันไดจะถูกสร้างให้มีการกัดหลายระดับบนแผ่นคงที่ (fixed plate) กระจกมาส์ก MFT ถูกพัฒนาขึ้นเพื่อลดขั้นตอนและจำนวนกระจกมาส์กของกระบวนการลิโธกราฟี โดยใช้เทคนิคการฉายแสงเพียงครั้งเดียวส่งผลให้ต้นทุนการผลิตลดลง

กระจกต้นแบบ MFT ชนิดใหม่นี้ ถูกสร้างขึ้นโดยการกำหนดค่าความหนาของชั้นฟิล์มโครเมียมที่แตกต่างกันเป็น 0, 4 , 14 และ 114 นาโนเมตรโดยที่ความหนาของชั้นฟิล์มบางเหล่านี้ส่งผลให้เกิดการจำกัดการส่องผ่านของพลังงานแสงผ่านกระจกมาส์กทำให้มีระดับความเข้มแสงที่แตกต่างกันทะลุผ่านไปยังฟิล์มน้ำยาไวแสง หลังจากการล้างน้ำยาไวแสงจะเกิดลวดลายที่มีความหนาแตกต่างกันเป็นรูปแบบโครงสร้างสามมิติ ซึ่งลวดลายเหล่านี้จะทำหน้าที่เป็นชั้นฟิล์มป้องกันการกัดโดยการหน่วงเวลาระหว่างการกัดบนพื้นผิวซิลิกอนแบบแห้งด้วยพลาสม่า (Reactive ion- etching) ดังนั้นกระบวนการนี้จึงส่งผลให้สามารถสร้างรูปแบบหลุมการกัดที่มีความลึกที่เหมาะสมบนแผ่นซิลิกอนที่ต้องการของเซ็นเซอร์คาปาซิทิฟทำให้ตรงบริเวณศูนย์กลางของโพรงนั้นถูกกัดลึกลงไป 1.5 ไมโครเมตรและส่วนที่เหลือนั้นถูกกำหนดได้ให้มีความลึก 1.0, และ 0.33 ไมโครเมตรตามลำดับ ทำให้ผลของคุณลักษณะทางไฟฟ้าของเซ็นเซอร์นี้มีค่าความจุไฟฟ้าสัมบูรณ์ตั้งต้น เท่ากับ 2.9 pF ขณะที่ โครงสร้างเซ็นเซอร์คาปาซิทิปแบบโครงสร้างทั่วไปมีค่า 2.2 pF มีค่าความจุไฟฟ้าเพิ่มขึ้น เท่ากับ 31.8 เปอร์เซ็นต์เมื่อเทียบขนาดของพื้นที่ของเมมเบรนที่เท่ากัน ดังนั้นเทคโนโลยีนี้ มีแนวโน้มส่งผลทำให้เกิดโอกาสในการปรับปรุงเซ็นเซอร์รุ่นใหม่ที่มีความดันต่ำพิเศษเพียงพอสำหรับการใช้งานไมโครโฟนที่มีขนาดเล็กจิ๋วต่อไป

Thesis	Design and Fabrication of Fixed-plate Staircase Structure Using of Three-dimensional Lithography for Capacitive Silicon Microphone with Multi-Film Thickness Mask
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Abstract

This thesis studied the design and fabrication of an air gap with staircase contour shaped (S-CTC) structure for capacitive MEMS microphone using a non-conventional multi-film thickness (MFT) masking process. This structure was formed with multi-level etching steps on the fixed plate. Three-dimensional (3D) lithography process was developed by using a single mask technique. This process not only eliminated the need for a conventional masking process, known as a binary intensity mask, but also reduced the number of masking steps and ultimately the cost of fabrication.

This new MFT mask was fabricated by varying the thickness of the chromium deposited film layer with 0, 4, 14, and 114 nanometers. These thicknesses limited the light transmission through the mask which could allow different levels of intensity to pass through it and expose to the photoresist film. After the photoresist was developed, the resulting patterns were formed with different thicknesses. These 3D photoresist patterns acted as a selective etching barrier during RIE (Reactive Ion Etching) silicon etching. Therefore, this process could form patterns with proper depths in the silicon as the desired three-dimensional staircase cavities in a single dry etching step. As per the design requirement, the center of the cavity was etched to the depth of 1.5 micrometers and the rest of the area was etched to depths of 1.0, 0.33 micrometer respectively. The electrical characteristic of the capacitive MEMS sensor showed that absolute capacitance of the S-CTC structure was 2.9 pF compared with a conventional structure value of 2.2 pF. This was 31.8 % higher while maintaining similar membrane active area. Therefore, this promising technology renders a unique opportunity to improve sufficiently the next generation of ultra-low-pressure sophisticated sensors for smallest microphone applications.

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Abbreviation

IC	Integrated circuit
MEMS	Micro electro mechanical system
SEM	Scanning electron microscope
CVD	Chemical vapor deposition
DRIE	Deep reactive ion etching
PEB	Post exposure bake
SB	Soft bake
DC	Direct current
PR	Photoresist
PMMA	Poly methyl methacrylate
TMAH	Tetramethyl ammonium
NMP	N-methylpyyrolidone
DQN	Diazoquinone – Novolak
DQ	Diazoquinone
PSRR	Power supply rejection ratio
SNR	Signal-to-noise ratio
ECM	Electret microphone
FET	Field-effect transistor
PCB	Printed circuit board
3-D	Three-dimensional
S-CTC	Staircase Contour to Cavity
MFT	Multiple film Thickness
TMEC	Thai microelectronics center
AOP	Acoustic over load point
dB-SPL	Decibels of sound pressure
Pa	Pascal
FEM	Finite element model
CDs	Critical dimensions
Cr	Chromium
Ni	Nickel
SCCM	Standard Cubic Centimeters per Minute
DWL	Direct laser
DIW	Deionized water
OM	Optical microscope
DSP	Double side polishing
LPCVD	Low-pressure Chemical Vapor Deposition
AFM	Atomic force microscope
UV	Ultraviolet light
RIE	Reactive Ion Etcher

List of symbols

a	Radius of circular membrane
h	Membrane thickness
$W_{(0)}$	Displacement of membrane
D	Flexural rigidity
r	Radial coordinate
x’	Plate moving distance
k	Relative permittivity
ε_0	Permittivity of space
A	Capacitance plate area
σ	Charge density
μm	Micrometer
I	Light intensity

Chapter 1
INTRODUCTION

Microelectromechanical system (MEMS), the silicon-based fabrication process of MEMS microphone, is one of the focal points in the semiconductor sensor industry. Due to its sheer volume in many successful applications of electronics devices and become ramp-up of economic demand for the leading supplier because the potential customer wanted regard to sharing on this market. Their MEMS products devices have been launched for the consumer for example such as pressure sensor, accelerometer, microphone, gyros.

In the mid-1960s has been the extraordinary discovery of piezo-resistivity in silicon-based pressure sensors, this continues widely traditionally with the commercial product about MEMS devices. Which there is derived from the history of micro-machined pressure sensors, and to examine recent developments in the field as well as additional considerations for capacitive and piezo-resistive devices. [1].

1.1 Background

Nowadays, MEMS Silicon (Si) typically based microphones business has gradually grown rapid developed to improve the Si-microphone. What the growth rate of MEMS product trend has will be replaced by the conventional electret microphone [2]. Simultaneously, the mobile communication industry has been growing in regard to modern smartphones. Therefore, the smartphone products were the complexity of featuring which offers special user interface function on that device and increases the number of the silicon microphone with its specific usage.

At present architecture of smartphone with new generation product models, there are embedded of many MEMS microphones dice per mobile device regard to performed properly with the complex audio operations required [3]. For example, some of the smartphone manufacturers such as iPhone-five product was assembled with three MEMS microphone chips to fabricated built-in for the phone's PCBA. There are three main purposes as which, first MEMS microphone is obtained to capturing main voice conversation, second is located on the back panel to ambient noise canceling for improves the sound quality, third is purposed to improve voice control performance for Siri’s software application. However, according to the MEMS silicon microphone sensor, there is a work functional based on the basic fundamental of physical property included of two main primarily functional backgrounds. There is an electrical functionality using for signal conditioning interface circuit and acoustic functionality uses as captures the sound pressure related to an acoustic signal.

In the sensor device system of Silicon MEMS microphone, the operating circuit diagram consists of two main elements such as the physical sensing element and Analog signal conditioner (ASIC) as shown in Fig. 1.1. These systems of MEMS element have to capture an incident of the sound pressure at the input state by MEMS sensing unit and then converses to an electrical for the sound signal at the output sensor state. The small signal level is prepared for higher sufficient condition for the pre-amplifier (PREAMP) unit. In addition, the amount of input sounds pressure is related to the changing of inside the mechanical part to deflected related to input of sensing elements as moving part as the diaphragm. Hence, the research topic in this thesis would be design considered, based on a sensing element for MEMS silicon microphone only with the capacitive sensing structure. Therefore, the output signal measuring of the changing in capacitance value.

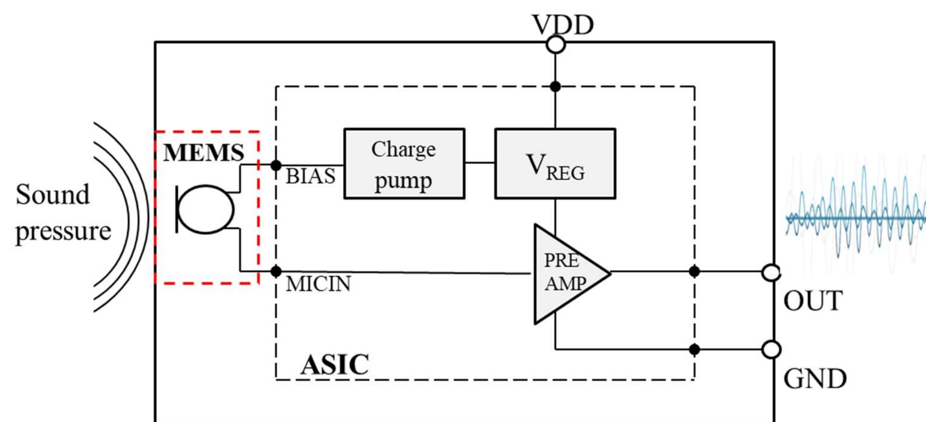


Fig 1.1 MEMS microphone schematic block diagram.

The most electronics sensor devices are related to the physical characteristic property which specified the performance of their sensors. There is involved factor such as sensor network loading impedance, current consumption, power supply rejection ratio (PSRR), etc. These factors are concerns to overall sensor performance.

As the same property characteristic of the acoustic device such as MEMS microphone encourages a mechanism with is directly capturing on sound pressure input related to mechanical damping and displacement membrane behavior. The output sensitivity is relative to the changing membrane, the sensitivity, and signal-to-noise ratio (SNR) is directly coupled to the quality of the sound. However, the SNR is a key function that is directly coupled to the clarity of the sound quality [4-7]. Currently, the most commercial MEMS microphone product maintained of the sensor sensitivity a range of -38 decibel (dB) and Signal to noise ratio is holding commercial specified around 64dB with mass production volume. Therefore, the type of some

smartphone manufacturers continues to keep the required product spec demand as higher and more of the SNR product performance for assembling into the generation of their innovative products. Furthermore, no sign of the stop of capping product demand [8]. Therefore, a higher signal-to-noise ratio of the MEMS microphone sensor was needed improves the performance for mobile-phone application. This is the main desired functionality must be adopting at the helm of its performance and mobile-phone manufacturers are demanding as higher SNR microphones. Incumbent silicon microphone suppliers are experiencing their cognitive limitations in critical SNR improvement due to their capacities sensing design and process.

The history of MEMS microphone development with capacitive sensor structure, and then the first condenser microphone was developed by E. Christopher. Wente at Bell Laboratories in 1916. However, this sensor device was used as an instrumental tool for measuring sound intensity. Later that, this structure was lead to continue developed for a condenser microphone with the smallest size as well as improved the signal quality for suitable of the sound signal tape recording. This is the standing point of MEMS microphone development and technology [9]. However, the most common of the microphone devices is designed for a musical apparatus, and there are commercial products regard to microphones were lauded to the consumers' market are used similarly as the dynamic, ribbon, and condenser microphone was referred on its characteristics and application purpose. Consequently, the general microphone they consist of each varies depending on the key mechanism of its sensing element structural. Therefore, the microphone can be designed with various other directional patterns and different acoustic impedance [10]. The dynamic microphone operation, when sound pressure is entered to the moving cone mounted with sensing coupling coil wire deflects move forward and backward across into the magnetic field. Meantime, the oscillator circuit will produce and generate an output voltage signal similar to the transformer acquired to sound pressure vibration. In the other hand, this characteristic behavior operates like the pressure microphone.

The crystals microphone demonstrates similar to the piezoelectric effected output that generates signal voltages when it shapes deformed and occurs with its orientation. This microphone structural implemented with using a thin film strip for the piezoelectric material to attach induced to a sensing diaphragm [11]. The keys mechanisms of the piezoelectric are comprised of two materials of thin film sheet of crystallizing plate to accumulate in certain materials. This sensor structure offers to increase the sensitivity gained with getting a higher yield of an opposite electrical polarity charge density when it was deflected with the driving force of the diaphragm deflection. Therefore, the magnitude of an output signal is related to the membrane stress and stain ratio that occurred on the material property deformation and

generating the output signal. However, as the crystal microphone's development in the past based on referring to the commercial products. There was applied using sensor membrane material such as the Rochelle-salt which can be generated a high output of the sensor signal gain. But unfortunately, this material is very sensitive to abundant moisture when exposed to a high-humidity environment and become too extremely fragile [12]. In the meantime, some material property has been found and its characteristic was similar to the ceramic materials characteristic properties which that material is the barium titanate and lead zirconate was introduced to apply for replacing Rochelle-salt. In this case, it nights improved by using this material to MEMS microphone structural which could be got the excellent alternative of sensing mechanism [13].

The summary of the various previous introduced of microphone product until now and it still continues developing as it performs. At that point, the electrical signal output of a piezoelectric microphone and condenser microphone is canned not comparable to sound signal quality better than the dynamic microphone and cannot be a contender for the musical market.

Now a day, the manufacturing of microelectronics technology has been extreme to develop high-level technology and high output capacity to fabricate of very small sensor devices. In the current market trend of the microphone with small package size, the most manufacturer is jumped playing on smart-phone and the same electronics gadget device business because of it very huge of the market size in the world. In the other hand, if we consider looking at microphone sensor that the capability to apply to the above mentioned. The commercial of microphone product there is the primary two products type launched in the market such as electret microphone (ECM) and silicon microphone (MEMS) only [14]. Most of the ECM is designed for small gadget devices but could not be compared with the studio standard microphones which they are more excellent frequency response characteristics.

However, the ECM consideration is structural construction might be similar to the family of condenser microphones, which is a typical use of the permanent polarized with electret material attached for moving plate diaphragm. Therefore, the ECM microphone is inexpensive of the unit price. However, unfortunately, with the ECM type is needed to work incorporate to circuitry interfacing with a field-effect transistor (FET) with conditioner circuit for the pre-amplifier and needed to match of high loading impedance to encourage the signal. Furthermore, the package of ECM devices is still farther bigger than MEMS microphone packaging. Therefore, micro-electro-mechanical systems based on silicon microphone come to replacing ECM in the mobile phone market and most of the electronics gadget devices.

In addition, information based on the microphone marketing survey, when did compare the market size. The EE Time online have reported and performed the economic analysis for the comparison of the market sharing of ECM and MEMS microphones. The market business microphone sensor based on MEMS devices has been hit $993 million in 2016[15]. The magazine is mentioned the published report from Yole Development (Lyon, France) as shown if Fig.1.2 the competition of market trend expected in units of million between ECM and MEMS microphone the rate of return compound annual growth rate (CAGR). The ECM microphone moderately obtains decrease CAGR of -2.6 % and MEMS linear increase CAGR of 11.3 % every year. However, Yole will reliably predict in 2022, which selling of MEMS and ECM for 5 billion units and sales rising to $20billion.

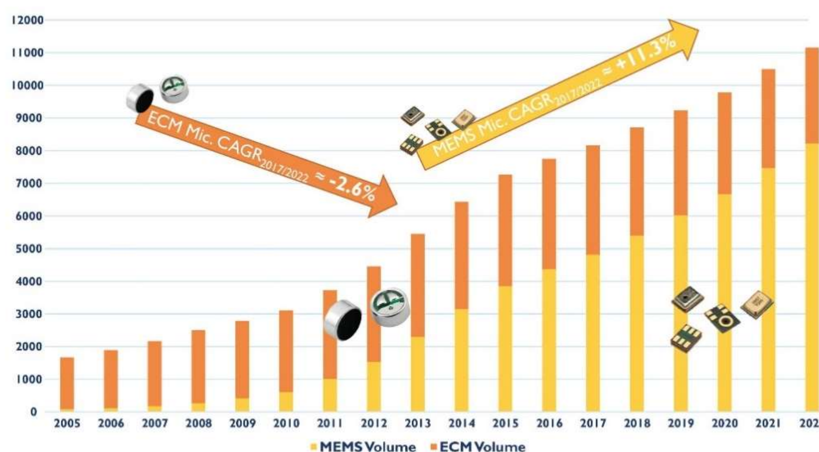


Fig. 1.2 The microphone market since 2005 (source: acoustic MEMS and audio solution 2017, Yale development).

Regarding the possible advantage of MEMS silicon-based with the fabrication process technology. In which it can be produced the devices scaling down of the device dimension in micrometers units for the MEMS sensor devices. Therefore, it can be produced with the large-scale production of MEMS product in the mass volume. At the well known, MEMS microphone has been outstanding to process performance and consistency of the device was maintaining continuous improvement to increase of the sensor sensitivity, low power consumption and offering significant as a high signal to noise ratio (SNR) of the devices.

The details in Table 1.1 is presented in comparison of sophisticated MEMS sensor in different type sensing element structural which were fabricated on a wafer substrate with silicon-based core technology consideration. The publisher literature-review of listening with type sensing element and their sensor performance listen.

However, based on overall information of three group of sensing element were considered. First, the optical sensing type it seems to be graduate obtained low-noise floor of the device performance but the readout system needed to include an optical sensor used to capture a moving membrane when its deflected. Therefore, this optical microphone is required complexity of packaging method.

T**able 1.1** MEMS sensing element comparison [16].

Author	Sensing	Sensitivity	Noise floor
Miles et.al	Optical	±	35.6*
Miles et.al	Optical	±	31.1*
Kadirvel er.al	Optical	±	70+
Miles er.al	Capacitive	±	43.1*
Scheeper er.al	Capacitive	22.4mV/Pa	23*
Martin et.al.	Capacitive	390μV/pa	41^{+}
Huang et.al.	Piezoresistive	1.1mV/Pa	53^{+}
Arnold et.al	Piezoresistive	±	52^{+}
Ashiqur et.al.	Piezoelectric	5.43mV/Pa	31.4^{+}

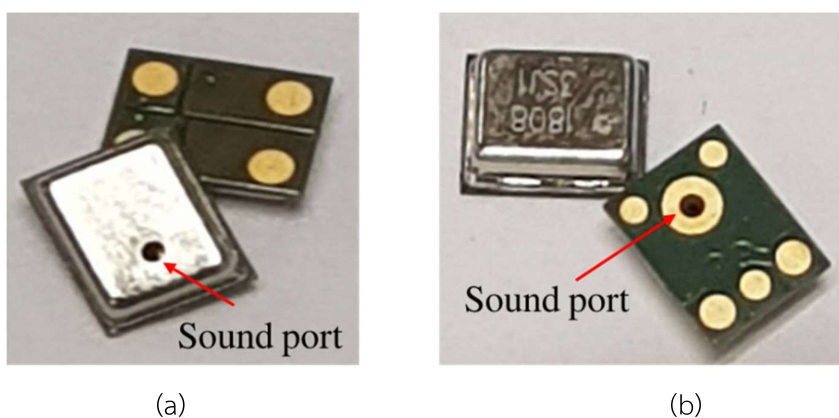
* A-weighted (dBA).
$^{+}$ At 1kHz frequency (dB SPL).
± Numerically not provided.

Second, the piezo material group with piezo resistive and piezoelectric both of these structures were needed to attach a thin film of piezo material directly deposited to the deflection membrane to obtaining of stress characteristics property. Then converts to an electric output signal. Based on the published results with a noise floor of the sensor performance graduate higher than other sensors and low-sensitivity as well as compares to the capacitive structure.

Third, capacitive sensing type which this structure seems to be achieved high-sensitivity and low noise floor. Therefore, upon consideration of the capacitive sensing structure is evidently of simply sensor structural with its component comprised of two conductor plates. For inducing an electric change density changing in capacitance values related to the deflection of the membrane. Regarding the comparison table, the transducer with a capacitive type author by Scheeper et.al. has achieved more extraordinary sensitivity of 22.4 mV/Pa. Due to the successful development of MEMS microphone sensor. As above mentioned, as well know of the capacitive structure is needed of the capacitor plate enlarger area to get higher of the capacitance values. However, it possibly will be become to limitation if needed the sensors dice size to be narrow down to below once square millimeter.

In this thesis concentrated studying only the MEMS microphone with a capacitive structure type. Due to this device was significantly achieved of the higher gain sensitivity than the other and noise floor significant performed. As well as the capacitive sensor, architecture is not complexity, moreover, the fabrication process is friendly as the same of CMOS compatibility process technology. However, beyond of MEMS silicon microphone in the market product cost competition. Therefore, the capacitive sensor structure quite to consistently of the improvement of the device, the way to increases, its performance as approaches at higher SNR to seem to be very interesting.

The final of working devices are needed to complete the microphone sensor packaging. Generally, in the MEMS microphone packaging level, they are having as the packaging separately in two types of the packaging method to assembly sensor as shown in Fig. 1.3. Thus, the microphone sensor depends on the product desirable application which assembled it into the printed circuit board (PCB) for the sound pressure entered a requirement. Fig. 1.3 (a), when assembled for the sound pressure, entered go thru at the same face to the membrane attach at the PCB of the same side with facing up. Fig. 1.3 (b) is shown of the bottom mount or inverse mount package, in this structure, the sound pressure is coming from at the opposite side direction.



(a) (b)

Fig. 1.3 Typical standard package of silicon microphone (a) bottom mount sound port, (b) top mount sound port.

Therefore, MEMS silicon microphone with the final packaging as mentioned regarding both structural configuring as shown in Fig. 1.4. In which two kind difference enclosed design with the cross-sectional view purposed to improve SNR. This is suitable based on the fluidic dynamic of an acoustic pressure flows spreading properties inside the package. However, the limitation of the capacitor plate area of MEMS capacitive sensor and ASIC are located inside of a metal lid which purposed to reduce the damping resonance acoustic noise as design consideration [17]. In addition,

this product packaging has also shielded of influence as external un-wanted excessive noise influence from radio-frequency interference (RFI). The possibility to improve the capacitive sensor sensitivity by fixing dropped sensitivity by increase the capacitor plates area and reduces the desired membrane thickness of the moving sensing element. But with both approaches will be delivering a negative impact on a device as capitation cost and unstable of the deflection membrane. Furthermore, an ultra-thin diaphragm is a weakness when exposed to the over-pressure and membrane deform with electrostatic collapsed [18], as shown in Fig. 1.4 which comprise two diverse structures. Fig 1.4 (a) is the conventional capacitive sensor structure with given the air gap-shape, this structure is called a BOX cavity it similar rectangle shape. As the same time as shown in Fig. 1.4 (b) there are offers to get the optimization of the useless area in the capacitance plate to compensate for increasing to be got higher capacitance value. In this structure, air gap was designed performed symmetrically shape to corresponding of the deflection membrane approach to an ideal case for the capacitor as parallel plates working operation and called this shaped as a contoured cavity (CTC).

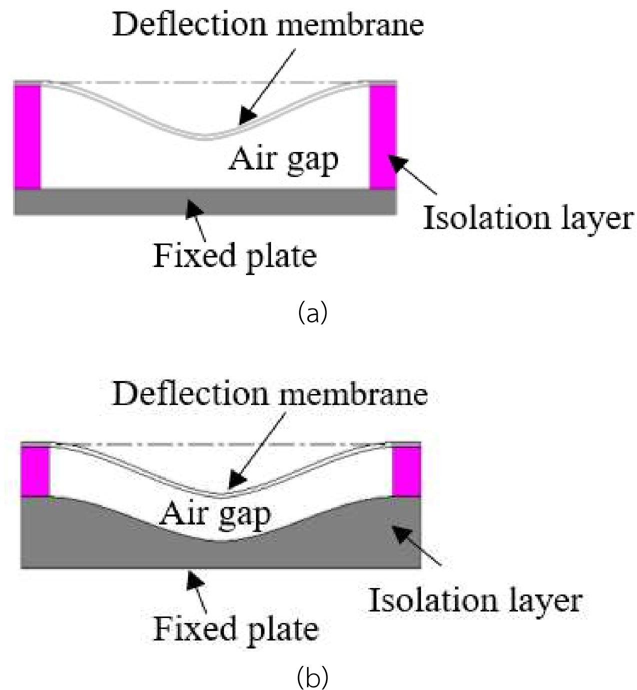


Fig. 1.4 Illustration of capacitive air gap structure (a) conventional BOX cavity, (b) Ideal case contour cavity.

According to the limitation an area of the capacitive sensor performance with the capacitive parallel plate structure, it was solved for those limitations of the conventional BOX air gap cavity. Thence, for circular moving plate membrane is maximum displacement range at the center parts of it is only. However, this membrane

deflection is occurring at only 2/3 of the diaphragm area when it was deformed. However, the 1/3 of the diaphragm area along the edges does not move parallel to the fixed plate due to close to the clamped area body. Therefore, the BOX structure there does not contribute to the overall change in capacitance value [19].

In this case, the assumption of the research study is optimized the rigid area of the fixed plate can be manipulated in relevance to a moving plate can be acquired. A capacitive sensor design fundamental with a contour curvature shape that the most optimal design to get the advantage of the rigid area. However, the fabrication process to achieve forming the contour in an ideal case style is more difficult. Therefore, as a multiple steps etching is needed to perform its shaped similar to staircase profile and multiple photomasks were required at lithography processes and it will drastically increase the cost of manufacturing and loses its competitive edge. Therefore, the challenging developing in which to be approaching both lithography and etching processes to be performed a single step process.

1.2 Research objective

The aim of this research is to design and develop the fabrication process of MEMS microphone structure with similar of a staircase contour cavity structure (S-CTC). Which is implemented of a new three-dimensional (3-D) lithography process as special technique method by using the multi-film transparency (MFT) mask, it would be formed a 3-D microstructure profile and fabricated on a silicon substrate. The research topic is included as following.

a) Study on MEMS capacitive silicon microphone structure design which obtains CTC structure.
b) Design and fabricates the MFT mask for single lithography process to formed the S-CTC profile.
c) To fabricates of MEMS sensor capacitive structure.
d) Device electrical characterization on wafer lever with probing station.

1.3 Thesis overview

This thesis is typically organized into six chapters. Chapter 1 properly introduced and motivated the key topic of this dissertation. The modeling of capacitive structure relevant to this work is discussed in chapter 2. The design and theoretical performance of 3-D lithography process are presented in chapter 3. Chapter 4 describes the details of device fabrication. The experimental results are discussed in chapter 5. Finally, concluding remarks is given in chapter 6.

Chapter 2
CAPACITIVE STRCUTURE SENSOR DESIGN

In this chapter, the detailed modeling of the deflection of the flexible membrane, an electrostatic force on parallel capacitance plate, finite element model and air gap structure desired is presented. The microphone device operation begins with the appropriate behavior of the sensitive membrane when it is exposed to the sound pressure. The incident of acoustic sound pressure at a movable part varying with its distance effects to output changing the capacitance.

2.1 Membrane deflection

The capacitive sensor for MEMS microphone application is generally comprised of two main components as known, there is a moving plate is called membrane (diaphragm) and the fixed plate (backplate). Both plates were isolated by an air gap and clamped them together by the isolation layer such as silicon dioxide material. In this case, the deflection membrane is used to reliably detect the exterior sound pressure and the sensing plate was affected by the changing of the gap between the capacitor plates [20].

However, the proper method to simplify for analysis the membrane properties is assumed that it is maintained with homogeneous, asymmetric, and linearly of elastic material. Which is circular microphone membrane is assumed as physical properties as the perfect clamped boundary condition on the circular membrane edge and assume as stress is free deformation of membrane material [21]. The Fig. 2.1 showed a schematic of idealizing of microphone membrane, there is a critical membrane radius is *a* and the membrane thickness is *h*.

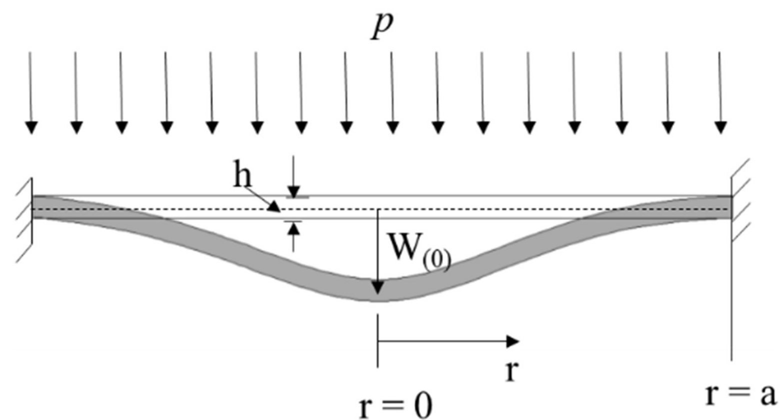


Fig 2.1 Schematic of deflection membrane.

The material relation is the property of elastic Young's modulus and Poisson's ratio assumed. The constant parameters of load pressure when applying the external pressure $\boldsymbol{p}$ incident to the membrane at the in-plane surface. While the magnitude of the flexible membrane is deflected to typically increase its gradual displacement $W_{(0)}$. Therefore, the moveable membrane was having small deflects at an initial neutral plane axis. The general differential equation form of intimate displacement of the circular membrane plate is given by [21]

$$\nabla^4 w = \frac{-p}{D} \tag{2.1}$$

Where

w is the membrane deflection plate distance

D is the flexural rigidity of the moving plate

The flexural rigidity with general equation yielded by

$$D = \frac{Eh^3}{12(1-v^2)} \tag{2.2}$$

Where,

E is Elastics young's modulus

h is membrane thickness,

v is Poisson ratio.

When the load is spread by an exterior sound pressure into the circular membrane and it was clamped boundary at around perimeter region an axisymmetric. Therefore, the flexible membrane deflects is only ordinarily occurred at radial cylinder coordinate of *r*, from equation (2.1) we can be simplified as

$$\frac{1}{r}\frac{d}{dr}\left\{r\frac{d}{dr}\left[\frac{1}{r}\frac{d}{dr}\left(r\frac{dw}{dr}\right)\right]\right\} = \frac{-p}{D} \tag{2.3}$$

To solving equation (2.3) with the boundary conditions of the clamped membrane plate characteristic in which attend the significant deflection traveling range at the center. The deflection is naturally zero at the clamped boundary, and plate slope at the clamped area to the center of the plate is assumed to zero. Respectively, the deflection of the moving plate is provided by

$$W(0) = \frac{-pa^2}{64D}\left[1 - \left(\frac{r}{a}\right)^2\right]^2 \tag{2.4}$$

Substituting this expression, the flexural rigidity from equation (2.2) into Equation (2.4) to govern the flexible membrane deflected geometry typically relates to including material properties and is given by

$$W_{(0)} = \frac{-3pa^2(1-v^2)}{16Eh^3}\left[1 - \left(\frac{r}{a}\right)^2\right]^2 \tag{2.5}$$

The membrane deflection shape is typically given by the practical term of $\left[1 - (\frac{r}{a})^2\right]^2$, while the center membrane displacement $W_{(c)}$ is given by

$$W_{(c)} = \frac{-pa^4}{64D} \tag{2.6}$$

2.2 Electrostatic forces on parallel plate capacitor

In the parallel plate capacitor theoretical is consisted of two conduct plates with obtained specific area *A* and plate separation *x*, the established equilibrium of mutual capacitance is given by

$$C = \frac{k\varepsilon_0 A}{x} \tag{2.7}$$

Where,

k is typically the relative permittivity of the dielectric material

ε_0 is permittivity of free space.

In this case relative permittivity of air equal to 1. However, the capacitive structure for the sensing of MEMS microphone is considered as one type of an electrostatic transducer element. Therefore, the electrostatic behavior of the sensor as used modeling as the two plate electrostatic moves in distance *x'* [22]. Accordingly, the time-varying domains of mutual capacitance can be defined as

$$C(t) = C_0\left[1 - \frac{x\prime(t)}{x}\right]^{-1} \tag{2.8}$$

When the voltage potential is applied to at the capacitor plate terminal pole, the charge density was induced to the plates surface [23]. Substituting these charge in equation (2.8), the desired voltage across the user terminal is written as

$$V(t) = \frac{Q(t)}{C_0}\left[1 - \frac{x\prime(t)}{x}\right] \tag{2.9}$$

The specific charge with difference polarity either as positive and potential negative between the parallel plate is induced result in an electrostatic force in the time-varying domain as given by [24]

$$F_e(t) = -\frac{1}{2}\frac{\varepsilon_0 A}{\left(x - x'(t)\right)^2}V^2(t) = -\frac{1}{2}\frac{Q^2(t)}{\varepsilon_0 A} \tag{2.10}$$

The relative of the electrostatic force and membrane physical mechanism will be further explained for an electrostatic pull-in mechanism [25]. The performance of an electrical characteristic for a capacitive sensor device when applies bias input voltage. The membrane deflection geometry formation as shown in Fig. 2.2. When two plates were applied by bias input voltage then extract the membrane travels force to a fixed plate.

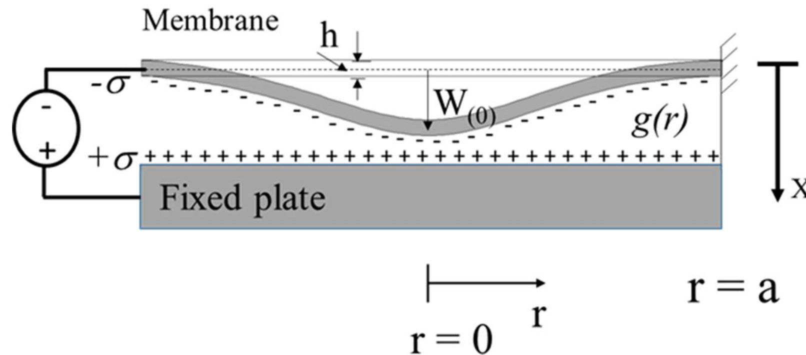


Fig.2.2 Two plate electrostatic transducer modeling [26].

The approximation was useful to provide physical insight into the behavior of the microphone as well as scaling information. The prediction of capacitance more accurately values based on a capacitive structure is needed to consider. However, the air gap is no longer assumed to be uniform. The deflection is assumed to be small of the charge density on the surface of the capacitor plate is constant. The capacitance is directly formed and merely given by the following

$$\int_{+}^{-} E.ds = \frac{Q}{C} \tag{2.11}$$

Where,

E is electric field

Q is electric charge

C is capacitance value.

Instead of two conductor plates with an infinitesimal area of ***dA***. However, with opposite surface charge densities of potential magnitude σ, the electric field at between two conductors plate is $-\hat{x}\sigma/\varepsilon_0$. A capacitance, ***dC***, exists and is given by

$$dC = \frac{dQ}{-\frac{\sigma}{\varepsilon_0}\int_{g(r)}^{0} ds} = \frac{dQ}{\frac{\sigma}{\varepsilon_0} g(r)} \tag{2.12}$$

By considering that $dQ = \sigma dA$, equation 2.12 is rewritten as

$$dC = \frac{\varepsilon_0 dA}{g(r)} \tag{2.13}$$

The total capacitance is found by integrating over the entire area of the conductor plates. The gap distance, *g(r)*, equal to the nominal gap range, g_0, to subtract the plate deflection geometry shape given by following equation

$$c = \int_{0}^{a} \frac{2\pi\varepsilon_0 r}{g_0 - w(0)\left[1-\left(\frac{r}{a}\right)^2\right]^2} dr \tag{2.14}$$

This functional integral was solved; it obtains two solutions: one for a positive deflection membrane

$$c = \left\{ \frac{\operatorname{arctanh}\left(\sqrt{\frac{w(0)}{g_0}}\right)}{\sqrt{\frac{w(0)}{g_0}}} . \frac{\varepsilon_0 \pi a^2}{g_0} : w(0) \geq 0 \right. \tag{2.15}$$

And negative deflection

$$c = \begin{cases} \frac{\arctan\left(\sqrt{\frac{-w(0)}{g_0 \geq}}\right)}{\sqrt{\frac{-w(0)}{g_0}}} . \frac{\varepsilon_0 \pi a^2}{g_0} : w(0) \leq 0 \end{cases} \tag{2.16}$$

The capacitance given in equation 2.15 and 2.16 in commonly is the mean capacitance multiplied by a scale factor when the membrane deflection is typically zero, the scale factor is one.

2.3 Finite element modeling

Finite element modeling is often performed on the MEMS membrane to determine the optimal position for the membrane deflection and the optimum shape of the capacitive structure gap between the plates. Therefore, the specific behavior of membrane deflection as such mechanical properties characteristic can be determined. The calculation method with a computer-aid analytical modeling has easier using to correct the predicting of membrane behavior and can be governing the desired product specification. However, this device was typically designed based on the infrastructure compatible with CMOS technology fabrication process at Thai microelectronics center (TMEC), to fabricate of the full loop of a 6-inches wafer of MEMS capacitive sensor structure. Based on this capacitive sensor's membrane is required using the polysilicon (Poly-Si) thin-film with LPCVD deposition material. This material property is widely used general for formed the gate electric interconnection as required of the low-resistance electrical property. Meanwhile, in this research studied was determined the properties of membrane for microphone application to capture of sound pressure. Which the sensing element as the following specification of the material properties has been used in this experiment modeling as presented in Table 2.1.

Table 2.1 Material properties of polysilicon for the simulation model.

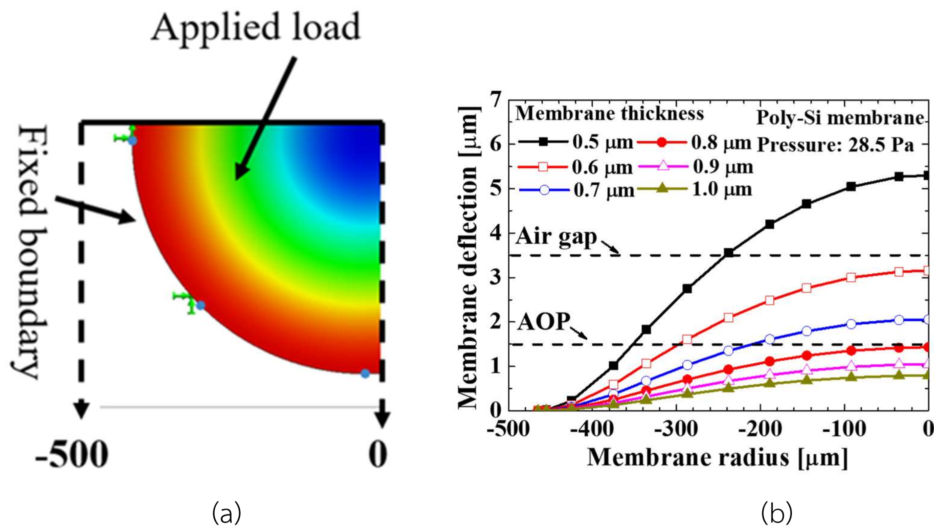
Property	Value	unit
Elastic Modulus	$1.6 \times 10^{+11}$	N/m^2
Poisson's ratio	0.22	
Mass density	2320	N/m^2
Yield strength	$1.45 \times 10^{+11}$	N/m^2

The simulation software for using the computer aids finite element modeling (FEM) designed is used the SolidWorks commercial software to predicting the behavior of moving plate membrane with corresponding to polysilicon thin-film material. This solver method, that performed to find out an appropriated the membrane thickness

that related applied maximum of sound pressure. The relation with the specified of the varying Poly-Si thickness was simulating of the desired membrane thickness of 0.5 μm to 1.0 μm. The membrane diameter was obtained as smallest than 1,000 micrometers and the membrane diameter of 930 μm was tested for this experiment.

Therefore, the varied membrane thickness was assumed that is related to deflection performance, due to the mechanical material stiffness and needed to define an appropriate membrane deflection suitable for MEMS microphone. However, in general terms, the desired performance of MEMS microphone devices is involved determined by limiting maximum load pressure when applied. The most condition that to define MEMS microphone product characteristic property, these parameters representative as the keys to developing for determining the capacitive sensor. The capacitive sensor with a narrow air gap configuration is limited due to the collapse of the membrane when exposed to high acoustic pressure and might be caused to non-linearity on frequency bandwidth characteristic. In this capacitive sensor structure designing, the maximum air gap is fixing determined at 3.5 micrometers for the sensor isolation layer between the capacitive plates. Therefore, the acoustic overload point (AOP) is performed to maintain at the target of 40%. The possibility of the maximum of membrane displacement ranges with the deflected state before collapsing to the back-plate [27].

Fig. 2.3 shows the model simulation was plotted, this performing related with membrane deflection characteristic property when applied the maximum load pressure, which the varying of membranes thickness from 0.5 μm to 1.0 μm was selected for validating into the simulation model. At the specified, the maximum load pressure of 28.5 Pa is applied into membrane at in-plan surface, which this number is equivalent to 123 Decibels of sound pressure level (dB-SPL). The consistent of membrane deflection resulted is related to the thickness as moving thin plate membrane are involved the plate deformation when exposed by over-load pressure. The thin membrane was significant got more plate deformed as far moving more than the thicker membrane, in this simulation resulted have been found that a 0.8 μm of the polysilicon membrane thickness was suitable offered as the best of the performance condition. Therefore, the AOP is used as the reference position to consider the base-line the determining of the capacitive sensor plate as corresponding with the material physical properties, that approaching to get the high achieved performance of silicon MEMS microphone.



(a) (b)

Fig. 2.3 The effects of polysilicon membrane thickness with FEM (a) the contoured deflection membrane (b) the relationship of polysilicon membrane thickness versus maximum applied load pressure.

In addition, the AOP is delivered as the designing limitation of the purposed for both plate capacitance structure, which is determined the maximum distance that can be referred to preventing the membrane deflection collapsed to the back-plate. However, the contoured shape of an air gap cavity due with membrane deflect will be formed to the back plate structure to compensate the optimal sensor structure. These profiling has correspondence with the maximums pressure was deployed. The normalized plotted of optimal polysilicon membrane of 0.8-micrometer deflected as shown in Fig. 2.4.

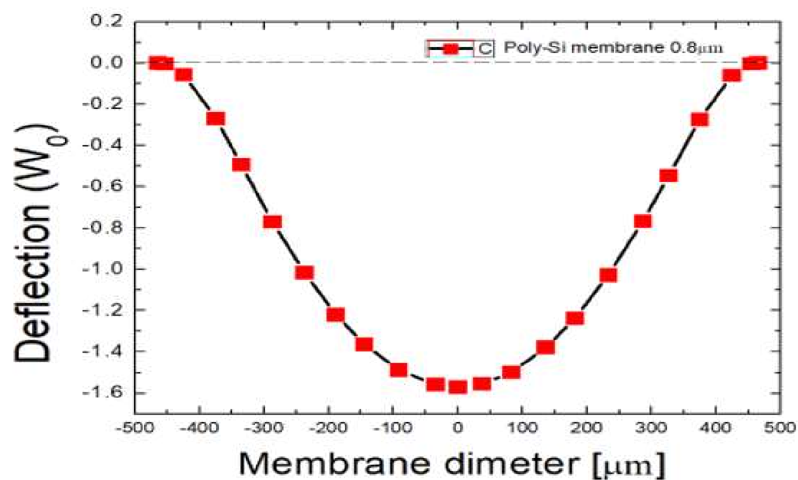


Fig 2.4 Normalized deflection of circular clamped membrane.

The behavior of the deflection membrane is related to the material properties that conduct to the moving plate bending deformation, such as contour curvature profiling structure. However, the output capacitance of the sensor can be predicted by using the simple parallel capacitor method to determine the sensor performance, this capacitive sensor structure is considered with the changing of a gap for calculating the predicted capacitance value. Therefore, we can properly calculate the capacitance value and sensor sensitivity corresponding to the diaphragm with its deflection. However, the MEMS microphone based on the sensing element with the capacitive structure can be predicted with an applied testing reference pressure of 1 Pascal (Pa) when the air gap changed in the parallel plate capacitor. The proportional of an air gap change is related to the changing of the output of sensor values, the membrane deflection leads instantly changing in the physical sensing element of the capacitive sensor then transfers the mechanical changing to the electrical signal.

The consideration of the distance between two plates adequately to taken into account the sound pressure input. Therefore, the sensitivity prediction of MEMS capacitive sensor is defined with the relation of applying pressure and gap changed [27]. Fig. 2.5. is shown the relationship of capacitance changing calculated from the polysilicon membrane with 0.8 μm thick deflected and relative the air gap changes. In the capacitance given in equation 2.14, the mean output capacitance is multiplied by a scale factor by one.

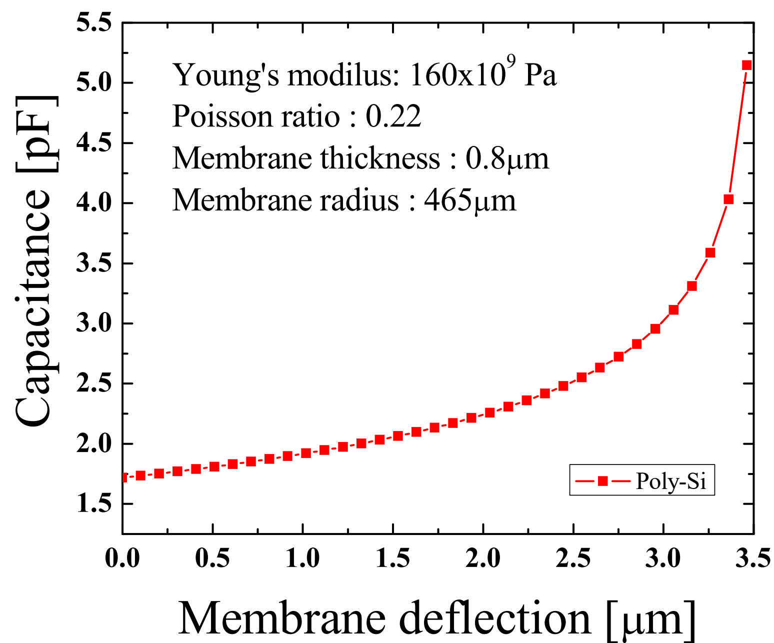


Fig. 2.5 The relative of deflection membrane and changing capacitance.

Therefore, the capacitance can be predicted by using of the simple parallel plate model where at the initial position state of a membrane refers at zero deflections (C_0), in this studied the predicted of capacitance with the fixed membrane diameter of 930 μm is equal 1.718 pF and the changing capacitance is obtained along with the gap changed. Furthermore, the geometry profile with membrane deflects on this shaped can be extrapolated to the capacitive structure design for MEMS microphone. In addition, Fig. 2.6 shows the simulation result of the polysilicon deflection model and the cross-sectional structure. However, this capturing imaged profile was represented of the contour profiling as shown in Fig. 2.6 (a), where the color ingredient shading shows that a contour plotted and its distribution represented of membrane deformation as well as applied indenting load pressure. Fig. 2.6 (b) is represented as a normalized of the referent of an initial membrane state at zero deflections, Fig. 2.6(c) is represented to the possibility of the maximum membrane deflecting a membrane and Fig. 2.6(d) is a collapsed position touching to the backplate.

However, the specified type of air gap is identical such as the conventional chamber gap, and it is called a box cavity (BOX). Evidently, the maximum deflection of the diaphragm ordinarily occurs at the center of a diaphragm, and 1/3 does not get any advantage of the air gap optimized at located along adjacent the region of the circumference section.

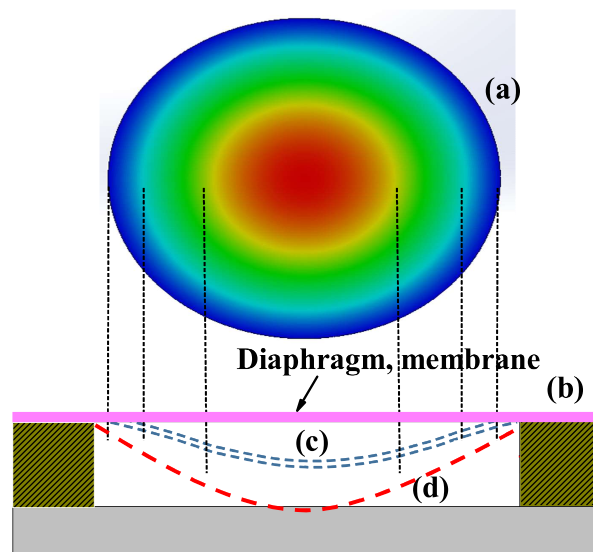


Fig. 2.6 The simulation results of the deflection of 0.8 μm and designed state parameters.

In this case, the backplate can be typically adjusting to re-forming the optimal air gap structure with defining the appropriate gap profile shape. The possibly that can improve the sensor performance as much as higher capacitance value, due to arranging of the gap of the capacitive sensor to become closer [28].

2.4 Capacitive plate structural design

In order to design the capacitive sensor structure with a curvature profile that desired to formed the back plate deflection membrane contoured with fixed plate formation. The considerable distance between the standard plates or air gap distance needs to be wisely determined. Therefore, a finite element model (FEM) is used to develop for determine as the precisely of the air gap thickness, and suitable membrane diameter size. Thus, to arbitrary constants as suitable based on the fabrication processes were chosen as correctly capacity of the processing method.

The polysilicon membrane same of 0.8 μm-thick circular shapes with a diameter of 930 μm was interpreted as the membrane. The modeling is first tested as acoustic overload pressure of 28.5 Pa to condition the air gap between both developed plates. The desired result shows that the AOP maximum membrane deflection reached 40% of the total air gap distance at the center of S-CTC and moving plate. Therefore, this modeling has been typically extended to objectively evaluate the maximum collapsing pressure. It was obtained that the membrane collapsed when the applied sound pressure was proportionately increased to 128 dB-SPL. The maximum air gap of 3.5 μm is instantly determined for the touching point of a collapsed membrane for this desired capacitive sensor structure. Therefore, the S-CTC structure is depended upon to properly compensate for the parallel distance between the two plates. The optimized silicon etched considerable depths calculated from FEM for S-CTC with three different step heights are approximately equivalent equal 1.5, 1.0 and 0.33 μm, respectively.

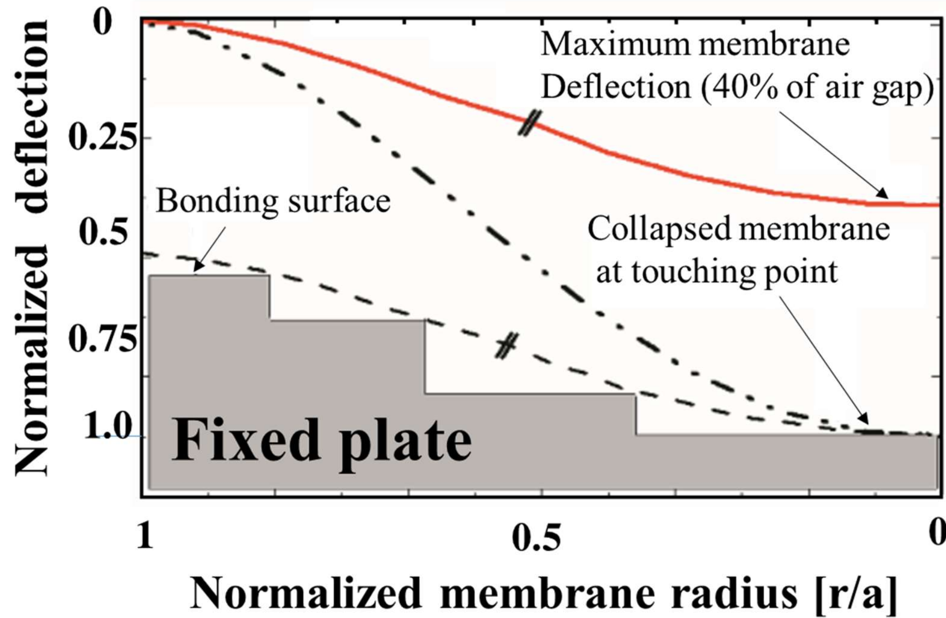


Fig. 2.7 Normalized membrane deflection on CTC structure.

As mentioned above, referring to the fundamental capacitive structural of the microphone device typically as the two parallel plates structure. The Fig. 2.7 is cross-sectional schematically to the considered state of the art corresponding introduces to the sensor design and determine the device structural as well as the air gap profile configuration. Therefore, this specified parameter of capacitive sensor with air gap structure, the fixed plate and the other electrode in common is called a diaphragm. Here, the diaphragm gently bends or there is attracted toward to the rigid electrode or the fixed plate. Furthermore, there is in the Fig. 2.8 describes three different forms of the chambers cavity including BOX, CTC, and S-CTC structures as shown in which Fig. 2.8 (b) shows a standard BOC structure, Fig. 2.8 (a) shows a CTC structure and, Fig. 2.8 (c) shows an S-CTC structure. The CTC structural is typically produces the optimum base on the optimal condition in which desired sufficient compensated the air gap distance between both the rigid plates. However, a polysilicon membrane is considered as constant deflects to the entire of the plate area while applying sound pressure. Therefore, Fig. 28 (a) is represented with an ideal structure that there is the most compensated the air gap achieved to get as higher outcome of the capacitance value. Accordingly, based on the optimization air gap with curvature on the fixed plate profile was geometrical along with a membrane deflection characteristic. However, at the current technology of the fabrication process still does not have practical solution methodology for fabricating based on this CTC structural formation. Therefore, many of manufacturers were fabricated only with conventional capacitive structure BOX

cavity, and it would become to the limitation of the capacitance plate area due to targeted of small dice size has been required to smallest. The ways how to move on steps forward the development based on the building the sensor with a capacitive structure which increases at the outcome capacitance values beyond with the limitation of capacitor area reducing. The fabricating such a design with the unique in case of an S-CTC structure as shown in Fig. 2.8 (c), the fixed plate is assumed as nearly parallel to the deflecting membrane. Therefore, it is expecting that the superior performance of the S-CTC structure would be similar to the CTC depend on the number of the staircase's steps. However, this structure would be a helping to support the process as well as flexible to fabricate in mass production at a competitive cost [29].

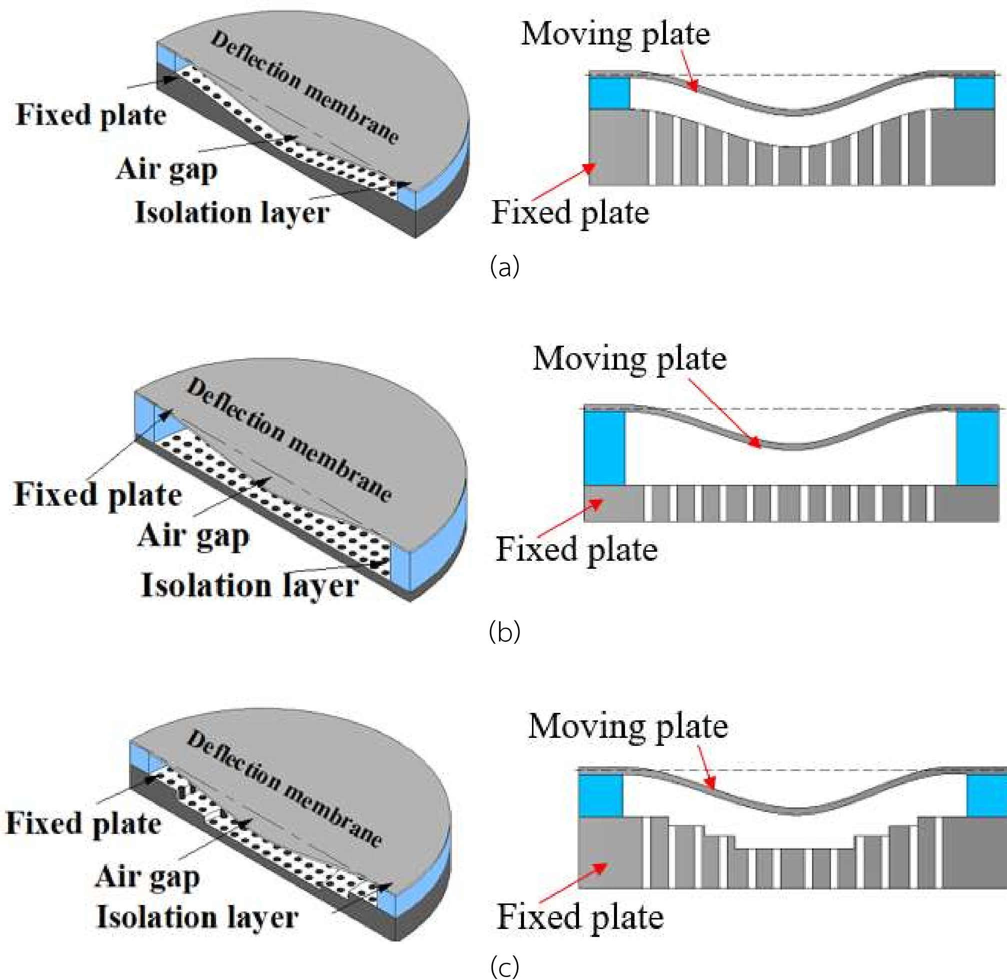


Fig. 2.8 MEMS silicon microphone capacitive structural cross-sectional profile (a) CTC cavity, (b) BOX cavity, and (c) S-CTC cavity.

Table 2.2 comparison of capacitive designed structure.

Criteria	Capacitive sensor structure		
	(1) CTC	**(2) Box**	**(3) S-CTC**
Capacitance (C_0)	40% increase	C_0 = nominal	20% to 40%
Plate area (A)	Similar membrane dimeter	Similar membrane dimeter	Similar membrane dimeter
Fabrication Process	None	Conventional process	Multi-mask layer
Cost	None	inexpensive	Depend on multi-layer
Process time	None	1 cycle	multi-cycle

The detail in Table 2.2 is the summary the comparison of each sensor structure which referring based on BOX cavity structure. Obviously, based on the calculation of the capacitance output in an ideal case with CTC structure is obtained higher increased at 40% and with S-CTC structure has increased in between with about 20-40% depending on the numbers of steps that constructing formed for S-CTC structure. The fabricating process of the BOX structure is used as the same of conventional processes and the fabricated of S-CTC is needed to repeat the process of lithography for patterning multi-level etched profiles and cavity etching were performed. Therefore, the manufacturing cost and processes cycle time of S-CTC structure is depending on the desired staircase structural with the number of steps were needed.

Chapter 3
THREE DIMENSIONAL LITHOGRAPHY PROCESS

In this chapter, a detail of the conventional and three dimensional (3-D) lithography process are presented. The 3-D lithography process with the using of multi-film (MFT) mask is a new development of photomask with chromium transparency thin film material, which it can be filtering or limit of the intensity of light exposure dose. The purposed the MFT mask reduces the structure of a multi-level of a capacitive S-CTC cavity etched depth and transfers it to mask layout design. The multi-levels of chromium thin were deposited on to the soda-lime glass substrate when exposed this MFT mask with light going thru to photoresist then the 3-D microstructure is formed. However, the photolithography is the main core process integration used in the semiconductor and MEMS fabrication process to transferring the design of the device and layering that layout transfers onto the costed photoresist by light. The insight the lithography process is an activity that related to the light intensity and photoresist will be constructed.

3.1 Positive photoresist physical property

The photoresist (PR) or resist obtains a light-sensitive material to compose a patterned coating material on wafer surface used in the photolithography process to form the devices to construct their patterns and critical dimension to open interested process areas. The resist forms structural itself by the light with the corresponding wavelength of the light is used. Generally, the photoresist is designed for sensing to wavelength of ultra-violet light (UV). The photoresist contrast is usually defined as the development rate performance with the function of an absorbed quantitative of exposure light dosage. This parameter governs the kinetics of the chemical reaction at the coating photoresist [30]. However, the photoresist with high contrast indicator shows at the minor dark erosion term and developing chemical from a certainty of dose D_0 depend on at a constant rate composition. However, in the meantime when the photoresist was exposed to the UV light with $D < D_0$ has stayed on the substrate. Fig.3.1 is shown normalized plot relation of the contrast curve profile responding of photoresist and some remaining of photoresist that related to film thickness coated after the development process, therefore, D^{-1}/D_0 represented as the function with the exposed dose. The patterns transferred structural profiling of the PR which providing which as contrast formation to an individual lithographic process. The requirement information of process-specific limitation that influenced on the concentration of development rate such as PR coated thickness, soft-bake temperature, rehydration exhaust, developer chemical, process development time. All of these is related

parameters of the framework factor and relevance to the temperature and humidity used [31]. The contrast curve is plotted with an ideal characteristic property of the type of positive resist. There is response function as a real contrast curve that influenced by $D^{-1}/D_0 < 1$ and considered with an exposure dose is equal zero. The dark erosion factor and a logarithmic in D^{-1}/D_0 responding function become greater than zero. However, the range of an energy exposure dosage is moving towards and remove the PR thick to the bottom D_c. Based on this stage responding curve is considered as called with "the dose to clear" located at the bottom region. Therefore, an exposure dosage among in between can be re-arranged to establishing for three dimensional structures that needed to formed and still remained at the coated photoresist material.

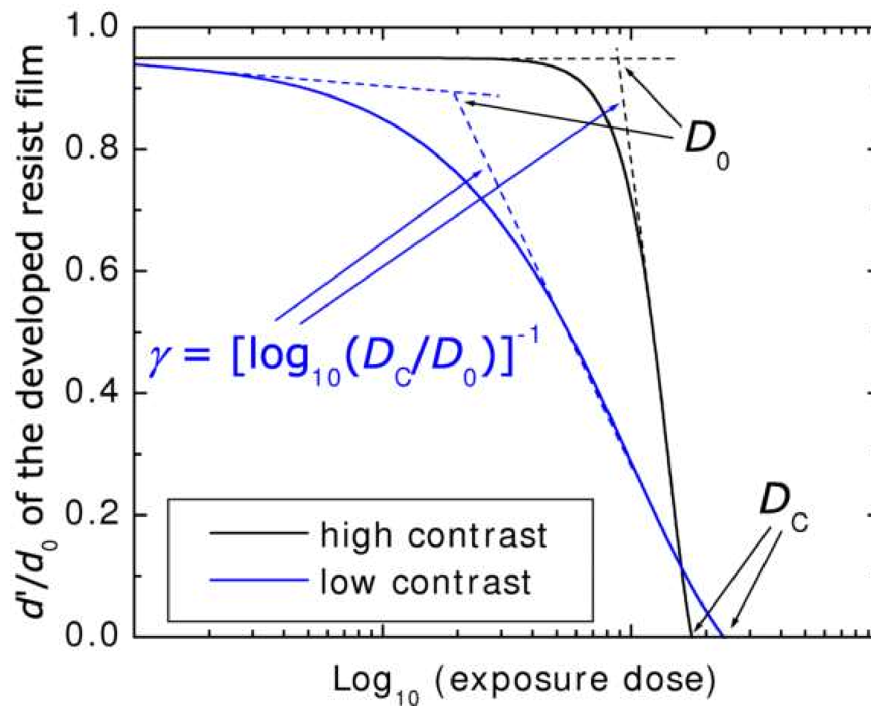


Fig. 3.1 Normalized contrast curve of the photoresist and development remain film [32].

3.2 Conventional lithography process

The lithography process is provided into two typical catalogs selective types which based depend on the process selection of photoresist material and process requirement. There are positive type and negative type as shown the process block diagram in Fig.3.2. The positive photoresist has chemical composition included with the three main principal components, first know as photosensitive component material

some time is called the photoactive compound (PAC), second is a novolak resin to provide to form the structural material based as stability and provided of the etch resistance property as the masking layer, and third a solvent material to holding the whole photoresist material in liquid state formed provides for coating process [33]. By which the positive PR mechanism property is to determine if an area is exposed and it becomes a dissolution when a process in the development steps. In the opposite side, the negative photoresist is a type of which the portion of the photoresist exposed to light becomes insoluble to the developer. The unexposed portion area of the photoresist is become dissolved by the developer [34]. However, in this academic research would be used only positive resist type for all the experimentation because of the lithography equipment is providing support only for positive photoresist tone.

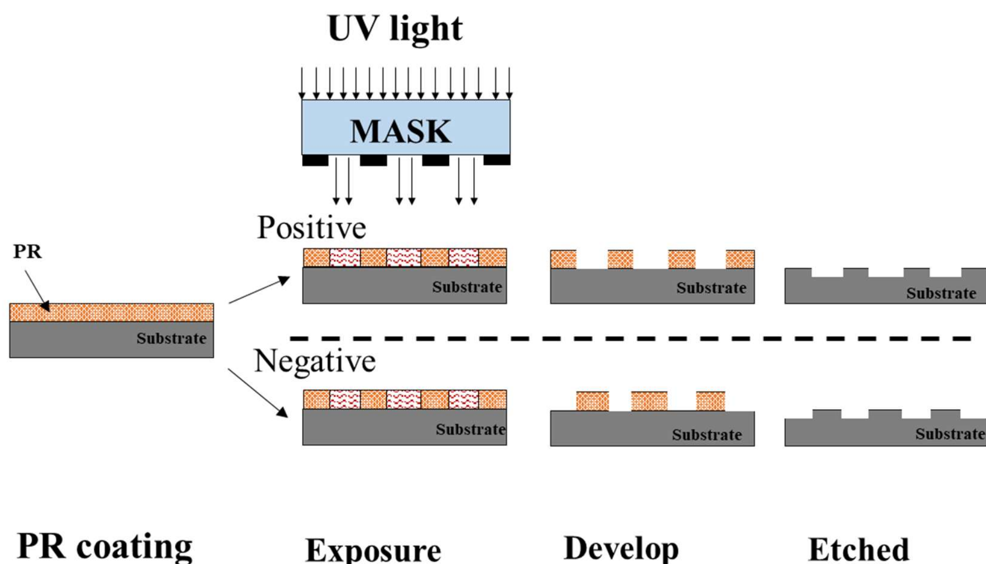


Fig. 3.2 Diagram of conventional lithography process positive and negative.

Based on the technology of Microelectromechanical system devices (MEMS), which this device structural has to consist the combination of many elements that required interfacing to more complexes of physical control function or input sensing device as needed. For example, microfluidic MEMS chip for the medical device such as micro-pumps its consists of many manipulates control valve and pump were fabricated [35]. However, the device physical design to get extreme with complexity special structure and its element sizing was fabricated in micrometers scale. Besides, the microstructure with fabrication process is refers based on the silicon wafer and some of the product is desired to be reached for approached the mechanical structural that desired to achieve as higher performance outcome. In addition, the MEMS devices involved in this research there is one of acoustical sensor that needed to detecting

ultralow pressure from sound and using of very thin membrane and its size in the micrometer scale.

3.3 Three dimensional lithography process

As general information related to MEMS devices that obtained as the specified requirement as upon the correspondence to as material properties. Therefore, there were expected to have of the particular structures such as three-dimensional (3-D) structure profile formation is needed for fabrication. However, the three-dimensional profile based on the lithography process utilizing to get advantage with fabricating in 3-D microstructure profile. It can be arranged with moderate control of the intensity of the exposure tool to form the 3-D structure profile and established at the coated photoresist material. Therefore, the photoresist with 3-D structural can be fabricated with control the amount of an exposure energy dose variation [36]. Fig. 3.3 shows a process block diagram of varying exposure dose and control the exposing area with shifting the exposure stage. The different location on the wafer substrate will be obtained a multi-level of UV light intensity dose. When developing the exposed patterns on the photoresist then the 3-D microstructure profile was formed and the staying PR-thick related. The transferring of the resist patterns and structural profile in resist height to the wafer substrate delaying the etched depth selectivity with the plasma etching method. At the wafer substrate will be transferred the same structure of PR profile to the underneath wafer as well as a single etch step [37].

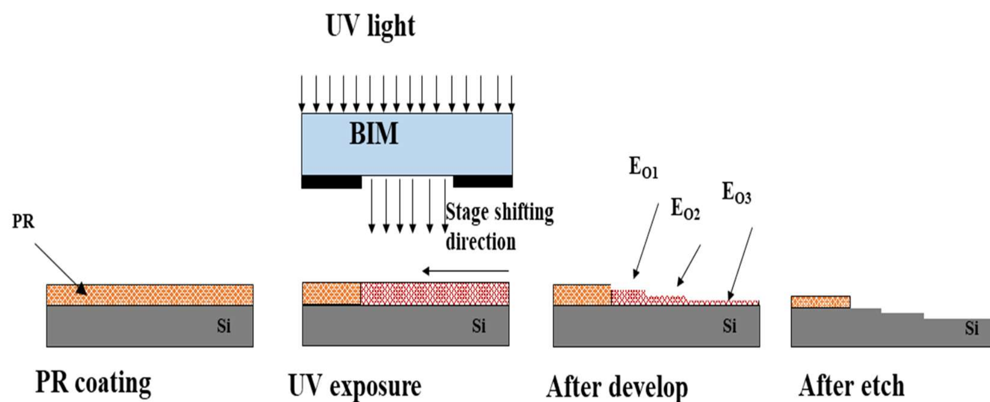


Fig. 3.3 Diagram of 3-D lithography process with multi-dosage variation.

3.3.1 Gray scale lithography

Concernedly, of the 3-D lithography with the one time exposed technology. The grayscale technique is an advantage involved to light diffraction modulated of an intensity magnitude and spreading interference of that incident light [38]. Therefore,

when the lighting exposed thru an obstruction slits patterns or their gap the output traveling of intensity spreading changed with become to varying modified the amplitude in multi-exposed energy dose into underneath photoresist. Therefore, the 3-D microstructural are formed relatedly with a density similar as grayscale image however the patterns and it is spacing feature size they required to obtained sub-resolution of the exposure critical dimension by projection optical limitation. The Fig.3.4 is shown the schematic based on the grayscale lithographic diagram process subsequence. Based on this fundamental theoretically of the grayscale mask concepts are designed based on limitation of which the components that obtained of extremely small pattern size. Their pitch and pixels on the mask plate use determine the percentage of the intensity of the light expose pass through the photomask then diffraction output energy portion is effect proportion shaded forms grayscale imaged corresponding with related the patterns density were formed [39]. This photomask plate carried out as percentage per unit area of the pixels and pixel pitch, it can be estimated as the following equation

$$\%T = \left(1 - \frac{A_P}{A_L}\right) \tag{3.1}$$

Where,

A_P is an obstruction pixel

A_L is the gap of that pixel the light can be passing thru its.

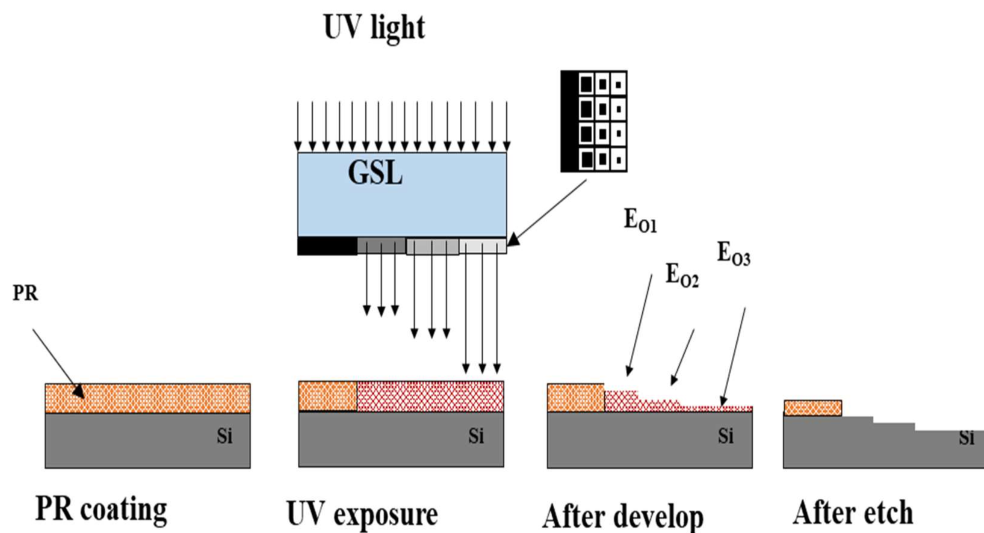


Fig. 3.4 Diagram of 3-D lithography based of grayscale mask.

The grayscale mask is tremendously effective to form a 3-D structure geometry profile but the realistic of the 3-D microstructure that formed on the coated photoresist. Which they are related to the energy light dosage and directly to construct resist thickness height formation and relative to the profile roughness performance outcome. However, the grayscale patterns that design layering on the mask substrate with arranging the pixels and pitches for controlling the intensity of the exposure energy dosage and very unique uses in the lithography process. Therefore, the grayscale patterns are needed its size decidedly to limited lower than sub-resolution of the exposure system and this mask will become overly critical dimensions (CDs) and limited, therefore this mask cost is exceedingly expensive.

3.3.2 Multi-film thickness mask (MFT mask)

This section explains the new concept of the multi-level film thickness mask. In this research study, the development was used this MFT mask to fabricate the staircase contour cavity structure (S-CTC). Which is fabricates on the fixed plate wafer with the capacitive structure for sensing element of the MEMS microphone application. The process flows block diagram based on this photomask design conception as shown in Fig. 3.5 which is the MFT mask is typical optimal the advantage of a grayscale mask (grayscale-mask) and binary intensity mask (BIM-mask). As well as it can be performing at the same utilizing with single-process steps to fabricate the 3-D microstructural pattern and etched. In addition, the 3-D microstructure formed on photoresist is used in single step lithography by electron-beam evaporation method to deposit the transparency thin film, which is chromium stack overlaying on nickel (Cr/Ni) for this process on the MFT mask making processes. However, this was demonstrated that MFT mask designed in which improvement of the adhesion of thin film properties deposited strength in between two-deposited thin film material and it can be generated exposure to form the 3-D patterning step similar to grayscale mask [40].

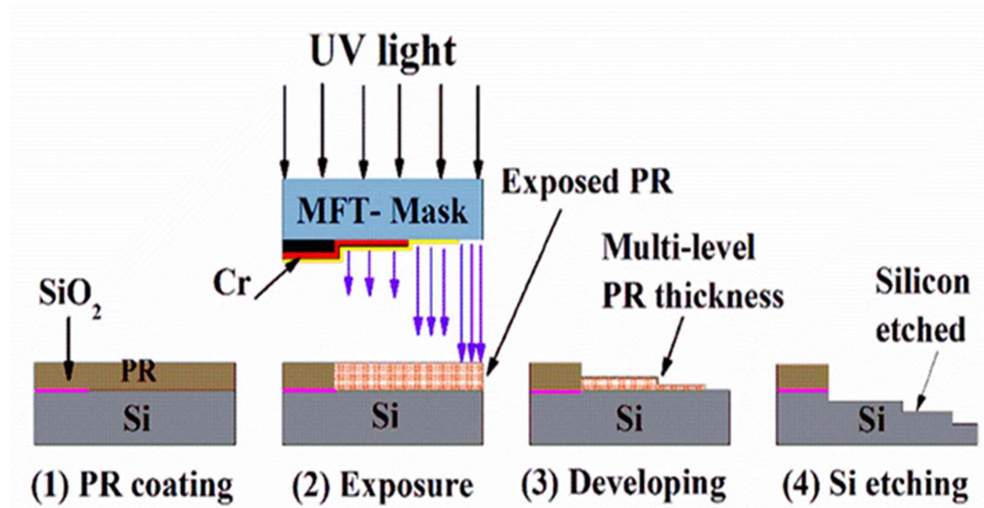


Fig. 3.5 Diagram of 3-D lithography with MFT mask.

3.4 MEMS capacitive microphone structure with 3-D lithography with MFT mask implementation [44].

As mentioned in the research objective chapter 1, a unique capacitive sensor structure was evaluated about the increasing of the capacitance values based on contour cavity between the air gaps. Normally, the fabricating process needed to performed under multi-layer fabrication process. Therefore, the implementing of MFT-mask would be reducing the multi-fabrication process required of the multi-levels of the etching profile to single process step and transferring this to 3-D lithography process with MFT mask making. Mostly, the purpose of developing the sensor device structure is needed to achieve as more significant higher of the final signal to noise ratio (SNR) in a device the silicon microphone.

This proceeds method based on the improvement of the fixed plate capacitance plate area to increase the capacitance values. In this design, the staircase contour cavity with capacitive sensor air gap style is formed to get maximal the changing capacitance value in which consideration the capacitance value during applied incidence load pressure. The MEMS microphone sensor with improving the sensing element will be increased its output performance. As mention in Fig. 2.8 at the previous chapter with the cross-sectional view of the staircase gap in Fig.2.8(b). According to the FEM modeling shows the necessary cavity depth which compensates to each stair should be expected for the fabrication process. In spite of the staircase, the cavity can be fabricated with multiple masking processes such as the convention of process fabrication. However, which the multiple masking processes will substantially increase manufacturing cost and in this way, the design would lose its competitive edge.

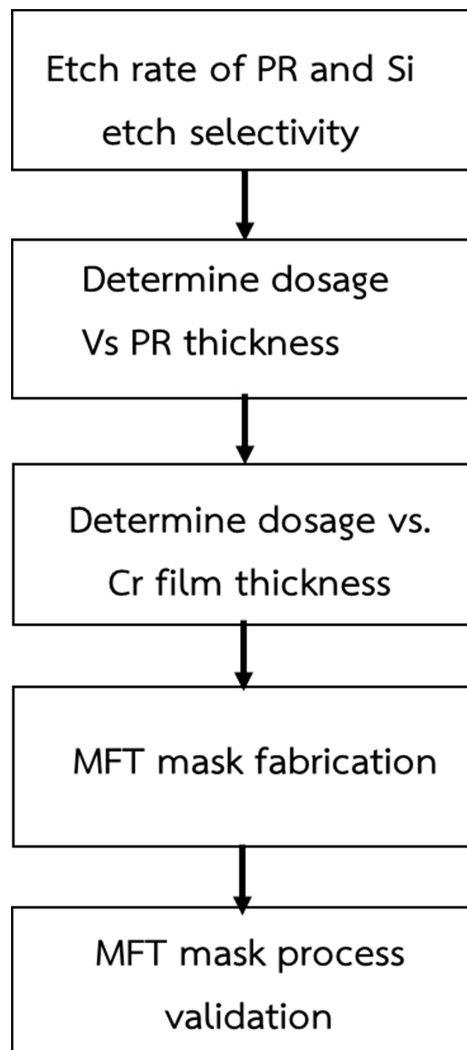


Fig. 3.6 Multi-film thickness development sequence diagram.

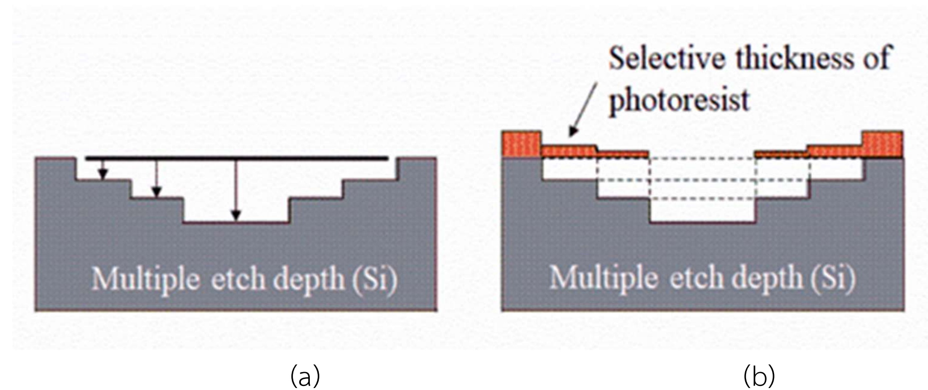
Therefore, the development of using a single mask process using MFT masking is offered an eminently desirable solution. The following block diagram as shown in Fig. 3.6 describes the sequence of developments way that utilizing the staircase air gap structure for capacitive sensor design.

3.4.1 Resist etch rate and silicon etch selectivity

The staircase contour cavity with air gap structure profile is depends upon the etched cavity depth compensated of the different etching depths is required to be perform into the silicon wafer as shown in Fig. 3.7(a). The method of achieving to etch control as a different etched trend of the cavity's depths with a single step etching process as shown in Fig. 3.7(b). In this case, there are targeted at three stairs desired

to form in the silicon substrate. However, this process is needed to find out the etching characteristic with plasma etch profiling that related to material properties as well as for determine to PR with 3-D microstructure profile. Therefore, cavity etched profile at the center portion is obtained the deepest area in the staircase. However, this center point was etched without any coated of photoresist coverage at the silicon surface. Then, the other two stairs areas were etched with as selective etch with the thickness of the photoresist to control delaying over that silicon surface. Therefore, to simultaneously etch all three stairs, this method depends on two key parameters to find out the best merit of processes control capability. There is: (1) the etched rate of silicon and photoresist based on this constant is defined the etching time to completed etching depth of that target on the silicon wafer, (2) etch selectivity of between silicon and the photoresist is determined an available parameter of designed each staircase height.

Base on the previous experiment result of the etched selectivity was verified as 1.3:1 aspect ratio (photoresist: silicon), the etching process was maintained as consistent of etching rate and higher selectivity of the material. Which is maintained getting better uniformity of an etching profile [41]. In the meantime, the etched selective profile and backplate etching profile targeted of this work as shown in Fig.3.7.



(a) (b)

Fig. 3.7 Cross sectional view of staircase and 3-D structure cavity formation.

The resulted in Fig. 3.8 shows the relation of plasma etched performance which rate selectivity of photoresist and silicon, the etching of two materials depends on the fluorocarbon mixture with oxygen (CF_4/O_2) gas flow rate ratio in the plasma vacuum chamber of reactive ion etching (RIE) reactor. When the gas molecular composition was energized by high power with radio frequency (RF) then the ion etching will be performed bombardment to the surface to remove the material by recombined to the volatile in gases state by-product to the exhaust and pumped away by the vacuum. In this mechanism due to the photoresist it material made from

novolak resin base composition comprised of carbon molecular. Therefore, in the RIE system an oxygen gas was used to etch to the resist material. While to fabricating the three-dimensional of S-CTC structure, the etched rate of resist material must be faster than silicon because the needed for improving 3-D sidewall resolutions. Hence, the varying of an oxygen flow rate in the RIE system has to investigated this means that the process chamber of the CF_4/O_2 gas flow ratio of 55/10 and 55/16 SCCM to find out the suitable oxygen flow rate condition. However, the etched uniformity across the wafer has decreased by increasing the oxygen gas flow rate. Therefore, the CF_4/O_2 gas flow ratio of 55/10 SCCM with etch selectivity between resist and silicon of 1.3 represented the most suitable condition [41].

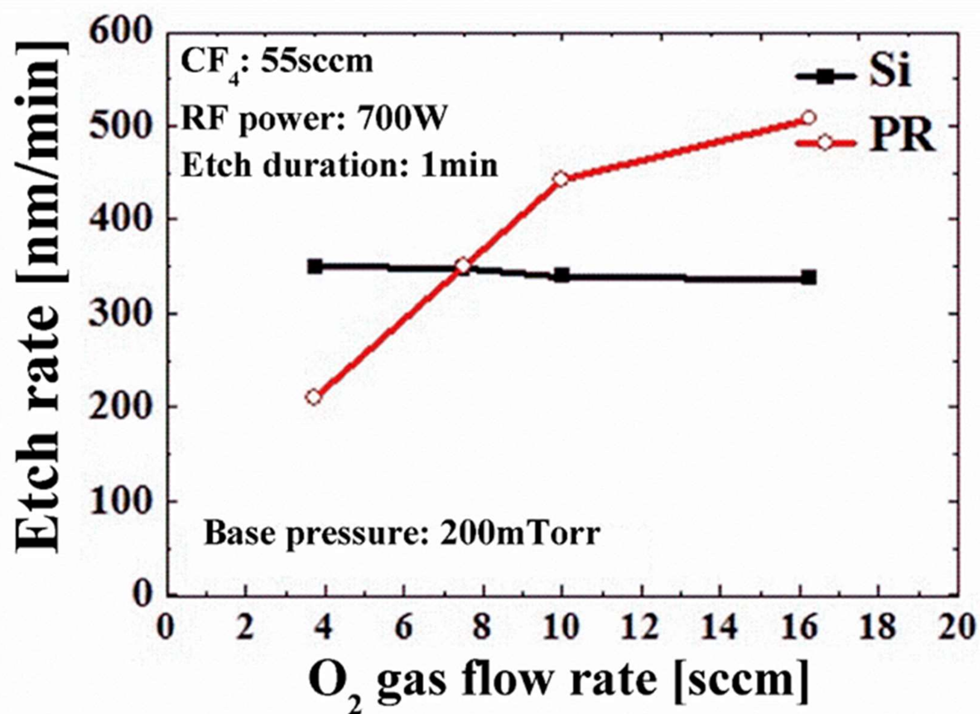


Fig. 3.8 The relation of silicon and photoresist etched rate effected with O_2 gas flow rate in CF_4/O_2 plasma.

3.4.2 Exposed dosage and photoresist thickness

Since we have established above the desired photoresist thickness to formed as the appropriated of staircase depth target with corresponding to resist selectivity and silicon material such as the wafer substrate. However, the etching method is representative to the main key of process factor to formed a there-dimensional structure with lithography process. Therefore, the desired exposure energy dose or lighting dosage to obtained the selective of the photoresist thickness is must proved.

This experiment was performed similar same as the conventional lithography process, except there is adding the arranging of the exposure dose that related to a certainly resist coating thickness. This method is performed by varying exposure energy from zero energy doses into the coated PR until the energy dose has completed developing the remained coated PR. Thus, the relationship of energy doses versus the remained PR thickness after the development process is determined as shown in Fig. 3.9. Based on the resulted show that remaining resist is partially removed and related to input energy dose. In this empirical result was found that the use of energy dosage that completed developing the coated PR of 5μm which using exposed energy at 210 mJ/cm2 as approximately. Therefore, the remained PR that leftover on the silicon substrate will be arranged to form the 3-D lithography desirable window for etching certainly to the depth profile and deploys for the staircase contour cavity then fabricate onto the silicon substrate.

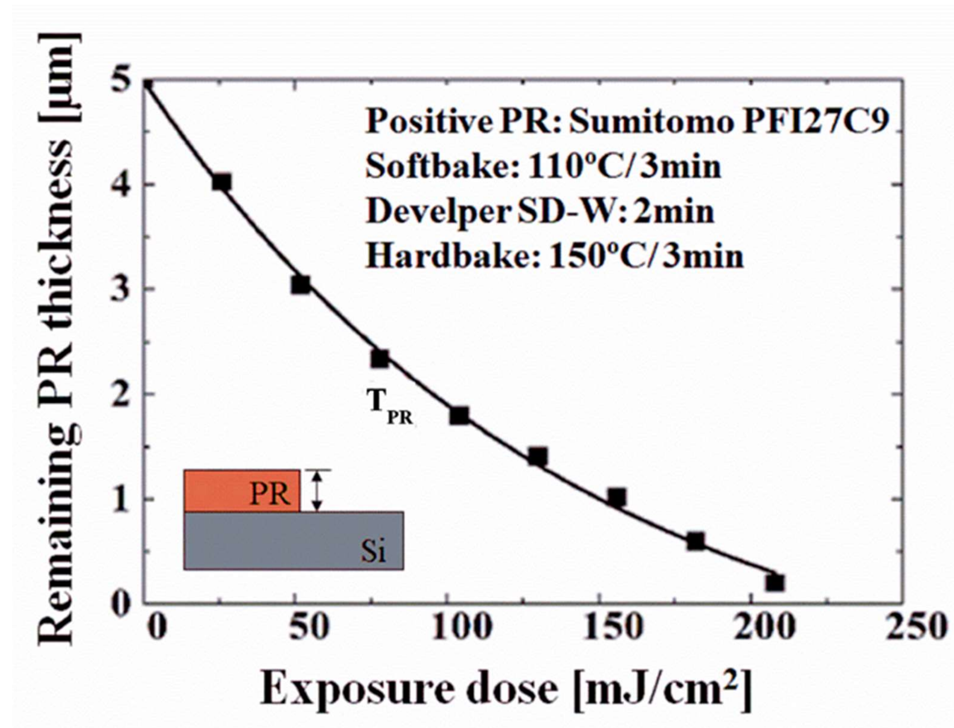


Fig. 3.9 The relative of resist developed thickness and exposure dose.

3.4.3 Exposed dosage and chromium film relation

Furthermore, as the previous section describes how to determine the correlation of an exposes energy that related to form multi-level of resist as defined to etch selectivity and etching rate that was performed by RIE system. This information is considered to optima the processing technique to achieved as single run on the

lithography process by transfers to the MFT mask designed to establish the method of the controlling energy dosage output through a chrome mask. However, the key idea behind the MFT mask, which there the thickness of the transparency chromium material and it can be control in the light intensity passing thru its. However, the exposed energy goes through this varied transparency film then changes in the intensity level output and the energy output through chrome film is governed by

$$I_x = I_0 e^{-\left(\frac{\mu}{\rho}\right)\rho} \tag{3.2}$$

Where

I_x is the transmitted moderate Light intensity through a medium

I_0 is the intensity of the light incident on the medium

μ is the coefficient of the light intensity absorption

ρ is medium density and x is the thickness of the medium.

The amount of light energy going through the chrome film was measured by Light transmission spectrometer (LTS) which the measurement wavelength (λ) was calibrated and sweep the measuring wavelength from 350 to 800nm for this experimenting procedure. The empirical result was found that the percentage of light transmission is relative to chromium thin film transparency in the range of nanometer. Then, extrapolation for the predicted of an exposes energy dose in milli-joules per square centimeter. Therefore, we can determine the relation of exposed energy that will be formed to photoresist and defined the correlation plotted as shown in Fig. 3.10. Thus, based on this information we can be considering which the desirable of chromium film thickness to deposit onto a newly MFT mask.

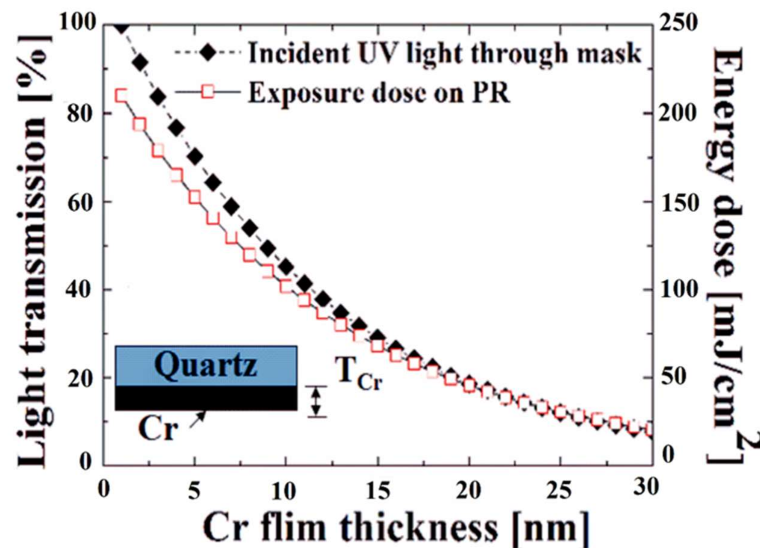
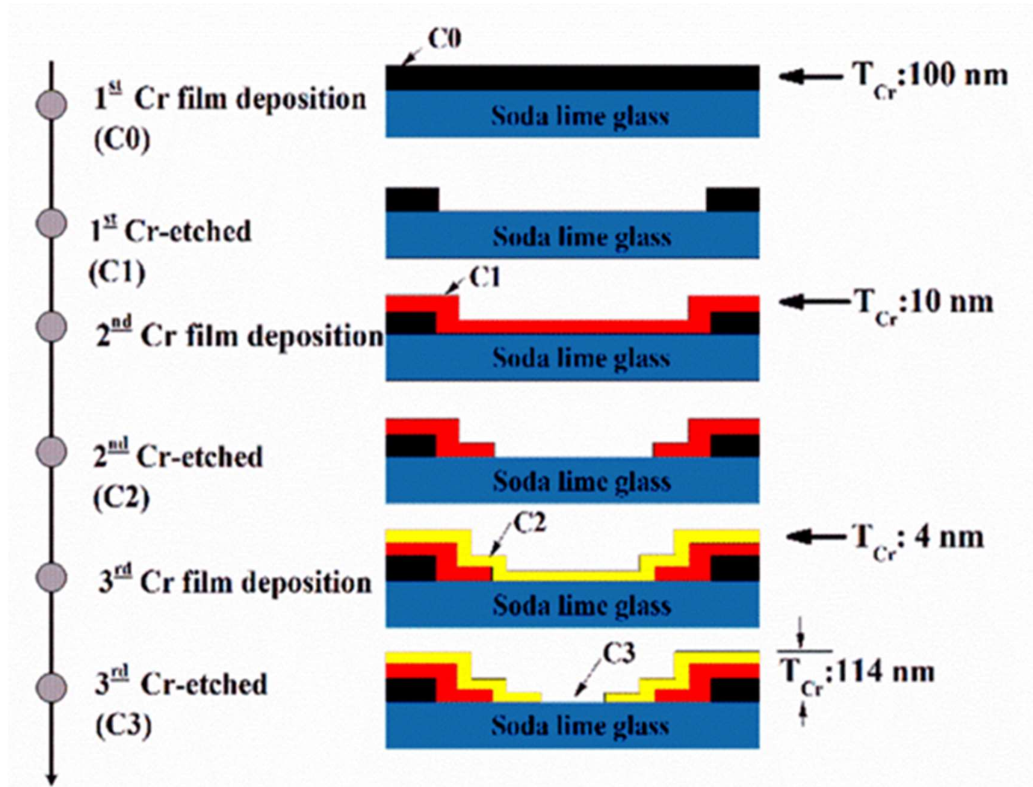


Fig. 3.10 Light transmission thru various Cr film thickness.

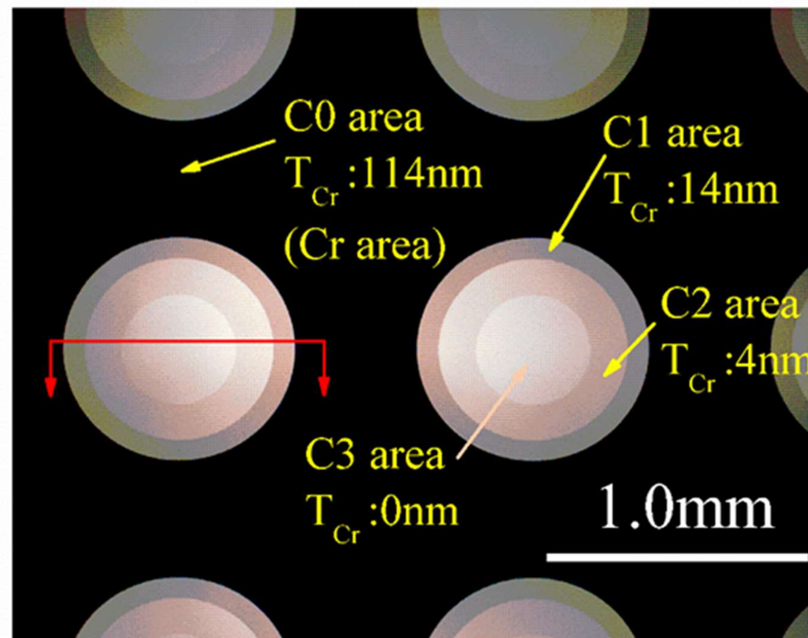
3.4.4 Chromium multi film thickness mask (MFT) fabrication

The capacitive MEMS sensor in this experiment was designed with the new specified of S-CTC structure that purposed to replace to current MEMS microphone structure with BOX cavity. Which is corresponding to the used of polysilicon membrane deflects characteristic properties. Therefore, the S-CTC with three-step of a staircase desired to compensates of an ideal case contour profile and silicon etching at a back plate wafer.

In this research is developed the MFT mask to reduce a multi-masking that proposed reduces the processing cycle to be a single process cycle time for contour cavity etch. The schematic flow diagram of MFT mask making process as shown in Fig. 3.11 then the MFT mask was fabricated and the process sequence details for fabricate of the MFT fabrication shown in fig 3.11 (a). However, this MFT mask making process is similar to a standard conventional of lithography process but coupled with additive and subtractive processes an area of contour cavity is needed. The process of mask making is included as starts with a raw material of 7X7 inches of binary intensity mask with an initial chrome thickness of 100 nm. Initially, the photoresist Shipley S1805 is spin-coated with mechanical chuck holder plate of the spinner and the mask substrate is baked at 100 °C for 90 seconds. At that time a circular-pattern (C1) is patterned with a Heidelberg direct laser. The pattern is written with a 120mW/cm2 power intensity (λ: 436 nm, g-line) and developed in the shipley MF-26A for 1 minute. The substrate is then post-baked at 120 °C for 90 seconds in the hot plate, the chrome is fully etched away inside a circular-pattern (C1). A chrome is etched using a CEP-200 from Micro-chrome-technology etchant. Then the residual resists with PR were stripped. Used removal chemical of a mixture of 70% concentration Sulfuric Acid (H_2SO_4) and 30% hydrogen peroxide (H_2O_2) with the concentration ratio of 4 to 1. This process performs at the settle temperature of 120°C for 10 minutes. At long last, the mask is rinsed with deionized water (DIW) for 10 minutes. At that moment another layer of chrome is deposited over the mask and a second circular (C2) is formed employing similar above-mentioned procedures except for varied time for chrome etching time. The third circular (C3) followed the identical procedure as C2. After that and Fig. 3.11(b) indicates the top-view of the mask. The thickness of the chrome film layers deposited directly corresponds to the chrome thickness, needed to produce the exact amount of exposure energy output needed to pattern and develop. The underlying photoresist used as a masking material to etch the desired staircase depth.



(a)



(b)

Fig. 3.11 Sequence of Multi-film thickness fabrication process flow diagram (a) MFT-mask masking short-process flow diagram (b) Multi-film thickness mask captured image.

3.4.5 MFT mask process validation

As a result, the positive resist lays under the Cr film receiving various energy dosages governed by the chromium film thickness as shown in equation (3.2). After the development of the photoresist, a three-dimensional with vertical sidewall slope profile with the varying of resist thickness is acquired. This 3-D photoresist structural profile goes beneath the silicon substrate via a particular step dry etching process. Finally, a staircase style cavity is formed where the etched depth in the silicon substrate varied as per the initial thickness of the photoresist layer.

The sequent to fabricate the fixed plate is included. First, a 5 μm-thick positive PR (Sumitomo PFI-27C9) was coated on a 6-inch silicon wafer and baked at 110 °C for 3 min. The wafer was then exposed with a UV exposure dose (λ: 365 nm, i-line). The exposure energy was varied from 80 to 240 mJ/cm^2 with a step increment of 20 mJ/cm^2. After exposure, the wafer was developed using a Sumitomo developer SD-W for 2 minutes and afterward hard baked at 150 °C for 3 minutes. Ultimately, the remaining PR film thickness was measured by using a step profilometer (TENCOR P-10). Fig. 3.12 shows the resulting PR film thickness in the wafer modulated by both the exposure dose and the Cr film thickness.

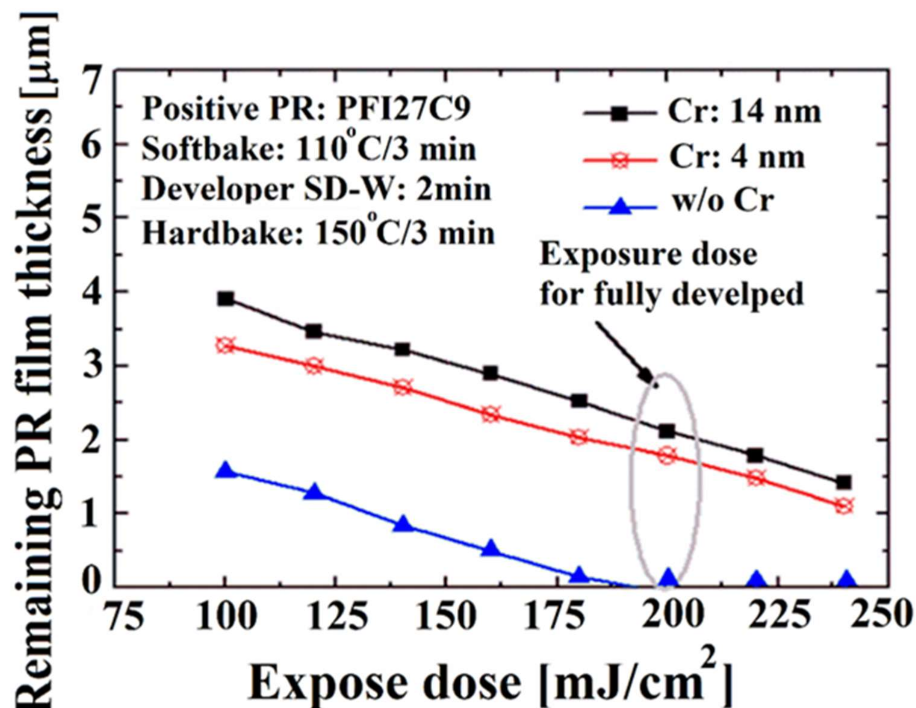


Fig. 3.12 The relation of the varying chromium film on MFT mask formed to PR film by varied exposure dose.

Based on the result it is obtained that the exposure dose of 200 mJ/cm^2 is needed for properly patterning staircase gap. At exposing energy of 200mJ/cm^2, C3 is completely developed while C1 (Cr: 14nm) and C2 (Cr: 4nm) are partially developed and the desired thickness of the photoresist is left behind. The remainder photoresist thicknesses are 1.6 microns and 2.21 microns respectively. This indicates that when the Cr film thickness was varied at 0, 4, 14 and 114 nm. Therefore, the percentage of light spreading through the MFT mask was exposed with 100%, 70%, 30%, and 0% respectively. Therefore, an MFT mask with three various steps of Cr film thickness can produce an S-CTC structure for Si microphone device. Fig. 3.13 shows a cross-sectional view of 3-D microstructure patterning using an MFT mask. Based on this concept, a proof experiment was carried out to the microphone product. The information below shows the details and outcome of the determination experiment to form a fixed plate chamber.

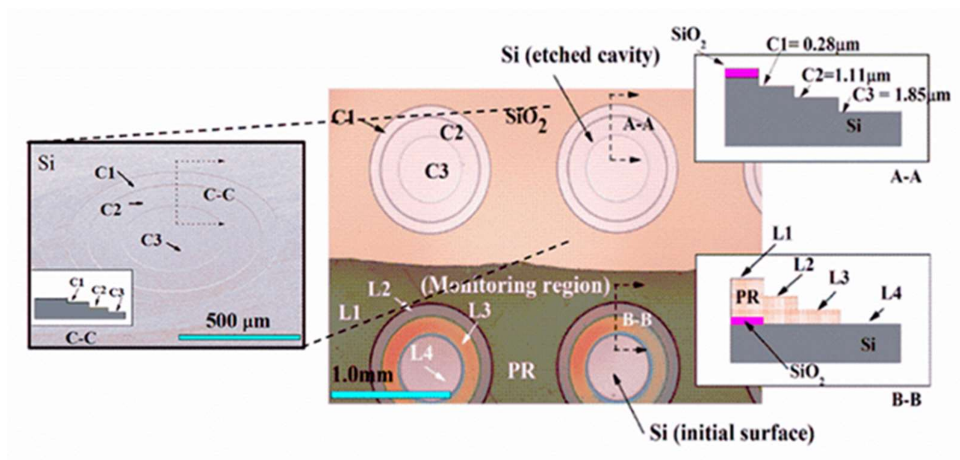


Fig. 3.13 The photograph of S-CTC structure fabricated on Fixed plate by single process etching of lithography process by MFT mask.

Chapter 4
MEMS CAPACITIVE SENSOR FABRICATION

The fabrication process of the MEMS capacitive sensor for silicon microphone is presented. In this chapter is divided into three segments and the MEMS device was fabricated at Thai microelectronics center (TMEC). The microphone sensor is based fundamental of the capacitance parallel plate theory was modeling and designed for fabrication. In previous studied, the ways to be reached to increased the capacitance sensor output based on limitation with small plate area the capacitor and gap of the plates. The sensing membrane size and rigidly fixed plate are needed to maximize as a concerned parameter is required. Therefore, extend cavities with staircase contour structure has desired to fabricate purposed to achieving improvements to more efficiency for the microphone sensor. Fig. 4.1 showed the cross-sectional MEMS capacitive sensor device based on introduced of S-CTC fabricated at the cover plate.

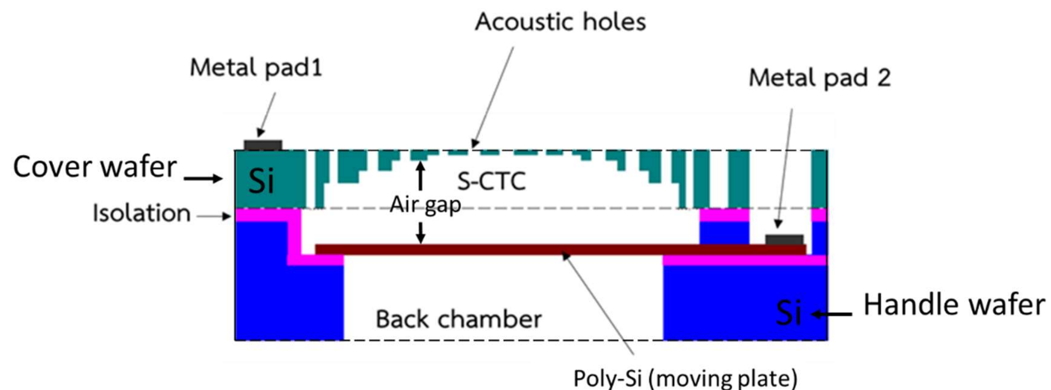


Fig. 4.1 The cross-sectional view of MEMS silicon microphone capacitive.

However, this chapter consists of four sections to describe there are: First, describes the process description the fabrication process of the moving plate by which a polysilicon was formed for the sensing membrane purpose detecting the sound pressure (handle wafer). Second, describes the fabrication process of the back plate plate (cover wafer) in which adding of the staircase contour cavity shaped structural fabricated to the plate, in this part the 3-D lithography process integration will be carried on by using MFT mask is performed. The third section is describing the device fabrication during the wafer has fusion bonding the bonding surface preparation will be described. The fourth described the back-end process for final process fabricated state to completed wafer fabrication of the capacitive sensor devices for MEMS

microphone packaging level. The whole process sequence of the main block diagram as shown in Fig. 4.2.

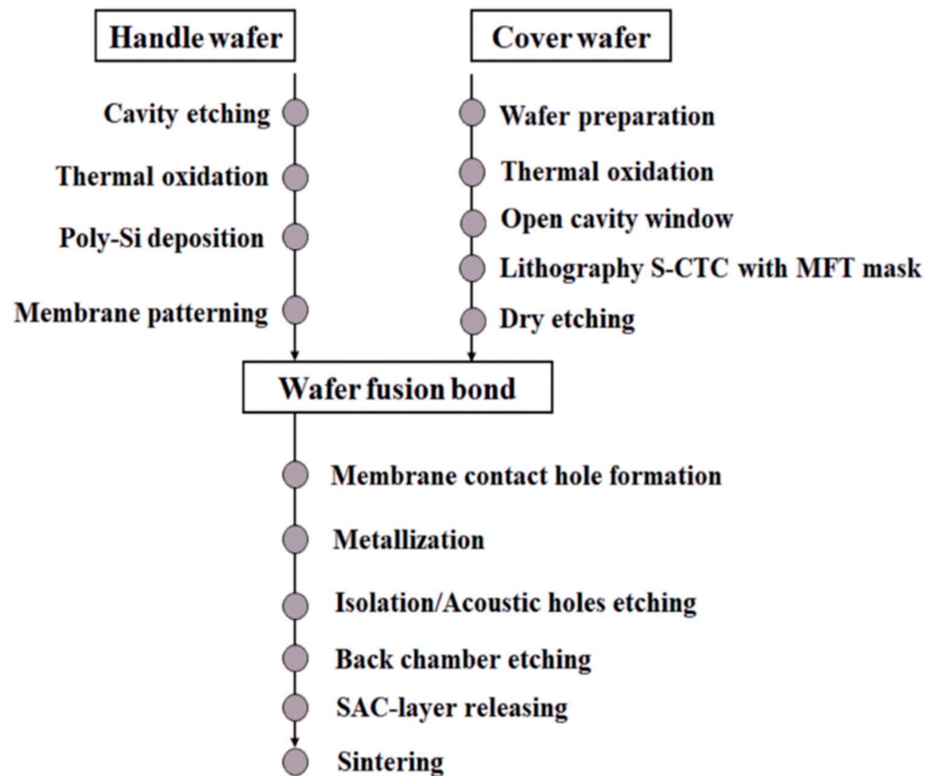


Fig. 4.2 Process flow diagram of silicon capacitive MEMS sensor.

4.1 Fabricating of diaphragm moving plate wafer (MP)

The process fabricates of the moving plate which this sensor membrane starting with silicon wafers N-type with 400μm thick (orientation: 100). The fabricating of handle wafer with double side polishing (DSP) is chosen in the work. Polycrystalline or polysilicon material is required to form the membrane (diaphragm). Consequently, the fabricated of a diaphragm wafer. As first begins the wafer was performed as an initial surface cleaning with RCA wet-cleaning method then a shallow cavity with 2.8 μm, it was etched onto the silicon substrate. Followed by growth silicon-dioxide of 2 μm with wet-oxidation process with based process condition of gas flow rate as aspect ratio of the hydrogen and oxygen rated (H_2: O_2; 8.5: 5) SLPM processes in the furnace column. Next, the desirable a 0.8μm thickness of polysilicon (Poly-Si) by in-situ doped method with the phosphine gas based (P_2H_4) to obtained of very low resistivity of the polysilicon for conducting plate for capacitance plate requirement. Whereas the amorphous silicon was deposited by using the Low-pressure Chemical Vapor

Deposition (LPCVD) process at 650 °C deposition temperature is required. Furthermore, a polysilicon thin film was patterned and etched for fabricating a membrane. Therefore, this thin film polysilicon was lying at inside shallow cavities as shown in the process block flow diagram in Fig. 4.3

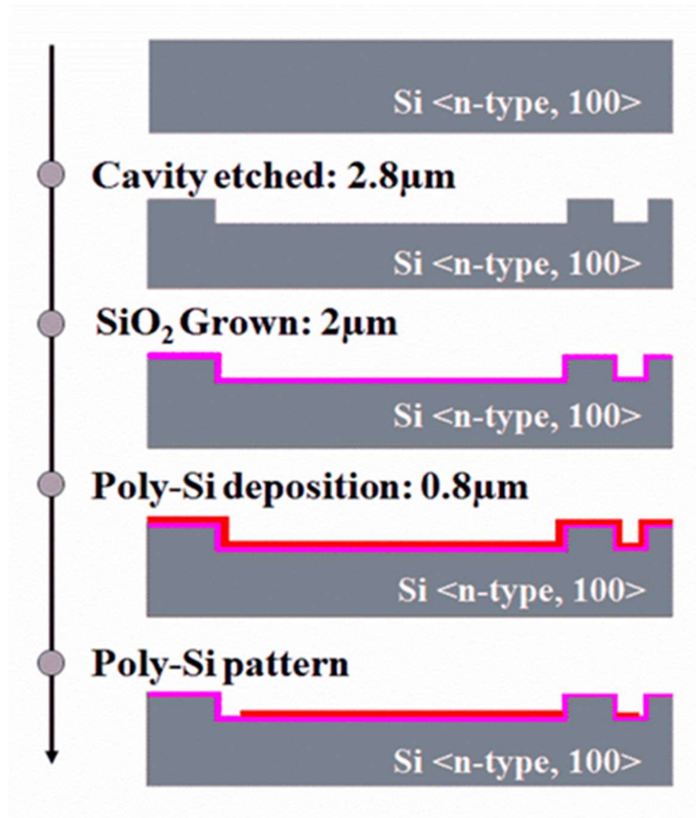


Fig. 4.3 Diaphragm wafer fabrication process flow block diagram.

This MEMS capacitive sensor structural fabrication method is required two wafers for processing fabricated sequent of the devices. Due to the PLCVD of polysilicon thin film is needed to form pattern and etching processes to fabricate a moving plate for a membrane. It seems to be that surface area of the bonding must expose to the etching condition and it causes to become rough of the surface profile as well influenced to the etched method. However, the etching method most common provides to dispose of selective material. Plasma etching with reactive ion etching (RIE) system, the major defect by product issued with an ion accelerated bombardment to wafer substrate has induced some damage rough-surface. The contaminants of organic material such as photoresist residual, nevertheless, keep on going imprint effects to the substrate surface. The roughness was generated by plasma etching processes, in the range of several tens of nanometer root mean square [42]. This is the primary issued for permanence fusion bonding surface. As the well known

the performance of wafer fusion bonding strength depend on the quality of the surface roughness with mounts both wafers as permanently. The surface roughness should be maintained at few nanometers this is required for the wafer direct fusion bonding process. Hence, the polysilicon Wet-process etching was chosen to consider used at this process sequence. The recommendations for utilizing a direct wafer bonding step: (1) ensure a particle-free bonding surface, that is, a clean environment. That is absolutely necessary for good bonding yield. (2) Protect the bonding surface during all fabrication step prior to direct wafer bonding. Any exposed of the bonding area to plasma or liquid etchants must be avoid.

4.1.1 Poly wet-etchant development

The fusion bonding technique is well adopted in fabricating the MEMS devices. However, the properly utilizing of wafer fusion bonding led to deployed uses as an ultra-polished of the surface for good quality to rely on surface energy. The morphology of an intermediate layer adhesion relies on the cohesive bond that is formed when the polished surfaces of two wafers are mated. According to etch the polysilicon as a membrane for MEMS microphone application this is perhaps due to the polysilicon being rough surface and difficult to bond directly. Unless the surface planarization by using correctly chemical-mechanical polishing to produce surface roughness scale at below 5.0 nanometers [43]. Therefore, wet chemistry etchant deploys use on this process for improve from the bonding surface. However, wet etchant chemistry roughens on the oxide surface in this studied was investigated which significant problem when the wafer is fabricated such which dry-etching has accommodated remained of slight imprinted residual defects on a substrate surface. In the other hand, wet-etchant chemical based of ammonium fluoride (NH_4F) in nitric acid (HNO_3): deionized water (DIW). According to the chemistry as the original concentration of Ammonium fluoride mixture formula was attacked to the PR masking layer. Therefore, in this work the etched rate and etch selectivity of polysilicon and silicon dioxide (SiO_2) were studied to find out the optimal suitable wet etchant to approach the final ultra-fine surface roughness profiling of each both material.

4.1.2 Polysilicon design of experimentation

Initially, we typically choose a polysilicon wet chemical that capable validity of room temperature formula. Therefore, HNO_3 (70%): NH_4F (40%): HO_2, chemical concentration in common used is 126:5:60 for single-crystal silicon and same etchant [52]. Base on the initially result which nominal chemistry was an extraordinary attack to the resist layer and the polysilicon was very high variation undercut greater than 12 microns of the critical dimension. Later, that chemistry was diluted by increasing

amount of DI water with changed from 60mL to 80 mL the polysilicon etched quality far better than original chemistry provided. n addition, for this experiment, there is perform varying a concentrations buffer agent based on ammonium fluoride form 1 to 5mL for unique solutions. However, the comparisons result in Table 4.1 which is to define an optimal of wet-etchant concentration mixing recipe for support on this practical purpose. In this experimental procedure was typically obtained as properly considered based on the polysilicon material is represented as buried oxide inside the shallow cavity. Whereas to find out the solution that preventing to damage of the substrate surface in which directly to bonding of oxide. Therefore, the masking layer with photoresist as before and after the process was prepared test samples.

Table 4.1 Polysilicon wet etchant recipe design of experiment.

Recipe_1 HNO_3: DIW: NH_4F (150:80:5)				HNO_3: DIW: NH_4F (126:60:5), Original		
NH_4F (x)	initial oxide 1064 (A)			NH_4F (x)	initial oxide 1064 (A)	
	Oxide etched/min (A)				Oxide etched/min (A)	
1	23.2			1.0	26.6	
2	37.2			2.0	47.0	
3	51.4			3.0	65.2	
4	63.0			4.0	74.4	
5	106.4			5.0	106.9	
Poly-Si : 6884 (A)				Poly-Si : 6884 (A)		
NH_4F	Poly etched /min (A)	selectivity		NH_4F	Poly etched/min (A)	selectivity
1	387.7	16.7		1.0	477.7	17.9
2	838.0	22.5		2.0	965.3	20.5
3	1415.3	27.5		3.0	1432.3	22.0
4	1846.7	29.3		4.0	0.0	*
5	*	*		5.0	0.0	*

Furthermore, to adequately investigate the etched rate and etch selectivity of polysilicon PLCVD film, in this study the silicon wafer with 2.0 μm of thermal oxidation thick was growth. Then, 0.6 μm thick in-situ polysilicon was deposited on silicon dioxide layer. Later, the consistent polysilicon pattern was etched by reactive ion etching to typically form the etch opening area. The wet chemistry of nitric acid (70%): water-deionized: ammonium fluoride (40%) mixtures with an arbitrary ratio of 126:60:x and 150:80:x by volume was handled to etch polysilicon for 3 minutes at room temperature. Based on Isotropic-etch curve of silicon, the ammonium fluoride volume was typically varied from 1.0 mL to 5.0 mL to optimize the etched selectivity between polysilicon and silicon dioxide. After photoresist was stripped, the remained

film thickness was reliably measured by ellipsometer [45], and the surface roughness was measured by an atomic force microscope (AFM) [46]. Based on this practical experiment, the initial thickness of test samples with polysilicon and Silicon dioxide film was 6884 ± 75 A° and 1064 ± 5 A°, respectively. The polysilicon film was completely etched within 3 minutes for both chemical mixtures with 126:60:5 and 150:8:5 volume ratios. Fig. 4.4 is shown that the chemical mixtures of 150:80:x volume. The used ratio is moderately suitable than the chemical mixtures of 126:60:x volume ratio due to its higher etching rate and etch selectivity. By varying the used volume of nitric acid from 150:80:1 to 150:80:4 mL, the polysilicon etched rated has proportionally increased from 388 to 1847 A°/min. The etch selectivity between polysilicon, and Silicon dioxide has increased from 16.7 to 29.3 compares to the nominal chemistry with was obtained etch selectivity of 17.9 to 22.2, respectively.

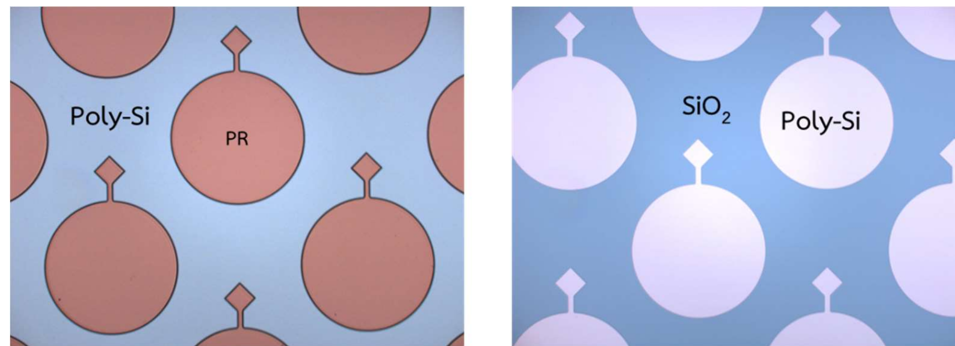


Fig. 4.4 Samples preparation of membrane patterns and SiO_2 bonding surface.

Fig. 4.5 typically showed that the root means square of oxide layer etched by the polysilicon etchant with 150:80:4 considerable volumes. When considering as the ratios for 3 minutes after has completely eliminated a polysilicon layer from the surface was 2.89 nm lower than 126:60:4 with 0.36 nm, which was typically almost three times the roughness of as-deposited oxide layer. It was gently suggested that polysilicon etchant with 150:80:4 precious volumes. Therefore, the ratio was suitable to suppress the oxide roughness due to higher etch selectivity and used implementing this process sequence.

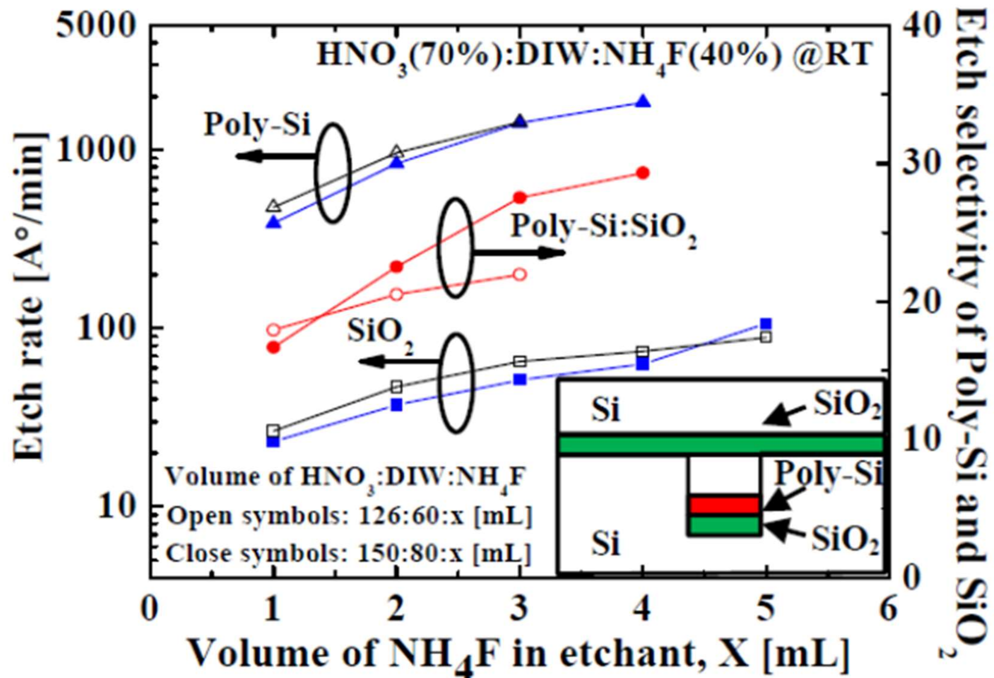


Fig. 4.5 Effects of volume of Ammonium fluoride in HNO_3: DIW: NH_4F mixture to the etch rate and etch selectivity of polysilicon and Silicon dioxide.

4.1.3 Surface roughness metrology

After the test samples have been done with an experiment related polysilicon etch with the wet chemistry etchant has been solved. later that the atomic force microscope (AFM) is used to correctly for analyzing the effected bonding surface and to validating of polysilicon wet etch solution. In addition, see more detail of samples preparation in which some sample of when it to the wet-etchant solution. In this case, the wet-etchant of HNO_3: DIW: NH_4F (150:80:4) mixture ratio was used. Table 4.2 summaries of the polysilicon wet etchant which two conditions optimal diluted concentration comparing with to nominal chemistry wet-etchant of HNO_3: DIW: NH4F (126:60:5). Which the mixture of wet-etchant of HNO_3: DIW: NH_4F (150:80:4) is comparable to the mixture HNO_3: DIW: NH_4F (126:60:3). However, this slightly smoother surface roughness of 0.21 nanometer and etch selectivity acquired of 27.5.

Table 4.2 The summary of polysilicon wet-etchant modification.

Criteria HNO3LDIW:NH4F	Oxide Etch rate (A)	Poly-Si etch rate (A)	Etch selectivity	Surface roughness (nm)
Bare silicon	n/a	n/a	*	0.13
Initial oxide	n/a	n./a	‘	0.38
126:60:5	93.1	*	‘	0.85
126:60:3	65.2	1432.3	22.2	0.29
150:80:4	51.4	1415.3	27.5	0.21

* over etched, ‘ no data

4.2 Fabricating of back plate (BP) wafer [44]

The back plate is one a rigidly fixed plate for silicon capacitive microphone structure as shown the process block diagram in Fig 4.6. The fabricates a BP wafer is begun with a thermal oxidation process as an initial sacrificial growth layer for protecting the surface inborn quality. Next, the gap desired area was patterned open a polysilicon etched. Which was located at the 6-inch silicon wafer, and oxide was etched away inside an area of cavity pattern for etching the S-CTC structure. However, in this process sequence in lithography process the resist coated is need to control of the uniformity of the PR thickness that providing specified etch selective factor to the silicon rate profile.

The MFT-mask process was carried out to proceed in the lithography process to formed 3-D microstructure on the photoresist. This step is performed with a single exposure by using the aligner EVG-620 with i-line wavelength (365nm) of ultraviolet light. The multi-level of remained PR represented S-CTC contour cavity. In addition, the process detail of lithography process had been done with an exposure dose of 200 mJ/cm^2 was used. Later on, the photoresist was developed. The remaining PR film thickness was measured with 9 points by using step profilometer [47]. It was that the remaining film thickness at L1. Then, developed the PR and hard-baked at 150 °C for 3 minutes. The result of the stayed to resist were acquired of 5.0 ± 0.10, 2.7 ± 0.06, and 1.8 ± 0.06 μm respectively. Next, the patterns were transferred to the silicon substrate underneath the photoresist by etching in reactive ion etcher (RIE) AMAT P5000. The oxygen gas flow ratio 55/10 and the chamber base pressure 200 mTorr, Energy power was 700 W and the etching time 4.5 minutes. Then after, the wafer with the remainder PR film was stripped by oxygen plasma asher.

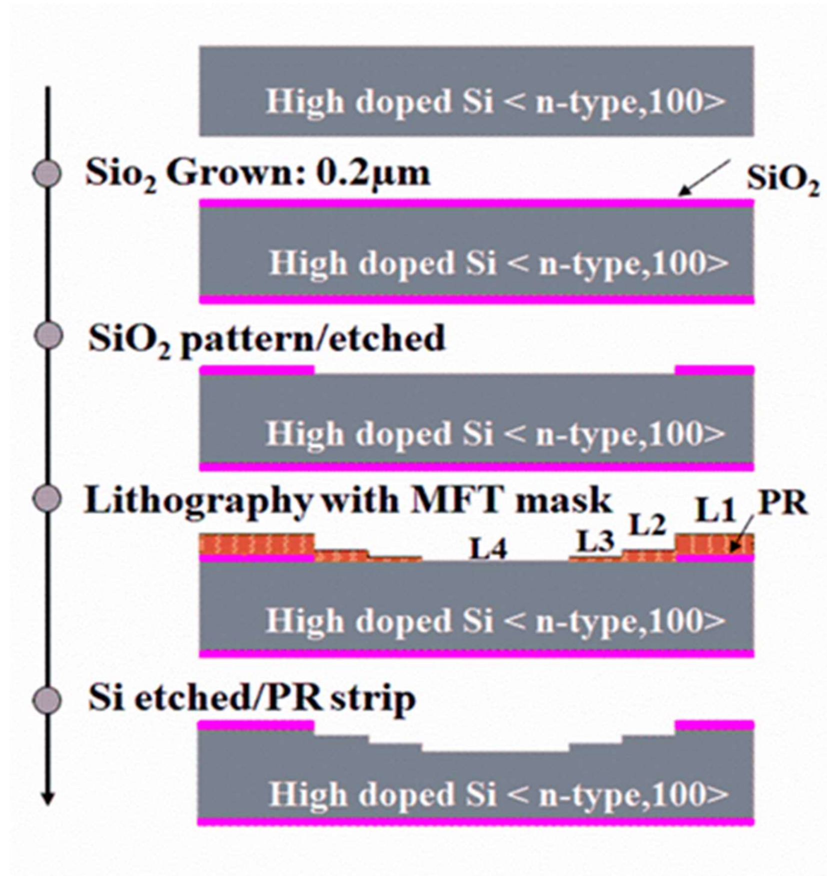


Fig. 4.6 Fixed plate fabrication process block flow diagram of S-CTC etched cavity.

4.3 Silicon microphone device fabrication

This section is typically describing of the process fabrication when both wafers BP and MP were completed of the process fabricate step as described in the previous sections. However, both wafers are needed to very surface cleanliness and particle-free of dust. A capacitive sensor based parallel plate type is desired which two wafers process fabrication. The typically performed the fusion bonding process is directly concerned about the bonding surface quality. However, this specific technique typically obtains the unique need to properly treat with high-temperature annealing to achieve of the high-strength property for permanence wafers bonded.

4.3.1 Wafer fusion bonding process

As well known, the fusion bonding process is comprised basic process as shown in Fig. 4.7. When both wafers are sufficiently completed cleaning steps, then after plasma activation at each the wafer surface to cooperate with approached high surface energy [48] was typically performed. The wafer with the pre-bonding process this work used alignment bonder that required to corrected alignment keys for both wafers. Later that, the entire wafer pre-bond surface was monitored by utilizing the

infrared camera. However, high-temperature annealing is helpfully for the permanence bonded. The plasma activation was performed properly to improve the hydrophilic property of the bonding surface. After that the pre-bonding process of two wafers and high-temperature desired annealing at 900 °C/30 minutes with nitrogen gas was performed. In addition, this process sequence steps the polysilicon material properties is needed to adjust to modification of the film mechanical stress and sheet resistance as well as conductivity of the capacitive plate and moving the membrane [49].

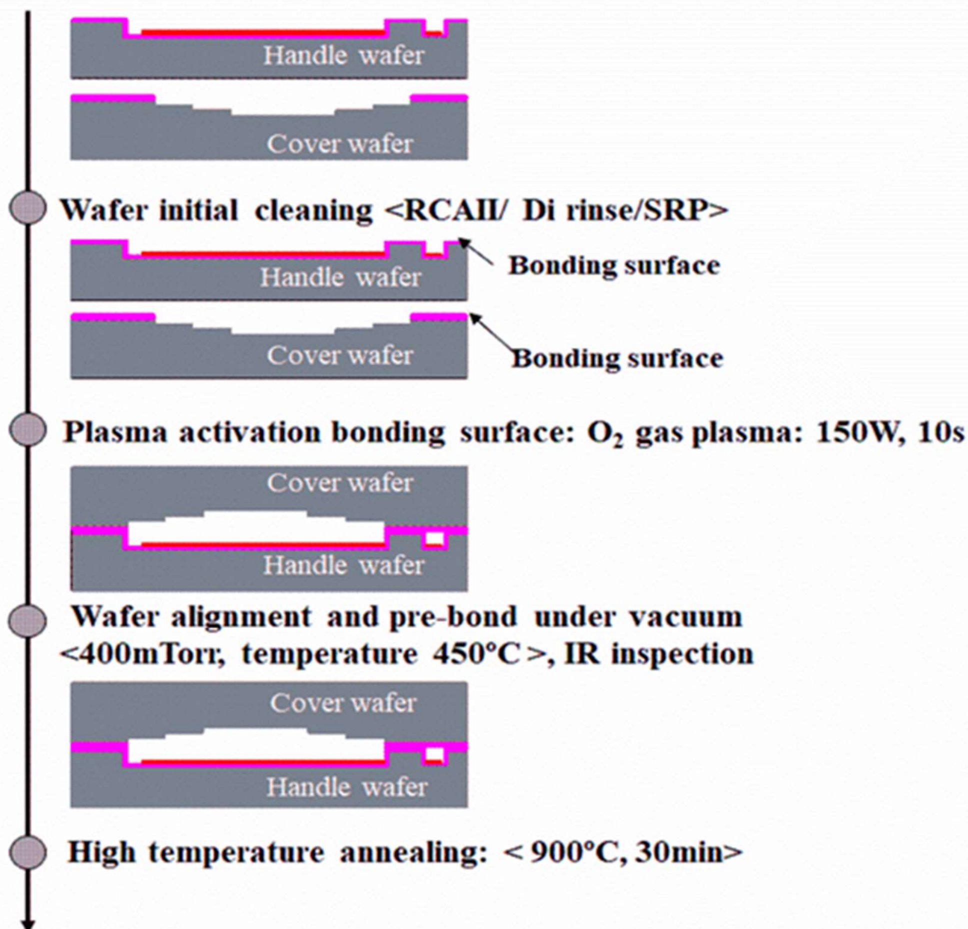


Fig. 4.7 Process block diagram of wafer fusion bonding.

4.3.2 Back-end process of MEMS microphone sensor process

The back-end process was faithfully performed with capacitive S-CTC structure as shown in Fig. 4.8. The processes flow diagram is properly included with the cover plate of the bonded wafers were grinded and to reduce the wafer thickness down to target with 15 ±5µm. Next sequent, the following process is included: open contact window to a polysilicon pad for membrane interconnection, sputtering of aluminum metal (AL) for the metal pad to the sensor of the capacitance plate. Next, perforation

acoustic holes etching for improving acoustic properties [50,51]. Etch the back chamber located at underneath the substrate then remove the sacrificial thermal (SAC) oxide layer to release the polysilicon membrane to free-moving from the rigid body. Finally, aluminum sintering process was done at 430 °C for 30 minutes. The final MEMS microphone based capacitive structure was successfully fabricated as shown in Fig. 4.9.

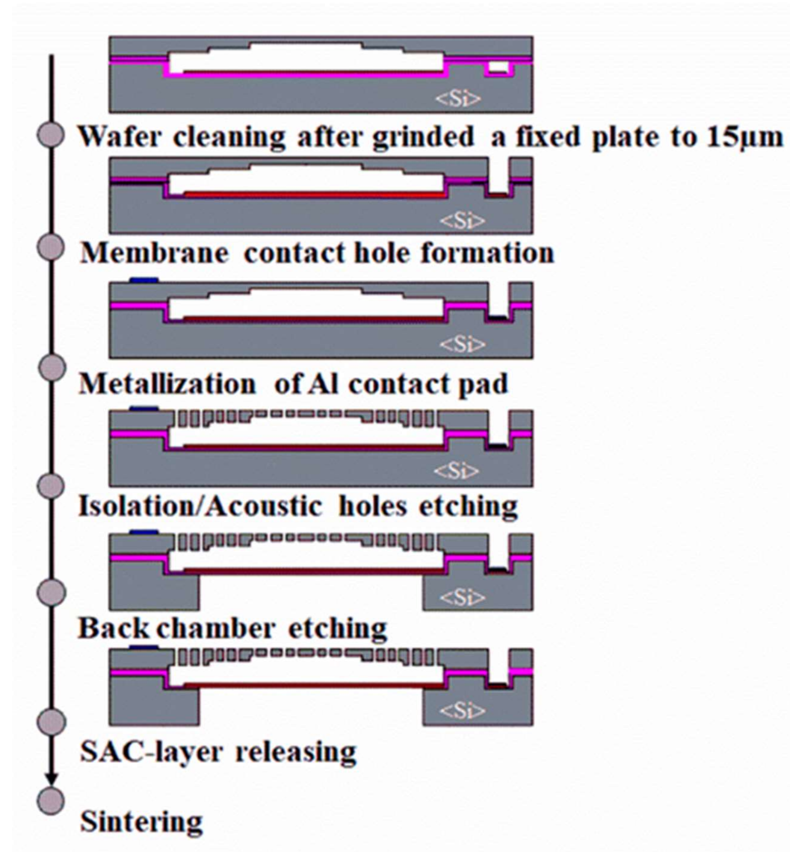


Fig. 4.8 MEMS capacitive back-end process flow diagram.

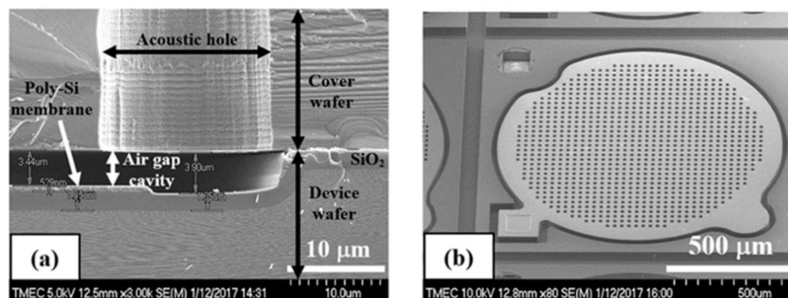


Fig. 4.9 FE-SEM image of completed MEMS based capacitive microphone sensor (a) SEM with cross-sectional image view, (b) Device perspective picture.

Charter 5
RESULT AND DISCUSSION

The key results of this work were given with the implement of 3-D lithography process by using MFT mask to fabricate the capacitive microphone structure. Therefore, the fixed plate with contour cavity structure is developed and described in chapter 2, chapter 3, and chapter 4 respectively. First, the capacitive microphone with fixed plate structure is designed relevantly of staircase contour structure is described. Second, in chapter 3, the processing technique integrated of a new method of 3-D lithography process which applied to the MFT mask constructs 3-D with staircase profile was fabricated. Third in chapter 4, to describe to MEMS capacitive silicon microphone fabricate process and device electrical characteristic of the MEMS microphone capacitive structure is investigated in this chapter.

5.1 MEMS microphone capacitive structure design discussion

The S-CTC of the fixed plate is an air gap structure profile that corresponded with membrane deflection as shown in Fig. 5.1. In order to design the capacitive sensor with an S-CTC structure. The distance between the plates and the maximum of an air gap distance needs to be decided to optimal. The finite element model (FEM) is used to govern the air gap then the membrane deflects is calculated with simulation software when applied with maximum pressure. However, based on this work targeted of maximum acoustic overload at 123 dB-SPL (28.3 Pa) and with 130 dB-SPL (63 Pa) of the sound pressure maximum level was equivalence. Table 5.2 is the calculation resulted that extracted from membrane simulation deflected model with a varied polysilicon membrane thickness of 0.5 to 1.0μm.

At the state of the art, the microphone capacitive structure designing is considered with the maximum gap of two plates distances that it obtained. Therefore, in this worked the air gap of the microphone sensor was constructed at maximum referent gap with 3.5 μm. Furthermore, this desired structural is provide for prevent the collapsing a membrane operating at 40% of the maximum of the gap range was performed. Based on the simulation results, the number equivalent percentage of deflections membrane relative to the maximum air gap. Significantly, the membrane with 0.8 μm-thickness was suitable membrane thickness for using of sensing of microphone application.

Table 5.1 Summary of polysilicon membrane thickness relative to deflection with applied AOP.

Membrane thickness (μm)	Membrane deflect (μm)	Air gap (μm)	% deflection
0.5	5.42	3.5	155%
0.6	3.11	3.5	89%
0.7	2.13	3.5	61%
0.8	1.48	3.5	42%
0.9	1.13	3.5	32%
1.0	0.84	3.5	24%

However, it was obtained that the membrane has collapsed when applied sound pressure increased to 130 dB-SPL. This state is referred to the touching point of a collapsed membrane as located at the maximum air gap distance of 3.5 μm. Therefore, the S-CTC structure is need to compensated for the parallel plate distance between two capacitor plates. The optimal silicon etched depths which calculated from FEM for S-CTC with three different step heights are 1.5, 1.0 and 0.33 μm, respectively.

5.2 3-D lithography with MFT mask validation result and discussion

As described in Chapter 3, the conceptual work ideal and the purpose of three-dimensional lithography processes with MFT mask implemented to form a contoured cavity for capacitive sensors structure. In addition, this has followed at based on FEM modeling resulted of the desirable of necessary membrane performance that corresponding to cavity depth.

However, each step of the staircase should get approached to maximal of higher to obtain the capacitance values. The staircase cavity desired depth profiling can be fabricated with conventional lithography but the substance of manufacturing cost will be increased. Therefore, MFT mask and 3-D lithography process are needed to replacing the conventional-lithography which offers a high-effective solution utilization to formed multi-level of etching profile fabrication process to be in one process cycle. However, first implementing of 3-D process integration the material etched rate and etch selectivity needed to verification its properties. Therefore, there must be investigating the processes capacity that related chosen an available with the photoresist and silicon for the final determined of etching control parameters during implemented 3-D lithography. The desirable of fixed plate contour cavity with three level staircase etched profile is performed of single-process lithography and etched with field emission scanning electron microscope (FE-SEM) captured image presented

in Fig. 5.1. The cavity etched depth is corresponding of the compensated to membrane deflection properties. This capacitive sensor structure's fixed plate with contour cavity S-CTC was designed by arrangement for three levels of the cavity etch targeted, C1, C2, and C3. In this S–CTC structure.

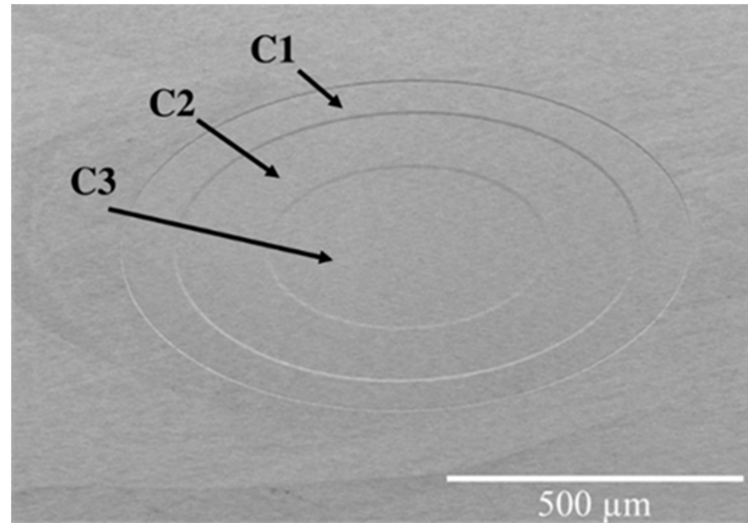


Fig. 5.1 SEM Captured image of Fixed plate with S-CTC structure.

The summary of 3-D lithography with full development process with validated of MFT mask formed an S-CTC cavity for as shown in table 5.2.

Table 5.2 Summary the relation of MFT mask lithography process.

Area	Si Etch target (μm)	PR remain (μm)	Cr Thickness (nm)	Transmission (%T)	Exposure dose (mJ/cm^2)
C3	0.3	2.21	14	0.304	60
C2	1	1.6	4	0.624	130
C1	1.5	0	0	1	208

5.3 Device fabrication process results and discussion

As mentioned in the previous Chapter 2 regarding to the staircase structure it can be performed by using the conventional process. The method of 3-D lithography process is more advantage and get lower cost effective [29]. Fig.5.2 shows the comparison of the fabrication process of a contour cavity with silicon fixed plate etched depth measured performance.

The measured between conventional fabrication process and 3-D lithography process with MFT mask. The 6-inch silicon substrate is etched and measured their cavity depth. However, the results were significantly undifferentiated with the variation of etched depth profile. Therefore, the silicon etched depth resulted of S-CTC structure at deeper located at C3 =1.85± 0.03 μm, C2=1.11 ± 0.08 μm and C1= 0.28 μm respectively. At the same time, the etched depth of control samples which convention fabrication process was 1.64 ± 0.03 μm, 0.88 ± 0.03 μm 0.27 ± 0.01 μm, and 0.88 ± 0.03 μm. In addition, the summary of the process performance in Table 5.3 is shown with the S-CTC structure etch target and the comparison of both typical two types based on the lithography process. The resulted of this experiment with MFT mask application has significantly of the final etched depth was a little greater than specification desirable from the target and variation higher than the conventional process.

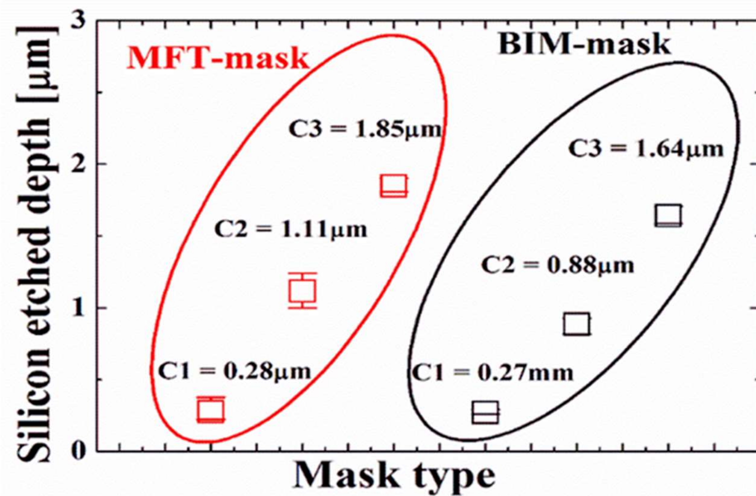


Fig. 5.2 Comparison etched depth of three different step heights of S-CTC structure with MFT-mask and conventional process.

Table 5.3 Comparison of silicon cavity S-CTC of MFT and BIM mask validation.

LOC	Etch target (μm)	BIM etched depth (μm)	BIM variation	MFT etched depth (μm)	MFT variation
C1	0.33	0.27	±0.01	0.28	±0.05
C2	1.0	0.88	±0.03	1.11	±0.08
C3	1.5	1.64	±0.03	1.85	±0.03

As mention in the previous chapter, the capacitive microphone structure consists of two wafers process fabrication requirement as shown in Fig. 5.3 of Bottom mount structure. The Fig 5.3(a) represents a substrate with heavily doped silicon of the fixed plate [55], which is included of fixed plate pad, acoustics holes, plate isolated as shown. An acoustic-holes has provided to reduce acoustics damping effects [56]. Therefore, if the hole is gaping, they would be disregarded the capacitor areas. However, in this design the optimal acoustic-hole size was 15 μm. desirable Fig 5.3(b) shows of the moving plate with a polysilicon membrane connected to the bonding pad via feed through located at rigidity area. The polysilicon material properties must achieve corresponding to meet the appropriate with electrical and mechanical properties as device desired. However, this experiment was found that the polysilicon with LPCVD deposition process which the optimal of thin film deposited by in-situ doped with phosphine with the deposition temperature at 650°C and annealing temperature at 900 °C was properly process parameter.

Based on this guideline was suitable for film electrical properties as low conductivity to lower than 20 Ω/Sq. And polysilicon film leftover stress-free was suitable for MEMS microphone desired relative with C-V characteristic as shown in Fig 5.4 with before adjustment of annealing temperature. The result shows there was gathered of two groups. Note that the C-V characteristics of MEMS-based capacitive microphone that annealed in N_2 ambient (14 SLM) at 850 °C in 30 minutes and 950 °C in 30 minutes. In case of the device with a more moderate annealing temperature of 850°C in 30 minutes, the capacitance of five numerous devices (A1, A2, A3, A4, and A5) called A-group devices were measured. It was founded that the variation of absolute capacitance of A-group devices is in the range of few pico-farads. Therefore, the bias voltage was varied from 2 to 8 Volt. However, all devices in A-group have a capacitance value higher than that of theoretically. The calculated capacitance value should be obtained which was equal to 2.2 pF. In addition, the C-V characteristics showed low pull-in voltage of 4.0 V and exhibited large variation of capacitance value. In case of the devices with a more excessive annealing temperature of 950°C in 30 minutes, the capacitance of three numerous devices (B1, B2, B3, B4, and B5) called B-group devices were measured. It was got that all the devices in B-group have an absolute capacitance value closed to the calculated value of 2.1 pF.

However, the C-V characteristics showed extremely high pull-in voltage that approximately at a biased voltage of 33 Volt [25]. The different of pull-in voltage of the samples with altered annealing condition might be related to residual compressive stress in the polysilicon membrane. The lower annealing temperature of 850°C in 30 minutes generated more significant residual compressive stress in the polysilicon membrane. Which compared to the higher annealing temperature of 950°C in 30

minutes. Therefore, the polysilicon membrane with an annealing temperature of 950°C condition may produce a higher pull-in voltage when compared to lower annealing temperature. Which this resulted, the annealing condition should be further optimized the trade-off between the leftover stress and achieved high consistency of changing capacitance value, and bright pull-in voltage to lower below 20 V.

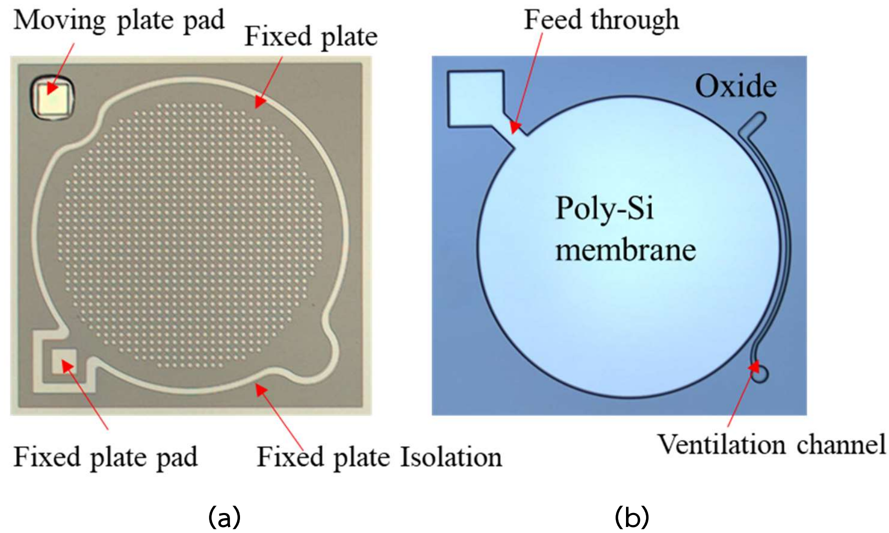


Fig. 5.3 Top view photograph of the microphone structure with back plate pattern and moving plate.

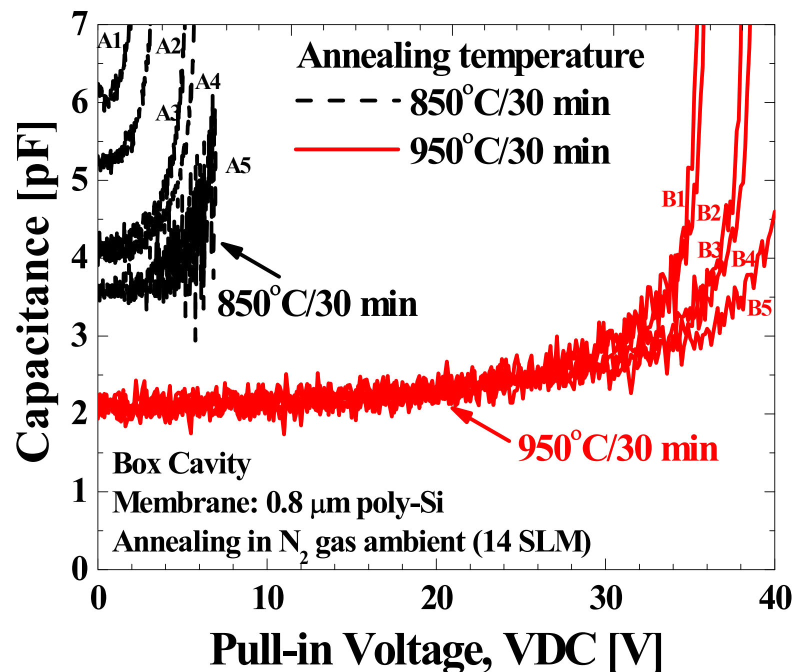


Fig 5.4 C-V characteristics of capacitive sensor with conventional box cavity before adjustment annealing temperature.

5.4 Capacitive sensor electrical characterization

This section, it is concluded chapter of the final state of the academic research study to perform an electrical measurement related to capacitance sensor based on the characteristic of the capacitance versus bias voltage (C-V). The method was acquired using the semiconductor device analyzer Agilent B1500A measurement tools. The C-V characterization of MEM silicon capacitive microphone as used of 0.8 μm-thick polysilicon for sensing membrane with it were annealed in N_2 ambient (14 SLM) at high-temperature at 900 °C in 30 minutes. The resulted of fabricated processes wafer was done, the C-V characteristic performance as shown in Fig. 5.5. It was significantly obtained constant capacitance at an initial zero bias voltage value was close to the predicting calculated value at 2.2 pF. Therefore, the results C-V characteristics of a capacitive sensor with the conventional box cavity structure and the staircase contour cavity structure.

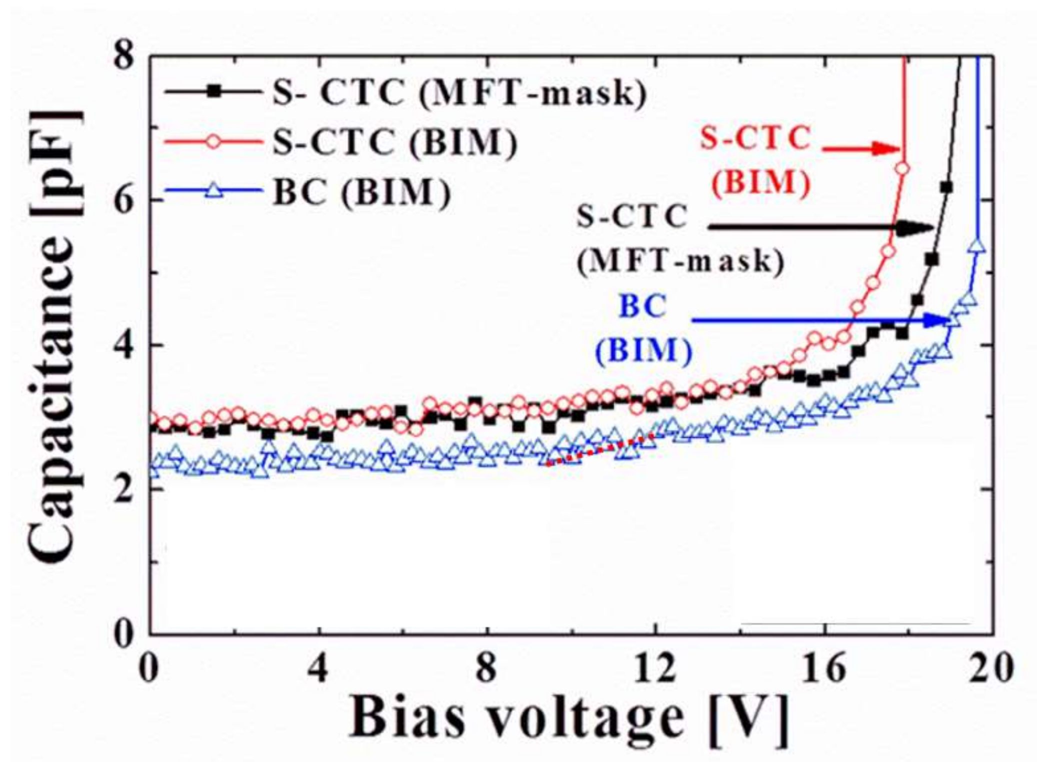


Fig. 5.5 C-V characteristics of capacitive sensor with conventional box structure and staircase contour structure.

However, in which both a conventional process and a multi-film masking process were used to fabricate air gap cavity. The measurement shows that the

average of an absolute capacitance for a BOX structure (BC) is obtained equal 2.2 pF and for an S-CTC is obtained higher of 2.9 pF. In addition, the changing capacitance at referent bias voltage based on this experimentation as listen in the summary in Table 5.4. Whereas, the pull-in voltage that captured between both group of S-CTC wafer which is deflected causing form an electrostatic forcing to bend at the flexible plate conducts to attract the membrane move to a back plate. Based on the resulted of S-CTC was obtained of the pull-in voltage above 16 Volt. Although, the results of both designs (BOX and S-CTC) has obtained the most of pull-in greater than 16 Volt, the collapsing voltage of the plates with S-CTC structure is maintained of 2 to 3 Volt. Earlier than the box cavity design in which the collapsing is closer to roughly 20 Volt. This accelerated collapsing of the plates in S-CTC, in this case is might be due to the thickness variations formed within the diaphragm.

Table 5.4 Summary of capacitance characterization.

Structure	**0V**	**12V**	**ΔC**	**Pull-In**
Box cavity	2.4 pf	2.75 pF	0.3pF	18.3V
S-CTC with MFT	2.9 pF	3.32 pF	0.42pF	16.5V
S-CTC with multi-layer	2.9 pF	3.31 pF	0.41pF	16.2V

However, the changing in capacitance (ΔC) value based on effected with bias input with sweeping voltage as shown in Fig.5.5. Based on the measure resulted, we can have assumed input voltage using for sensor microphone when packaging them to the pre-amplifier dice with charge-pump bridge regulator circuit consideration. In this case, defined at 12 volts, the changing capacitance with 12 VDC biased was obtained at 0.3 pF for BOX structure and 0.41 pF and 0.42 pF for S-CTC structure respectively.

Chapter 6
CONCLUSION

This thesis studied to investigate the fabricating an air gap with a unique feature of the cavity with a staircase contour shape with the using of non-conventional multi-film thickness masking in lithography process. However, the staircase-shaped contour cavity was formed the air gap structure between the capacitor plates. Whereas, the moving plate (membrane) in a capacitive pressure sensor deflects towards the fixed plate with optimizing of the capacitance value and change in capacitance value.

The structure is defined with multi-level etching steps on the fixed plate formation with newly of multi-film thickness mask was designed by varying the thickness of the chromium film deposited layer. Which is can be regulated the light emission through the mask that the MFT of 0, 4, 14, and 114 nanometers respectively. This mask was then used to expose the photoresist layer which is a part of a layer that forms the 3-d microstructure profile desired fabricate on a silicon substrate. While, the exposure sequence in the lithography process, which is varying of thicknesses of chrome layers that allows the intensity of lights to pass through and expose the photoresist layer beneath the mask. At that point, the photoresist was developed, and a pattern was established with 3-D microstructure such staying of the resist as different step as 2.21, 1.6, 0 μm respectively. The thickness of the photoresist varies in accordance with various exposure energies passed through the chrome file. This varied photoresist thickness acts as a selective etching barrier during deep RIE of silicon etching such as 1.3 : 1 (PR : Si) selectivity. Single dry etching of silicon was carried out and a desired three-dimensional staircase cavity pattern was formed as per the design need which is the center portion of the membrane area was etched total depth of 3.5 micrometers and the rest of the area etched was compensated formed at fixed pated target of 1.5, 1.0, 0.33 micrometer respectively and the result were obtained of 0.28, 1.11, and 1.85 micrometer.

The results show that the absolute capacitance value with an S-CTC structure is 31.8% higher than a conventional Box cavity (BC) structure. The capacitance value changes from 2.2 pF to 2.9 pF and changing capacitance at bias voltage 12VDC obtained at 0.3 pF for BOX structure and 0.41 pF and 0.42 pF for S-CTC structure respectively. For capacitor plates that maintains a similar area. Both capacitor plates are formed by fusion bonding two silicon substrate in which each plate is developed.

MEMS device based on the capacitive structure was fabricated on the wafer level, which represents the primary sensing element for assembling into the final microphone packaged. Therefore, the acoustical and electrical characteristics property

related to the final microphone product has not included in this thesis. However, this is promising technology renders an opportunity to improve the next generation of ultra-low pressure sensors for microphone applications.

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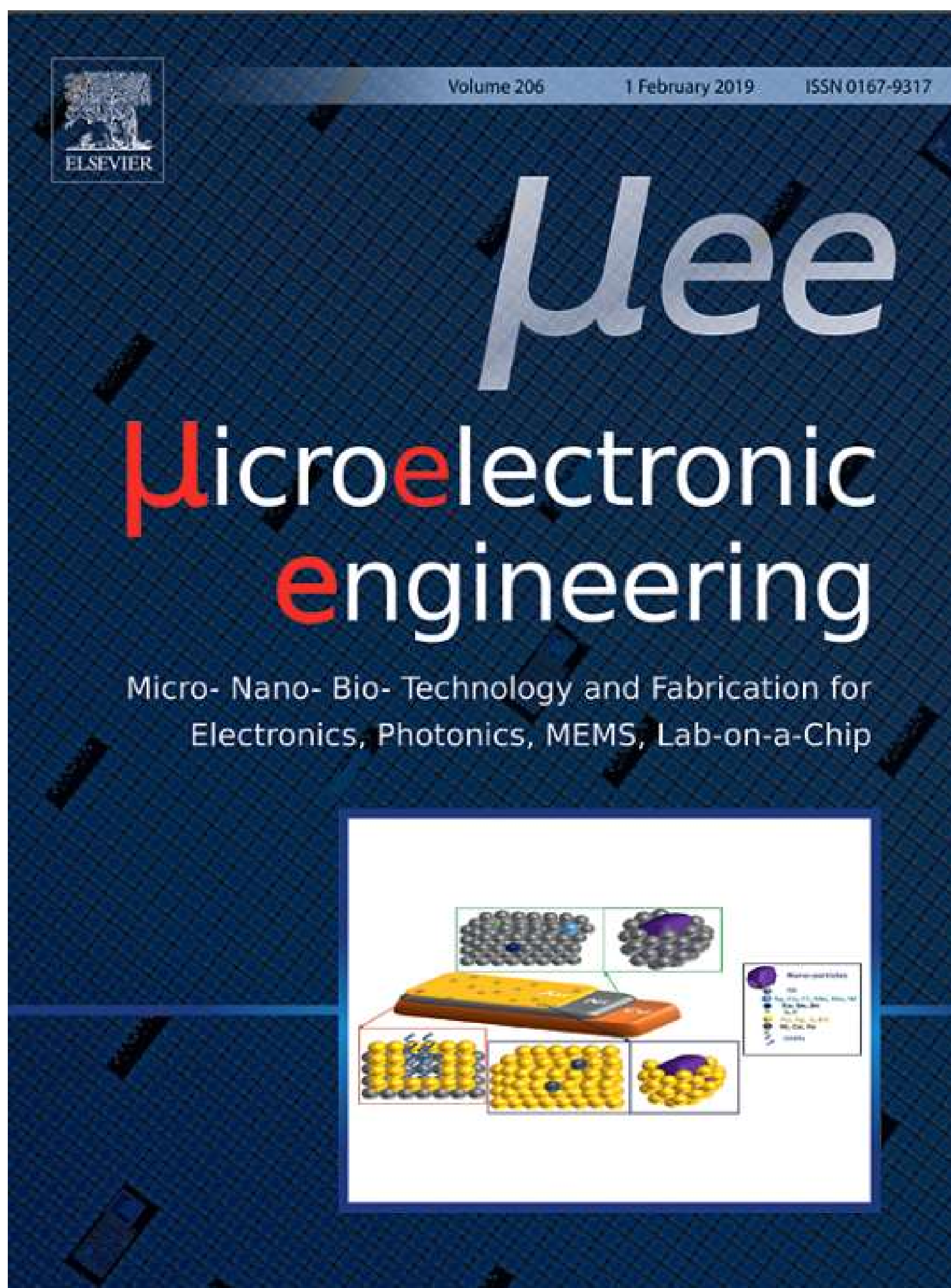
Appendix

Appendix A

Paper publications



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Research paper

Fabrication of MEMS-based capacitive silicon microphone structure with staircase contour cavity using multi-film thickness mask

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ABSTRACT

In this work, a silicon capacitive microphone structure with a three-dimensional staircase style contour cavity (S-CTC) is developed using a newly developed Multi Film Thickness photo lithography process. This newly developed Multi Film masking process overrides the conventional wisdom in which the staircase style cavity is formed using multiple exposures of mask and multiple etchings of silicon. With this newly developed photo lithographic technique, a Multi Film Thickness (MFT) mask is fabricated with varying chromium film thicknesses such as 0, 4, 14, and 114 nm thick. The mask was then evaluated to fabricate a microphone structure with a three-dimensional staircase style cavity. Once the mask was patterned onto a substrate, a single dry etching of silicon was carried out and a desired three-dimensional stair cavity pattern was achieved. Surprisingly, our results show that a capacitive sensor with an S-CTC structure has an increased absolute capacitance value by an average of 30% in comparison to a conventional box cavity (BC) structure. This may indeed improve SNR as we anticipated. The capacitance value changed from 2.2pf to 2.9pf for the same dimension of devices. This promising technology renders an opportunity to improve the next generation of ultra-low-pressure sensors for microphone applications.

1. Introduction

Silicon (Si) microphones, a type of Micro-Electro-Mechanical System (MEMS) microphone is one of the focal points in the semiconductor sensor industry due to its sheer volume application. In early 2000, Si microphones were first introduced in mobile phones by Motorola [1]. Since then, the Si microphone business has grown steadily and, in most cases, has replaced the conventional electret microphone. Simultaneously, the mobile communication industry has been growing in regard to smart phones, due to a smart phone's sophistication which offers unique features that increases its usage. At present, some smart phone models have as many as three or four microphones per mobile device [2].

A microphone functionality and its sophistications are divided into two basic categories: 1) electrical functionality and 2) acoustic functionality. The electrical functionality such as impedance, current consumption, and power supply rejection ratio (PSRR) all have an indirect impact on sound quality. The acoustic functionality such as frequency response, sensitivity and signal-to-noise ratio (SNR) are directly coupled to the quality of the sound. Among those parameters, the SNR is a key function that is directly coupled to the clarity of the sound [3–6]. Currently, the most capable microphones in mass market are performing in the sensitivity range of −38 dB (decibels) and an SNR of −64 dB for mass volume applications. However, sophisticated customers keep demanding higher SNR microphones with no sign of capping it [7]. With this functionality at the helm of its performance, mobile phone manufacturers are demanding higher SNR microphones. Incumbent Si microphone suppliers are facing their limitations in SNR improvement due to their capacitive sensing design and process. Thus, an alternative sensing technology such as piezoelectric technology should be considered in a second wave of microphones and is currently being explored by a few companies [8]. Despite its limitations, the capacitive Si microphone is still widely used in mobile phones due to the advantages of simpler packaging [9–11]. But with the introduction of piezoelectric technology, competitors in the market will need to adapt as such to improve acoustic functionality, such as increased SNR.

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The total acoustic noise of a Si microphone depends on both the electrical performance and the mechanical performance of the sensor. The electrical noise is mainly due to leakage current density (J_g) between both capacitor plates and the acoustic noise is mainly due to the damping property of the sensor. Larger gaps between the plates with an adequate number of acoustic holes produces lower noise. However, the larger gap between the plates and the large number of holes severely reduce its capacitance value due to a loss in plate area and thereby reducing sensor sensitivity. One way to approach this issue is to increase the diaphragm area and reduce the thickness of the diaphragm. However, both approaches have a negative impact in competing cost. The die size increases as the area of a diaphragm increases, which leads to higher chip cost. Moreover, an ultra-thin diaphragm is susceptible to over-pressure collapse and electrostatic collapse [12,13]. Thus, the limitation of the performance with capacitive-based Si microphones are due to their structural limitations. One of those structural limitations is the conventional BOX cavity design. The maximum deflection of the diaphragm occurs at the center of a diaphragm and only 2/3 of the diaphragm area from a dynamic deflection responds to the external sound wave pressure. This means that 1/3 of the diaphragm along the edges (rigid area) does not move parallel to the fixed plate and therefore does not contribute to the overall change in capacitance value [14]. In this case, if the rigid area of the diaphragm can be manipulated in relevance to a fixed plate, a much higher and optimal capacitance value can be obtained. A capacitive sensor design with a contour shaped or staircase style cavity structure (S-CTC) is the most optimal design to take advantage of the rigid area. But in order to achieve this staircase style cavity, a multiple step etching is required and requires multiple masking processes. This drastically increases the cost of manufacturing and loses its competitive edge. Therefore, a new technique is explored to consolidate both masking and etching processes into a single step process to achieve the same result as a multiple step process.

The conventional multi-step litho-etch process uses a binary intensity mask (BIM) which is not the best patterning process to fabricate suitable 3D structures [15,16]. Presently, gray-scale lithography (GSL) is a patterning process that can fabricate smooth curvature 3D structures such as a curvature CTC (CTC) structure. However, GSL is a very expensive patterning process due to the cost of ultra-fine GSL masks [17,18]. Hence, we propose using the multi-film thickness mask (MFT-mask), which provides a low-cost patterning process to form a similar 3D structure such as the staircase pattern resulting from the one exposure step to a GSL mask [19,20].

2. Capacitive sensor structure and operating principle

2.1. Structure of Si microphone with various cavity structures

As mentioned above, one of the basic components of a capacitive microphone device are the two parallel plates or electrodes which are isolated by a thin air gap. When a biasing voltage (V_b) is applied to these electrodes, an electrostatic force is formed between both electrodes and the electrodes are attracted toward each other. In the case of capacitive sensing, one electrode is rigid, and the other electrode is a membrane or diaphragm. Here, the diaphragm bends or is attracted toward the rigid electrode [14]. Generally, polysilicon (Poly-Si) film is used as a sensing membrane for many sensing devices including Silicon microphones. The picture below describing three different forms of cavities including BC, CTC, and S-CTC structures (Fig. 1) in which Fig. 1(a) shows a standard BC structure, Fig. 1(b) shows a CTC structure and, Fig. 1(c) shows a S-CTC structure. CTC structures produce the optimum condition in which the distance between both the rigid plate (Fixed plated) and the poly membrane is constant for the entire plate area while applying sound pressure. However, fabricating such a design would require a gray scale masking process which is prohibitive in cost. In the case of an S-CTC structure, the fixed plate is nearly parallel to the deflected membrane. Therefore, it is expected that the performance of the S-CTC structure would be similar to the CTC structure and would be just as convenient to fabricate in mass production at a competitive cost.

2.2. Simulation of membrane deflection on contour cavity structure

The capacitance value (C_v) of a Si microphone can be calculated by using the concept of a parallel plate capacitor. The general reference capacitance without any applied pressure of the parallel plate capacitor can be defined as the following equation.

$$C_0 = \frac{\varepsilon A}{d} \tag{1}$$

C_0 is an initial capacitance value, ε is a relative vacuum permittivity, A is the surface area of the plate and d is the gap between two parallel plates.

When the sound wave pressure is applied to the flexible membrane, the membrane or diaphragm is deflected. The capacitance value between the fixed plate and moving plate is changed according to the level of the membrane deflection and the air gap distance between those plates. The variation of overall capacitance value C_1 of the capacitive-based Si microphone can be defined as the following equation.

$$C_1 = \int_0^a \frac{\varepsilon_0 2\pi r}{d - w(r)} dr \tag{2}$$

where C_1 is the overall capacitance value when the diaphragm is deflected by the distance of w, a is the membrane radius and d is an air gap [21].

In order to design the capacitive sensor with an S-CTC structure, the distance between the plates or air gap distance needs to be determined. Therefore, a Finite Element Model (FEM) is developed to determine the air gap using Solidwork™ solver Fig. 2. For the membrane thickness and size, arbitrary parameters suitable for fabrication were chosen as a baseline. Poly membrane of 0.8 µm-thick circular shape with a diameter of 930 µm was construed as the membrane. In addition, the following poly-Si properties were utilized for the modeling: Young's modulus of 160 MPa, Poisson's ratio of 0.22 and tensile residual stress of 5.0 MPa. The modeling is first tested at maximum sound pressure or known as acoustic overload pressure (AOP) of 28.5 Pa, equal to 123 dB-sound pressure level (dB-SPL) to determine the air gap between both plates. The result shows that the AOP maximum membrane deflection reached 40% of the total air gap distance at the center of CTC and moving plate. The modeling then extended to evaluate maximum collapsing pressure [Fig. 2(b)]. It was found that membrane collapsed when the applied sound pressure was increased to 130 dB-SPL [22,23]. The touching point of a collapsed membrane is located at the air gap distance of 3.5 µm. Therefore, the S-CTC structure is required to compensate the parallel distance between the two plates. The optimized Si-etched depths calculated from FEM for S-CTC with three different step heights are 1.5, 1.0 and 0.33 µm, respectively.

3. Development of staircase cavity using MFT masking

3.1. Concept and Purpose of MFT masking development

This paragraph explains the concept and purpose of this multi-film thickness (MFT) masking development. As mentioned above, a unique capacitive sensor design is being evaluated to achieve a higher SNR device. In this design, staircase style air gaps (cavity) are formed to maximize the capacitance value and change in capacitance value during sound sensing. The Fig. 1(c) illustrates the cross-sectional view of the staircase cavity and Fig. 2(b) of the FEM model shows the necessary cavity depth at which each stair should be if expected to produce higher SNR. As mentioned before, the staircase cavity can be fabricated with multiple masking processes; however, multiple masking processes will

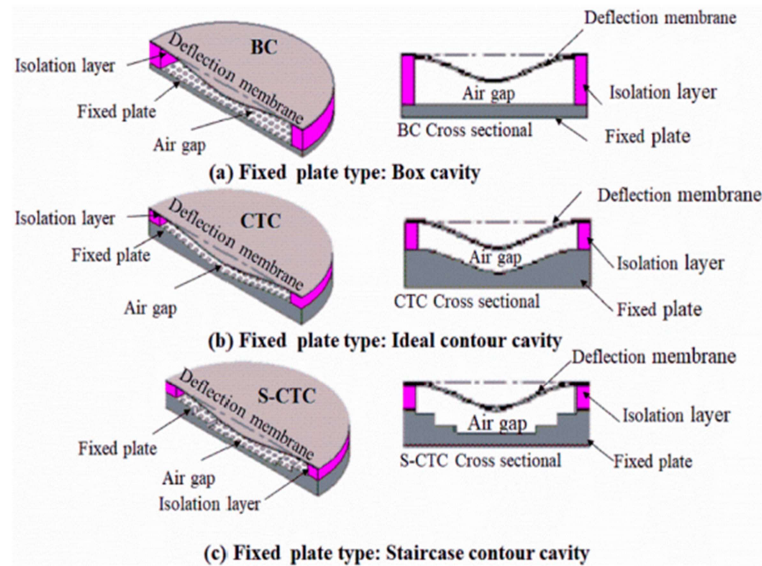

Fig. 1. Cross-sectional schematic diagrams of MEMS-based capacitive Si microphone with different cavity structures (a) Conventional box cavity (BC) (b) Curvature contour cavity (CTC) and (c) Staircase contour cavity (S-CTC).

substantially increase manufacturing cost and thus the design would lose its competitive edge. Therefore, the development of using a single mask process with MFT masking is a highly desirable solution. The following block diagram (Fig. 3) describes the sequence of developments that result in the desired outcome of utilizing the staircase cavity for capacitive sensor design.

3.2. Etch rate and Etch selectivity (PR: Silicon)

The stair case cavity requires different etch depths in silicon Fig. 4(a). The purpose here is to achieve these different etch depths in a single step etching process. As shown in Fig. 4(b), there are three stairs formed in the silicon substrate. The centre portion of the stair is the deepest point in staircase. This centre point is etched without any photoresist coverage over its silicon surface. However, the other two stairs were etched with a selective thickness of photoresist over its silicon surface. In order to simultaneously etch all three stairs, the method depends on two key parameters: 1) the etch rate of silicon and photoresist and 2) etch selectivity between silicon and the photoresist. The selectivity is chosen as 1.3:1 for photoresist: silicon. Although higher selectivity is available, 1.3:1 is chosen to maintain better

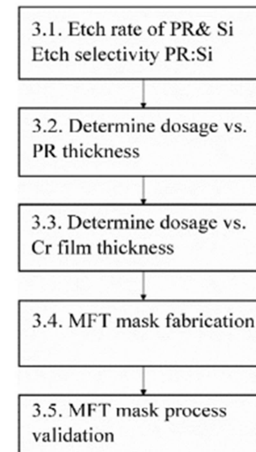

Fig. 3. MFT development sequence.

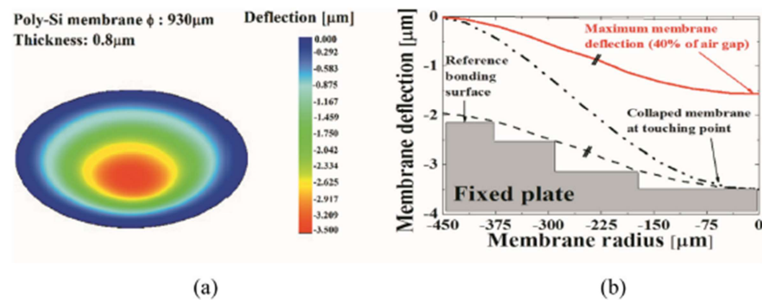

Fig. 2. The FEM simulation results of 0.8 μm-thick circular poly-Si membrane deflection on CTC structure that corresponding to the applied sound wave pressure (a) Contour plot of the membrane deflection and (b) Air-gap distance variation between fixed plate and moving plate across the diameter of poly-Si membrane.

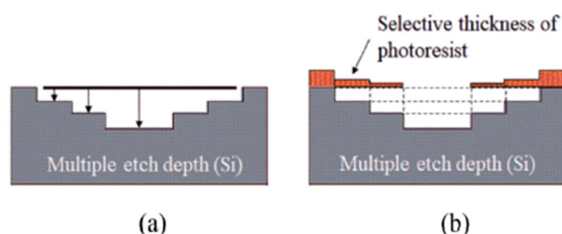

Fig. 4. Cross sectional view of Staircase design and 3-D cavity formation.

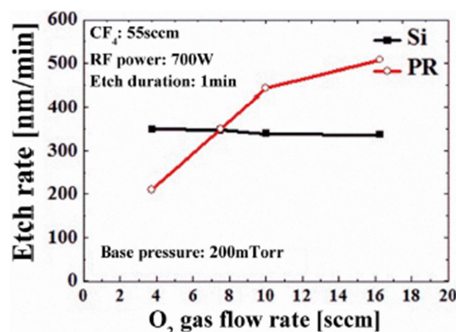

Fig. 5. Effect of O_2 gas flow rate in CF_4/O_2 plasma on the etch rate of silicon and PR.

uniformity of etching. The information is gathered from previous publication [24]. The graph Fig. 5 shows the etch rate of both silicon and photoresist. The selectivity is chosen from the graph to suitably fit the staircase desired etch depth.

3.3. Determine dosage to control PR thickness

Since we have established above the desired photoresist thickness to form the appropriate staircase depth, we must now establish the desired exposer energy or dosage to achieve the selective thickness of photoresist as shown in Fig. 6 for it to remain after photoresist development. The experiment is like a standard photoresist lithography process, except here the photoresist is underdeveloped to maintain a certain thickness over the pattern. It means that the photoresist over the pattern is partially removed and the remaining photoresist is left to etch certain depth for the stair cavity in silicon substrate.

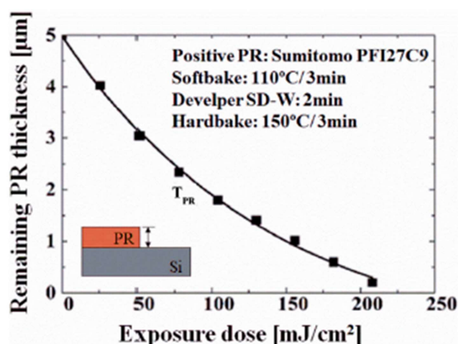

Fig. 6. PR thickness vs Exposure dose.

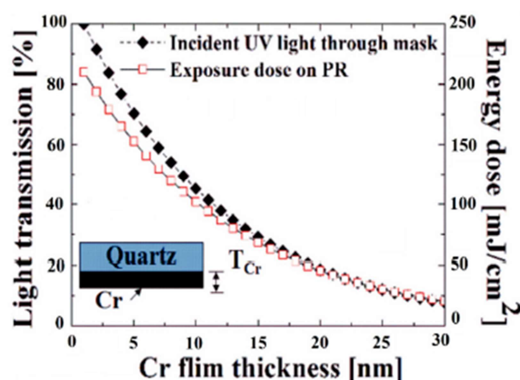

Fig. 7. Light transmission thru various Cr film thickness.

3.4. Dosage vs. chrome film thickness

Since we have established above the necessary dosage required to selectively develop photoresist thickness, we must now establish the controlling energy dosage output through a chrome mask. The key idea behind the MFT mask is that when the thickness of the chromium film (*Cr*) varies in the mask, the exposed energy through this varied film changes the energy output level and that exposes the photoresist to various energy levels [20]. The energy output through chrome film is governed by eq.3. The amount of energy going through the chrome film is determined by the thickness of film as shown in Fig. 7.

$$I_x = I_0 e^{-\left(\frac{\mu}{\rho}\right)\rho x} \tag{3}$$

where I_x is the transmitted light intensity through a medium, I_o is the intensity of the light incident on the medium, μ is coefficient of the light intensity absorption, ρ is medium density and x is the thickness of medium.

3.5. Design and making of MFT-mask for product fabrication

As shown in Fig. 8(a), the product requires altogether three stairs that are etched in silicon. There are three circular patterns corresponding to the staircase patterned and etched. This means that the MFT mask requires three corresponding patterns in the mask. To achieve the said requirement, a corresponding MFT mask is fabricated and the following process sequence shows the details of MFT fabrication.

This MFT mask-making process is similar to a standard wafer photolithography process which is coupled with additive and subtractive processes. It starts with a raw material of 7 × 7 inches of binary intensity mask (BIM) with an initial chrome thickness of 100 nm. First PR (Shipley S1805) is spin coated and the substrate is baked at 100 °C for 90 s. Then a circular pattern (C1) is patterned with a Heidelberg Direct Laser (DWL). The pattern is written with a 120 mW/cm^2 power intensity (λ: 436 nm, g-line) and developed in the Shipley MF-26A for 1 min. The substrate is then post baked at 120 °C for 90 s in the hot plate. Finally, the chrome is fully etched away inside circular pattern (C1). A chrome is etched using a CEP-200 Micro-chrome-technology etchant. Then another layer of chrome is deposited over the mask and a second circular (C2) is formed using same above-mentioned procedures except for varied time for chrome etching time. Third circular (C3) followed the same procedure as C2. After that, the remaining PR is removed by a mixture of 70% concentration Sulfuric Acid (H_2SO_4) and 30% Hydrogen Peroxide (H_2O_2) with the ratio of 4 to 1 at 120 °C for 10 min. Finally, the mask is rinsed with deionized water (DIW) for 10 mins. The Fig. 8(b) shows full process flow and Fig. 8(c) shows the top view of mask.

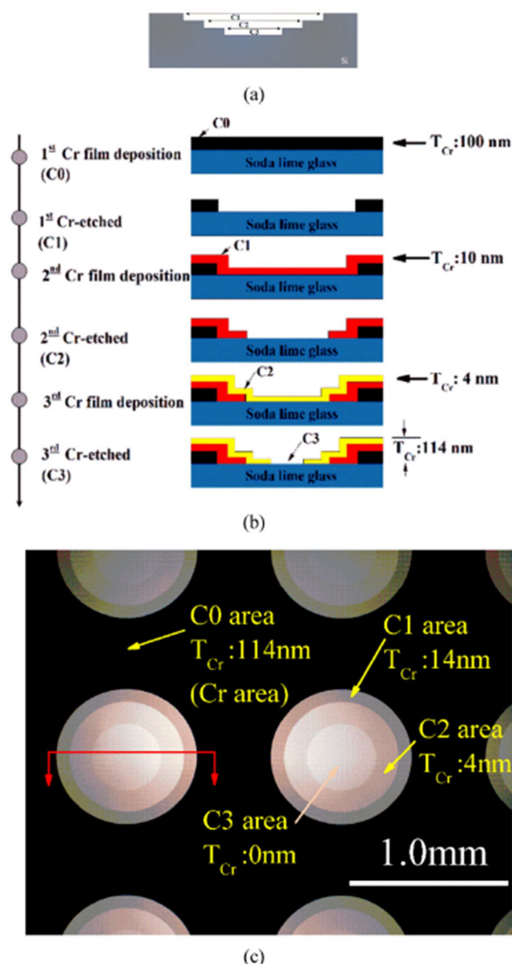

Fig. 8. The MFT-mask with three different steps for S-CTC patterning (a) Cross section view of circular patterns exposed and etched in silicon to form staircases (b) Cross-sectional schematic diagram of fabrication process of MFT-mask and (b) Top-view OM image of MFT-mask.

The thickness of the chrome film layers deposited directly corresponds to the chrome thickness needed to produce the exact amount of exposure energy output needed to pattern and develop the underlying photoresist which is used as a masking material to etch the desired staircase depth.

3.6. FMT mask validating

As a result, the positive photoresist (PR) lays under the Cr film receiving various energy dosages governed by the chromium film thickness as shown in Eq. (3). After development of the PR, a three dimensional (3D) vertical sidewall slope profile with varying PR thickness is obtained. This 3D photoresist structure goes beneath the Si substrate via a single step dry etching process. Finally, a staircase style cavity is formed where the etch depth in the silicon substrate varied as per the initial thickness of the photoresist layer. The Fig. 9 shows a cross sectional view of 3D microstructure patterning using a MFT-mask. Based on this concept, a validation experiment was carried out. The information below shows the details and outcome of the validation experiment.

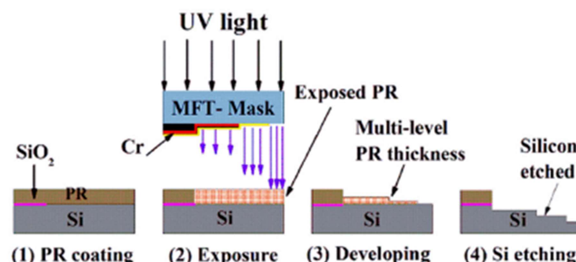

Fig. 9. Cross-sectional schematic diagram of 3D microstructure patterning by using MFT-mask.

First, a 5 µm-thick positive PR (Sumitomo PFI-27C9) was coated on a 6-in. silicon wafer and baked at 110 °C for 3 min. The wafer was then exposed with a UV exposure dose (λ: 365 nm, i-line). The exposure energy was varied from 80 to 240 mJ/cm^2 with a step increment of 20 mJ/cm^2. After exposure, the wafer was developed using a Sumitomo developer SD-W for 2 min and subsequently hard baked at 150 °C for 3 min. Finally, the remaining PR film thickness was measured by using a step profilometer (TENCOR P-10). Fig. 10 shows the resulting PR film thickness in the wafer modulated by both the exposure dose and the Cr film thickness. Based on the result it is found that the exposure dose of 200 mJ/cm^2 is required for properly patterning staircase cavity. At an exposing energy of 200 mJ/cm^2, C3 is fully developed while C1 (Cr: 14 nm) and C2 (Cr: 4 nm) are partially developed and the desired thickness of photoresist is left behind. The remainder photoresist thicknesses are 1.78 µm and 2.21 µm respectively. This means that when the Cr film thickness was varied at 0, 4, 14 and 114 nm, the percentage of light transmission through the MFT-mask was 100%, 70%, 30% and 0%, respectively. Therefore, an MFT-mask with three different steps of Cr film thickness can produce a S-CTC structure for Si microphone device.

4. Fabrication of capacitive sensor

The design of this capacitive sensor device consists of two wafer substrates. The fabrication of this capacitive sensor is divided into three segments. The first segment is forming a diaphragm (Handle wafer). The second segment is forming the fixed plate (Cover wafer) in which the staircase contour cavity (S-CTC) is fabricated. The third segment is device fabrication which includes fusion bonding in this case. The process flow of the Si microphone with S-CTC structure is shown in Fig. 11.

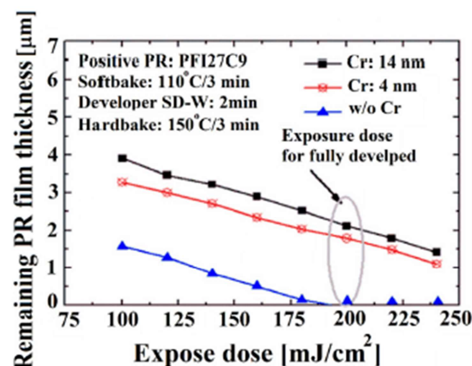

Fig. 10. Effects of Cr film thickness on the remaining PR film thickness by varied an exposure dose through the MFT-mask.

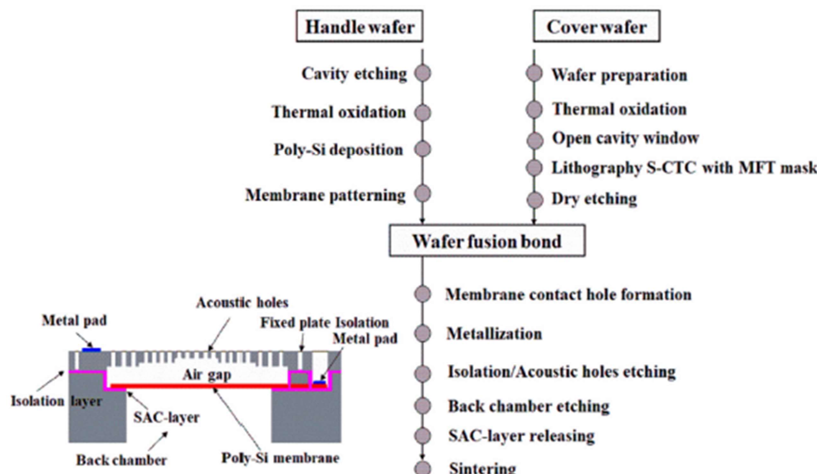

Fig. 11. Process flow for capacitive microphone with S-CTC structure.

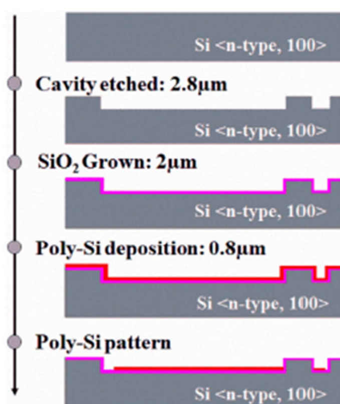

Fig. 12. Diaphragm wafer fabrication.

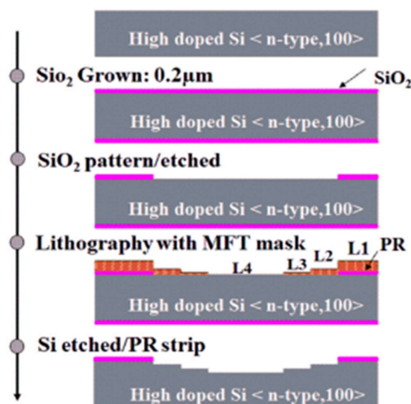

Fig. 13. Back plate fabrication.

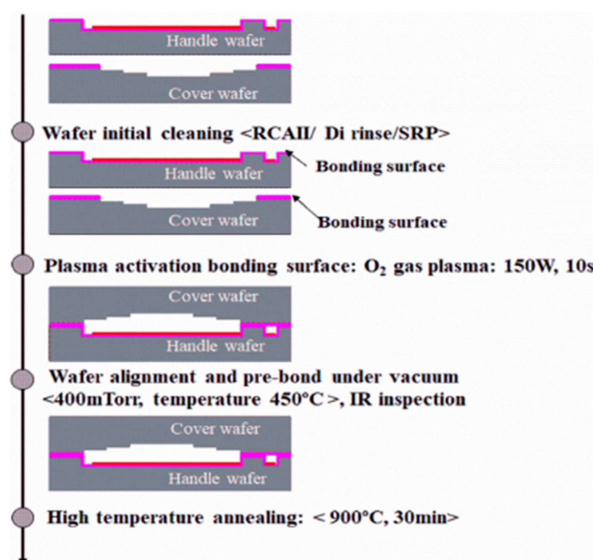

Fig. 14. Wafer fusion bonding schematic.

4.1. Fabricating diaphragm wafer

To fabricate a diaphragm wafer, the following steps were done. First a shallow cavity of a 2.8 μm in depth was etched in the silicon substrate. Followed by a 2 μm of thermal oxide (SiO2) was grown in the substrate. Subsequently a 0.8 μm thickness of in-situ doped LPCVD polysilicon was deposited at 650 °C. The polysilicon was then patterned and etched to form a diaphragm layer inside cavity (see Fig. 12).

4.2. Fabricating back plate (BP) wafer

To fabricate a BP wafer, a thermal oxide (SiO2) of desired thickness was first grown on the wafer. Then the cavity area was patterned, and oxide was etched away within the cavity. Lastly, a selective thickness of PR was coated over the wafer and the MFT masking process was carried out. After patterns were formed using the MFT mask, the cavity was etched using dry etch (see Fig. 13). In terms of MFT, a single lithography process with an exposure dose of 200 mJ/cm^2 was done through the MFT-mask over various Cr film thicknesses of 0, 4, and 14 nm. Then the PR was developed. The remaining PR film thickness was measured for 9 points in each area by using step profilometer. It was found that the remaining of PR film thickness at L_1, L_2, L_3 and L_4 position after developed and hard baked at 150 °C for 3 min are 5.0 ± 0.10, 2.7 ± 0.06, 1.8 ± 0.06 μm, respectively. Next, the patterns were

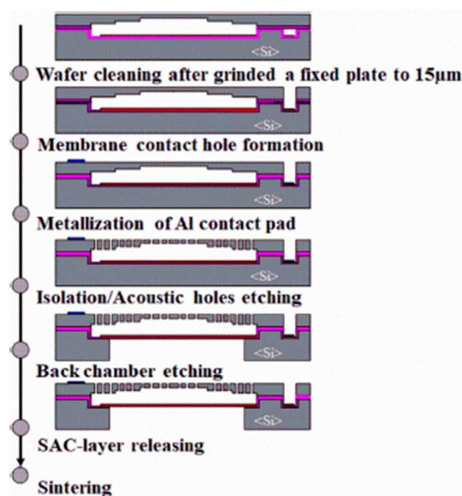

Fig. 15. After wafer fusion bonded process fabrication.

transferred to the Si substrate by etching in Reactive Ion Etcher (RIE) AMAT P5000. The CF_4/O_2 gas flow ratio was 55/10 sccm. The chamber base pressure was 200 mTorr, RF power was 700 W and the etching time was 4.5 min.

4.3. Device fabrication

The fusion bonding process is comprised of plasma activation, wafer pre-bond, high-temperature annealing, and grinding the bonded wafer [25]. The plasma activation was performed in order to improve a hydrophilic property of the bonding surface as shown in the Fig. 14. After pre-bonding two wafers, high-temperature annealing at 900 °C/30 min in N2 ambience was performed. Note that the annealing process is required to adjust film stress and a sheet resistance of the poly-Si membrane [26,27].

Next, the cover plate of the bonded wafers was grinded to reduce the wafer thickness down from 15 to 20 μm. Then the subsequent process included: poly-Si pad opening, metallization, perforation holes etching [28,29], back chamber etching, and sacrificial (SAC) oxide release to free the membrane of the microphone shown in Fig. 15. Finally, aluminium sintering process was done in forming gas at 430 °C for 30 min.

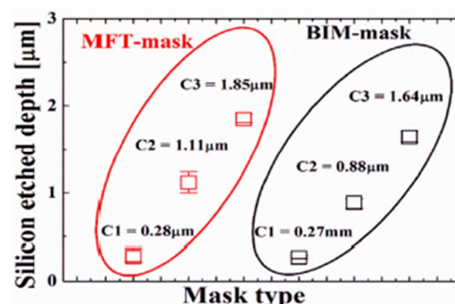

Fig. 17. Comparison etched depth of three different step heights of S-CTC structure fabricated by MFT-mask and multi-steps lithography process.

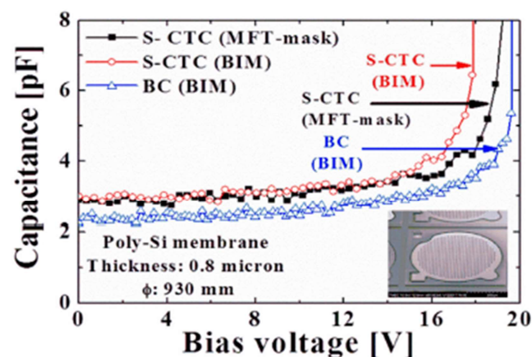

Fig. 18. C–V characteristics of capacitive sensor with conventional box cavity (BC) structure and staircase contour cavity (S-CTC) structure.

5. Results and discussion

5.1. MFT process

The results in Fig. 16 shows the top-view optical image and the scanning electron microscopy (SEM) image of an S-CTC. It was found that the qualities of a Si-etched pattern in section A-A (test sample prepared with conventional multiple masking process) was quite similar to the quality of MFT patterned and etched cavity (C–C). The Si etch depth of S-CTC structure were 0.28 ± 0.05 μm, 1.11 ± 0.08 μm and 1.85 ± 0.03 μm, respectively. The etch depth of control samples were 0.27 ± 0.01 μm, 0.88 ± 0.03 μm and 1.64 ± 0.03 μm,

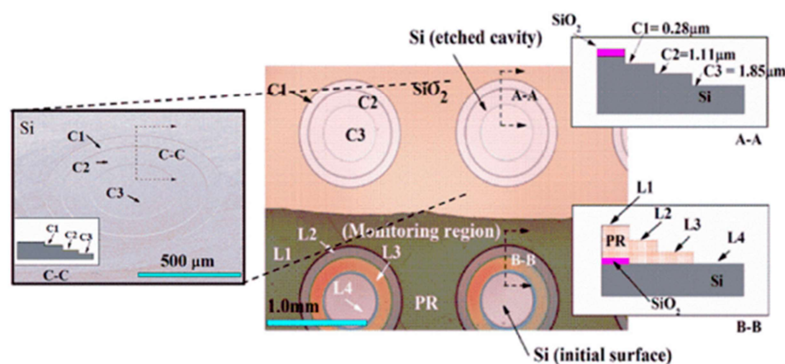

Fig. 16. Top-view OM image and SEM image of S-CTC structure fabricated by single exposure using MFT-mask. Section A-A is a Si-etched patterning region and section B–B is a monitoring region of PR pattern.

respectively. Therefore, no significant differences found between both methods (see Fig. 17).

5.2. Capacitive sensor

The capacitance C−V characteristics were obtained using a semiconductor device analyser Agilent B1500A. The absolute capacitance (C_v) and bias voltage (V_g) were extracted from C−V curves. The results in Fig. 18 show the C−V characteristics of a capacitive sensor with the conventional box cavity (BC) structure and the staircase contour cavity (S-CTC) structure in which both a binary masking process (BIM) and a multi film masking process (MFT) were used to fabricate cavities. The measurements show that the average absolute capacitance for a BC design is 2.2 pF and for a S-CTC is 2.9 pF. In addition, the pull-in between both plates due to electrostatic forces are beginning roughly above 16 V [30]. Although both cavity designs have a pull-in that begins above 16 V, the collapsing voltage of plates in S-CTC is 2 to 3 V earlier than the box cavity design in which the collapsing is closer to roughly 20 V. This accelerated collapsing of the plates in S-CTC is perhaps due to the thickness variations formed within the diaphragm, coming from the stair cavity fabrication whereas the box cavity design has a uniform thickness diaphragm.

6. Conclusions

The purpose of this new photolithography and etching process is to fabricate a unique capacitive ultra-low-pressure sensor for high SNR microphones and its consequent applications. Our target customers are mobile phone manufacturers and other peripheral applications. This is a consumer market and cost is a critical factor. Our product has to be highly competitive to incumbent products. This new technique developed delivers on our expectations. The MFT masking process enables us to consolidate multiple masking processes into a single masking and subsequently a single step in the silicon etching process. As a result of this new development, the capacitive Silicon microphone with three different steps ordinarily needed to create a staircase contour cavity (S-CTC) can be now fabricated by using both a single masking step as well as a single etching step. The qualities of a staircase structure fabricated by an MFT-mask not only renders similar qualities to those fabricated by conventional multiple masking steps but also reduces the masking cost substantially. However, this technique has not yet been implemented in mass volume fabrication and therefore has to be studied before 100% before such implementation.

The increased percentage of a capacitance value of a Si microphone with an S-CTC structure is an average 30% higher than the standard parallel plate box cavity for a given die size. The capacitance of a sensor with an S-CTC jumped to 2.9 pF from 2.2 pF as compared to a box cavity design. Therefore, the MFT masking process should be further evaluated for its repeatability and reliability. Upon subsequent successful outcomes after further evaluation, it can be implemented in fabricating an S-CTC in silicon microphone.

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Effects of Annealing Process on the Electrical Properties of MEMS Capacitive Microphone

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Abstract— **In this paper, the effects of annealing temperature after pre-bonding device wafer and cover wafer during wafer fusion bonding process on the electrical properties of MEMS-based capacitive microphone with 0.53 µm thick poly-Si membrane were investigated. By the annealing in N_2 ambient (14 SLM) at 900°C for 30 min, the device exhibited capacitance of 2.0 pF with pull-in voltage of 12 V. The significantly improvement of electrical properties is related to the reducing of residual stress in poly-Si membrane to near-zero level by using suitable annealing condition.**

Keywords — Annealing, C-V characteristics, MEMS capacitive microphone, Polysilicon membrane, Pull-in voltage, Residue stress

I. Introduction

A capacitive pressure sensor is very accurate and especially suitable for measuring ultra-low pressure in the range of a few Pascal such as a recent application of technique is used in the microphone mobile phones. The future performance trend of MEMS microphone is derived from its signal-to-noise ratio (SNR) value, currently those out in the market, state of the art microphones, there is offered the maximum sensitivity of -38 dB with SNR in the range of 63 to 66 dB. Furthermore, low cost is also a factor when selecting the components [1]. In general, the polysilicon (Poly-Si) has already been commonly used in the semiconductor industry. On the other related field such as Micro Electro Mechanical System (MEMS), poly-Si usage had been reported for moving elements such as flexible spring membranes and the rigid body electrode as the back-plate of capacitive microphone element [2]. Other material such as aluminum was also chosen as the candidate for membrane material [3]. Some devices used double poly-Si layers in the commercial product [4]. The key benefits of poly-Si were its common usage in the semiconductor industry such as gate electrode in CMOS, very high conformity film and high performance mechanical and electrical properties, and therefore, highly suitable the stability and flexible membrane all of these led to commercially application in MEMS-based capacitive microphones. The device is comprised of two parallel plates which are isolated by the air gap. When biasing voltage is applied to that electrode, an electrostatic force will attract the membrane causing deformation. Normally poly-Si film is deposited, doped and then annealed at high temperature to achieve the desired sheet resistance and suitable film stress for sensing membrane, which is the most critical parameter functionality of the working devices.

In the field of sound wave pressure measuring application, the membrane will deflect when pressure is applied up on it [5]. The capacitance value between these plates will change according to the level of deflection. Its reference capacitance without applied pressure can be defined as

$$C_0 = \frac{\varepsilon A}{d} \tag{1}$$

Where, C_0 is an initial absolute capacitance value, ε is a relative vacuum permittivity, A is the surface area of the plate and d is the gap between the two plates.

When sound pressure is applied to a flexible membrane, it changes the air gap between two plates. In turn, the overall capacitance value, C_1 , changes. It can be defined by the following equation:

$$C_1 = \int_0^{2\pi} \frac{\varepsilon_0 r}{d0 - W_0\left[1-\left(\frac{r}{a}\right)^2\right]^2} \tag{2}$$

Where, C_1 is the changing capacitance when the diaphragm is deflected (W_0). Therefore, In-plane deflection membrane.

$$C = \frac{tan^{-1}\left(\sqrt{\frac{W_0}{d_0}}\right)}{\sqrt{\frac{W_0}{d_0}}} \cdot \frac{\varepsilon_0}{d_0} \pi a^2 \tag{3}$$

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The opposite side

$$C = \frac{tanh^{-1}\left(\sqrt{\frac{W_0}{d_0}}\right)}{\sqrt{\frac{W_0}{d_0}}} \cdot \frac{\varepsilon_0}{d_0} \pi a^2 \quad (4)$$

Based on surface microfabrication technology, the limitation is placed on the need to limit of the air gap in order to provide some isolation between the two plates. However, silicon-on-insulator (SOI) wafers or stack up bonded wafers can offer some flexibility regarding the degree of freedom on this issued. The state of the art designs was able to maximize the air gap distance while retaining high performance that can still prevent an issue such as leakage current through the plates. It can become the potential weak point in term of electrical noise distribution. Due to the audio signal quality requirement, most audio devices are required to be as noise-free as possible. MEMS-based microphone can be used to achieve higher level clarity with SNR appropriate for the high-performance audio system. Therefore, the method of predicting a capacitance value which related to the properties of poly-Si membrane, especially film stress, is the way to obtain higher SNR for MEMS-based capacitive microphone.

In this paper, the effects of an annealing temperature on the electrical properties of MEMS-based capacitive microphone with poly-Si membrane were studied. Furthermore, the effects of annealing temperature on the residual stress in poly-Si membrane will be also investigated.

II. METHODOLOGY

The capacitive type MEMS microphone devices have two main elements, one is a moving part and the other is a rigid backplate. The membrane is used to detect acoustic pressure causing membrane deflection that will induce the electric field from the backplate and cause charge transfer. The change transfer represents audio signal. In this paper, the Finite Element Method (FEM) in Solidwork Solver software is used to predict the behavior and performance of MEMS capacitive microphone devices by calculate the deflection of circular membrane and thereby calculating capacitance value as a function of membrane diameter and applied sound pressure using Eq. 1 to Eq. 4. In FEM modeling, the following input parameters of poly-Si membrane were used; Young's modulus of 160 MPa, Poisson's ratio of 0.22, tensile stress of 5 MPa, membrane thickness of 0.5 μm to 1.0 μm and the diameter of membrane was 930 μm.

Figure 1 shows the predicted membrane deflection when applied pressure of 28.5 Pa (123 decibel sound pressure level, dB-SPL), which is referred to an acoustic overload point (AOP) in the sound pressure level to prevent the membrane collapsed to the back plate. The device shown the best performance when the thickness of poly-Si membrane is 0.8 μm. The membrane deflection has increased linearly by increasing the membrane radius. The magnitude of the maximum membrane deflection is varied with the amplitude of the incident force at maximum acoustic pressure of 123 dB-SPL. For small deflection, the membrane deflection (W_0) can be defined as,

$$W_0 = \frac{Pa^4}{64D} \quad (5)$$

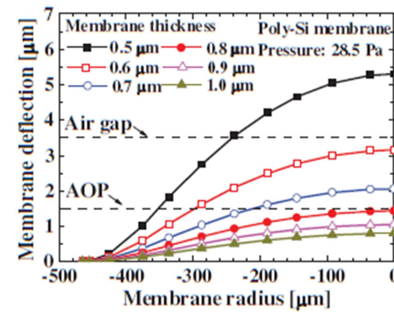

Fig. 1. Effects of poly-Si membrane thickness on the predicted membrane deflection obtained from FEM simulation when the applied pressure is 28.5 Pa.

Where a is a radius of the membrane, D is the flexural rigidity of membrane, E is Young's modulus, h is the membrane thickness, and v is Poisson's ratio [6]. The flexural rigidity of the membrane can be defined as following equation:

$$D = \frac{Eh^3}{12(1-v^2)} \quad (6)$$

Therefore, from Eq. (1) and Eq. (2), we can calculate a capacitance value of diaphragm deflection either when applying the testing pressure of 1.0 Pa, or predict the capacitance at the different surface area of the diaphragm plate [7]. Figure 2 shows the relation between membrane deflection and capacitance values. Note that, C_0 is the predicted capacitance at the initial state and C_1 is the calculated capacitance when a pressure of 1.0 Pa is applied to the poly-Si membrane.

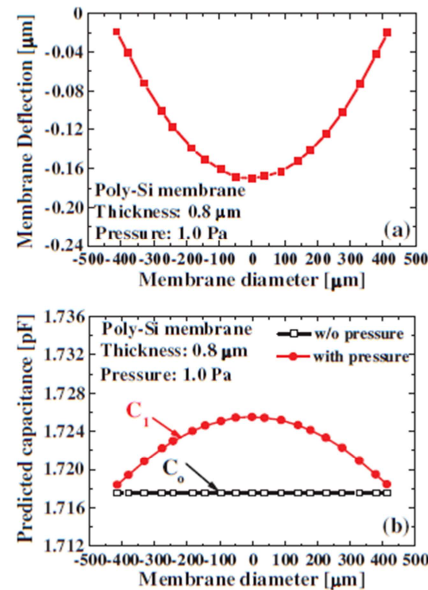

Fig. 2. The characteristics of 0.8 μm thick poly-Si membrane obtained from FEM simulation as a function of membrane diameter when the applied pressure is 1.0 Pa (a) predicted membrane deflection and (b) predicted capacitance.

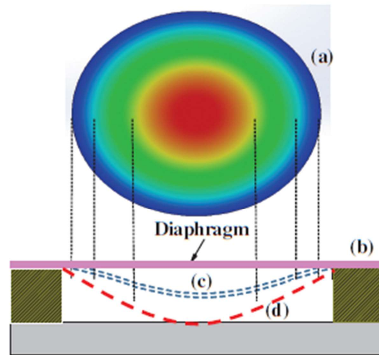

Fig. 3. The simulation results of the deflection of 0.8 µm thick poly-Si membrane. (a) FEM contour image of the deflected membrane, (b) Initial state of the membrane, (c) Deflected membrane at linear region, and (d) Collapsed membrane that contact to the backplate after deflection.

Figure 3 shows the result of FEM simulation as well as illustrated a cross-sectional image of various states of the membrane including the initial state in Fig. 3(b), the membrane deflection in Fig. 3(c), and the collapsed membrane in Fig 3(d). The capacitance changed with the deflected membrane can be compared to the initial capacitance value of zero deflection membrane to finding the characteristics of the device based on changing values.

III. FABRICATION PROCESS

The fabrication of the MEMS capacitive microphone can be separated into two groups. The first group is to create the device wafer, on which the membrane will be fabricated. The second group is the fabrication of the back plate wafer, where the shape of the cavity will be created. These two wafers will then be bonded together. The summary of the process flow is shown in Fig. 4. Only the fabrication of interest will be on the device wafer group. The starting n-Si(100) wafer is used as a substrate. After cleaning the Si surface, the SiO_2 layer was thermally grown to form an isolation layer between a Si substrate and the backplate wafer. Then, amorphous silicon (a-Si) film with in-situ doped phosphine was deposited by using Low-Pressure Chemical Vapor Deposition (LPCVD) method at 560°C.

After fabricated the device wafer and the cover wafer separately, those wafers will be bonded together by using direct wafer fusion bonding method including plasma activation, wafer pre-bond, high-temperature annealing, and grinding the bonded wafer [8]. The plasma activation was performed in order to formed hydrophilic property of wafer bonding surface. After pre-bonding the two wafers, they were annealed at high temperature to form the hard bonding interface. The annealing was done in N_2 gas ambient (14 SLM) at the temperature of 850°C, 900°C, and 950°C for 30 min. The process condition of the annealing process was carefully optimized to minimize film stress and sheet resistance of poly-Si membrane. The next step was to grind a bonded wafer on the cover plate side down to 15 µm thickness.

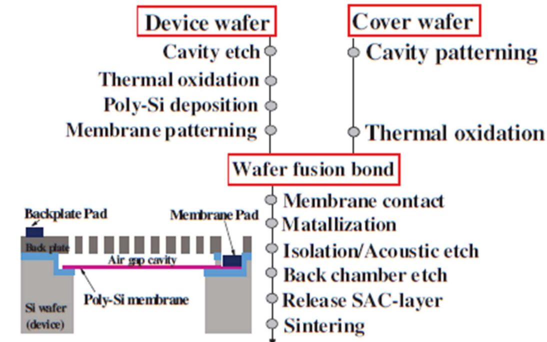

Fig. 4. Process flow of MEMS capacitive microphone fabrication and schematic cross-sectional structure of the device.

At this point, the bonded wafer was ready for further processing steps, namely, poly-Si pad opening, metallization, perforation holes etching, back chamber etching, releasing the sacrificial oxide (SAC) layer to free the membrane, and the sintering process.

IV. RESULTS AND DISCUSSION

The cross-sectional SEM images of air gap cavity and top-view scanning electron microscope (SEM) images of the MEMS-based capacitive microphone device are shown in Fig. 5 (a) and Fig. 5 (b), respectively. The capacitance-voltage (C-V) characteristic was measured by varied the bias voltage (VDC) from 2 to 40V using semiconductor device analyzer Agilent B5000A to determine the absolute capacitance and VDC.

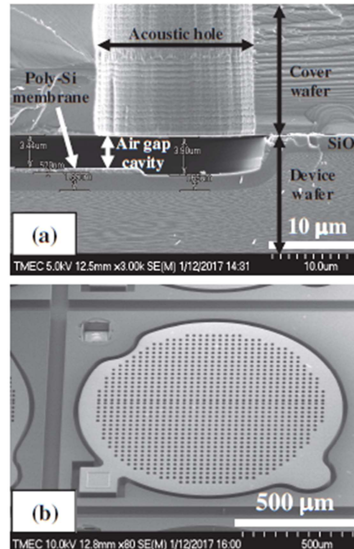

Fig. 5. SEM images of fabricated MEMS-based capacitive microphone device. (a) Cross-sectional view of air gap cavity and (b) Top-view of the device.

Note that the actual thickness of poly-Si membrane is 0.53 µm, which is thinner than the design due the film shrinkage after high temperature annealing process. The C-V characteristics of MEMS-based capacitive microphone that annealed in N_2 ambient (14 SLM) at 850°C/30 min and 950°C/30 min are shown in Fig. 6. In case of the device with lower annealing temperature of 850°C/30 min, the capacitance of 5 different devices (L1, L2, L3, L4, and L5) called L-group devices were measured. It was founded that the variation of absolute capacitance of L-group devices are in the range of few picofarad (pF) when the bias voltage was varied from 2 V to 8 V. All the devices in L-group have a capacitance value higher than that of theoretically calculated capacitance value, which is equal to 2.0 pF. In addition, the C-V characteristics showed low pull-in voltage of 4.0 V and exhibited large variation of capacitance value.

In case of the devices with higher annealing temperature of 950°C/30 min, the capacitance of 3 different devices (H1, H2, and H3) called H-group devices were measured. It was found that all the devices in H-group have an absolute capacitance value closed to the calculated value of 2.0 pF. However, the C-V characteristics showed very high pull-in voltage approximately at bias voltage of 33 V [9]. The different of pull-in voltage of the samples with different annealing condition might be related to residual compressive stress in poly-Si membrane. Lower annealing temperature of 850°C/30 min generated higher residual compressive stress in poly-Si membrane compared to the higher annealing temperature of 950°C/30 min. However, poly-Si membrane with higher annealing temperature of 950°C/30 min has higher pull-in voltage compared to the membrane with lower annealing temperature. Therefore, the annealing condition should be further optimized to trade-off between the residual stress, the capacitance value, and the pull-in voltage of the devices.

Figure 7 showed the C-V characteristic of MEM-based capacitive microphone with 0.53 µm thick poly-Si membrane annealed in N_2 ambient (14 SLM) at 900°C/30 min. It was found that the absolute capacitance value is closed to the calculated value of 2.0 pF when the bias voltage is in the range of 1 to 12 V. The pull-in voltage is significantly decreased from 33 V to 12 V by increased the annealing temperature from 850°C/30 min to 900°C/30 min due to the reducing of tensile stress in membrane.

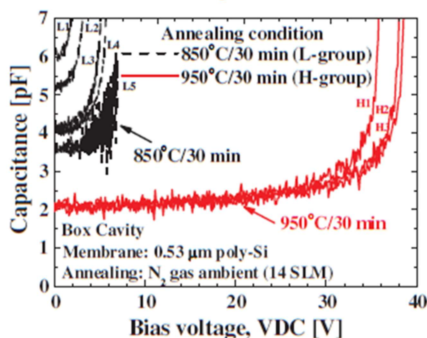

Fig. 6. C-V characteristics of MEMS-based capacitive microphone with box cavity and 0.53 µm thick poly-Si membrane annealed in N_2 gas ambient (14 SLM) at 850°C/30 min (L-group) and 950°C/30 min (H-group).

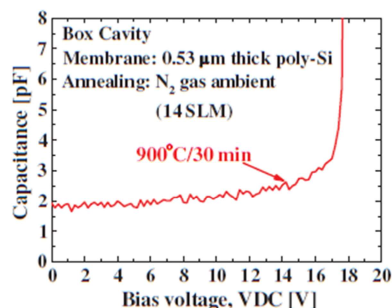

Fig. 7. C-V characteristic of MEMS-based capacitive microphone with 0.53 µm thick poly-Si membrane annealed in N_2 gas ambient (14 SLM) at 900°C/30 min.

It can be concluded that the annealing process at 900°C/30 min is the suitable condition to obtained high qualities poly-Si membrane with near zero residual tensile stress, which is able to be further applied for MEMS-based capacitive microphone.

V. CONCLUSIONS

The annealing process after pre-bonding device wafer and cover wafer is one of the most important parameters to the qualities of poly-Si membrane for MEMS-based capacitive microphone. By annealed the 0.53 µm thick poly-Si membrane in N_2 ambient at 900°C/30 min, the capacitance of 2.0 pF and the pull-in voltage of 12 V were obtained. The improvement of electrical properties of device is due to the reducing of residual stress in poly-Si membrane by the annealing process.

ACKNOWLEDGMENT

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Fabrication of Contour Cavity using Multi-exposure Lithography for MEMS Capacitive Microphone

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Abstract— **This paper presents a novel technique to optimize a capacitive pressure sensor with multi-exposure dose lithography. As part of achieving high signal to noise ratio (SNR) in microphone, a new design was implemented. The new design defies the conventional wisdom of parallel plate theory and implement a concept of contour cavity (backplate) to follows the diaphragm deflection. This 3-dimensional contour cavity (CC) is fabricated by multi-exposure dose lithography with single silicon etching process. The CC structure with different etched depth of 0.65, 1.15, and 1.57 micron were fabricated by multi-exposure dose of 92, 120, and 210 mJ/cm² on 5.0 micron thick photoresist and single step etching with CF_4/O_2 plasma (Si/PR etch selectivity: 1.3). Due to this novel contour cavity design, polysilicon membrane with 0.8 micron thick and a diameter of 930 micron structure produces the capacitance value of 2.88 pF, which is 28.6% higher than that of conventional parallel plate capacitive sensor.**

Keywords—3-D lithography, Box cavity, Contour cavity, Membrane, MEMS capacitive microphone, Multi-exposure, Silicon microphone

I. Introduction

Since early 1980s, semiconductor based capacitive pressure sensor has been widely accepted and used in number of industries. In early 2000, a variant of capacitive sensor capable of measuring sound pressure (microphone) entered the consumer markets of mobile phone industry in high volume. This microphone is generally described as MEMS (Micro Electro Mechanical Systems) microphone or Silicon microphone. Nevertheless, of naming convention, typical capacitive microphone currently roaming around in the market construed with two parallel plates and the plates are isolated by a thin airgap in the range of few microns. One of the plate is fixed plate and another plate is a moving plate or sensing plate, which is a thin diaphragm. The basic operational principle of the microphone is such that while the electrodes are biased, a sound wave, in the range of 20 Hz to 20 KHz frequency applied to the diaphragm. The diaphragm then oscillates and thereby changing the distance between plates. This, in turn, modulates the electrostatic force formed between both plates. This modulated force converts the sound wave into an electrical signal. Since the first introduction of the microphone into to mobile phone application, the demand for quality and performance has always been on the rise. Signal to noise ratio (SNR) is most favored performance. Major customers using SNR as a driving force to improve the quality of the microphone. In microphone, noise is generated in sensor, pre-amplifier, and packaging. In the past few years, the improvement of SNR obtained by using few approaches that are low noise Op-Amp with positive feedback signal [1], optimize the fabrication process to compensate the process tolerances and packaging induced stress between membrane and backplate [2]. Regardless of all these above-mentioned improvement, current state of the art microphones can only offer maximum SNR of -66 dB in commercial mass volume market. Therefore, a breakthrough needed to further advance the SNR. This requires an out of box thinking. The same out of box thinking led to this new innovative novel idea of contour cavity design from box cavity (Fig. 1).

II. Contour Cavity Concept

To improve the SNR performance of MEMS capacitive pressure sensor, two of the most important output parameters should be tackled carefully and these are sensitivity and acoustic noise. For an example, to improve acoustic noise in the sensor the following parameters should be furnished to the need. The gap between plates should be higher, larger number of acoustic holes and larger isolation between plates. However, sensitivity and acoustic noise are interdependent functions and many of the input parameters influence them are in opposite sides. For an example, shallow cavity gives a better sensitivity but give a false hope on noise. It increases the noise. Therefore, a compromise approach, a 3-dimensional (3-D) contour cavity (CC) design invented [3] in order to reduce the impact of these conflicting input parameters

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one on another and, yet, achieve the optimum performance. The CC allows maximum displacement at the center of the membrane while narrowing the distance in air gap toward clamped edges. Whereas, the displacement of the membrane on the conventional air gap structure called box cavity (BC) backplate limits the capacitance value due to larger gap toward clamped edges. Therefore, the concept of 3-D CC, which the air gap distance between the deflected membrane and the CC backplate is constant across the diameter of membrane, is introduced [4].

III. CONTOUR CAVITY DESIGN

Contour cavity backplate design expressing basic theory of capacitance and its application to pressure sensing. The capacitance value between these plates will change according to the level of deflection. Its reference capacitance without applied pressure can be defined as

$$C_0 = \frac{\varepsilon A}{d} \tag{1}$$

Where, C_0 is an initial absolute capacitance value, ε is a relative vacuum permittivity, A is the surface area of the plate and d is the gap between the two plates.

When sound pressure is applied to a flexible changing the air gap between two plates, it changes the overall capacitance value, C_1 . It can be defined by the following equation:

$$C_1 = \int_0^{2\pi} \frac{\varepsilon_0 r}{d0 - W_0\left[1-\left(\frac{r}{a}\right)^2\right]^2} \tag{2}$$

Where, C_1 is the changing capacitance when the applied pressure causing the diaphragm deflection (W_0). Therefore, In-plane deflection membrane.

$$C = \frac{tan^{-1}\left(\sqrt{\frac{W_0}{d_0}}\right)}{\sqrt{\frac{W_0}{d_0}}} \cdot \frac{\varepsilon_0}{d_0}\pi a^2 \tag{3}$$

The opposite side

$$C = \frac{tanh^{-1}\left(\sqrt{\frac{W_0}{d_0}}\right)}{\sqrt{\frac{W_0}{d_0}}} \cdot \frac{\varepsilon_0}{d_0}\pi a^2 \tag{4}$$

The cross-sectional view of capacitive microphone with conventional box cavity and 3-D CC is shown in Fig. 1 (a) and Fig. 1 (b), respectively. In this paper, the Finite Element Method (FEM) in Solidwork Solver software [5] is used to design 3-D CC backplate by calculating the deflection of circular membrane and thereby calculating capacitance value as a function of membrane diameter and applied sound pressure using Eq. 1 to Eq. 4. For FEM modeling, The following input parameters of polysilicon were used; Young's modulus of 160 MPa, Poisson's ratio of 0.22, tensile stress of 5 MPa, and membrane thickness of 0.8 μm and the diameter of membrane was 930 μm. Note that, the applied sound pressure was varied at 1.0, 28.5, and 63.2 Pa. Figure 2 shows the effects of sound-

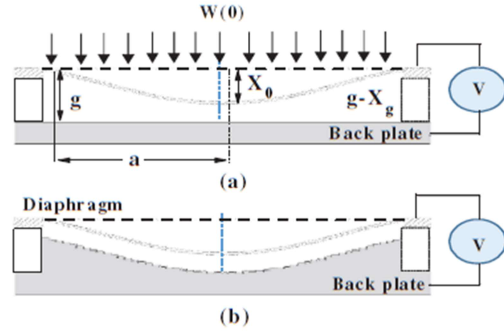

Fig. 1. Capacitive microphone with different back plate and cavity structure (a) Conventional box cavity (b) 3-D contour cavity.

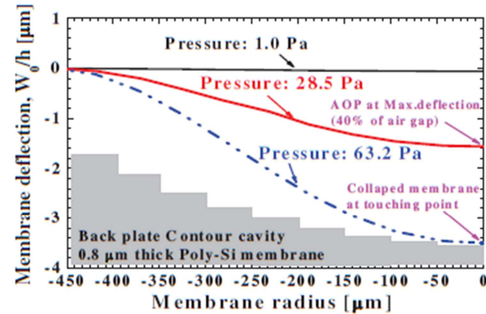

Fig. 2. Effects of sound pressure on the membrane deflection at different position of poly-Si membrane calculated by FEM model.

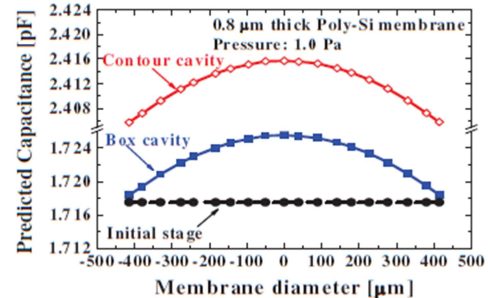

Fig. 3. Effects of the cavity structure on the predicted capacitance of 0.8 micron thick poly-Si membrane when applied the pressure of 1.0 Pa.

pressure on the membrane deflection at different position of poly-Si membrane calculated by FEM model [4]. It was found that the maximum deflection distance has occurred at the center of the membrane. When the pressure of 28.5 Pa maximum operating range was applied, the center of membrane was deflected around 1.568 μm from the base line. This position is maximum deflection which is equal to 40% of total air gap distance between two parallel plates to maintain the distance between deflection membrane and CC. The membrane was collapsed or touching to the cavity with the maximum air gap of 3.5 μm when the

pressure of 63.2 Pa burst pressure was applied. Note that, the membrane deflection is parallel to the CC structure across the membrane radius. The results in Fig. 3 showed that the capacitance of the 0.8 μm thick poly-Si membrane with the diameter of 930 μm at the initial stage (C_0) is 1.718 pF. By applying the pressure of 1.0 Pa, the BC and CC structures showed C_0 of 1.718 pF and 2.406 pF, respectively. The maximum capacitance of BC and CC structures are 1.724 pF and 2.414 pF, respectively. This means, the maximum capacitance of CC structure is 28.6% higher than that of the microphone with BC structure.

IV. SINGLE MASK LITHOGRAPHY AND FABRICATION

By using the grey-scale lithography (GSL), the curvy profile 3-D structure of CC can be formed in one lithography step and single etch step. Despite its advantages, the GSL mask is expensive and relatively difficult to fabricate [6]. However, on the hand, to achieve similar result at reduced cost, a patterning process called multi-exposure dose lithography was invented [6]. The concept of this patterning process is by varying exposure dose in multiple lithography steps on the same binary intensity mask (BIM) with only single etch step. This tends to offer more economical fabrication process for making capacitive pressure sensor with 3-D CC structure.

A. Fabrication of 3-D Contour Cavity Back Plate

A 3-D contour cavity that comprises of three different height of silicon-etched surface can be fabricated using a multi-exposure dose lithography by varying the exposure dose (E) across the area coated with the uniform photoresist (PR) film. The exposed PR is then developed and etched in a single step to form 3-D CC structure as the process steps shown in Fig. 4. The PR absorption during the exposure and its dissolution mechanism in the development step is most important input factors to the multi-exposure dose lithography, which is extensively adopted for 3-D CC structure design.

By changing the UV light intensity, the light energy that penetrates through the thickness of photoresist film was rendered according to Beer's law as shown in Eq. 5.

$$I_z = I_s e^{-\alpha z} \quad (5)$$

Where I_z is the light intensity at the target depth z, I_s is the intensity of incident light at the top surface of target, and α is the coefficient of light absorption, which can be determined from Dill's ABC parameters of PR.

In this experiment, Sumotomo PFI27C9 positive PR with the thickness of 5.0 micron was spin coated on 6-inch Si wafer using TEL track model-1. The soft-bake was done using hotplate at 110°C/3 min. The exposure dose was varied from 25 to 225 mJ/cm^2 with steps of 25 mJ/cm^2. After exposure, developed the photoresist with 2.38% tetra methyl ammonium hydroxide (TMAH) developer SD-W for 2 min. Then, rinse in DI water for 1 min and dry spin for 30 secs. The hardbake was done using hotplate at 180°C/3 min. The thickness of the remained PR film is then measured using a Tencor-P10 step profilometer. Then etched the wafer with a Reactive Ion Etch (RIE) tool (AMAT P5000) under base pressure of 200 mTorr and RF power of

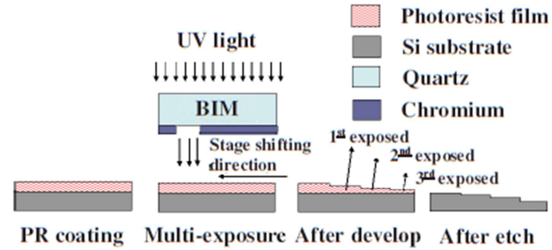

Fig. 4. A fabrication of a 3-D contour cavity using the BIM with multi-exposure dose lithography and a single-etching process step.

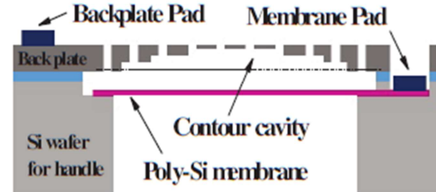

Fig. 5. Schematic cross-sectional structure of MEMS-based capacitive microphone with 3-D contour cavity.

700 W/1 min. The CF_4 gas flow rate was fixed at 55 sccm and the O_2 gas flow rate was varied at 4, 7, 10, and 16 sccm. The remained photoresist film thickness was also measured after silicon etching to define the etch selectivity between Si and PR. Later remained PR film was removed by O_2 plasma ashing and Piranha acid solution. The Si etch depth was measured to determine the Si etching rate.

B. Fabrication of Capacitive Microphone

The structure and process flow of MEMS capacitive microphone that comprises of handle wafer and cover is shown in Fig. 5. Firstly, the cavity was formed on handle wafer by etching process. Then, the SiO_2 film was grown by thermal oxidation followed by poly-Si membrane deposition utilizing low-pressure chemical vapor deposition (LPCVD) method. Later that the poly-Si membrane was patterned by lithography and etching processes. The CC structure was formed on cover wafer by multi-exposure dose and single etching process. After oxidation of cover wafer, the handle wafer was bonded together with cover wafer by fusion bonding method and grind down to 15 μm. Then contact pad was patterned and etched and aluminum was deposited and patterned. [7]

V. RESULTS AND DISCUSSION

To fabricate the CC structure with three different cavity heights of 0.5 μm (C1), 1.0 μm (C2), and 1.5 μm (C3) that can maintain the parallel air gap distance between CC and membrane across the membrane diameter, the condition of multi-exposure dose lithography and etch selectivity between PR and Si should be optimized. The profile of the multi-dose exposed PR after developed is step-like. The thinner remained PR film at a different location is corresponding to higher exposure dose exposed on the film. The relation between the exposure dose and the PR film thickness is shown in Fig. 6.

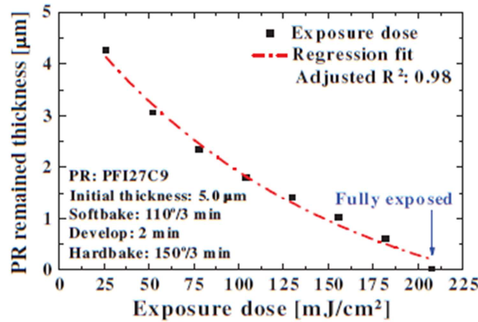

Fig. 6. Effects of exposure dose on the photoresist remained thickness after developed.

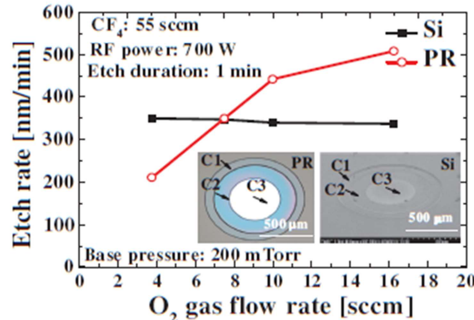

Fig. 7. Effects of O_2 gas flow rate in CF_4/O_2 plasma on the etch rate of silicon and photoresist.

At the exposure dose level of 208 mJ/cm^2, complete film of photoresist can be thoroughly developed off the wafer. The exposure dose of 92, 120, and 210 mJ/cm^2 is required to fabricate C1, C2, and C3 Si-etched depth. The results in Fig. 7 shown that the etch rate of PR and Si is depended on the CF_4/O_2 gas flow ratio. To fabricate the 3-D CC structure, the etch rate of PR must be higher than Si. This means, CF_4/O_2 gas flow ratio of 55/10 and 55/16 sccm is suitable condition. However, the etch uniformity across wafer has decreased by increased the O_2 gas flow rate. Therefore, the CF_4/O_2 gas flow ratio of 55/10 sccm with the etch selectivity between PR and Si of 1.3 is the most suitable condition. The Si etch depth of CC structure at C1, C2, and C3 positions are 0.65, 1.15, and 1.57 µm, respectively. Note that, the uniformity of PR remained thickness and Si etch depth measured at 9 different CC positions of C1, C2, and C3 are 4.51%, 3.35%, 2.16% and 4.39%, 3.12%, 1.92%, respectively. The capacitance-voltage (C-V) characteristics of the devices with BC and CC structure were measured by varied the V_g from 2 to 20 V using semiconductor device analyzer Agilent B5000A.

The results in Fig. 8 show C-V characteristics of the device. After annealed the poly-Si membrane in N_2 ambient at 900°C/30 min (14 SLM), the obtained capacitance of BC and CC structure are 2.22 and 2.88 pF, respectively whereas the pull-in voltage of both devices is between 8 to 12 V [8]. It can be concluded that CC structure improve the performance of the device by increased the capacitance value of 28.6% higher than that of conventional BC structure.

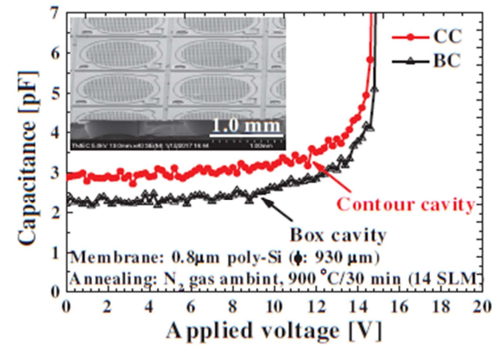

Fig. 8. C-V characteristics of MEMS-based capacitive microphone with box cavity and contour cavity structures.

VI. CONCLUSIONS

The capacitive microphone with the 3-D CC structure with three different Si-etched levels was successfully fabricated by using multi-exposure dose lithography and single etch process. The performance of the device with CC structure was significantly improved comparing to conventional BC structure. This is due to well maintain the constant air gap distance between membrane and CC structure across the membrane diameter. Further characterization is continuing for SNR and will be published in future.

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