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วงจรซีมอสลดทอนสัญญาณช่วงความถี่กว้าง

Ultra-Wideband CMOS Attenuator

ทุนวิจัยภายใต้บันทึกข้อตกลงความร่วมมือ รหัสโครงการ KREF156203

คณะผู้วิจัย

หัวหน้าโครงการ นายฉัตรพล ภคศิริ

ผู้ร่วมวิจัย นาย Sen Wang

นาย Fu-Sheng Zhu

ได้รับการสนับสนุนเงินวิจัยจาก กองทุนวิจัย ประจำปี พ.ศ. 2562

วิทยาลัยนวัตกรรมการผลิตขั้นสูง

สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง

บทคัดย่อ

ในปัจจุบันอุปกรณ์ไร้สายได้เข้ามามีบทบาทในชีวิตประจำวัน วงจรสำหรับการส่งสัญญาณไร้สายจึงจำเป็นต้องมีการพัฒนาเพื่อเพิ่มประสิทธิภาพ ในวงจรด้านรับสัญญาณ วงจรลดทอนสัญญาณเป็นวงจรสำคัญในการควบคุมสัญญาณที่เข้ามาให้มีขนาดที่เหมาะสมเพื่อไม่ให้สัญญาณที่แรงจนเกินไปทำให้วงจรอื่นๆเสียหาย วงจรลดทอนสัญญาณในโครงการนี้จะศึกษาวงจรลดทอนสัญญาณแบบช่วงความถี่กว้าง (ultra-wideband) สำหรับการลดทอนสัญญาณจะความคุมโดยใช้ตัวเลขแบบดิจิตอลจำนวน 4 บิท ซึ่งสร้างบนพื้นฐานกระบวนการซีมอสแบบ 0.18μm โครงสร้างของวงจรเป็นแบบตัว T ซึ่งแต่ละบิทจะมีคุณสมบัติในการลดทอนสัญญาณที่ต่างกัน วงจรได้ถูกออกแบบโดยใช้ค่าที่เหมาะสมในการจัดเรียงลำดับของแต่ละบิทเพื่อให้มีประสิทธิภาพทางด้านความสูญเสียสัญญาณน้อย มีความทนทานต่อสัญญาณแรง ($P_{1\text{-dB}}$) ค่าความผิดพลาดของแอมพลิจูดที่น้อยกว่า 0.13 dB จะอยู่ในความถี่ช่วงกว้าง 3.1 ถึง 10.8 GHz ซึ่งจะทำให้วงจรสามารถใช้งานได้หลากหลายมากขึ้น

คำสำคัญ : attenuator, CMOS, RMS amplitude error, ultra-wideband.

Research Title: Ultra-wideband CMOS attenuator

Researcher: Chatrpol Pakasiri (King Mongkut's Institute of Technology Ladkrabang)

Faculty: College of Advanced Manufacturing Innovation

Researcher: Sen Wang (National Taipei University of Technology, Taiwan)

Researcher: Fu-sheng Zhu (National Taipei University of Technology, Taiwan)

ABSTRACT

At present, wireless devices play key role in modern society. Transmitter circuits performance need to be more and more efficient. Similarly, receiver circuits are also important and needed to be improved. In receivers, attenuator circuits play key role in controlling appropriate signal level going through the circuit. If the input signal is too strong, it can damage circuits in the following blocks. In this project, the attenuator is designed for ultra-wideband application. It is controlled by a 4 digital bit circuit. Also, it was built on 0.18 μm CMOS process, which is low production cost process. The schematic is in T form. Each of the bits has different characteristics. The circuit was optimized in sequence order of the bits so that the overall performance of the attenuator is optimum, e.g., low amplitude error (less than 0.13 dB in the frequency range of 3.1 to 10.8 GHz, high $P_{1\text{-dB}}$ point. Because of the ultra-wideband character, the circuits can be applied in many applications.

Keywords : attenuator, CMOS, RMS amplitude error, ultra-wideband.

กิตติกรรมประกาศ

คณะผู้วิจัยขอขอบคุณ National Chip Implementation Center (CIC) ที่ให้การสนับสนุนในการทำวงจรรวม การวิจัยครั้งนี้ได้รับทุนสนับสนุนการวิจัยจากสถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบังผ่านทางทุนวิจัยภายใต้บันทึกข้อตกลงความร่วมมือ รหัสโครงการ KREF156203 และ จาก National Taipei University of Technology ผ่านทาง National Taipei University of Technology-King Mongkut's Institute of Technology Ladkrabang (NTUT-KMITL) Joint Research Program รหัสโครงการ NTUT-KMITL-106-02 ประจำปีงบประมาณ พ.ศ. 2562

ฉัตรพล ภคศิริ

Sen Wang

Fu-Sheng Zhu

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Chapter 1

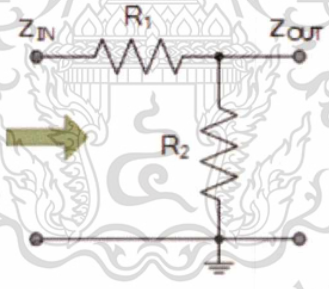
Introduction

In wireless communication, low cost circuits are normally in high demand. Therefore, most of the systems are implemented on chip as integrated circuit. At present, CMOS (Complementary metal-oxide-semiconductor) is the most popular one due to its low cost. In receiver system, an attenuator circuit plays key role in controlling signal level to be input to the receiver.

1.1 Problem background

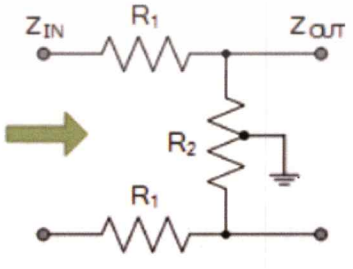
In wireless receiving circuit, a coupler circuit is a critical block in receiving signal. Once the signal is received, the attenuator circuit will maintain the input signal level such that the signal can be operated properly in the following circuit blocks. It tasks in general are attenuating the input signal and maintaining signal integrity.

Attenuators can be categorized as passive and active types. Passive attenuators mainly consist of resistors. The signal level can be lower by using proper combination of resistors. Simple attenuator structures are shown in Fig. 1 [1].



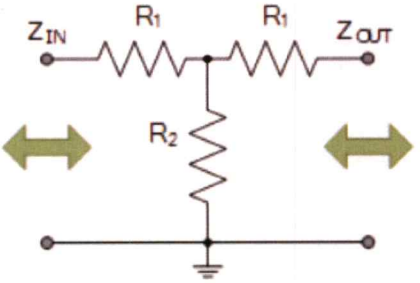
"L"-pad Configuration

(a)

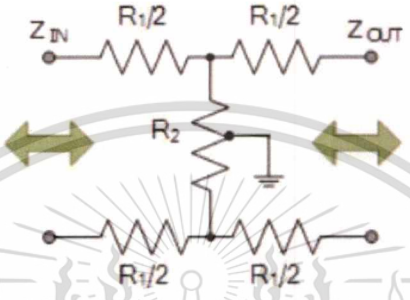


"U"-pad Configuration

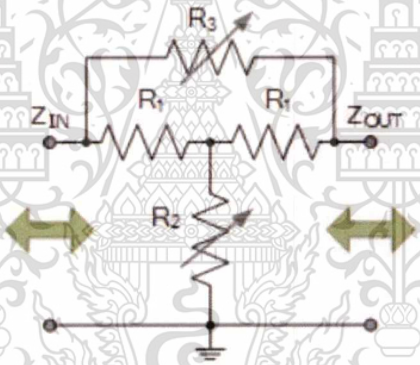
(b)



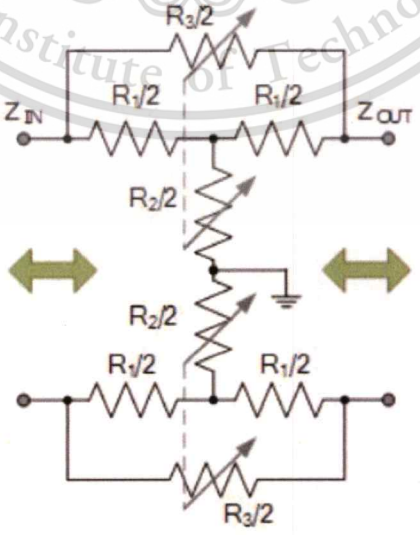
(c)



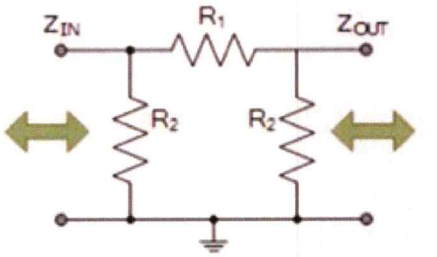
(d)



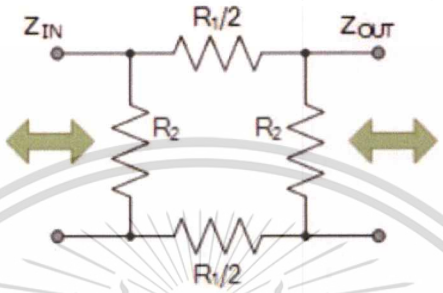
(e)



(f)



(e)



(f)

Fig.1.1 Passive attenuator configurations: (a) L-pad, (b) U-pad, (c) T-pad, (d) H-pad, (e) unbalanced bridged T (f) balanced bridged T (e) unbalanced Pi-pad (f) balanced O-pad [1]

The active attenuators use transistor in implementing passive resistors. Therefore, the topologies of the active inductors are usually the same as those of the passive attenuators. In this research, an active attenuators is proposed in T-Pad structure.

1.2 Research Purpose

To design a compact attenuator which can be used in ultra-wide microwave frequency range.

1.3 Research Scope

A CMOS circuit prototype of ultra-wideband attenuator circuit.

1.4 Methodology

Based on the passive attenuator structure, some of the circuit components such as resistors are replaced by CMOS switch. By using transistor, the circuit size is reduced. Four attenuators are combined in switched attenuator form [1] to achieve higher attenuation value. The switched attenuator topology is shown in Fig. 1.2 [1]. The attenuator level can be adjusted by choosing a combination of attenuator bits as well.

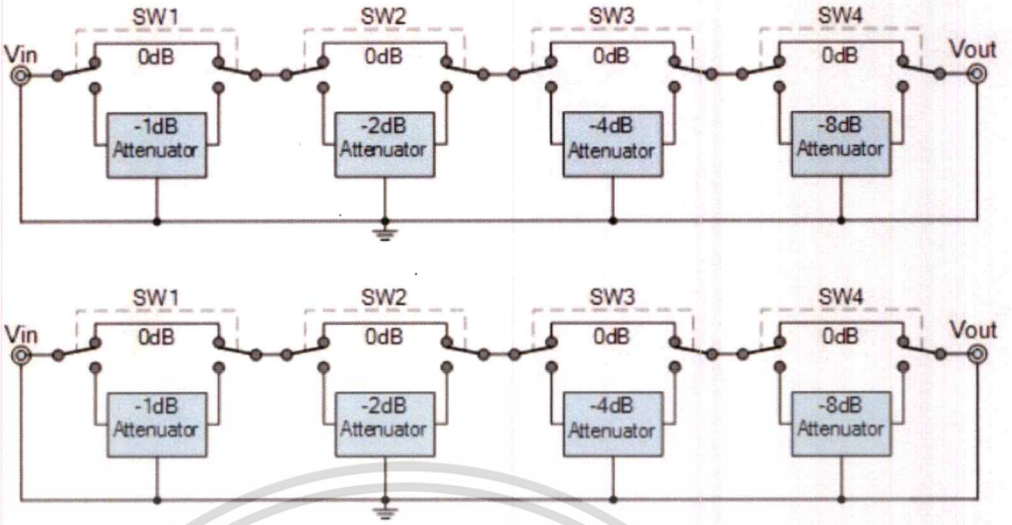


Fig. 1.2 A four bit switched attenuator topology [1].

1.5 Research Benefits

The attenuator circuit can be used in most receiver circuits and the design technique can be applied to be used in other applications as well.

This report organizes as follows: chapter 2 introduces attenuator circuits, chapter 3 shows analysis and design of attenuator circuit on CMOS process and finally chapter 4 draws conclusions.

Chapter 2

Design of the 4-Bit Digital Step Attenuator

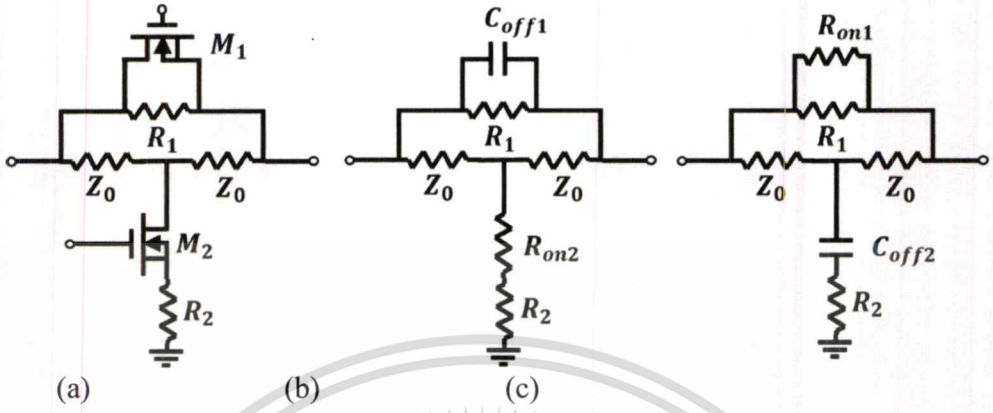
Recently, variable gain amplifiers (VGA) and power gain control designs in the transmitter/receiver (T/R) chain are commonly implemented in modern communication systems [2]-[3]. However, fully passive attenuators [4]-[7] have advantages over VGAs used in transceivers of the phased-array systems, e.g., no required DC power consumption, precise output amplitude and high linearity. In order to avoid complex phase calibration in the systems, the attenuator with series capacitors achieve a constant transmission phase [5]. Typically, the attenuators are classified as switched T/Pi type [3-4], switched bridge-T type [6], and distributed attenuators [7]. These types of the attenuators use MOS transistors to control switches on/off so that the insertion loss (attenuation amount) can be specified. The distributed attenuator has ultra-low insertion losses because no series MOS switch is used in the signal path. However, it occupies large chip area due to the implementation of distributed transmission lines [7]. The switched T/Pi type attenuators consume smaller chip area [4-5], but the parasitic effects of the MOS switch on/off control will influence the transmission phase, insertion losses, matching networks, and therefore result in poor RMS amplitude errors.

This research presents 4-bit ultra-wideband CMOS attenuator based on switched bridge-T type attenuators. The design techniques consist of the proper bit ordering arrangement to improve its insertion losses/power handling capability and small series inductors added in the RF path to broaden its input/output matching responses. Therefore, this work achieves low RMS amplitude errors in the frequency range of 3.1 GHz to 10.8 GHz.

2.1 Design of the 4-bit digital step attenuator

Figures 2.1 shows the topology of switched bridged-T type attenuator and its equivalent circuits at the attenuation state and reference state. When the transistor M_1 turns off and the transistor M_2 turns on, the attenuator presents attenuation state as shown in Fig. 2.1(b) where C_{off1} represents the off-capacitance of the series transistor M_1 and R_{on2} is on-resistance of the shunt transistor M_2. On the contrary, when M_1 turns on and M_2 turns off, the attenuator is in reference state as shown in Fig. 2.1(c) where

R_{on1} is on-resistance of the series transistor M_1, C_{off2} is the off-capacitance of the shunt transistor M_2.



(a) (b) (c)

Figure 2.1. Switched bridged attenuators: (a) switched bridged-T type attenuator, and its equivalent circuit at (b) attenuation state and (c) reference state.

$$\begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} = \begin{pmatrix} \frac{Z_0^2 + 2Z_0R_2 + R_1R_2 + R_1Z_0}{R_1(Z_0^2 + 2R_2Z_0)} & \frac{Z_0^2 + 2Z_0R_2 + R_1R_2 + R_1Z_0}{R_1(Z_0^2 + 2R_2Z_0)} \\ \frac{Z_0^2 + 2Z_0R_2 + R_1R_2 + R_1Z_0}{R_1(Z_0^2 + 2R_2Z_0)} & \frac{Z_0^2 + 2Z_0R_2 + R_1R_2 + R_1Z_0}{R_1(Z_0^2 + 2R_2Z_0)} \end{pmatrix} \quad (2.1)$$

$$S_{11} = S_{22} = (R_1(2R_2 + Z_0)) / (4R_1R_2 + 3R_1Z_0 + 4R_2Z_0 + 2Z_0^2) \quad (2)$$

$$S_{12} = S_{21} = (2R_1R_2 + 2R_1Z_0 + 4R_2Z_0 + 2Z_0^2) / (4R_1R_2 + 3R_1Z_0 + 4R_2Z_0 + 2Z_0^2) \quad (3)$$

To facilitate the theoretical analysis of the bridged-T network at attenuation state in Fig. 2.1(b), the C_{off1} and R_{on2} are neglected. Moreover, the admittance matrix (Y-matrix) is adopted in analyzing the bridged-T network by adding the admittance matrix of R_1 and the that of T-network (Z_0 and R_2) which are in parallel. The 2×2 Y-matrix of the attenuator at attenuation state is given by Equation (2.1). Then its corresponding scattering parameters can also be obtained by converting the admittance matrix to scattering matrix as expressed in Equations (2.2) and (2.3). By fixing Z_0, the values of R_1 and R_2 determine the S_{12} and S_{21}, namely, the insertion losses of the network. For the design purposes, the attenuation amounts (A) in dB and

the reference impedance can be specified. The relationships among attenuation amounts (A), the reference impedance (Z_0=50Ω), R_1, and R_2 are shown in Equations (2.4) and (2.5) [7].

$$R_1 = Z_0(10^{\frac{A}{20}} - 1) \quad (2.4)$$

$$R_2 = \frac{Z_0}{(10^{\frac{A}{20}} - 1)} \quad (2.5)$$

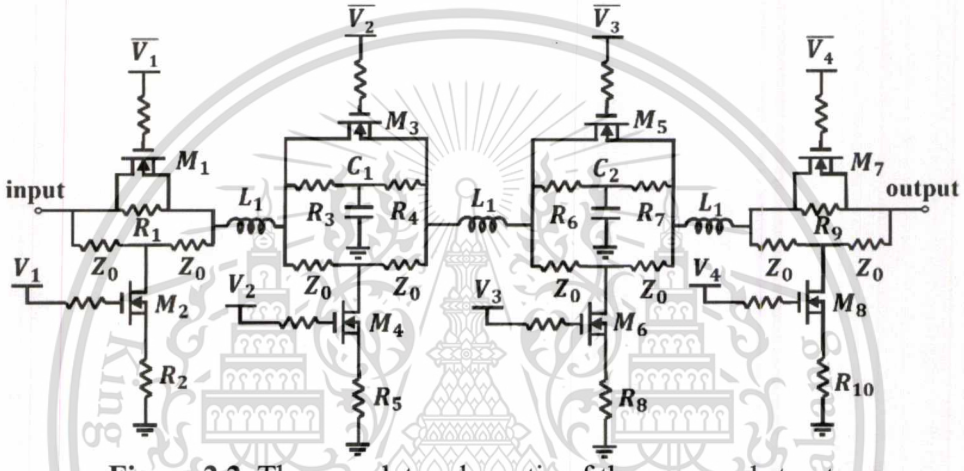


Figure 2.2. The complete schematic of the proposed structure.

Table 2.1
Component Values of the Proposed Attenuator

R_1=14Ω	R_3=18Ω	$R_{5,8}$=438Ω	R_7=24Ω	R_{10}=724Ω
R_2=2KΩ	R_4=102Ω	R_6=5Ω	R_9=13Ω	L_1=0.3nH
$M_{1,2,8}$ W/L(μm)=24/0.18		$M_{3,5,7}$ W/L(μm)=150/0.18		$M_{4,6}$ W/L(μm)=18/0.18

The bit ordering is decided by the insertion loss and input P_{1dB} considerations. Typically, lower insertion losses of the attenuator at the reference state are preferred. Moreover, to handle large input signal power, the higher attenuation bits are used at subsequent stages since they have lower power-handling capabilities due to the larger voltage difference between the drain and source of the series switch. To study lower insertion losses at the reference state, three designs of bit ordering arrangement are considered: ordering #1 (0.5-4-2-1 dB), ordering #2 (0.5-1-2-4 dB), and ordering #3

(4-2-1-0.5 dB). The design #1 and #2 use the lowest attenuator while the design #3 uses the highest attenuator for the first bit. The simulated insertion losses and input power at P_{1dB} of each type at 5 GHz can be observed in Fig. 3. From the figure, it is shown that the $|S_{21}|$of type #3 decreases most rapidly. From the insertion loss side, type #1 features lower insertion loss compared to type #2, and therefore the 0.5-4-2-1 dB ordering is adopted.

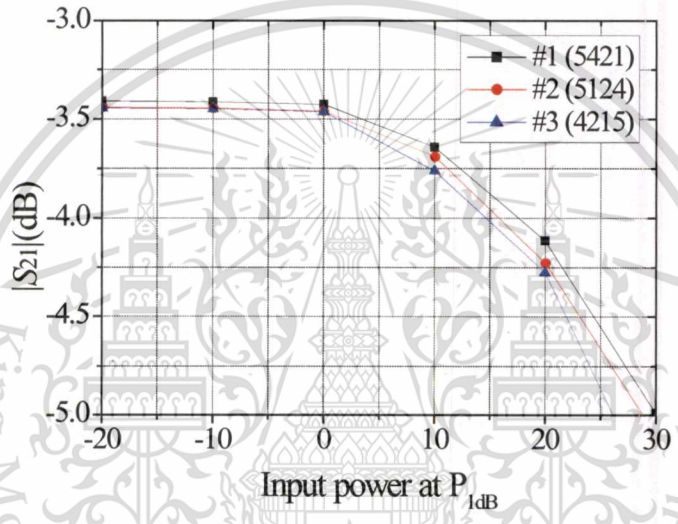


Figure 2.3. Simulated magnitude of |S21| (dB) versus input power at P_{1dB} for the reference state using different bit orderings at 5 GHz.

For a 4-bit attenuator, four switched bridged-T type attenuators from Fig. 2.1 are used. Figure 2.2 shows the complete schematic of the proposed 4-bit attenuator. Its circuit parameters are tabulated in Table 2.1. Each bit provides 0.5-dB, 1-dB, 2-dB, and 4-dB attenuation. By ignoring the impedance of the transistors, the return losses ($|S_{11}|$ and $|S_{22}|$) in Equation (2.2) are theoretically frequency-independent functions. Therefore, it is expected that wide-band responses can be achieved. However, the input and output return losses of the proposed attenuator become worsen from the assumed cases due to some parasitic effects in the RF path. In order to solve this phenomenon and take chip area of this circuit into consideration, three small 0.3-nH

inductors (L_1) are added between each bit to resonate out all the parasitic capacitances. Therefore, the return losses are improved significantly from 3 to18 GHz as shown in Fig. 2.4(a) and (b). Each line in the figure represents a state of the four switched bridged-T circuit which is a combination of reference states and attenuation states.

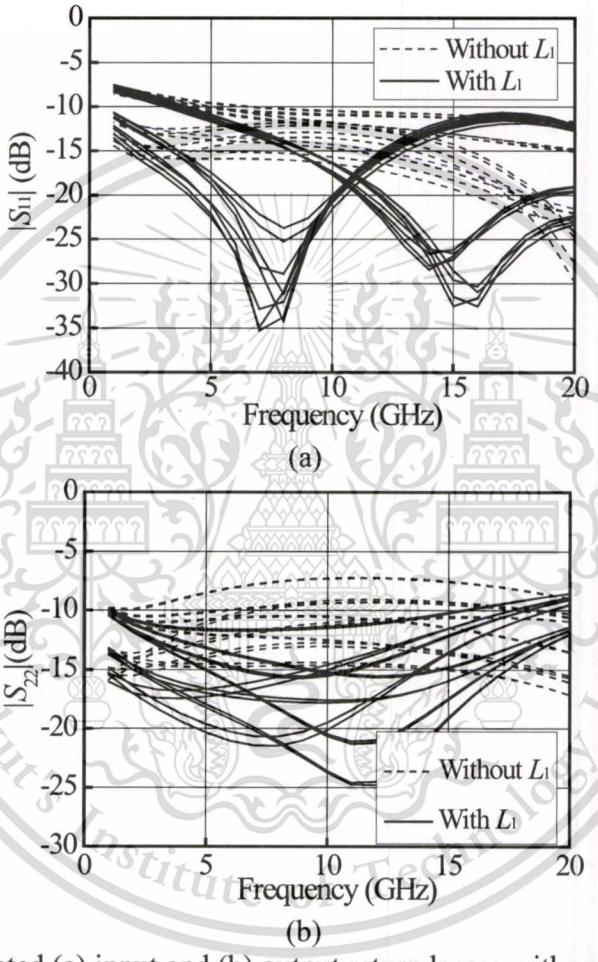


Figure 2.4. Simulated (a) input and (b) output return losses with and without L_1.

Chapter 3

Implementation and Measurement

The design is implemented in a standard mixed-signal/RF bulk 0.18-μm CMOS process which is provided by TSMC (Taiwan Semiconductor Manufacturing Company). The process provides metal-insulator-metal capacitor (MIM) capacitors and poly resistors. According to Table 2.1, some small resistances (5~24 Ω) are required, and therefore the rplpoly (P^+ Poly resistor with silicide) device is used. The large resistances are realized by the rphpoly (P^+ Poly resistor without silicide) device. To minimize resistive losses of the three series inductors L_1 in the RF path, the top metal layer made of 2.3-μm-thick AlCu is used to realize these inductors. Figure 3.1 shows the chip photo of the fabricated attenuator with a chip are of 1.2 mm^2 including all testing pads. It is noted that on-chip bypass capacitors are also added to the bias path to prevent the power noises.

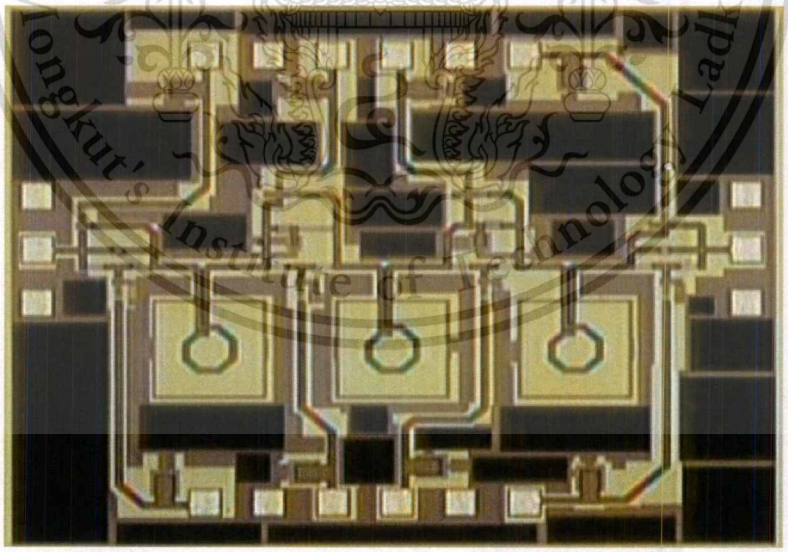


Figure 3.1. The photograph of 4-bit ultra-wideband attenuator.

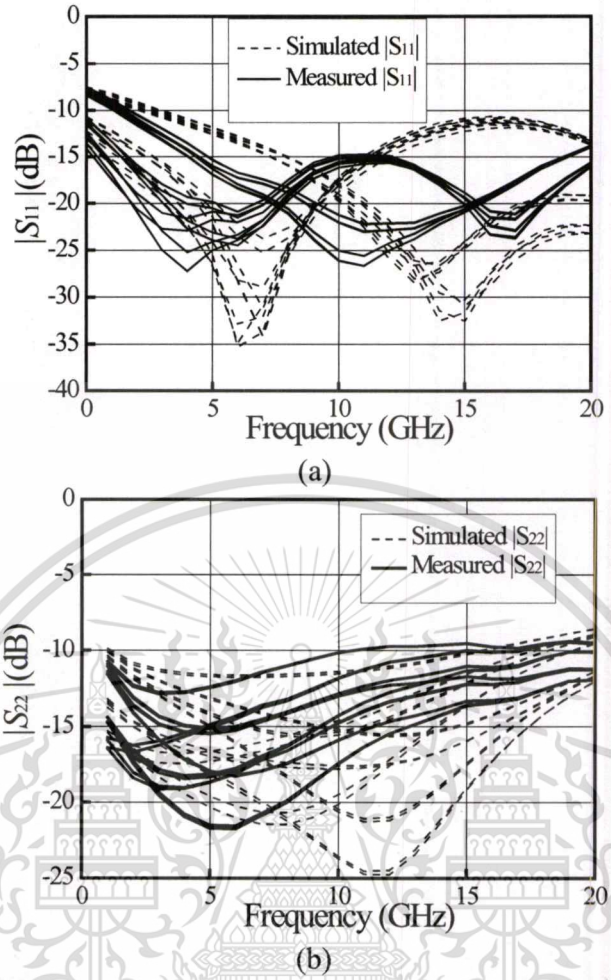


Figure 3.2. Simulated and measured results of (a) $|S_{11}|$ and (b) $|S_{22}|$.

On-wafer measurements were conducted and three groups of 3-pin (PGP) DC probe and two (GSG) RF probes were used to characterize the circuit performances. All measured results were calibrated to eliminate the undesired parasitic of the testing pads. The gate control voltage is 1.8 V. The measured $|S_{11}|$ and $|S_{22}|$ were better than 10 dB from 3.1 to 10.6 GHz as shown in Fig. 3.2(a) and Fig. 3.2(b), respectively. Note that in Fig. 6 and 7, each line in the figure represents a state of the four switched bridged-T circuit which is a combination of reference states and attenuation states. Good agreement between simulated and measured results is also demonstrated. Figure 7 presents the measured attenuation relative to that of the first state (reference state), the range of the attenuation is about 7.5 dB with 0.5 dB step (16 states) from 3.1 to 10.6 GHz. The RMS error is defined as

$$RMSE = \sqrt{\frac{\sum_{t=1}^{n}(x - x_t)^2}{n}} \tag{3.1}$$

where x is the desired attenuation step (the step of this circuit is set at 0.5 dB), x_t is the measured attenuation step between the t^{th} state and the $(t+1)^{th}$ state and n is the total number of the states. The RMS amplitude error of this design varies between 0.11 dB and 0.15 dB from 3 to 11 GHz. The measured input P_{1dB} at 5 GHz is about 15 dBm as shown in Fig. 3.3. Finally, Table 3.1 summarizes the specification of the proposed design and other previous reported digital attenuators. This work demonstrates low RMS amplitude error and insertions losses while maintains good input P_{1dB}.

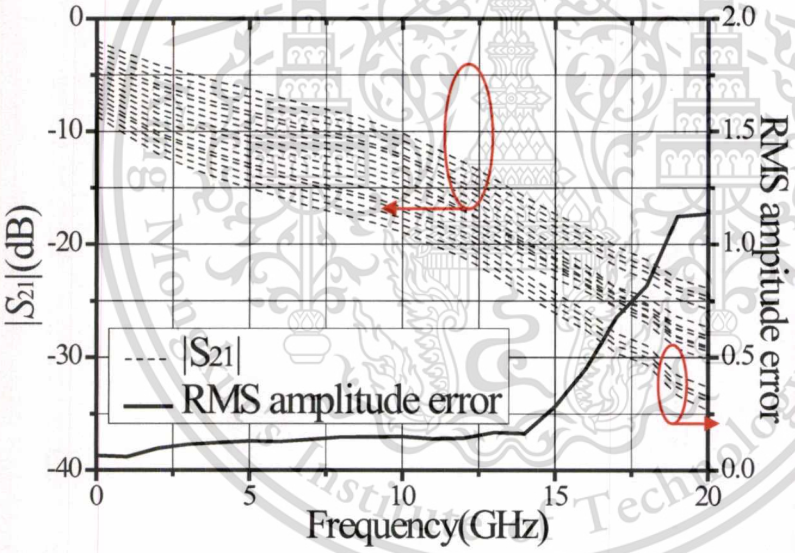


Figure 3.3. Measured results of each attenuation states and RMS amplitude errors.

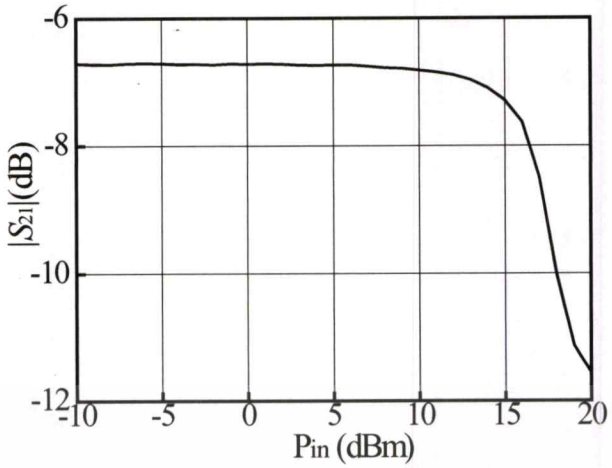


Figure 3.4. Measured input P_{1dB} at 5 GHz.

Table 3.1
Comparison of Previous Reported On-Chip Digital Attenuator

Ref.	[3]	[5]		[4]	[6]	This Work
Freq. (GHz)	7.7-10.8	8-12		36-52	10-50	3.1-10.8
Technology	0.25-μm BiCMOS	0.18-μm CMOS		0.12-μm BiCMOS	0.12-μm BiCMOS	0.18-μm CMOS
Topology	Switched Pi/T	Switched Pi/T + L	Switched Pi/T + C	Switched Pi/T	Distributed	Switched bridged T+inter-bit L
Resolution (dB)	0.13	0.5	0.5	1	3	0.5
No. of bits	7	6	6	3	4	4
R.L.(dB)	>15	>10	>11	>10	>8	>10
I.L.avg.(dB)	11.4	8.7	10.6	5.2	2.5	8.1
RMS AMP. ER. (dB)	<0.13	<0.3	<0.4	<1.4	N/A	<0.13
Input P1dB (dBm)	12.5	15	13	20	5	15

Chapter 4

Conclusions

In this paper, a 4-bit ultra-wideband attenuator is designed, implemented, and verified in a standard 0.18-μm standard CMOS process. This design adopts switched bridge-T type topology for each attenuation bit. Based on insertion losses and the input P_{1dB} considerations, the bit ordering 0.5-4-2-1 dB is employed in this design. To further improve the input/output return losses while maintains low insertion losses, three small inductors are placed between each bit in the RF signal path. Good agreement between simulated and measured results demonstrates the feasibility of the proposed design concept. In addition, this work also achieves the low RMS amplitude error and broadband response, and it could be integrated into many transceivers such as phased-array or ultra wideband systems.

Summary of outputs

C. Pakasiri, F.-S. Zhu and S. Wang "A 4-bit ultra-wideband complementary metal-oxide-semiconductor attenuator with low root-mean-square amplitude error," International Journal of RF and Microwave Computer-aided Engineering, e21922, 2019. (ISI: impact factor (2018) 1.472 Quartile 3)

บรรณานุกรม/เอกสารอ้างอิง

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ภาคผนวก ก
สรุปค่าใช้จ่ายการดำเนินโครงการวิจัย

สัญญาเลขที่ KREF156203

โครงการ วงจรกระจายสัญญาณสำหรับเครือข่ายไร้สาย

Coupler Circuit for Wireless Application

รายงานสรุปการเงินรอบ 10 เดือน

ชื่อหัวหน้าโครงการวิจัย ผู้รับทุน นาย ฉัตรพล ภคศิริ

รายงานในช่วงตั้งแต่วันที่ 1 มี.ค. 2562 ถึงวันที่ 31 ต.ค. 2562

สรุปงบประมาณค่าใช้จ่ายที่ใช้นับตั้งแต่เริ่มทำการวิจัยถึงปัจจุบัน

หมวดค่าใช้จ่าย	งบประมาณรวม ทั้งโครงการ	ค่าใช้จ่าย จากรายงานครั้งก่อน	ค่าใช้จ่าย งวดปัจจุบัน	รวมค่าใช้จ่าย สะสมถึงปัจจุบัน	คงเหลือ (หรือเกิน)
งบดำเนินงาน					
ค่าใช้สอย	275,000	218,159.85	-	218,159.85	56,840.15
ค่าวัสดุ	25,000	27,392.98	6,794.50	34,187.48	(9,187.48)
รวม	300,000	245,551.85	6,794.50	252,347.33	47,652.67

จำนวนเงินที่ได้รับและจำนวนเงินที่ใช้จ่าย

งวดเงินที่ได้รับ	จำนวนเงินที่ได้รับ(บาท)	เมื่อ (ระบุวัน เดือน ปี)
งวดที่ 1	285,000	22 มี.ค. 2562
งวดที่ 2	-	-
ดอกเบี้ย ครั้งที่ 1	180.39	25 มิ.ย. 2562
รวม	285,180.39	❶

งวดที่	จำนวนเงินที่ใช้จ่าย (บาท)	
งวดที่ 1	245,551.85	
งวดที่ 2	6,794.50	

รวม	252,347.33	❷

จำนวนเงินคงเหลือ ❶ - ❷ 32,833.06 **บาท**

ลงนามหัวหน้าโครงการวิจัยผู้รับทุนโครงการ

ลงนามเจ้าหน้าที่การเงิน

ภาคผนวก ข
ผลผลิตที่ได้จากงานวิจัย

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RESEARCH ARTICLE

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A 4-bit ultra-wideband complementary metal-oxide-semiconductor attenuator with low root-mean-square amplitude error

Chatrpol Pakasiri[1] | **Fu-Sheng Zhu**[2] | **Sen Wang**[2]

[1]College of Advanced Manufacturing Innovation, King Mongkut's Institute of Technology Ladkrabang, Ladkrabang, Bangkok, Thailand

[2]Department of Electronic Engineering, National Taipei University of Technology, Taipei, Taiwan

Correspondence
Chatrpol Pakasiri, College of Advanced Manufacturing Innovation, King Mongkut's Institute of Technology Ladkrabang, 1 Soi Chalongkrung 1, Ladkrabang, Bangkok, Thailand.
Email: chatrpol.pa@kmitl.ac.th

Sen Wang, Department of Electronic Engineering, National Taipei University of Technology, 1, Sec. 3, Chung-Hsiao E. Road, Taipei, Taiwan.
Email: wangsen@ntut.edu.tw

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Abstract

This article presents the 4-bit ultra-wideband complementary metal-oxide-semiconductor (CMOS) attenuator in a standard 0.18-μm CMOS process. This design adopts switched bridge-T type topologies for each attenuation bit. Based on insertion losses and input $P_{1\text{-dB}}$ considerations, the circuit performances can be optimized by the proper bit ordering arrangement. Therefore, the bit ordering 0.5-4-2-1 dB is employed in the 4-bit attenuator. Moreover, series inductors are added between each bit to further improve the input and output return losses. Measured results demonstrate that the attenuation range of the circuit is 7.5 dB with 0.5 dB step and the root-mean-square (RMS) amplitude error is between 0.11 and 0.13 dB from 3.1 to 10.8 GHz. The differences between simulated and measured RMS amplitude errors are less than 0.2 dB, which demonstrates the good agreement and feasibility of the design concept. The measured input $P_{1\text{-dB}}$ is 15 dBm at 5 GHz and the chip area is 1.12 mm^2 including all testing pads.

KEYWORDS
attenuator, CMOS, RMS amplitude error, ultra-wideband

1 | INTRODUCTION

Recently, variable gain amplifiers (VGA)[1,2] and power gain control designs such as power divider and combiners[3,4] in the transmitter/receiver (T/R) chain are commonly implemented in modern communication systems. However, fully passive attenuators[5,6] have advantages over VGAs used in transceivers of the phased-array systems, for example, no required DC power consumption, precise output amplitude and high linearity. In order to avoid complex phase calibration in the systems, the attenuator with series capacitors achieve a constant transmission phase.[5] Typically, the attenuators are classified as switched bridge-T type,[5] switched Pi/T type,[7,8] and distributed attenuators.[6] These types of the attenuators use metal-oxide-semiconductor (MOS) transistors to control switches on/off so that the insertion loss (attenuation amount) can be specified. The distributed attenuator has ultra-low insertion losses because no series MOS switch is used in the signal path. However, it occupies large chip area due to the implementation of distributed transmission lines. The switched T/Pi type attenuators consume smaller chip area, but the parasitic effects of the MOS switch on/off control will influence the transmission phase, insertion losses, matching networks, and therefore result in poor root-mean-square (RMS) amplitude errors.

This article presents 4-bit ultra-wideband complementary MOS (CMOS) attenuator based on switched bridge-T type attenuators. The design techniques consist of the proper bit ordering arrangement to improve its insertion losses/power handling capability and small series inductors added in the RF path to broaden its input/output matching responses. Therefore, this work achieves low RMS amplitude errors in the frequency range of 3.1 GHz to 10.8 GHz. The article is organized as follows. Section 2 provides the details of the proposed 4-bit digital step attenuator. Section 3 describes the implementation and measurement of the design. Finally, Section 4 concludes this work.

2 | DESIGN OF THE 4-BIT DIGITAL STEP ATTENUATOR

Figure 1 shows the topology of switched bridged-T type attenuator and its equivalent circuits at the attenuation state and reference state. When the transistor M_1 turns off and the transistor M_2 turns on, the attenuator presents attenuation state as shown in Figure 1B where C_{off1} represents the off-capacitance of the series transistor M_1 and R_{on2} is on-resistance of the shunt transistor M_2. On the contrary, when M_1 turns on and M_2 turns off, the attenuator is in reference state as shown in Figure 1C where R_{on1} is on-resistance of the series transistor M_1, C_{off2} is the off-capacitance of the shunt transistor M_2.

$$\begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} = \begin{pmatrix} \frac{Z_0^2+2Z_0R_2+R_1R_2+R_1Z_0}{R_1\left(Z_0^2+2R_2Z_0\right)} & -\frac{Z_0^2+2Z_0R_2+R_1R_2+R_1Z_0}{R_1\left(Z_0^2+2R_2Z_0\right)} \\ -\frac{Z_0^2+2Z_0R_2+R_1R_2+R_1Z_0}{R_1\left(Z_0^2+2R_2Z_0\right)} & \frac{Z_0^2+2Z_0R_2+R_1R_2+R_1Z_0}{R_1\left(Z_0^2+2R_2Z_0\right)} \end{pmatrix} \quad (1)$$

$$S_{11} = S_{22} = \left(R_1\left(2R_2+Z_0\right)\right) / \left(4R_1R_2+3R_1Z_0+4R_2Z_0+2Z_0^2\right) \quad (2)$$

$$S_{12} = S_{21} = \left(2R_1R_2+2R_1Z_0+4R_2Z_0+2Z_0^2\right) / \left(4R_1R_2+3R_1Z_0+4R_2Z_0+2Z_0^2\right) \quad (3)$$

To facilitate the theoretical analysis of the bridged-T network at attenuation state in Figure 1B, the C_{off1} and R_{on2} are neglected. Moreover, the admittance matrix (Y-matrix) is adopted in analyzing the bridged-T network by adding the admittance matrix of R_1 and the that of T-network (Z_0 and R_2) which are in parallel. According to the principle of Y-matrix, the Y_{11} and Y_{22} are $([(Z_0//R_2)+Z_0]+R_1)^{-1}$. On the contrary, the Y_{12} and Y_{21} are $-([(Z_0//R_2)+Z_0]+R_1)^{-1}$. The Z_0 is set to 50 Ω, which is also known as the reference impedance. So the 2 × 2 Y-matrix of the attenuator at attenuation state is given by Equation (1). Then its corresponding scattering parameters can also be obtained by converting the admittance matrix to scattering matrix as expressed in Equations (2) and (3).[9] By fixing Z_0, the values of R_1 and R_2 determine the S_{12} and S_{21}, namely, the insertion losses of the network. For the design purposes, the attenuation amounts (A) in dB and the reference impedance can be specified. The relationships among attenuation amounts (A), the reference impedance (Z_0 = 50 Ω), R_1, and R_2 are shown in Equations (4) and (5).[8]

$$R_1 = Z_0\left(10^{\frac{A}{20}}-1\right) \quad (4)$$

$$R_2 = \frac{Z_0}{\left(10^{\frac{A}{20}}-1\right)} \quad (5)$$

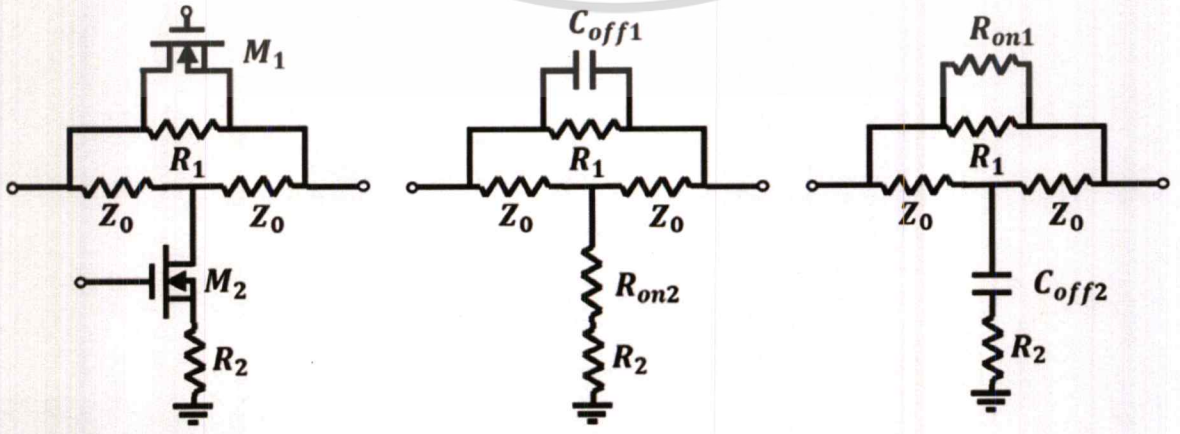

FIGURE 1 (A) Switched bridged-T type attenuator, and its equivalent circuit at (B) attenuation state and (C) reference state

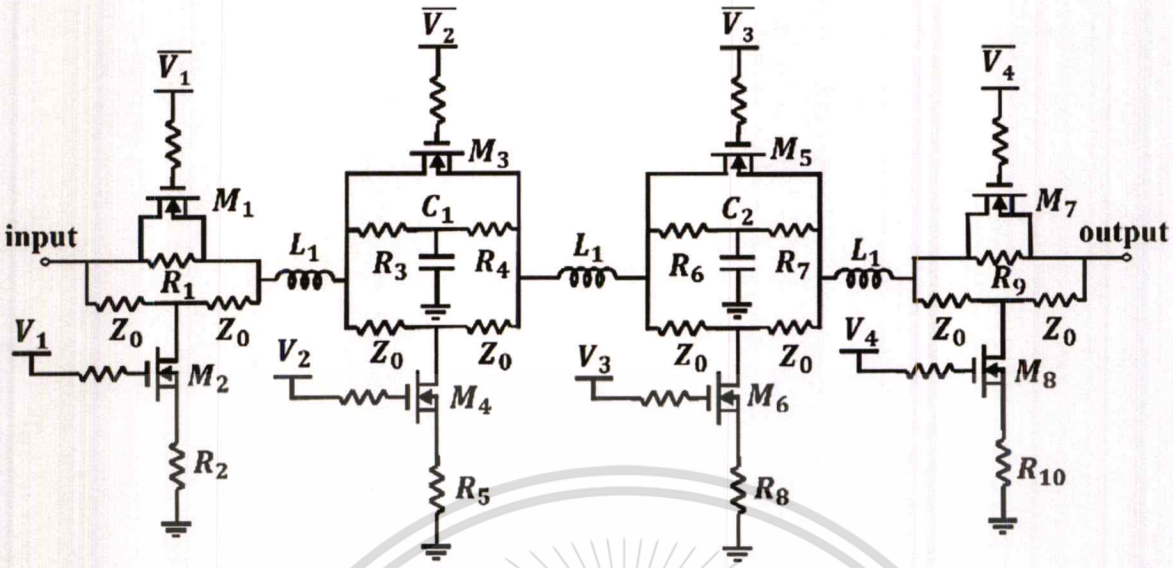

FIGURE 2 The complete schematic of the proposed structure

TABLE 1 Component values of the proposed attenuator

$R_1 = 14\ \Omega$	$R_3 = 18\ \Omega$	$R_{5,8} = 438\ \Omega$	$R_7 = 24\ \Omega$	$R_{10} = 724\ \Omega$
$R_2 = 2\text{K}\Omega$	$R_4 = 102\ \Omega$	$R_6 = 5\ \Omega$	$R_9 = 13\ \Omega$	$L_1 = 0.3\text{nH}$
$M_{1,2,8}$ W/L (μm) = 24/0.18		$M_{3,5,7}$ W/L (μm) = 150/0.18		$M_{4,6}$ W/L (μm) = 18/0.18

For a 4-bit attenuator, four switched bridged-T type attenuators from Figure 1 are used. Figure 2 shows the complete schematic of the proposed 4-bit attenuator. Its circuit parameters are tabulated in Table 1. Each bit provides 0.5-dB, 1-dB, 2-dB, and 4-dB attenuation. The bit ordering is decided by the insertion loss and input $P_{1\text{-dB}}$ considerations. The input and output return losses are not considered because they can be improved by matching networks. Typically, lower insertion losses of the attenuator at the reference state are preferred. Moreover, to handle large input signal power, the higher attenuation bits are used at subsequent stages since they have lower power-handling capabilities due to the larger voltage difference between the drain and source of the series switch. To study lower insertion losses at the reference state and loading effect, which is caused by changing different states, bit ordering arrangement examples for extreme results in insertion loss and power handling are considered. Three designs of bit ordering are arranged as follows: ordering #1 (0.5-4-2-1 dB), ordering #2 (0.5-1-2-4 dB), and ordering #3 (4-2-1-0.5 dB). The design #1 and #2 use the lowest attenuator at the first bit. They presume to have the lowest insertion loss and the highest power handling. While the design #3 is the extreme opposite that it presumes to have the highest insertion loss and lowest power handling. The simulated insertion losses and input power at $P_{1\text{-dB}}$ of each type at 5 GHz can be observed in Figure 3.

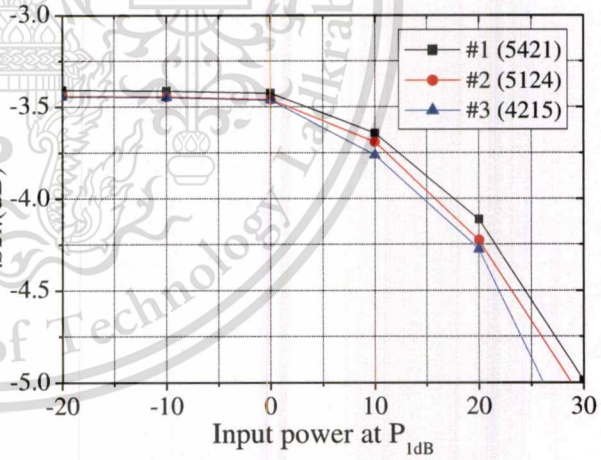

FIGURE 3 Simulated magnitude of $|S_{21}|$ (dB) vs input power at $P_{1\text{-dB}}$ for the reference state using different bit orderings at 5 GHz

From the figure, it is shown that the $|S_{21}|$ of type #3 decreases most rapidly. From the insertion loss side, type #1 features lower insertion loss compared to type #2, and therefore the 0.5-4-2-1 dB ordering is adopted.

By ignoring the impedance of the transistors, the return losses ($|S_{11}|$ and $|S_{22}|$) in Equation (2) are theoretically frequency-independent functions. Therefore, it is expected that wideband responses can be achieved. However, the

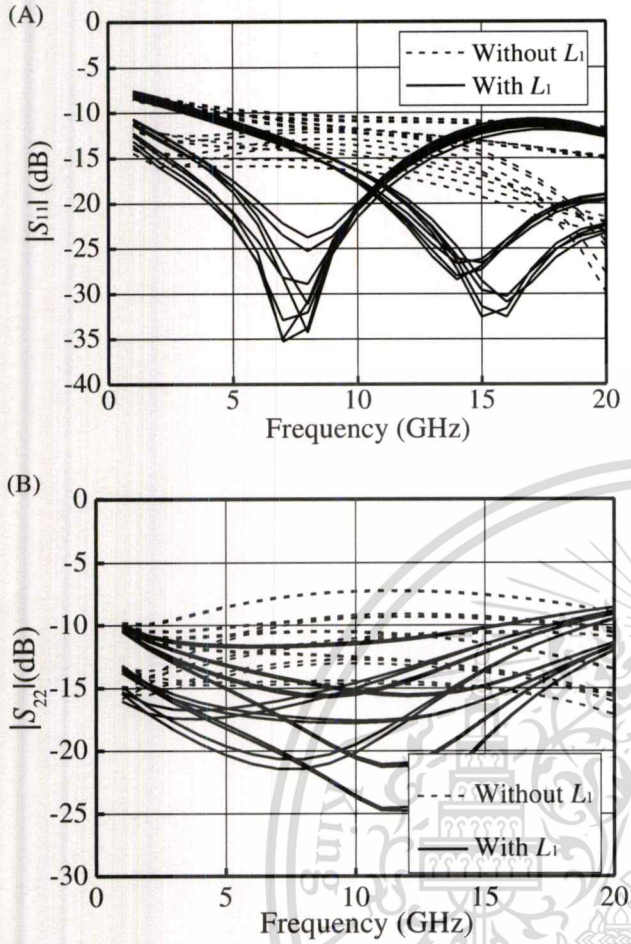

FIGURE 4 Simulated (A) input and (B) output return losses with and without L_1

input and output return losses of the proposed attenuator become worsen from the assumed cases due to some parasitic effects in the realistic circuit layout of signal lines. In order to solve this phenomenon between each bits and take chip area of this circuit into consideration, three small 0.3-nH inductors (L_1) are added between each bit to resonate out all the parasitic capacitances. Therefore, the return losses are improved significantly from 3 to18 GHz as shown in Figure 4A,B. Each line in the figure represents a state of the four switched bridged-T circuit, which is a combination of reference states and attenuation states.

3 | IMPLEMENTATION AND MEASUREMENT

The design is implemented in a standard mixed-signal/RF bulk 0.18-μm CMOS process, which is provided by TSMC (Taiwan Semiconductor Manufacturing Company). The process provides metal-insulator-metal capacitors and poly resistors. According to Table 1, some small resistances

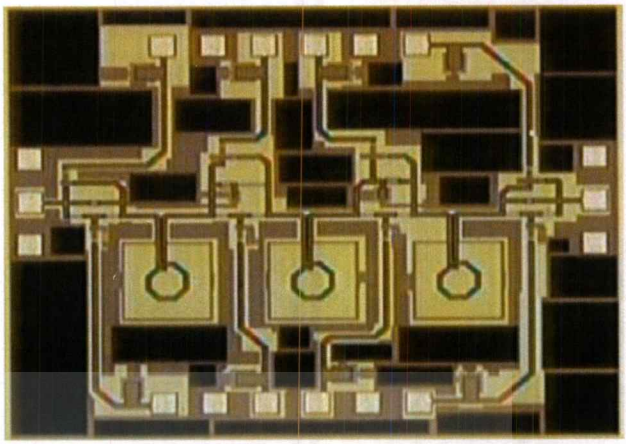

FIGURE 5 The photograph of 4-bit ultra-wideband attenuator

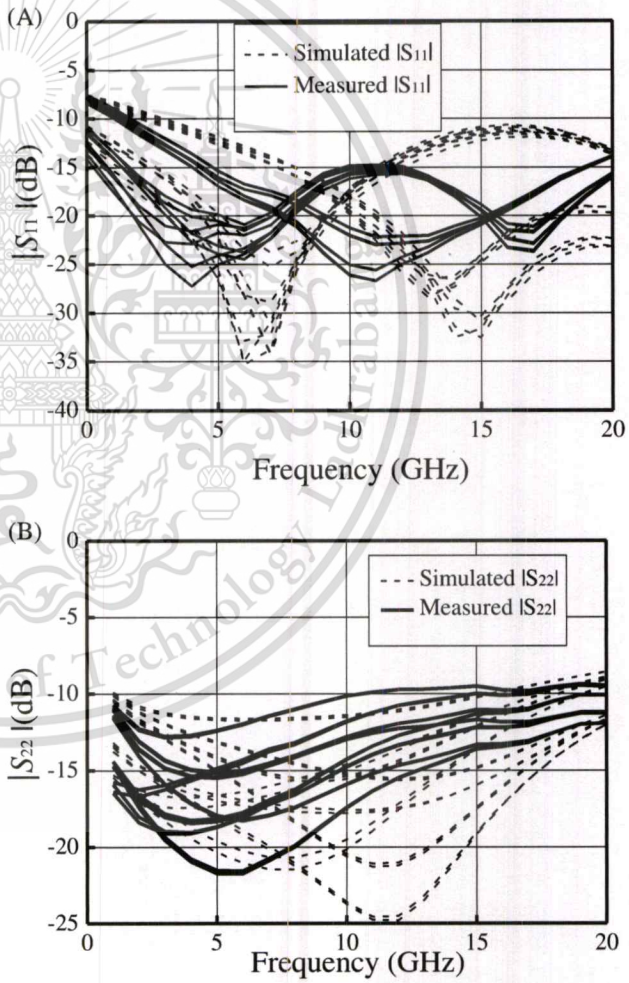

FIGURE 6 Simulated and measured results of (A) $|S_{11}|$ and (B) $|S_{22}|$

(5-24 Ω) are required, and therefore the rplpoly (P^+ poly resistor with silicide) device is used. The large resistances are realized by the rphpoly (P^+ poly resistor without silicide)

device. To minimize resistive losses of the three series inductors L_1 in the RF path, the top metal layer made of 2.3-μm-thick AlCu is used to realize these inductors. Figure 5 shows the chip photo of the fabricated attenuator with a chip are of 1.2 mm^2 including all testing pads. It is noted that on-chip bypass capacitors are also added to the bias path to prevent the power noises.

On-wafer measurements were conducted and three groups of 3-pin (PGP) DC probe and two (GSG) RF probes were used to characterize the circuit performances. All measured results were calibrated to eliminate the undesired parasitic of the testing pads. The gate control voltage is 1.8 V. The measured $|S_{11}|$ and $|S_{22}|$ were affected by the parasitic effect of the realistic circuit lines and the bulky testing pads, so the phenomenon of frequency shift occurred. But the results were still better than 10 dB from 3.1 to 10.6 GHz as shown in Figure 6A and 6B, respectively. Note that in Figures 6 and 7, each line in the figure represents a state of the four switched bridged-T circuit,

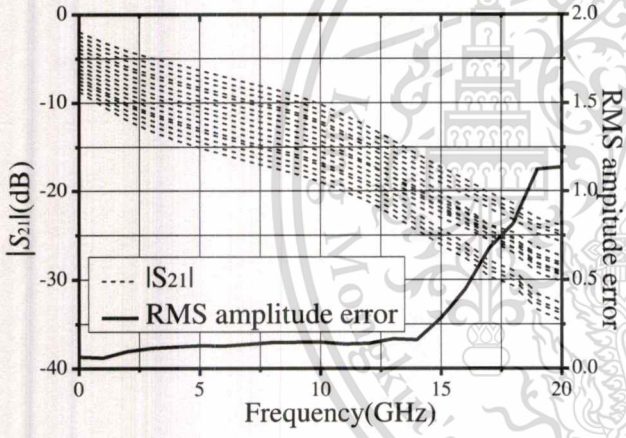

FIGURE 7 Measured results of each attenuation states and RMS amplitude errors

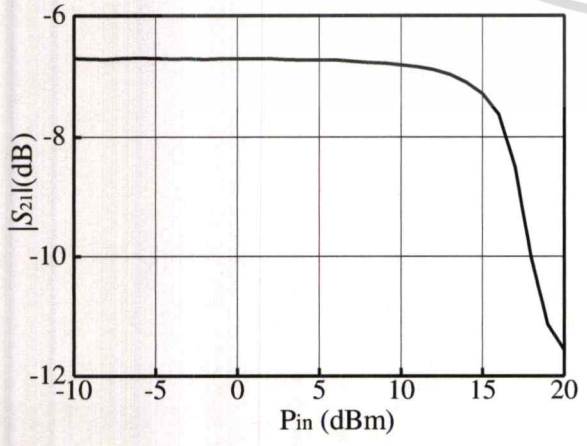

FIGURE 8 Measured input $P_{1\text{-dB}}$ at 5 GHz

TABLE 2 Comparison of previously reported on-chip digital attenuator

Ref.	7		5		8		6	This work	
Freq. (GHz)	7.7-10.8	6-12.5	8-12		36-52		10-50	3.1-10.8	
Technology	0.25-μm BiCMOS		0.18-μm CMOS		0.12-μm BiCMOS		0.12-μm BiCMOS	0.18-μm CMOS	
Topology	Switched Pi/T		Switched Pi/T + L		Switched Pi/T + C		Distributed	Switched bridged T + inter-bit L	
Resolution (dB)	0.13	0.26	0.5	0.5	0.5	1	3	0.5	
No. of bits	7	6	6	6	6	3	4	4	
R.L. (dB)	>15	>13	>10	>11	>10	>10	>8	>10	
$I.L._{avg.}$ (dB)	11.4	12.7	8.7	10.6	5.2		2.5	8.1	
RMS AMP. ER (dB)	<0.13	<0.26	<0.3	<0.4	<1.4		N/A	<0.13	
Input $P_{1\text{-dB}}$ (dBm)	12.5	12.5	15	13	20		5	15	

which is a combination of reference states and attenuation states. Good agreement between simulated and measured results is also demonstrated. Although the RMS amplitude errors in low frequencies are less than 0.2 dB, the measured results show poor return losses due to the input and output matching networks. Therefore, the practical application of this design is limited from 3.1 to 10.6 GHz. Figure 7 presents the measured attenuation relative to that of the first state (reference state), the range of the attenuation is about 7.5 dB with 0.5 dB step (16 states) from 3.1 to 10.6 GHz. The RMS error is defined as

$$\mathrm{RMSE} = \sqrt{\frac{\sum_{t=1}^{n} (x - x_t)^2}{n}} \tag{6}$$

where x is the desired attenuation step (the step of this circuit is set at 0.5 dB), x_t is the measured attenuation step between the tth state and the $(t + 1)$th state and n is the total number of the states. The RMS amplitude error of this design varies between 0.11 and 0.15 dB from 3 to 11 GHz. The measured input $P_{1\text{-dB}}$ at 5 GHz is about 15 dBm as shown in Figure 8. Finally, Table 2 summarizes the specification of the proposed design and other previously reported digital attenuators such as switched Pi/T and switched Pi/T with inductor/capacitance, and this work demonstrates low RMS amplitude errors and insertion losses while maintains good input $P_{1\text{-dB}}$.

4 | CONCLUSION

In this article, a 4-bit ultra-wideband attenuator is designed, implemented, and verified in a standard 0.18-μm standard CMOS process. This design adopts switched bridge-T type topology for each attenuation bit. Based on insertion losses and the input $P_{1\text{-dB}}$ considerations, the bit ordering 0.5-4-2-1 dB is employed in this design. To further improve the input/output return losses while maintains low insertion losses, three small inductors are placed between each bit in the RF signal path. Good agreement between simulated and measured results demonstrates the feasibility of the proposed design concept. At last, this work also achieves the low RMS amplitude error and broadband response, and it could be integrated into many transceivers such as phased-array or ultra-wideband systems.

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ORCID

Chatrpol Pakasiri https://orcid.org/0000-0002-0387-8105
Sen Wang https://orcid.org/0000-0001-9715-3422

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AUTHOR BIOGRAPHIES

Chatrpol Pakasiri received his B.S. degree in electronics engineering from King Mongkut's Institute of Technology Ladkrabang, Thailand in 1996. He received M.S. and Ph.D. degrees from the Department of Electrical and Computer Engineering, University of Houston, USA in 2001 and 2005, respectively. He also graduated M.S. from the EECS Department, National Chiao Tung University, Taiwan in 2013. Since 2014, he has joined the College of Advanced Manufacturing Innovation, King Mongkut's Institute of Technology Ladkrabang, Thailand, where he is currently assistant

professor. His research interests are active and passive RF circuits and antennas.

Fu-Sheng Zhu received his B.S. degree in electrical engineering from the National Taipei University of Technology, Taipei, Taiwan in 2017, the M.S. degree in Graduate Institute of Electrical Engineering from National Taipei University of Technology Taipei, Taiwan, in 2019. His research interests are RF CMOS attenuator and phase shifter.

Sen Wang (S'05-M'10) received his B.S. degree in electrical engineering from the National Taiwan University, Taipei, Taiwan in 2004, the M.S. degree and Ph.D. degree in Graduate Institute of Communication Engineering from National Taiwan University, Taipei, Taiwan, in 2006 and 2009, respectively. He joined the Faculty of the Department of Electronic Engineering, National Taipei University of Technology, Taipei, Taiwan, as an assistant professor in February 2010. He is currently as an associate professor, and continues his research on integrated circuit designs for research and development of RF system-on-chip, integrating active and passive microwave/millimeter-wave RF signal-processing components into a single chip. His research activities also involve the design and development of CMOS millimeter-wave and microwave active and passive circuits, the field theory analysis and design, and radar system engineering. Many research results are published in the top IEEE and IET journals or transactions.

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ประวัตินักวิจัย

1. **Research Team Information**

1.1 Personal Data

Name-Last Name Chatrpol Pakasiri

Present Position Teacher

Position Title Lecturer

Education

Degree Level	Major	Institute or University	Graduation Year
Ph.D.	**Electrical and Computer Engineering**	**University of Houston, Texas, U.S.A.**	**2005**
M.S.	**Electrical Engineering and Computer Science**	**National Chiao Tung University, Taiwan**	**2013**
M.S.	**Electrical and Computer Engineering**	**University of Houston, Texas, U.S.A.**	**2001**
B.S.	**Electronic Engineering**	**King Mongkut's Institute of Technology Ladkrabang**	**1996**

Point of Contact College of Advanced Manufacturing Innovation, King Mongkut's Institute of Technology Ladkrabang , 1 Soi Chalongkrung 1, Ladkrabang, Bangkok, Thailand 10520

Research Experience or Field of Expertise Microwave passive and active circuit, antenna design, numerical electromagnetics

1.2 Work/Experience

Research Output/Creative Work/Innovations/Patents

- Projects & Patents:
  - Directive magnetic antenna for HF band (3 MHz – 30 MHz) (Thai Petty Patent Submitting)
  - Study of DC motor simulation
  - Design of power amplifier at 900 MHz
- Selected Publication lists (International Journals)

  [1] Chao-Han Tsai ,I-No Liao , Pakasiri, C., Hsin-Cheng Pan , Yu-Jiu Wang, "A Wideband 20 mW UHF Rectifier in CMOS," IEEE Microwave and Wireless

Components Letters, vol. 25, pp. 388-390, June 2015.

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2. **Research Team Information**

2.1 Personal Data

Name-Last Name Sen Wang

Present Position Teacher

Position Title Associate Professor

Education

Degree Level	Major	Institute or University	Graduation Year
Ph.D.	**Communication Engineering**	**National Taiwan University**	**2009**
M.S.	**Communication Engineering**	**National Taiwan University**	**2006**
B.S.	**Electrical Engineering**	**National Taiwan University**	**2004**

Point of Contact Microwave/Millimeter-wave Integrated Circuits Lab., Department of Electronic Engineering, National Taipei University of Technology, 1, Sec. 3, Zhongxiao E. Rd., Taipei, 10608, Taiwan

Research Experience or Field of Expertise Integrated circuit designs for research and development of RF system-on-chip, integrating active and passive microwave/millimeter-wave RF signal-processing components into a single chip. Design and development of CMOS millimeter-wave and microwave active and passive circuits. Field theory analysis and design of radar system engineering.

2.2 Work/Experience

Research Output/Creative Work/Innovations/Patents

- Projects & Patents:
  - Applications of Synthetic Waveguide on CMOS
  - Design and application of CMOS semi-passive inductors using tapped-inductor feedback
  - Microwave Rectenna Design
  - Design of a low-low, low-power, and high-selectivity CMOS BPF using active capacitor and feedback inductor

- Design and Implementation of Differential DVB LNA and System Verification
- Design and Implementation of Microwave Intruder-detection Transceiver
- Design and Implementation of Ka-band multi-antenna transceiver

- Awards:
  - Outstanding Research Award 2011, EE College, National Taipei University of Technology
- Selected Publication lists (International Journals)

[1] S. Wang, and B.-Z. Huang "Compact CMOS branch-line coupler using high-Q slow-wave transmission lines," Microwave and Optical Technology Letters, vol. 55, no. 5, pp. 1174-1178, May 2013.

[2] S. Wang, and W.-J. Lin "Design of low-power and high-gain CMOS LNA with current-reused topology," Microwave and Optical Technology Letters, vol. 55, no. 10, pp. 2429-2431, October 2013.

[3] M.-J. Chiang, S. Wang, and C.-C. Hsu, "Miniaturized Printed Slot Antenna with Multi-Ring Technique for Dual-band and Broadband Operations," IET Microwaves, Antennas & Propagation, vol. 8, Iss. 6, pp. 409-414, June 2014.

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[13] S. Wang and R.-H. Chang, "2.4-GHz CMOS bandpass filter using active transmission line," Electronics Letters, vol.52, no. 5, pp. 371-372, Mar. 2016.

[14] S. Wang and C.-Y. Xiao, "A 7/24-GHz CMOS VCO with High Band Ratio Using a Current-Source Switching Topology," accepted by IEEE Trans. on Ultrasonics, Ferroelectrics, and Frequency Control.

[15] S. Wang, C.-H. Lee, and Y.-B. Wu, "Fully-integrated 10-GHz Active Circulator and Quasi-Circulator using bridged-T networks in standard CMOS," accepted by IEEE Trans. on Very Large Scale Integration (VLSI) Systems.