ULTRA-LOW POWER CMOS ANALOG INTERGRATED CIRCUITS FOR BIOMEDICAL APPLICATIONS

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หัวข้อวิทยานิพนธ์	วงจรรวมอนาล็อกแบบซีมอสที่ใช้กำลังไฟต่ำมากสำหรับการประยุกต์ใช้งานด้านการแพทย์
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บทคัดย่อ

วิทยานิพนธ์นี้นำเสนอเทคนิคการออกแบบวงจรกรองความถี่เลือกผ่านอันดับ 4 ชนิดทรานส์คอนดักแตนซ์กับตัวเก็บประจุ และ วงจรแปลงสัญญาณอนาล็อกเป็นดิจิตอลแบบลอการึทึม 6 บิตโดยใช้โครงสร้างชนิด Successive Approximation ซึ่งเป็นส่วนหนึ่งของประมวลผลส่วนหน้า สำหรับอุปกรณ์การแพทย์ชนิดฝังภายในร่างกาย วงจรกรองความถี่เลือกผ่านพื้นฐานอันดับ 2 ถูกออกแบบโดยมีพื้นฐานมาจากต่อตัวเก็บประจุกับตัวเหนี่ยวนำชนิดแอคทีฟ มอสทรานซิสเตอร์ถูกนำมาใช้สำหรับการสร้างตัวเหนี่ยวนำแบบแอคทีฟและถูกออกแบบให้ทำงานในย่านต่ำกว่าแรงดันขีดเริ่มเพื่อให้สามารถทำงานที่แรงดันไฟเลี้ยงต่ำและใช้กำลังงานต่ำ เทคนิคการลดทอนสัญญาณอินพุตโดยใช้ตัวเก็บประจุถูกนำมาประยุกต์ใช้เพื่อเพิ่มความเป็นเชิงเส้นให้กับวงจรกรองความถี่ วงจรที่ออกแบบถูกจำลองผลการทำงานโดยใช้เทคโนโลยีซีมอส 0.18 ไมโครเมตรที่แรงดันไฟเลี้ยง 1 โวลต์ ผลที่ได้จากการจำลองการทำงานบ่งชี้ว่า วงจรกรองความถี่เลือกผ่านสามารถปรับเปลี่ยนค่าความถี่กลางได้ตั้งแต่ 80 เฮิร์ท จนถึง 6.18 กิโลเฮิร์ท จากการเปลี่ยนค่าไบอัสกระแสของวงจร ที่ความถี่ 945 เฮิร์ท ค่า Quality Factor เท่ากับ 3 แรงดันไฟเลี้ยง 1 โวลต์ วงจรมีสัญญาณรบกวนที่อินพุต 174.2 ไมโครโวลต์ ใช้กำลังงานเพียง 6 นาโนวัตต์ มีค่าพิสัยพลวัตกว้าง 57.8 เดซิเบล วงจรที่ออกแบบมีความทนทานต่อเปลี่ยนแปลงของกระบวนการสร้างและจากแรงดันไฟเลี้ยง พื้นที่ของวงจรประกอบด้วยวงจรกรองอันดับ 4 วงจรบัฟเฟอร์และวงจรกำเนิดกระแสอ้างอิงเท่ากับ 0.08 ตารางมิลลิเมตร ดังนั้นวงจรนี้มีความเหมาะสมต่อการใช้งานที่หลากหลายโดยเฉพาะกับงานที่ใช้มีสัญญาณความถี่ต่ำต้องการการใช้ไฟเลี้ยงต่ำและกำลังงานต่ำ

สำหรับการออกแบบวงจรแปลงสัญญาณอนาล็อกเป็นดิจิตอลแบบลอการึทึม 6 บิต มีการทำงานแปลงสัญญาณสองช่วงเพื่อให้ได้การประมาณเชิงเส้นแบบฟังชันก์ลอการึทึม ข้อดีของวงจรแปลงสัญญาณอนาล็อกเป็นดิจิตอลแบบลอการึทึมคือ เหมาะสมกับสัญญาณที่มีขนาดการเปลี่ยนแปลงกว้าง ตัวอย่างของสัญญาณประเภทนี้ได้แก่ สัญญาณเซลล์ประสาทสมองและสัญญาณเสียงในระบบประสาทหูเทียม วงจรมีการบีบอัดสัญญาณและแปลงเป็นดิจิตอลที่เอาท์พุต การแปลงสัญญาณของ

วงจรที่ออกแบบแบ่งออก 2 ส่วน คือ ส่วนแรกคือการแปลงสัญญาณแบบหยาบซึ่งจะได้สัญญาณดิจิตอล 3 บิตแรก จากนั้นมีการแปลงแบบละเอียดซึ่งจะได้สัญญาณดิจิตอล 3 บิตหลัง วงจรที่ออกแบบถูกจำลองผลการทำงานโดยใช้เทคโนโลยีซีมอส 0.35 ไมโครเมตรที่แรงดันไฟเลี้ยง 1.8 โวลต์ ผลที่ได้จากการจำลองการทำงานบ่งชี้ว่า วงจรที่นำเสนอใช้กำลังงานอยู่ในช่วง 4.36 ถึง 14.6 ไมโครวัตต์ ที่ความชักตัวอย่าง 25 กิโลเฮิร์ตซ์ วงจรแปลงสัญญาณอนาล็อกเป็นดิจิตอลที่ออกแบบมีค่า DNL อยู่ในช่วง +0.26/-0.32 LSB และค่า INL อยู่ในช่วง +0.19/-0.45 LSB มีค่า ENOB เท่ากับ 4.97 บิต และค่า SNDR เท่ากับ 31.7 เดซิเบล ที่ช่วงของสัญญาณอินพุต 1 โวลต์

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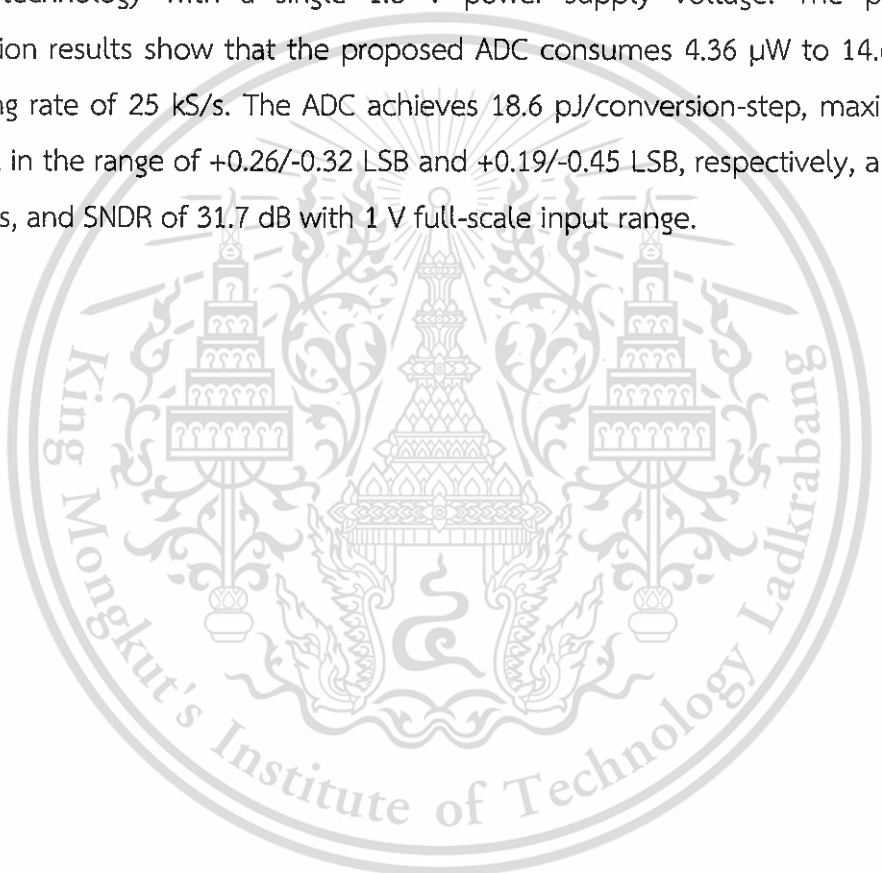
ABSTRACT

The thesis is concerned with the design and realization of low power programmable 4^{th}-order, G_m-C filter and 6-bit, two-step successive approximation logarithmic ADC, which can be used as the key building blocks of an analog front-end of implantable medical devices.

In the filter design, the core 2^{nd}-order filter stage is realized by adding a coupling capacitor to a simple cascode gyrator-C active inductor structure. A single MOSFET is used as the transconductor element for the implementation of the active inductor. Low-power and low-frequency filter is achieved by biasing the transistors in the weak inversion region. The capacitive input attenuation technique is used to enhance the linearity of the filter. The proposed filter was designed and simulated with a 1-V power supply voltage with process parameters from a standard 0.18 μm CMOS technology. The post-layout simulation results show that the centre frequency of the filter can be tuned from 80 Hz to 6.18 kHz by programming the bias currents of the filter through a 3-bit digital-to-analog converter. At a centre frequency of 945 Hz and the quality factor of 3, the proposed filter achieves 174.2 μV input-referred noise, while consumes only 6 nW from a 1-V single power supply voltage. The filter exhibits a dynamic range of 57.6 dB with robust performance against process and voltage variations. The area of the overall circuit including the core 4^{th}-order bandpass filters with voltage buffer and bias current generator is 0.08 mm^2. The filter is suitable for biomedical applications that require low-frequency, wide-tuning range as well as ultra-low power and low-voltage operation.

In the ADC design, a two-step operation is proposed to obtain a piecewise-linear approximation of the desired logarithmic transfer function. The logarithmic ADC offers attractive solutions for neural recording and closed-loop deep brain stimulation as both applications require a wide dynamic range. It can directly convert and compress input signals with logarithmic encoding. In the two-step ADC operation, the first conversion step performs a 3-bit logarithmic coarse conversion while the second conversion step carries out a 3-bit linear fine conversion. The proposed ADC was designed and simulated by using process parameters from a standard 0.35 μm CMOS technology with a single 1.8 V power supply voltage. The post-layout simulation results show that the proposed ADC consumes 4.36 μW to 14.6 μW at a sampling rate of 25 kS/s. The ADC achieves 18.6 pJ/conversion-step, maximum DNL and INL in the range of +0.26/-0.32 LSB and +0.19/-0.45 LSB, respectively, an ENOB of 4.97-bits, and SNDR of 31.7 dB with 1 V full-scale input range.



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Yuwadee Sundarasaradula

TABLE OF CONTENTS

TABLE OF CONTENTS (CONT.)

LIST OF FIGURES

LIST OF FIGURES (CONT.)

LIST OF FIGURES (CONT.)

LIST OF TABLES

LIST OF ABBREVIATIONS

ADC	Analog-to-digital converter
AP	Action Potential
BER	Bit error rate
BPF	Bandpass filter
BTE	Behind-the-ear
C	Coding coefficient
CMOS	Complementary metal-oxide-semiconductor
CMRR	Common-mode rejection ratio
CT	Continuous-time
CS	Common source
CD	Common drain
CG	Common gate
DAC	Digital-to-analog converter
DBS	Deep brain stimulator
DNL	Differential nonlinearity
DR	Dynamic range
DSP	Digital signal processor
ECG	Electrocardiogram
EEG	Electroencephalogram
ENOB	Effective number of bit
FFT	Fast Fourier transform
FoM	Figure of merit
ICHA	Information concentration at high amplitude
ICLA	Information concentration at low amplitude
IM3	Third order Intermodulation Distortion
INL	Integral nonlinearity
LFPs	Local field potentials
LSB	Least significant bit
MIFG	multiple-input floating-gate
MOSFET	Metal oxide semiconductor field effect transistor

LIST OF ABBREVIATIONS

MSB	Most significant bit
NCI	Non-concentrated information
OTA	Operational transconductance amplifier
PGA	Programmable gain amplifier
PMOS	P-type metal-oxide-semiconductor
PVT	Process, Voltage, Temperature
rms	Root-mean-square
SAR	Successive approximation register
SFDR	Spurious-free dynamic range
S/H	Sample-and-hold
SNDR	Signal-to-noise-plus-distortion ratio
SNR	signal-to-noise ratio
STN	Subthalamic Nucleus
THD	Total harmonic distortion

Chapter 1

Introduction

1.1 Motivation and Background

The public health service is one of the strategies of the national economic and social development plan of Thailand. Although this effort leads to 99.4 percent of Thai people being covered by the health security system, the service should be improved through better quality and coverage. The estimation and projection of population predict that many countries have changed to an ageing society and Thailand also will be an ageing society by 2025 [1]. The demographic structure has changed as the segment of older population increases while the segment of younger and worker decrease. The older segment of the population requires and utilizes an average of 3–5 times more healthcare services than younger and worker people. The result has several direct effects in terms of lacking financial support, the health professional shortage, and insufficient medical supplies and equipment in the future. A limited number of health professionals will be a high incidence of medical error and strained patient-doctor relations. This emerging issue has excitingly prompted my interest in research innovations in healthcare devices.

Innovations in healthcare technology particularly through the use of life-impact biomedical devices and systems are turning the passive health services to be the efficient proactive self-healthcare taker. In the future, not only the patient but possibly everyone in everyday life will be closely monitored their vital signs and communicate with their service providers as a part of preventive healthcare. Eventually, the service will be shifted from a hospital-centered treatment to a patient-centric healthcare monitoring. The key to achieve that is the implantable and wearable biomedical devices which require the advances in both integrated circuit technology and innovative circuit design.

Nowadays, implantable and wearable medical devices are being used in many parts of the body to replace or act as a fraction or the whole biological structure, such as a pacemaker, cochlear implant or bionic ear, retinal prosthesis and deep brain stimulation (DBS). These devices help patient's condition lives and allow them to be more independent. For instance, a pacemaker, commercially available

implantable devices, is designed to monitor a patient's electrocardiography (ECG) signal continuously. The electrical stimulation is delivered through electrodes via a stimulation circuit when a missing heartbeat is detected [2].

In the foreseeable future, the developing CMOS-based DNA detection will be capable of biological readout information from the cell which will be useful for identifying bacteria and preventing an outbreak. Neurostimulation of the deep brain and other regions of the brain are being researched for treatment of many neurological disorders. Wireless body area network (WBAN) is intended for the future generation of short-range communication electronic devices for in-, on- and around the body, including a network of biomedical sensors for healthcare monitoring. For example, wireless ECG and Electroencephalogram (EEG), closely monitoring and processing our vital signs, are essential parts of telemedicine providing clinical healthcare at a distance and in many cases save lives in emergency situations.

The success and availability of these devices not only resolve the problems of a growing of medical errors, inadequate staffing and lack of coverage but also reduce long-term costs, and improve the quality of life. It also helps scientists and researchers to get valuable information about what is happening inside of a living body.

1.2 Examples of implantable medical devices

1.2.1 Cochlear implant

It is well-known that cochlear implant is the world's most successful medical prostheses. Today's estimated shows that more than 330,000 profoundly deaf people in the world are fitted with this device in their inner ear or cochlea. It allows them to hear almost normally [3]. The cochlear implant can restore hearing by directly stimulating the auditory nerve that conducts electrical impulses from the ear to the brain. The mechanical topology of a cochlear implant at the moment is depicted in Figure 1.1. It is a partially implanted system [4] as the electrodes, and a wireless receiver is implanted inside the body while a microphone, sound processor, and wireless transmitter are placed outside the body. The major challenge of the cochlear implant is to design the sound processor located behind-the-ear (BTE) into fully implanted inside the body and powered by an implantable battery or an energy harvester.

The operation of the cochlear implant starting from a microphone transforms sound into electrical signals, which is amplified by a low-noise preamplifier. The signal is further processed by 8-20 channels of signal processors, which transform the sound frequency patterns into the corresponding electrode stimulation patterns. The programmable bandpass filters separate the signals based on its different frequency to the envelope detector. The envelope of the filtered signals is used to control the amplitude of the stimulating biphasic pulses. Since the dynamic range of electrical current pulses in a cochlear implant is 3-20 dB, a nonlinear compression function (e.g., logarithmic analog to digital converter; logarithmic ADC) is used to ensure that the envelope output is suitable for the dynamic range of electrically generated hearing [5, 6]. Finally, the signals and power are transmitted through the skin via the telemetry system to the implanted receiver-stimulator. This stimulator generates the electrical currents to stimulate the electrodes in the cochlear. In typical, the number of implanted electrodes used for stimulation is 8 to 20.

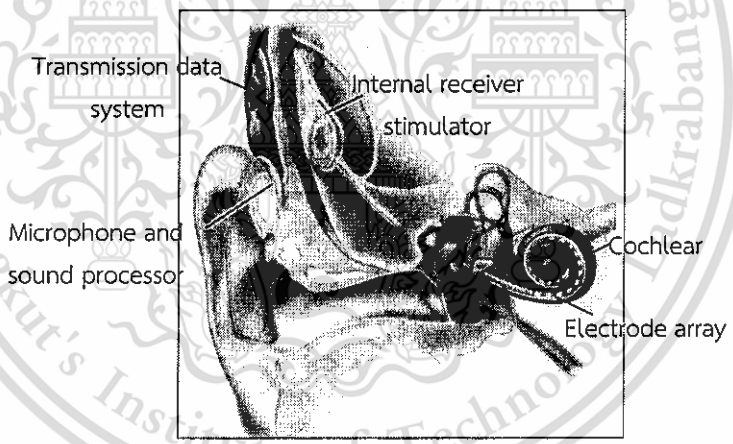

Figure 1.1 The mechanical topology of a cochlear implant [4]

1.2.2 Neural recording and deep brain stimulation

A human brain is an extremely complex structure. It contains an estimated 85 billion neurons, 100 trillion synapses, and 100 chemical neurotransmitters [7]. Neural recording systems and DBS are being built to understand how the brain functions and used for diagnosis and treatment. It is available for patients who suffer from brain-related diseases like Parkinson's Disease, Tremor, Dystonia and other motor disorders [8].

DBS delivers controlled electric pulses to excite specific region in their brain, which is most commonly the Subthalamic Nucleus (STN) through extension microwires and electrodes. These pulses will block the abnormal nerve signals that cause movement or affective disorders [9, 10]. A neurostimulation is a very effective neurosurgical procedure for the patients whose condition cannot be controlled with medications. Multichannel DBS distributed of neural signals is required as the most effective in alleviating Parkinson's disease locations are still trying to discover. The multichannel neural recording also demands to unlock the neural activities from a large number of neurons. Therefore the number of recording channels and stimulating sites are targeted hundreds to thousands.

Existing stimulation is based on continuous open-loop stimulation [8]. The clinician will program patent's neurostimulator to reduce symptoms while minimizing any side effects. A unique set of signal amplitudes, pulse widths and frequency that are the most effective for treatment each patient is employed. Follow-up appointments will be scheduled to maximize the benefits of the treatment. It may take several visits to adjust the stimulation before the right settings are determined. Open-loop stimulation loses its efficacy over time due to plasticity and other changes in the brain, requiring periodic recalibration of stimulation parameters. Hence, the major challenge of open-loop stimulation aims to perform closed-loop stimulation [11-14]. Stimulation parameters are adapted in real time using recorded neural signals as feedback signals track the dynamics of the brain. Thus, the system maintains the therapeutic effects over time. Figure 1.2 shows a conceptual diagram of neural recording and closed-loop DBS [13].

The neural signal of interest is composed of low-frequency local field potential (LFP) signal and high-frequency Action Potential (AP) or spike signal. The LFP signal represents a spatial average of neural activity in the neighborhood of the electrode and its amplitudes up to 5 mV and frequencies in the range from 1 Hz to 100 Hz. The spike signals, associated with the extracellular electrical activity of a single neuron unit, have amplitudes up to 500 μV with frequencies from 100 Hz to 7 kHz [15, 16]

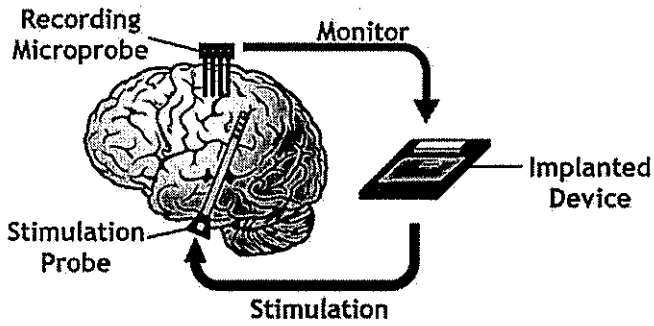

Figure 1.2 Conceptual diagram of neural recording and close loop DBS [13]

1.2.3 Analog front-end circuit for implantable medical devices

Despite there have been different functionalities of implantable medical devices, the electronic systems of these devices have much in common. Figure 1.3 shows a general block diagram of a typical implantable medical device including an energy source, data telemetry, a sensing block/monitoring, signal processing for algorithm and system control, and a therapeutic stimulation. The development of fully integrated cochlear implant, neural recording and DBS are among examples of implanted medical devices that are still in the research and development stage. For implementation, the trade-offs between performance, power consumption, device size, compatibility and robustness need to be carefully taken into account. The analog front-end block is one of the most critical specifications as an accurate information relies on the quality and accuracy of pre-possessing biopotential signals. A number of researchers have sought to determine several types of the analog front-end circuit. There are many challenging issues still needed to be addressed at both circuits and system levels. The ultra-low power dissipation is mainly focussed which the system can ideally function more than 10 years without the need for a battery replacement. Moreover, the heat generated from the circuit must be minimal to ensure that there is no damage to the surrounding tissues.

The typical architecture of the analog front-end interfacing circuit consists of three fundamental blocks: (1) a low-noise amplifier, (2) bandpass filter, and (3) analog to digital converter as shown in Figure 1.4. A low-noise, wide dynamic range analog front-end circuit is required due to the low-level amplitude of the biopotential signals in the order of microvolts. The amplifier is used to amplify the weak signals before filtering and the data conversion. Typically, a low-noise, low-power and mid-

band gain of 40 dB to 60 dB amplifier is expected. Since the biopotential signals are very small, the input-referred noise has to be minimized. The input-referred noise of the front-end amplifier consists of a thermal noise component and a flicker noise component. In general, the thermal noise and flicker noise can be reduced by choosing a large transconductance and large size input transistor, respectively. The chopper-stabilized is another technique to reduce the flicker noise in the input referred noise as chopping mitigates the low-frequency flicker noise of the amplifier [17-19].

Following pre-amplification, a bandpass filter is required to reduce spurious frequencies beyond the bandwidth of interest or to separate the signals based on frequency band before converting these analog signals to digitals signals. For example, neural recording amplifier is typically achieved with combined a bandpass filter [12, 16, 19-23]. The cut-off frequencies are either programmable or tunable with a bandwidth of sub-Hz to 7 kHz. The low-frequency cut-off prevents a large DC offset from the electrode, and the high-frequency cut-off eliminates the unnecessary out-of-band noise. For cochlear implant, filter banks in the audio-frequency with 8-20 channels are employed related to implanted electrode. The transconductance-capacitor (G_m-C) topology has shown to be an outstanding choice for low power operation.

ADC is a key building block that links the natural world of biopotential signals and the world of digital processing. Conversion of these signals requires an ultra-low-power operation e.g. in μW to nW range, medium-resolution typically 8-12 bit. The Successive approximation converter is widely used for implementation because this architecture has minimum analog complexity, low-power consumption and digital scalability with technology. The SAR architecture includes only one comparator, DAC typically composed of binary-weighted capacitors, and control logic.

Low power and low noise requirements are challenging to achieve simultaneously. Meanwhile, noise levels are usually reduced as the power consumption is increased. For this reason, these designs are often a compromise to a trade-off between power and noise levels.

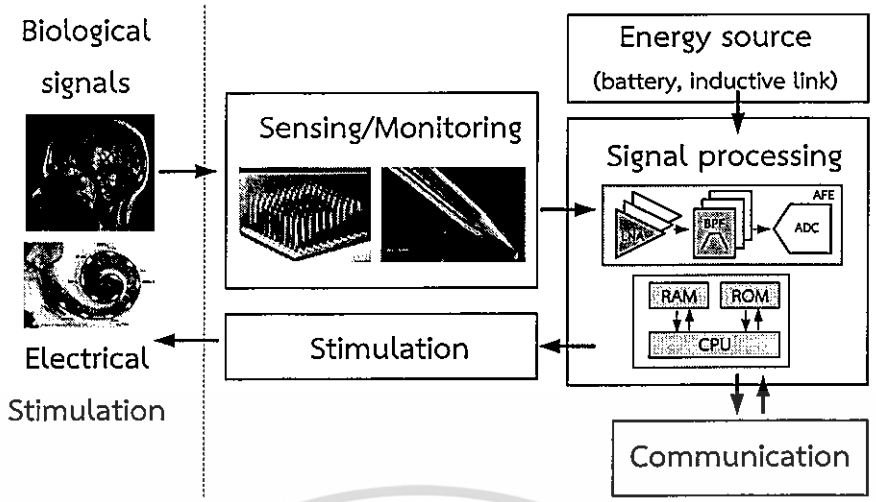

Figure 1.3 A general block diagram of typical implantable medical devices

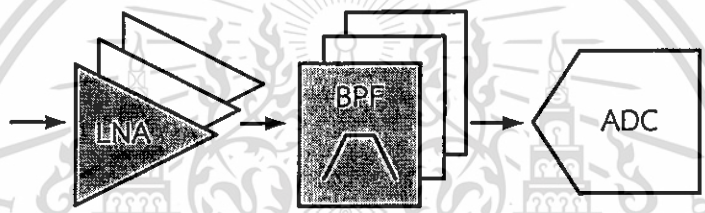

Figure 1.4 An analog front-end circuit

1.3 Thesis organization

The motivation and background of implantable medical devices are introduced. Examples of implantable medical devices such as a cochlear implant, neural recording and closed-loop DBS are reviewed. A general block diagram of a typical implantable medical device particularly analog front-end circuit is discussed. The proposed G_m-C filter and logarithmic SAR ADC suitable for implantable devices are introduced as the thesis distribution. Chapter 2 presents a review of G_m-C filter architecture and the operation of a conventional SAR ADC. The comparison between linear ADC and logarithmic ADC architecture are discussed for using in implantable medical devices. In Chapter 3, details the proposed simple, high-Q, programmable, G_m-C bandpass filter, which consumes only a few nanowatts of power dissipation. The capacitive input attenuation technique is used to increase the linearity of the filter. The design of the process, voltage-insensitive bias current is proposed to adjust the center frequency of the filter. Key design considerations and analysis of noise,

and bandwidth are shown. Post-layout simulation results are presented and compared with existing filters. Chapter 4 describes the proposed 6-bit, logarithmic SAR ADC. The structure and circuit implementation of crucial building blocks of SAR ADC are considerations. The desired logarithmic relationship is realized by using a piecewise-linear approximation, and the ADC circuit is implemented by using a two-step successive approximation structure. Post-layout simulation results both static and dynamic performance are showed and compared with existing ADCs. Finally, Chapter 5 is the summary and suggestions for future work.

Chapter 2

Overview of low power G_m-C filters and Successive Approximation ADCs

In this chapter, an overview of the transconductance-capacitor (G_m-C) filters and successive approximation analog to digital converters (SAR ADC) are introduced. In section 2.1, the general requirements of bandpass filters (BPF) for biomedical applications such as ECG, spikes recording, LFPs recording, cochlear implant and breathing detection are described. Several techniques for wide linear range operational transconductance amplifier (OTA) and subthreshold G_m-C filters for nanopower operation are presented. The Figure-of-merit (FoM) for performance comparison of existing BPFs is described. In section 2.2, a performance comparison of various architectures of ADCs including SAR, pipeline, sigma-delta and flash is described and the suitable ADC architecture for biomedical application is deduced. The basic operation of SAR ADC and a nonlinear ADC, in particular logarithmic ADC for biopotential signals such as neural and audio signals are presented. Finally, performance parameters for comparison between linear ADC and Logarithmic ADC are summarized.

2.1 Overview bandpass filter for biomedical applications

2.1.1 General BPF requirements for biomedical filters

The bandpass filter is used as a part of analog front-end preprocessing blocks in several biomedical applications such as a cochlear implant [5, 24-27], breathing detection [28] cardiac pacemaker [29-31] [30-33] . The filter separates desired signals from other signals and noise by making use of the difference in their energy frequency spectra. Figure 2.1 shows an approximate frequency and amplitude distribution of common biopotential signals [34]. The range of amplitudes and frequency contents is major factors which influence the design specifications for processing and recording. The amplitude range determines the required dynamic range (DR) of the signals. The common biopotential signals have a very low-frequency content from DC to a few kHz and have amplitudes in the range of μV-mV.

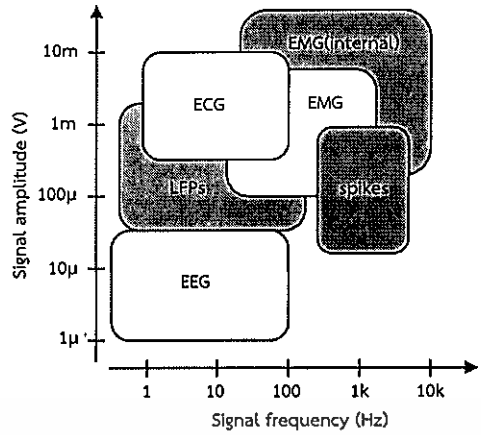

Figure 2.1 Approximate frequency and amplitude distribution of common biopotential signals [34]

For example, the filter used in a cochlear implant divides the input signal, which is amplified by a low-noise preamplifier into frequency bands and then are processed and sent to individual electrode. The frequency discrimination of the cochlear system is essential for the extraction of spectral content in auditory signals. The filter should be tunable over the audio frequency range which spans from 20 Hz to 20 kHz. The DR is approximately 80 dB. The high-Q bandpass filter is also needed to isolate frequency information. The envelope of the filtered signals is used to control the amplitude of the stimulating biphasic pulses. A logarithmic ADC is implemented to ensure that the envelope output is suitable for the dynamic range of electrically generated hearing. Figure 2.2 shows a general block diagram sound processing used in the cochlear implant [5].

Implantable cardiac pacemaker and the electrocardiogram (ECG) microstimulator are medical device to help control abnormal heart rhythms and providing electrical pulses when the heart does not function properly. The BPF is generally used in the pacemaker sensing system block diagram as shown in Figure 2.3 [33, 35]. It comprises a low noise amplifier, filter, ADC and DSP. A low-noise amplifier is used to amplify the weak ECG signals. Depending on the electrodes used, the ECG signal swing can also vary from 50µV up to 4mV [36] and thus the required dynamic range is 44 dB [37, 38]. The BPF is placed behind the preamplifier with the recommended bandwidth of 0.05-150 Hz and 0.05-250 Hz for adults and children, respectively [32, 39, 40].

Figure 2.4 depicts the principal components of the breathing monitoring system [41]. The microphone sends the respiratory sound signal to a bandpass filter which passes frequencies in the range respiratory sounds. The sixth-order BPF is required with a passband of 500-900Hz. The filtered signal is passed to a rectifier and a feature recognition section to a transmitter which sends an appropriate signal.

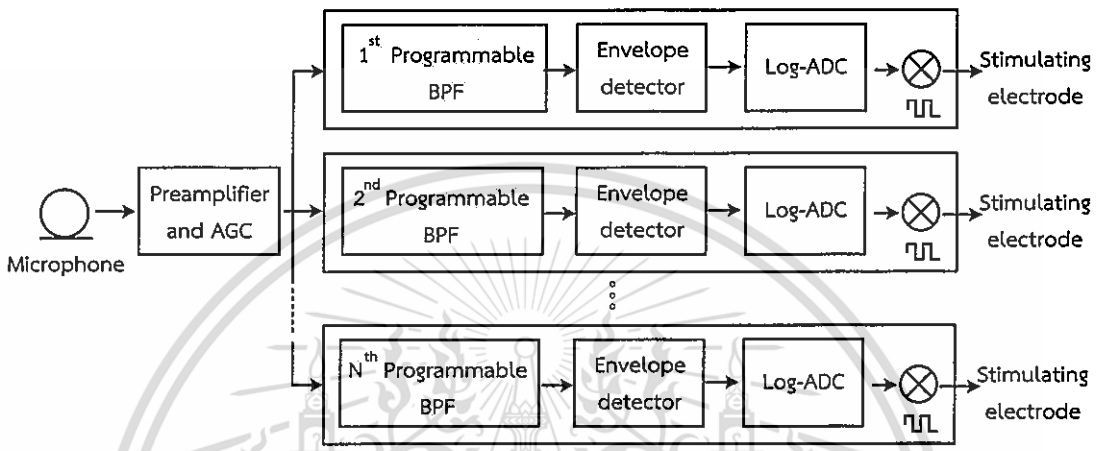

Figure 2.2 A general block diagram sound processing used in the cochlear implant [5]

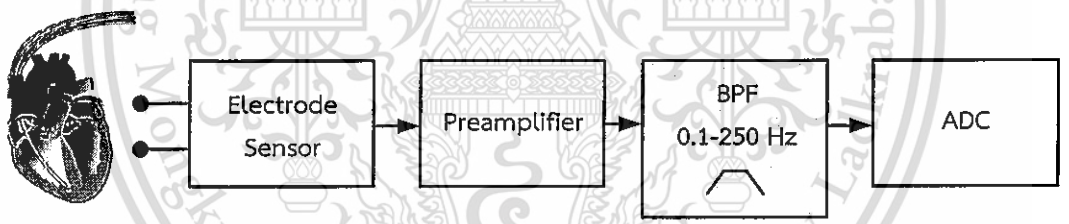

Figure 2.3 Sensing system block diagram for implantable pacemaker applications [33, 35]

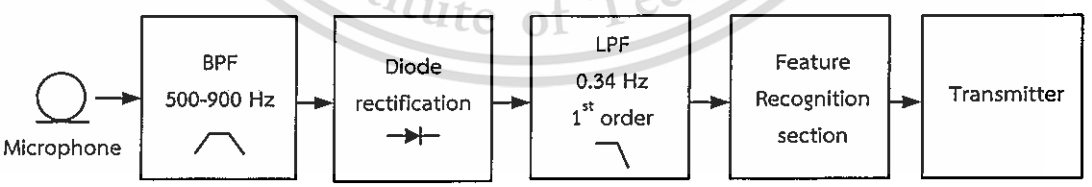

Figure 2.4 A block diagram of the system and the most relevant blocks implementing the proposed breathing detection algorithm [41]

The other required performance BPF of neural prosthetic applications including, filtering of neural signals as high-frequency spikes and low-frequency LFPs are summarized in Table 2.1. Typically, low noise, wide dynamic range, low distortion,

compact physical area, low power consumption and wide tuning range are the general specifications for most biopotential signals that required for the filter implementation.

Table 2.1 Approximate frequency and amplitude distribution of common biopotential signals and required BPF performance

Applications	Signal characteristic		BPF required performance	
	Amplitude	BW (Hz)	DR (dB)	Filter order
ECG [36], [32, 39, 40].	50μV - 4mV	0.1-150,250	44	4
Spike recording [19]	10μV - 100μV	100-7k	>60 dB Spikes+LFPs	2
LFP recording [19]	up to 5mV	1Hz - 100		
Cochlear implant [5]	5μV-50mV	100 – 10k	60	>2
breathing detection [28]	n/a	500-900	44	6

2.1.2 Nanopower BPF design

Various types of continuous-time filters, including opamp-RC filters, RLC ladder filters and G_m-C filters [31, 42-46], can be used for biomedical applications.

In an op amp-RC filter, the opamps must have sufficient gain-bandwidth in order to maintain the virtual ground condition at its inputs over a wide range of frequencies. Thus, the power consumption of the filters is directly related to that of opamps, which usually results in a relatively larger power dissipation comparing with a G_m-C filter operating at the same frequency.

G_m-C filters have been successfully employed in the design of low-frequency filters. This topology offers key advantages in terms of tunability, circuit simplicity, nanopower operation and a compact physical area. The center frequency of the G_m-C topology is typically determined by the ratio of G_m/C. However, since the small values of the on-chip capacitors typically in the order of tens pF for the realizable area in the circuit implementation, the filter can be obtained only using the ultra-low G_m, typically in the order of a few nA/V or less.

To meet the power consumption and area requirements for the G_m-C filter, the number of OTAs should be minimized because the larger number of OTAs means higher power consumption, larger chip area, more noise, and more parasitic effects. Subthreshold G_m-C filter has shown to be an excellent choice in low-power, low-voltage, and low-frequency biopotential signals. Conducting a very low-current in subthreshold operation results in a very low transconductance that helps in designing a very low-frequency G_m-C filter. The performance of G_m-C filters directly depends on its OTA. One important drawback of the subthreshold G_m-C filter is the narrow linear range of the OTAs affecting the linearity of the overall system. The reason is that subthreshold current in MOS transistors operating in subthreshold depends exponentially on the gate voltage.

2.1.2.1 Wide-linear-range OTA

Various design strategies to improve linearity performances of the OTAs and overcome the deterioration of its specifications have been proposed in the literature [47-54]. The techniques are as follow: 1) input attenuation, 2) source-degeneration, 3) nonlinear terms cancellation, and 4) the multiple-input floating-gate (MIFG) MOS transistors.

In the input attenuation technique, the linearity improvement is accomplished as the nonlinear terms of the output current is reduced by reducing the input voltage. The bulk driven transistor is one of the attenuation techniques that can be used for reducing input signal [55-59]. The input signal is applied to the bulk rather than the gate of the transistor. Since the input signal is applied to the bulk, this removes the limitation of threshold voltage requirements in low voltage operation. The bulk transconductance is typically 2–5 times smaller than the gate transconductance. However, this issue leads to limit the gain, gain-bandwidth product and high input referred noise that may still limit the signal dynamic range. The passive attenuation is another technique used resistive- or capacitive-attenuation. It allows for simple scaling of attenuation ratio for adjusting the linear range and does not introduce harmonic distortions.

In the source-degeneration technique, the linearity improvement is implemented by stacking diode-connected transistors at the differential input transistors. However, this technique increases noise factor of the OTAs, and then the

noise-linearity trade-off is necessary [31, 55, 60-65]. Moreover, this technique limits the voltage headroom which requires higher supply voltage and thus reduces dc input operating range [55].

In the nonlinear terms cancellation technique, the linearity improvement is realized as the superposition of two differential structures with opposite behaviors of nonlinearity [66-69]. Hence, the total distortion at the output of the transconductance can be reduced. However, this technique generally relies on fully balanced topology to achieve better linear V_{id} - I_{out} conversion. Thus, the output current might suffer from significant second-order harmonics due to mismatch of process parameter tolerance and temperature gradient [70].

In the multiple-input floating-gate (MIFG) MOS transistor technique [51, 71-74], it provides a voltage division at its floating gate that allows both low voltage operation and large linear range. However, this technique needs extra fabrication processes which would not be useful in standard CMOS technology.

Although the linearity of transconductance is improved as mentioned above, the increasing of power consumption and the circuit complexity are main drawbacks designing filter operating in the nanopower. Note that the term nanopower defines a class of circuits with power consumption of just a few nanowatts. MOSFETs operating in subthreshold and the element replacement as active devices are widely used for designing the nanopower BPF. Moreover, the concept idea using only a single transistor as the transconductance amplifier is attractive in terms of extremely low power operation and reasonable physical size. The common source (CS) amplifier can provide a negative transconductor as the output current flows into the amplifier when applying a positive input voltage. The common drain (CD) and common gate (CG) amplifier can provide positive transconductors as the output current flows out of the amplifier when applying a positive input voltage. The approach [75] shows that the FoM of G_m-C filter is the lowest number reported and move closer to the FoM's fundamental limit (see in Figure 2.9). The detail will be more discussed in section 2.1.3, 2.1.4 and Chapter 3.

2.1.2.2 Subthreshold operation

In subthreshold operation, the drain current through the transistor channel is diffusion and changes exponentially related to the gate voltage, similar to a bipolar

transistor. The subthreshold operation has become increasingly important because of its lower current and therefore lower power consumption which is well suited for biomedical applications. The transconductance efficiency (g_m/I_d) is maximized, and also the low values of V_{DSAT} enable V_{DD} minimization. However, there are disadvantageous as the exponential sensitivity of the voltage-to-current characteristic of the transistors results in a highly sensitive to transistor mismatch, power-supply noise, and temperature. The unity gain cutoff frequency is more subject to parasitics degrading energy efficiency by about a factor of two.

The drain current of a subthreshold NMOS transistor, the subthreshold slope factor (n) and I_{SS} are given by

$$I_{DS} = I_{SS}\exp\left(\frac{V_{GS}-V_{th}}{nU_T}\right)\left[1-\exp\left(-\frac{V_{DS}}{U_T}\right)\right] \tag{2.1}$$

$$n = \frac{C_{ox}+C_{jo}}{C_{ox}} \tag{2.2}$$

$$I_{ss} = 2n\mu C_{ox}U_T^2\frac{W}{L} \tag{2.3}$$

where U_T is the thermal voltage, V_{GS} and V_{DS} are the gate to source and drain to source voltages, respectively. μ is the mobility of carriers, C_{ox} is the gate oxide capacitance per unit area, and W/L is the aspect ratio of the transistor.

The drain current of a PMOS transistor is given by

$$I_{SD} = I_{SD_0}\exp\left(-\frac{V_{SD}}{nU_T}\right)\left[\exp\left(-\frac{V_{SD}}{U_T}\right)-1\right] \tag{2.4}$$

$$I_{SD_0} = I_0\exp\left(\frac{V_{SG}}{nU_T}\right) \tag{2.5}$$

The transconductance of a transistor in the subthreshold region is determined by taking the derivative of $\partial I_D/\partial V_{GS}|_{V_{DS-constant}}$ with respect to resulting in

$$g_m = \frac{I_D}{nU_T} \tag{2.6}$$

The unity gain cutoff frequency (f_T) in weak inversion is as follows:

$$f_T \cong \frac{g_m}{2\pi C_{gb}} \cong \frac{\frac{I_D C_{OX}}{U_T(C_{OX}+C_{jO})}}{2\pi\left(\frac{C_{OX}C_{jO}}{C_{OX}+C_{jO}}\right)} \cong \frac{I_D}{2\pi U_T C_{jO}} \tag{2.7}$$

In (2.6) for a fixed drain current, the transconductance of MOS transistors is maximized in the subthreshold region. In other words, a targeted value of transconductance can be achieved with less drain current in the subthreshold region than in strong inversion.

2.1.3 Existing BPF for biomedical applications

In [24, 30], the BPF is basically from a parallel RLC bandpass filter used in cochlear implant and cardiac pacemaker as shown in Figure 2.5. For synthesizing G_m-C bandpass filter, passive devices including inductors and resistors are replaced by active devices. For example, the inductors are replaced by gyrator-C which is based on two transconductance amplifiers and a capacitor. After the transformation, the inductors and resistors become electronically controllable through the setting of transconductances. Figure 2.5 (b) shows a 2nd-order G_m-C bandpass filter based RLC realized by four OTAs. The G_{m1} feeds the input while G_{m4} implements a grounded resistor. The gyrator G_{m2}, G_{m3} and C_2 acts as an inductance.

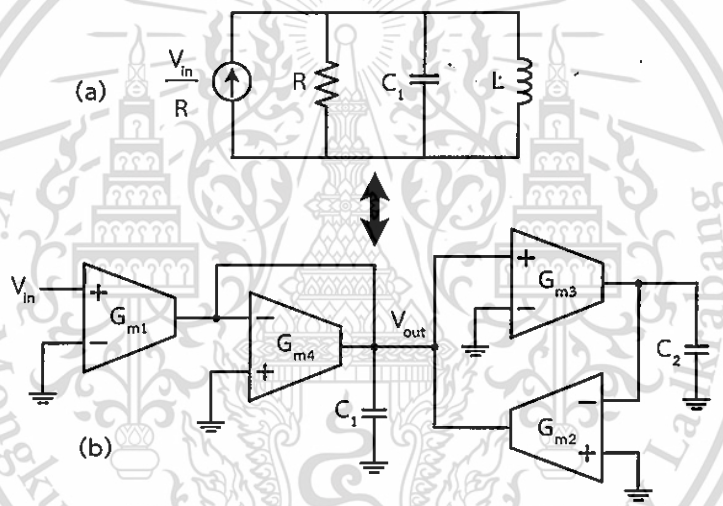

Figure 2.5 (a) Parallel RLC bandpass filter and (b) G_m-C replacement of the filter [24, 30]

The transfer function of the parallel RLC is as follow

$$H(s) = \frac{G_{m1}}{G_{m4}} \left[\frac{s\frac{G_{m4}}{C_1}}{s^2 + s\frac{G_{m4}}{C_1} + \frac{G_{m2}G_{m3}}{C_1C_2}} \right] \tag{2.8}$$

Therefore, the passband gain (K), the center frequency (ω_0) and, the quality factor (Q) are given by

$$K = \frac{G_{m1}}{G_{m4}} \quad \omega_0 = \sqrt{\frac{G_{m2}G_{m3}}{C_1C_2}} \quad Q = \sqrt{\frac{C_1C_2}{G_{m2}G_{m3}}} \frac{1}{G_{m4}} \tag{2.9}$$

At a center frequency of 1.4 kHz and quality factor of 4, the filter has 70dB of dynamic range and consumes 2.55 μW. The passband gain, ω_0 and, Q can be adjusted through the transconductances.

The ladder filter topology is widely used in several biomedical application such as wearable breathing detector [41], portable EEG systems [76] and cardiac microstimulator [29, 30]. The element replacements as active devices are also used for designing a ladder topology similarly to an RLC bandpass filter.

The BPF in [25] is basically from a cascade of first-order highpass and first-order lowpass filters. The first-order filters highpass and lowpass filter are built using transconductance amplifiers. The G_{m1} and G_{m2} effectively behave as a resistor. The capacitive-attenuation technique is used to increases the linear range of the transconductors as shown in Figure 2.6. It allows for simple scaling of attenuation ratio for adjusting the linear range. It also does not introduce harmonic distortion, and no consume static or dynamic power.

The transfer function of this filter is given by:

$$H(s) = \frac{s\frac{G_{m2}}{(A+1)C}}{s^2+s\frac{G_{m2}}{(A+1)C}+\frac{G_{m1}G_{m2}}{[(A+1)C]^2}} \tag{2.10}$$

where $C_1 = C_2 = C$

The center frequency, the quality factor (Q) and the passband gain (K) are given by

$$\omega_0 = \frac{\sqrt{G_{m1}G_{m2}}}{(A+1)C}, Q = \sqrt{\frac{G_{m1}}{G_{m2}}}, K = 1 \tag{2.11}$$

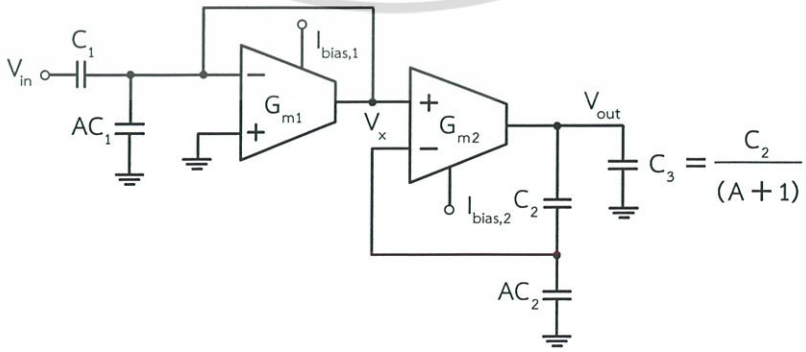

Figure 2.6 A cascade of first-order highpass and first-order lowpass filters with the capacitive-attenuation technique [25]

The structure in [77] uses the same filter topology as used in [25]. However, at the transistor level, it uses a single $M_{1,2}$ and $M_{3,4}$ transistors as resistor R_1 and R_2, respectively. This structure consists of only four MOSFETs and four capacitors without counting current sources and requires only two branches of current consumption as shown in Figure 2.7. This structure consumes only 14.4 nW which are much less than other commonly used topologies such as G_m-C. 1% THD is achieved with 80 mV_{pp} input, along with 50 mV_{rms} input-referred noise resulting in a dynamic range of 55 dB. The 4th-order filter is directly cascading two biquads with occupy 330 µm × 400 µm. The center frequency can be easily controlled via the transconductance. However, the quality depends on the ratio of C_2 and C_1 and is fixed.

The transfer function of the biquad is then derived as:

$$H(s) = -\frac{s\frac{C_1}{g_m}}{s^2\frac{C_1C_2}{g_m^2}+s\frac{C_1}{g_m}+1} \tag{2.12}$$

The center frequency, the quality factor (Q) and the passband gain (K) are given by

$$\omega_0 = \frac{g_m}{\sqrt{C_1C_2}}, Q = \sqrt{\frac{C_2}{C_1}}, K = 1 \tag{2.13}$$

A higher-order filter in [25], [77] is greatly simplified by cascading two identical 2nd-order bandpass filter stages. A simple source follower is employed as a voltage buffer to avoid the loading effect between two 2nd-order filter stage.

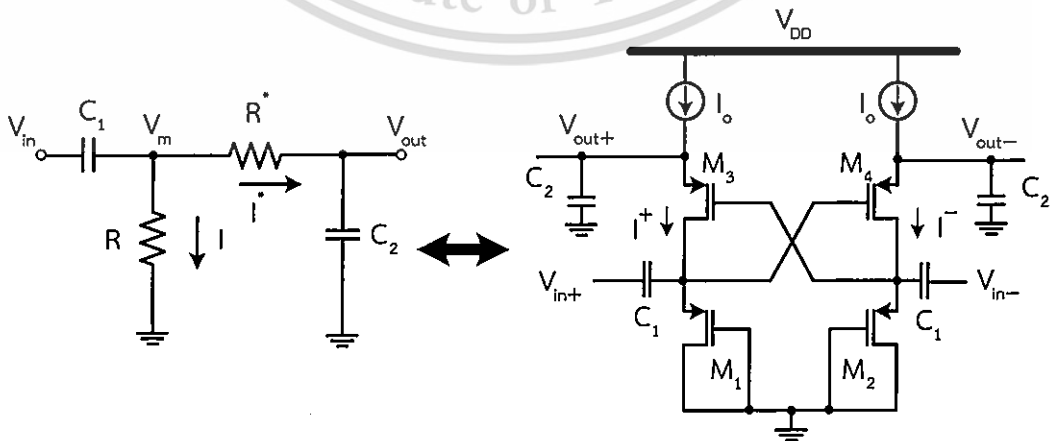

Figure 2.7 Bandpass biquad and its equivalent RC prototype [77]

In [75], the G_m-C BPF is implemented by using a single transistor as the OTAs as shown in Figure 2.8. This structure indicates that at 1 kHz center frequency, a dynamic range of 47 and 55dB (THD 1% and 5%, respectively) is obtained from 2 nW power consumption. The chip occupies 64 µm x 225 µm fabricated in a 0.18 µm CMOS process. Although this structure achieves the lowest FoM compared to other existing designs to date, the maximum value of the quality factor is limited to only 0.5 which may not be sufficient for cochlear implant and hearing aids. The maximum value of the passband gain is also limited to 0.5. To accomplish higher quality factors and gain, additional circuit elements and power consumption are thus required.

The transfer function of the bandpass filter is given by (2.14). The passband gain (K), the center frequency (ω_o) and the quality factor (Q) of the bandpass filter are given by (2.15), respectively.

$$H(s) = \frac{-s\frac{G_1}{C_2}}{S^2+s\left(\frac{G_2}{C_2}+\frac{G_1}{C_1}\right)+\frac{G_1G_2}{C_1C_2}} \tag{2.14}$$

For $G_{m1} = G_{m2} = G_m$,

$$K = \frac{C_1}{C_1+C_2}, \omega_0 = \frac{G_m}{\sqrt{C_1C_2}}, Q = \frac{\sqrt{C_1C_2}}{C_1+C_2}, \tag{2.15}$$

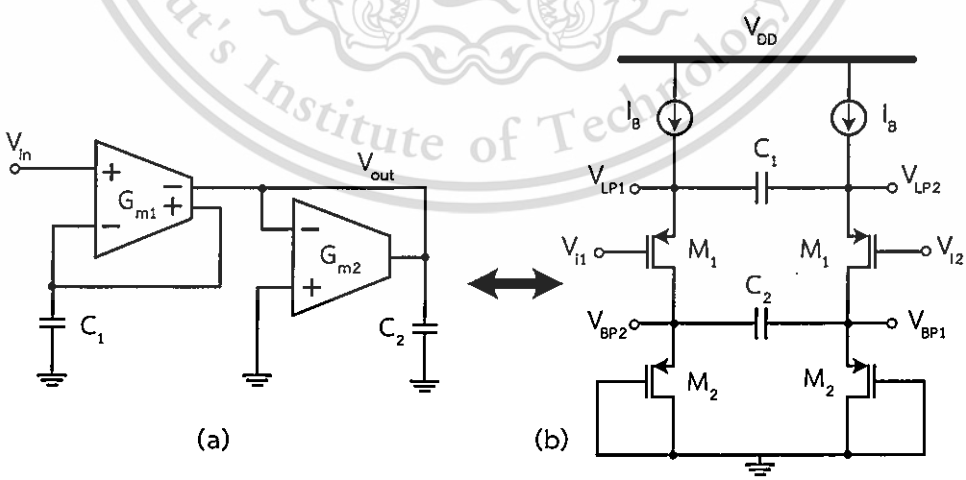

Figure 2.8 (a) Block diagram of a single-ended, 2nd-order BPF and (b) a filter implementation using a single MOSFET as a G_m element [75]

2.1.4 Figure of merit (FoM) of filter

Different filter designs are usually compared to a figure of merit (FoM) which is typically a ratio of power consumption needed to achieve the required number of poles, bandwidth and dynamic range. In the literature, there are two slightly different definitions of FoM for comparison of analog filters. Recently the FoM is defined in [41] shown in (2.16), where P is power consumption, V_{DD} is the power supply voltage, N is the filter order, f_C is the center frequency, and DR is dynamic range. The other well-known FoM is defined in [78] without V_{DD} in the numerator.

$$\mathrm{FoM} = \frac{\mathrm{P x V_{DD}}}{\mathrm{N x f_c x\ DR}} \tag{2.16}$$

For low power analog circuits that employ weak-inversion MOSFETs, reduction of the power supply voltage while retaining the same bandwidth and signal-to-noise ratio will fundamentally impose an increment of power consumption by the same factor [78]. Let's consider two exact filter designs; one operates with a higher V_{DD} and the other with a lower V_{DD}. Using the FoM without V_{DD}, the filter with a lower V_{DD} will have a larger FoM because of the fundamental increase in power consumption. Thus, the FoM without V_{DD} hides true circuit design effort and performance for low power and low voltage operation. On the other hand, the FoM with V_{DD} in (2.16) neutralizes the fundamental effect of increased power consumption as the result of scaling down V_{DD}. Thus it will reflect a fairer comparison between two filter designs with higher and lower power supply voltages.

Figure 2.9 shows the FoM versus power per pole of the filter of various biomedical BPFs collected from 2003 to 2016 [25-27, 41, 71, 75-77, 79-81]. The figure indicates that the BPF in [80] based on G_m substitution of first-order highpass and first-order lowpass filters is basically the same structure in [25]. The FoM improvement is about 10 times less than the FoM in [25] due to using a low power G_m. The filter introduced in [77] uses the same filter topology as using in [25, 80] achieved about almost an order of magnitude improvement. The reason for this is that replacing the MOSFETs behave as a resistor. This structure requires only two branches of current consumption. Recently, the BPF in [75] realized by using a single transistor as the OTAs shows a significant FoM improvement which is about 10 times less than the FoM in [77].

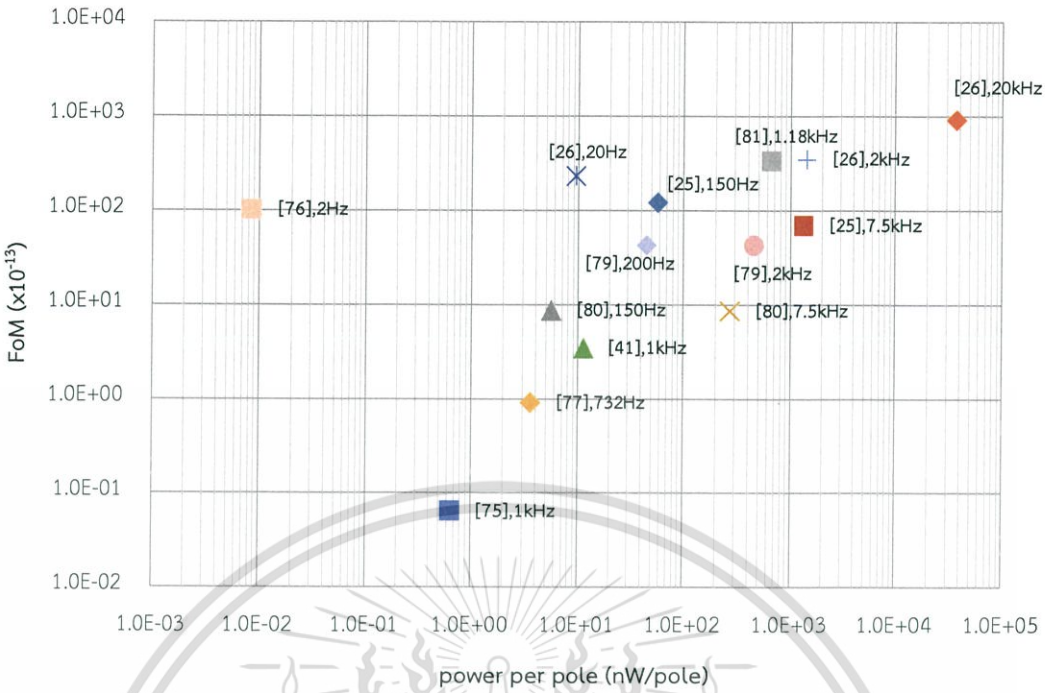

Figure 2.9 FoM versus power per pole of the filter

In this thesis, a G_m-C BPF based on the cascode gyrator-C active inductor using only a single transistor as the OTAs will be described. The capacitive attenuator is also used to improve linearity performances. The proposed bandpass filter will be described in full detail in Chapter 3.

2.2 Overview ADC for biomedical applications

2.2.1 Architecture Selection

Analog to digital converter (ADC) is one of the key building blocks that interface between analog signals and digital processing units. Fundamental architectures of analog to digital converters including SAR, Pipeline, Sigma-Delta and Flash cover most of the resolution-bandwidth space in energy efficient way. A well-known FoM of ADC is calculated to compare the performance of the ADC to provide a platform for energy efficiency comparison. This merit is used to calculate of how much energy is required to perform a conversion step. This FOM has units of energy per conversion step and is defined as

$$\mathrm{FoM} = \frac{\mathrm{P}}{\mathrm{f_s} 2^{\mathrm{ENOB}}} \tag{2.17}$$

$$\mathrm{ENOB} = \frac{\mathrm{SNDR}-1.67}{6.02} \tag{2.18}$$

where ENOB is the effective number of bits, calculated from SNDR in (2.18), and f_S is the sampling frequency of the signal. SNDR is the signal-to-noise-distortion ratio in dB measured with a sinusoidal input. Figure 2.10 shows the FoM and sampling frequency for all ADCs published in ISSCC and VLSI between 2000 and 2016 and logarithmic ADC for biomedical applications (data adapted from [82]).

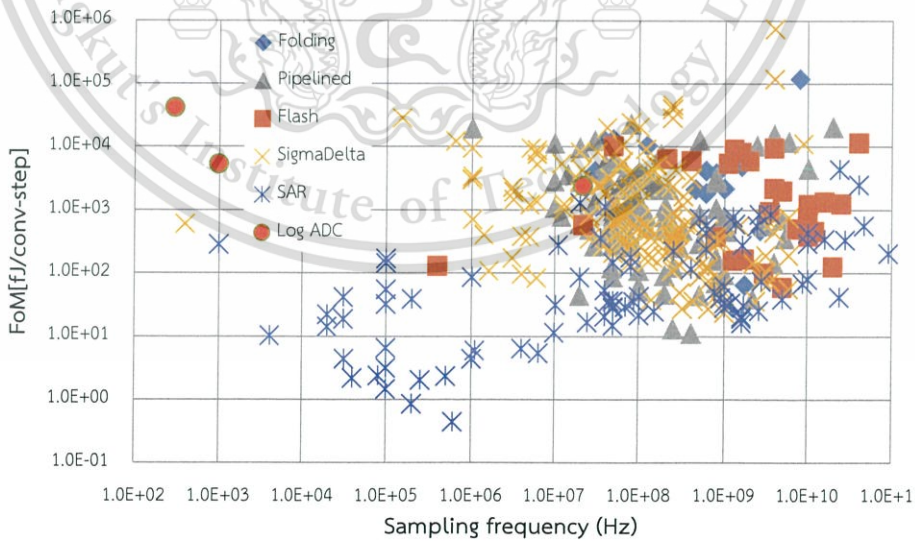

Figure 2.10 The FoM and sampling frequency of fundamental architectures published ISSCC and VLSI between 2000 and 2016 and logarithmic ADC for biomedical applications (data adapted from [82]

The figure indicates that among various ADC architectures, the SAR architecture has demonstrated the highest power efficiency over other architectures for all sampling frequencies.

2.2.2 The Successive Approximation ADC

The SAR architecture basically consists of four basic building blocks: sample and hold (S&H), DAC (typically composed of N-bit binary-weighted capacitor), comparator and SAR control logic. The block diagram of SAR ADC is shown in Figure 2.11. The operation is as follow: The comparator starts with comparing the input voltage with the threshold voltage levels from the DAC which equal to mid-full-scale-level to generate MSB. Depending on the comparison outcome, the output comparator is then processed by the digital control logic, which generates a control signal to the DAC. This feedback logic performs a binary search to find the correct digital output bits to minimize the difference between the DAC voltage and the analog input. The conversion is successively from the most significant bit (MSB) to the least significant bit (LSB). It requires N clock cycles and thus, N comparisons to complete a conversion. The binary search takes time-consuming to complete a conversion. However, it significantly relaxes the hardware complexity because all N comparisons share and uses the same set of hardware.

There are some disadvantages of the SAR ADC architecture as follows:

- The operation SAR architecture is a serial nature so that this architecture is suited for moderate speeds.
- The number of unit capacitors for an N-bit SAR ADC is required as $2^{N}C_{unit}$ for single-ended implementation and 2^{N+1} C_{unit} for differential implementation. Therefore the resolution of ADC is limited by the number of unit capacitors.
- The offset comparator noise causes performance degradation of the ADC.

2.2.3 Nonlinear ADC for biomedical applications

Recently, the designs of signal-specific nonlinear ADCs have been proposed. In general, signals can be divided into mainly three types depending on the concentration of information in the amplitude domain [83]:

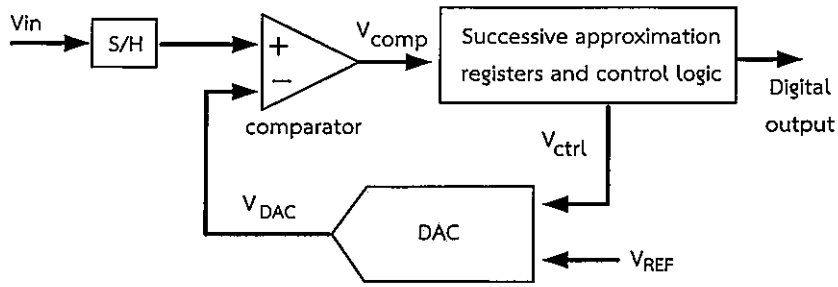

Figure 2.11 The block diagram of SAR ADC

1) Non-concentrated information (NCI) is defined as a uniformly distributed signal which is normally converted by linear ADC.

2) Information concentration at low amplitude (ICLA) is defined as the concentrated information is more of the lower side of amplitude signal. It means that the lower amplitude is more the resolution in the quantization than the higher amplitude. A logarithmic ADC is used to perform ADC with non-uniform quantization step for this type

3) Information concentration at high amplitude (ICHA) is defined as the concentrated information is more emphasis on the higher side of amplitude signal. This means that for large amplitudes the signals are quantized with fine resolution. An exponential ADC is realized to perform ADC for this type.

Various nonlinear ADC types have been proposed for several biomedical applications such as cochlear implant, neural recording and stimulation in the literature. In [84] proposed logarithmic ADC for cochlear implant, the logarithmic ADC is used to compress the wide range envelope signal to narrower signal as shown in Figure 2.2. For normal-hearing listeners can detect about 200 discriminable intensity steps within their dynamic range, while implant patients can only discriminate between 8–50 intensity steps. Thus, the compressed signals are not more than 30-dB dynamic range with a typical value being about 10 dB [84]. The compressed signals are transmitted through the skin via the telemetry system to the implanted receiver stimulator to stimulate the electrodes in the cochlear. Therefore, 6-bit logarithmic ADC is sufficient. The logarithmic ADC requires at least 60-dB dynamic range, 300 Hz sampling rate and 6 physical bits to handle the envelope variation in speech.

In neural recording and DBS, spike and LFP signals are normally processed separately in the frequency domain where each signal is filtered and amplified with isolated signal paths. This results in a large number of amplifiers and filters that lead to higher power dissipation and chip area. However, both spike and LFP signals are important for prosthetics and neuroscience interpretation, and it is thus optimal to measure both signals simultaneously. Features of the LFP signals, in particular, the energy of LFPs, have emerged as more effective feedback indicators for DBS. The approach in [11, 13] presents a wide dynamic range logarithmic pipeline ADC can replace the analog filtering to measure both signals simultaneously. Figure 2.12 shows a block diagram of the analog front-end log-based closed-loop DBS system. This approach can save power consumption and area as it requires less number of bits while achieving the same DR compared to a conventional linear ADC. A logarithmic ADC is used to digitize neural signals in a small number of bits while preserving the high DR characteristic of neural signals. The sampling rate should be more than 20 kHz, and the required dynamic range should be 60 dB due to the differences in both amplitude and frequency contents of spikes and LFPs (see Table 2.1).

In [83], the piecewise-linearly-approximated exponential, two-step SAR ADC is proposed to digitize spike signals. It is assumed that the spikes are already amplified. These signals are quantized with fine resolution while the small background noise is quantized with coarse resolution. This exponential ADC achieves higher resolution with the same number of physical bits compared with linear ADC, less transition causing lower power consumption and lower background noise.

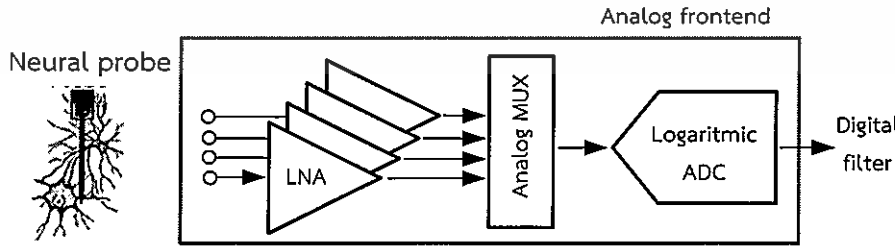

Figure 2.12 a block diagram of the analog front-end log-based closed-loop DBS system

Table 2.2 Nonlinear ADC required performance

Applications	ADC type	ADC required performance		
		DR (dB)	fs	resolution
Cochlear implant [84]	Logarithmic	60	>300Hz	6
Neural recording and DBS [11, 13]	Logarithmic	60	>20 k	Depending on current stimulator resolution
Spikes recording [83]	Exponential	60	>20 k	n/a

In this thesis, a logarithmic SAR ADC is proposed for cochlear implant system, neural recording and close-loop deep brain stimulation. The proposed ADC will be described in Chapter 4.

2.2.4 Logarithmic ADC

A logarithmic ADC can be realized either by using a nonlinear device with a linear ADC [84] or by performing the required signal operations in the logarithmic domain with conventional ADC architectures such as pipeline [11, 13, 85], cyclic [86], or lookup table [87]. For example, logarithmic pipeline ADC, converting signal operations of a linear ADC to its logarithmic counterpart involves replacing subtraction with division (or multiplication) and multiplication-by-two with squaring. In logarithmic SAR ADC, a straightforward method to realize is to employ the conventional linear SAR ADC structure and substitute the linear charge-redistribution digital to analog converter (DAC) with a logarithmic counterpart.

The logarithmic ADC performs analog-to-digital conversions with non-uniform quantization, in another word; the LSB size varies with the input signal level. Small analog input amplitudes are quantized with fine resolution, while large analog input amplitudes are quantized with coarse resolution.

An N-bit logarithmic ADC converts an analog input voltage (V_{in}) to an N-bit digital output code (D_{out}) according to a logarithmic mapping described by (2.19)

$$D_{out} = \frac{2^N}{C} \cdot \log_b \left(\frac{V_{in}}{V_{FS}} \cdot b^C \right) \tag{2.19}$$

where N is the number of bits, b is the base of the logarithmic function, C is defined as the code efficiency factor, and V_{FS} is the full-scale analog input voltage range.

The ADC's logarithmic mapping relationship in (2.19) can be adjusted by the values of C and b. The input voltage is divided by the full-scale ADC analog input range, mapping the input to a nominal range from 0 to 1. Figure 2.13 shows characteristic of an ideal 3-bit logarithmic ADC with assorted values of b and C with V_{FS}=1 V while threshold voltage levels, LSB_{min}, and DR of 3-bit logarithmic ADC with assorted values of b and C are summarized in Table 2.3. It can be deduced that larger values of C and b will result in a more nonlinear logarithmic mapping, which emphasizes on the conversion of small input amplitudes and yields a larger DR.

In contrast to an N-bit linear ADC which has a constant LSB (least significant bit) size of $V_{FS}/2^N$, the LSB size of an N-bit logarithmic ADC varies with the input amplitudes. For small input amplitudes, the LSB size is small and has the minimum value of (2.20) when D_{out} changes from 0 to 1. For large input amplitudes, the LSB size is larger and has the maximum value of (2.21) when D_{out} changes from code 2^N-2 to 2^N-1 Note that the logarithm of the LSB size is constant for a logarithmic ADC.

$$LSB_{min} = V_{FS} \cdot b^{-C} \cdot \left(b^{C/2^N} - 1\right) \tag{2.20}$$

$$LSB_{max} = V_{FS}\left(1 - b^{-C/2^N}\right) \tag{2.21}$$

The DR of an ADC is defined by the ratio of the maximum input amplitude to the minimum resolvable input amplitude. Thus, in theory, the DR in decibels of an N-bit linear ADC is equal to $20\log_{10}(2^N)$, while the DR of an N-bit logarithmic ADC is given by (2.22).

$$DR = 20\log_{10}\left(\frac{V_{FS}}{LSB_{min}}\right) = 20\log_{10}\left(\frac{b^C}{b^{C/2^N}-1}\right) \tag{2.22}$$

2.2.5 Performance parameter of logarithmic ADC

2.2.5.1 Static Parameters

Static parameters refer to the performance of the ADC on some static or dc input voltage. The most common static metrics include differential nonlinearity (DNL), integral nonlinearity (INL), offset error and gain error. The offset error is the output occurring for the input code that should produce zero output.

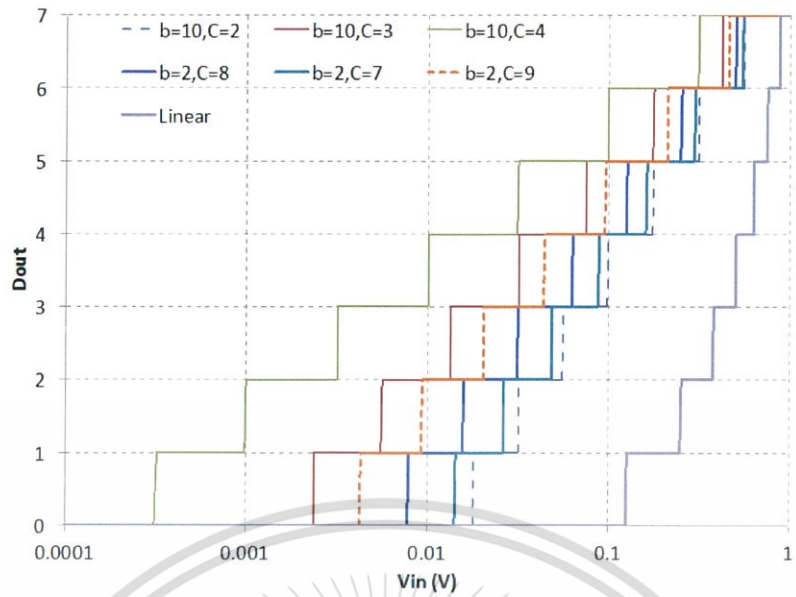

Figure 2.13 Characteristic of an ideal 3-bit logADC with assorted values of b and C

Table 2.3 Threshold voltage levels, LSB_{min}, and DR of 3-bit logarithmic ADC with assorted values of b and C

$V_{in,th}$ (V)	b=10,C=2	b=10,C=3	b=10,C=4	b=2,C=7	b=2,C=8	b=2,C=9	Linear ADC
D_{out}=7	0.562341325	0.421696503	0.316227766	0.545253866	0.5	0.458502022	0.875
D_{out}=6	0.316227766	0.177827941	0.1	0.297301779	0.25	0.210224104	0.75
D_{out}=5	0.177827941	0.074989421	0.031622777	0.162104944	0.125	0.096388177	0.625
D_{out}=4	0.1	0.031622777	0.01	0.088388348	0.0625	0.044194174	0.5
D_{out}=3	0.056234133	0.013335214	0.003162278	0.048194088	0.03125	0.020263118	0.375
D_{out}=2	0.031622777	0.005623413	0.001	0.026278013	0.015625	0.009290681	0.25
D_{out}=1	0.017782794	0.002371374	0.000316228	0.014328188	0.0078125	0.004259796	0.125
D_{out}=0	0.01	0.001	0.0001	0.0078125	0.00390625	0.001953125	0
LSB_{min} (mV)	7.783	1.371	0.216	6.516	3.906	2.307	0.125
DR (dB)	42.18	57.26	73.30	43.72	48.16	52.74	18.06

The gain error quantifies the slope deviation of the transfer function from the actual staircase slope when the offset error has been reduced to zero. For test and measurement, offset error and gain error are important error sources and need to be removed or calibrated out.

The INL error is used to measure of accuracy that specifies the deviation of a converter's input–output relationship away from ideal straight line transfer function. Since it is the total deviation from the ideal straight line transfer function, the INL for a specific code can be obtained by summing all the previous DNL's up to that code. The DNL is defined as the deviation of the actual step size from the ideal step size that causes the transition. Linear ADC step-size is the smallest change in input voltage required, obtaining a unit change in the output code. V_{LSB} is equal to $V_{REF}/2^N$ for an N-bit ADC. Typically, INL and DNL are measured by slowly sweeping the converter input over its full-scale range. Both DNL and INL are usually expressed as a fraction of the ideal LSB size.

In a logarithmic ADC, the definitions of DNL and INL for a logarithmic ADC are similar to a linear ADC except that in a logarithmic ADC the ideal step size is different for each code. A logarithmic LSB size is defined by the difference of the logarithm of the analog input amplitudes for two adjacent digital output codes, D_{n+1} and D_n. The logarithmic LSB size, expressed in decibel, is a constant value for fixed values of C and N, and it is independent of the analog input level and the full-scale input range. The logarithmic LSB size, the INL and DNL are given by

$$\mathrm{LSB_n(dB)} = \log_{10}\left(i_N(D_{n+1})\right) - \log_{10}\left(i_N(D_n)\right) = \frac{C}{2^N} \tag{2.23}$$

$$\mathrm{DNL_n} = \frac{\mathrm{LSB_{n,ideal}(dB) - LSB_{n,actual}(dB)}}{\mathrm{LSB_{n,ideal}(dB)}} \tag{2.24}$$

$$\mathrm{INL_n} = \sum_{i=0}^{n} \mathrm{DNL_i(dB)} \tag{2.25}$$

2.2.5.2 Dynamic Parameters

Dynamic parameters are used to evaluate the ADC performance with a time-varying input voltage signals. Some of the important dynamic performance parameters are Signal-to-Noise Ratio (SNR), Signal-to-Noise and Distortion Ratio (SNDR) and Effective Number of Bits (ENOB).

Table 2.4 Comparison performance parameter between linear and logarithmic ADC

Parameters	Linear ADC	Log ADC
Resolution	the number of bits at the output of ADC	Physical: the number of bits at the output of ADC Max resulution: the minimum resolvable input amplitude
LSB size	$LSB_{constant} = V_{FS}/2^N$	$LSB_{min} = V_{FS} \cdot b^{-C} \cdot \left(b^{C/2^N} - 1\right)$ $LSB_{max} = V_{FS}\left(1 - b^{-C/2^N}\right)$ $LSB_n(dB) = \log_{10}\left(i_N(D_{n+1})\right) - \log_{10}\left(i_N(D_n)\right) = \frac{C}{2^N}$
DR	$DR = 20\log_{10}(2^N)$	$DR = 20\log_{10}\left(\frac{b^C}{b^{C/2^N} - 1}\right)$
INL	$INL_n = \sum_{i=0}^{n} DNL_i$	$INL_n = \sum_{i=0}^{n} DNL_i(dB)$
DNL	$DNL_n = \left(\frac{V_{in}(i+1) - V_{in}(i)}{V_{LSB,ideal}}\right)$	$DNL_n = \frac{LSB_{n,ideal}(dB) - LSB_{n,actual}(dB)}{LSB_{n,ideal}(dB)}$
SNDR	sinusoidal input	exponential input
ENOB	$ENOB = \frac{SNDR^* - 1.76}{6.02}$ (*) (* sinusoidal input)	$ENOB = \frac{SNDR^{**} - 1.76}{6.02}$ (** exponential input)

In a linear ADC, to measure these parameters, a pure sinusoid input is applied to the ADC, and the ADC output spectrum is analyzed using Fast Fourier Transform (FFT). SNR is the ratio of sinusoid power to total noise power excluding harmonic distortion. The ratio of sinusoid power to total noise power at the output is the SNDR of the ADC.

In logarithmic ADC, a pure sinusoidal waveform input signal is not a suitable to evaluate the SNDR of the ADC as a digital representation of a waveform which is a logarithmic function of the input. Instead, an exponential function of a sinusoidal waveform is more appropriate because the digital output codes will give a uniform representation of the sinusoidal waveform. The definitions of ENOB, SNR and SNDR are still similar to a linear ADC.

Comparison performance parameter between linear ADC and Logarithmic ADC are summarized in Table 2.4.

Chapter 3

Low-power Tunable High-Q 4th-order G_m-C BPF

This chapter present the realization of the low-power tunable high-Q G_m-C bandpass filter suitable for many biomedical applications that require low-frequency, wide-tuning range as well as ultra-low power and low voltage operation. The work in this chapter was originally published in [92] used in RF applications. The filter is based on the cascode gyrator-C active inductor using only a single transistor as the transconductance element. The filter structure in [92] provides circuit's simplicity and requires a minimum number of active elements (only two G_m cells) leading to consume the power. Moreover, the passband gain, the center frequency and the quality factor can be easily controlled via the transconductance. The high-Quality factor is improved by the cascode active inductor and negative resistance. In this chapter a programmable current generator based on self-cascode MOSFET and self-biased circuit with a 3-bit DAC is introduced to adjust the center frequency. The capacitive input attenuation technique is employed to improve the linearity of the filter as it does not introduce harmonic distortion.

This chapter is organized as follows: Section 3.1 presents design specifications and considerations realization of the BPF. The G_m-C bandpass filter based on the cascode gyrator-C active inductor which consumes only a few nanowatts of power dissipation is described 3.2. Noise analysis and programmable bias current generator are introduced in the subsequent section. Sections 3.2 and 3.3 present the post-layout simulation results and conclusion, respectively.

3.1 Realization of the bandpass filter for biomedical applications

3.1.1 2nd-order and 4th-order bandpass filter circuits

A 2nd-order G_m-C bandpass filter is realized by adding a coupling capacitor to the gyrator-C active inductor, as shown in Figure 3.1 (a). A simple analysis can show that the transfer function of the bandpass filter is given by (3.1), where G_{o1} and G_{o2} are the output conductances of G_{m1} and G_{m2}, respectively. It can be shown that the passband gain (K), the center frequency (ω_o) and the quality factor (Q) of the bandpass filter are given by (3.2)-(3.4), respectively.

$$H(s) \cong \frac{K \cdot s\left(\frac{G_{o2}}{C_2+C_{in}}+\frac{G_{o1}}{C_1}\right)}{s^2+s\left(\frac{G_{o2}}{C_2+C_{in}}+\frac{G_{o1}}{C_1}\right)+\frac{G_{m1}G_{m2}}{C_1(C_2+C_{in})}} \quad (3.1)$$

$$K = \frac{G_{m1}C_{in}}{G_{o2}C_1+G_{o1}(C_{in}+C_2)} \quad (3.2)$$

$$\omega_o = \sqrt{\frac{G_{m1}G_{m2}}{C_1(C_2+C_{in})}} \quad (3.2)$$

$$Q = \frac{\sqrt{G_{m1}G_{m2}C_1(C_{in}+C_2)}}{G_{o2}C_1+G_{o1}(C_{in}+C_2)} \quad (3.4)$$

Figure 3.1 (b) shows a simple single-ended realization of the 2nd-order bandpass filter by using a single MOSFET as the transconductance element. The common-gate stage M_1 and the common-source stage M_2 realize G_{m1} and G_{m2}, respectively. Both MOSFETs are biased to operate in the weak inversion region in order to achieve large transconductance-to-current efficiency (g_m/I_D). The capacitive attenuation of the input signal, formed by C_{in} and C_2, helps reducing signal distortion from large input voltage signals.

Figure 3.2 shows a fully-differential realization of the 2nd-order bandpass filter, which is employed to suppress even harmonic distortions and to increase signal swing. The quality factor of the single-ended filter is limited by large G_{o1} and G_{o2}.

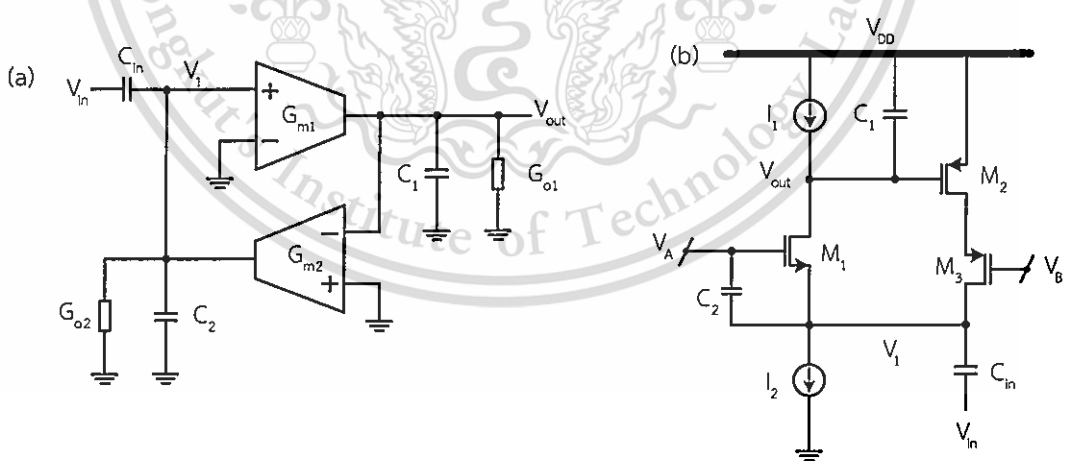

Figure 3.1 (a) Block diagram of a single-ended, 2nd-order bandpass filter topology and (b) a filter implementation using a single MOSFET as a G_m element

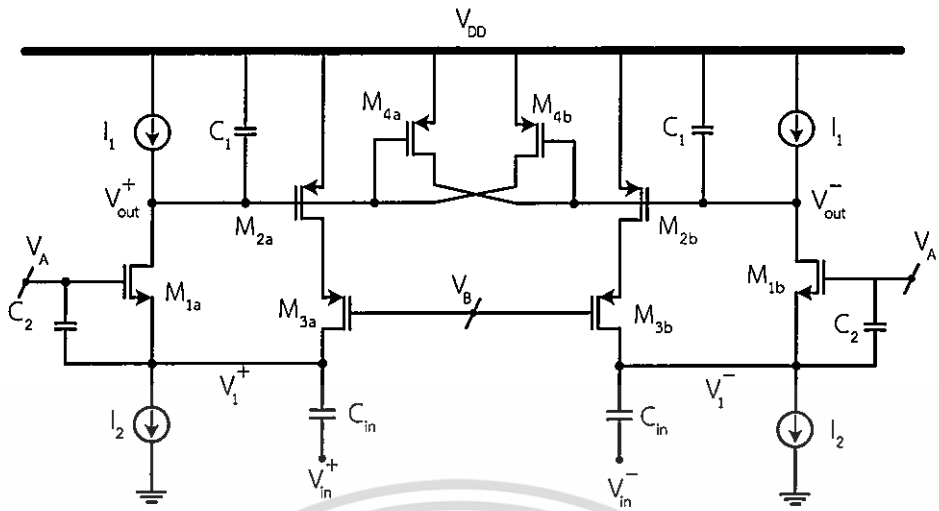

Figure 3.2 The proposed schematic diagram of a fully-differential 2nd-order bandpass filter

In the fully-differential implementation, cascode transistors ($M_{3a,b}$) are used to reduce G_{o2} and a differential cross-coupled negative resistor, realized by $M_{4a,b}$, is used to reduce G_{o1}. From the differential cross-coupled negative resistor shown in Figure 3.2, the output conductances of G_{m1} is reduced from $G_{o1} \approx \frac{1}{r_{oI1//gm1}r_{o1}r_{oI2}}$ to $G_{o1}{}' \approx G_{o1} - g_{m4}$. Using cascode transistors, the output conductances of G_{m2} is reduced from $G_{o2} \approx \frac{1}{r_{o2}} // \frac{1}{g_{m1}}$ to $G_{o2}{}' \approx \frac{1}{g_{m2}r_{o2}r_{o3}} // \frac{1}{g_{m1}}$ where $r_{oI1,I2}$ is drain-source resistance of the non-ideal bias current source and r_{o1} is drain-source resistance of the M_1. Thus the quality factor and passband gain of the filter can be enhanced given by $Q = \frac{\sqrt{G_{m1}G_{m2}C_1(C_{in}+C_2)}}{G_{o2}{}'C_1+G_{o1}{}'(C_{in}+C_2)}$ and $K = \frac{G_{m1}C_{in}}{G_{o2}{}'C_1+G_{o1}{}'(C_{in}+C_2)}$, respectively.

Since M_1 and M_2 are biased in the subthreshold region, their transconductances are directly proportional to their bias currents, as described by (3.5), where U_T is the thermal voltage and n is the subthreshold slope factor. Hence, varying the bias currents I_1 and I_2 change G_{m1} and G_{m2}, respectively, thus the center frequency and quality factor of the filter can be tuned. In this work, I_2 is equal to NI_1, where N is a current scaling factor. The center frequency of the filter can be adjusted by varying I_1. The Q-value of the filter can be adjusted by changing the value of I_1 and N.

$$G_{m1,2} \approx g_{m1,2} = \frac{I_{D1,2}}{nU_T} \tag{3.5}$$

One advantage of the filter topology in Figure 3.2 is that a higher-order bandpass filter can be easily realized by directly cascading a number of 2^{nd}-order filter stages, thanks to the input coupling capacitor. Furthermore, the DC operating points of each 2^{nd}-order filter stage can be optimized independently thus the design of a higher-order filter is greatly simplified. Hence, a 4^{th}-order bandpass filter, which is realized by cascading two identical 2^{nd}-order bandpass filter stages, is demonstrated. A simple source follower is employed as a voltage buffer to avoid the loading effect between two 2^{nd}-order filter stages, as depicted in Figure 3.3

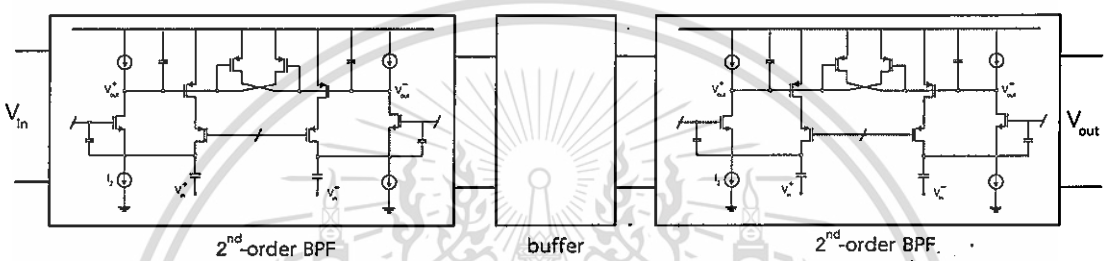

Figure 3.3 Block diagram of cascaded 4^{th} -order BPF

3.1.2 Noise analysis

Noise of the single-ended 2^{nd}-order bandpass filter can analyze by considering the noise model of the gyrator-C active inductor in Figure 3.4 (a), where $Y_1=sC_1+G_{o1}$, $Y_2=sC_2+G_{o2}$, and $\overline{v_{ni1}^2}$ and $\overline{v_{ni2}^2}$ are the total input-referred mean square noise voltage sources of G_{m1} and G_{m2}, respectively. By performing an elementary noise analysis, it is straightforward to show that Figure 3.4 (a) can be equivalently represented by Figure 3.4 (b), where the mean-square voltage and current noise generators are respectively given by (3.6) and (3.7). Thus the total input-referred mean square noise voltage of Figure 3.4 (b) can be described by (3.8), where $Y_{in} = (Y_1Y_2 + G_{m1}G_{m2})/Y_1$ is the equivalent admittance of the gyrator-C active inductor at node 2.

$$\overline{v_n^2} = \overline{v_{ni1}^2} \tag{3.6}$$

$$\overline{i_n^2} = Y_2^2 \cdot \overline{v_{ni1}^2} + G_{m2}^2 \cdot \overline{v_{ni2}^2} \tag{3.7}$$

$$\overline{v_{nt2}^2} = \overline{v_n^2} + \frac{\overline{i_n^2}}{Y_{in}^2} = \overline{v_{ni1}^2}\left(1 + \left(\frac{Y_2}{Y_{in}}\right)^2\right) + \left(\frac{G_{m2}^2}{Y_{in}^2}\right)\overline{v_{ni2}^2} \tag{3.8}$$

Using Figure 3.4 (b) and (3.8), the noise model of the 2nd-order bandpass filter can be simplified to Figure 3.4 (c), and the total input-referred mean square noise voltage of the filter can be described by (3.9), which reveals that noise of the active inductor is multiplied by a factor of $\left(1+\frac{Y_{in}}{sC_{in}}\right)^2$ when it is referred to the input of the filter. Note that the term $\left|\frac{Y_{in}}{sC_{in}}\right| > 1$ at low center frequencies and $\left|\frac{Y_{in}}{sC_{in}}\right| < 1$ at high center frequencies. Therefore, the input-referred noise of the bandpass filter will be approximately equal to the noise of the active inductor at high center frequencies, and it will be larger when the filter is tuned to low center frequencies.

$$\overline{v_n^2} = \overline{v_{nt2}^2}\left(1+\frac{Y_{in}}{sC_{in}}\right)^2 \tag{3.9}$$

Let's now calculate $\overline{v_{ni1}^2}$ and $\overline{v_{ni2}^2}$ of the fully-differential 2nd-order bandpass filter in Figure 3.2. Since the circuit is fully symmetrical, noise can be calculated by considering half of the circuit as redrawn with associated noise sources in Figure 3.5 (a). Weak-inversion MOSFETs M_5 and M_6 realize the DC bias current sources, I_1 and I_2, respectively. Comparing the circuit in Figure 3.2 and Figure 3.5 (a), it can be recognized that G_{m1} is realized by a CG circuit in Figure 3.5 (b) and G_{m2} is realized by a cascode circuit in Figure 3.5 (c). Thus, by calculating the input-referred noise sources of Figure 3.5 (b) and Figure 3.5 (c) and assuming that $g_m >> g_o$, $\overline{v_{ni1}^2}$ and $\overline{v_{ni2}^2}$ can be approximately described by (3.10) and (3.11), respectively, where $\overline{i_{ndj}^2}$ is the drain current noise source of MOSFET M_j.

$$\overline{v_{ni1}^2} = \frac{\overline{i_{nd1}^2}+\overline{i_{nd4}^2}+\overline{i_{nd5}^2}}{g_{m1}^2} \tag{3.10}$$

$$\overline{v_{ni2}^2} = \frac{\overline{i_{nd2}^2}+\overline{i_{nd3}^2}+\overline{i_{nd6}^2}}{g_{m2}^2} \tag{3.11}$$

In this work, the gate area of each MOSFET is chosen to be sufficiently large so that the drain current noise is dominated by the thermal noise, and the flicker noise can be neglected. In Figure 3.2, the DC bias currents of $M_{1a,b}$ are equal to $I_{M1a,b}=I_1+I_{M4a,b}$ and the DC bias currents of $M_{2a,b}$ are equal to $I_{M2a,b}= I_2-I_{M1a,b} =(N-1)I_1-I_{M4a,b}$. In this work, the aspect ratios of $M_{4a,b}$ are much smaller than those of $M_{2a,b}$, thus $I_{M4a,b}$ is much smaller than $I_{M2a,b}$. Hence, $I_{M1a,b}\approx I_1$ and $I_{M2a,b}\approx (N-1)I_1$. Since all

MOSFETs are biased in the weak inversion region, the thermal drain current noise sources of M_1-M_5 can be described as

$$\overline{i_{nd1}^2} = 2qI_1\Delta f, \tag{3.12}$$

$$\overline{i_{nd2}^2} = 2qI_1(N-1)\Delta f, \tag{3.13}$$

$$\overline{i_{nd3}^2} = 2qI_1(N-1)\Delta f, \tag{3.14}$$

$$\overline{i_{nd4}^2} = 2qI_1\alpha(N-1)\Delta f, \tag{3.15}$$

$$\overline{i_{nd5}^2} = 2qI_1\Delta f \tag{3.16}$$

$$\overline{i_{nd6}^2} = 2qNI_1\Delta f, \tag{3.17}$$

where q is the electron charge, Δf is the bandwidth of interest and $\alpha = \frac{(W/L)_4}{(W/L)_2} \ll 1.$, The noise contribution of the cascode transconductor M_3 and the negative resistor M_4 can be negligible due to the degeneration at relatively low center frequency and $\alpha \ll 1$ respectively. Therefore, the primary noise sources are M_1, M_2, M_5 and M_6. By substituting the MOSFETs' drain current noise sources into (3.10) and (3.11) and using the relationships in (3.6)-(3.9), the total equivalent input-referred mean square noise voltage of the 2nd-order bandpass filter can be described by (3.18).

$$\frac{\overline{v_{ni}^2}}{\Delta f} = \left(1+\frac{Y_{in}}{sC_{in}}\right)^2 \cdot \left[\frac{4qI_1}{G_{m1}^2}\left(1+\left(\frac{Y_2}{Y_{in}}\right)^2\right)+\frac{2qI_1(2N-1)}{Y_{in}^2}\right] \tag{3.18}$$

The right-hand side of (3.18) consists of two terms in the square bracket. The first term is the noise contribution of G_{m1} (the CG transconductor), while the second term is the noise contribution of G_{m2} (the cascode transconductor). Since $G_{m1} = I_1/nU_T$, it can be deduced from (3.18) that increasing I_1 will reduce the noise contribution of G_{m1} while increasing the noise contribution of G_{m2}. At low center frequencies (i.e. small I_1), noise contribution of G_{m1} will be more dominant. Therefore, designing the filter for lowest noise performance may be obtained by choosing an optimal value of I_1. However, the choice of I_1 is not completely independent as it also affects the center frequency and the Q-value of the filter. Furthermore, (3.17), also suggests that the noise contribution of G_{m2} will be dominant when N is large (i.e. for higher filter Q values).

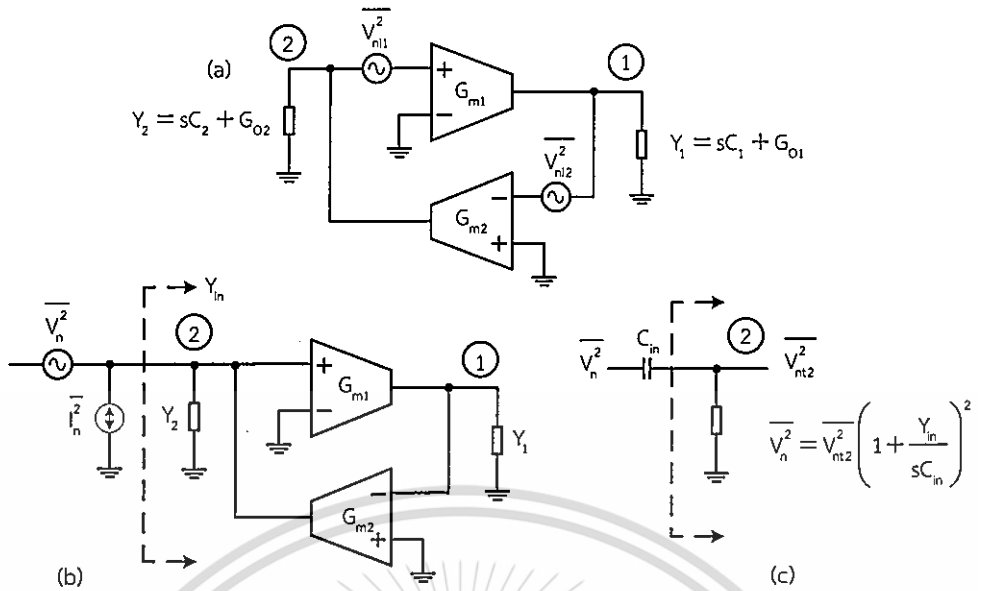

Figure 3.4 (a) Noise model of a gyrator-C active inductor, (b) equivalent noise generators of a gyrator-C active inductor, and (c) equivalent noise model of the 2^{nd}-order bandpass filter.

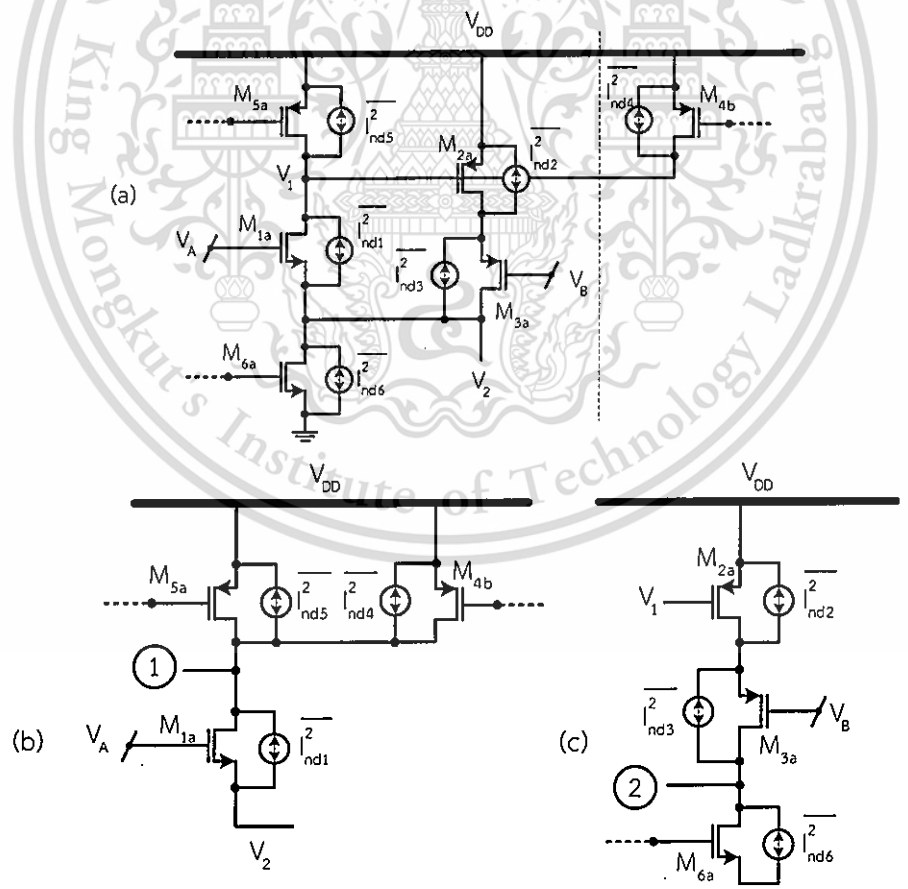

Figure 3.5 Circuits with associated noise sources for noise analysis: (a) the 2^{nd}-order bandpass filter (b) the common-gate stage (G_{m1}), and (c) the cascode stage (G_{m2}).

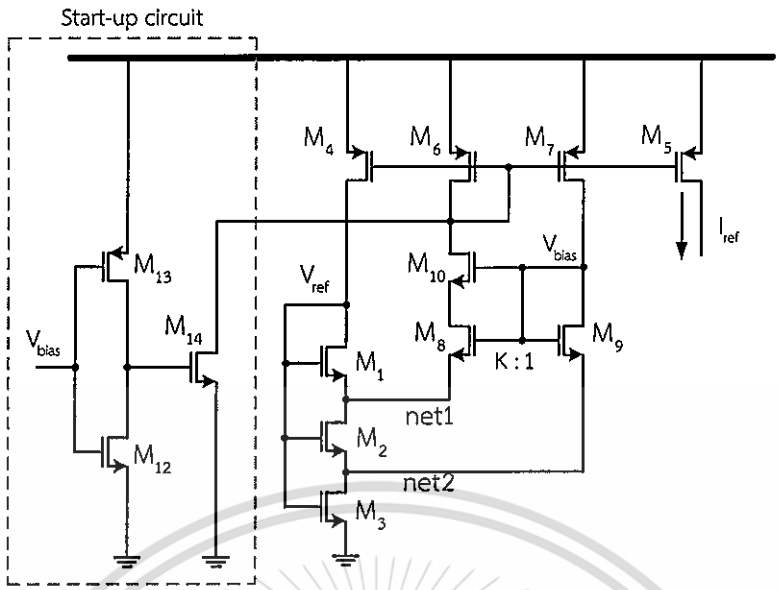

Figure 3.6 Schematic diagram of a PTAT current reference

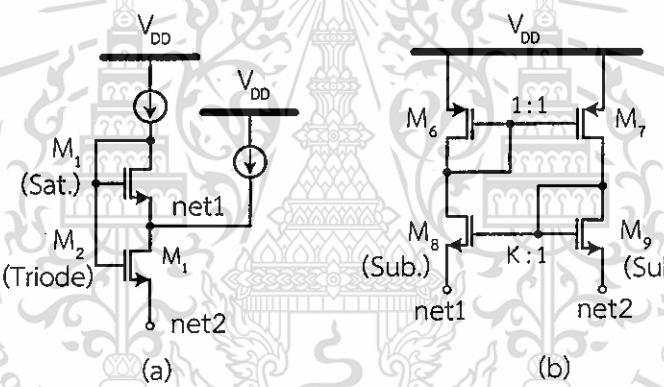

Figure 3.7 Schematic diagram of a) the self-cascode MOSFET b) self-biased circuit

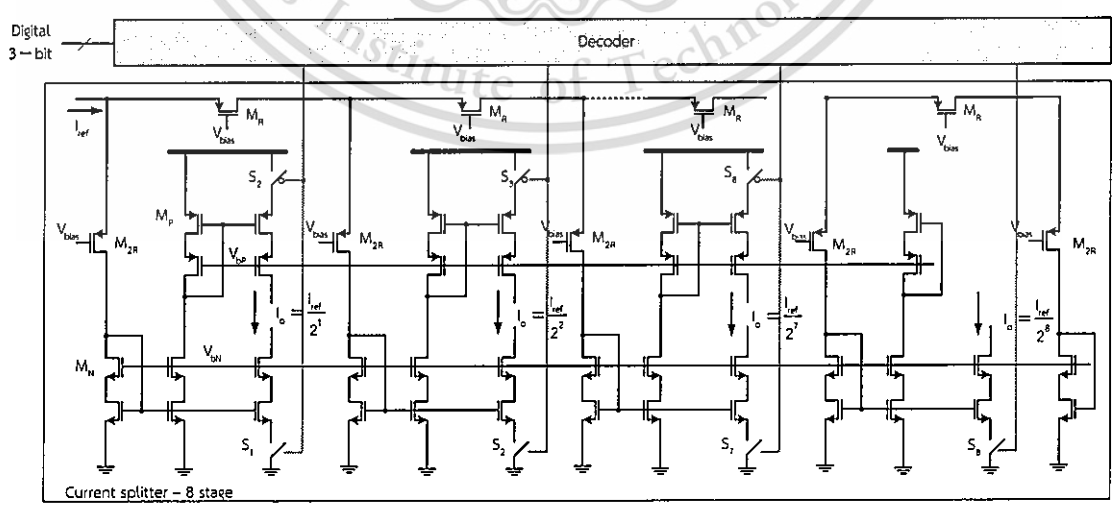

Figure 3.8 Schematic diagram of a binary weight current splitting and a decoder

3.1.3 Programmable bias current generator

In this work, the center frequency of the proposed filter can be adjusted by controlling the filter bias currents. A programmable current generator consists of a process, voltage-insensitive (PTAT) current reference (I_{REF}), a 3-bit, R-2R current divider, and a digital decoder represented in Figure 3.6 and Figure 3.8, respectively.

The PTAT current reference using a MOSFET based on the structure [88, 89] is shown in Figure 3.6. The current reference consists of two main functional elements as a self-cascode MOSFET (SCM) and a self-biased circuit (SBC) as shown in Figure 3.7. Transistor M_8 and M_9 operate in weak inversion region. The currents flowing through M_8 and M_9 can be expressed as

$$I_{M8} = S_{M8} I_0 \exp\left(\frac{V_{GS}-V_{th}}{nU_T}\right) \tag{3.19}$$

$$I_{M9} = S_{M9} I_0 \exp\left(\frac{V_{GS}-V_{th}}{nU_T}\right) \tag{3.20}$$

where V_{th} is the threshold voltage, n is the subthreshold slope factor, U_T = kT /q is the thermal voltage, V_{GS} is the gate to source voltage. S_{M8} and S_{M9} are the W/L ratios of the transistors M_8 and M_9, I_0 is $2n\mu_n C_{ox}\left(\frac{kT}{q}\right)^2$ and W and L are the transistor length and width. It can also obtain that

$$I_{M8} = \frac{S_{M6}}{S_{M7}} I_{M9} \tag{3.21}$$

Using (3.19-3.21), the drain to source voltage of transistor M_2 can be given by

$$V_{DS2} = V_{net1} - V_{net2} = nU_T \ln(K_1) \tag{3.22}$$

where K1 = $(S_{M7}S_{M8})/(S_{M6}S_{M9})$, and S_{M6}, S_{M7}, are the W/L ratios of M_6 and M_7, respectively. In this work, the transistor M_1 operates in the saturated region, the transistors M_2 and M_3 are in the triode region. The current of M_2-M_3 can be described from the following equation

$$I_{M1} = \frac{1}{2}\acute{k} S_{M1}(V_{ref} - V_{net1} - V_{th})^2 \tag{3.23}$$

$$I_{M2} = \acute{k} S_{M2}(V_{ref} - V_{net2} - V_{th} - \frac{V_{DS2}}{2})V_{DS2} \tag{3.24}$$

$$I_{M3} = \acute{k} S_{M3}(V_{ref} - V_{th} - \frac{V_{net2}}{2})V_{net2} \tag{3.25}$$

where $\acute{k}$ is the transconductance parameter of MOS transistors and the W/L ratios of M_1, M_2 and M_3 are and S_{M1}, S_{M2} and S_{M3}, respectively. As a result, V_X can be obtained from the following equation.

$$V_X = V_{ref} - V_{net1} - V_{th} = V_{DS2}(K_2 + \sqrt{1 + (K_2)^2}) \quad (3.26)$$

where $K_2 = \frac{S_{M2}}{S_{M1}}$. Then (3.23) was substituted with (3.26) so that the reference current I_{ref} is described as

$$I_{ref} = \acute{k}(nU_T)^2 K_{eff} \quad (3.27)$$

where $K_{eff} = \frac{1}{2} S_{M1}[\left(K_2 + \sqrt{1 + (K_2)^2}\right)\ln(K_1)]^2$

The I_{ref} is mirrored to the R-2R current splitter, which is built by using unit-sized transistors (M_R, M_{2R}). For N-stages splitter, the current of each stage is reduced to a factor $I_k=I_{ref}/2^k$, where I_k is the current at the k^{th} stage of the current splitter. The output currents of the splitter are mirrored to the filter circuit and can be controlled using a 3-bit digital decoder.

3.2 Post-layout simulation results

The proposed fully-differential 4^{th}-order bandpass filter was designed and simulated by using process parameters from a standard 0.18-µm CMOS technology. The circuit was designed to operate at 1-V single power supply voltage. The layout of the proposed bandpass filter consisting of the 4^{th}-order bandpass filter and the programmable current generator is shown in Figure 3.9. The total occupied area is 305 µm x 290 µm. The capacitors C_{in}, C_1, and C_2, are 0.8 pF, 1 pF, and 3.6 pF, respectively. Thus, the input signal is attenuated by a factor of 5.5. The dimension of MOSFETs of the filter, current generator, and R-2R current splitter are summarized in Table 3.1 and Table 3.2, respectively.

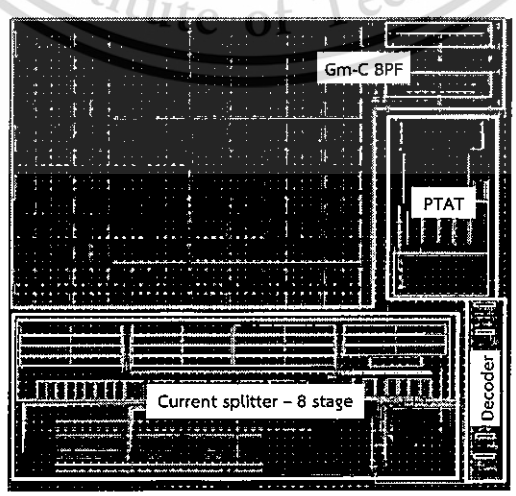

Figure 3.9 Layout of the proposed filter with the size of 305µm x 290µm

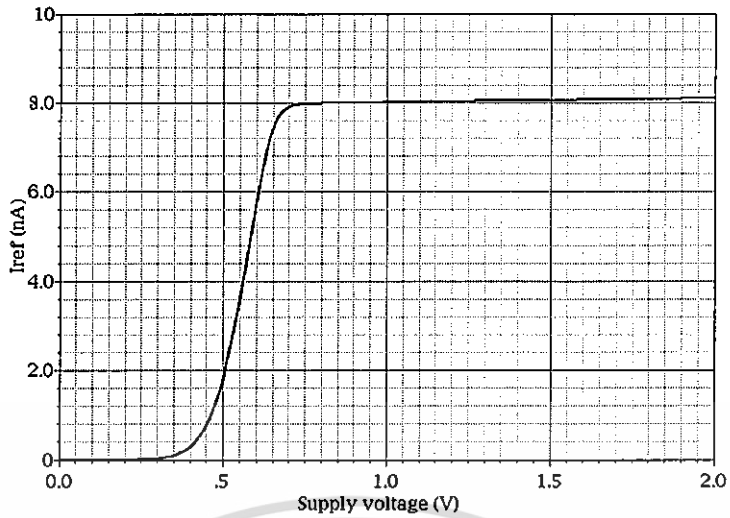

Figure 3.10 Simulated current reference versus supply voltage

Table 3.1 Transistor sizes of the of the proposed bandpass filter

Components	size
M_1	1μm/30 μm
M_2	1 μm /5 μm
M_3	1 μm /30 μm
M_4	1 μm /40 μm
C_1	1pF
C_2	3.6pF
C_{in}	800fF

Table 3.2 Transistor sizes of the current reference, the binary weight current splitting, and the decoder

Components	size	Components	size
M_1	1 μm /250 μm	M_{12}	10 μm /0.18 μm
M_2	1 μm /150 μm	M_{13}	0.25 μm /150 μm
M_3	1 μm /50 μm	M_{14}	0.5 μm /0.5 μm
$M_{4,5,6,7,11}$	2 μm /50 μm	M_R	10 μm /5 μm
M_8	26.4 μm /40 μm	M_{2R}	10 μm /10 μm
M_9	4 μm /40 μm	M_P	4 μm /30 μm
M_{10}	10 μm /8 μm	M_N	2 μm /30 μm

In this work, the PTAT current reference is 8 nA. The fixed current reference is scaled down to picoamperes using the 8-stage binary-weight current splitter. The total integrated output noise current of the current generator is 0.15 pA, which is significantly less that the minimum output current of the circuit. The performance of the current reference is summarized in Table 3.3. The simulated current reference as a function of the supply voltage from 0 V to 2 V is illustrated in Figure 3.10. The line sensitivity of the current reference is 1.01%/V.

The decoder configuration of the control switches of a binary weight current splitting and the corresponding center frequencies, which are programmable from 80 Hz to 6.18 kHz, are shown in Table 3.4.

At a nominal center frequency of 945 Hz and the Q-value of 3, I_1 and I_2 are equal to 0.5 nA and 1nA (i.e. N=2) respectively. The core filter circuit consumes only 4 nW. The voltage buffer and the programmable current generator consume 2 nW and 45.7 nW, respectively. Figure 3.11 shows the simulated AC magnitude responses of the first and the second filter stages of the 4^{th}-order bandpass filter with the center frequency of 945 Hz and the Q-value of 3. The center frequencies of the filter are programmed by adjusting both I_1 and I_2, which are set by the 3-bit DAC. Figure 3.12 shows the center frequency tuning characteristic of the filter. The center frequency is tuned from 80 Hz to 6.18 kHz when I_1 is changed from 38.5 pA to 4 nA. The passband gain of the filter is changed from -2.7dB to 0 dB.

The Q-value remains virtually constant at 3 since N is kept constant at 2. Note that the bias current of the voltage buffer is also generated from the programmable bias current generator so that it can be adjusted along with I_1 to achieve the optimum bandwidth and power consumption. The total current consumption of the core filter circuits (including the buffer) varies from 462 pW to 48 nW when the center frequency is tuned. Note that one-third of the total power consumption belongs to the buffer.

To demonstrate the Q-tuning of the filter, from (3.4) the Q-tuning can be adjusted by changing I_1 and I_2. Figure 3.13 shows the Q-tuning, which the Q-value was tuned from 2 to 50 by varying N from 1.5 to 6. The center frequency was set to fix at a nominal center frequency of 945 Hz. The current source I_1 and I_2 were used to bias the filter independently to keep the center frequency of the filter unchanged.

Table 3.3 Summary of the simulated performance of the current reference

I_{REF}	8nA
Supply voltage	1 V
Area	60 μm x 110 μm
Sensitivity to Process and Mismatch 100runs (%)	2.58
Line sensitivity (%/V)	1.01
Sensitivity to temperature (%/C)	0.23
Sensitivity to process corner (%)	1.25

Table 3.4 The decoder configuration of the control switches of a binary weight current splitting and the corresponding center frequencies

Code	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	f_c
000	1	0	0	0	0	0	0	0	6.18 kHz
001	0	1	0	0	0	0	0	0	3.2 kHz
010	0	0	1	0	0	0	0	0	1.75 kHz
011	0	0	0	1	0	0	0	0	945 Hz
100	0	0	0	0	1	0	0	0	510 Hz
101	0	0	0	0	0	1	0	0	273 Hz
110	0	0	0	0	0	0	1	0	147 Hz
111	0	0	0	0	0	0	0	1	80 Hz

Transient simulations were performed to investigate the linearity of the filter with 945-Hz center frequency and the Q-value of 3. Figure 3.14 plots the simulated output %THD against the input amplitude when applying a 945 Hz sinusoidal input signal. It can be seen that the output THD reaches 1% when the input amplitude is 132 mV. Two-tone intermodulation tests were also performed by applying a two-tone input signal of 950 Hz and 1 kHz. Figure 3.15 plots the simulated third-order intermodulation.

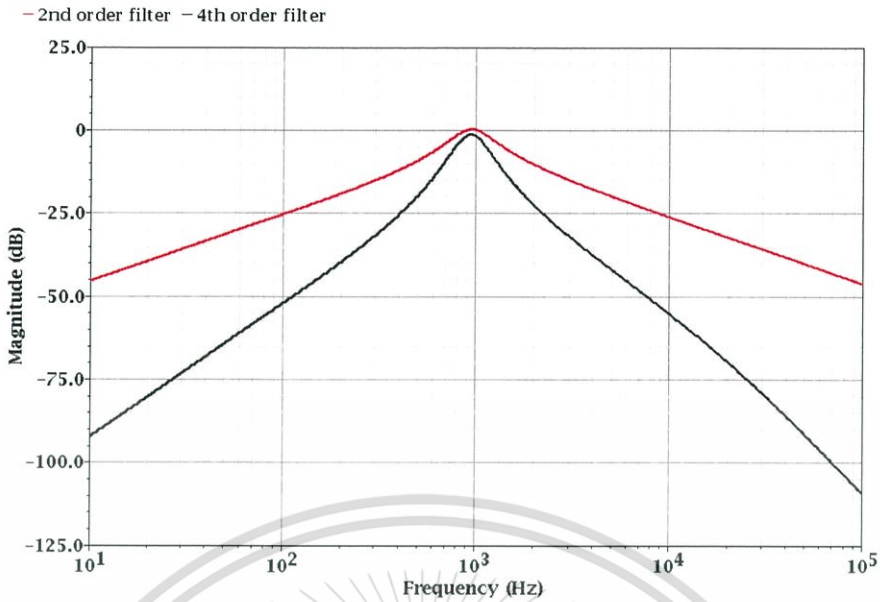

Figure 3.11 Simulated frequency responses of the 2nd-order filter and the 4th-order filter with f_c = 945 Hz

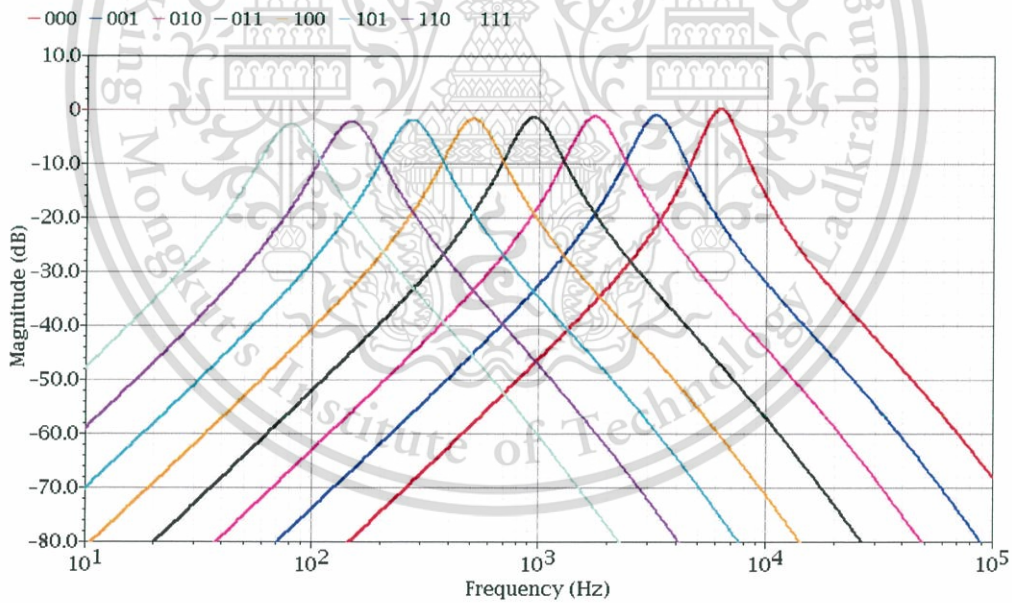

Figure 3.12 Simulated frequency response of the 4th-order filter with center frequency tuning from 80 Hz to 6.18 kHz

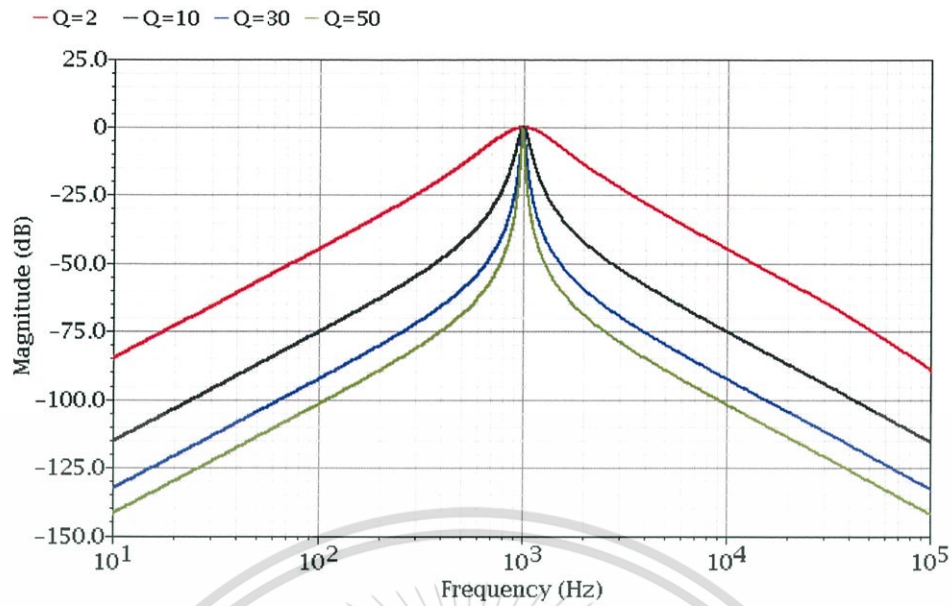

Figure 3.13 Simulated frequency response of the 4th-order filter with Q tuning range from 2 to 50

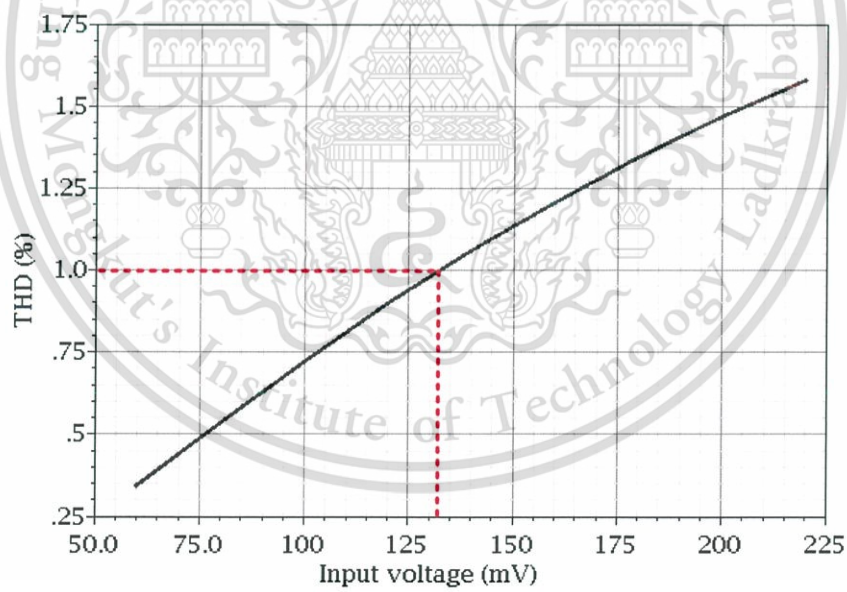

Figure 3.14 Simulated harmonic distortion of the 4th-order filter with f_c = 945 Hz

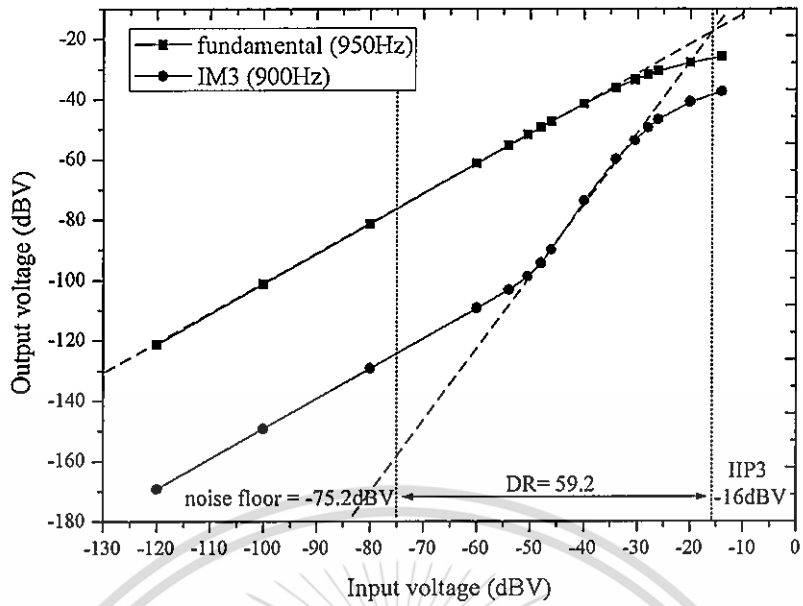

Figure 3.15 The third-order intermodulation of the 4th -order filter with f_c = 945 Hz

The output IIP3 is estimated to be -16 dBV. The simulated input-referred noise voltage, integrated from 805 Hz to 1.1 kHz, is about 174.2 μV. Therefore, the calculated input signal dynamic range is about 57.6 dB and 59.2 dB for the maximum tolerable 1% THD and IM3. Table 3.5 summarizes the simulated performance of the 4th -order bandpass filter with the center frequency tuned from 80 Hz to 6.18 kHz. The simulated performance of the proposed bandpass filter is summarized and compared with other prior designs as shown in Table 3.6.

In practice, the MOSFET's transconductance and the capacitance change with device mismatches and process variations. Hence, MOSFETs with long channel lengths and the common-centroid and symmetrical layout are used to minimize these effects. The effects of various non-idealities under different parameters are verified as follows, (1) process variation and mismatches, (2) supply voltage variation, (3) temperature variation and (4) process corner. Monte Carlo simulation was performed to evaluate the effects of device mismatches and process variation on the performance of the filter. Figure 3.16 shows a simulated histogram of the filter at the center frequency of 945 Hz, which is obtained with 100 samples and a sigma of 3. Note that assuming the Gaussian statistical process variation, sigma of 3 means that 99.73% of variations fall within +/-3 standard deviations (SD) of the mean value. The histogram shows the mean value of 940.6 Hz with a standard deviation of 4.48

Hz, which is equal to 0.45% of errors. Figure 3.17 shows a simulated histogram of total harmonic distortion of 4th-order filter with 100 samples and a sigma of 3. The result shows that the error of 1% THD is 16.3%

Figure 3.18 plots the simulated center frequency of 945 Hz and the Q-value of 3 under 5 cases of process variations as (typical-typical (tt), slow-slow (ss), fast-fast (ff), slow-NMOS-fast-PMOS (snfp) and fast-NMOS-slow-PMOS (fnsp). The worst-case variation with process corner is 1.23%. The results show that the center frequency of the filter is robust under process variations. The worst-case variation with temperature ranging from 0°C – 80°C is 13.23%.

Table 3.7 summarizes the variation of the center frequency of the 4th-order filter under process, supply voltage, and temperature variations. It can be deduced that the performance of the filter is quite robust under process and supply voltage variations at all process corners. However, the center frequency of the filter varies substantially with temperature due to the variation of the reference current from the bias current generator. This can be improved by using a temperature compensated current reference.

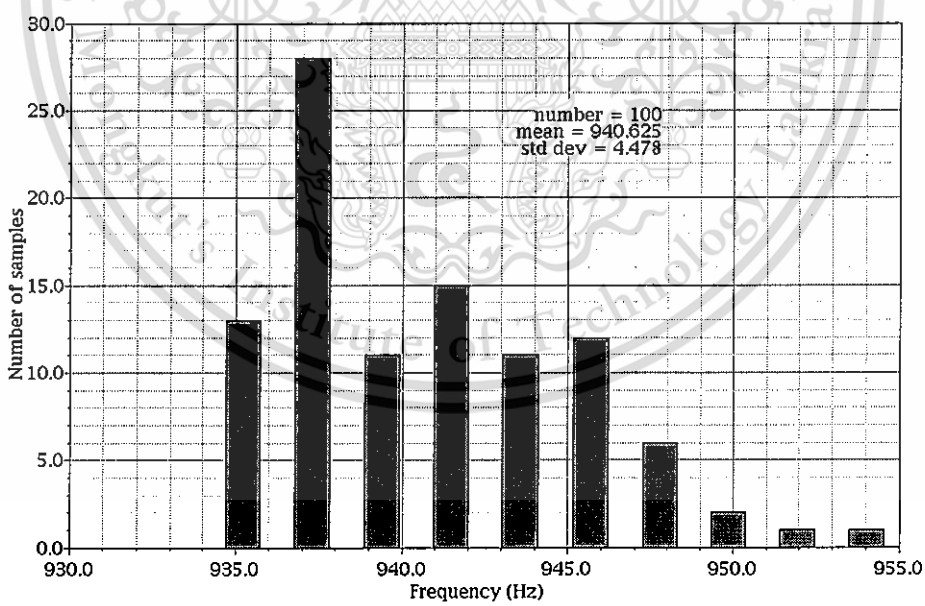

Figure 3.16 Histogram of the center frequency of 4th -order filter using Monte Carlo simulation with 100 samples and sigma of 3

Table 3.5 Summary of the simulated performance of the proposed bandpass filter at various center frequencies

Technology	0.18μm							
Area	305μm x 290μm =0.088mm^2							
Supply voltage	1 V							
f_c (Hz)	80	147	273	510	945	1.75k	3.2k	6.18k
Power consumption of 4th-order filter and buffer (nW)	0.462	0.875	1.66	3.2	6	12	23.4	48
Input amplitude (mV) (@THD=1%)	119.2	121.4	127	128	132	140	141.5	155
Input amplitude (mV) (@IM3=-40dB)	158.5	177.8	177.8	146.2	158.5	153.1	149.6	147.9
Input-referred noise (μV)	154.6	154.3	157.6	164.5	174.2	188.7	207.9	213.5
DR (dB) (@THD=1%)	57.7	57.9	58.1	57.8	57.6	57.4	56.7	57.2
DR (dB) (@IM3=-40dB)	60.2	60.3	61	59.0	59.2	58.2	57.1	56.8
FoM (x10^{-13})	0.25	0.26	0.26	0.27	0.28	0.3	0.32	0.34

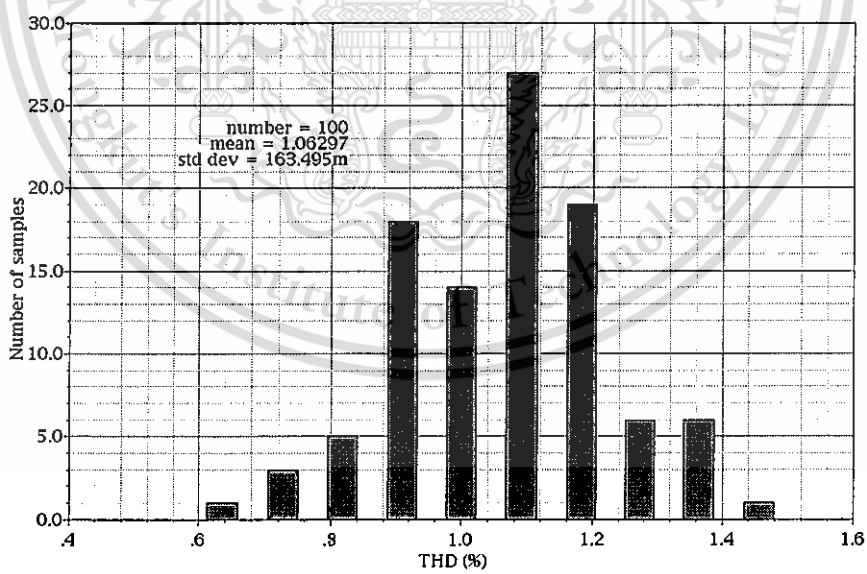

Figure 3.17 Histogram of total harmonic distortion of 4th-order filter using Monte Carlo simulation with 100 samples and sigma of 3

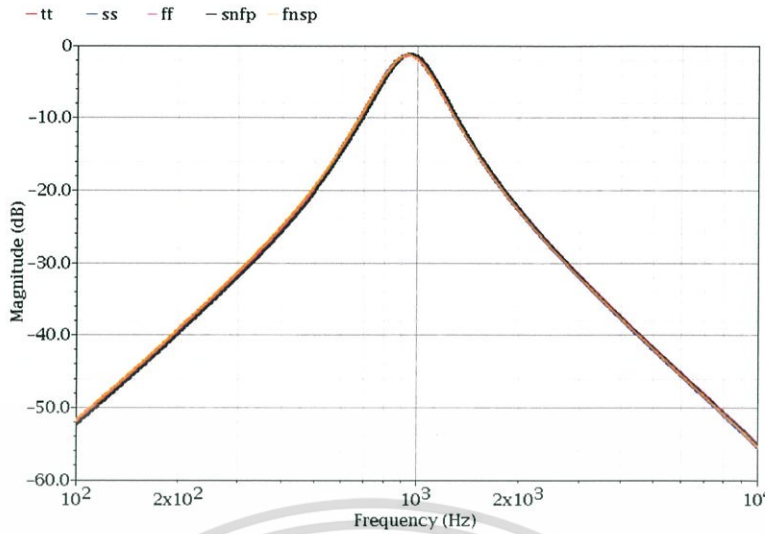

Figure 3.18 Effect of process variation of the center frequency of 4th-order filter at f_c = 945 Hz.

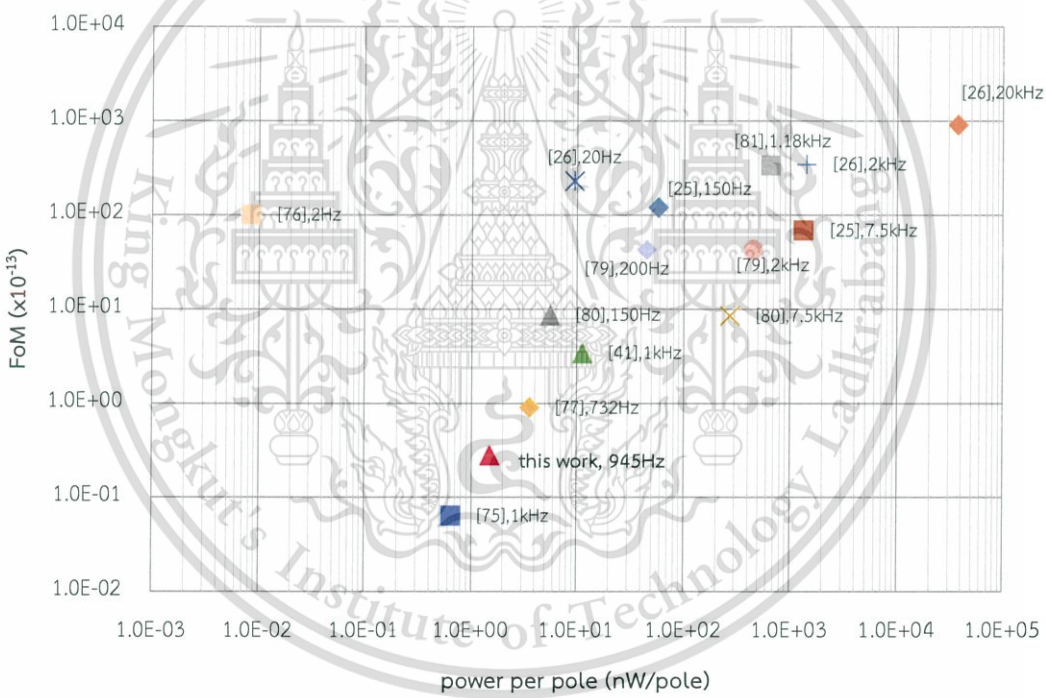

Figure 3.19 Comparison between FoM and power per pole with other prior designs

Different filter designs are usually compared by FoM defined in (2.16) which is typically a ratio of power consumption needed to achieve the required number of poles, bandwidth and dynamic range. At a center frequency of 945 Hz, the proposed filter achieves the second best FoM comparisons in Figure 3.19. However, the best FoM approached in [75] attain very low Q (<0.5) which may not be sufficient for some applications such as cochlear implant and hearing aids.

Table 3.6 Performance summary and comparison of low-power bandpass filters

Parameter	[25]*m	[81]*m	[77]*m	[75]*m	[52]*m	This work*s
Filter order	4	2	4	4	6	4
CMOS process (μm)	1.5	0.5	0.18	0.18	0.35	0.18
Architecture	G_m-C	G_m-C with compression	RC, using MOSFET as R	G_m-C, using MOSFET as G_m	G_m-C	G_m-C, using MOSFET as G_m
f_c (kHz)	0.1-10	0.075-12	0.732	0.125-16	0.1-25	0.08-6.18
Q	1.4	2 - 10	1.5	0.48	2	2 - 50
Power dissipation (core filter)	230nW (f_c=141Hz)	1.32uW (f_c=1.18kHz, Q=2)	14.4nW (f_c=732Hz)	2nW (f_c=1kHz)	68nW (f_c=670Hz)	6nW (f_c=945Hz, Q=3)
Supply voltage (V)	2.8	3.3	1	0.5	1	1
input noise (μV)	776	2200	50	78	50	174.2
THD (%)	5	4.3	1	1	1	1
DR (dB)	67.5	55	55	47	49	57.6
FoM ($x10^{-13}$)	169	336	0.89	0.053	3.4	0.28
Area (mm^2)	n/a	0.07	0.132	0.014	0.234	0.088

*m = measurement, *s= simulation

Table 3.7 Summary of the simulated center frequencies with variations of process parameters, mismatch, supply voltage, temperature, and process corner

code	Center frequency (Hz)			
	Process and Mismatch (100run)	Supply voltage (10% variation)	Temperature 0°C – 80°C	Process corner
000	6.18k ± 0.032%	6.18k ± 4.82%	6.18k ± 15.23%	6.18k ± 1.7%
001	3.2k ± 0.023%	3.2k ± 1.97%	3.2k ± 13.38%	3.2k ± 1.19%
010	1.75k ± 0.26%	1.75k ± 1.71%	1.75k ± 12.80%	1.75k ± 1.43%
011	941 ± 0.48%	945 ± 1.16%	945 ± 13.23%	945 ± 1.23%
100	510 ± 0.2%	510 ± 0.98%	510 ± 12.75%	510 ± 1.39%
101	272 ± 0.49%	273 ± 0.55%	273 ± 12.82%	273 ± 2.01%
110	146.5 ± 0.6%	147 ± 0.54%	147 ± 12.24%	147 ± 3.20%
111	80 ± 0.62%	80 ± 0.75%	80 ± 47.5%	80 ± 5.44%

Chapter 4

A 6-bit, two-step successive approximation logarithmic ADC

ADC is one of the key building blocks interfacing between analog signals and digital processing. For biomedical applications, the conversion of low-frequency biopotential signals does not require high speed but low power dissipation. Logarithmic ADC is used where wide dynamic range is required such as cochlear implants, hearing aids, neural recording and stimulation. It can directly convert and compress input signals with logarithmic encoding. The logarithmic ADC offers attractive solutions for reduced hardware complexity, low-power consumption, the ability to handle large input signal dynamic range, reduction of noise and data bit-rate, and compensation of nonlinear sensor characteristics.

This chapter presents the architecture and the circuit level implementation of the proposed logarithmic ADC. The design specifications and considerations are introduced in section 4.1. The proposed logarithmic SAR ADC along with the operation is discussed in section 4.2. Section 4.3 describes the detailed circuit implementation of ADC building blocks including the logarithmic and linear DAC, comparator, buffer, and SAR control logic. The post-layout simulation and measurement results are described in section 4.4 and section 4.5, respectively. Section 4.6 provides the conclusion of the chapter.

4.1 Design specifications and considerations

The proposed logarithmic ADC is targeted for a replacement of linear ADC in some applications such as cochlear implants, neural recording and DBS which require wide dynamic range. The logarithmic ADC resolution is set by the current stimulator resolution in the electrode for a cochlear implant or DBS. In this work, 6 bits, 25 kHz sampling frequency are selected. For achieved the design specifications, this work employs the following methods:

1) As the desired information of neural and audio signals are more concentrated on the smaller amplitudes of the signal, a logarithmic ADC characteristic is chosen.

2) The SAR ADC architecture is selected to realize the logarithmic characteristic since it provides high energy efficiency, and a simple structure, requiring only a comparator, a bank of capacitors with switches, and a small amount of digital control logic.

3) A straightforward method to realize a logarithmic SAR ADC is to employ the conventional linear SAR ADC structure and substitute the linear charge redistribution DAC with a logarithmic counterpart. However, it is very difficult to achieve practically due to noise, linearity and matching constraints. A two-step charge redistribution DAC is proposed which is equivalent to a piecewise linear approximation of the logarithmic function.

4.2 The system architecture of the SAR logarithmic ADC

Figure 4.1 shows the system architecture of 6-bit, two-step SAR logarithmic ADC consisting of S/H, logarithmic and linear DAC, comparator, buffer and SAR control logic. An N-bit logarithmic ADC converts V_{in} to N-bit digital output code (D_{out}) described previously by (2.19). The ADC's logarithmic mapping relationship can be adjusted by the values of C and b. In this work, b=2 and C=8 are chosen to design the logarithmic ADC with because the threshold voltage values (see Table 2.3) are in the form of powers of 2, which allows an easy and practical realization of the logarithmic charge redistribution DAC. However, using (2.19), the 6-bit logarithmic ADC with b=2 and C=8 will have LSB_{min} = 0.354 mV (i.e. equivalent to LSB of an 11.5-bit linear ADC) which is very difficult to achieve practically due to noise, linearity and matching constraints.

To alleviate this practical difficulty, a two-step charge redistribution DAC is proposed. The first conversion step performs a 3-bit logarithmic coarse conversion and the second step performs a 3-bit linear fine conversion. This is equivalent to a piecewise linear approximation of the logarithmic function, as depicted in Figure 4.2. The first conversion step employs two 3-bit logarithmic DACs and determine the segment of the piecewise linear approximation (i.e. $([S1-S2], [S2-S3], \ldots)$. The digital output code for logarithmic quantized can be derived as (2.19). The second step employs a fine conversion which the input signal is the linear quantized in segment.

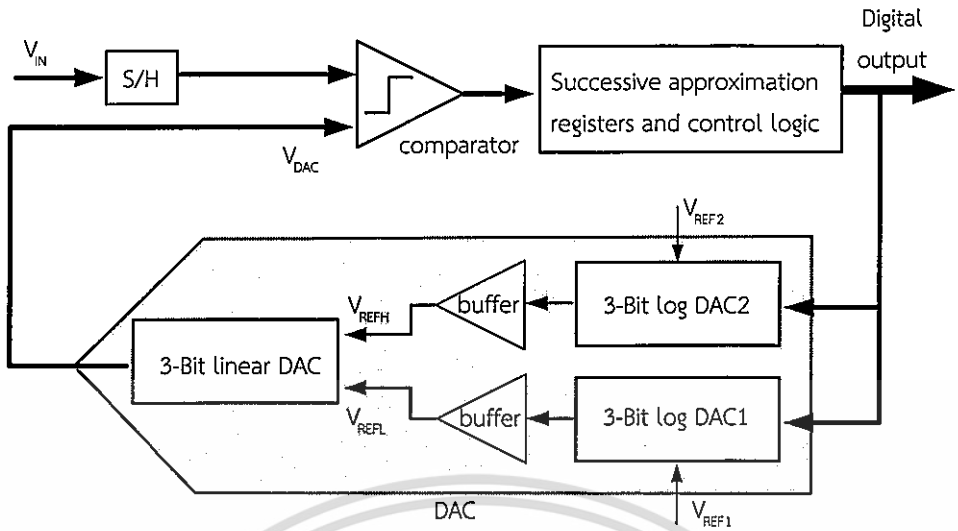

Figure 4.1 Simplified block of the proposed SAR logADC

The operation of the SAR logarithmic ADC is identical to its linear counterpart. It requires N clock cycles and N comparisons to complete a conversion. The conversion is successively from the most significant bit (MSB) to the least significant bit (LSB). The algorithm starts by 3-bit logarithmic DAC of segment selection. The comparator compares the input voltage with the threshold voltage levels from the logarithmic DAC. Depending on the comparison outcome, the output comparator is then processed by the digital control logic, which generates a control signal to the logarithmic DAC. Assuming that the comparator output voltage V_{comp} is high, the voltage levels from the logarithmic DAC is set $V_{DAC(i+1)}=V_{DAC(i)}x2^{i}$, i=1,2,...N. If V_{comp} is low, the voltage levels from the logarithmic DAC is set $V_{DAC(i+1)}=V_{DAC(i)}/2^{i}$. The sequence successively repeated until all 3-bit logarithmic coarse conversions are decided. The flow graph for the SAR logarithmic approach is shown in Figure 4.3. Figure 4.4 represents all possible conversions of 3-bit logarithmic switching procedures.

For the second step, a linear ADC is used to digitize the input signals for the remaining 3 bits. The analog output voltages of the logarithmic DACs will be utilized as the high and low reference voltages (V_{REFH} and V_{REFL}) for the linear DAC. This can be obtained by setting $V_{REF2}=2V_{REF1}$, where V_{REF1} and V_{REF2} are the reference voltages of the $logDAC_1$ and $logDAC_2$, respectively. Thus, given the same digital input code, the analog output voltage of $logDAC_2$ is twice that of $logDAC_1$ (i.e. $V_{REFH} = 2V_{REFL}$)

corresponding to the boundary of each segment. For example, the output codes from the first conversion, $D_5D_4D_3$ are 100 which are in the S5-S6 segment of Figure 4.2. The conversion is then successively comparing the input voltage with the threshold voltage levels from the linear DAC which equal to mid-scale-level of the S5-S6 segment. The process repeats until all 3-bit linear fine conversion is decided.

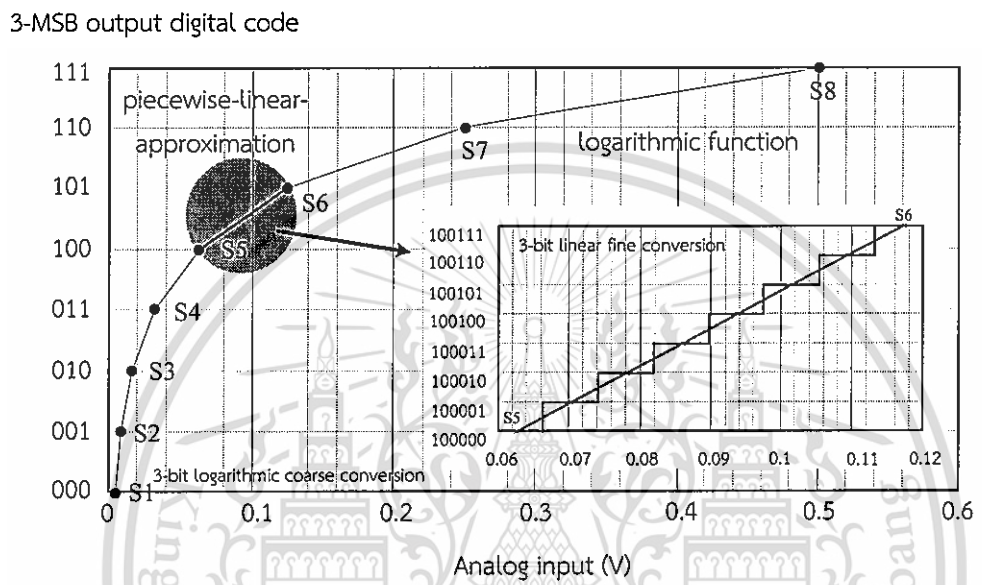

Figure 4.2 Piecewise linear approximation of the proposed 6-bit SAR logarithmic ADC

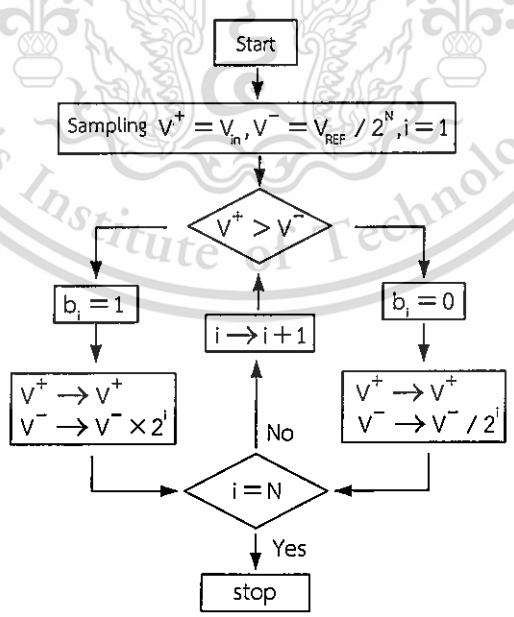

Figure 4.3 The flow graph for the SAR logarithmic approach

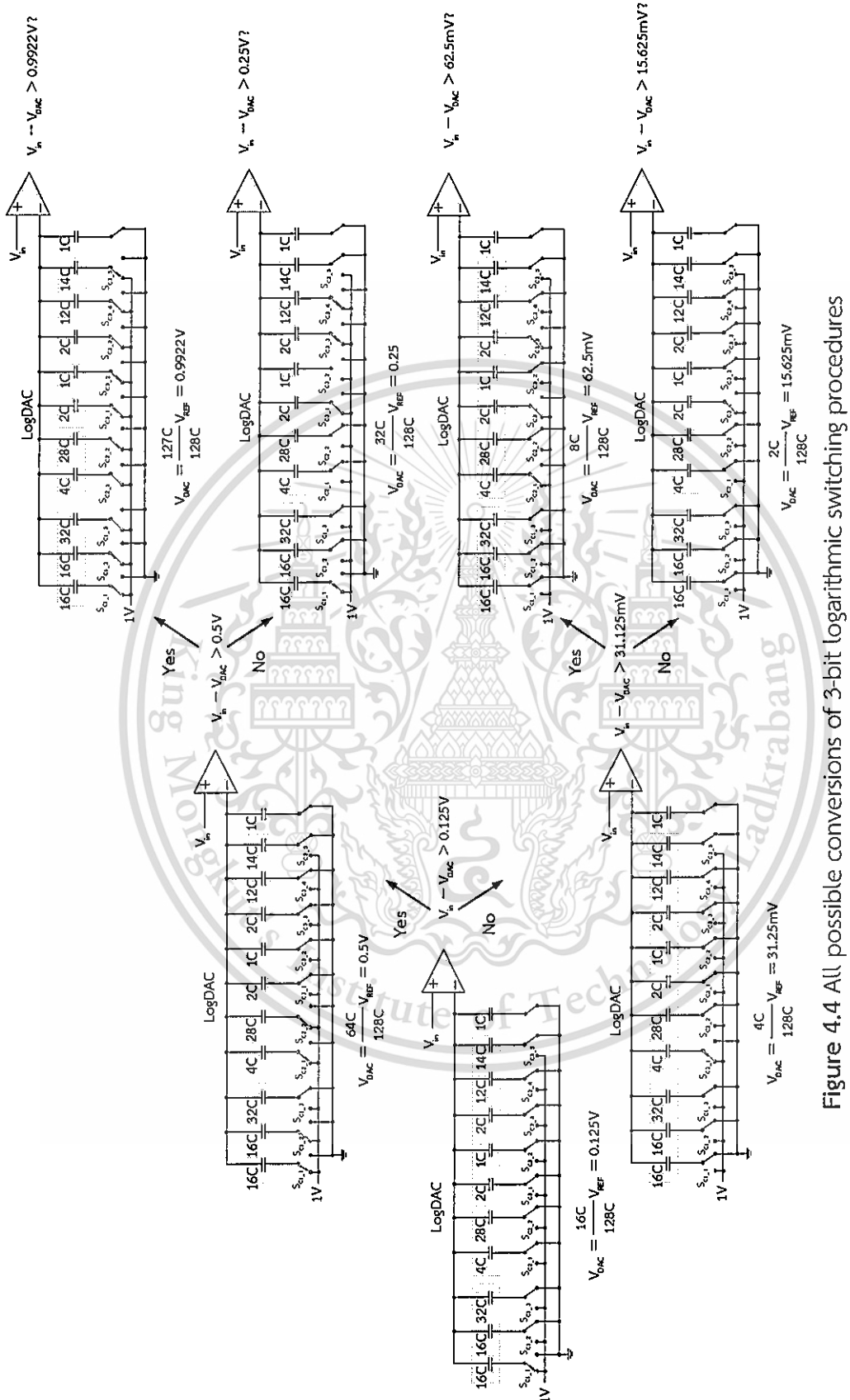

Figure 4.4 All possible conversions of 3-bit logarithmic switching procedures

4.3 Circuit Implementation of the ADC

In this section, the detailed implementation of the circuit building blocks of the logarithmic ADC including capacitive DAC, comparator, buffer, and the SAR control logic is described as follow.

4.3.1 Capacitive DAC

The capacitive DAC determines the accuracy of SAR ADC as it generates voltage levels to compare with the comparator in bit-conversion phases. The precisely ratio capacitors are important as the number of bits increase, the ratio of the MSB capacitor to the LSB capacitor becomes more difficult to control which turns to significant mismatch issues. Therefore, each capacitor in the array is constructed out of a unit capacitance. The unit-size capacitance should be kept as small as possible to reduce the charging or discharging energy during capacitor switching. However, a small capacitance exhibits larger thermal noise (kT/C) and is more sensitive to process variation.

The logarithmic DACs and linear DAC, which the control switch (S_{ci}) signal are generated by the SAR control logic, are realized as depicted in Figure 4.5. Note that the choice of b=2 and C=8 allows an easy and practical implementation of the logarithmic DACs' capacitor arrays since all capacitance values are in the form of an integer multiple of a unit-size capacitance (C_{unit}). The total capacitance for each logarithmic DAC is $128C_{unit}$ thus LSB_{min} is equal to $(1/128)V_{REF1}$. Considering the kT/C and matching accuracy, C_{unit} of the logarithmic DACs and linear DAC are set to 50 fF and 800 fF, respectively. Thus, the total capacitance used in the logarithmic DACs and linear DAC are 12.8 pF and 6.4 pF, respectively. Figure 4.6 shows the layout floorplan of the capacitor arrays. These employ symmetrical common-centroid with surrounding the dummy grounded capacitors, to improve the matching from parasitics, cutting edge effects and process variation. To minimize the effects of charge injection, the bottom-plate sampling is employed, and CMOS transmission gates realize all switches.

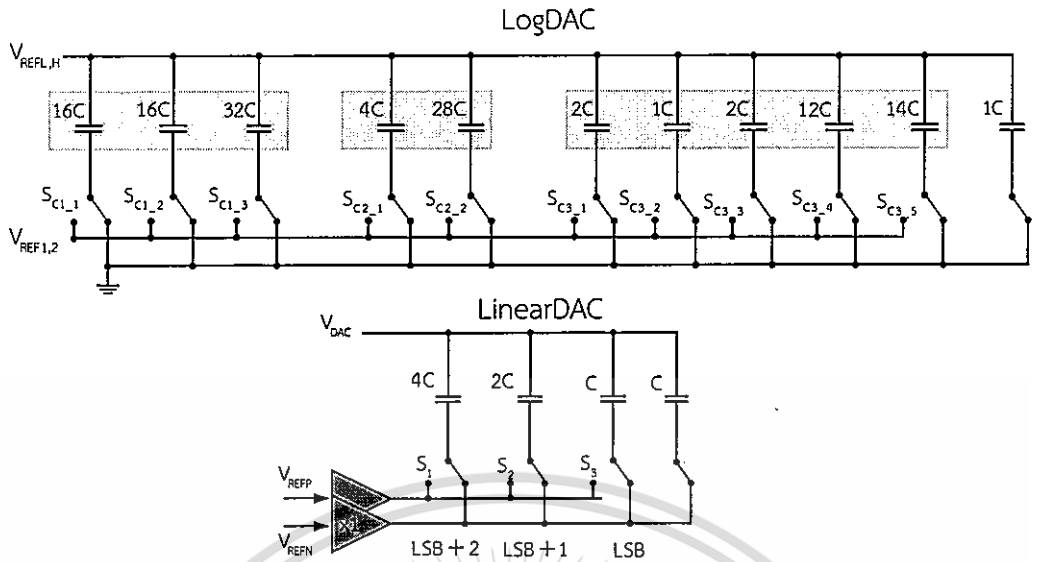

Figure 4.5 The conventional passive charge-redistributed capacitor arrays of logDAC and linearDAC

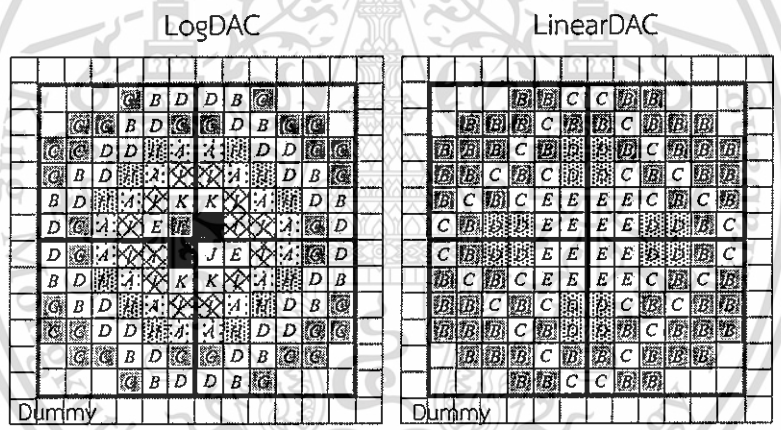

Figure 4.6 Common-centroid and symmetrical layout of logarithmic DAC and linearDAC

4.3.2 Double-tail latch-based comparator

The comparator is one of the most important building blocks in SAR ADC. It generates a logic output high or low based on the differential input voltage. The comparator based on the topology in [90] is shown in Figure 4.7. This topology consists of two stages: input gain stage with current mirror active load and output latch stage. The operation of the comparator is as follow: The PMOS differential pair converts the differential input voltage into a differential output current. Assuming the case $V_{in}^{+} > V_{in}^{-}$, V_{outN} discharges faster than V_{outP} (discharged by the drain current $I_{M6} >$

I_{M3}, where I_{M6}= I_{M2} and I_{M3}= I_{M4} from the current mirror). The corresponding pMOS transistor (M_{10}) will turn on the latch regeneration caused by back-to-back inverters (M_{10}, M_{11} and M_{12}, M_{13}). Thus, V_{outn} pulls to high and V_{outp} discharges to low. If V_{in}^{+} < V_{in}^{-}, the circuits works vice versa.

The cross-coupled NAND gates are used as SR latch to store the output of the comparator then keep it fixed in the reset phase. Inverters are used in between to prevent output glitching while the comparator is latching.

The proposed 6-bit logarithmic ADC has the minimum LSB size of 488.28 μV. Note that it is calculated from the minimum analog output voltages of the logarithmic DAC_1 and DAC_2 divided by 2^3 from the 3-bit linear DAC. The input offset voltages of the comparator should be smaller than 0.5 LSB.

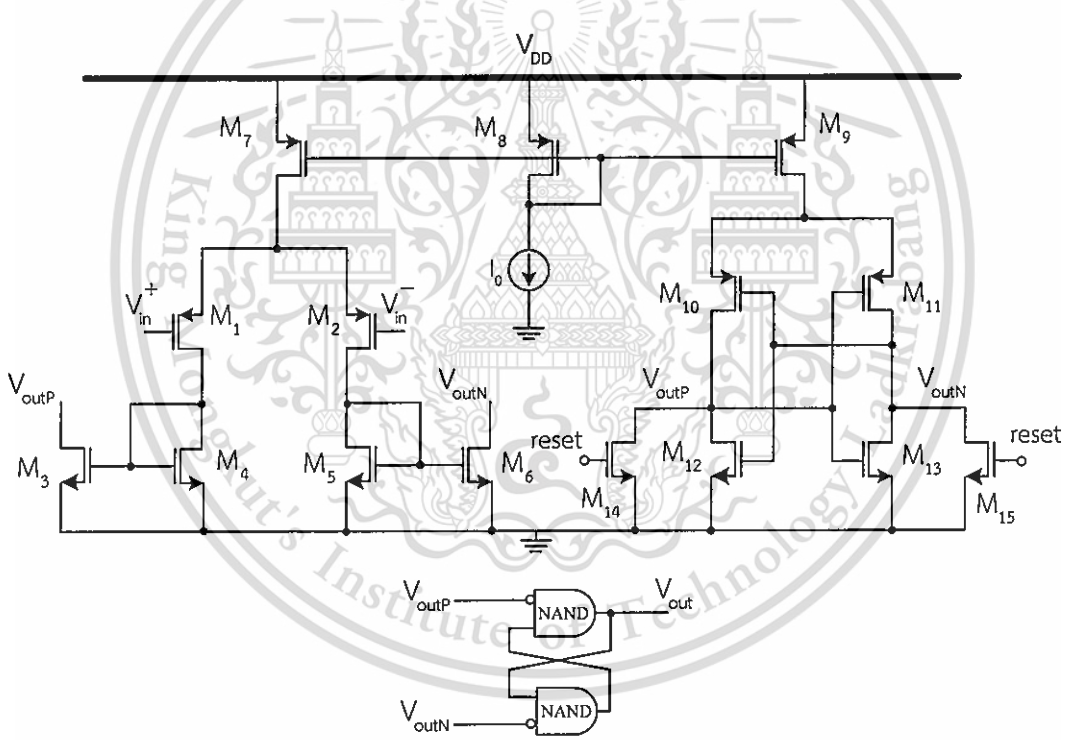

Figure 4.7 Double-tail latch-based comparator

The offset comparator originates from mismatches non-identical devices such as input transistor pair. Therefore, the behaviour of the comparator might arbitrarily change as the comparator may result in the high voltage at its output when the input voltage is less than the reference voltage. Also, it may lead to low voltage when the input voltage is higher than the reference.

The offset comparator is impacted by process variation, which can be formulated as follows:

$$\sigma^2_{comp} \cong \sigma^2(\Delta V_T) + \left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 \quad (4.1)$$

where

$$\sigma^2(\Delta V_T) = \frac{A^2_{VT}}{W \cdot L} \quad (4.2)$$

$$\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 = \frac{A^2_{\beta}}{W \cdot L} \quad (4.3)$$

Therefore, the second term in equation 4.1 is neglected and the input referred offset of a comparator can be approximated by

$$\sigma_{comp} \cong \frac{A_{V_T}}{\sqrt{(WL)}} \quad (4.4)$$

Hence, the areas of the input differential pair should be designed to be large so as to address the common-mode input dependent offset. Transistor sizes of double-tail static latch comparator are summarized in Table 4.1

The simulated input voltage difference and the percentage of probability output=high are shown in Figure 4.8

Table 4.1 Transistor sizes of double-tail static latch comparator

Components	size	Components	size
M_1	40 µm /2 µm	M_9	10 µm /10 µm
M_2	40 µm /2 µm	M_{10}	3 µm /0.5 µm
M_3	60 µm /2 µm	M_{11}	3 µm /0.5 µm
M_4	60 µm /2 µm	M_{12}	4 µm /0.5 µm
M_5	60 µm /2 µm	M_{13}	4 µm /0.5 µm
M_6	60 µm /2 µm	M_{14}	4 µm /1 µm
M_7	10 µm /10 µm	M_{15}	4 µm /1 µm
M_8	10 µm /10 µm		

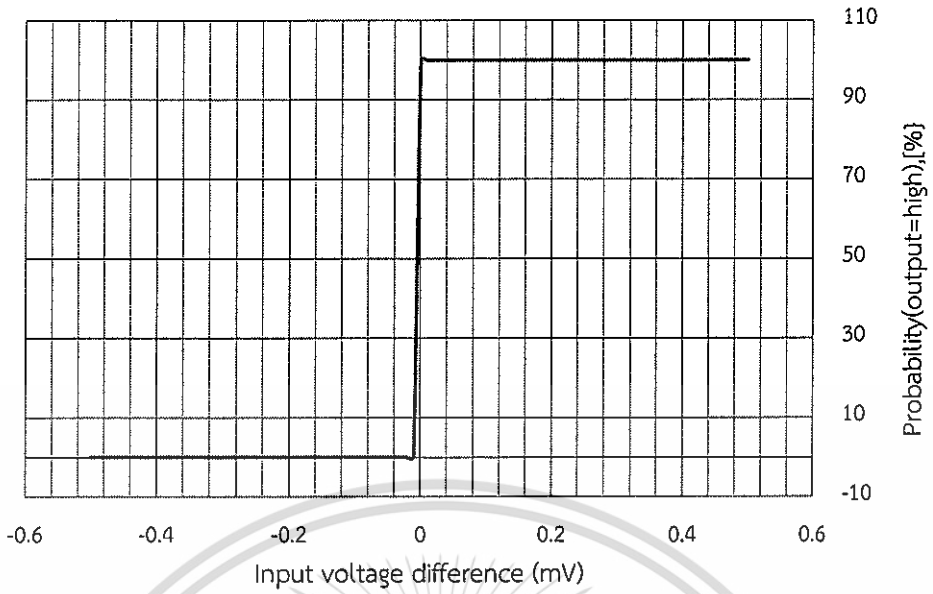

Figure 4.8 The simulated input voltage difference and the percentage of probability output=high

4.3.3 Buffer

The analog output voltages of the logarithmic DACs will be used as the high and low reference voltages for the linear DAC. The remaining 3 bits are realized through the linear DAC. The voltage buffer is required to transfer logarithmic DAC voltage to linear DAC. It prevents the loading effect between the logarithmic DAC and linear DAC. The buffer should be able to handle the voltage levels from $(1/128)V_{REF1,2}$ to $(127/128)V_{REF1,2}$ which is equal to 3.906 mV to 0.992 mV

A two-stage opamp CMOS is an implementation for the unity-gain voltage buffer as shown in Figure 4.9. The first-stage opamp is the folded-cascode with single-ended output while the second-stage is a simple common-drain amplifier. Transistor sizes of the unity-gain voltage buffer are summarized in Table 4.2.

The overall voltage gain can be expressed as

$$A_v \approx \left[g_{m1,2}[g_{m14}r_{o14}(r_{o2}//r_{o4})]//(g_{m11}r_{o11}r_{o10}) \times g_{m15}\left(\frac{1}{g_{m15}}//r_{o16}\right)\right] \quad (4.5)$$

The minimum and maximum output swing voltage of the first-stage opamp is determined by

$$V_{DS(sat)4} + V_{DS(sat)11} \leq v_{out} \leq V_{DD} - V_{SD(sat)10} - V_{SD(sat)10} \quad (4.6)$$

The minimum and maximum output swing voltage of the second-stage opamp is given by

$$V_{DS(sat)16} \leq v_{out} \leq V_{DD} - V_{GS15} \quad (4.7)$$

The unity-gain buffer was simulated under 1.8V single power supply voltage. The bias current was set to 100nA. Figure 4.10 shows the tracking behaviour of the output unity-gain buffer with sweeping input voltages from -0.25V to 1.2V. It can be observed that the output follow the input which is sufficient for the design requirement. Figure 4.11 depicts the simulated transient response to a 20-kHz, 1-V step input under a 6.4 pF load capacitor. The slew rates are found to be 0.53V/μs and 0.55 V/μs for the rising and falling edges, respectively.

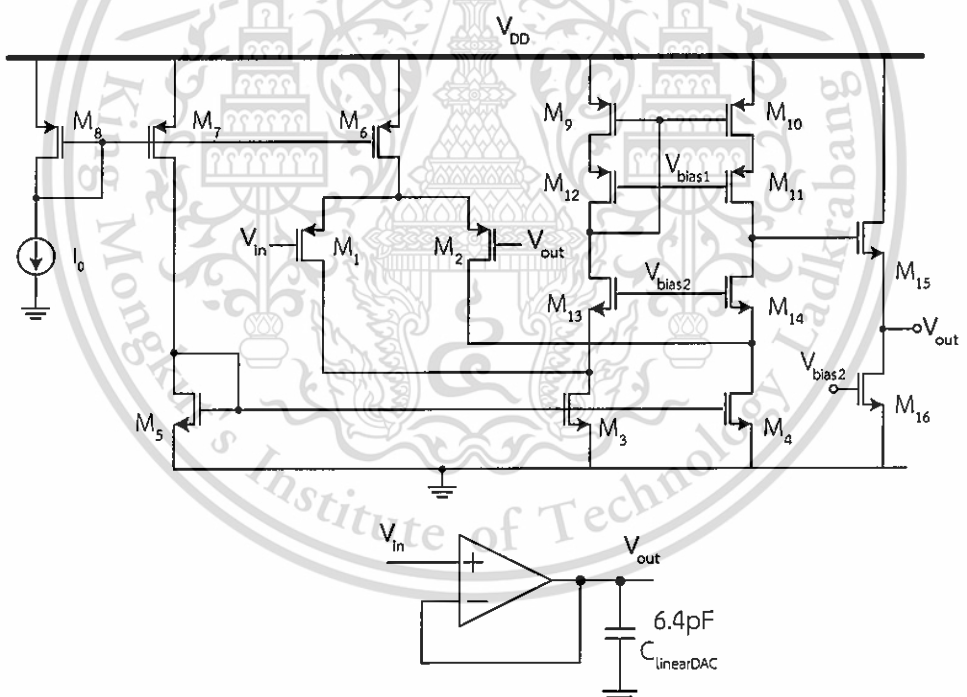

Figure 4.9 The schematic diagram of the two-stage folded-cascode as the voltage buffer

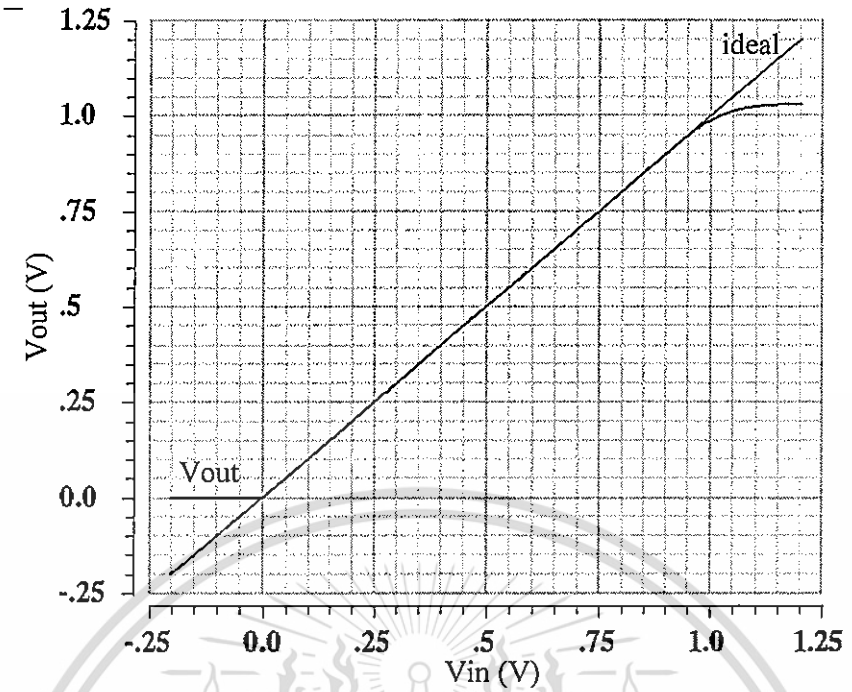

Figure 4.10 DC voltage transfer characteristic

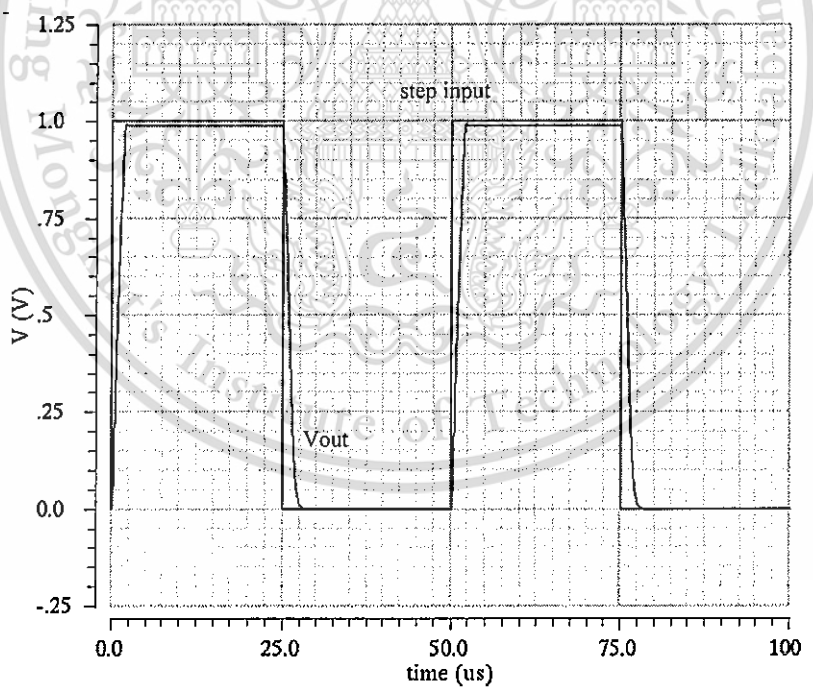

Figure 4.11 Simulated step response of the unity-gain buffer with a capacitive load of 6.4 pF, 20 kHz.

Table 4.2 Transistor sizes of unity-gain voltage buffer

Components	size	Components	size
M_1	20 µm /3 µm	M_9	2 µm /4 µm
M_2	20 µm /3 µm	M_{10}	2 µm /4 µm
M_3	6 µm /4.5 µm	M_{11}	2 µm /4 µm
M_4	6 µm /4.5 µm	M_{12}	2 µm /4 µm
M_5	6 µm /4.5 µm	M_{13}	1.5 µm /5 µm
M_6	6 µm /4 µm	M_{14}	1.5 µm /5 µm
M_7	6 µm /4 µm	M_{15}	40 µm /1 µm
M_8	6 µm /4 µm	M_{16}	1 µm /4 µm

4.3.4 Synchronous SAR control logic

The proposed ADC utilizes synchronous SAR logic. It generates the necessary control commands depending on the value of bits successively based on the result of the comparator.

Figure 4.12 shows the SAR control logic including a shift register called a sequencer (the lower flip-flop row) and a code register (the upper flip-flop row). Figure 4.13 shows the time sequence of the SAR logic. Eight clock cycles are required to complete a single conversion, with six clock cycles for conversion and two cycles for sampling data and storing data. A 200-kHz system clock and the sampling clock of 25 kHz are used. The 1^{st} clock cycle is the reset phase which is needed for avoiding the possible residual charge of the DAC. The input is also sampled in this cycle to track the input signal. The 2^{nd} clock cycle, the comparator performs a comparison between the input signal and the threshold voltage levels from the DAC. Based on the comparator result, the data is stored in the registers. The control signals for the DAC are generated using both the outputs of the sequencer and the data register. The DAC then sets the threshold voltage levels for the next conversion cycle. The same process is successively repeated for MSB to LSB which is in the 2^{nd} to 7^{th} clock cycle to complete the conversion process. The 8^{th} clock cycle latches the output data.

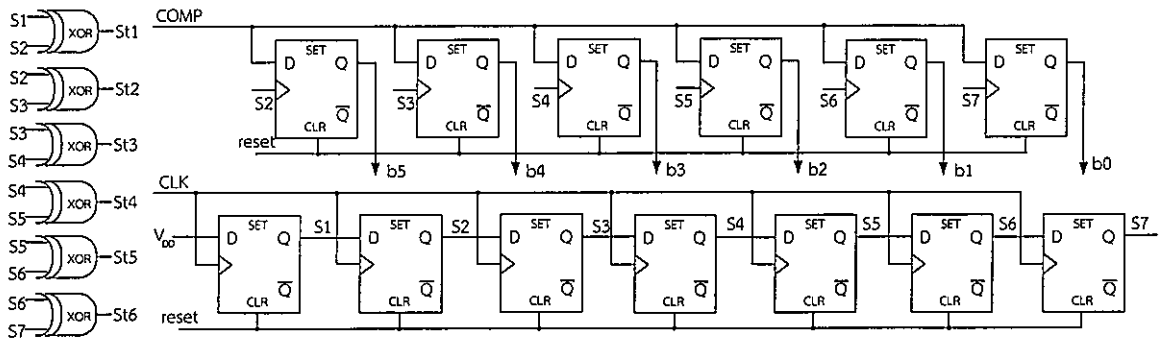

Figure 4.12 The SAR control logic

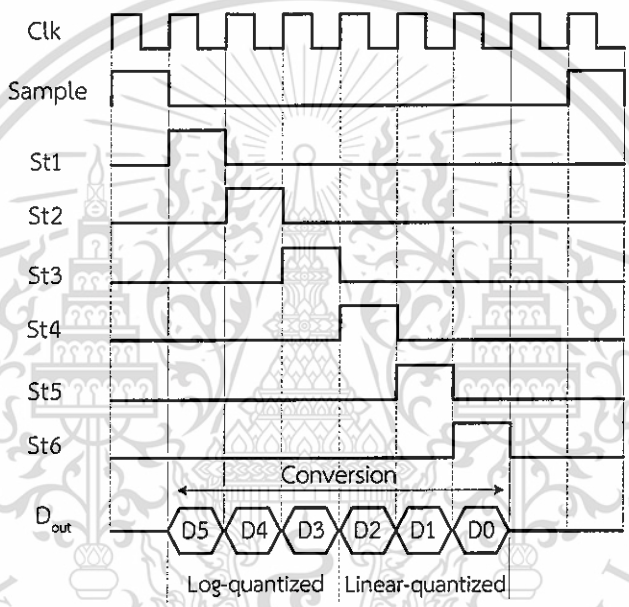

Figure 4.13 The time sequence of the SAR logic

4.4 Post-layout simulation results

The proposed SAR logADC was designed and simulated with process parameters from a standard 0.35 μm CMOS technology under 1.8 V single power supply voltage. The hold capacitance of the sample-and-hold circuit is 7.8 pF. The ADC's full-scale input range is set to 1 V. The reference voltages of logarithmic DAC_1 and logarithmic DAC_2 were set to 0.5 V and 1 V, respectively. The sampling frequency is 25 kHz. All results presented in this section are obtained from post-layout simulations including extracted parasitics. The dynamic power consumption of the ADC is dependent on the input signal amplitudes and varies from 4.36 μW to 14.6 μW.

Figure 4.14 shows the ideal and simulated input-output characteristics of the proposed logarithmic ADC. The input range, from 3.9 mV to 0.9375V produces the digital output code from 0 to 63. Figure 4.15 shows the calculated differential nonlinearity (DNL) and integral nonlinearity (INL), which are in the range of +0.26/-0.32 LSB and +0.19/-0.45 LSB, respectively.

The dynamic performance of the ADC is evaluated by performing transient simulations with time-varying input voltage signals. In a linear ADC, a sinusoidal input signal is used, and the output digital codes are converted to the waveform to calculate the effective number of bit (ENOB) and the signal-to-noise-and-distortion ratio (SNDR).

However, for a logarithmic ADC, an exponential function of a sinusoidal waveform is more suitable because it produces a sinusoidal waveform of the digital output codes [86]. In this work, a simple common-source amplifier with a weak-inversion input PMOS and a resistor load is used to generate the desired exponential input waveform. Figure 4.16 shows the waveforms of the exponential input voltage and the reconstructed output of the ADC when a 100 mV, 100 Hz sinusoidal signal is applied to the common-source amplifier. The ADC input signal has a voltage swing between 3 mV to 850 mV, and the reconstructed ADC output has a voltage swing between 0.2 V to 0.7 V. A 4096-point Fast Fourier Transform (FFT) was used to calculate the spectral component of the reconstructed ADC output. The signal-to-noise-distortion ratio (SNDR) is 31.7 dB, which is equivalent to an effective number of bits (ENOB) of 4.97. The proposed ADC achieves the maximum resolution of 11-bit when the input amplitude is below 7.81 mV and achieves the minimum resolution of 4-bit when the input amplitude is more than 0.5 V. Therefore, the dynamic range is 66 dB. Note that the dynamic range is 30 dB higher than that of a 6-bit linear ADC.

The FoM as defined previously in (2.17) used to compare the performance of the proposed ADC with other reported ADCs. The proposed ADC achieves the FoM of 18.6 pJ/conversion-step with the average power of 9.23 μW. The performances of the proposed ADC are summarized and compared with other prior designs as shown in Table 4.3.

Table 4.3 Performance summary and comparisons

Parameter type	This work	[84]*m	[91]*s	[86]*s	[83]*m
Type	Logarithmic	Logarithmic	Logarithmic	Logarithmic	Exponential
Topology	SAR	Dual-slope	Pipeline	Cyclic	SAR
Supply	1.8	3	1.62	1	1.8
Power	4.36-14.6 μW	3 μW	2.54 mW	0.33 μW	40 μW
Sampling rate	25 kS/s	300 S/s	22 MS/s	1 kS/s	25 kS/s
Number of bits	6	8	8	6	8
ENOB (bit)	4.97	7.85	5.62	5.95	N/A
Full-scale range	1 V	350 nA	1 V	100 nA	1 V
Max. INL	+0.19/-0.45	0.5	0.77	0.88	+4.3/-2.1
Max. DNL	+0.26/-0.32	1	0.32	0.8	+0.8/-0.9
SNDR (dB)	31.7	49	35.6	37.6	N/A
DR	66	60.1	80	40	64.1
FoM (pJ/conv-step)	18.6	41.7	2.38	5.33	N/A
Area (mm^2)	0.164	4.84**	0.56	N/A	0.036
Process (μm)	0.35	1.5	0.18	0.18	0.18

*m = measurement, *s= simulation

**with PAD and testing circuit area

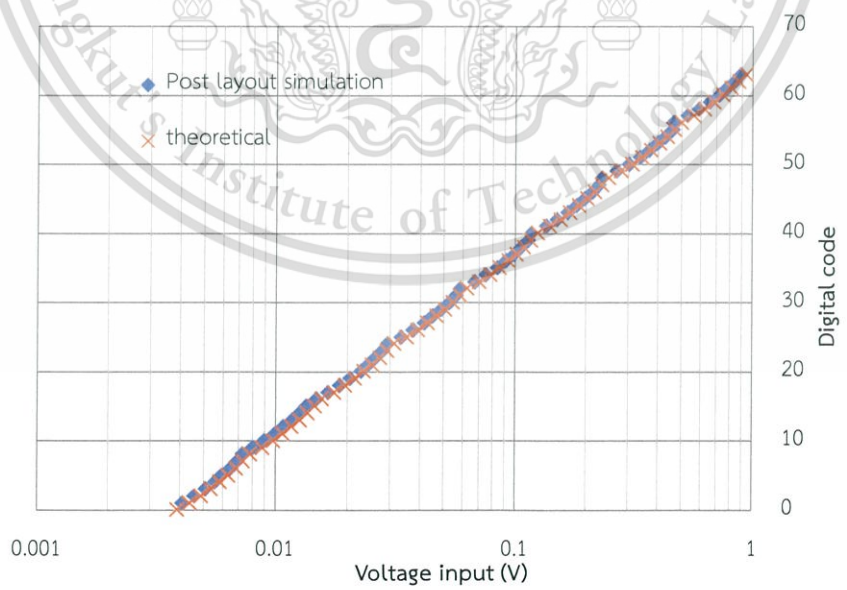

Figure 4.14 Input-output characteristic of the proposed 6-bit logADC

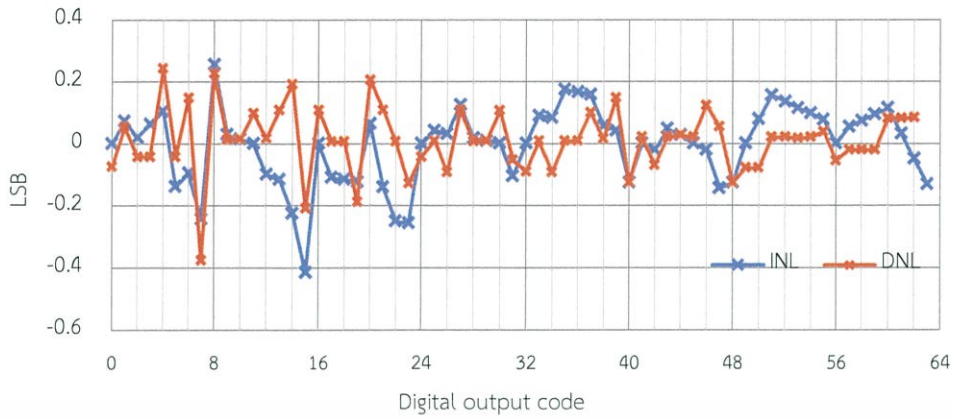

Figure 4.15 Simulated INL and DNL

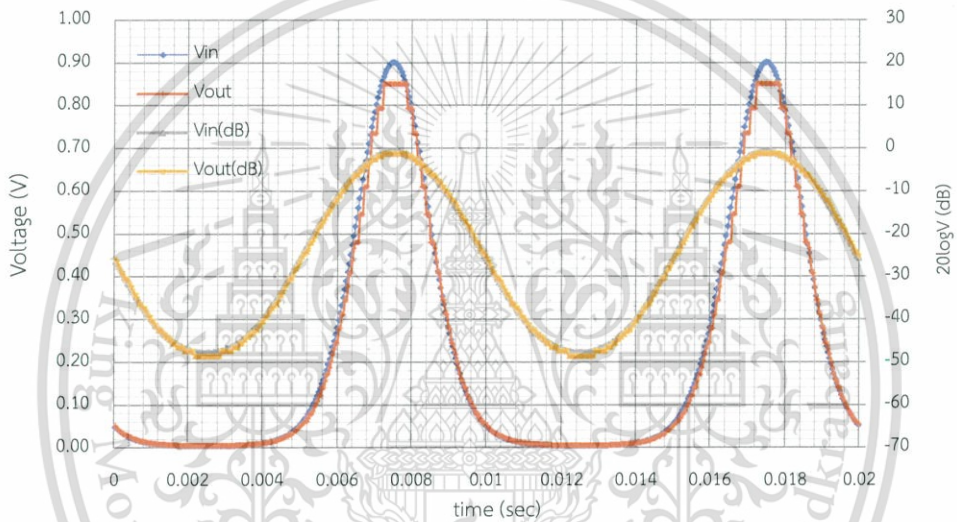

Figure 4.16 Waveforms of the ADC input and the reconstructed output voltages

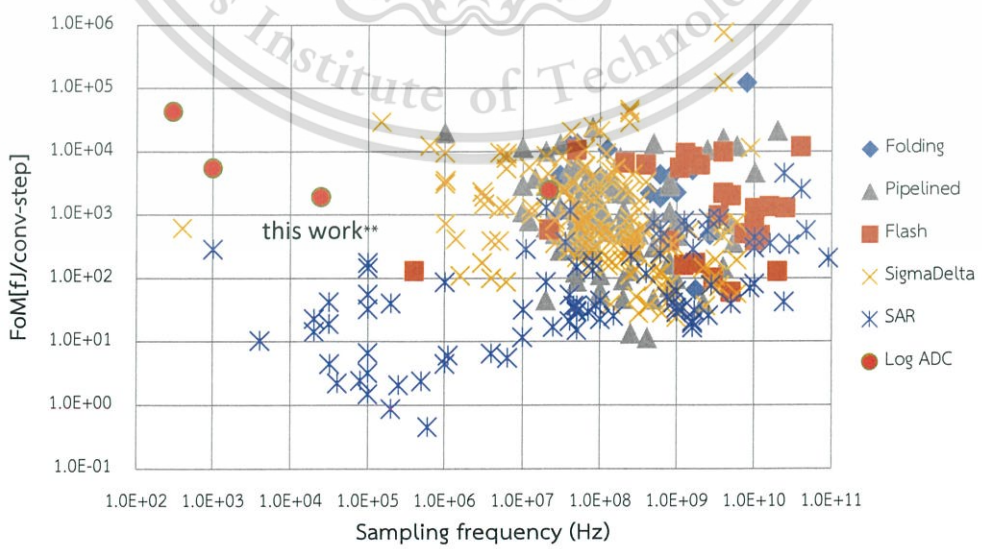

Figure 4.17 The comparisons of ADC performance with other approaches

4.5 Measurement results

The full micrograph and the zoomed-in view of proposed ADC are depicted in Figure 4.18 which occupies a total area of 0.164 mm^2 (400 µm x 410 µm). Figure 4.19 depicts the schematic of the ADC test setup. The sinusoidal differential input and the reset and clock signals are provided using Agilent 30 MHz function/arbitrary waveform generator AFG3102. Keithly 2602A source meter is used to provide the reference bias current to the chip. The power supply and voltage reference are from the voltage regulator which supply from the 3V battery. Power supplies and voltage reference are decoupled on board as well as on-chip. Figure 4.20 shows a photograph of the test PCB.

Figure 4.21 Measured input-output characteristic of the prototype 3-bit logarithmic SAR ADCFigure 4.21 plots the measured 3-bit course conversion input-output characteristics of the prototype chip, compared with the theoretical and post-layout simulation when input voltage is increased from 0 to 1V. The transfer characteristics exhibit linearity over the input amplitude ranging from 0.01 V to 1V, which is equal to the input dynamic range of 40 dB. Figure 4.22 plots the calculated integral nonlinearity (INL) and differential nonlinearity (DNL). The maximum INL and DNL are +0.2/-0.1 LSB and +0.5/-0.1 LSB, respectively.

Figure 4.23 shows the measured 6-bit, two step input-output characteristic of prototype chip compared with the theoretical and post-layout simulation. The transfer characteristics exhibit linearity over the input amplitude ranging from 0.01 V to 1V for 3-bit course conversion. For 3-bit fine conversion, the transfer characteristics exhibit linearity over the input amplitude ranging from 0.1 V to 1V. The input is below 0.1V for 3-bit course conversion At Vin < 0.1 V, the fine conversion error may occur from the commode-noise coupling in the input, power supply due to the single-ended structure is unable to suppress even harmonic distortions, noise as the maximum LSB step size in only 3.9 mV.

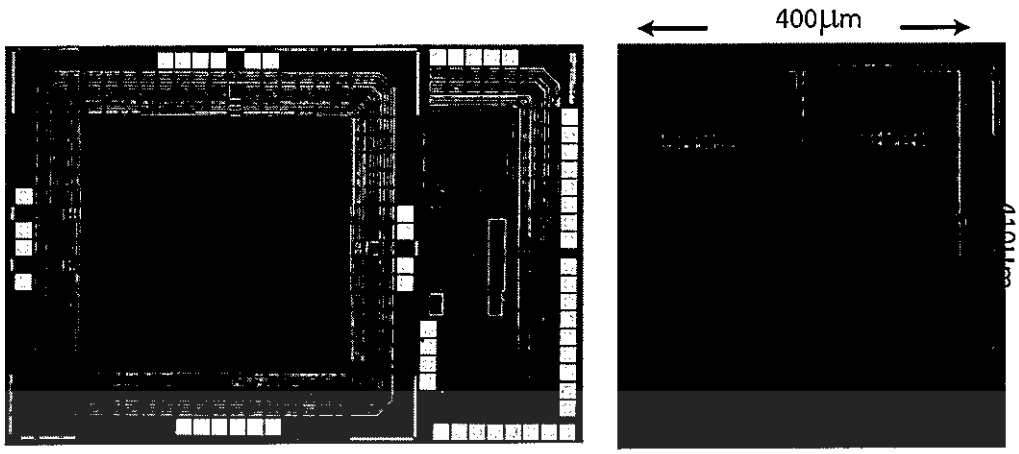

Figure 4.18 Layout of the proposed logADC with the size of 400 µm × 410 µm

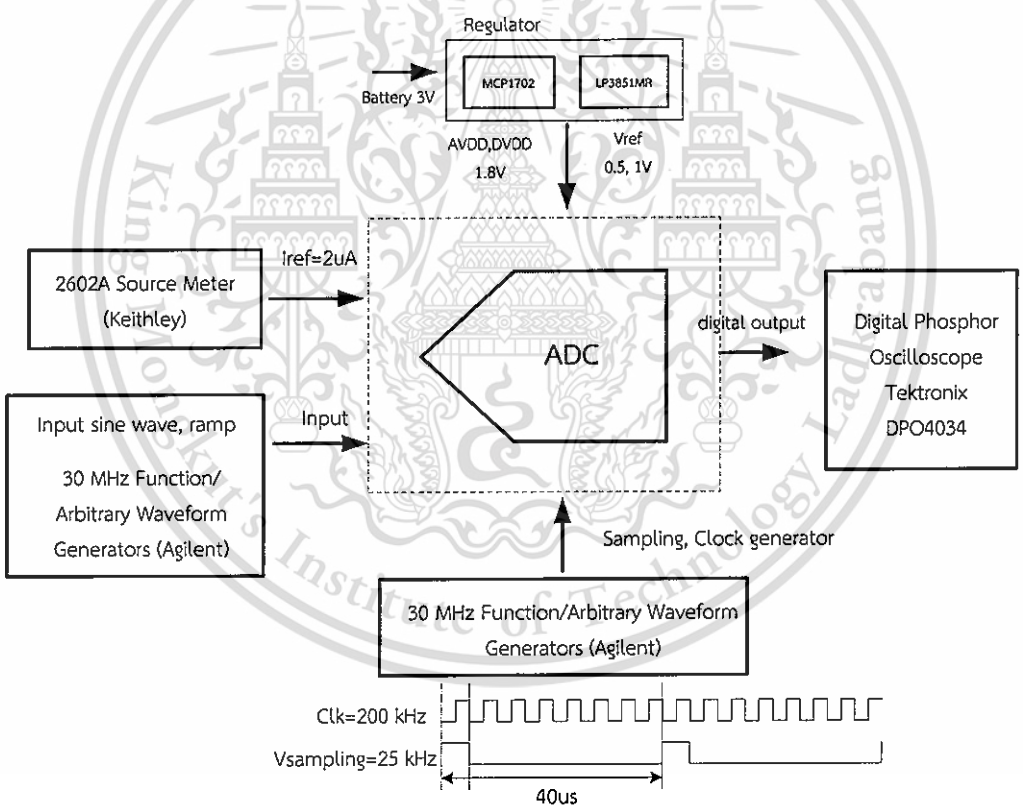

Figure 4.19 The schematic of test setup

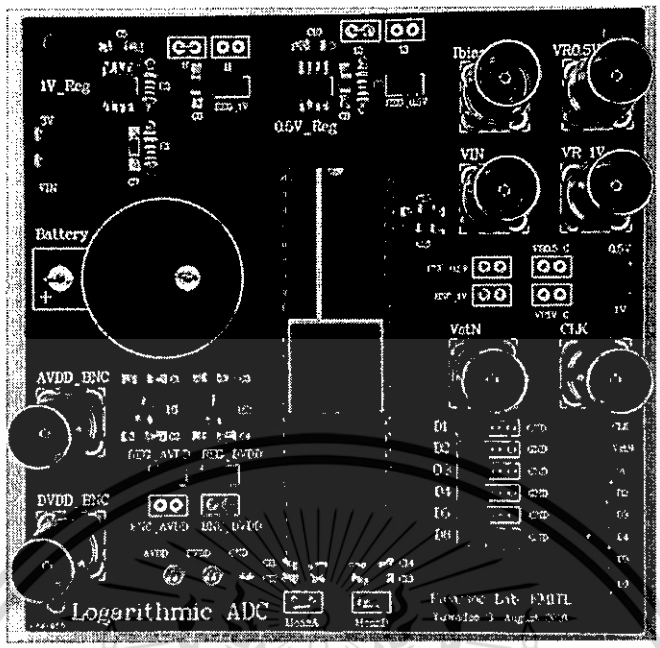

Figure 4.20 PCB photograph

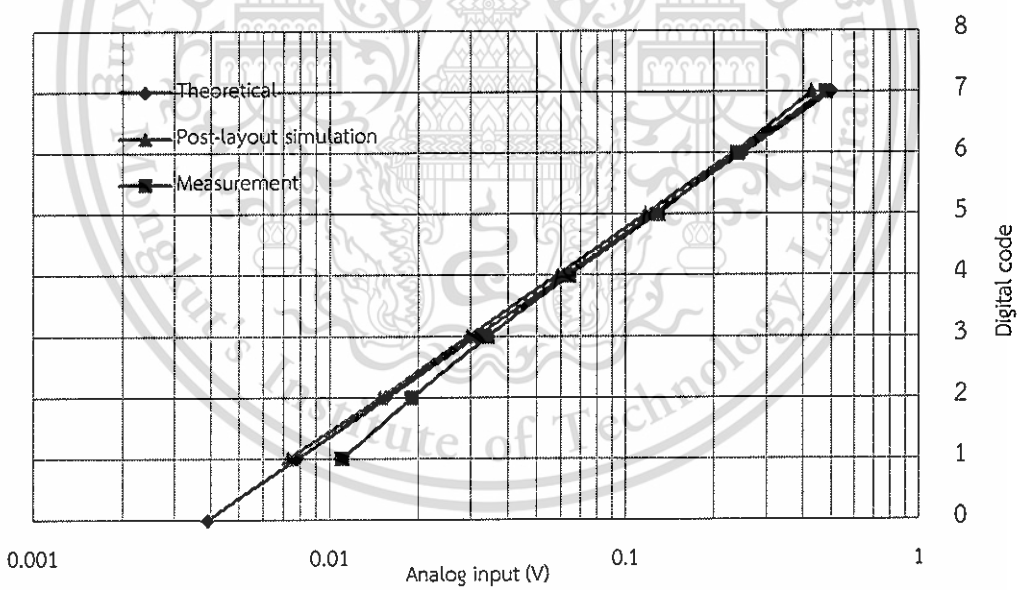

Figure 4.21 Measured input-output characteristic of the prototype 3-bit logarithmic SAR ADC

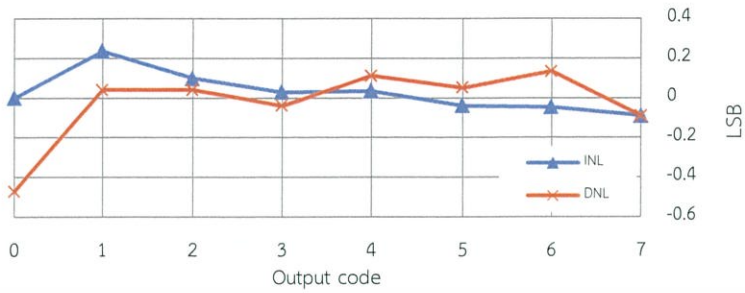

Figure 4.22 Measured INL and DNL.

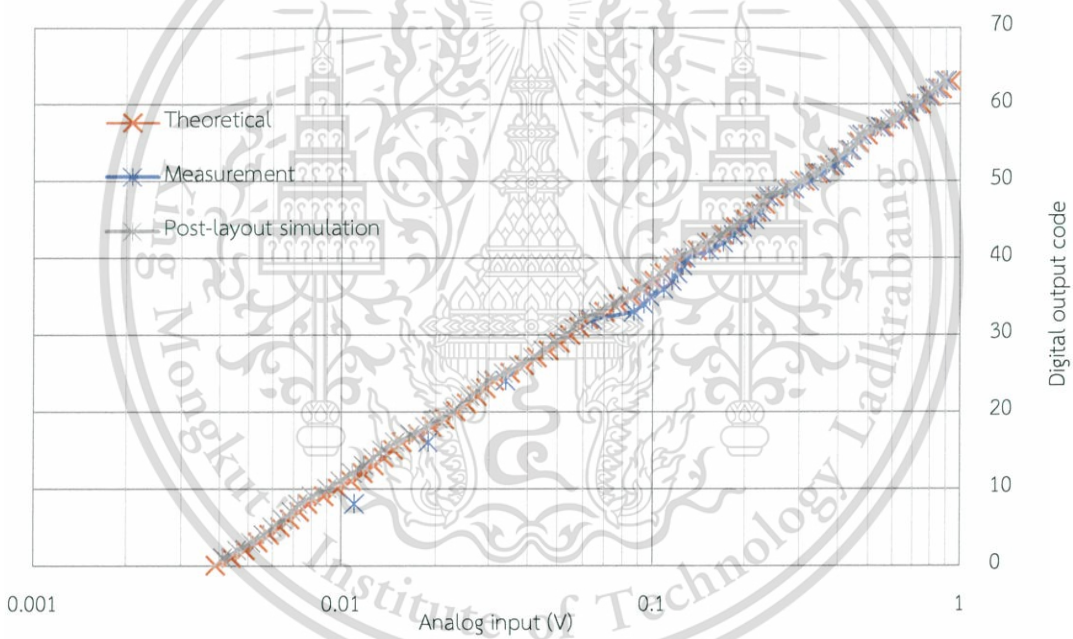

Figure 4.23 The measured input-output characteristic of the proposed 6-bit logarithmic ADC

Chapter 5

Conclusions and future work

This thesis has described the design and implementation of ultra-low power biomedical sensor interface circuits, in particular, the BPF and ADC that are suitable for implantable medical devices.

5.1 Conclusions

In Chapter 1, the motivation of innovations in healthcare technology and background of implantable medical innovations was discussed. The cochlear implant and neural recording and DBS are examples of implantable medical devices which present many challenging issues still needed to be addressed. Low power dissipation is the main concern for a system which is desired to be operating for up to 10 years without the need for a battery replacement. The BPF and ADC, which are parts of the analog front-end block, are designed and realized in this research work.

An overview of low power BPF and ADC was described in Chapter 2. G_m-C filter topologies have shown to be a good choice in low-power and low-voltage systems. Various techniques to improve linearity performances of the G_m, the subthreshold operation and the gyrator-based active inductor were reviewed. Several design strategies for low power BPFs have attempted to meet requirements of the low noise, wide dynamic range, compact physical area, low-power consumption and wide-tuning range filter. In the second part of this chapter, a performance comparison of various architectures of ADCs was described. The SAR architectures have shown to be high energy efficiency and a simple structure. The logarithmic coding technique offers an attractive solution for systems requiring wide dynamic range, such as in neural recording and cochlear implant.

In Chapter 3, a low-power, tunable high-Q 4th-order G_m-C BPF based on the gyrator-C active inductor was proposed. The filter structure was realized by using a single MOSFET as the transconductor element. The capacitive input attenuation technique was used to improve the linearity of the filter. The filter was verified by post-layout simulation in a 0.18 μm CMOS technology. The power consumption of the filter was in the order of pW to a few nW depending on the center frequency. The quality factor, passband gain and center frequency were easily tunable from 80

Hz to 6.18 kHz by changing the transconductances. The cascode active inductor and negative resistance techniques have been employed to improve the quality factor. The Q-value of the filter was tuned from 2 to 50 by varying the ratio of the bias current of transconductor.

A two-step logarithmic SAR ADC was described in Chapter 4. The two-step ADC conversion was proposed to achieve a piecewise linear approximation of the desired logarithmic function. The DAC presented in this work was divided into logarithmic DAC and linear-DAC. The filter has been verified by post-layout simulation and measurement in a 0.35 μm CMOS technology. The entire system consumed 4.36 μW to 14.6 μW from a 1.8 V supply. The SNDR was 31.7 dB, which is equivalent to the ENOB of 4.97. The ADC achieves 18.6 pJ/conversion-step, maximum INL and DNL of 0.45 LSB. The proposed ADC succeeds the maximum resolution of 11-bit when the input amplitude is below 7.81 mV and achieves the minimum resolution of 4-bit when the input amplitude is more than 0.5 V.

5.2 Possible future work

This section lists the future work that can be done to improve the performance of the proposed circuits in this work.

1. Although a higher-order bandpass filter can be cascading a number of second-order filter stages, it requires a voltage buffer to avoid the loading effect between two identical 2^{nd}-order filter. This should be developed by design each 2^{nd}-order filter stage independently thus the design of a higher-order filter is greatly simplified. This can allow for further reducing power consumption and chip area.
2. The proposed single-ended logarithmic ADC in Chapter 4 should be designed to a fully-differential to suppress even harmonic distortions, common-mode noise and to increase signal swing.

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APPENDIX A

Analysis of the 2nd-order active inductor based G_m-C bandpass filter

A.1 Transfer function

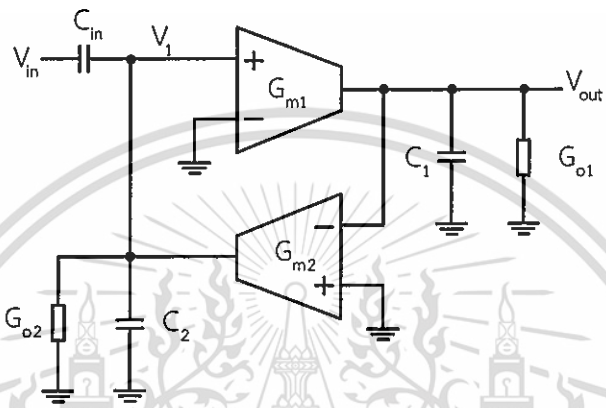

Figure A.1 Block diagram of a single-ended, 2nd-order bandpass filter topology

Consider the block diagram of a single-ended, 2nd-order Gm-C bandpass filter topology shown in Figure A.1. We note that in order to simplify analysis, the transconductances of the transconductors are constant. Write KCL at node V_1 and node V_{out}

Node V_1 $$sC_{in}(V_{in} - V_1) = G_{m2}V_{out} + (G_{o2} + sC_2)V_1 \quad (A.1)$$

Node V_{out} $$G_1V_1 = V_{out}(G_{o1} + sC_1) \quad (A.2)$$

Then

$$V_1 = \frac{V_{out}(G_{o1}+sC_1)}{G_1} \quad (A.3)$$

Then (A.1) was substituted with (A.3) so that the transfer function $H_{(s)}$ is described as

$$sC_{in}V_{in} - \frac{sC_{in}V_{out}(G_{o1}+sC_1)}{G_1} = G_{m2}V_{out} + (G_{o2} + sC_2)\frac{V_{out}(G_{o1}+sC_1)}{G_1} \quad (A.4)$$

(A.4) become

$$\frac{V_{out}}{V_{in}} = \frac{\frac{sC_{in}G_{m1}}{C_1(C_2+C_{in})}}{s^2+s\left(\frac{G_{o2}}{C_2+C_{in}}+\frac{G_{o1}}{C_1}\right)+\frac{G_{m1}G_{m1}}{C_1(C_2+C_{in})}+\frac{G_{o1}G_{o1}}{C_1(C_2+C_{in})}} \quad (A.5)$$

We assume $\frac{G_{m1}G_{m1}}{C_1(C_2+C_{in})} \gg \frac{G_{o1}G_{o1}}{C_1(C_2+C_{in})}$

$$\frac{V_{out}}{V_{in}} \cong \frac{\frac{sC_{in}G_{m1}}{C_1(C_2+C_{in})}}{s^2+s\left(\frac{G_{o2}}{C_2+C_{in}}+\frac{G_{o1}}{C_1}\right)+\frac{G_{m1}G_{m1}}{C_1(C_2+C_{in})}} \quad (A.6)$$

The transfer function of a generic bandpass is

$$H(s) = K\frac{s\frac{\omega_0}{Q}}{s^2+s\frac{\omega_0}{Q}+{\omega_0}^2} \quad (A.7)$$

For the proposed G_m-C bandpass filter, the center frequency is given by

$$\omega_0 = \sqrt{\frac{G_{m1}G_{m1}}{C_1(C_2+C_{in})}} \quad (A.8)$$

Solving for the quality factor (Q)

$$\frac{\omega_0}{Q} = \frac{G_{o2}}{C_2+C_{in}} + \frac{G_{o1}}{C_1} \quad (A.10)$$

$$Q = \frac{\sqrt{G_{m1}G_{m2}C_1(C_{in}+C_2)}}{G_{o2}C_1+G_{o1}(C_{in}+C_2)} \quad (A.11)$$

And the passband gain K is

$$K\left(\frac{\omega_0}{Q}\right) = \frac{sC_{in}G_{m1}}{C_1(C_2+C_{in})} \quad (A.11)$$

$$K = \frac{G_{m1}C_{in}}{G_{o2}C_1+G_{o1}(C_{in}+C_2)} \quad (A.12)$$

APPENDIX B

List of publications

JOURNALS

1. **Y. Sundarasaradula** and A. Thanachayanont, "A 1-V, 6-nW Programmable 4th-order bandpass filter for biomedical applications," in *Int. Journal of Analog Integrated Circuit and Signal Processing*,2016

INTERNATIONAL CONFERENCES

1. **Y. Sundarasaradula**, T. Constandinou and A. Thanachayanont, "A 6-bit, two-step successive approximation logarithmic ADC for biomedical applications," in *Proc. Int. 23rd IEEE Int. Conf. on Electronics Circuit and System,* 2016.
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