ON THE SYNTHESIS OF A CLASS OF ELECTRONICALLY TUNABLE IMMITTANCE FUNCTION SIMULATORS EMPLOYING VDTAs

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หัวข้อวิทยานิพนธ์	การสังเคราะห์ตัวจำลองฟังก์ชันอิมมิตแตนซ์แบบปรับค่าได้ทางอิเล็กทรอนิกส์โดยใช้ VDTA
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บทคัดย่อ

วิทยานิพนธ์ฉบับนี้นำเสนอการออกแบบและสังเคราะห์วงจรจำลองฟังก์ชันอิมมิตแตนซ์แบบปรับค่าได้ด้วยวิธีการทางอิเล็กทรอนิกส์โดยใช้วงจร VDTA (voltage differencing transconductance amplifier) เป็นอุปกรณ์แอคทีฟหลัก ซึ่งประกอบด้วย วงจรคูณค่าอิมพีแดนซ์ที่ปรับค่าได้ วงจรจำลองตัวเหนี่ยวนำและตัวเก็บประจุไฟฟ้าแบบลอยตัว และวงจร FDNR (frequency-dependent negative resistance) วงจรจำลองฟังก์ชันอิมมิตแตนซ์ที่นำเสนอในวิทยานิพนธ์นี้ ใช้อุปกรณ์พาสซีฟในการสังเคราะห์วงจรจำนวนน้อยและต่อในแบบเทียบกราวด์ทั้งสิ้น ทั้งยังสามารถปรับค่าองค์ประกอบสำคัญของวงจรได้ด้วยวิธีการทางอิเล็กทรอนิกส์ โดยการควบคุมอัตราขยายค่าความนำของวงจร VDTA นอกจากนี้ในวิทยานิพนธ์ฉบับนี้ยังได้กล่าวถึงตัวอย่างการประยุกต์ใช้วงจรที่นำเสนอในการสังเคราะห์วงจรกรองสัญญาณแลดเดอร์ ซึ่งแสดงให้เห็นถึงสมรรถนะของวงจรที่ทำให้สามารถปรับค่าคุณสมบัติสำคัญของวงจรได้ทางอิเล็กทรอนิกส์ ในที่นี้ได้ใช้โปรแกรม PSPICE ทำการจำลองการทำงานของวงจรเพื่อศึกษาและตรวจสอบคุณสมบัติในการทำงานของวงจรที่นำเสนอและวงจรประยุกต์ใช้งานว่ามีความสอดคล้องเป็นไปตามหลักการทางทฤษฎี

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ABSTRACT

This thesis deals with the canonical topologies for simulating a class of electronically controllable immittance functions based on the employment of the recently introduced active building block, namely voltage differencing transconductance amplifiers (VDTAs), as fundamental active components. The actively simulated immittance functions developed in this thesis are generalized tunable impedance multipiler, floating inductance, capacitance simulators. frequency-dependent negative resistance (FDNR). All the developed simulators uses a minimum number of passive components, which are grounded. The equivalent values of the realized simulators can be tuned by electronic means through the transconductance parameters of the VDTAs. Some illustrative applications on the syntheses of active RLC ladder filters using the proposed actively immittance function simulators are also given that demonstrates the possibility of electronic tuning. To verify the theoretical expectation, all the simulators and their applications are designed and simulated with PSPICE program.

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Sumalee Unhavanich

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CHAPTER 1

Introduction

1.1 Statement and Signification of The Problems

Actively simulated immittances, namely inductance simulator, capacitance multiplier and frequency-dependent negative resistances (FDNR), are essential electric circuits that are widely found in several areas of analog signal processing applications, and are also the fundamental active building blocks in general active network synthesis. Since simulated immittances are the most often used in area like active filters, oscillator design, gyrators, and cancellation of unwanted parasitic elements, they have became important research issues [1]. This is attributed to their effective small chip area, weight, electronic tunability features, integrability, and cost. In addition, the FDNR-based filters have been particularly successful in achieving the low-sensitivity property of classical LC filters [2]. Recent literatures have attracted comparatively more attention to this class filter [3]-[8]. Therefore, special attention was then paid to the design and synthesis of various immittance function simulators by the use of different high-performance active building blocks such as second-generation current conveyor (CCII) [9]-[11], third-generation current conveyor (CCIII) [12], operational transresistance amplifier (OTRA) [13]-[14], and four-terminal floating nullor (FTFN) [15]. That is why replacement of physical inductors

and capacitors by synthetic ones in conventional passive LC filters belongs to the well-known methods of high-order low-sensitivity filter design.

1.2 State of The Art

The ever present demand of a miniaturize and compact circuits and systems has stimulated the fabrication of complete analog function circuits on a small silicon chip area named as integrated circuit (IC). In order to enhance the performance of analog processing IC, the analog researchers prefer to use active building blocks. During the last decade, a huge number of active building blocks that suitable for analog signal processing were noticed [16]. Many attentions are focused on such novel active element design with electronic tunability property. Therefore, these elements have also favarable features in several particular applications. The first development in this area was started with discovery of current conveyor by Smith and Sedra [17], Fabre [18], and Svoboda et. al. [19]. As a result, many other active buliding blocks obtained from the circuit ideas in [17]-[19], which allow the possibility of electronic control their parameters, were developed and innovated, as well as frequently applied for circuit design and synthesis. In 2008, great circuit ideas in the field of active building blocks for providing the potentiality in a class of analog signal processing applications were reviewed and summarized [16]. Among these, the newly introduced active element called voltage differencing transconductance amplifier (VDTA) is also introduced, as an alternative to the existing current differencing transconductance

amplifier (CDTA) [20]. In the VDTA device, the differential input voltage, rather than current as in CDTA, is transformed to the output current at the z-terminal by the first transconductance gain and the voltage drop at the terminal z is then conveyed to the output currents at the terminals x+ and x- by the second transconductance gain. Accordingly, a large number of analog function circuits and systems based on based on VDTAs have recently been developed [21]-[25].

This dissertation describes the results of some researches and studies on the design and synthesis of a class electronically tunable immittance function simulators for analog signal processing applications which include ladder LC filter design and general active network synthesis. The described simulators have been created employing VDTAs as the main active building blocks.

1.3 Aims of The Dissertation

This dissertation thesis deals with the design and synthesis of immittance function simulators based on the use of VDTAs as active elements, which is considered to be an effective approach in active network synthesis and ladder filter design. The possibility of the electronic control property is one of the major features of the design. Therefore, three main lines of the research will be attacked in this work. The first topic deals with a realization of a general impedance multiplier circuit comprising only two VDTAs and one scaling impedance, which is capable of electronic tuning to the grounded impedance functions, i.e. resistor, capacitor and

inductor. The second objective of study focuses on the structural configuration of two novel topologies for simulating electronically controllable floating inductor and capacitor. The simulators are composed of only grounded capacitor as passive elements, resulting in canonical structures and quite suitable for further integration. The final objective pursued in this thesis, then, is the successful design and implementation of the floating FDNR simulator topology consisting three VDTAs and two grounded capacitors. No external passive resistor is required for this realization. It should be noted here that, all the immittance function simulators having electronic tuning option of the important parameters should be preferred, especially in IC implementation point of view. The workability of the simulators developed in this thesis has been proved by PSPICE simulation for various parameters and comparing it with the theoretical analysis. To justify the usefulness of the circuits, some illustrative examples are also provided.

1.4 Novel Concepts of The Thesis

In the following paragraph, novel concepts and techniques contributed in this thesis are summarized into these categories.

1) Firstly, one of the newly proposed active building blocks namely voltage differencing transconductance amplifier (VDTA) has been used to developed various immittance function simulators, where can be our focus concentrated in view of the

fact that the possibility of circuit performance tuning through the external bias current is achieved.

2) The second line of this study focuses on a circuit design of an actively generalized impedance multiplier using only two VDTAs and one external impedance to be scaling. The proposed impedance multiplier circuit requires no component-matching conditions for its realization. It also provides electronic adjustability to the realized impedance multiplification functions by the transconductance gains of the VDTAs.

3) The third deals with the topologies of floating inductance and capacitance simulations using VDTAs as active components together with a grounded capacitor as a passive component [25]. The merit of these schemes is that the values of the simulated inductor and capacitor are tunable electronically through the transconductance parameters of the VDTAs. They also do not require any alteration of circuit components. Since the developed simulators use only a grounded capacitor, their structures are resistorless and suitable for IC design [26].

4) The fourth aim of this thesis is to present a simple design for the synthesis of an electronically tunable floating FDNR simulator circuit [8]. The approach shows that the resulting circuit contains only three VDTAs and two grounded capacitors without needing any external resistors. The equivalent *D*-element value of the realized FDNR can be adjusted electronically by adjusting the supplied bias currents of the VDTAs.

In conclusion, it can be realized that this thesis offers some novel simulator circuits having improved performances with respect to electronic tunability, component count, integrability, silicon chip area economization and power consumption. These simulators can be of great value in active filter design and analog signal processing area. Next, we will outline the contents of each chapter.

1.5 Organization of The Thesis

The main thrust of this thesis has been on the realization of the new circuit configurations for simulating the electronically tunable immittance functions using recently introduced active element, namely voltage differencing transconductance amplifier (VDTA). The main context of the dissertation is organized into six chapters, and five appendices. Each chapter includes references at its end. Each chapter contains a brief introduction of the study undertaken along with the detailed circuit descriptions, transfer function analysis, parameters used in that circuit, and the computer simulation results of the circuits belonging to the scope of that particular chapter, as well as sub-conclusion. All these simulators have been realized for further implementation in IC technology. The contents of the thesis can be summarized as follows.

Chapter 1 is the introduction of the research undertaken in this dissertation. This section begins with the statement and significance of the research topic, and subsequent the state of the art in the field of active building blocks suitable for analog

signal processing circuits. In the next section, the objectives and the new concepts of the work to design various immittance function simulators have been presented. Finally, the organization of the thesis will also be described in this section.

Chapter 2 is mainly concerned with the main characteristic of the VDTA device, which is the active circuit building block mainly used in this thesis. There is an elaboration on how this device is useful in realizing various analog function circuits, and why this should be selected for the design of circuits. This chapter starts with the description of the distinguishing features of the VDTA, and subsequently gives details of some of circuit design techniques for realizing the VDTA. It also describes the historical development and some realizations of the VDTA element.

In chapter 3, a simple circuit configuration for realizing an impedance multiplier using VDTAs as the major active components is presented and analyzed. The proposed impedance multiplier circuit contains only two VDTAs along with external impedance under control. The equivalent value of the realized multiplier can be tuned electronically through the transconductance parameters of the VDTAs. The non-ideal analysis and the sensitivity study of the proposed circuit are investigated in detail. To demonstrate the performance of the proposed multiplier circuit and verify the theory, PSPICE simulations with TSMC 0.35-μm CMOS process parameters are accomplished.

Chapter 4 outlines the simulation of the floating inductor and capacitance multiplier circuit. It describes the two novel topologies using only VDTAs and a

grounded capacitor. The influences of the VDTA non-idealities on the performance of the simulators are discussed in detail. The developed simulators can be tunded electronically, and do not require any component-matching condition. All the capacitors are grounded, hence suitbale for monolithic design. The characteristics of the proposed simulator circuits have been demonstrated using PSPICE simulation.

In chapter 5, a detailed discussion on the simulation of an electronically tunable FDNR simulator circuit is given. The configuration is constructed with only three VDTAs and two grounded capacitors without any external resistors. The presented FDNR simulator exhibits electronic tuning of its *D*-element value via the bias currents of the VDTAs. As application examples, the fourth-order Butterworth bandpass and lowpass filters are designed based on the use of the proposed tunable floating FDNR simulator. Finally, the theoretical formulations presented in this chapter are verified by simulation results.

Chapter 6 of the dissertation describes the conclusion of the work done and also lists some of the future work which can be carried out in this area.

Finally, appendices are given, which contain the detailed analysis of the proposed simulators developed in this thesis.

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CHAPTER 2

Voltage Differencing Transconductance Amplifier (VDTA):

Characteristics, Historical Developments and Some Realizations

---

2.1 Introduction

Ever since the introduction of the current differencing transconductance amplifier (CDTA) in 2003, it has been successfully acknowledged to be a versatile active building block in designing analog circuits [1]. The CDTA can be considered as a collection of current differencing unit and multi-output transconductance amplifier; it thus offers large dynamic range and wide bandwidth similar to its current-mode counterparts such as a current differencing buffered amplifier (CDBA) [2] and an operational transconductance amplifier (OTA) [3]. Various types of CDTA-based applications were and are being reported in the literature; see [4]-[12] and the reference cited therein. On the other hand, due to its current-mode operation nature, this element is therefore suitable for realizing of particularly current-mode filters and oscillators. In order to achieve the inherent advantages of voltage-mode signal processing, an innovative design which does not involve a current differencing unit is highly desirable. Moreover, the disadvantage of this device when operating in voltage-mode is that several external passive resistors are necessary at the input terminals for current to voltage conversion.

In 2008, a brief introduction of recently reported modern active building blocks is given [13]. Among other things, the voltage differencing transconductance amplifier (VDTA) is another modern active building block recently introduced. This device was modified from the above mentioned CDTA device, in which the current differencer at the front-end stage is replaced by the voltage differencing unit. The VDTA is basically composed of two separate voltage-controlled current sources (normally represented by OTAs) with the required number of outputs and these sub-circuits are interconnected internally. This reveals that VDTA solutions offer electronic adjustability through their two independent transconductance parameters, and, thus the VDTA is quite suitable for electronically tunable active circuit synthesis. Another advantageous feature of the use of the VDTA as an active element is that compact structures in some applications can be achieved easily [13]-[14]. All these advantages make the VDTA an alternative choice for the implementation of analog signal processing circuits and solutions [15]-[21].

The main emphasis of this chapter is to address the basic concept of the VDTA and its property. It also describes the historical developments of the VDTA element in both CMOS and bipolar technologies, and some of VDTA-based basic circuit blocks leading up to the development of analog signal processing circuits and systems.

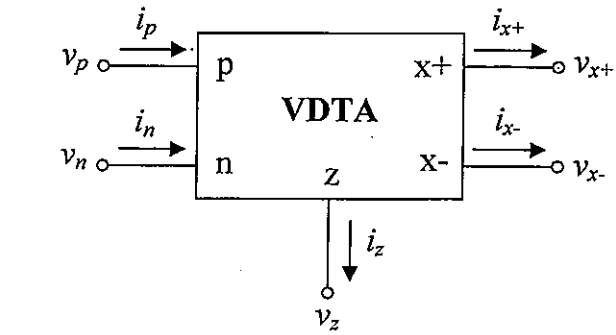
2.2 Description of VDTA

2.2.1 Ideal Behavior

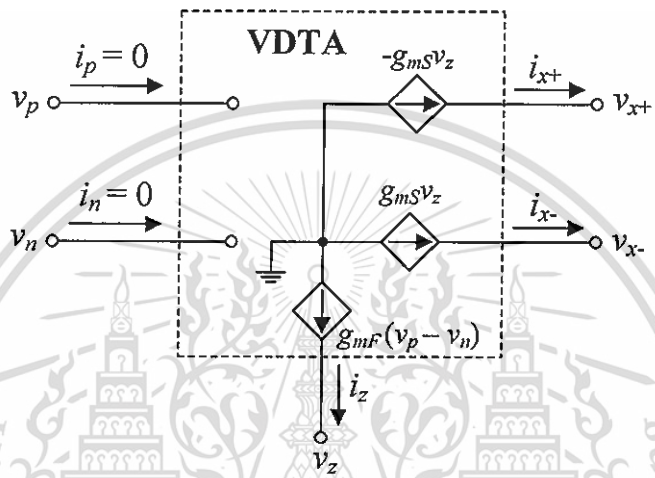
As shown symbolically in Figure 2.1, the VDTA is a five-teminal active building blcok, whcih consists actually of two interconnected transconductance stages. Each of them provides two separate electronically tunable trnasconducances g_{mF} and g_{mS}. A number of outputs of the first and second transconductance sction varies according to the particular requirements of intended applications [14], [16]-[17], which willl be discussed in the following section. The ideal operation of the VDTA can be characterized by the following matrix equation:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ g_{mF} & -g_{mF} & 0 \\ 0 & 0 & g_{mS} \\ 0 & 0 & -g_{mS} \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix} \tag{2.1}$$

From figure 2.1, the VDTA has a pair of high-impedance voltage inputs p and n and high-impedance current terminals z, x+ and x-. This device consists of an input voltage subtractor that transfers a differential input voltage (v_p-v_n) to the current through the z-terminal (i_z) by the first transconductance gain (g_{mF}), and a dual output transconductance amplifier that converts the corresponding voltage drop at the z-terminal to currents at the x-terminals by the second transconductance gain (g_{mS}). In general, both transconductances of the VDTA are controllable electronically by external supplied volatge or current.



(a)



(b)

Figure 2.1 : Ideal behavior of the VDTA.

(a) circuit representation (b) equivalent circuit

2.2.2 Non-ideal Behavior

In practice, the deviation from the ideal VDTA behavior can be divided into two categories, i.e. parasitic gain effects and parasitic impedance effects. Considering the parasitics and transfer errors, the simplified equivalent circuit represented the behavior of the non-ideal VDTA can be illustrated in figure 2.2 [19]. These result

from the shunt parasitic impedances ($R_p//C_p$), ($R_n//C_n$), ($R_z//C_z$), ($R_{x+}//C_{x+}$) and ($R_{x-}//C_{x-}$) appearing in parallel with the corresponging terminal p, n, z, x+ and x-, respectively. More specifically, β_F and β_S are the parasitic transconductance gains for the first and second stages of the VDTA, respectively. These parasitic values slightly differ from their ideal unit values by the effect of the VDTA tracking errors, those absolute values being much less than unity. Therefore, for the non-ideal case, the terminal relations of the VDTA describing in equation (2.1) can be rewritten by :

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ \beta_F g_{mF} & -\beta_F g_{mF} & 0 \\ 0 & 0 & \beta_S g_{mS} \\ 0 & 0 & -\beta_S g_{mS} \end{bmatrix} \cdot \begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix} \tag{2.2}$$

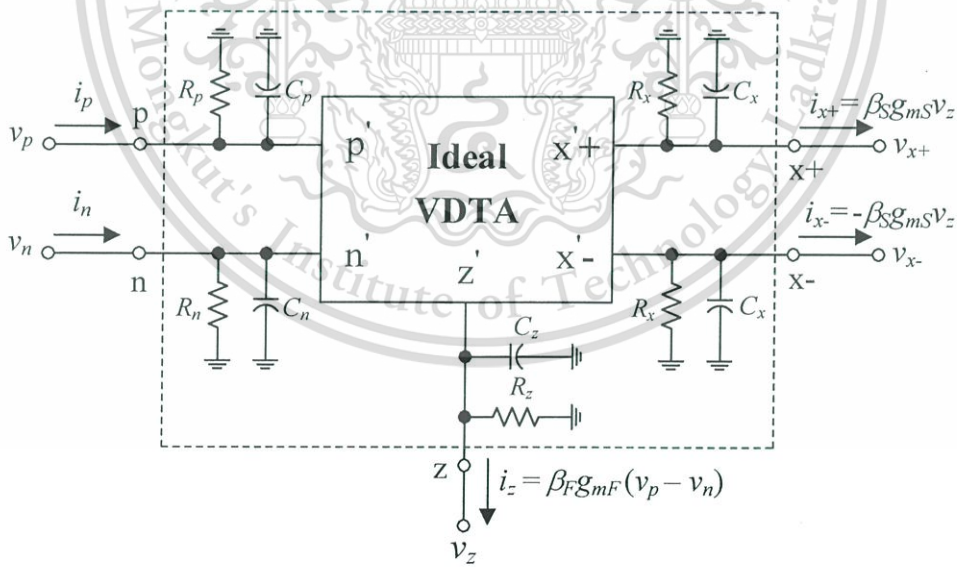


Figure 2.2 : Non-ideal behavioral model of the VDTA including parasitic elements.

2.3 Historical Developments and Some Realizations of VDTA

This section considers the design approaches for CMOS and bipolar VDTAs. Various circuit configurations, which can be used to implement this element, will be discussed in the following detail.

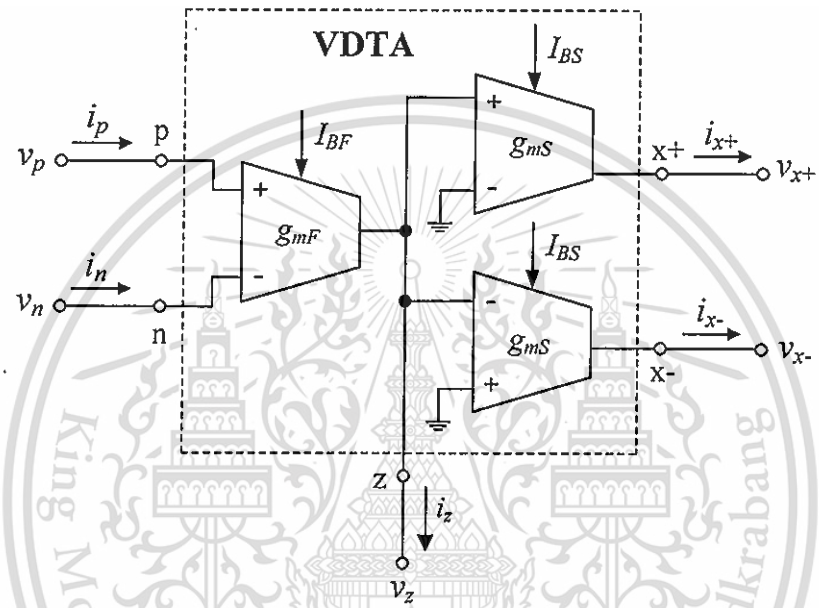


Figure 2.3 : Practical realization of VDTA using commercially available IC OTAs.

2.3.1 Practical VDTA Realization with Commercially Available IC OTAs

According to the basic concept of the VDTA element, it is actually composed of two voltage-controlled current sources with the required number of outputs and these sub-circuits are interconnected internally. An early practical realization of the VDTA can be obtained by using commercially available IC OTAs, such as CA3080 from Intersil [22], MAX435 from Maxim Integrated [23] and LM13700 by National Semiconductor [24]. From the model behavior in Figure 2.1, the practical VDTA

realization by using commercially available IC OTAs is represented in Figure 2.3. For example, if the well- known OTA CA3080 having a differential input and a single output is employed, the transconductances of the VDTA which are adjusted by two external biasing currents and strongly dependent on the ambient temperature can be given by, respectively, :

$$g_{mF} = \frac{I_{BF}}{2V_T} \tag{2.3}$$

and

$$g_{mS} = \frac{I_{BS}}{2V_T} \tag{2.4}$$

where I_{BF} and I_{BS} are respectively the external DC biasing currents of the first and second OTA, and $V_T \cong 26$ mV at 27°C is the usual thermal voltage given by kT/q, k = Boltzmann's constant = 1.38×10^{-23} J/K, T = the absolute temperature (in kelvins), and $q = 1.6\times10^{-19}$ Couloumb. However, the common drawback of OTAs is the low-level input voltage providing the linear mode of the amplifier. This can be in conflict with the requirements for a large dynamic range of signals being processed. When the VDTA is used to design for current-mode operation, the current limitations of the device should also be carefully monitored.

2.3.2 Simple CMOS Realization of VDTA Using Floating Current Sources

In 2011, A. Yesil, F. Kacar and H. Kuntman have suggested a simple CMOS-based VDTA circuit realization [14]. This technique is based on the use of a floating current source (FCS) [25], which realizes the dual-output transconductance. A complete implementation of this VDTA consisting of two Arbel-Goldminz

transconductances is presented in Figure 2.4. The circuit was designed in the TSMC (Taiwan Semiconductor) 0.35-μm CMOS process technology [Appendix A], and the aspect ratios of the MOS transistors have been provided in Table 2.1. According to the simulation results obtained from [16] and [20], the simulated performance of this VDTA element is summarized in Table 2.2.

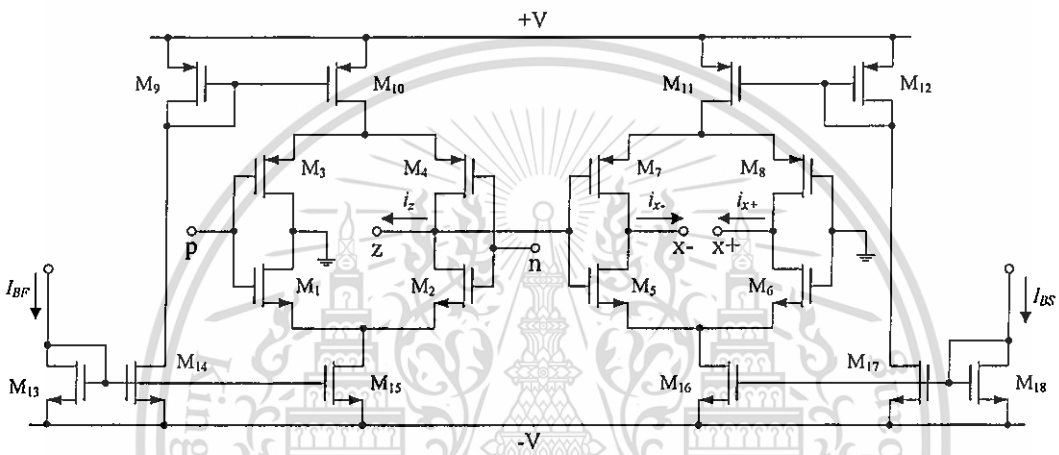


Figure 2.4 : Simple VDTA realization using two FCSs.

Table 2.1 : Transistor dimensions of the CMOS VDTA structure shown in Figure 2.4.

Transistors	W (μm)	L (μm)
M_1-M_2, M_5-M_6	16.1	0.7
M_3-M_4, M_7-M_8	28	0.7
M_9-M_{12}	21	0.7
M_{13}, M_{18}	7	0.7
M_{14}-M_{17}	8.5	0.7

Table 2.2: Simulated performance of the two FCS VDTA given in Figure 2.4.

Parameter	Value ($I_{BF} = I_{BS} = 10\mu A$)	Value ($I_{BF} = I_{BS} = 100\mu A$)
Transconductances g_{mF} and g_{mS} ($g_{mF} = g_{mS}$)	0.173 mA/V	0.512 mA/V
p terminal and n terminal input resistances ($R_p = R_n$)	> 2 GΩ	> 2 GΩ
z+ terminal output resistance	> 1 MΩ	> 1 MΩ
x+ terminal and x- terminal output resistances	> 1 MΩ	> 1 MΩ
3-dB frequency from p to z+ terminal	> 8 MHz	> 1 MHz

According to the input terminals, the output current at the terminal z (i_z) is generated. The intermediate voltage at the terminal z (v_z) is converted to the output currents at the terminals x+ (i_{x+}) and x- (i_{x-}). In this case, the g_{mF}- and g_{mS}-values of this element are determined by the output transistor transconductances, which can respectively be approximated as :

$$g_{mF} \cong \left(\frac{g_1 g_2}{g_1 + g_2}\right) + \left(\frac{g_3 g_4}{g_3 + g_4}\right) \tag{2.5}$$

and

$$g_{mS} \cong \left(\frac{g_5 g_6}{g_5 + g_6}\right) + \left(\frac{g_7 g_8}{g_7 + g_8}\right) \tag{2.6}$$

where $g_i = \sqrt{I_{Bi}\mu C_{ox}\frac{W_i}{L_i}}$ is the transconductance value of the i-th transistor (i = 1, 2, ..., 8), I_{Bi} is the bias current of the i-th transistor, μ is the effective carrier mobility,

C_{ox} is the gate-oxide capacitance per unit area, and W and L are the effective channel width and length of the i-th MOS transistor, respectively.

The major drawback of the VDTA structure given in Figure 2.4 is that the output resistance of the traditional FCS stage is not high enough for utilizing in some application. In order to increase the output resistance, the improved FCS stage can be employed [26]. Although the output impedance value obtained from this structure is improved, the output voltage swing drops up to $V_{DS(sat)}$.

To improve the output voltage swing of the VDTA in Figure 2.4, the CMOS VDTA realization of Figure 2.5 is designed in which the simple current mirrors in previous study are replaced with wide-swing cascade current mirrors [27]. In addition, the terminal zc has been indicated in this structure and the copy of the current i_z (i_{zc}) is available at this terminal. According to principle current mirros, the advantage features of the wide-swing cascade current mirror are superior to high accuracy and high-output resistance. As a consequence, the minimum output voltage of the wide swing cascade mirror is about $2V_{DS(sat)}$ [28].

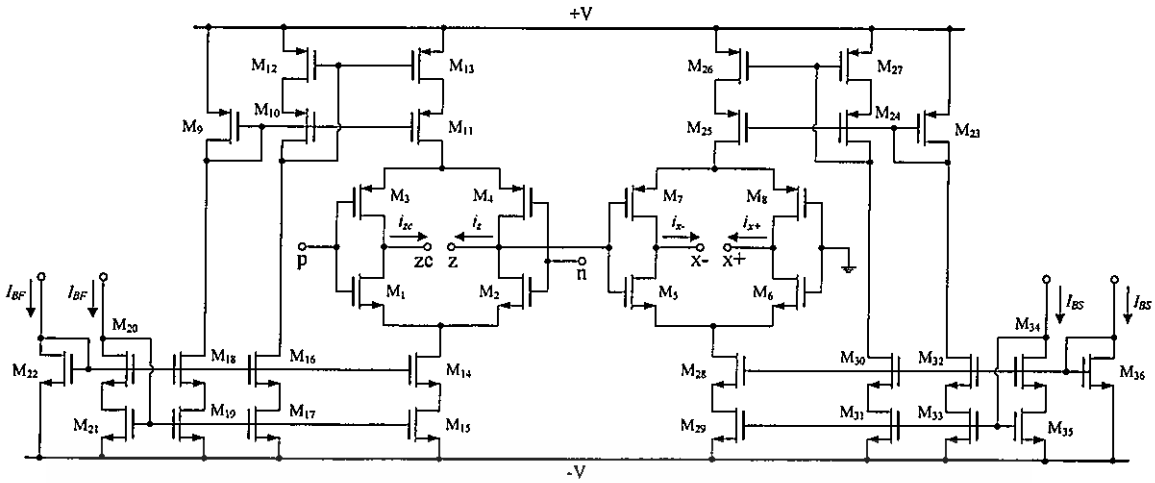


Figure 2.5 : CMOS VDTA realization with improved cascode current mirrors.

2.3.3 CMOS VDTA Realization Based on Bulk-Driven CMOS Technique

For low-voltage low-power applications, the VDTA element can be advantageous to implement with the utilization of the bulk-driven CMOS technique [29]. Figure 2.6 shows the two-stage bulk-driven implementation of OTA. The first combines of the bulk-driven differential input stage M_1 and M_2, and the current mirror M_3 and M_4 acting as an active load. The second stage is a simple inverter M_6 with active load M_7. The OTA output is connected to the output of the differential input stage through the compensation capacitor C_C and the resistor R_C, since the capacitor C_C actually acts as a Miller capacitance in the output stage. By properly setting the gate-source voltage to a value sufficient to turn on the transistor, then the operation of the bulk-driven MOS transistor becomes a depletion type.

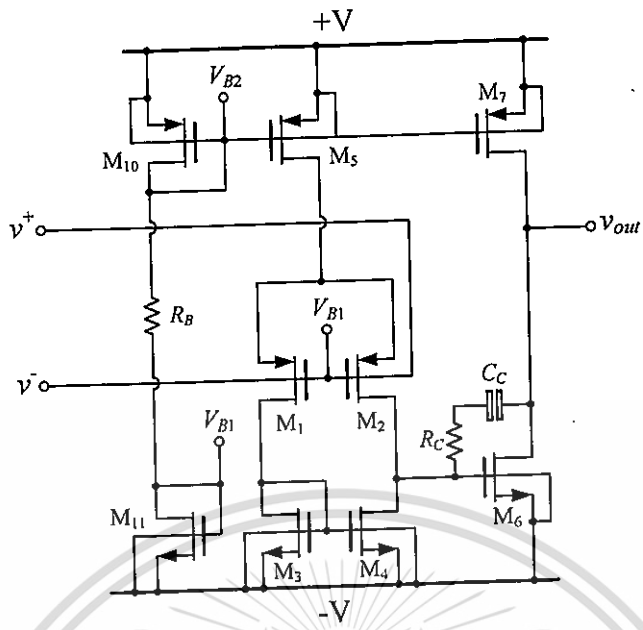


Figure 2.6 : CMOS implementation of bulk-driven OTA.

Based on the above bulk-driven OTA, one possibility implementation of the VDTA is shown in Figure 2.7 [30], which is realized by means of two OTAs of differential input single output type (DISO) and single input differential output type (SIDO). In DISO OTA of Figure 2.7(a), an additional bulk-driven voltage buffer M_{1B}-M_{9B} is connected between the terminal n and R_{adj1} to perform the high-input impedance level. Clearly, the circuit behavior can be modeled as Figure 2.7(b). This circuit is designed in the 0.18-μm MIETEC real CMOS process parameters with low supply voltage, namely ±0.6V, and the total power consumption was found to be 206 μW [31].

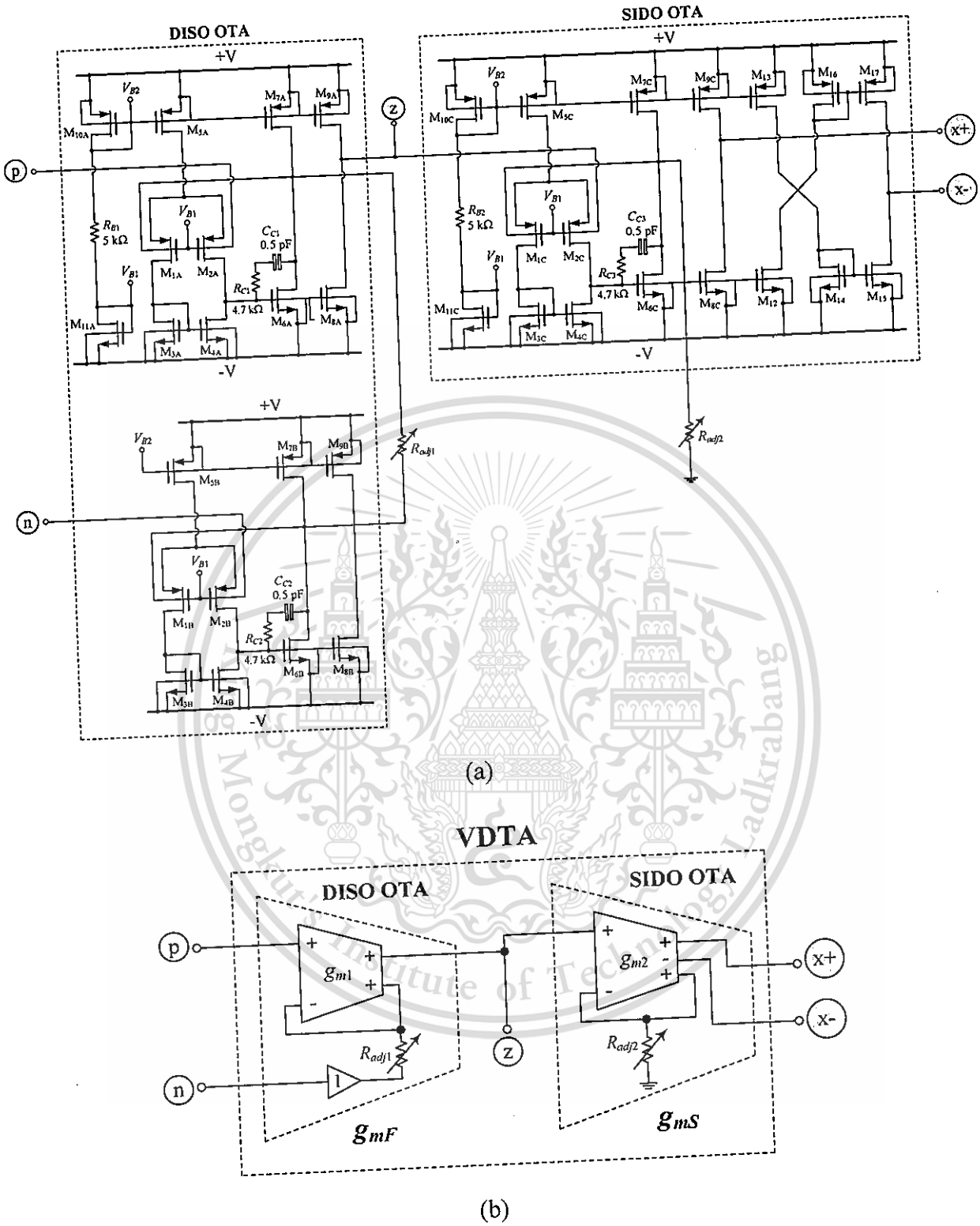


Figure 2.7 : VDTA realization based on bulk-driven OTA.

As it is seen from Figure 2.7(b), the VDTA transconductance parameters g_{mF} and g_{mS} can be tuned conveniently by adjusting the feedback resistors R_{adj1} and R_{adj2}, respectively. Straightforward analysis of the equivalent circuit of Figure 2.7(b) leads to the relations for the resulting variation of g_m by R_{adj}, as follows:

$$g_{mF} = \frac{g_{m1}}{1 + g_{m1}R_{adj1}} \tag{2.7}$$

and

$$g_{mS} = \frac{g_{m2}}{1 + g_{m2}R_{adj2}} \tag{2.8}$$

It is obvious from above relations that the transconductance g_{mF} (or g_{mS}) can be changed from g_{m1} (or g_{m2}) to zero, when changing the value of R_{adj1} (or R_{adj2}) from zero to infinity.

2.3.4 Modified VDTA with MO-CCII

In 2014, the lately modified VDTA has been developed by J. Jerabek, R. Sotner and K. Vrba [21]. Figure 2.8 illustrates the CMOS transistor-level structure of the modified VDTA, which was supplemented by the well-known structure of multi-output second-generation current conveyor (MO-CCII). This configuration is mainly composed of two OTA sections and one MO-CCII. In this structure, the MO-CCII functions as a dual-output current follower that helps to obtain the required number of current outputs of the first OTA stage, and the transistor-level solution of both OTA sections has been adopted from the structure presented in [16]. It should be mentioned that, in case of the first OTA section, the number of current outputs can be changed easily according to particular requirements. The modified VDTA of Figure

2.8 was designed and simulated in the TSMC LO (Logic Process) EPI (Epitaxial wafers) 0.18-μm CMOS technology [32] in PSPICE. Summary of the important simulated performance of this VDTA element is provided in Table 2.3.

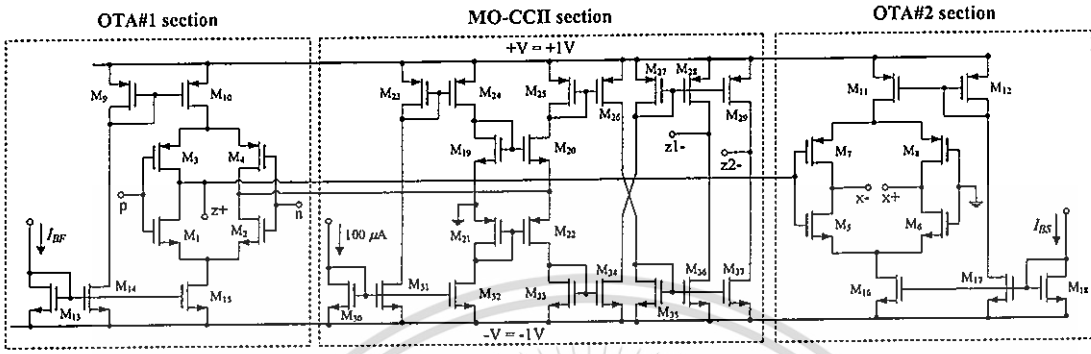


Figure 2.8 : Modified VDTA with MO-CCII section.

Table 2.3 : Performance data of the modified VDTA shown in Figure 2.8.

Parameter	Value ($I_{BF} = I_{BS} = 10$ μA)	Value ($I_{BF} = I_{BS} = 100$ μA)
Transconductances g_{mF} and g_{mS} ($g_{mF} = g_{mS}$)	0.115 mA/V	0.789 mA/V
p terminal and n terminal input resistances ($R_p = R_n$)	> 1 GΩ	> 1 GΩ
z+ terminal output resistance (R_{z+})	1.33 MΩ	187 kΩ
z_1- terminal and z_2- terminal output resistances ($R_{z1-} = R_{z2-}$)	149 kΩ	149 kΩ
x+ terminal and x- terminal output resistances ($R_{x+} = R_{x-}$)	663 kΩ	93 kΩ
3-dB frequency from p to z+ terminal	> 1 GHz	> 1 GHz
3-dB frequencies from p to z_1- and p to z_2- terminal	290 MHz	146 MHz

2.4 Basic Analog Functions Using VDTAs

In the following, we present a brief summary of some of the basic analog function realizations using VDTAa as fundamental active elements, which have been proposed from time to time.

2.4.1 Voltage Lossy Integrator

An electronically controllable voltage lossy integrator can easily be obtained using single VDTA and grounded capacitor as shown in figure 2.9. Since $i_z = g_{mF}v_{in}$ and $i_{x-} = -g_{mS}v_z = -g_{mS}v_o$, the current summation at the terminal z will be

$$i_z + i_{x-} = i_C$$

or

$$g_{mF}v_{in} - g_{mS}v_o = sCv_o \tag{2.9}$$

From above equation, the voltage transfer function of the circuit can be written as :

$$\frac{v_o}{v_{in}} = \left(\frac{g_{mF}}{g_{mS} + sC}\right) \tag{2.10}$$

Clearly, the circuit in Figure 2.9 acts as an electronically variable voltage lossy integrator.

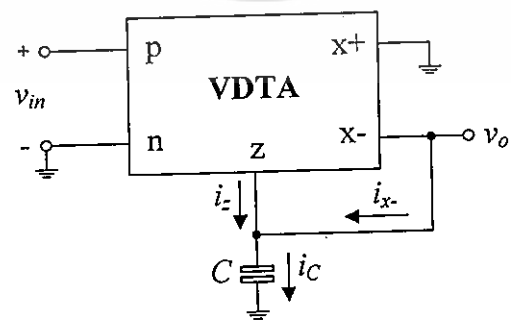


Figure 2.9 : VDTA-based voltage lossy integrator.

2.4.2 Current Lossless Integrator

Similarly, the tunable current lossless integrator circuit can be easily realized by using a single VDTA and grounded passive components, as depicted in Figure 2.10. With $i_z = g_{mF}v_{in} = g_{mF}(i_{in}/sC)$ and $i_o = g_{mS}v_z = g_{mS}(i_zR)$, then the corresponding relation of the ideal integrator in Figure 2.10 becomes :

$$\frac{i_o}{i_{in}} = \frac{g_{mF}g_{mS}R}{sC} \tag{2.11}$$

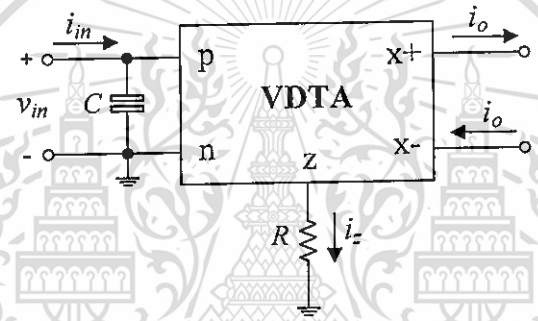


Figure 2.10 : VDTA-based current lossless integrator.

2.4.3 Voltage Proportional Block

Figure 2.11 illustrates the voltage proportional block based on the realization with a single VDTA. As can be seen, we can write the current at the terminal z as follows :

$$i_z = -i_{x-} \tag{2.12}$$

where $i_z = g_{mF}v_{in}$ and $i_{x-} = g_{mS}v_z = g_{mS}v_o$. Consequently, its voltage transfer relationship can be found to be :

$$\frac{v_o}{v_{in}} = \frac{g_{mF}}{g_{mS}} \tag{2.13}$$

As expressed by equation (2.13), this circuit performs as an electronically controllable voltage amplifier without needing any external passive resistors. Also from equation (2.13), it is worth mentioning here that the volateg transfer gain can be tuned linearly and electronically through adjusting the transconductance ratio (g_{mF}/g_{mS}). In addition, the usage of any external passive resistors is not necessary for this structure, which is especially important for achieving higher integration.

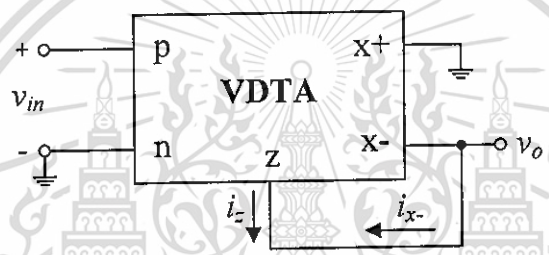


Figure 2.11 : Simple voltage proportional block using single VDTA.

2.4.4 Current Proportional Block

Another canonical structure is shown in Figure 2.12. As shown in the figure, the current proportional block can be realized very conveniently using a single VDTA with the following current realtion :

$$i_{in} = -i_z = -\left(-g_{mF} v_z\right) \tag{2.14}$$

and

$$i_o = g_{mS} v_z \tag{2.15}$$

Combining equation (2.14) into equation (2.15), and rearranging leads to

$$\frac{i_o}{i_{in}} = \frac{g_{mS}}{g_{mF}} \tag{2.16}$$

The gain of this block is electronically adjustable by controlling g_{mS} and/or g_{mF}.

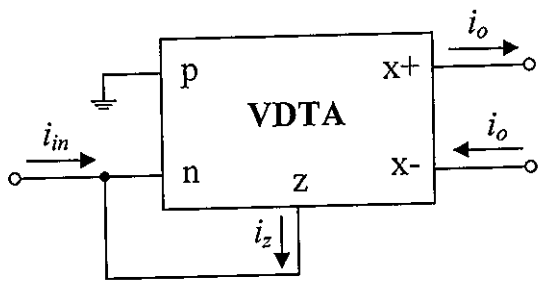


Figure 2.12 : Simple current proportional block using single VDTA.

2.5 Sub-conclusion

This chapter mainly concentrates on the essential characteristics of the VDTA including the detailed circuit descriptions, and circuit parameters. It also briefly describes the historical developments and some basic entities leading up to the implementation of VDTA elements. The great merit of the VDTA-based circuit realization is that the two separate transconductance gains are available as a design parameter. Thus, the need for external passive resistors is of course eliminated, which can be very conveniently implemented in monolithic form. In addition, this chapter also explains the basic VDTA-based active building blocks, which will be used simple VDTA realization using two FCSs in the design of impedance simulator circuits in all subsequent chapters.

2.6 References

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CHAPTER 3

Generalized Tunable Impedance Multiplier

3.1 Introduction

An impedance multiplier is a kind of active circuit that effectively inflates the impedance presented by the load. Accordingly, the generalized impedance multiplier is a useful element for various functional analog applications, such as active filters, oscillators, biasing and impedance matching, and cancellation parasitic elements. A most appropriate application of the impedance multiplier is in the simulation of the tunable passive element such as resistor (R), inductor (L) and capacitor (C). It may also be used in IC fabrication for simulating large valued R, L and C. During the past few years, several attempts to realize general impedance function simulators using various analog active building blocks have been presented in the open literature [1]-[13]. However, they still suffer from the following weakness. For example, the works presented in [1]-[9], [14] contain three or more active devices. In [1]-[8], [10]-[13], they cannot be adjusted electronically.

Although a large number of modern electronic active building blocks have been reviewed and considered as alternatives to the classical voltage-mode operational amplifier [15], the voltage differencing transconductance amplifier (VDTA) has been found to be particularly attractive in various analog signal processing and signal generating applications [16]-[19]. This device combines the advantages of voltage

differencing unit and the transconductance amplifier. Survey of literature reveals that little attention has been paid for implementing such type impedance function multiplier topologies by employing VDTAs as active elements [20]-[21].

Considering these facts, in this chapter, an actively generalized impedance multiplier using VDTAs as active elements is introduced. This multiplying circuit comprises only two VDTAs and the scaling impedance. The proposed impedance multiplier circuit can provide electronic control to grounded impedance functions, i.e. resistor, capacitor and inductor, by means of transconductance gains of the VDTAs. The multiplier does not require critical active and passive component matching conditions and/or cancellation constraints for its realization. The non-ideal analysis and the sensitivity study of the proposed circuit are investigated in detail. Some simulation results are used to support the theoretical analysis.

3.2 Circuit Description

The configuration for realizing electronically tunable impedance multiplier is depicted in Figure 3.1. It uses only two VDTAs and one grounded scaling impedance. The use of grounded passive impedance makes the proposed circuit suitable for monolithic integrated circuit (IC). Using the VDTA relationship given in equation (2.1) and by doing routine circuit calculation, the input impedance (Z_{in}) of the proposed circuit in Figure 3.1 can be found as [Appendix B.1] :

$$Z_{in} = \frac{v_{in}}{i_{in}} = KZ_x \tag{3.1}$$

where
$$K = \frac{g_{mF2}g_{mS2}}{g_{mF1}g_{mS1}} \tag{3.2}$$

and g_{mFi} and g_{mSi} are the transconductance gains of the i-th VDTA (i = 1, 2). It is evident from equation (3.2) that the proposed circuit of Figure 3.1 simulates the Z_x-impedance multiplier with a multiplication factor K. Also note that the multiplication factor K is controlled electronically by the ratio of VDTA transconductance gains.

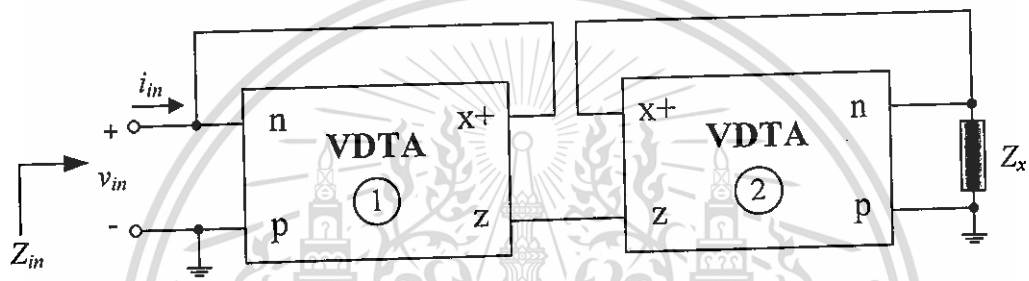

Figure 3.1 : Electronically tunable generalized impedance multiplier circuit with only two VDTAs.

In above expressions, if $Z_x = Z_{Lx} = sL_x$ is taken, then an inductance multiplier simulator can be obtained as :

$$Z_{in} = sKL_x = sL_{eq} \tag{3.3}$$

where the realized equivalent inductance value (L_{eq}) is found as:

$$L_{eq} = KL_x \tag{3.4}$$

On the other hand, if $Z_x = Z_{Cx} = 1/sC_x$ is chosen, equation (3.1) becomes :

$$Z_{in} = \frac{K}{sC_x} = \frac{1}{sC_{eq}} \tag{3.5}$$

Thus, the circuit of Figure 3.1 realizes the capacitance multiplier whose an equivalent value is given by :

$$C_{eq} = \frac{C_x}{K} \tag{3.6}$$

If $Z_x = Z_{Rx} = R_x$, the circuit simulates the resistance multiplier with the value of

$$R_{eq} = KR_x \tag{3.7}$$

From above expressions, it can be concluded that the realized L_{eq}, C_{eq} and R_{eq} can be tuned by means of the transconductances g_{mFi} and g_{mSi}.

3.3 Effect of Tracking Errors

In case of the non-ideal characteristic condition, the VDTA terminal relations from equation (2.2) is considered. Taking into account the VDTA non-ideality, an input impedance of the configuration in Figure 3.1 can be modified as [Appendix B.2] :

$$Z_{in} = \left(\frac{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}}{\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}} \right) Z_x \tag{3.8}$$

where β_{Fi} and β_{Si} are the transconductance tracking errors for the first and second stages (β_F and β_S) of the i-th VDTA (i = 1, 2), respectively.

Normalized active and passive sensitivities of Z_{in} are calculates as [Appendix B.3] :

$$S_{\beta_{F1}}^{Z_{in}} = S_{\beta_{S1}}^{Z_{in}} = -1 \tag{3.9}$$

$$S_{\beta_{F2}}^{Z_{in}} = S_{\beta_{S2}}^{Z_{in}} = 1 \tag{3.10}$$

and $$S_{Z_x}^{Z_{in}} = 1 \tag{3.11}$$

which are less than unity in magnitude. Therefore the proposed simulator of Figure 3.1 exhibits low active and passive sensitivities.

3.4 Performance Verification by Simulations

To confirm the results of the theoretical analysis discussed above, the proposed general impedance multiplication circuit of Figure 3.1 has been simulated with PSPICE program. For this purpose, The CMOS VDTA structure given in Figure 2.4 was realized in simulations using TSMC 0.35-μm CMOS technology. The aspect ratios of the MOS transistors are also based on Table 2.1. The supply voltages were chosen as : +V = -V = 1.5 V. The bias current I_B (= I_{BF} = I_{BS}) is given externally to control the transconductance parameter of the VDTA.

In case of the inductance multiplier, the circuit of Figure 3.1 was realized by taking the following active and passive components : g_{mFi} = g_{mSi} = 0.38 mA/V (I_{BFi} = I_{BSi} = 20 μA), and L_x = 0.1 mH. With these component values, the value of the realized equivalent inductance is L_{eq} = 0.1 mH. Figure 3.2 shows the simulated waveforms of the input voltage and current through the proposed inductance multiplier circuit of Figure 3.1, when a sinusoidal input voltage signal with 100 mV peak value at frequency f = 100 kHz was applied to the circuit. From the figure, it can be measured that the phase shift between the voltage (v_{in}) and current (i_{in}) approximately 88°, which corresponds to the theoretically predicted equal to 90°.

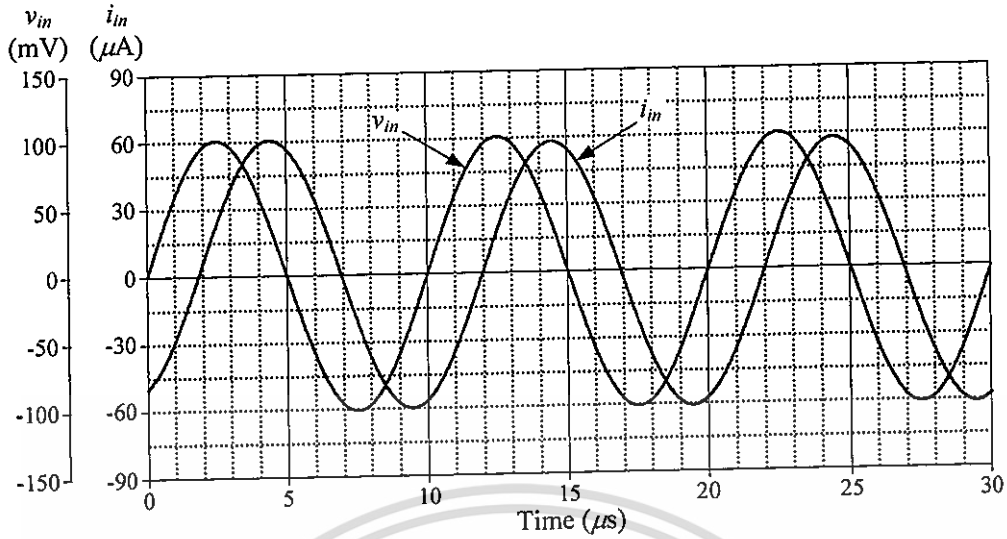

Figure 3.2 : Waveforms of input voltage and current for the realized inductance multiplier circuit of Figure 3.1.

In order to demonstrate the electronic tuning property of the grounded inductance multiplier circuit in Figure 3.1, the multiplication factor K was adjusted to the following values :

(i) $K = 0.1$ ($g_{mF1} = 0.38$ mA/V, $g_{mS1} = 0.95$ mA/V, $g_{mF2} = g_{mS2} = 0.19$ mA/V);

(ii) $K = 0.5$ ($g_{mF1} = 0.38$ mA/V, $g_{mS1} = 0.53$ mA/V, $g_{mF2} = g_{mS2} = 0.38$ mA/V);

(iii) $K = 1$ ($g_{mF1} = g_{mS1} = g_{mF2} = g_{mS2} = 0.38$ mA/V);

(iv) $K = 5$ ($g_{mF1} = g_{mS1} = g_{mF2} = 0.38$ mA/V, $g_{mS2} = 1.37$ mA/V);

(v) $K = 10$ ($g_{mF1} = g_{mS1} = 0.19$ mA/V, $g_{mF2} = 0.38$ mA/V, $g_{mS2} = 9.53$ mA/V).

The above settings lead to obtain the realized equivalent inductance value L_{eq} as : 0.01 mH, 0.05 mH, 0.1 mH, 0.5 mH and 1 mH, respectively. Figure 3.3 illustrates the corresponding impedance characteristics of the multiplier circuit in Figure 3.1 with respect to frequencies for five different values of K. As can be seen

from Figure 3.3, the impedances increase with the frequency and the proposed inductance multiplier circuit operates pretty well between 30 kHz and 10 MHz.

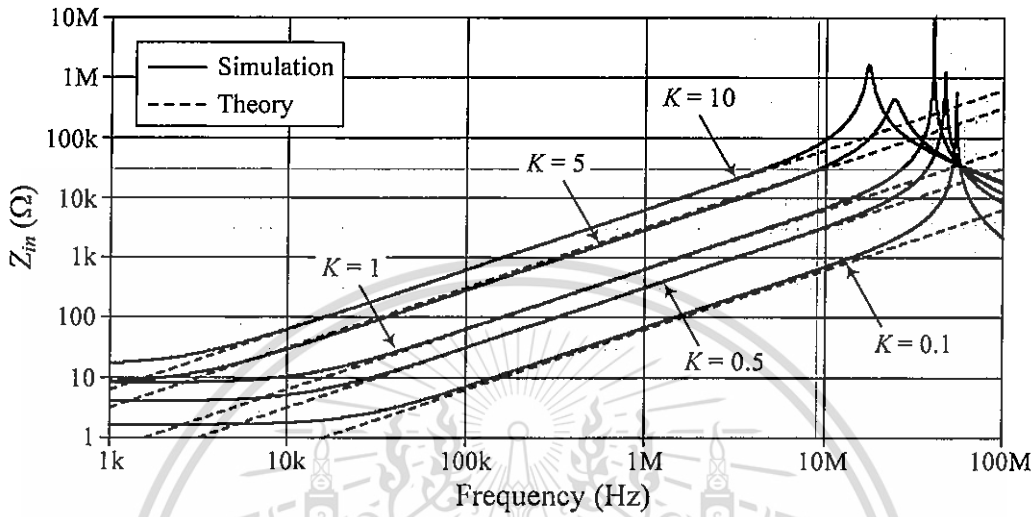

Figure 3.3 : Ideal and simulated impedance responses of the inductance multiplier circuit in Figure 3.1 for different values of the multiplication factor *K*.

To further evaluate the performance of the multiplier circuit shown in Figure 3.1, the grounded capacitance multiplier circuit is simulated with the following components : $g_{mFi} = g_{mSi} = 0.38$ mA/V and $C_x = 0.1$ nF. The simulated results of the time response analysis for i_{in} and v_{in} are given in Figure 3.4 with 100 mV (peak) sine wave at 100 kHz input. It can be observed that the realized impedance exhibits a positive 91° phase shifting as expected. In the same manner, the frequency responses of the proposed capacitance multiplier for five different values of *K*, are also shown in Figure 3.5. The simulations were done by varying $K = 0.1, 0.5, 1, 5, 10$ with the same component values setting as mentioned above. This results in the values of the

realized equivalent capacitance C_{eq} as : 1 nF, 0.2 nF, 0.1 nF, 0.02 nF and 0.01 nF, respectively. From Figure 3.5, we can see that the circuit operates correctly along the frequency range from 1 kHz to 400 kHz.

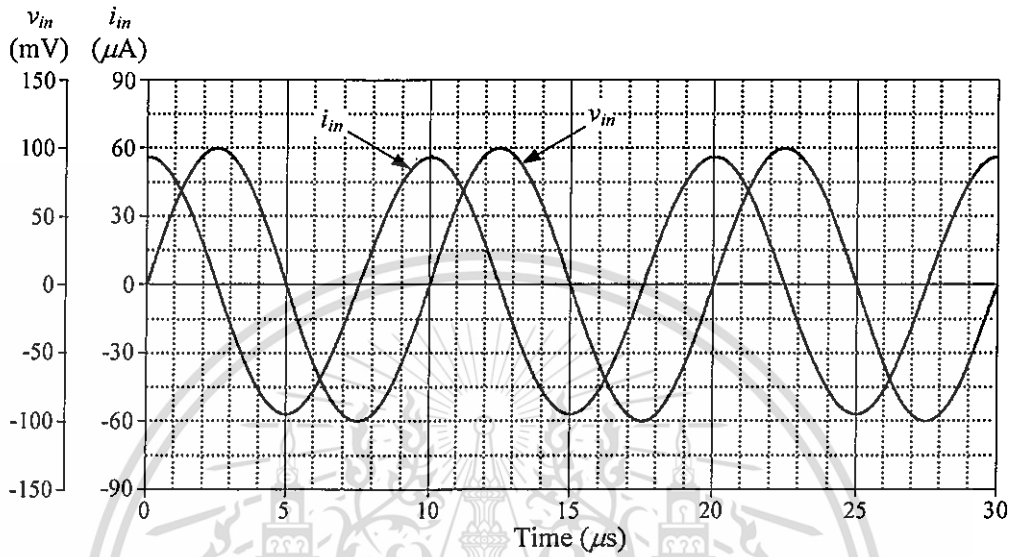

Figure 3.4 : Waveforms of input voltage and current for the realized capacitance multiplier circuit of Figure 3.1.

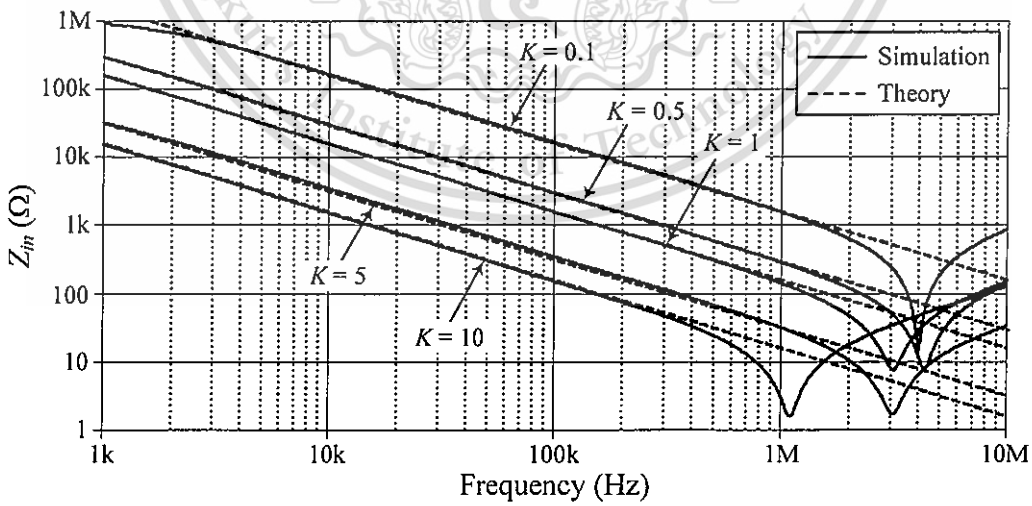

Figure 3.5 : Ideal and simulated impedance responses of the capacitance multiplier circuit in Figure 3.1 for different values of the multiplication factor K.

3.5 Sub-conclusion

This chapter has been presented the simple realization scheme of an electronically tunable impedance multiplier circuit based on VDTAs. The proposed impedance multiplier circuit is realizable by only two VDTAs and a single scaling impedance, thus results in a canonical structure and suitable for IC implementation. The simulated equivalent values of the presented impedances, namely L_{eq}, C_{eq} and R_{eq}, can be adjusted electronically via the biasing currents of the VDTAs. Simulation results based on TSMC 0.35-μm CMOS process parameters have been performed and the results well confirm the theoretical expectation.

3.6 References

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CHAPTER 4

Floating Inductance and Capacitance Simulators

4.1 Introduction

Floating inductance and capacitance simulator circuits are very useful active building blocks in many applications such as active filter design, sinusoidal oscillator design and cancellation of parasitic elements. This is due to the well-known fact that the use of the physical inductor and capacitor, particularly of large values, is either not permitted or is unwanted in the integrated circuit technology, because their characteristic are far from the ideal behavior, and it requires a large chip area. Although on chip inductors in spiral is a new research area, they still occupy a large chip area and have low quality factor (Q), and their values are very small, usually in order of 1 nH. Accordingly, to overcome these limitations, many circuits for the simulation of floating inductor and capacitors using various active elements have been introduced in the literature [1]-[16]. A survey of the literature shows that the floating simulator realizations in [1]-[16] still suffer from the following weakness :

(i) they require more than one active or one passive components for floating inductance simulation [1], [5]-[16];

(ii) they have either two of more active devices or more than one passive element for floating capacitance simulation [2]-[5], [7], [11], [13], [15]-[16];

(iii) they use some floating passive components [1]-[2], [4], [7]-[9], [14];

(iv) they employ any external passive resistors [1]-[2], [4], [7]-[9], [11], [13]-[15];

(v) they cannot be tuned electronically [1]-[2], [4], [6]-[9], [13]-[14].

In recent years, great emphasis has been placed on the use of new active elements in various analog active circuit designs, e.g., amplifiers, oscillators, filters or more generally, analog signal processing circuits [17]. The voltage differencing transconductance amplifier (VDTA) is a recently introduced active element. This element is composed of the current source controlled by the difference of two input voltages and a multiple-output transconductance amplifier, providing electronic tuning ability through its transconductance gains. Therefore, the VDTA device is very suitable for electronically tunable active circuit synthesis. Another advantageous feature of the use of the VDTA as an active element is that compact structures in some applications can be achieved easily [18]-[23]. All these advantages make the VDTA an alternative choice for the implementation of voltage-mode analog signal processing circuits.

In this chapter, two novel topologies for realizing a floating inductor and a floating capacitor employing VDTA as a novel active element are discussed. The proposed inductor is generated with only one VDTA and one grounded capacitor, while the proposed capacitor is generated with two VDTAs and one grounded capacitor. Both of the floating simulators can be tuned electronically through the transconductance parameter of the VDTA. They also do not require any realization

conditions. Since the circuits are composed of only grounded capacitor without requiring any external passive resistor, they are canonical structures and quite suitable for fully integrated circuit design [24]. Some applications together with the simulation results are also given to illustrate the performance of the proposed floating simulator circuits.

4.2 Description of the VDTA-based Floating Inductance Simulator

The proposed floating inductance simulator circuit is shown in Figure 4.1. It is composed of one VDTA and one grounded capacitor, without needing an external passive resistor. Straightforward analysis of the floating inductor in Figure 4.1 yields the following short-circuit admittance matrix [Appendix C.1] :

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \frac{g_{mF} g_{mS}}{sC_1} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{4.1}$$

or we can obtain the following input impedance :

$$Z_{in} = s\left(\frac{C_1}{g_{mF} g_{mS}}\right) = sL_{eq} \tag{4.2}$$

It is clearly seen from above expression that the circuit of Figure 4.1 can simulate a floating inductor with an equivalent inductance value $L_{eq} = C_1/g_{mF}g_{mS}$. Also note that the value of L_{eq} can be adjusted electronically through either g_{mF} or g_{mS} of the VDTA. In addition, if we let $v_1 = 0$ or $v_2 = 0$, then the proposed circuit can be used as a grounded inductor.

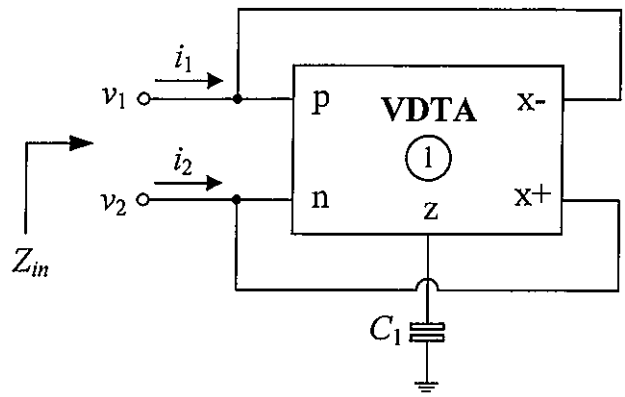

Figure 4.1 : VDTA-based floating inductance simulator circuit.

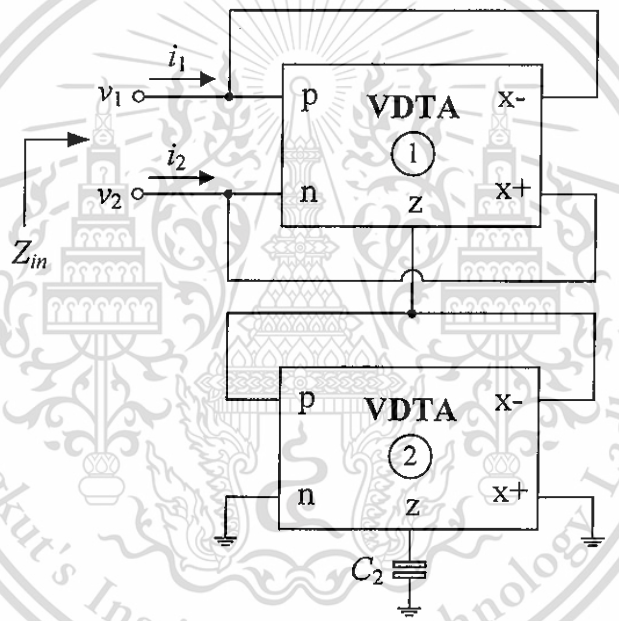

Figure 4.2 : VDTA-based floating capacitance simulator circuit.

4.3 Description of the VDTA-based Floating Capacitance Simulator

Figure 4.2 shows the proposed floating capacitance simulator circuit. It should be noted that the structure in Figure 4.2 is obtained from Figure 4.1 by replacing the capacitor C_1 with the circuit of Figure 4.1. Therefore, an input impedance of the circuit can be given by [Appendix C.2] :

$$Z_{in} = \frac{g_{mF2}g_{mS2}}{sC_2 g_{mF1}g_{mS1}} = \frac{1}{sC_{eq}} \tag{4.3}$$

Here, the parameters g_{mFi} and g_{mSi} represent the transconductances g_{mF} and g_{mS} of i-th VDTA (i = 1, 2), respectively. One can see from equation (4.3) that the circuit shown in Figure 4.2 realizes a floating capacitor whose the simulated equivalent capacitance is found as : $C_{eq} = C_2 g_{mF1}g_{mS1}/g_{mF2}g_{mS2}$.

4.4 Analyses of Non-Ideal and Parasitic Effects

In this section, the non-ideal performance and the effect of parasitic elements are examined. It may be useful to discuss the VDTA non-ideality in the following subsections.

4.4.1 Non-Ideal Gain Effects

To evaluate the effects of the non-ideal gains at high frequencies, we first assume that frequency-dependent transconductance gains of the VDTA can each be described using a single-pole model as follows [25] :

$$g_{mF}(s) = \frac{g_{mF0}}{1 + s\tau_F} \tag{4.4}$$

and

$$g_{mS}(s) = \frac{g_{mS0}}{1 + s\tau_S} \tag{4.5}$$

where g_{mF0} and g_{mS0} are the transconductance gains at low frequencies, $\omega_F = 1/\tau_F$ and $\omega_S = 1/\tau_S$ are the corresponding pole frequencies. In general, the values of these poles will depend on practical implementation of the VDTA. Combining equations (4.2)-

(4.5), the frequency-dependent input impedances of the floating simulator circuits in Figures 4.1 and 4.2 can be re-written, respectively, as follows [Appendix C.3] :

$$Z_{in} = \left(\frac{sC_1}{g_{mF0}g_{mS0}}\right)\left[\frac{(s+\omega_F)(s+\omega_S)}{\omega_F\omega_S}\right] \tag{4.6}$$

and

$$Z_{in} = \left(\frac{g_{mF10}g_{mS10}}{sC_2g_{mF20}g_{mS20}}\right)\left(\frac{\omega_{F1}\omega_{S1}}{\omega_{F2}\omega_{S2}}\right)\left[\frac{(s+\omega_{F2})(s+\omega_{S2})}{(s+\omega_{F1})(s+\omega_{S1})}\right] \tag{4.7}$$

The above expressions illustrate that the useful operating-frequency regions of the proposed floating impedance simulators in Figures 4.1 and 4.2 can respectively be defined as [26] :

$$\omega << \min\{\omega_F, \omega_S\} \tag{4.8}$$

and

$$\omega << \min\{\omega_{F1}, \omega_{S1}, \omega_{F2}, \omega_{S2}\} \tag{4.9}$$

It is also considered from equation (4.7) that if $\omega_{F1} \cong \omega_{F2}$ and $\omega_{S1} \cong \omega_{S2}$, then the effects of these parasitic poles can be ignored.

4.4.2 Parasitic Element Effects

Furthermore, parasitic impedances appearing at terminals of VDTA are analyses. In order to consider these parasitic impedances, the non-ideal equivalent circuit shown in Figure 2.2 can be used. Ideally, the parasitic resistances R_p, R_n, R_z and R_x appearing in parallel, respectively, at corresponding terminals p, n, z and x are approximately equal to infinity, and parasitic capacitances C_p, C_n, C_z and C_x approximately equal to zero. Consider the simulator circuits in Figures 4.1 and 4.2 including parasitic elements given in Figure 2.2. We see that the z-terminals of the VDTA in both circuits are terminated by grounded capacitors C_1 and C_2; hence, these

capacitors appear in parallel with the z-terminal parasitic ($R_z//C_z$). However, since the external capacitors C_1 and C_2 chosen in design are usually in excess to the expected parasitic capacitance C_z (C_1, C_2 >> C_z), this effect can be absorbed at working frequencies. Therefore, the parasitic effect is not noticeable if the values of C_1 and C_2 are chosen as :

$$\left(\frac{1}{sC_1}\right),\left(\frac{1}{sC_2}\right) << R_Z \tag{4.10}$$

4.5 Simulation Results and Discussions

The behaviors of the electronically tunable resistorless floating inductor and capacitor in Figures 4.1 and 4.2 have been demonstrated by PSPICE simulation. The simulations were performed by using a CMOS realization as shown in Figure 2.4 with DC supply voltages equal to ±1.5V. The CMOS transistors in VDTA implementation were simulated using 0.35-μm TSMC CMOS technology process parameters, where the dimensions of MOS transistors are given in Table 2.1. In all cases, the floating simulator circuits given in Figure 4.1 and 4.2 were simulated with $C_1 = C_2 = 1$ nF.

For the floating inductance simulator of Figure 4.1, the VDTA's transconductances were varied as : $g_m = g_{mF} = g_{mS} \cong 0.27$ mA/V ($I_B = I_{BF} = I_{BS} = 20$ μA), $g_m \cong 0.54$ mA/V ($I_B = 80$ μA) and $g_m \cong 0.81$ mA/V ($I_B = 180$ μA) for simulating $L_{eq} = 13.74$ mH, 3.43 mH, 1.52 mH, respectively.

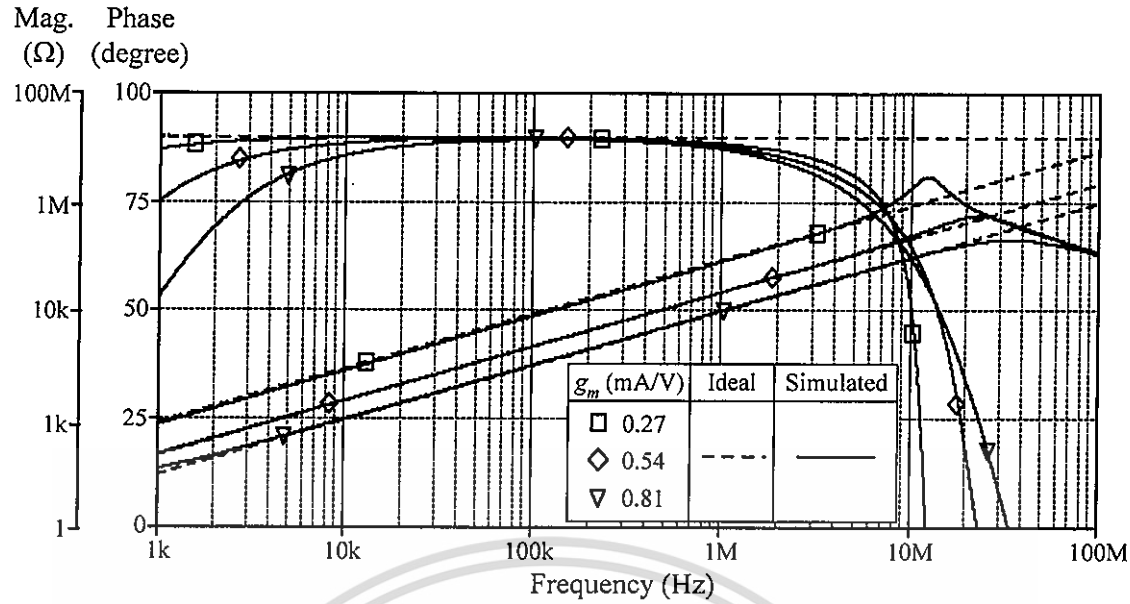

Figure 4.3 : Ideal and simulated frequency responses of the floating inductance simulator in Figure 4.1.

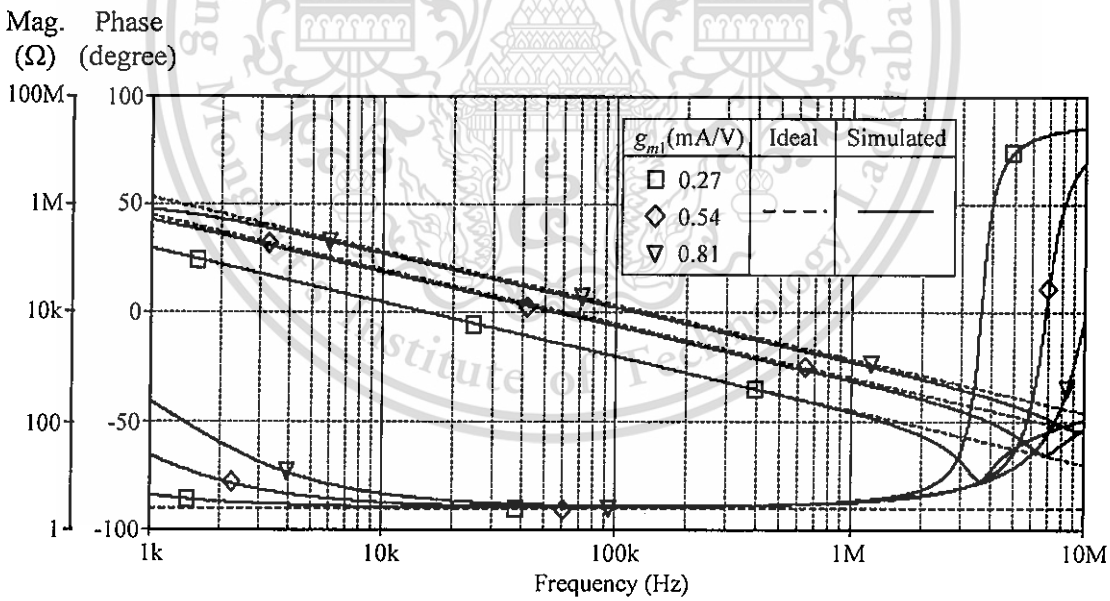

Figure 4.4 : Ideal and simulated frequency responses of the floating capacitance simulator in Figure 4.2.

Likewise, for the floating capacitance simulator of Figure 4.2, the transconductance values were selected as : $g_{m2} = g_{mF2} = g_{mS2} \cong 0.27$ mA/V, and $g_{m1} = g_{mF1} = g_{mS1} \cong 0.27$ mA/V, 0.54 mA/V and 0.81 mA/V, which results in : $C_{eq} = 1$ nF, 0.25 nF, 0.11 nF, respectively. The impedances of the simulator circuits of Figures 4.1 and 4.2 relative to frequency are also shown in Figures 4.3 and 4.4, respectively. It appears from both figures that the ideal and simulated magnitude and phase responses are in good agreement for a set of selected values.

4.6 Applications to Active Filter Realizations

As an example to demonstrate the performance of the derived inductance simulator of Figure 4.1, the fifth-order lowpass Butterworth filter shown in Figure 4.5 was designed with the de-normalized cut-off frequency of $f_c = \omega_c/2\pi = 300$ kHz.. The circuit was simulated with the ideal inductor and our proposed floating inductor. For this purpose, the component values of the proposed floating inductor in Figure 4.1 were taken as follows : $g_m \cong 0.27$ mA/V, $C_1 = 1$ pF for $L_{eq1} = L_{eq5} \cong 13.7$ μH, and $g_m \cong 0.15$ mA/V, $C_1 = 1$ pF for $L_{eq3} \cong 44.5$ μH. The theoretical and simulation results for the filter of Figure 4.5 are given in Figure 4.6.

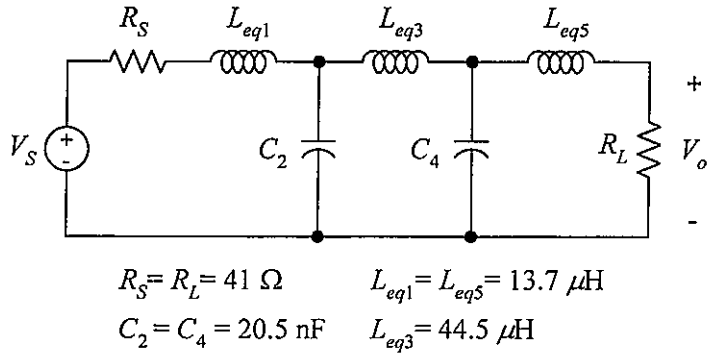

Figure 4.5 : Fifth-order lowpass Butterworth filter with f_C = 300 kHz.

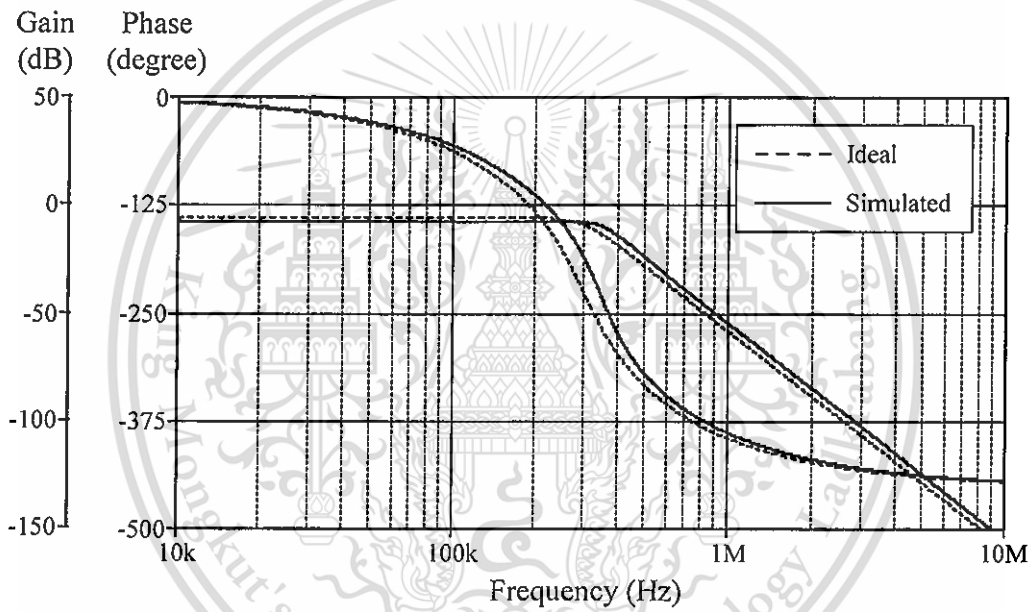

Figure 4.6 : Ideal and simulation results obtained from the filter of Figure 4.5.

Furthermore, to demonstrate an application of the realized floating capacitor of Figure 4.2, it is employed in the RLC bandpass filter as shown in Figure 4.7. The floating capacitor circuit is simulated with the following component values : C_2 = 1 nF and $g_{mF1} = g_{mS1} = g_{mF2} = g_{mS2} \cong 0.27$ mA/V ($I_{BF1} = I_{BS1} = I_{BF2} = I_{BS2} = 20\ \mu$A), which results in C_{eq}= 1 nF. Figure 4.8 shows the frequency responses of the bandpass

filter of Figure 4.7, which appears that the ideal and simulated magnitude and phase responses are in good agreement for a set of selected values over several decades.

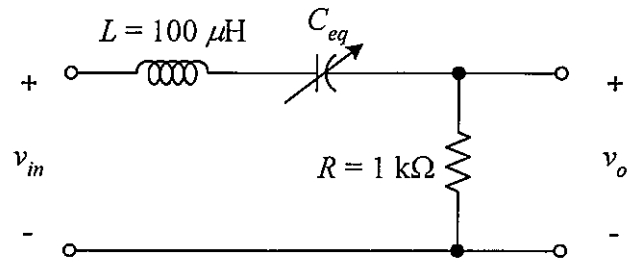

Figure 4.7 : RLC bandpass filter.

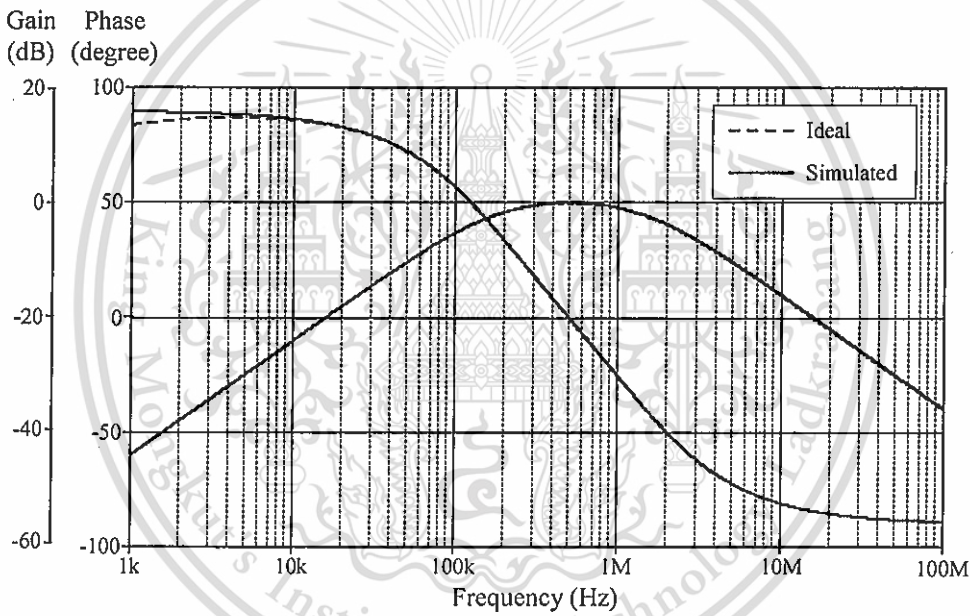

Figure 4.8 : Ideal and simulated frequency responses of Figure 4.7.

Moreover, in order to demonstrate the electronic controllability of the proposed floating capacitor, the value of C_{eq} in Figure 4.7 was adjusted to 1 nF, 0.25 nF and 0.11 nF, by changing $g_{mF1} = g_{mS1} \cong 0.27$ mA/V, 0.54 mA/V and 0.81 mA/V, respectively, while keeping $g_{mF2} = g_{mS2}$ constant at 0.27 mA/V. This tuning leads to

obtain the center frequency $f_c \cong 0.5$ MHz, 1 MHz and 1.5 MHz, respectively. The simulated magnitude responses of the bandpass filter in Figure 4.7 with electronically variable C_{eq} are depicted in Figure 4.9. From the results, the corresponding f_c are obtained as : 0.49 MHz, 0.94 MHz and 1.39 MHz, respectively.

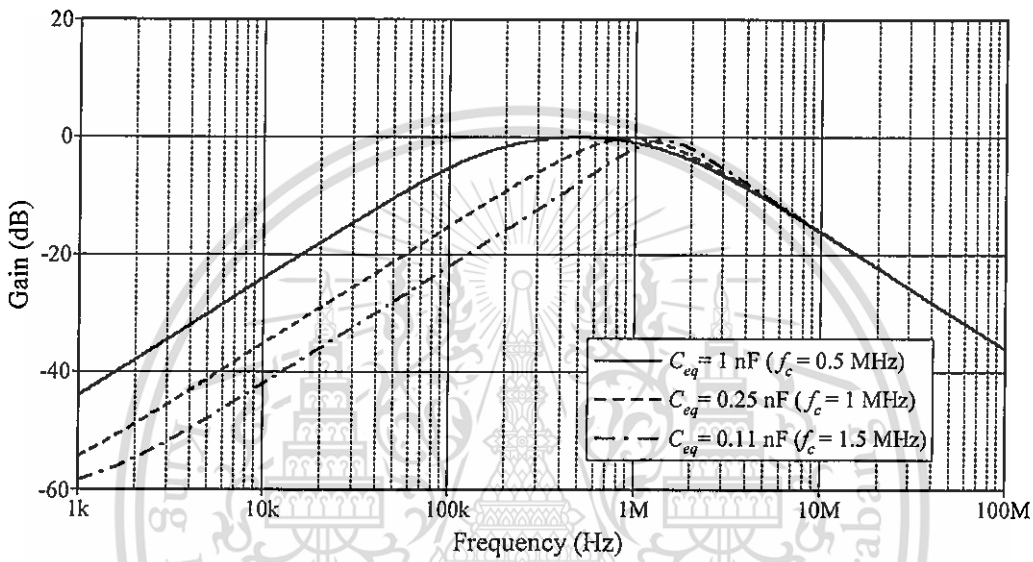

Figure 4.9 : Simulated magnitude responses of Figure 4.7 with electronically variable C_{eq}.

4.7 Sub-conclusion

In summary, floating inductance and capacitance simulation schemes have been described in this chapter. They are realized using only a single VDTA for inductance simulation and needing two VDTAs for capacitance simulation. Both of the simulators employ only a grounded capacitor, which is suitable for integrated circuit implementation. The values of the simulated inductance and capacitance are tunable

by adjusting the bias current of the VDTA. The usefulness of the introduced simulator circuits is demonstrated on the filter design examples.

4.8 References

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CHAPTER 5

Simulation of Frequency-Dependent Negative Resistance

5.1 Introduction

Frequency-Dependent Negative Resistances (FDNRs) are very useful elements for the design and synthesis active filter. Also, FDNR can be used in applications of using floating inductance [1]. Several FDNR implementations using various active devices were proposed in literature [2]-[9]. However, the works in [2]-[8] require at least three passive components and most of them are floating. In [9], at least four active components were realized. As mentioned earlier in the previous chapter, the voltage differencing transconductance amplifier (VDTA) has been introduced in [10] as an alternative active building block for implementing analog signal processing circuits. This element is composed of the current source controlled by the difference of two input voltages and a multiple-output transconductance amplifier, providing electronic tuning ability through its transconductance gains. This means that the VDTA device is very suitable for electronically tunable active circuit synthesis. Another advantageous feature of the use of the VDTA as an active element is that compact structures in some applications can be achieved easily [11]-[15].

Considering this fact, the objective of this chapter is to present an alternative approach of the floating FDNR simulator topology. The realized FDNR consists of three VDTAs and two grounded capacitors; accordingly, it is suitable for integrated

circuit (IC) implementation point of view [16]. The D-element value of the simulated FDNR circuit can be tuned electronically tunable through the transconductance parameters of the VDTAs. As application examples, the designs of fourth-order Butterworth bandpass and lowpass filters based on the use of the proposed FDNR simulator have been demonstrated. Computer simulations are also performed to show the characteristics of the simulator circuit, and to verify the mathematical analyses.

5.2 Proposed Floating FDNR Simulator Circuit

Figure 5.1 shows the proposed floating FDNR simulator circuit. This simulation contains only three VDTAs and two grounded that is beneficial from the fabrication point of view. The admittance matrix for the configuration of Figure 5.1 can be derived as the following expression [Appendix D] :

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \frac{s^2 C_1 C_2 g_{mF1} g_{mS1}}{g_{mF2} g_{mF3} g_{mS3}} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}, \tag{5.1}$$

or the input admittance of the simulator is realized as :

$$Y_{in} = s^2 \left(\frac{C_1 C_2 g_{mF1} g_{mS1}}{g_{mF2} g_{mF3} g_{mS3}} \right) = s^2 D_{eq} \tag{5.2}$$

Equation (5.2) reveals that the circuit of Figure 5.1 realizes a floating FDNR with an equivalent *D*-element (D_{eq}) given by:

$$D_{eq} = \left(\frac{C_1 C_2 g_{mF1} g_{mS1}}{g_{mF2} g_{mF3} g_{mS3}} \right) \tag{5.3}$$

From equation (5.3), it is easy to see that the D_{eq}-value of the FDNR can be tuned by electronic means through either g_{mF} or g_{mS} of the VDTAs. In addition, if we let $v_1 = 0$ or $v_2 = 0$, then the tunable grounded FDNR can easily be realized.

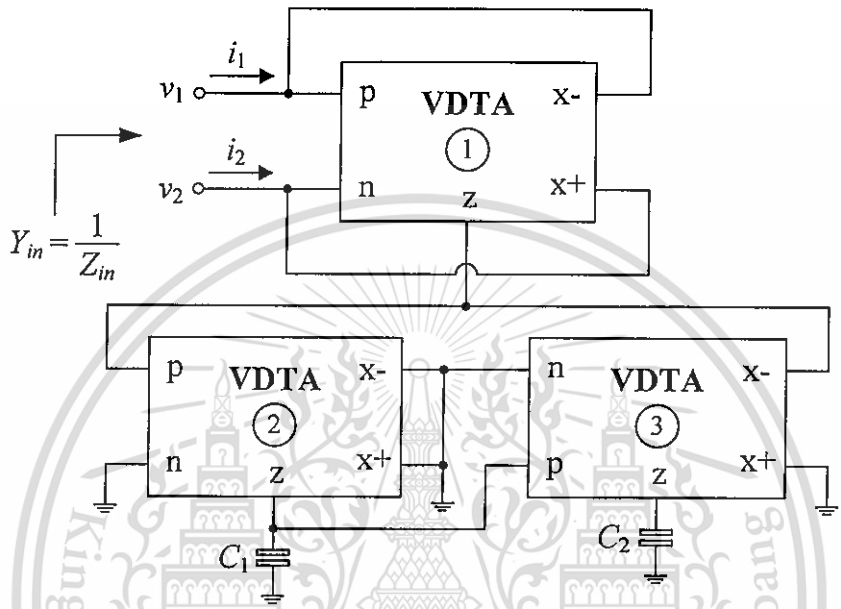


Figure 5.1 : Proposed VDTA-based floating FDNR simulator circuit.

5.3 Simulation Results and Performance Verification

In order to evaluate the behavior of the simulator circuit in Figure 5.1, the computer simulation with PSPICE program has been performed. In simulations, the VDTA was performed by the schematic CMOS implementation given in Figure 2.4 with supply voltages +V = -V= 1.5 V. The CMOS transistors in VDTA implementation were simulated the 0.35-μm CMOS technology extraced from TSMC company. The dimensions of MOS transistors are given in Table 2.1.

As an example, the component values were chosen as : $C_1 = C_2 = 1$ nF, $g_{mF1} = g_{mS1} = g_{mF2} = g_{mS2} \cong 0.60$ mA/V ($I_{BF1} = I_{BS1} = I_{BF2} = I_{BS2} = 100$ μA), and $g_{mF3} = g_{mS3} \cong 0.77$ mA/V ($I_{BF3} = I_{BS3} = 200$ μA), which results in $D_{eq} = 1$ fFs. Figure 5.2(a) shows the frequency response of the impedance of the proposed floating FDNR simulator circuit in Figure 5.1 relative to frequency. It can be observed that the circuit operates pretty well between 20 kHz and 2 MHz. To further demonstrate the electronic tunability of the proposed FDNR, the simulator was also simulated by varying $g_{mF3} = g_{mS3} \cong 0.77$ mA/V, 0.93 mA/V and 1 mA/V, to obtain $D_{eq} = 1.00$ fFs, 0.66 fFs, and 0.50 fFs, respectively. The frequency characteristics of the inductance simulator for various g_{mF3} values are shown in Figure 5.2(b). As depicted in Figure 5.2, the simulation results are in close agreement with the prediction, and confirm that the value of D_{eq} can be adjusted electronically by the transconductance gain of the VDTA.

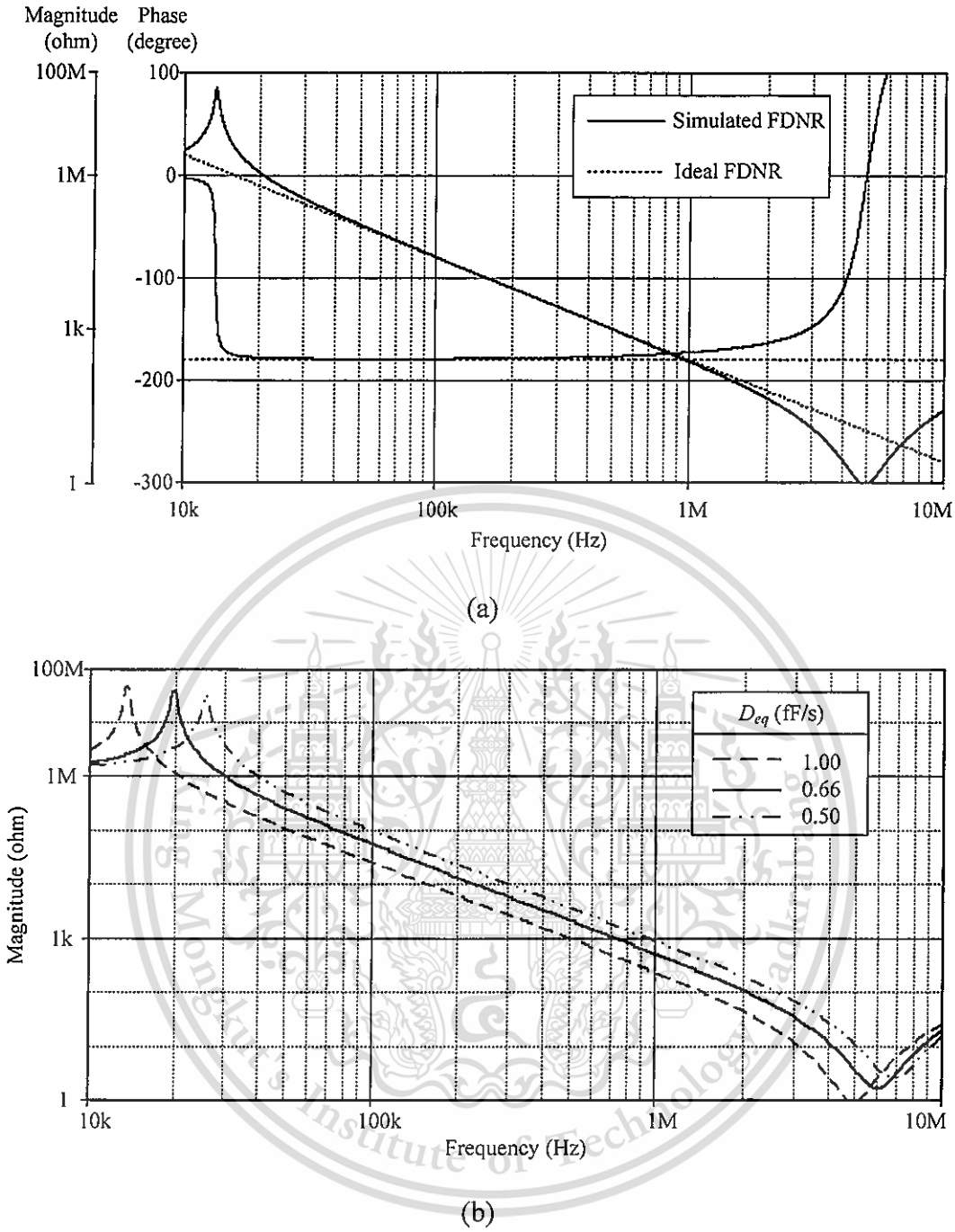
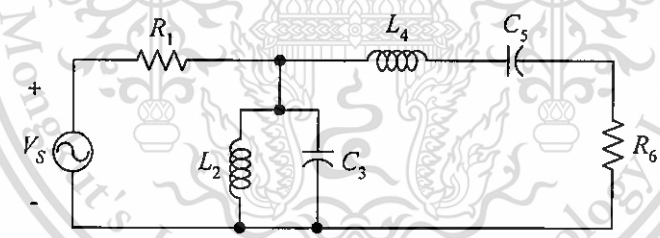


Figure 5.2 : Simulated frequency responses of impedance of the tunable floating FDNR simulator circuit in Figure 5.1.

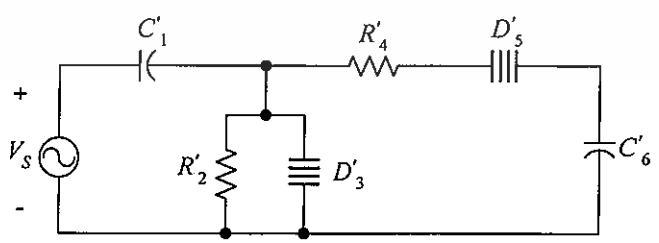
(a) magnitude and phase characteristics (b) electronic tuning of the D_{eq}-value.

5.4 Application Examples

In this section, the realized floating FDNR simulator in Figure 5.1 is used in the RLC fourth-order Butterworth bandpass filter prototype shown in Figure 5.3(a), where $R_1 = R_6 = 1\ \Omega$, $L_2 = 0.225\ \mu$H, $C_3 = 1.225\ \mu$F, $L_4 = 11.25\ \mu$H, $C_5 = 22.5$ nF [17]. This filter is designed to obtain fourth-order Butterworth characteristic whose bandwidth and center frequency are $BW = 32$ kHz and $f_c = 316$ kHz respectively. By applying Bruton transformation [18] and using magnitude scaling constant ($k_m = 10^9$) and variable impedance scaling method, i.e. dividing the impedance of each element in the Figure 5.3(a) by k_m, the *RLC* passive filter is converted into *CRD* filter as shown in Figure 5.3(b) where all FDNRs are realized using the realized FDNR circuit of Figure 5.1.



(a)



(b)

Figure 5.3 : Fourth-order Butterworth bandpass filter.

(a) RLC passive prototype (b) equivalent CDR circuit with FDNRs.

In Figure 5.3(b), the resulting circuit components are obtained as : C'_1 = 1 nF, R'_2 = 225 Ω, D'_3 = 11.25 fFs, R'_4 = 11.25 kΩ, D'_5 = 11.25 aFs, and C'_6 = 1 nF. According to these component values, the voltage transfer function of the bandpass filter in Figure 5.3(b) is given by :

$$H(s) = \frac{(4.043\times10^{10})s^2}{s^4 + (2.843\times10^{5})s^3 + (7.925\times10^{12})s^2 + (1.121\times10^{18})s + (1.554\times10^{25})} \quad (5.4)$$

The magnitude and phase characteristics of the filters are shown in Figure 5.4(a) and 5.4(b), respectively. From the figures, it appears that the theoretical and simulated results are in good agreement.

To illustrate another application of the proposed FDNR simulator, a fourth-order Butterworth lowpass filter shown in Figure 5.5(a) was designed and simulated. In Figure 5.5(a), the normalized component values are $R_S = R_L$ = 1 Ω, L_1 = 0.7654 H, C_2 = 1.848 F, L_3 = 1.848 H and C_4 = 0.7654 F [19]. By applying Bruton transformation [18] and selecting $k_m = 1.59 \times 10^3$ and frequency scaling constant k_f = 628.32×10^3, the prototype RLC passive filter in Figure 5.5(a) can be transformed to the CRD filter as shown in Figure 5.5(b) where the elements D'_2 and D'_4 were constructed using the proposed FDNR simulator circuit in Figure 5.1. As a result, the de-normalized component values of Figure 5.5(b) were obtained as : $C_S = C_L$ = 1 nF, R'_1 = 1.22 kΩ, D'_2 = 2.94 fFs, R'_3 = 2.94 kΩ and D'_4 = 1.22 fFs. The simulated gain and phase characteristics of the fourth-order Butterworth lowpass filters in Figure 5.5(b) are displayed in Figures 5.6(a) and 5.6(b), respectively.

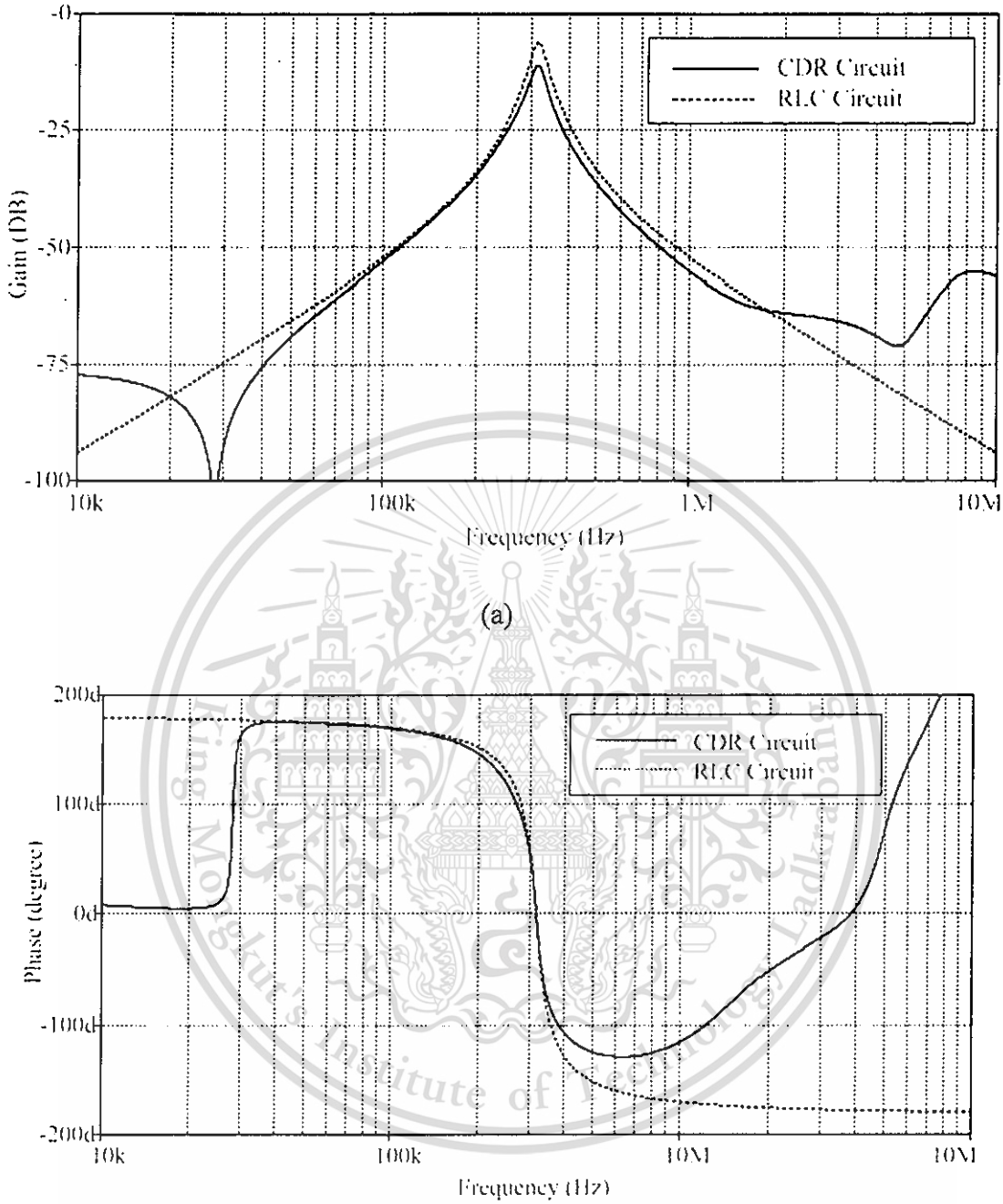


Figure 5.4 : Simulated frequency characteristic of the filter in Figure 5.3(b).

(a) gain responses (b) phase responses

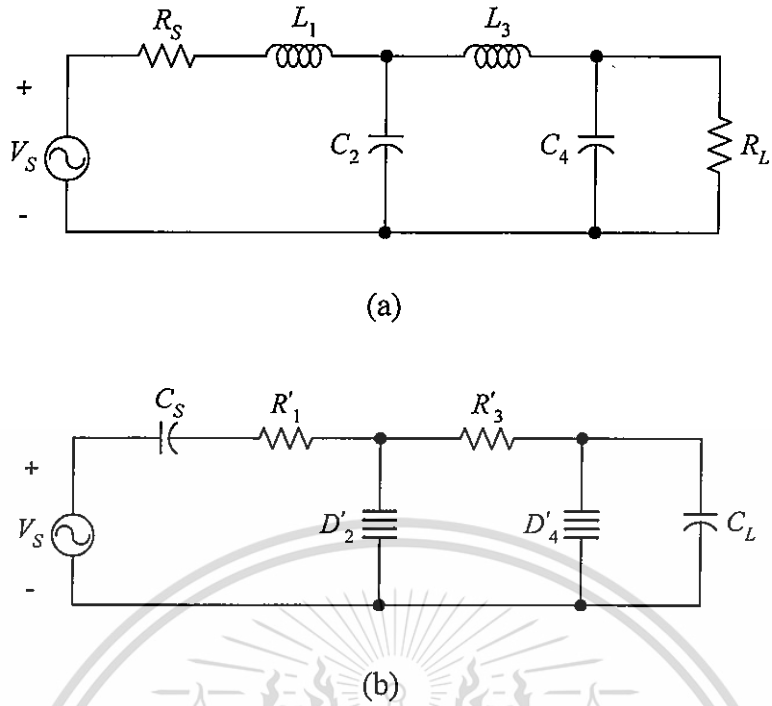
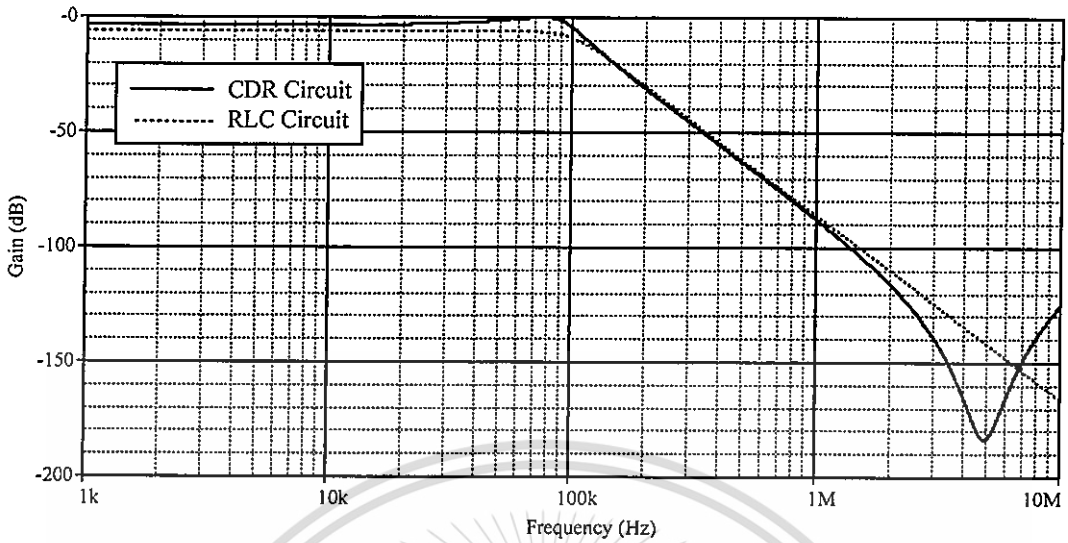


Figure 5.5 : Fourth-order Butterworth lowpass filter.

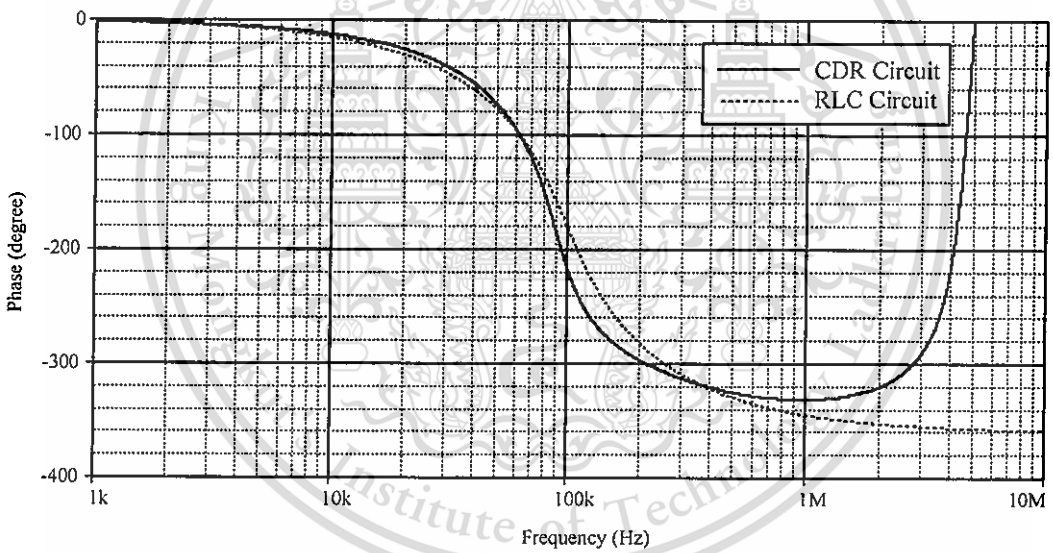
(a) RLC passive prototype (b) equivalent CDR circuit with FDNRs

5.5 Sub-conclusion

This chapter describes an electronically tunable floating FDNR simulator circuit based on the use of the voltage differencing transconductance amplifier (VDTA) and only two grounded capacitor. The important gain of floating FDNR simulator is that its value can be adjusted electronically by changing bias currents of the VDTAs. To demonstrate the performance of the proposed circuit, it is used to construct fourth-order Butterworth bandpass and lowpass filters. PSPICE simulation results verify that the performances of the proposed circuit and its applications are in good agreement with the prediction of the analysis performed.



(a)



(b)

Figure 5.6 : Simulated frequency characteristic of the filter in Figure 5.5(b).

(a) gain responses (b) phase responses

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CHAPTER 6

Conclusions and Suggestions

6.1 Conclusions and Discussions

In conclusion, the main contribution of this dissertation is the design and synthesis of floating immittance function simulator with electronically controllable property. A recently introduced active building block, namely voltage differencing transconductance amplifier (VDTA) has been employed to implement various actively simulated immittances, such as impedance multiplication, inductance and capacitance simulations, as well as frequency-dependent negative resistance (FDNR). The key performances of the developed floating immittance function simulators are the gain adjustment flexibility with the help of electronically controlled transconductance parameters of the VDTA. With respect to the design, all the simulated active circuits requires minimum passive components, all of which are grounded. Some illustrative applications on the continuous-time filter constructed with the realized simulator circuits were also discussed and investigated. The feasibility of all simulators developed in this thesis is verified with PSPICE simulations using TSMC 0.35-μm CMOS real process parameters. The comparison with the theoretical expectation demonstrates that the proposed ones have some advantageous features over available literature.

Here, it is worth mentioned that the important results of this work have already published in international journals with ISI impact factor (2 papers in the following journals) :

- W. Tangsrirat and **S. Unhavanich**, "Voltage differencing transconductance amplifier-based floating simulators with a single grounded capacitor", **Indian Journal of Pure & Applied Physics**, vol.52, no.6, pp.423-428, 2014 (Impact Factor 2012 = 0.854). [1]

- W. Tangsrirat and **S. Unhavanich**, "Signal flow graph realization of single-input five-output current-mode universal biquad using current follower transconductance amplifiers", Revue Roumaine Des Sciences Techniques, vol.59, no.2, pp.183-191, 2014 (Impact Factor 2012 = 0.337). [2]

and presented at international conferences (4 papers in the following conferences) :

- **S. Unhavanich**, P. Mongkolwai and W. Tangsrirat, "Simulation of frequency-dependent negative resistance (FDNR) using voltage differencing transconductance amplifiers (VDTAs)", **Proceedings of Annual Conference on Engineering and Information Technology (ACEAIT-2015)**, Osaka, Japan, 22-24 March, pp.489-496, 2015. [3]

- **S. Unhavanich**, O. Onjan and W. Tangsrirat, "Tunable capacitance multiplier with a single voltage differencing buffered amplifier", **Proceedings of the International MultiConference of Engineers and Computer Scientists 2016 (IMECS 2016)**, Vol II, 16-18 March, Hong Kong, pp.568-571, 2016. [4]

- O. Onjan, **S. Unhavanich** and W. Tangsrirat, "SFG actualization of general n^{th}-order voltage transfer functions using VDBAs", **Proceedings of the International MultiConference of Engineers and Computer Scientists 2016 (IMECS 2016)**, Vol II, 16-18 March, Hong Kong, pp.585-589, 2016. [5]

- W. Tangsrirat, T. Pukkalanun, **S. Unhavanich**, "Simple realization of BiCMOS current-controlled conveyor transconductance amplifier (CCCTA)", **Proceedings of Annual Conference on Engineering and Information Technology (ACEAIT-2014)**, 28-30 March, Tokyo, Japan, pp.1244-1250, 2014. [6]

All the published papers can be found in Appendix E.

6.2 Suggestions for Future Work

With respect to the above discussion, the author believes that there is always room for future work and domains for more exploration. According to the work, interesting topics for future study can be, which may facilitate further work.

As previously discussed in section 2.3.2, the output resistance of the VDTA structure given in Figure 2.4 is not enough high for some given signal processing applications. This is mainly caused by the performance of the traditional floating current source (FCS) stage used for realizing the g_m-cell of the VDTA. Therefore, a simple suggestion one is, of course, that the performance improvement of the FCS should be further developed and investigated in order to increase the output resistance value of the VDTA.

Another drawback of the VDTA using two Arbel-Goldminz transconductors is that the output voltage swing is restricted at about $V_{DS(sat)}$. Therefore, a suggestion for further work may be to go for the design of this circuit with a modified architecture so that the whole structure becomes high-output voltage swing.

For the proposed floating FDNR of Figure 5.1, we found that the configuration was constructed with three VDTAs, which significantly requires a large chip area and a high-power consumption in case of integration. Thus, a challenging question for the further study is that how we can reduce the number of VDTAs without losing the features of the VDTA-based FDNR realization. As a result, the circuit can reduce hardware and power consumption. It is also advantageous in terms of saving chip area from the point of view of integrated circuit implementation.

6.3 References

[1] W. Tangsrirat and S. Unhavanich, "Voltage differencing transconductance amplifier-based floating simulators with a single grounded capacitor", **Indian Journal of Pure & Applied Physics,** vol.52, no.6, pp.423-428, 2014.

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APPENDIX A

SPICE Model Parameters

TSMC 0.35 μm n-well CMOS Real Process

TSMC (Taiwan Semiconductor Manufacturing Company, Ltd.)

NMOS TRANSISTOR

```
*
.MODEL      CMOSN_TSMC35    NMOS    LEVEL=3
+TOX=7.9E-9     NSUB=1E17     GAMMA=0.5827871
+PHI=0.7      VTO=0.5445549      DELTA=0
+UO=436.256147     ETA=0     THETA=0.1749684
+KN=2.055786E-4     VMAX=8.309444E4     KAPPA=0.2574081
+RSH=0.0559398      NFS=1E12     TPG=1
+XJ=3E-7       LD=3.162278E-11      WD=7.046724E-8
+CGDO=2.82E-10     CGSO=2.82E-10       CGBO=1E-10
+CJ=1E-3       PB=0.9758533          MJ=0.3448504
+CJSW=3.777852E-10      MJSW=0.3508721
*
```

PMOS TRANSISTOR

```
*

.MODEL    CMOSP_TSMC35    PMOS    LEVEL=3

+TOX=7.9E-9    NSUB=1E17    GAMMA=0.4083894

+PHI=0.7    VTO=-0.7140674    DELTA=0

+UO=212.2319801    ETA=9.999762E-4    THETA=0.2020774

+KP=6.733755E-5    VMAX=1.181551E5    KAPPA=1.5

+RSH=30.0712458    NFS=1E12    TPG=-1

+XJ=2E-7    LD=5.000001E-13    WD=1.249872E-7

+CGDO=3.09E-10    CGSO=3.09E-10    CGBO=1E-10

+CJ=1.419508E-3    PB=0.8152753    MJ=0.5

+CJSW=4.813504E-10    MJSW=0.5

*
```

APPENDIX B

Performance Analysis for the Generalized Tunable Impedance Multiplier of Figure 3.1

B.1 Derivation for the Input Impedance (Z_{in})

By superimposing all the signal currents on the corresponding terminals of the tunable impedance multiplier in Figure 3.1, the configuration can be redrawn as illustrated in Figure B.1. Therefore, the derivation of the small signal input impedance (Z_{in}) of this circuit is given below.

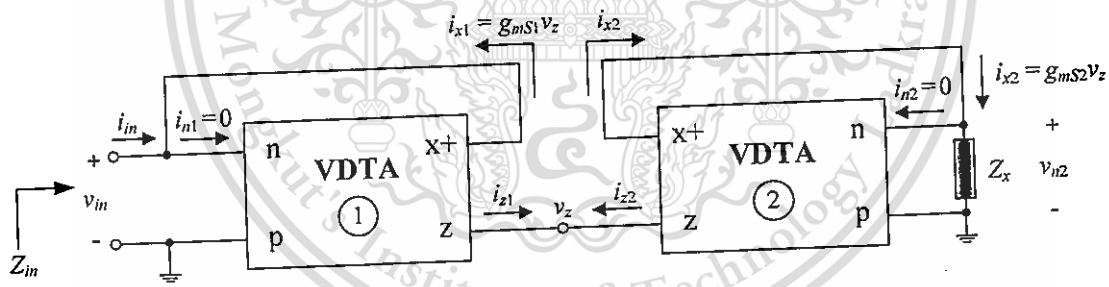


Figure B.1 : Configuration for determining the input-impedance function of the impedance multiplier circuit in Figure 3.1.

Applying Kirchoff's current law (KCL) at the input terminal, the summation of the currents can be given by

$$i_{in} + i_{x1} = i_{n1} \quad .$$

Now $i_{n1} = 0$, gives

$$i_{in} = -i_{x1} \quad . \tag{B.1}$$

With equation (2.1), the current i_{x1} at the terminal x+ of the VDTA1 can be calculated as :

$$i_{x1} = g_{mS1} v_z \quad . \tag{B.2}$$

By substituting equation (B.2) into equation (B.1), then we have

$$i_{in} = -i_{x1} = -g_{mS1} v_z \quad . \tag{B.3}$$

Also, from equation (2.1), the output currents flowing out from the z-terminals are determined as, respectively, :

$$i_{z1} = g_{mF1}(v_{p1} - v_{n1}) = g_{mF1}(0 - v_{in}) = -g_{mF1} v_{in} \quad , \tag{B.4}$$

and

$$i_{z2} = g_{mF2}(v_{p2} - v_{n2}) = g_{mF2}(0 - v_{n2}) = -g_{mF2} Z_x i_{x2} \quad . \tag{B.5}$$

Based on the same basic VDTA characteristic, the current i_{x2} of VDTA2 is exactly the same as equation (B.2), so that

$$i_{x2} = g_{mS2} v_z \quad . \tag{B.6}$$

Combining equations (B.5), (B.6) and (B.6), we find that

$$i_{z2} = -g_{mF2} g_{mS2} Z_x v_z = \left(\frac{g_{mF2} g_{mS2} Z_x}{g_{mS1}} \right) i_{in} \quad . \tag{B.7}$$

Similarly, KCL at the node z gives

$$i_{z1} = -i_{z2} \quad . \tag{B.8}$$

Substituting i_{z1} from equation (B.4) and i_{z2} from equation (B.7) into equation (B.8) yields

$$-g_{mF1} v_{in} = -\left(\frac{g_{mF2} g_{mS2} Z_x}{g_{mS1}} \right) i_{in} \quad . \tag{B.9}$$

Therefore, we can now compute the input impedance Z_{in} as :

$$Z_{in} = \frac{v_{in}}{i_{in}} = \left(\frac{g_{mF2} g_{mS2}}{g_{mF1} g_{mS1}} \right) Z_x \quad . \tag{B.10}$$

B.2 Effect of the VDTA Tracking Errors

Taking into account the non-ideal relationship, the terminal characteristics of the non-ideal VDTA can be rewritten as :

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ \beta_F g_{mF} & -\beta_F g_{mF} & 0 \\ 0 & 0 & \beta_S g_{mS} \\ 0 & 0 & -\beta_S g_{mS} \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix} , \qquad \text{(B.11)}$$

where β_F and β_S are respectively the voltage tracking errors for the first and second stages of the VDTA. Reanalysis the circuit configuration of Figure B.1 with equation (B.11), the input impedance function for this case can be derived as follows.

Consider the VDTA1, we have for the input current (i_{in}) at the terminal +x as :

$$i_{in} = -i_{x1} \quad , \qquad \text{(B.12)}$$

where the current i_{x1} can be defined from equation (B.11) as :

$$i_{x1} = \beta_{S1} g_{mS1} v_z \quad . \qquad \text{(B.13)}$$

From above two equations, the input current (i_{in}) is then obtained as :

$$i_{in} = -i_{x1} = -\beta_{S1} g_{mS1} v_z \quad . \qquad \text{(B.14)}$$

Likewise, using equation (B.11), the output currents i_{z1}, i_{z2} and i_{x2} can also be calculated as, respectively, :

$$i_{z1} = \beta_{F1} g_{mF1} (v_{p1} - v_{n1}) = \beta_{F1} g_{mF1} (0 - v_{in}) = -\beta_{F1} g_{mF1} v_{in} \quad , \qquad \text{(B.15)}$$

$$i_{z2} = \beta_{F2} g_{mF2} (v_{p2} - v_{n2}) = \beta_{F2} g_{mF2} (0 - v_{n2}) = -\beta_{F2} g_{mF2} Z_x i_{x2} \quad , \qquad \text{(B.16)}$$

and

$$i_{x2} = \beta_{S2} g_{mS2} v_z \quad . \qquad \text{(B.17)}$$

Also, taking $i_{z1} = -i_{z2}$, and substituting i_{x2} from equation (B.17) yields

$$-\beta_{F1} g_{mF1} v_{in} = -\left(\frac{\beta_{F2} \beta_{S2} g_{mF2} g_{mS2} Z_x}{\beta_{S1} g_{mS1}} \right) i_{in} \quad , \tag{B.18}$$

which rearranges to

$$Z_{in} = \frac{v_{in}}{i_{in}} = \left(\frac{\beta_{F2} \beta_{S2} g_{mF2} g_{mS2}}{\beta_{F1} \beta_{S1} g_{mF1} g_{mS1}} \right) Z_x \quad . \tag{B.19}$$

B.3 Analysis of Active and Passive Sensitivities

The term "sensitivity" is used to express the degree of influence of a variation in the value of one (or more) component on the performance of the circuit in which it is embedded. In general, the relative sensitivity of a parameter Y to the component of variation x can be defined as:

$$S_x^G = \frac{\%\text{change in G}}{\%\text{change in } x} = \frac{(\Delta G/G)\times 100\%}{(\Delta x/x)\times 100\%} \quad , \tag{B.20}$$

which can be manipulated in the following form :

$$S_x^G = \frac{\partial G/G}{\partial x/x} = \frac{x}{G}\frac{\partial G}{\partial x} \quad . \tag{B.21}$$

In the case of general impedance multiplication function in Figure 3.1, the sensitivity of Z_{in} with respect to active and passive components are defined as follows :

$$S_x^{Z_{in}} = \frac{x}{Z_{in}}\frac{\partial Z_{in}}{\partial x} \quad . \tag{B.22}$$

In order to demonstrate this matter, let us consider the generalized tunable impedance multiplier circuit in Figure 3.1, where its non-ideal input impedance is found as :

$$Z_{in} = \frac{v_{in}}{i_{in}} = \left(\frac{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}}{\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}}\right)Z_x \quad . \tag{B.23}$$

For example, from equation (B.22), the critical active sensitivity of Z_{in} to the variations in β_{F1} is therefore given by

$$S_{\beta_{F1}}^{Z_{in}} = \frac{\beta_{F1}}{Z_{in}} \frac{\partial Z_{in}}{\partial \beta_{F1}} \quad . \tag{B.24}$$

Inserting β_{F1} from equation (B.23) into (B.24) results in

$$S_{\beta_{F1}}^{Z_{in}} = \left[\frac{\beta_{F1}}{\left(\frac{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}}{\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}} \right) Z_x} \right] \left[\frac{\partial \left(\frac{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}}{\beta_{F1}\beta_{S1}g_{mF1}g_{mS1}} \right) Z_x}{\partial (\beta_{F1})} \right]$$

$$= \left[\frac{\beta_{F1}^2}{\left(\frac{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}Z_x}{\beta_{S1}g_{mF1}g_{mS1}} \right)} \right] \left[\left(\frac{\beta_{F2}\beta_{S2}g_{mF2}g_{mS2}Z_x}{\beta_{S1}g_{mF1}g_{mS1}} \right) \left(\frac{\partial \beta_{F1}^{-1}}{\partial \beta_{F1}} \right) \right]$$

$$= (\beta_{F1})^2 (-1)(\beta_{F1})^{-2} = -1 \tag{B.25}$$

Above expression readily indicates that the Z_{Ain}-sensitivity with respect to β_{F1} is equal to -1. In the same manner, it is easy to show that the sensitivities of the input impedance Z_{in} with respect to the deviations in the active and passive component values are calculated to be :

$$S_{\beta_{S1}}^{Z_{in}} = -1 \tag{B.26}$$

$$S_{\beta_{F2}}^{Z_{in}} = S_{\beta_{S2}}^{Z_{in}} = 1 \tag{B.27}$$

and

$$S_{Z_x}^{Z_{in}} = 1 \quad . \tag{B.28}$$

Clearly, it is obvious from equations (B.26)-(B.28) that all the active and passive sensitivities of Z_{in} of the impedance multiplier in Figure 3.1 are within unity in magnitude.

APPENDIX C

Performance Analysis for Floating Inductance and Capacitance Simulators Proposed in Chapter 4

C.1 Derivation for the Input Impedance (Z_{in}) of the Floating Inductor in Figure 4.1

According to the VDTA-based floating inductance simulator structure of Figure 4.1, it can be redrawn as illustrated in Figure C.1. Therefore, a detailed analysis for determining the short-circuit admittance matrix equation of the scheme is as follows.

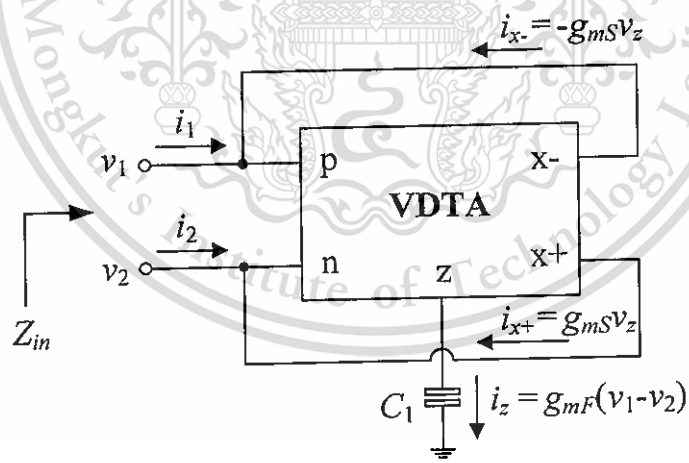


Figure C.1 : Configuration for determining the input impedance of the floating inductor circuit in Figure 4.1.

Considering $i_1 = -i_{x-}$ and $i_2 = -i_{x+}$, the input currents i_1 and i_2 are

$$i_1 = -i_{x-} = -(-g_{mS} v_z) = g_{mS} v_z \quad , \tag{C.1}$$

and

$$i_2 = -i_{x2} = -g_{mS} v_z \quad , \tag{C.2}$$

where

$$v_z = \left(\frac{1}{sC_1}\right) i_z = \left(\frac{g_{mF}}{sC_1}\right)(v_1 - v_2) \quad . \tag{C.3}$$

Substituting v_z from equation (C.3) into (C.1) and (C.2), yields

$$i_1 = -i_2 = \left(\frac{g_{mS} g_{mF}}{sC_1}\right)(v_1 - v_2) \quad . \tag{C.4}$$

Now, the input impedance (Z_{in}) for the simulator in Figure C.1 can be derived as :

$$Z_{in} = \left(\frac{v_1 - v_2}{i_1}\right) = -\left(\frac{v_1 - v_2}{i_2}\right) = s\left(\frac{C_1}{g_{mS} g_{mF}}\right) \quad , \tag{C.5}$$

where the realized equivalent inductance can be computed as :

$$L_{eq} = \left(\frac{C_1}{g_{mS} g_{mF}}\right) . \tag{C.6}$$

C.2 Derivation for the Input Impedance (Z_{in}) of the Floating Capacitor in Figure 4.2

Consider the circuit configuration of Figure C.2(a). It is obvious that this configuration is obtained from the scheme of Figure C.1 by replacing the capacitor C_1 with VDTA2 and the capacitor C_2. Therefore, the input impedance of the circuit can be derived as follows.

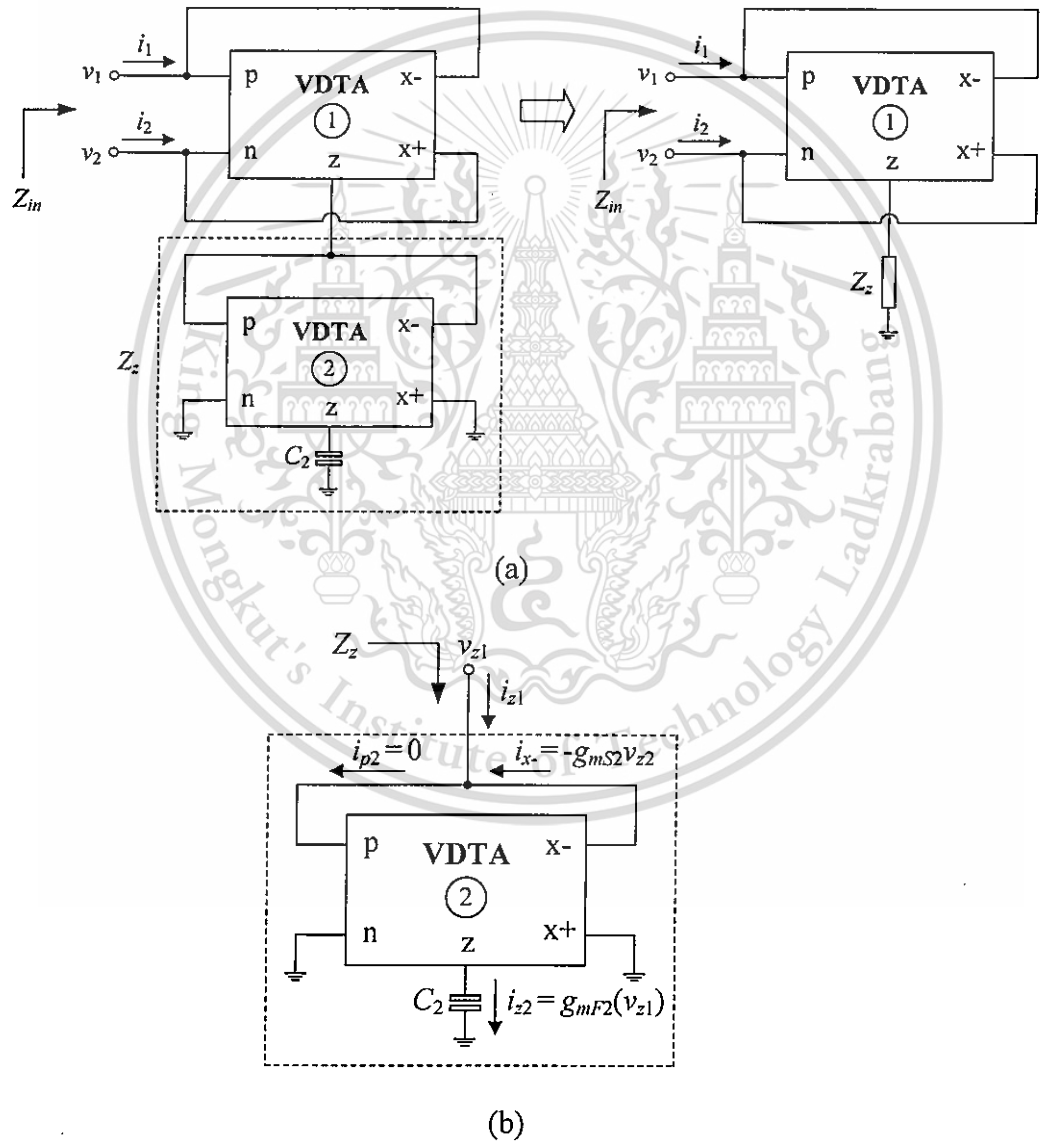


Figure C.2 : Configuration for determining the input impedance of the floating capacitor circuit in Figure 4.2.

By inspection of Figure C.2(a), if we now let that VDTA2 and C_2 perform as the impedance Z_z. Hence, analysis of the input impedance Z_{in} of this simulator can be done in the same previous steps. As a result of equation (C.5), the Z_{in} is found as :

$$Z_{in} = \left(\frac{v_1 - v_2}{i_1}\right) = -\left(\frac{v_1 - v_2}{i_2}\right) = \left(\frac{1}{g_{mF1} g_{mS1} Z_z}\right) \quad , \tag{C.7}$$

where $$Z_z = \frac{v_{z1}}{i_{z1}} \quad . \tag{C.8}$$

To find the relationship between v_{z1} and i_{z1}, Kirchoff's current law (KCL) is utilized. From KCL at the node z1 of Figure C.2(b), we obtain

$$i_{z1} + i_{x-} = 0 \quad , \tag{C.7}$$

where $$i_{x-} = -g_{mS2} v_{z2} \quad , \tag{C.8}$$

and $$v_{z2} = \frac{i_{z2}}{sC_2} = \frac{g_{mF2} v_{z1}}{sC_2} \quad . \tag{C.9}$$

Substitution of equations (C.8) and (C.9) into (C.7) yields

$$i_{z1} - g_{mS2} v_{z2} = i_{z1} - g_{mS2}\left(\frac{g_{mF2} v_{z1}}{sC_2}\right) = 0 \quad . \tag{C.10}$$

Rearranging above equation gives

$$Z_z = \frac{v_{z1}}{i_{z1}} = \frac{sC_2}{g_{mF2} g_{mS2}} \quad . \tag{C.11}$$

Combining equations (C.7) and (C.11) shows that the input impedance Z_{in} for the floating capacitance simulator of Figure C.2(a) is :

$$Z_{in} = \frac{g_{mF2} g_{mS2}}{sC_2 g_{mF1} g_{mS1}} = \frac{1}{sC_{eq}} \quad , \tag{C.12}$$

which gives the equivalent capacitance :

$$C_{eq} = \frac{C_2 g_{mF1} g_{mS1}}{g_{mF2} g_{mS2}} \quad . \tag{C.13}$$

C.3 Effect of the VDTA Non-Ideal Gains

At high-frequency operation, the frequency-dependent transconductance gains of the VDTA can each be characterized by the following single-pole model :

$$g_{mF}(s) = \frac{g_{mF0}}{1 + s\tau_F} \tag{C.14}$$

and

$$g_{mS}(s) = \frac{g_{mS0}}{1 + s\tau_S} \tag{C.15}$$

where g_{mF0} and g_{mS0} are the transconductance gains at low frequencies, $\omega_F = 1/\tau_F$ and $\omega_S = 1/\tau_S$ are the corresponding pole frequencies. In general, the values of these poles will depend on practical implementation of the VDTA.

Now, substituting $g_{mF}(s)$ from equation (C.14) into (C.5) for g_{mF} and rearranging leads to

$$Z_{in} = \left(\frac{sC_1}{g_{mF0}g_{mS0}}\right)\left[\frac{(s+\omega_F)(s+\omega_S)}{\omega_F\omega_S}\right] \tag{C.16}$$

Also, inserting equation (C.15) into equation (C.12), and solving this for Z_{in} of Figure C.2(b) gives

$$Z_{in} = \left(\frac{g_{mF10}g_{mS10}}{sC_2g_{mF20}g_{mS20}}\right)\left(\frac{\omega_{F1}\omega_{S1}}{\omega_{F2}\omega_{S2}}\right)\left[\frac{(s+\omega_{F2})(s+\omega_{S2})}{(s+\omega_{F1})(s+\omega_{S1})}\right] \tag{C.17}$$

APPENDIX D

Derivation for the Input Admittance (Y_{in}) of the Floating Frequency-Dependent Negative Resistance in Figure 5.1

Reconsider the proposed VDTA-based floating FDNR shown in figure 5.1. Here, to derive the input admittance (Y_{in}), its configuration is shown again in Figure D.1(a). The derivation for Y_{in} proceeds as follows.

With the same principle as section C.2, the input admittance looking into the terminals p and n of the VDTA1 is thus equal to :

$$Y_{in} = \frac{1}{Z_{in}} = \left(\frac{i_1}{v_1 - v_2}\right) = -\left(\frac{i_2}{v_1 - v_2}\right) = g_{mF1} g_{mS1} Z_z \quad , \tag{D.1}$$

where

$$Z_z = \frac{v_{z1}}{i_{z1}} \quad . \tag{D.2}$$

A simplified circuit used to determine the equivalent impedance Z_z is shown in Figure D.1(b). From this circuit, we find that :

$$i_{z1} + i_{x-} = 0 \quad , \tag{D.3}$$

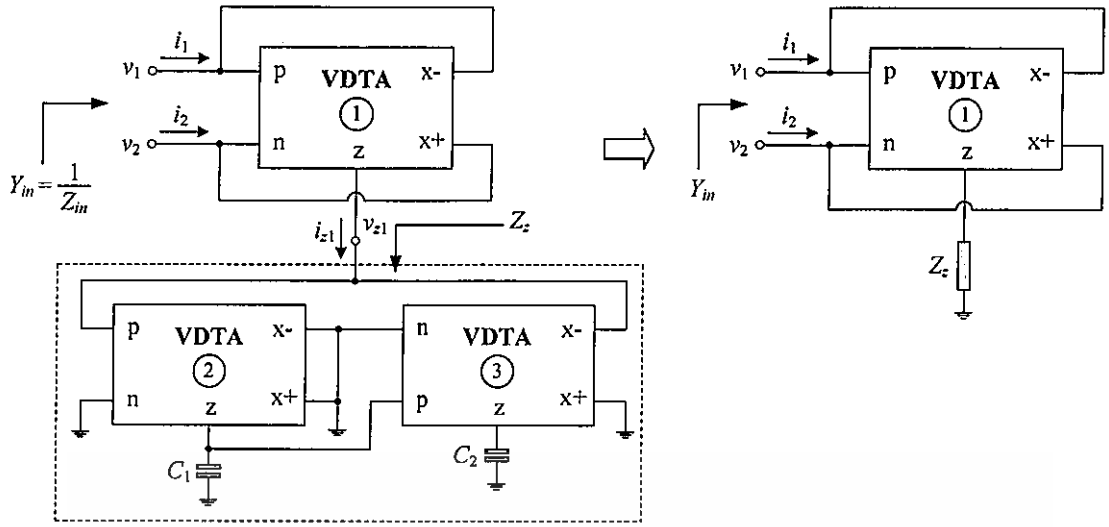
where

$$i_{x-} = -g_{mS3} v_{z3} = -\left(\frac{g_{mS3}}{sC_2}\right) i_{z3} \quad , \tag{D.4}$$

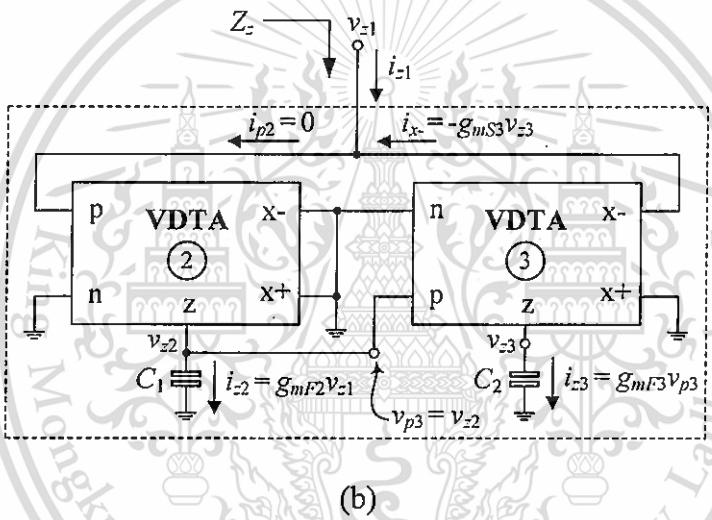
$$i_{z3} = g_{mF3} v_{p3} = g_{mF3} v_{z2} = \left(\frac{g_{mF3}}{sC_1}\right) i_{z2} \quad . \tag{D.5}$$

and

$$i_{z2} = g_{mF2} v_{p2} = g_{mF2} v_{z1} \quad . \tag{D.6}$$



(a)



(b)

Figure D.1 : Configuration for determining the input admittance of the floating FDNR circuit in Figure 5.1.

Substituting for i_{z3} from equation (D.6) in (D.5), we find

$$i_{z3}=\left(\frac{g_{mF2}g_{mF3}}{sC_1}\right)v_{z1} \quad . \tag{D.7}$$

Also, using equation (D.7) in (D.4) yields

$$i_{x-}=-\left(\frac{g_{mF2}g_{mF3}g_{mS3}}{s^2C_1C_2}\right)v_{z1} \quad . \tag{D.8}$$

Thus, substituting equations (D.8) into (D.3) yields

$$i_{z1} = \left(\frac{g_{mF2} g_{mF3} g_{mS3}}{s^2 C_1 C_2} \right) v_{z1} \quad . \tag{D.9}$$

Rearranging above equation, we get

$$Z_z = \frac{v_{z1}}{i_{z1}} = \frac{s^2 C_1 C_2}{g_{mF2} g_{mF3} g_{mS3}} \quad . \tag{D.10}$$

Therefore, from equations (D.10) and (D.1), we now obtain the input admittance function of the configuration shown in Figure D.1 as follows :

$$Y_{in} = \frac{1}{Z_{in}} = s^2 \left(\frac{C_1 C_2 g_{mF1} g_{mS1}}{g_{mF2} g_{mF3} g_{mS3}} \right) = s^2 D_{eq} \quad , \tag{D.11}$$

where the realized equivalent D-element can be obtained as :

$$D_{eq} = \frac{C_1 C_2 g_{mF1} g_{mS1}}{g_{mF2} g_{mF3} g_{mS3}} \quad . \tag{D.12}$$

APPENDIX E

International Publication Papers

The part of this dissertation leads the research papers that can be published in international journals with ISI impact factor, and international conferences. The list of publication papers is as follows.

E.1 Publication Papers in International Journals

[1] W. Tangsrirat and **S. Unhavanich**, "Voltage differencing transconductance amplifier-based floating simulators with a single grounded capacitor", *Indian Journal of Pure & Applied Physics*, vol.52, no.6, pp.423-428, 2014. (Impact Factor 2012 = 0.854).

[2] W. Tangsrirat and **S. Unhavanich**, "Signal flow graph realization of single-input five-output current-mode universal biquad using current follower transconductance amplifiers", *Revue Roumaine Des Sciences Techniques*, vol.59, no.2, pp.183-191, 2014. (Impact Factor 2012 = 0.337).

E.2 Publication Papers in International Conferences

[1] **S. Unhavanich**, P. Mongkolwai and W. Tangsrirat, "Simulation of frequency-dependent negative resistance (FDNR) using voltage differencing transconductance amplifiers (VDTAs)", *Proceedings of Annual Conference on Engineering and Information Technology (ACEAIT-2015)*, Osaka, Japan, 22-24 March, pp.489-496, 2015.

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[3] O. Onjan, **S. Unhavanich** and W. Tangsrirat, "SFG actualization of general n^{th}-order voltage transfer functions using VDBAs", *Proceedings of the International MultiConference of Engineers and Computer Scientists 2016 (IMECS 2016)*, Vol II, 16-18 March, Hong Kong, pp.585-589, 2016.

[4] W. Tangsrirat, T. Pukkalanun, **S. Unhavanich**, "Simple realization of BiCMOS current-controlled conveyor transconductance amplifier (CCCTA)", *Proceedings of Annual Conference on Engineering and Information Technology (ACEAIT-2014)*, 28-30 March, Tokyo, Japan, pp.1244-1250, 2014.

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http://www.niscair.res.in; http://nopr.niscair.res.in; Impact Factor 0.854 (JCR 2012)

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CONTENTS

Authors for correspondence are indicated by (*)

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Voltage differencing transconductance amplifier-based floating simulators with a single grounded capacitor

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Two simple configurations for simulating the resistorless floating inductor and capacitor using voltage differencing transconductance amplifier (VDTA) as a novel active element have been presented in this paper. The proposed floating simulated inductance circuit uses only one VDTA and one grounded capacitor, whereas the proposed floating simulated capacitance circuit uses two VDTAs and one grounded capacitor. The equivalent values of the realized simulators can be tuned electronically through the transconductance parameter of the VDTA. Both of the circuits also do not require any realization conditions. The proposed circuits together with their applications are demonstrated using PSPICE simulation with 0.35 μm TSMC CMOS technology.

Keywords: Voltage differencing transconductance amplifier, Floating inductance simulator, Floating capacitance simulator

1 Introduction

Floating simulator circuits are very useful active building blocks in many applications such as filter design, oscillator design and cancellation of parasitic elements. This is due to the well-known fact that the use of the physical inductor and capacitor, particularly of large values, is either not permitted or is unwanted in the integrated circuit technology. Accordingly, many circuits for the simulation of floating inductor and capacitors using various active elements have been introduced in the literature[1-16]. A survey of the literature shows that the floating simulator realizations[1-16] still suffer from the following weakness:

(i) More than one active or one passive component for floating inductance simulation[1,5-16] is required.
(ii) They have either two of more active devices or more than one passive element for floating capacitance simulation[2-5,7,11,13,15,16].
(iii) They use some floating passive components[1-2,4,7-9,14].
(iv) They employ any external passive resistors[1-2,4,7-9,11,13-15].
(v) They cannot be tuned electronically[1-2, 4, 6-9, 13,14].

In recent years, great emphasis has been placed on the use of new active elements in various analog active circuit designs, e.g., amplifiers, oscillators, filters or more generally, analog signal processing circuits[17]. The voltage differencing transconductance amplifier (VDTA) is a recently introduced active element. This element is composed of the current source controlled by the difference of two input voltages and a multiple-output transconductance amplifier, providing electronic tuning ability through its transconductance gains. Therefore, the VDTA device is very suitable for electronically tunable active circuit synthesis. Another advantageous feature of the use of the VDTA as an active element is that compact structures in some applications can be achieved easily[17,18]. All these advantages make the VDTA an alternative choice for the implementation of voltage-mode analog signal processing circuits.

Two topologies for realizing a floating inductor and a floating capacitor employing VDTA as a novel active element have been presented. The proposed inductor is generated with only one VDTA and one grounded capacitor, while the proposed capacitor is generated with two VDTAs and one grounded capacitor. Both of the proposed floating simulators can be tuned electronically through the transconductance parameter of the VDTA. Since the circuits are composed of only grounded capacitor without requiring any external passive resistor, they are canonical structures and quite suitable for fully integrated circuit design[19]. Some applications together

with the simulation results are also given to illustrate the performance of the proposed floating simulator circuits.

2 Basic Concept of the VDTA

As symbolically shown in Fig. 1, the VDTA is a versatile active building block, where p and n are high-impedance input terminals and z, x+ and x− are high-impedance output terminals. The terminal relations of this device can be characterized by the following matrix equation[17,18] :

$$\begin{bmatrix} i_z \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} g_{mF} & -g_{mF} & 0 \\ 0 & 0 & g_{mS} \\ 0 & 0 & -g_{mS} \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix} \quad \ldots(1)$$

where g_{mF} and g_{mS} are the first and second transconductance gains of the VDTA, respectively. From Eq. (1), the differential input voltage from the terminals p and n is transformed into output currents at the terminal z with first transconductance gain (g_{mF}). The voltage drop at the terminal z (v_z) is transformed into output currents at the terminal x+ and x-with second transconductance gain (g_{mS}). In general, the transconductance gains of the VDTA are electronically controllable.

Recently, the simple CMOS realization of the VDTA is introduced[18]. Figure 2 shows the internal structure of the circuit, which is composed of two Arbel-Goldminz transconductances[20]. In this case, the g_{mF}- and g_{mS}- values of this element are determined by the output transistor transconductance, which can respectively be approximated as:

$$g_{mF} \cong \left(\frac{g_1 g_2}{g_1 + g_2}\right) + \left(\frac{g_3 g_4}{g_3 + g_4}\right) \quad \ldots(2)$$

and

$$g_{mS} \cong \left(\frac{g_5 g_6}{g_5 + g_6}\right) + \left(\frac{g_7 g_8}{g_7 + g_8}\right) \quad \ldots(3)$$

where $g_i = \sqrt{I_{Bi}\mu C_{ox}\frac{W_i}{L_i}}$ is the transconductance value of the i-th MOS transistor (i = 1, 2, …, 8), I_{Bi} the bias current, μ the effective carrier mobility, C_{ox} the gate-oxide capacitance per unit area and W and L are the effective channel width and length of the i-th transistor, respectively.

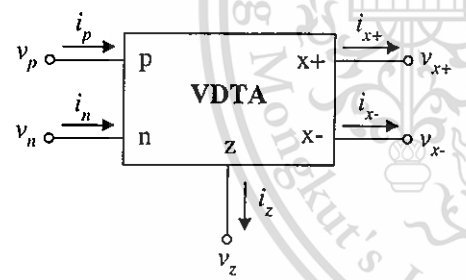


Fig. 1 — Electrical symbol of VDTA

3 Proposed Floating Inductor

The proposed floating inductance simulator circuit is shown in Fig. 3. It is composed of one VDTA and

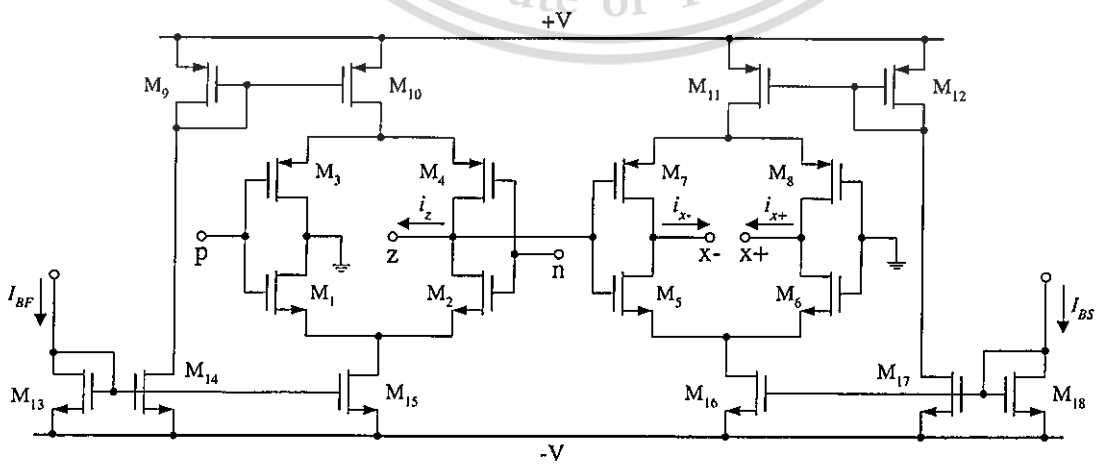


Fig. 2 — CMOS implementation of the VDTA derived from Ref.(18)

one grounded capacitor, without needing an external passive resistor. Straightforward analysis of the proposed floating inductor in Fig. 3 yields the following short-circuit admittance matrix:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{g_{mF}g_{mS}}{sC_1}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad \ldots(4)$$

or we can obtain the following input impedance:

$$Z_{in} = \frac{sC_1}{g_{mF}g_{mS}} = sL_{eq} \quad \ldots(5)$$

It is clearly seen from expression given in Eq.(5) that the circuit of Fig. 3 can simulate a floating inductor with an equivalent inductance value $L_{eq} = C_1/g_{mF}g_{mS}$. Also note that the value of L_{eq} can be adjusted electronically through either g_{mF} or g_{mS} of the VDTA. In addition, if we let $V_1 = 0$ or $V_2 = 0$, then the proposed circuit can be used as a grounded inductor.

4 Proposed Floating Capacitor

Figure 4 shows the proposed floating capacitance simulator circuit. It should be noted that the structure in Fig. 4 is obtained from Fig. 3 by replacing the capacitor C_1 with the circuit of Fig. 3. Therefore, an input impedance of the circuit can be given by:

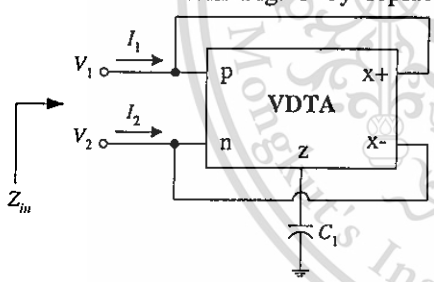


Fig. 3 — Proposed floating inductance simulator circuit

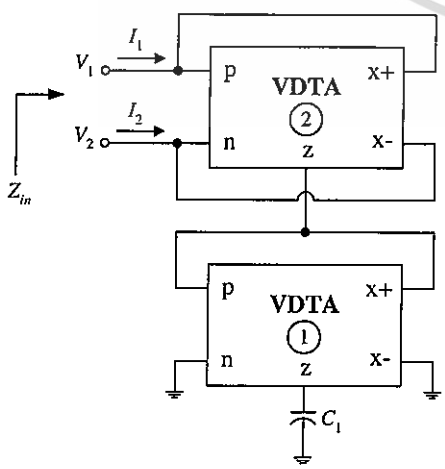


Fig. 4 — Proposed floating capacitance simulator circuit

$$Z_{in} = \frac{g_{mF1}g_{mS1}}{sC_1g_{mF2}g_{mS2}} = \frac{1}{sC_{eq}} \quad \ldots(6)$$

where the parameters g_{mFi} and g_{mSi} represent the transconductances g_{mF} and g_{mS} of i-th VDTA (i = 1, 2), respectively. One can see from Eq. (6) that the circuit shown in Fig. 4 realizes a floating capacitor whose the simulated equivalent capacitance is found as : $C_{eq} = C_1g_{mF2}g_{mS2}/g_{mF1}g_{mS1}$.

5 Analyses of Non-Ideal and Parasitic Effects

The non-ideal performance and the effect of parasitic elements are examined. It may be useful to discuss the VDTA non-ideality in the following sub-sections.

5.1 Non-Ideal Gain Effects

To evaluate the effects of the non-ideal gains at high frequencies, we first assume that frequency-dependent transconductance gains of the VDTA can each be described using a single-pole model as follows :

$$g_{mF}(s) = \frac{g_{mF0}}{1+s\tau_F} \quad \ldots(7)$$

and $$g_{mS}(s) = \frac{g_{mS0}}{1+s\tau_S} \quad \ldots(8)$$

where g_{mF0} and g_{mS0} are the transconductance gains at low frequencies, $\omega_F = 1/\tau_F$ and $\omega_S = 1/\tau_S$ are the corresponding pole frequencies. In general, the values of these poles will depend on practical implementation of the VDTA. Combining Eqs (5)-(8), the frequency-dependent input impedances of the proposed floating simulator circuits in Figs 3 and 4 can be re-written, respectively, as follows :

$$Z_{in} = \left(\frac{sC_1}{g_{mF0}g_{mS0}}\right)\left[\frac{(s+\omega_F)(s+\omega_S)}{\omega_F\omega_S}\right] \quad \ldots(9)$$

and

$$Z_{in} = \left(\frac{g_{mF10}g_{mS10}}{sC_1g_{mF20}g_{mS20}}\right)\left(\frac{\omega_{F1}\omega_{S1}}{\omega_{F2}\omega_{S2}}\right)\left[\frac{(s+\omega_{F2})(s+\omega_{S2})}{(s+\omega_{F1})(s+\omega_{S1})}\right] \quad \ldots(10)$$

Eqs (9) and (10) indicate that the useful operating-frequency regions of the proposed floating impedance simulators in Figs. 3 and 4 can, respectively, be defined as :

$$\omega << \min\{\omega_F, \omega_S\} \quad \ldots(11)$$

and

$$\omega << \min\{\omega_{F1}, \omega_{S1}, \omega_{F2}, \omega_{S2}\}. \quad \ldots(12)$$

It is also considered from Eq. (10) that if $\omega_{F1} \cong \omega_{F2}$ and $\omega_{S1} \cong \omega_{S2}$, then the effects of these parasitic poles can be ignored.

5.2 Parasitic Element Effects

Furthermore, parasitic impedances appearing at terminals of VDTA are analyses. In order to consider these parasitic impedances, the non-ideal equivalent circuit shown in Fig. 5 can be used. Ideally, the parasitic resistances R_p, R_n, R_z and R_x appearing in parallel, respectively, at corresponding terminals p, n, z and x are approximately equal to infinity, and parasitic capacitances C_p, C_n, C_z and C_x approximately equal to zero. Consider the proposed circuits in Fig. 3 and 4 including parasitic elements shown in Fig. 5. We see that the z-terminal of the VDTA in both circuits is terminated by a grounded capacitor C_1; hence, C_1 appears in parallel with the z-terminal parasitic ($R_z//C_z$). However, since the external capacitor C_1 chosen in design is usually in excess to the expected parasitic capacitance C_z ($C_1 >> C_z$), this effect can be absorbed at working frequencies. Therefore, the parasitic effect is not noticeable if the value of C_1 is chosen as :

$$\frac{1}{sC_1} << R_Z \quad \ldots(13)$$

6 Performance Simulations and Applications

The performances of the proposed floating inductor and capacitor in Figs 3 and 4 are shown by PSPICE simulation. The simulations were performed by using a CMOS realization as shown in Fig. 2 with *dc* supply voltages equal to ±1.8 V. The CMOS transistors in VDTA implementation were simulated using 0.35 μm TSMC CMOS technology process parameters. The dimensions of MOS transistors are given in Table 1.

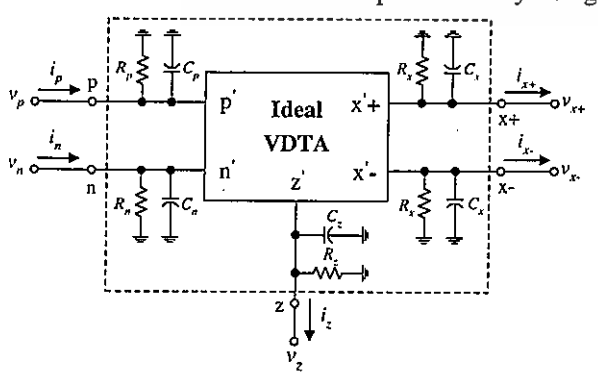


Fig. 5 — Parasitic impedances of the VDTA

The proposed floating simulator circuits shown in Figs 3 and 4 were simulated with C_1 = 1 nF. For the floating inductance simulator of Fig. 3, the VDTA's transconductances were varied as : $g_m = g_{mF} = g_{mS} \cong$ 0.27 mA/V ($I_B = I_{BF} = I_{BS} = 20$ μA), $g_m \cong 0.54$ mA/V ($I_B = 80$ μA) and $g_m \cong 0.81$ mA/V ($I_B = 180$ μA) for simulating L_{eq} = 13.74 mH, 3.43 mH, 1.52 mH, respectively. Likewise, for the floating capacitance simulator of Fig. 4, the transconductance values were selected as : $g_{m2} = g_{mF2} = g_{mS2} \cong 0.27$ mA/V, and $g_{m1} = g_{mF1} = g_{mS1} \cong 0.27$, 0.54 and 0.81 mA/V, which results in : C_{eq} = 1, 0.25, 0.11 nF, respectively. The impedances of the simulator circuits of Figs 3 and 4 relative to frequency are also shown in Figs 6 and 7, respectively. It appears from Figs 6 and 7 that the ideal and simulated magnitude and phase responses are found to be in good agreement for a set of selected values.

As an example to demonstrate the performance of the derived inductance simulator of Fig. 3, the 5-order lowpass Butterworth filter shown in Fig. 8 was designed with the de-normalized cut-off frequency of $f_c = \omega_c/2\pi = 300$ kHz.. The circuit was simulated with the ideal inductor and our proposed floating inductor.

Table 1 — Dimensions of MOS transistors of the VDTA circuit as shown in Fig. 2

Transistors	W (μm)	L (μm)
$M_1 - M_2$, $M_5 - M_6$	16.1	0.7
$M_3 - M_4$, $M_7 - M_8$	28	0.7
$M_9 - M_{12}$, $M_{14} - M_{17}$	56	0.7
M_{13}, M_{18}	7	0.7

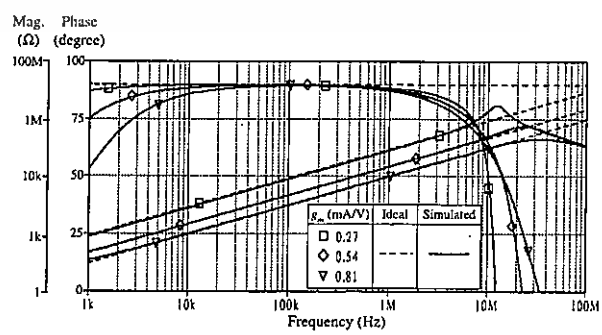


Fig. 6 — Ideal and simulated frequency responses of the proposed floating inductance simulator in Fig.3

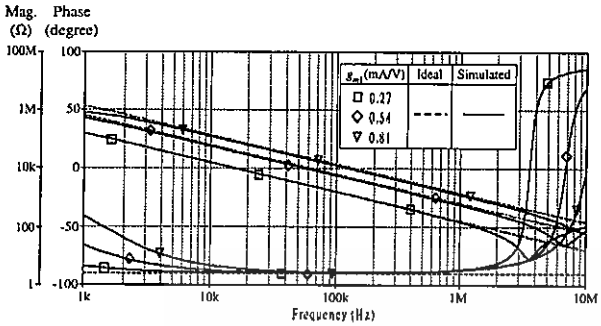
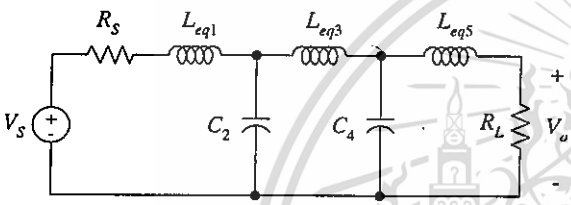


Fig. 7 — Ideal and simulated frequency responses of the proposed floating capacitance simulator in Fig. 4



$R_S = R_L = 41\ \Omega$ $L_{eq1} = L_{eq5} = 13.7\ \mu$H

$C_2 = C_4 = 20.5$ nF $L_{eq3} = 44.5\ \mu$H

Fig. 8 — 5th-order lowpass Butterworth filter with $f_0 = 300$ kHz

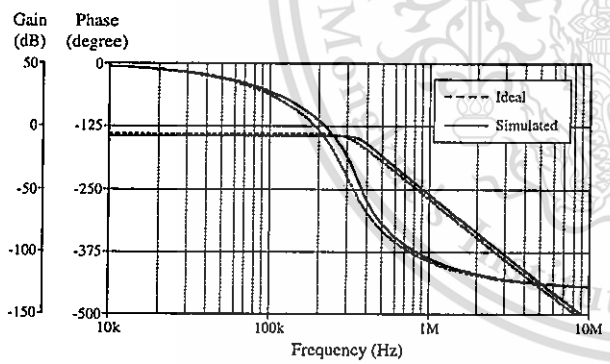


Fig. 9 — Theoretical and simulation results obtained from the filter of Fig. 8

For this purpose, the component values of the proposed floating inductor in Fig.3 were taken as follows : $g_m \cong 0.27$ mA/V, $C_1 = 1$ pF for $L_{eq1} = L_{eq5} \cong 13.7\ \mu$H, and $g_m \cong 0.15$ mA/V, $C_1 = 1$ pF for $L_{eq3} \cong 44.5\ \mu$H. The theoretical and simulation results for the filter of Fig. 8 are shown in Fig. 9.

Further, to demonstrate an application of the proposed floating capacitor of Fig. 4, it is employed in the RLC bandpass filter as shown in Fig. 10. The floating capacitor circuit is simulated with the following component values : $C_1 = 1$ nF and $g_{mF1} =$

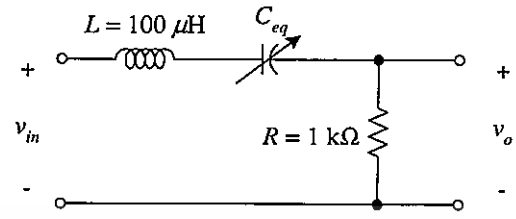


Fig. 10 — RLC bandpass filter

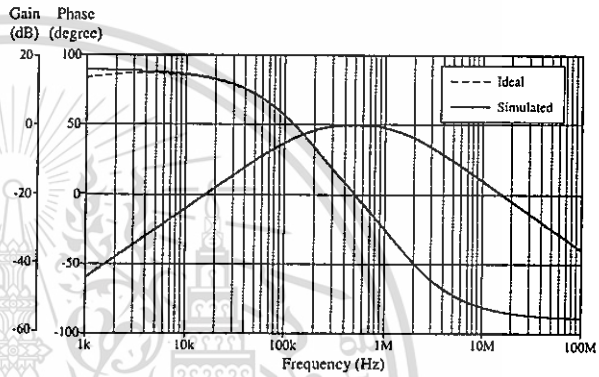


Fig. 11 — Ideal and simulated frequency responses of Fig.10

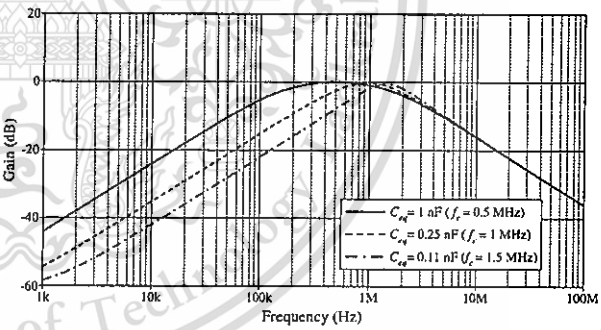


Fig. 12 — Simulated magnitude responses of Fig.10 with electronically variable C_{eq}

$g_{mS1} = g_{mF2} = g_{mS2} \cong 0.27$ mA/V ($I_{BF1} = I_{BS1} = I_{BF2} = I_{BS2} = 20\ \mu$A), which results in $C_{eq} = 1$ nF. Fig. 11 shows the frequency responses of the bandpass filter of Fig. 10, which appears that the ideal and simulated magnitude and phase responses are in good agreement for a set of selected values over several decades. Moreover, in order to demonstrate the electronic controllability of the proposed floating capacitor, the value of C_{eq} in Fig. 10 was adjusted to 1, 0.25 and 0.11 nF, by changing $g_{mF1} = g_{mS1} \cong 0.27$, 0.54 and 0.81 mA/V, respectively, while keeping $g_{mF2} = g_{mS2}$ constant at 0.27 mA/V. This tuning leads to obtain the center frequency $f_c \cong 0.5$, 1 and 1.5 MHz,

respectively. The simulated magnitude responses of the bandpass filter in Fig. 10 with electronically variable C_{eq} are shown in Fig. 12. From the results, the corresponding f_c are obtained as: 0.49, 0.94 and 1.39 MHz, respectively.

7 Conclusions

The floating inductance and capacitance simulation schemes have been described in the present paper. They are realized using only a single VDTA for inductance simulation and needing two VDTAs for capacitance simulation. Both of the proposed circuits employ only a grounded capacitor, which is suitable for integrated circuit implementation. The values of the simulated inductance and capacitance are tunable by adjusting the bias current of the VDTA. The usefulness of the proposed circuits is demonstrated on the filter design examples.

Acknowledgement

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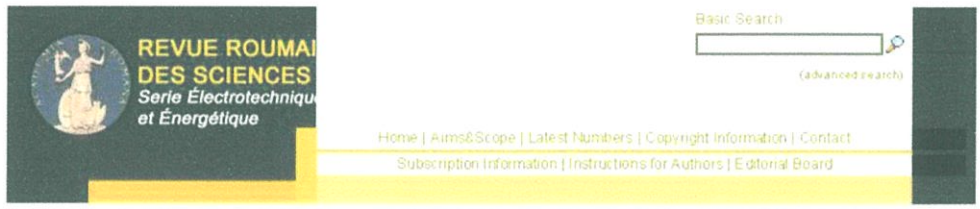

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SIGNAL FLOW GRAPH REALIZATION OF SINGLE-INPUT FIVE-OUTPUT CURRENT-MODE UNIVERSAL BIQUAD USING CURRENT FOLLOWER TRANSCONDUCTANCE AMPLIFIERS

WORAPONG TANGSRIRAT[1], SUMALEE UNHAVANICH

Key words: Signal flow graph (SFG), Current follower tranconductance amplifier (CFTA), Biquad filter, Current-mode circuit, Resistor-less circuit.

In this paper, a design procedure for the realization of all current-mode biquadratic transfer functions is presented. The synthesis technique is deduced from a signal flow graph representation using current follower transconductance amplifiers (CFTAs). The proposed configuration has single low-impedance input and five high-impedance outputs, and comprises three CFTAs and two grounded capacitors. No passive resistor is required for the circuit realization, thus it is an active-C structure suitable for integration.

1. INTRODUCTION

Recently, the conception of the current follower transconductance amplifier (CFTA) has been introduced [1]. This device is slightly modified from the conventional current differencing transconductance amplifier (CDTA) [2, 3] by replacing the current differencing unit with a current follower. Thus, the CFTA element is conceptually a combination of the current follower and the multi-output operational transconductance amplifier. Consequently, several structures for realizing current-mode active filters using CFTAs were developed [4–13]. Interesting circuit realizations of universal filters using signal flow graph (SFG) can be found in [4–8]. However, the filter structures in [4, 5] require external passive resistors. In [6], the circuit provides only three second-order filtering functions at most. Moreover, the works in [7, 8] employ a lot of active components.

Therefore, this work largely focuses on presenting a general synthesis procedure for realizing all standard second-order current transfer functions. The proposed method is based on drawing a SFG directly from the given transfer function and then obtaining, from the graph, the active C filter involving CFTAs. The resulting circuit using only three CFTAs and two grounded capacitors simultaneously realizes all the five standard second-order current transfer functions, namely

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lowpass (LP), bandpass (BP), highpass (HP), bandstop (BS) and allpass (AP). All capacitors used are grounded, which make the circuit especially suitable for monolithic implementation. Computer simulation results obtained from PSPICE program illustrate the properties of the proposed design procedure.

2. CURRENT FOLLOWER TRANCONDUCTANCE AMPLIFIER (CFTA)

The CFTA device is mainly combined by the current follower and multi-output transconductance amplifier. The circuit representation of the CFTA is shown in Fig.1, where f is the low-impedance input terminal and z, $+x$, x are the high-impedance output terminals. The port relations of the CFTA can be described by :

$$v_f = 0\ ,\ i_z = i_f \text{ and } i_x = g_m v_Z\ , \tag{1}$$

where g_m is the transconductance gain of the CFTA. According to above terminal equation, the current of z-terminal (i_z) follows the current of f terminal (i_f). The voltage drop at z-terminal (v_z) is then converted to currents at $+x$ and $-x$ terminals by a transconductane g_m and $-g_m$, respectively. Generally, the g_m value is adjustable over several decades by a supplied bias current/voltage, which lends electronic controllability to design circuit parameters.

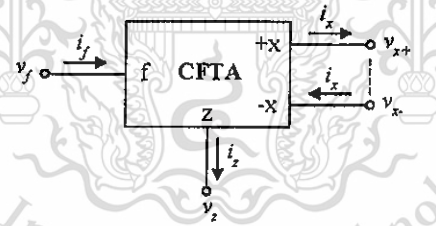

Fig. 1 – Circuit representation of the CFTA.

One possible implementation of CFTA in bipolar technology is shown in Fig. 2 [11, 12]. Transistors Q_1–Q_6 constitute a current follower stage that provides the current through the z terminal to follow the input current at the f-terminal and also exhibits the low-input resistance at the f terminal. The multiple-output transconductance amplifier formed by transistors Q_7–Q_{25} will convert to the currents i_x flowing through the x terminals. Thus, the transconductance (g_m) realized by the configuration in Fig. 2 is approximately found as :

$$g_m = \frac{I_O}{2V_T}\ , \tag{2}$$

where V_T is the thermal voltage (approximately 26 mV at 27°C) and I_O is the external bias current of the CFTA.

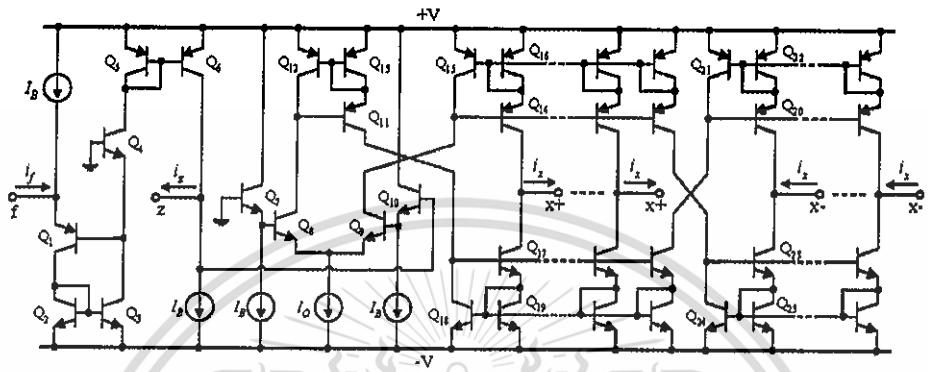

Fig. 2 – Bipolar implementation of the CFTA.

3. SFG REPRESENTATION AND CFTA REALIZATION

In this section, a SFG representation and coresponding CFTA-based circuit realization for a general biquadratic current transfer function synthesis are given. The synthesis procedure is based on drawing the SFG of the biquadratic filtering function, and then realizing the CFTA-C circuit from the given graph. In Fig. 3, the SFG for realizing a current-mode universal biquadratic filter is shown, which consists of two lossless integrators and unity-gain forward and feedback paths. According to the well-known Mason's gain formula [14], the current transfer functions of this graph can be expressed as :

$$\frac{I_{HP}}{I_{in}} = \frac{b_2 s^2}{D(s)}, \quad \frac{I_{BP}}{I_{in}} = \frac{b_1 s}{D(s)}, \quad \frac{I_{LP}}{I_{in}} = \frac{1}{D(s)},$$

$$\frac{I_{AP}}{I_{in}} = \frac{b_2 s^2 - b_1 s + 1}{D(s)}, \quad \frac{I_{BS}}{I_{in}} = \frac{b_2 s^2 + 1}{D(s)} \tag{3}$$

and $$D(s) = b_2 s^2 + b_1 s + 1,$$

where I_{HP}, I_{BP}, I_{LP}, I_{AP} and I_{BS} are the HP, BP, LP, AP and BS current responses, respectively. It should be noted that all the five standard biquadratic current transfer functions can be synthesized simultaneously from the graph of Fig. 3. This means that any circuit deduced from the SFG of Fig. 3 will function as a universal biquadratic filter.

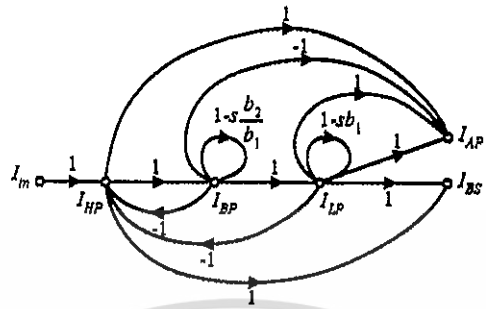

Fig. 3 – SFG for realizing general biquadratic transfer functions.

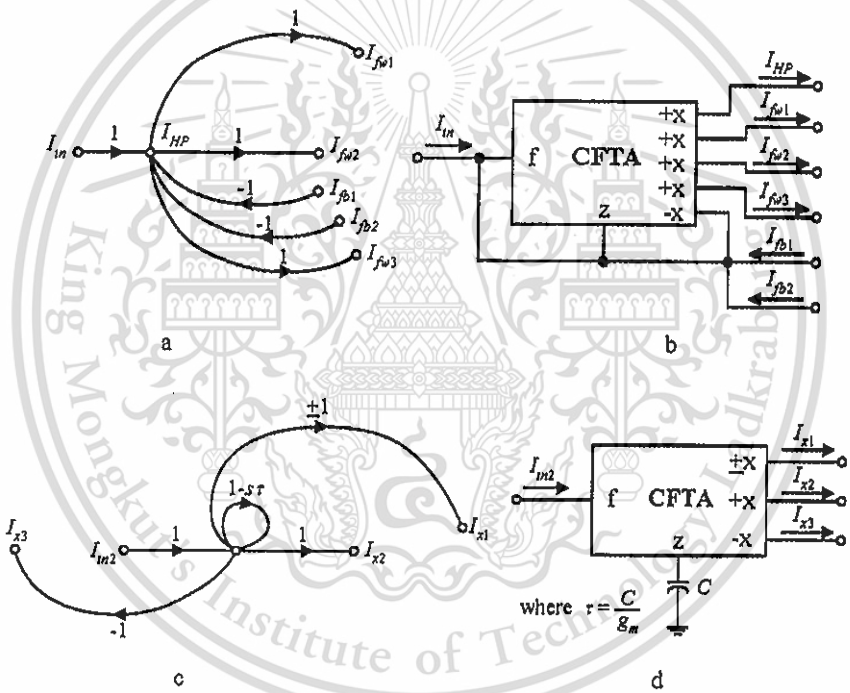

Fig. 4 – Sub-graphs and their corresponding CFTA-C sub-circuit realizations.

Considering the SFG synthesis of general biquadratic current transfer functions in Fig. 3. It is clearly seen that the graph consists of two basic operations, which are multi-output current follower and current lossless integrator, as redraw in Figs. 4 a and 4 c, respectively. Using the current and voltage relations of the CFTA given in equation (1), these two sub-graphs can be realized using CFTA by the corresponding sub-circuits as shown in Figs. 4 b and 4 d, respectively. For the CFTA-based realization, it can readily obtain the CFTA-C circuit by interconnecting the sub-circuits of Figs. 4 b and 4 d according to the overall SFG representation of

Fig. 3. Therefore, the CFTA-C circuit realizing universal second-order current transfer functions can be shown in Fig. 5. For this realization, the configuration contains three CFTAs as active elements and two capacitors as passive elements. Note that the circuit uses only grounded capacitors that is suitable for the integrated circuit implementation point of view, and also exhibits low-input impedance and high-output impedance terminals that are desirable for cascading in current-mode operation [9].

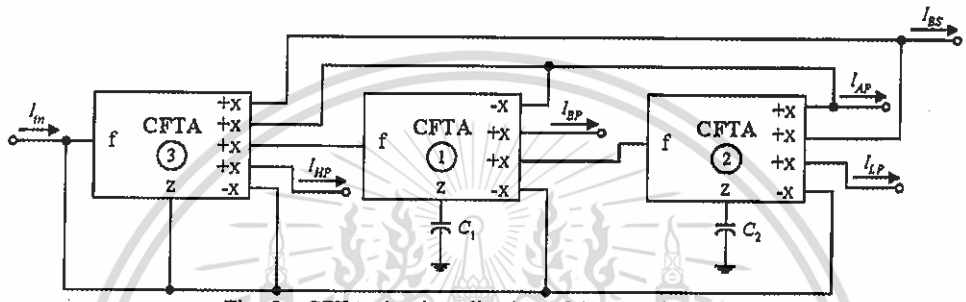

Fig. 5 – CFTA circuit realization of the SFG in Fig.3.

From Fig. 5, the design equations can be obtained through comparing Fig. 3 with Fig. 5. The results are summarized as follows :

$$\frac{b_2}{b_1}=\frac{C_1}{g_{m1}} \quad \text{and} \quad b_1=\frac{C_2}{g_{m2}}. \qquad (4)$$

Above expressions indicate that the coefficients b_i (i = 1, 2) of the realized functions can be tuned electronically by adjusting the g_{mi} value of the i-th CFTA.

In all cases, the natural angular frequency (ω_0), quality factor (Q) and bandwidth (BW) of the proposed filter are found as :

$$\omega_0=\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}, \qquad (5)$$

$$Q=\sqrt{\frac{g_{m2}C_1}{g_{m1}C_2}}. \qquad (6)$$

It is to be noted from above relations that the resultant frequency filter provides the possibility of electronic tuning the characteristic frequency ω_0 and Q by the value of g_{m2}, independently of the parameter

$$BW=\frac{g_{m1}}{C_1}. \qquad (7)$$

4. NON-IDEAL ANALYSIS

In case of the non-ideal CFTA, the relationship of the terminal voltage and current given in equation (1) can be rewritten as :

$$v_f = 0 \ , \ i_z = \alpha i_f \ \text{ and } \ i_x = g_m v_z \ , \tag{8}$$

where $\alpha = (1-\varepsilon_i)$ and ε_i ($|\varepsilon_i| << 1$) is the current tracking error from f to z terminals of the CFTA. Therefore, taking the non-idealities of the CFTA into account, the modified parameters ω_0, Q and BW of the proposed filter given in Fig. 5 become :

$$\omega_0 = \sqrt{\frac{\mu\alpha_1\alpha_2 g_{m1} g_{m2}}{C_1 C_2}} \ , \tag{9}$$

$$Q = \sqrt{\frac{\alpha_2 g_{m2} C_1}{\mu\alpha_1 g_{m1} C_2}} \ , \tag{10}$$

$$BW = \frac{\mu\alpha_1 g_{m1}}{C_1} \ , \tag{11}$$

and

$$\mu = \frac{\alpha_3 g_{m3} r_{z3}}{1-\alpha_3(1+g_{m3} r_{z3})} \ , \tag{12}$$

where α_i is the parameter α of the i-th CFTA, and r_{z3} is the parasitic resistance at the z-terminal of the CFTA3.

The active and passive sensitivities of the parameters ω_0 , Q and BW for this biquad filter are calculated as below :

$$S^{\omega_0}_{\mu,\alpha_1,\alpha_2,g_{m1},g_{m2}} = -S^{\omega_0}_{C_1,C_2} = \frac{1}{2} \tag{13}$$

$$S^{Q}_{\mu,\alpha_1,g_{m1}} = -S^{Q}_{\alpha_2,g_{m2}} = -S^{Q}_{C_1} = S^{Q}_{C_2} = -\frac{1}{2} \ , \tag{14}$$

$$S^{BW}_{\mu,\alpha_1,g_{m1}} = -S^{BW}_{C_1} = 1 \ . \tag{15}$$

Sensitivity analyses show that all magnitudes of ω_0, Q and BW sensitivities are found to be not more than unity in magnitude.

5. PERFORMANCE VERIFICATION AND DISCUSSION

To verify the theoretical analysis, the proposed design procedure given above has been simulated with PSPICE simulation program. To implement the CFTA active device in simulations, the bipolar technology structure depicted in Fig.2 has been employed [11, 12] using transistor model PR100N (PNP) and NP100N (NPN) real process parameters. The DC supply voltages and bias current were selected as: $+V = -V = 2$ V and $I_B = 100$ μA, respectively.

As an example, the illustrative CFTA-based second-order current transfer function synthesis of Fig. 5 was designed with $f_0 = \omega_0/2\pi \cong 159$ kHz. For this purpose, the de-normalized component value were chosen as: $C_1 = C_2 = 1$ nF, $g_{m1} = 1.4$ mA/V ($I_{O1} \cong 74$ μA), $g_{m2} = 0.7$ mA/V ($I_{O2} \cong 37$ μA) and $g_{m3} = 1$ mA/V ($I_{O3} \cong 52$ μA). The simulated responses comparing with the theoretical values are shown in Figs. 6–8, respectively. From the results, it can be seen that the simulation results agree very well with theoretical predictions.

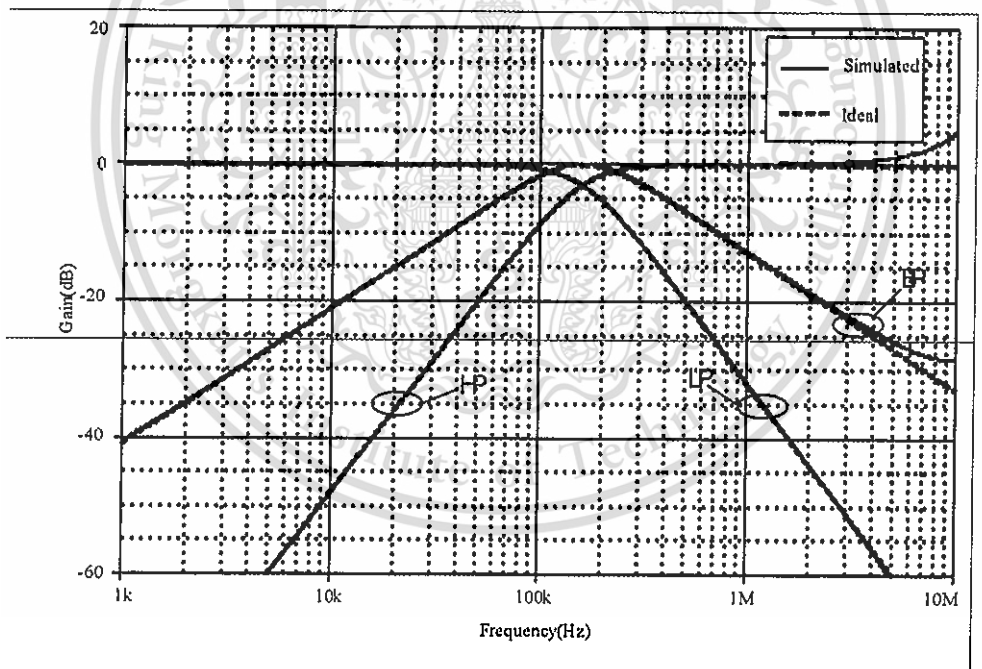

Fig. 6 – Ideal and simulated results for the LP, BP and HP current responses of the proposed circuit in Fig. 5.

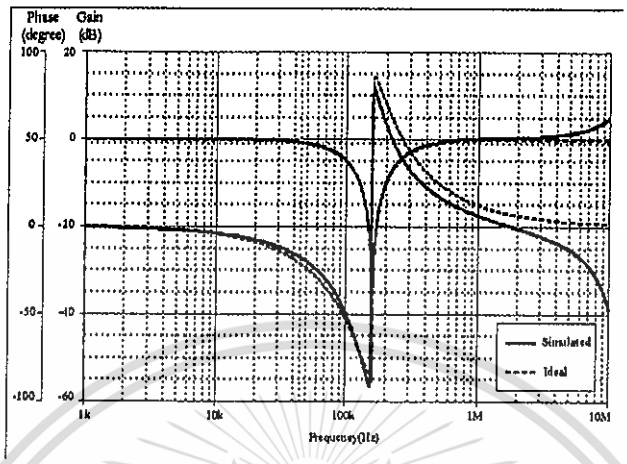

Fig. 7 – Ideal and simulated frequency characteristics for the BS response.

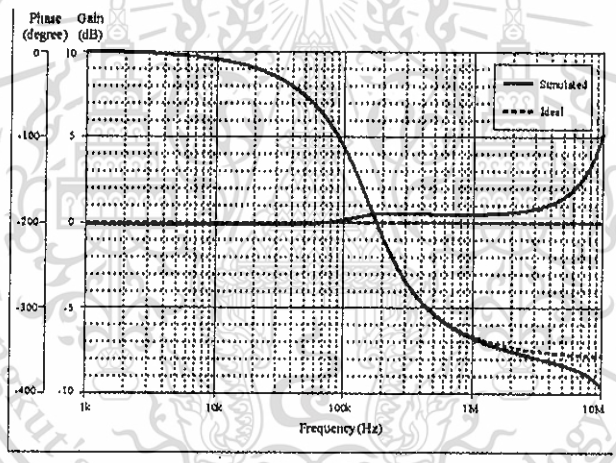

Fig. 8 – Ideal and simulated frequency characteristics for the AP response.

6. CONCLUSION

This work presents a synthesis procedure for realizing universal biquad filter by a resistor-less circuit. By using the SFG representation, the universal filters can be realized employing three CFTAs and two grounded capacitors. The resulting circuit obtained from the presented method is a canonical structure and especially suitable for integration. The proposed circuit can generate LB, BP, HP, BS and AP simultaneously. It has low-input and high-output impedances, and also convenient electronic controllability through the g_m value of the CFTA.

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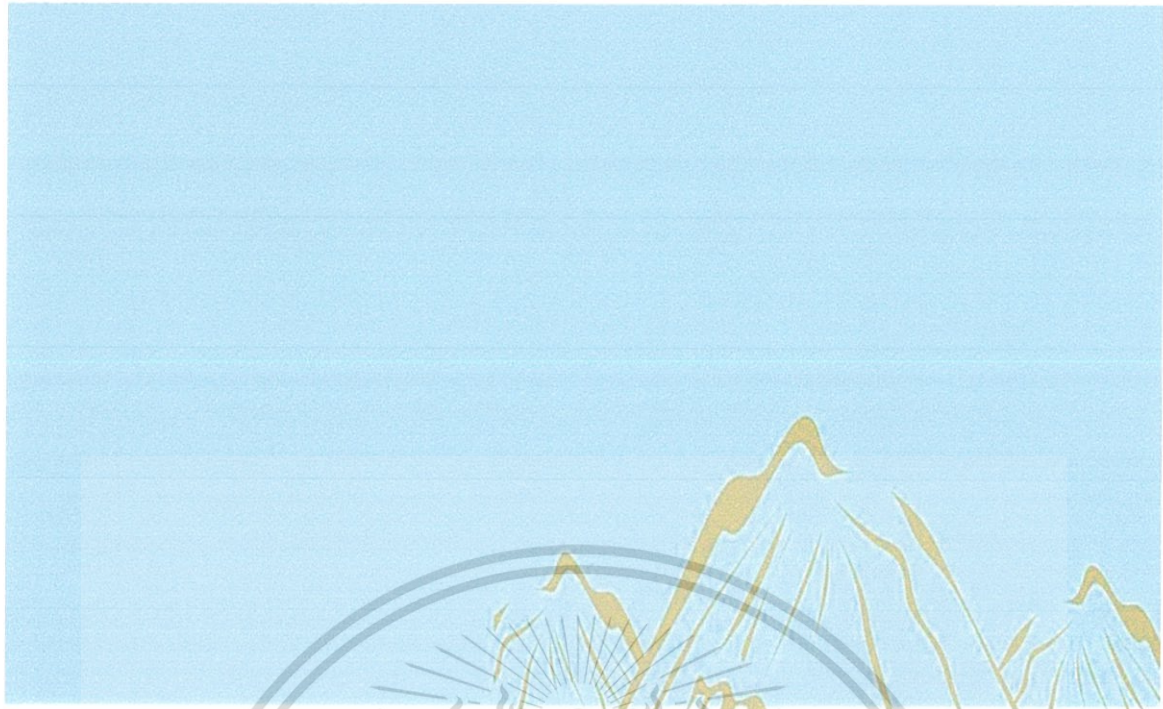

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Simulation of Frequency-Dependent Negative Resistance (FDNR) Using Voltage Differencing Transconductance Amplifiers (VDTAs)

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ABSTRACT

In this paper, the simple realization of an electronically controllable floating frequency-dependent negative resistance (FDNR) simulator circuit is introduced. The proposed FDNR simulator consists of solely three voltage differencing transconductance amplifiers (VDTAs) and two grounded capacitors without needing external resistors. The equivalent value of the realized D-element (D_{eq}) is electronically tunable by means of the VDTA transconductance values. Application examples on the fourth-order Butterworth bandpass filter realization using the proposed tunable floating FDNR are also performed. The simulation results obtained from PSPICE using TSMC 0.35-μm CMOS technology have been provided to confirm the theoretical analyses.

Keyword: Voltage Differencing Transconductance Amplifier (VDTA); Frequency-Dependent Negative Resistance (FDNR), Floating Simulator

1. Introduction

Frequency-Dependent Negative Resistances (FDNRs) are very useful elements for the design and synthesis active filter. Also, FDNR can be used in applications of using floating inductance. Several FDNR implementations using various active devices were proposed in literature [1]-[5]. However, the works in [1]-[4] require at least three passive components and most of them are floating. In [5], at least four active components were realized. Recently, the new active building block, namely voltage differencing transconductance amplifier (VDTA), has been introduced [6]. This element is composed of the current source controlled by the difference of two input voltages and a multiple-output transconductance amplifier, providing electronic tuning ability through its transconductance gains. This means that the VDTA device is very suitable for electronically tunable active circuit synthesis.

The objective of this work is to present an alternative approach of the floating FDNR simulator topology using only three VDTAs and two grounded capacitors. Accordingly, the simulator is very suitable for integrated circuit (IC) implementation point of view. The D-element value of the simulated FDNR can be tuned electronically tunable through the transconductance parameters of the VDTAs. As application examples, the design of fourth-order Butterworth filter based on the use of the proposed FDNR simulator is demonstrated. PSPICE simulations are also performed to show the characteristics of the simulator circuit, and to verify the mathematical analyses.

2. Principle of the VDTA Operation

2.1 Basic Concept

As symbolically shown in Fig.1, the VDTA device is an active five-terminal building block, when p and n are input terminals, and z, +x and -x are output terminals. The terminal relations of this device can be expressed by the following matrix equation :

$$\begin{bmatrix} i_z \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} g_{mF} & -g_{mF} & 0 \\ 0 & 0 & g_{mS} \\ 0 & 0 & -g_{mS} \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix} \qquad (1)$$

where g_{mF} and g_{mS} are the first and second transconductance gains of the VDTA, respectively. From eq.(1), the differential input voltage from p and n terminals ($v_p - v_n$) is transformed into the current through the terminal z (i_z) by the transconductance g_{mF}. The voltage drop at the terminal z (v_z) is then converted to output currents at the terminals +x (i_{x+}) and -x (i_{x-}) by the transconductance g_{mS}. In general, the transconductance gains of the VDTA can be controlled electronically by the external bias voltage/current.

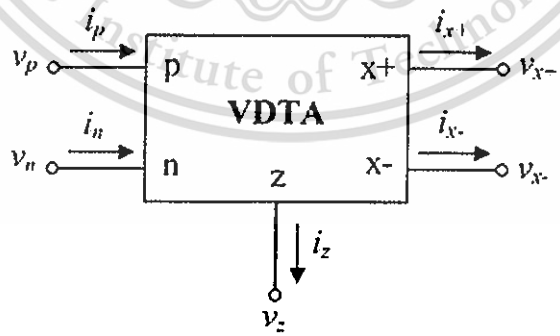


Figure 1. Electrical symbol of the VDTA.

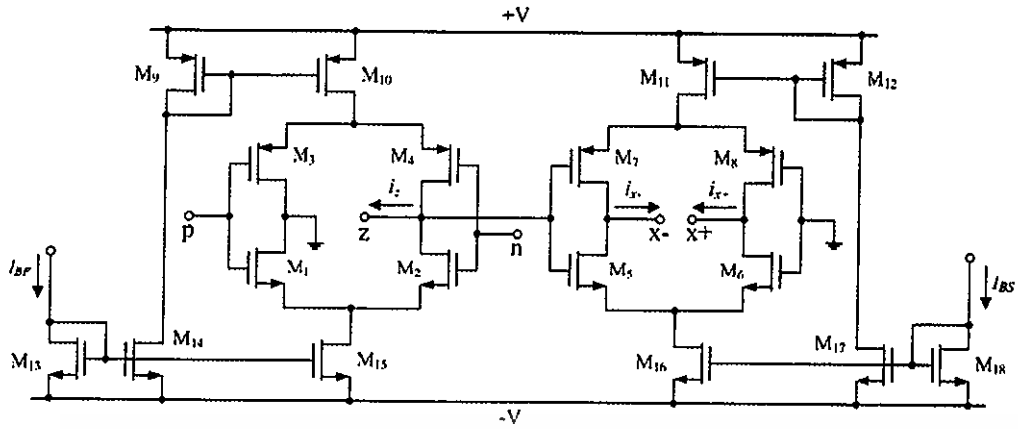


Figure 2. CMOS realization of the VDTA.

The simple CMOS realization of the VDTA is shown in Fig.2. In this case, the g_{mF}- and g_{mS}-values of this element are determined by the output transistor transconductance, which can respectively be approximated as :

$$g_{mF} \cong \left(\frac{g_1 g_2}{g_1 + g_2}\right) + \left(\frac{g_3 g_4}{g_3 + g_4}\right) \tag{2}$$

and

$$g_{mS} \cong \left(\frac{g_5 g_6}{g_5 + g_6}\right) + \left(\frac{g_7 g_8}{g_7 + g_8}\right), \tag{3}$$

where $g_i = \sqrt{I_{Bi}\mu C_{ox}\frac{W_i}{L_i}}$ is the transconductance value of the i-th transistor ($i = 1, 2, \ldots, 8$),

I_{Bi} is the bias current of the i-th transistor, μ is the effective carrier mobility, C_{ox} is the gate-oxide capacitance per unit area, and W and L are the effective channel width and length of the MOS M_i, respectively.

3. Proposed Floating FDNR Simulator Circuit

Fig.3 shows the proposed floating FDNR simulator circuit. This simulation contains only three VDTAs and two grounded that is beneficial from the fabrication point of view. The admittance matrix for the configuration of Fig.3 can be derived as the following expression :

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{s^2 C_1 C_2 g_{m1}}{g_{mF2} g_{m3}} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{4}$$

where $g_{m1} = g_{mF1}g_{mS1}$ and $g_{m3} = g_{mF3}g_{mS3}$. Thus, the circuit of Fig.3 realizes a floating FDNR with an equivalent floating admittance given by

$$Y_{eq} = s^2 D_{eq} = \frac{s^2 C_1 C_2 g_{m1}}{g_{mF2} g_{m3}} \tag{5}$$

where $$D_{eq} = \frac{C_1 C_2 g_{m1}}{g_{mF2} g_{m3}} \quad . \tag{6}$$

From eq.(5), it is easy to see that the value of the FDNR can be tuned by electronic means through either g_{mF} or g_{mS} of the VDTA. In addition, if we let $V_1 = 0$ or $V_2 = 0$, then the tunable grounded FDNR can easily be realized.

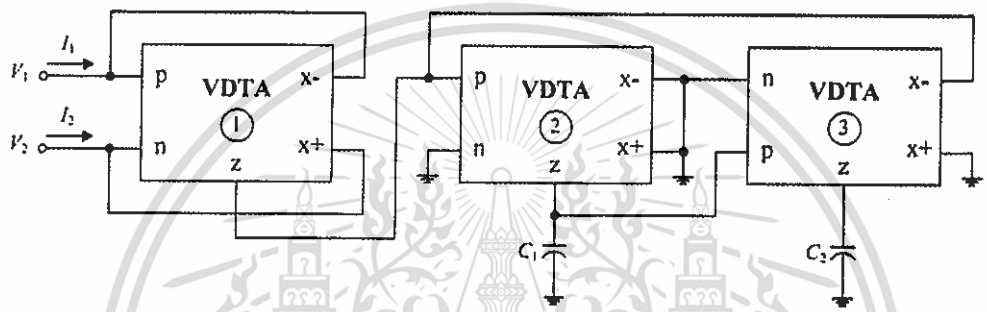


Figure 3. Proposed floating FDNR simulator circuit.

4. Simulation Results and Performance Verification

To evaluate the behavior of the proposed circuit in Fig.3, it is simulated using PSPICE simulation. In simulations, the VDTA was performed by the schematic CMOS implementation given in Fig.2 with supply voltages of +V = -V= 1.8 V. The CMOS transistors in VDTA implementation were simulated the 0.35 μm TSMC process parameters. The dimensions of MOS transistors are given in Table 1.

Table 1. Transistor aspect ratios of the VDTA given in Fig.2.

Transistors	W (μm)	L (μm)
$M_1 - M_2$, $M_5 - M_6$	16.1	0.7
$M_3 - M_4$, $M_7 - M_8$	28	0.7
$M_9 - M_{12}$, $M_{14} - M_{17}$	56	0.7
M_{13}, M_{18}	7	0.7

As an example, the component values were chosen as : $C_1 = C_2 = 1$ nF, $g_{mF1} = g_{mS1} = g_{mF2} = g_{mS2} \cong 0.60$ mA/V ($I_{BF1} = I_{BS1} = I_{BF2} = I_{BS2} = 100$ μA), and $g_{mF3} = g_{mS3} \cong 0.77$ mA/V ($I_{BF3} = I_{BS3} = 200$ μA), which results in $D_{eq} = 1$ fFs. Fig.4 shows the frequency response of the impedance of the proposed floating FDNR simulator circuit in Fig.3 relative to frequency. It can be observed that the circuit operates pretty well between 20 kHz and 2 MHz. To further demonstrate the

electronic tunability of the proposed FDNR, the simulator was also simulated by varying g_{mF3} ($= g_{mS3}$) $\cong$ 0.77 mA/V, 0.93 mA/V and 1 mA/V, to obtain D_{eq} = 1.00 fFs, 0.66 fFs, and 0.50 fFs, respectively. The frequency characteristics of the inductance simulator for various g_{mF3} values are shown in Fig.5. As depicted in both figures, the simulation results are in close agreement with the prediction, and confirm that the value of D_{eq} can be adjusted electronically by the transconductance gain of the VDTA.

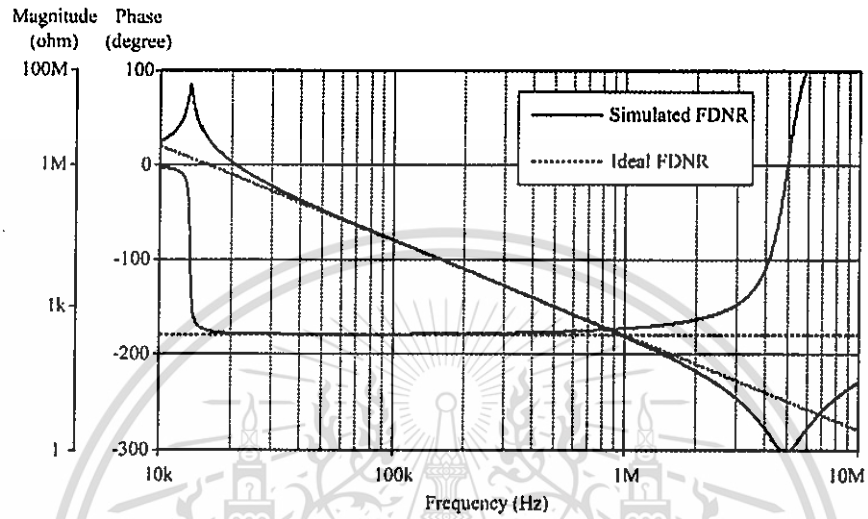


Figure 4. Magnitude and phase responses of the proposed FDNR in Fig.3.

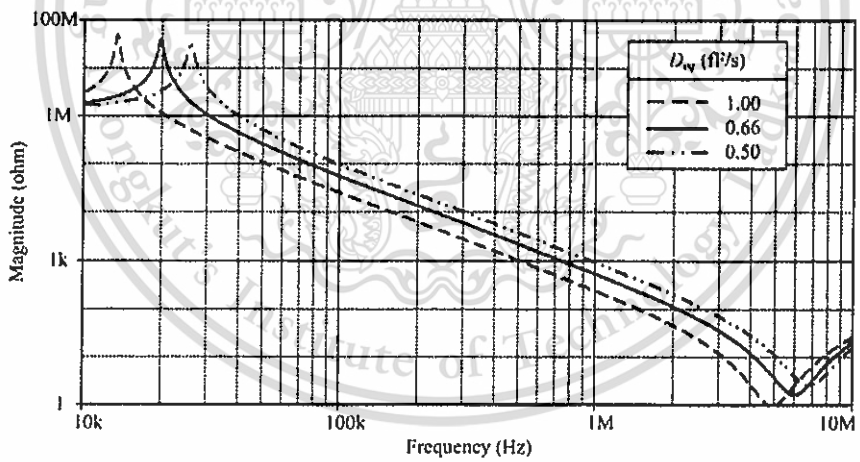


Figure 5. Electronic tuning of the D_{eq}-value of the proposed FDNR in Fig.3.

5. Application to Filter Realization

In this section, the proposed floating FDNR simulator in Fig.3 is used in the RLC fourth-order Butterworth bandpass filter prototype shown in Fig.6(a), where $R_1 = R_6 = 1\ \Omega$, $L_2 = 0.225\ \mu$H, $C_3 = 1.225\ \mu$F, $L_4 = 11.25\ \mu$H, $C_5 = 22.5$ nF [7]. This filter is designed to obtain fourth-order Butterworth characteristic whose bandwidth and center frequency are $BW = 32$ kHz and $f_o =$ 316 kHz respectively. By applying Bruton transformation and using magnitude scaling

constant ($k_m = 10^9$) and variable impedance scaling method, i.e. dividing the impedance of each element in the Fig.6(a) by k_m, the *RLC* passive filter is converted into *CRD* filter as shown in Fig.6(b) where all FDNRs are realized using the proposed circuit in Fig.3. In Fig.6(b), the resulting circuit components are obtained as : $C'_1 = 1$ nF, $R'_2 = 225\ \Omega$, $D'_3 = 11.25$ fFs, $R'_4 = 11.25$ kΩ, $D'_5 = 11.25$ aFs, and $C'_6 = 1$ nF. According to these component values, the voltage transfer function of the bandpass filter in Fig.6(b) is given by :

$$H(s) = \frac{(4.043\times10^{10})s^2}{s^4 + (2.843\times10^{5})s^3 + (7.925\times10^{12})s^2 + (1.121\times10^{18})s + (1.554\times10^{25})} \qquad (7)$$

The magnitude and phase characteristics of the filters are shown in Figs.7(a) and 7(b), respectively. From the figures, it appears that the theoretical and simulated results are in good agreement.

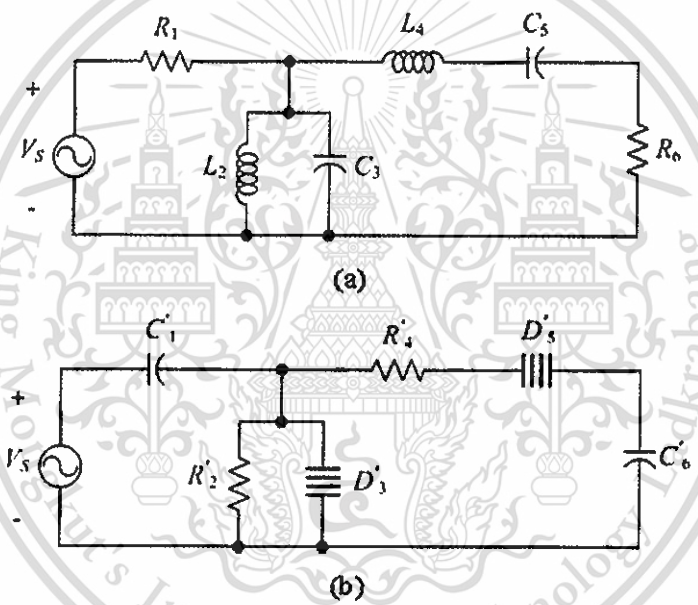
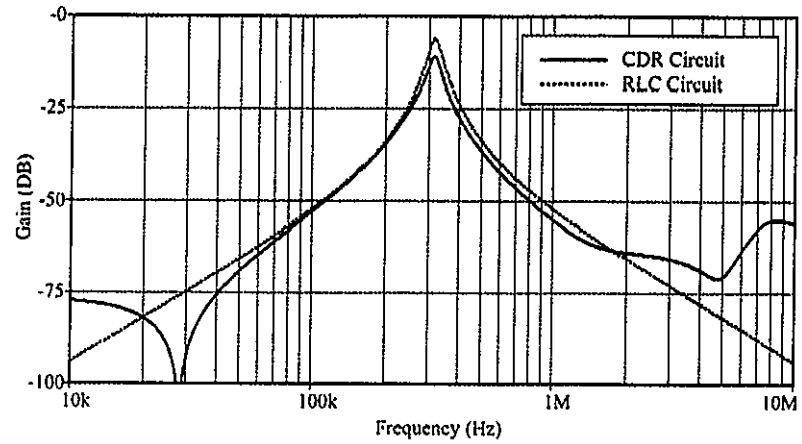
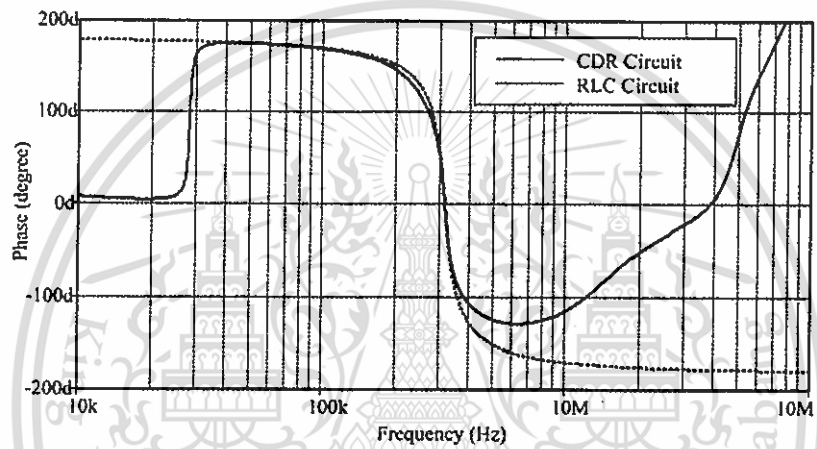


Figure 6. Fourth-order Butterworth bandpass filter.
(a) RLC passive prototype (b) equivalent CDR circuit with FDNRs.



(a)



(b)

Figure 7. Simulated frequency characteristic of the filter in Fig.6. (a) gain response (b) phase response.

6. Conclusions

This paper describes an electronically tunable floating FDNR simulator circuit based on the use of the voltage differencing transconductance amplifier (VDTA) and only two grounded capacitor. The important gain of floating FDNR simulator is that its value can be adjusted electronically by changing bias currents of the VDTAs. To demonstrate the performance of the proposed circuit, it is used to construct fourth-order Butterworth bandpass filter. PSPICE simulation results verify that the performances of the proposed circuit and its applications are in good agreement with the prediction of the analysis performed.

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Tunable Capacitance Multiplier with a Single Voltage Differencing Buffered Amplifier

Sumalee Unhavanich, Oosana Onjan, and Worapong Tangsrirat, *Member, IAENG*

Abstract—**This work describes the grounded electronically tunable capacitance multiplier circuit using voltage differencing buffered amplifier (VDBA) as an active element. The proposed capacitance simulator is simulated using one VDBA, one floating capacitor and one grounded resistor. The realized equivalent capacitance can be tuned electronically through the transconductance gain of the VDBA. The effect of the VDBA non-idealities on the realized equivalent capacitance has also been discussed in detail. As an application, active RC lowpass filter is realized using the proposed tunable capacitance simulator. PSPICE simulation results show a good agreement with the theoretical analysis, and verify the behaviors of the proposed simulator and its application.**

Keywords — **capacitance multiplier, Voltage Differencing Buffered Amplifier (VDBA), impedance simulator**

I. Introduction

A capacitance multiplier circuit is a useful active building block in many very large-scale integration (VLSI) analog circuits, especially for active RC filter and oscillator designs and cancellation of parasitic elements. This is well recognized that the large-valued physical capacitor is either not impractical or permitted to fabricate in the integrated circuit technology. Accordingly, the need for designs grounded capacitance multiplication topology with high equivalent integrated capacitance value is important for VLSI implementation point of view. Many capacitance multiplier circuit realizations employing more than two active elements were introduced [1]-[8]. In view of low power consumption and small silicon area on the chip, it is preferable to realize the simulator with a minimum number of active and passive components. Nowadays, modern electronic active building blocks are gaining importance in analog signal processing applications and designs. In [9], modern day active components have been reviewed and discussed. One of them is the circuit principle called as VDBA (voltage differencing buffered amplifier). Its several applications, such as active filters, sinusoidal oscillators and immittance function simulators, were also introduced to demonstrate its usefulness and versatile [10]-[13].

In this work, we largely consider a grounded capacitance simulator realization using one VDBA as active components together with one floating capacitor and one grounded resistor as passive components. The equivalent capacitance value (C_{eq}) of the proposed simulation scheme can be controlled electronically through the transconductance parameter (g_m) of the VDBA. The behavior of the proposed capacitance simulator was evaluated through the PSPICE simulation. A first-order RC lowpass filter using the proposed circuit was also simulated.

II. Voltage Differencing Buffered Amplifier (VDBA)

The schematic symbol of the VDBA is shown in Fig.1. Basically, the VDBA device consists of the transconductance amplifier as an input stage, and the unity-gain voltage buffer as an output stage. Thus, the basic operation of this device can be characterized by the following equations [9]-[10] :

$$i_p = i_n = 0, \quad i_z = g_m(v_p - v_n) \quad \text{and} \quad v_w = v_z \qquad (1)$$

where g_m is the small-signal transconductance gain of the VDBA. Generally, the g_m-value is electronically controllable over several decades by a supplied bias current/voltage, which lends electronic tunability to design circuit parameters. From eq.(1), the differential input voltage between the terminals p and n (v_p-v_n) is converted to a current at the z-terminal (i_z) by a g_m-parameter. The voltage across the z-terminal (v_z) is then conveyed to the output voltage at the w-terminal (v_w).

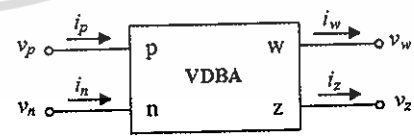

Fig. 1. Schematic symbol of the VDBA.

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III. Description of The Proposed Capacitance Multiplier

The proposed capacitance multiplier circuit is shown in Fig.2. It employs only one VDBA, one capacitor floating C_1, and one grounded resistor R_1. Using eq.(1) and deriving the proposed circuit of Fig.2, its input impedance Z_{in} is realized of value :

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{s(1+g_m R_1)C_1} = \frac{1}{sC_{eq}} \qquad (2)$$

It can easily be realized that the proposed circuit of Fig.2 simulates a grounded capacitance with its equivalent value :

$$C_{eq} = (1+g_m R_1)C_1 \qquad (3)$$

From above expression, it is relevant to note that an external capacitor C_1 has to be multiplied by the resistance R_1 and transconductance g_m. Since the g_m-value usually depends on the biasing current of the VDBA, the realized C_{eq} is electronic programmability.

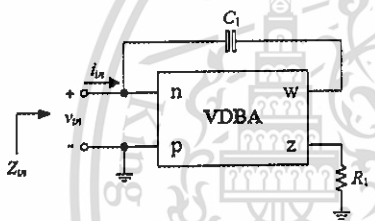

Fig. 2. Proposed tunable capacitance multiplier circuit.

IV. Tracking Error Analysis

The non-ideal relations for the VDBA can be described as :

$$i_p = i_n = 0, \quad i_z = \alpha g_m (v_p - v_n) \quad \text{and} \quad v_w = \beta v_z \qquad (4)$$

where $\alpha = (1 - \varepsilon_{gm})$ and $\beta = (1 - \varepsilon_v)$. Also, $|\varepsilon_{gm}| << 1$ denotes the transconductance inaccuracy, and $|\varepsilon_v| << 1$ denote the voltage tracking error from terminal z to terminal w, respectively. Considering the VDBA non-idealities in the proposed circuit of Fig.2, and solving for C_{eq} will obtain :

$$C_{eq} = (1+\alpha\beta g_m R_1)C_1 \qquad (5)$$

It should be noted that the non-ideal transfer gains of the VDBA have slightly effect on the realized C_{eq}. However, this small discrepancy can be compensated by appropriately tuning the transconductance parameter g_m of the VDBA.

V. Simulation Results and Example

The performance of the proposed circuit of Fig.2 has been simulated by PSPICE program. For simulations, the bipolar realization of the VDBA given in Fig.3 [12] has been employed using the typical parameters bipolar transistor model PR100N (PNP) and NP100N (NPN). The DC supply voltages and bias currents were chosen as : +V = -V = 1.5V and I_Q = 50 μA, respectively. In this structure, the small-signal transconductance gain (g_m) is approximated to :

$$g_m = \frac{I_O}{2V_T} \qquad (6)$$

where V_T is the thermal voltage that is equal to 26 mV at 27°C.

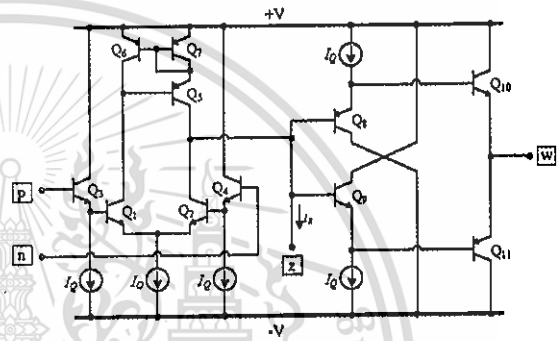

Fig. 3. Bipolar realization of the VDBA used in simulations [12].

As an example, the proposed capacitance multiplier of Fig.2 is realized with the following component values : I_O = 50 μA (g_m = 0.96 mA/V), R_1 = 10 kΩ and C_1 = 0.1 nF. The simulated time waveforms of v_{in} and i_{in} through the capacitance simulator are shown in Fig.4, where the frequency of v_{in} is f = 100 kHz. As expected, the results indicate that the current i_{in} leads the voltage v_{in} by approximately 90°. The total power consumption is found as : 0.89 mW.

The simulated frequency characteristics for the input impedance Z_{in} of the proposed tunable capacitance multiplier circuit of Fig.2 comparing with the theoretical responses are shown in Fig.5. The following passive component values : R_1 = 10 kΩ and C_1 = 0.1 nF are selected, and the external DC bias current (I_O) of the VDBA is varied from 20 μA, 50 μA, 250 μA to 520 μA, which result in g_m = 0.4 mA/V, 1 mA/V, 5 mA/V and 10 mA/V, respectively. By setting these parameters, the realized equivalent capacitance C_{eq} can be obtained as : 0.5 nF, 1 nF, 5 nF and 10 nF. The resulting characteristics show that the proposed circuit works pretty well between 100 Hz and 100 kHz approximately. Also from Fig.5, it is proven that the circuit can exhibit an electronically tunable capacitance over a wide range by adjusting the g_m-value of the VDBA.

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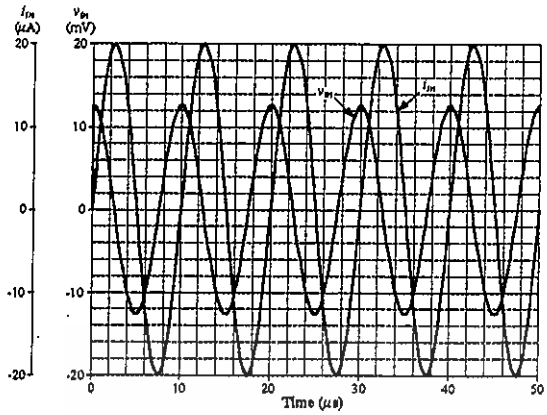

Fig. 4. Simulated time-domain responses for v_{in} and i_{in} of the proposed capacitance multiplier in Fig.2.

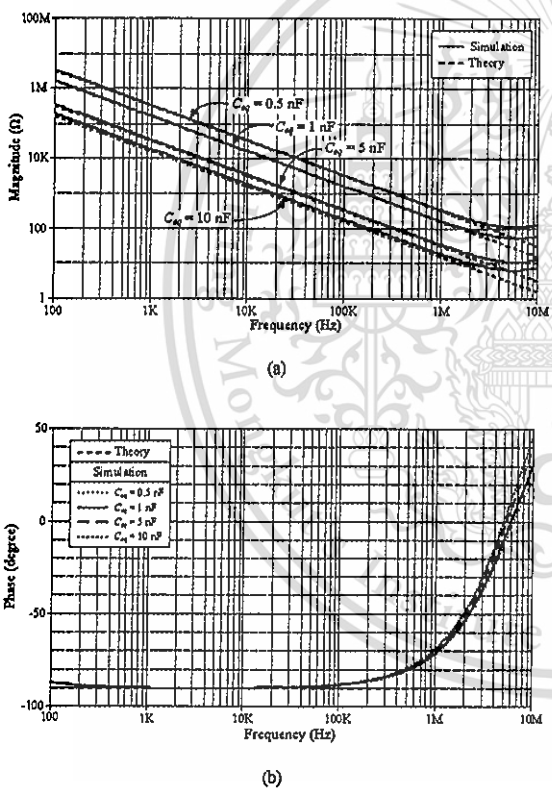

Fig. 5. Simulated frequency characteristics for Z_{in} of the proposed capacitance multiplier in Fig.2.

(a) magnitude responses (b) phase responses

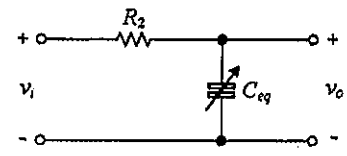

Fig. 6. Active RC first-order lowpass filter.

As an application example, the proposed capacitance simulator in Fig.2 is utilized in the implementation of an active RC lowpass filter shown in Fig.6. The cut-off frequency ($f_c = \omega_c/2\pi$) of the circuit can be obtained as :

$$\omega_c = \frac{1}{R_2 C_{eq}} \tag{7}$$

Since the value of C_{eq} can be controlled with the external biasing current, the cut-off frequency (f_c) is electronically tunable. In addition to take the effect of the VDBA non-idealities into account, eq.(7) turns to

$$\omega_c = \frac{1}{(1+\alpha\beta g_m R_1) R_2 C_1} \tag{8}$$

The sensitivities of ω_c with respect to the active and passive components can be found as :

$$S_{\alpha}^{\omega_c} = S_{\beta}^{\omega_c} = S_{g_m}^{\omega_c} = S_{R_1}^{\omega_c} = -\frac{\alpha\beta g_m R_1}{1+\alpha\beta g_m R_1} \tag{9}$$

and

$$S_{R_2}^{\omega_c} = S_{C_1}^{\omega_c} = -1 \tag{10}$$

From the above expressions, the circuit sensitivities are very small, since all of which are less than unity in absolute value.

To demonstrate the performance of an illustrative lowpass filter in Fig.6, the component values are selected as follows : R_1 = 10 kΩ, C_1 = 0.1 nF, R_2 = 1 kΩ and C_{eq} = 10 nF, 5 nF, 1 nF and 0.5 nF, respectively. This results in f_c = 15.9 kHz, 31.8 kHz, 159 kHz and 318 kHz, respectively. Fig.7 shows the theory and simulated frequency responses of the active RC lowpass filter in Fig.6 with the proposed electronically tunable C_{eq}. The corresponding f_c obtained from the simulated results are approximated to : 18.4 kHz, 34.1 kHz, 154 kHz and 294 kHz, respectively. As a result, the corresponding errors for f_c are -15.69%, -8.01%, 2.91% and 7.37%. The results of the circuit simulations are close to the theoretical one as expected.

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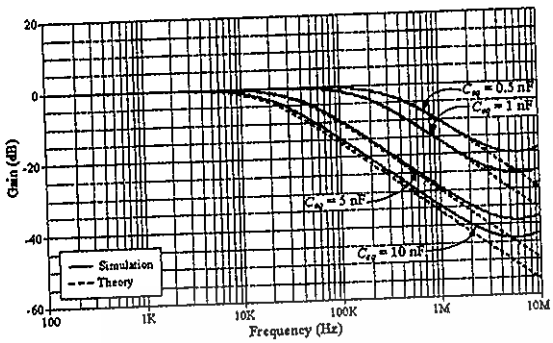
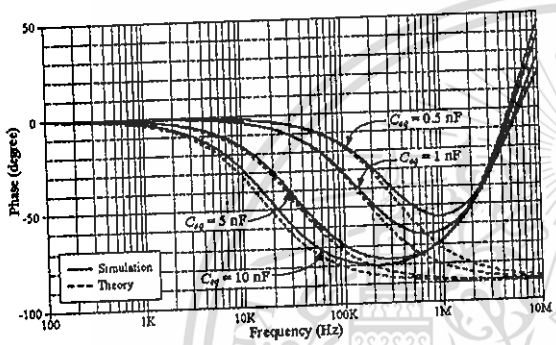


(a)



(b)

Fig. 7. Simulated frequency responses of the active first-order RC lowpass filter of Fig.6.

(a) gain responses (b) phase responses

VI. Conclusion

In this study, an electronically tunable capacitance multiplier based on using VDBA is proposed. The proposed capacitance simulator is designed with a single VDBA and only two passive components. The equivalent capacitance of the realized simulator can be tuned electronically by adjusting the transconductance parameter g_m of the VDBA. The proposed capacitance simulator contains a minimum number of components and exhibits very low various sensitivities. The proposed circuit is used to construct the active RC lowpass filter example and the simulation results are used to display the workability of the circuits.

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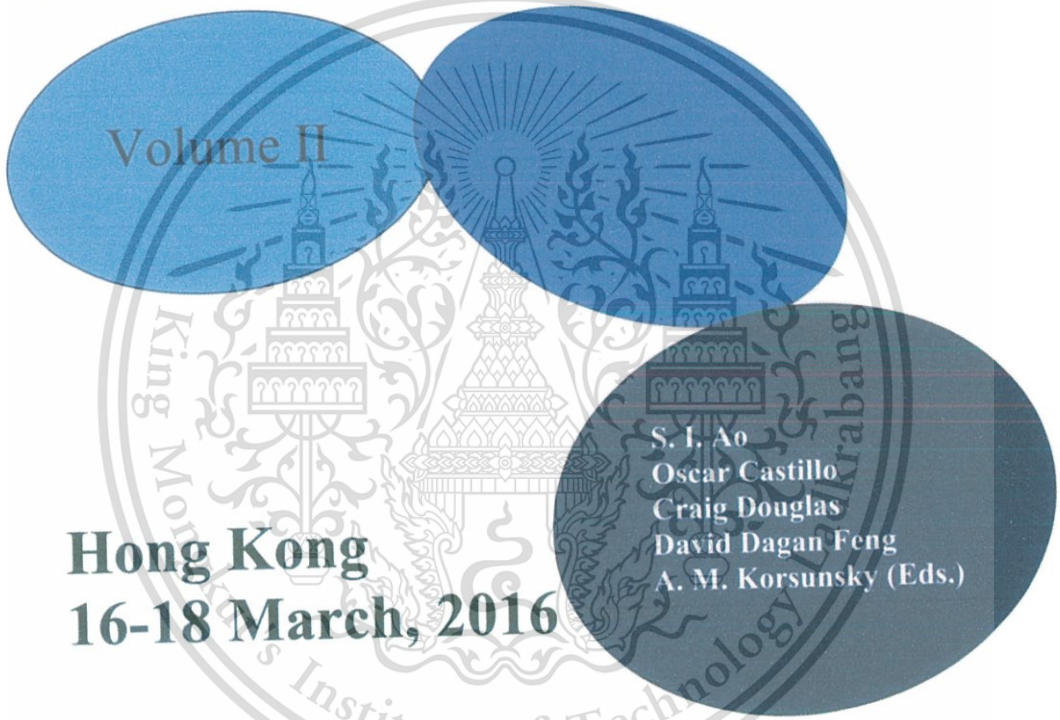

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SFG Actualization of General nth-Order Voltage Transfer Functions Using VDBAs

Oosana Onjan, Sumalee Unhavanich, and Worapong Tangsrirat, *Member, IAENG*

***Abstract*—This work presents the synthesis of general nth-order voltage transfer functions with voltage differencing buffered amplifiers (VDBAs) using signal flow graph (SFG) technique. Without the employment of external passive resistors, the designed procedure requires only *n* VDBAs and *n* capacitors for nth-order transfer function realization. As application examples, the first-order allpass and standard biquadratic function realizations are demonstrated. The simulation results by PSPICE have also been provided, which verify the usefulness of the presented technique.**

***Keywords* — Signal Flow Graph (SFG), Voltage Differencing Buffered Amplifier (VDBA), universal filter**

I. Introduction

RECENTLY, analog active building blocks were developed and invented continuously. Among these, the voltage differencing buffered amplifier (VDBA) is the newly defined active circuit building block [1]. This device is slightly modified from the conventional current differencing buffered amplifier (CDBA) by replacing the current differencing unit with a transconductance amplifier [2]. The difference between VDBA and CDBA is that the VDBA inputs are voltages as for the CDBA inputs are currents. Many applications based on the use of the VDBAs as active elements in analog signal processing area have also been developed in the literature [3]-[7]. In addition, the works of [8]-[17] have proposed the actively circuit realizations of an nth-order voltage transfer function synthesis based on the signal-flow-graph (SFG) approach employing various active elements. However, all the available SFG circuit realizations employ an excessive number of active and passive elements, at least *n* active devices, *n* resistors and *n* capacitors.

Considering this fact, the work described in this paper mainly focuses on presenting a general synthesis procedure for realizing general nth-order voltage transfer functions. The proposed method is based on drawing a SFG directly from the given transfer function and then obtaining, from the graph, the active-C circuit configurations involving VDBAs. The resulting circuit uses only *n* VDBAs and *n* capacitors without needing any external passive resistors for nth-order transfer function realization. It has been shown that the design procedure proposed here is a canonical number of active and passive elements. Two illustrative examples together with PSPICE simulation results illustrate the usefulness of the proposed design procedure.

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II. Voltage Differencing Buffered Amplifier (VDBA)

The VDBA symbol is shown in Fig. 1. The relative characteristic between current and voltage of this device can be described by the following matrix [18]:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ v_{w+} \\ v_{w-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_{w+} \\ i_{w-} \end{bmatrix} \quad (1)$$

where g_m is the transconductance gain of the VDBA. According to eq.(1), the differential input voltage between the terminals p and n (v_p- v_n) is then converted to a current at the z-terminal (i_z) by a g_m-parameter. The output voltages at terminals w+ (v_{w+}) and w- (v_{w-}) follow the voltage across the z-terminal (v_z). The voltages v_{w+} and v_{w-} will be of equal magnitude but different phases.

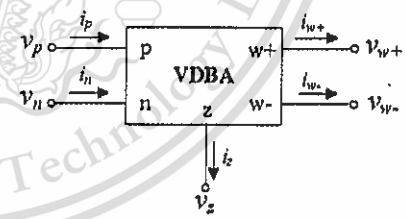

Fig. 1. Circuit symbol of the VDBA.

III. SFG Actualization Procedure

The general form of an nth-order voltage transfer function can be expressed by the following equation:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{b_n s^n \pm b_{n-1}s^{n-1} \pm \cdots \pm b_2 s^2 \pm b_1 s + 1}{b_n s^n + b_{n-1}s^{n-1} + \cdots + b_2 s^2 + b_1 s + 1} \quad (2)$$

where V_{in} and V_{out} are the input and the output voltages, respectively. The above equation can be represented by the SFG of Fig. 2. It can be observed that the graph is mainly

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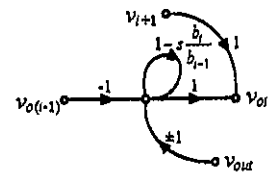
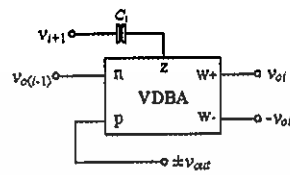
composed of the cascading connection of the sub-graph shown in Fig. 3(a). Each sub-graph performs the lossless integrator, and its corresponding active-C sub-circuit involving VDBA is shown in Fig. 3(b). Therefore, according to Fig. 2 and 3, the resulting VDBA-based circuit can be realized in Fig. 4. It is important to note that the proposed technique requires only n VDBAs and n capacitors for realizing n^{th}-order transfer function.



(a)



where $\frac{b_i}{b_{i-1}} = \frac{C_i}{g_{mi}}$ and $i = 1, 2, 3, \ldots, n$

(b)

Fig. 3. Sub-graph of Fig. 2 and its corresponding VDBA-based circuit.

$$b_1 = \frac{C_1}{g_{m1}}$$

$$\frac{b_2}{b_1} = \frac{C_2}{g_{m2}}$$

$$\vdots$$

$$\frac{b_{n-1}}{b_{n-2}} = \frac{C_{n-1}}{g_{m(n-1)}}$$

and

$$\frac{b_n}{b_{n-1}} = \frac{C_n}{g_{m(n)}} \quad (3)$$

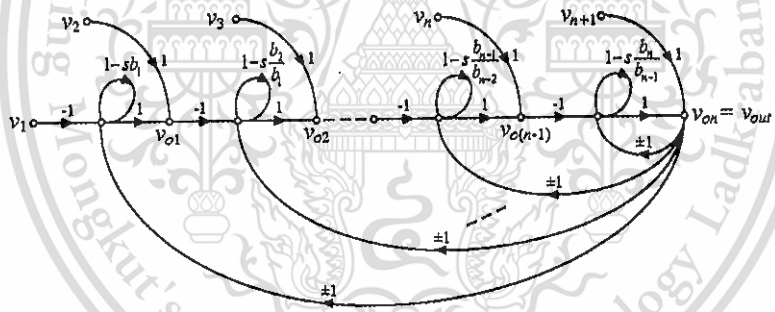


Fig. 2. Signal flow graph representation of eq. (2).

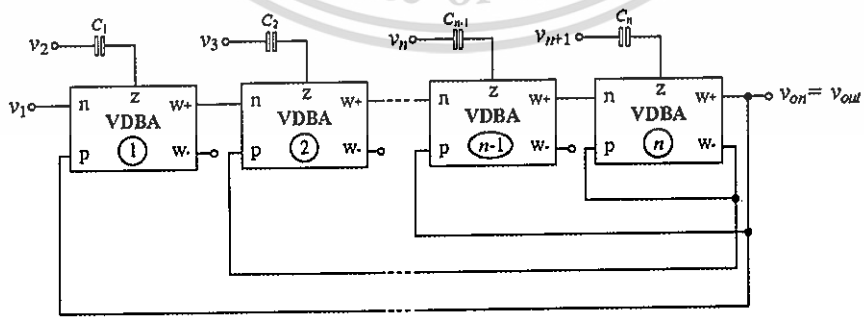


Fig. 4. The realization of n^{th}-order universal voltage transfer functions of eq. (2) using VDBAs.

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IV. Illustrative Examples

The utility of the proposed procedure will be demonstrated by the two following examples:

A. First-order allpass realization

The transfer function of the first-order allpass filtering function can be defined by the following equation:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{sb_1 - 1}{sb_1 + 1} \tag{4}$$

where $b_1 = C_1/g_{m1}$.

The SFG representation of eq. (4) can be given in Fig. 5(a), and its corresponding VDBA-C circuit realization can then be obtained as Fig. 5(b). As can be observed, the realized circuit consists of only one VDBA and one capacitor. In this case, the pole frequency (ω_p) and phase shift (ϕ) of the circuit are obtained as:

$$\omega_p = 2\pi f_p = \frac{g_{m1}}{C_1} \tag{5}$$

and

$$\phi = \pi - 2\tan^{-1}\left(\frac{\omega C_1}{g_{m1}}\right). \tag{6}$$

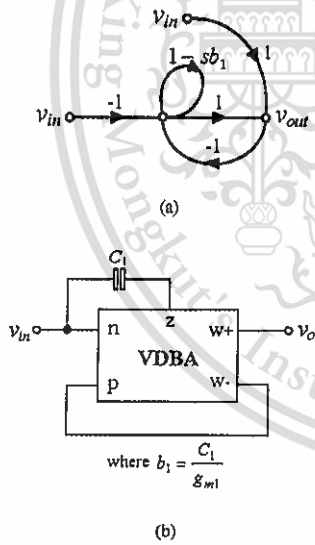

Fig. 5. SFG realization of the first-order allpass function.

B. Second-order universal functions

The general form of the standard second-order voltage transfer functions can be given by the following expression:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{b_2 s^2 - b_1 s + 1}{b_2 s^2 + b_1 s + 1}. \tag{7}$$

The above expression can be represented by SFG diagram as shown in Fig. 6(a), and its realization involving VDBA-C can be shown in Fig. 6(b). In this case, two VDBAs and two capacitors are required. As a result of eq. (7), the voltage transfer function of Fig. 6(b) in term of the circuit component values can be written as:

$$V_{out}(s) = \frac{s^2 V_3 - \left(\frac{g_{m2}}{C_2}\right) s V_2 + \left(\frac{g_{m1} g_{m2}}{C_1 C_2}\right) V_1}{s^2 + \left(\frac{g_{m2}}{C_2}\right) s + \left(\frac{g_{m1} g_{m2}}{C_1 C_2}\right)} \tag{8}$$

where g_{mi} are the transconductance gain of the i-th VDBA (i = 1, 2). According to eq. (8), the standard second-order voltage transfer functions can be realized by the following conditions.

1) The lowpass (LP) function is realized, if $V_1 = V_{in}$ and $V_2 = V_3 = 0$.
2) The highpass (HP) function is realized, if $V_3 = V_{in}$ and $V_1 = V_2 = 0$.
3) The bandpass (BP) function is realized, if $V_2 = V_{in}$ and $V_1 = V_3 = 0$.
4) The bandstop (BS) function is realized, if $V_2 = 0$ and $V_1 = V_3 = V_{in}$.
5) The allpass (AP) function is realized, if $V_1 = V_2 = V_3 = V_{in}$.

Also from eq. (8), the pole frequency (ω_p), and the quality factor (Q) of circuit can be given by:

$$\omega_p = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \tag{9}$$

and

$$Q = \sqrt{\frac{g_{m1} C_2}{g_{m2} C_1}} \tag{10}$$

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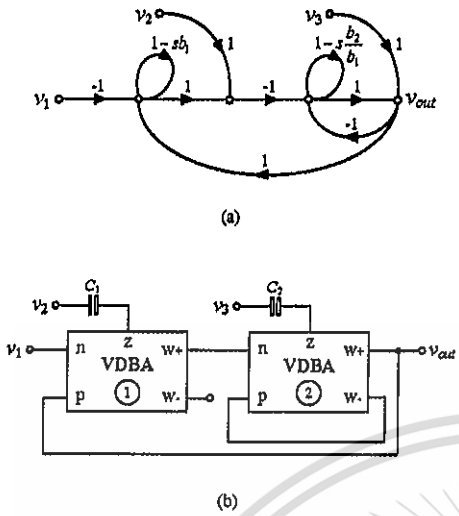

Fig. 6. Realization of the second-order universal filtering functions using SFG.
(a) SFG representation (b) circuit realization

To obtain the first-order allpass voltage response with the pole frequency of $f_p \cong 766$ kHz. The circuit was designed with the following active and passive components: $I_{B1} = 25\ \mu A$ ($g_{m1} \cong 0.96$ mA/V) and $C_1 = 0.2$ nF. Fig. 8 shows the ideal and simulated frequency characteristics of the first-order allpass filter realization of Fig. 5. The time domain responses are also shown in Fig.9, where the phase shift is recorded to be 84°.

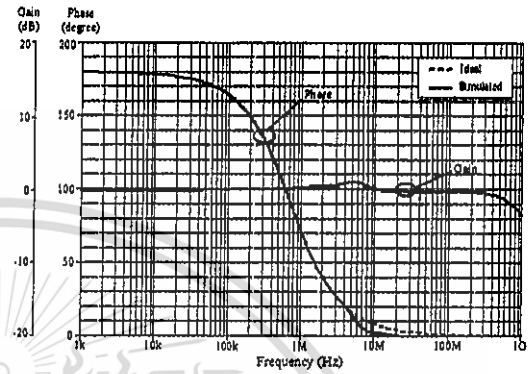

Fig. 8. Frequency response of the first-order allpass filter in Fig.5.

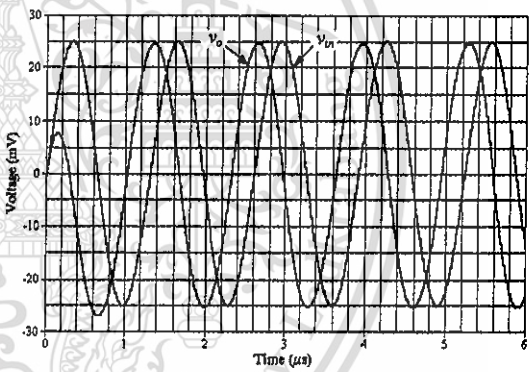

Fig. 9. Time domain responses of the first-order allpass filter in Fig. 5

V. Simulation Results

To verify the feasibility of the designed procedure, the realized circuits have been simulated with PSPICE program. In simulations, the BiCMOS VDBA shown in Fig. 7 has been performed with the standard 0.35-μm BiCMOS technology [18]. The transistors sizes were chosen as: 14/0.7 and 28/0.7 for all NMOS and PMOS transistors, respectively. The supply voltages were V = ±0.75 V, and biasing currents were $I_A = 25\ \mu A$. The small-signal effective transconductance (g_m) of the VDBA in Fig. 7 is given by:

$$g_m = \frac{I_B}{V_T} \tag{11}$$

where $V_T \cong 26$ mV at 27 °C is the thermal voltage, and I_B is the external DC bias current.

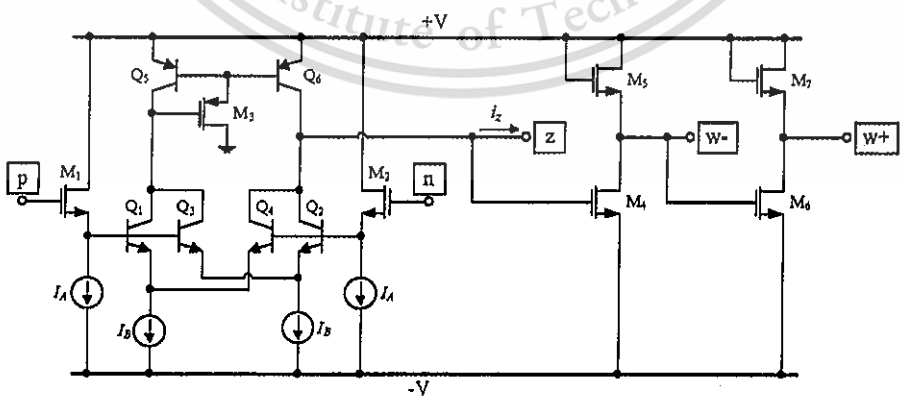

Fig. 7. BiCMOS realization of the VDBA.

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The ideal and simulated frequency responses of the second-order universal biquadratic filter in Fig. 6(b) are shown in Figs. 10 and 11. The results are obtained with $I_{B1} = I_{B2} = 38\ \mu A$ ($g_{m1} = g_{m2} \cong 1.414$ mA/V) and $C_1 = C_2 = 1$ nF. This results in $f_p = 255$ kHz and $Q = 1$. From the results, the locations of the simulated f_p are about: 215.29 kHz, 219.92 kHz, 217.30 kHz, and 213.98 kHz for LP, HP, BS, and BP responses, which correspond to the following absolute errors: 4.33%, 3.28%, 3.38%, and 4.92%, respectively.

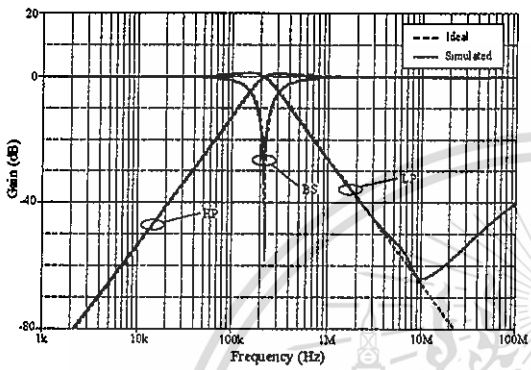

Fig. 10. Frequency characteristics for the LP, HP, and BS responses of Fig. 6(b).

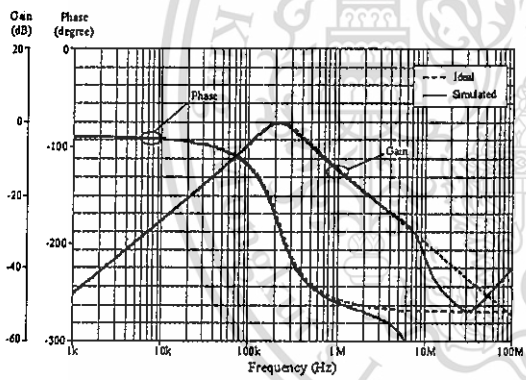

Fig. 11. BP frequency response of Fig. 6(b).

VI. Conclusion

This work has been presented the SFG actualization of n[th]-order general voltage transfer functions using n VDBAs and n capacitors. The proposed circuit is canonic in a number of active and passive components and enjoys the ability of electronic tuning. Applications on the first- and second-order filtering function realizations have been provided, which verify the utility of the proposed procedure.

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Simple Realization of BiCMOS Current-Controlled Conveyor Transconductance Amplifier (CCCTA)

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Abstract

In this paper, the simple realization of the current-controlled conveyor transconductance amplifier (CCCTA) in BiCMOS technology is introduced. The proposed BiCMOS CCCTA provides the advantages of low-voltage operation, wide dynamic range, and simple circuit structure. Its characteristics, i.e. parasitic resistance and current transfer, are also tunable electronically by external bias currents. The realized circuit is suitable for fabrication using standard 0.35 μm BiCMOS technology. PSPICE simulation results demonstrating the circuit characteristic are performed.

Keyword: Current-Controlled Conveyor Transconductance Amplifier (CCCTA), BiCMOS technology, analog signal processing

1. Introduction

Since an introduction of the newly defined active building block namely, the current conveyor transconductance amplifier (CCTA) in 2005 [1], this device has been gaining an increasing attention that led to a number of analog function circuits. Basically, the CCTA device can be realized by cascading the second-generation current conveyor with the multi-output transconductance amplifier in monolithic form. By combining the advantages of both circuit technologies, the CCTA possesses wide bandwidth, high-slew rate, high dynamic range, and low power consumption. For these reasons, the CCTA is suitable for a class of analog signal processing which can process in both current and voltage signals. Hence, a great number of numerous analog adjustable functions is available in open literature [1]-[3].

In 2008, the current-controlled conveyor transconductance amplifier (CCCTA) which is a modified version of the CCTA, was introduced in bipolar technology [4]. Since its introduction, the CCCTA has been widely used in applications for continuous-time signal processing.

The parasitic resistance looking into the x-terminal (R_x) of the circuit is used to advantage in current-controlled circuit parameter, since it is easily adjusted by an external biasing current. This advantage allows the implementation of numerous electronically tunable functions.

In recent integrated circuit technology, there are two basic technologies that are known as bipolar and CMOS technologies. For the bipolar transistor technology, they have higher transconductance gain (g_m), low-noise performance and better high-frequency performance that their CMOS counterparts [5]. On the other hand, the advantage of the CMOS technology includes high-input impedance level, low power dissipation and small chip area. The circuit realized in BiCMOS technology will therefore provide the advantages of both technologies.

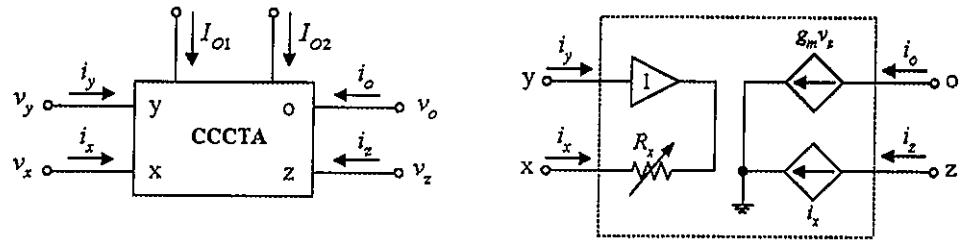
The aim of this work is to realize a current-controlled conveyor transconductance amplifier (CCCTA) structure suitable for integration in BiCMOS technology. The proposed CCCTA is simple structure and capable of operate at low voltage of ±1V, as well as has a wide bandwidth. The characteristics of the proposed CCCTA are demonstrated by PSPICE simulation results using 0.35-μm BiCMOS real process parameters. The results show good agreement with the expected values.

2. Basic Concept of the CCCTA

Basically, the CCCTA is a conceptually combination of second generation current-controlled conveyor (CCCII) and transconductance amplifier. Its electrical symbol and equivalent circuit can be shown in Fig.1. As shown, the CCCTA device consists of two input terminals (y and x) and two output terminals (z and o). The x-terminal is a low-input impedance terminal while the y-terminal is the high-input impedance terminal. The z and o-terminals are two types of high-output impedance terminals. The property of the CCCTA can be described by the following matrix :

$$\begin{bmatrix} i_y \\ v_x \\ i_z \\ i_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ R_x & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & g_m & 0 \end{bmatrix} \begin{bmatrix} i_x \\ v_y \\ v_z \\ v_o \end{bmatrix} \qquad (1)$$

where R_x and g_m are the finite parasitic resistance looking into the x-terminal, and the transconductance gain of the CCCTA, respectively. Here, R_x and g_m depend on the external DC bias currents I_{O1} and I_{O2}, respectively.



(a) (b)

Figure 1. CCCTA (a) circuit symbol (b) its equivalent circuit

3. Proposed BiCMOS CCCTA Realization

The schematic BiCMOS realization of the proposed CCCTA is shown in Fig.2. The circuit mainly consists of second-generation current-controlled conveyor (CCCII) and transconductance amplifier. It is designed by combining bipolar and CMOS technologies in order to utilize the main advantages of each technology, i.e., higher transconductance, higher frequency, low power consumption, and small silicon area. The groups of transistors Q_1-Q_2 and Q_3-Q_4, which are assumed to be well matched, act as transconductance amplifiers to convert the voltage signal to the current signal. The current mirroring has been achieved by simple current mirror circuits (M_5-M_7), (M_8-M_9), (M_{10}-M_{12}) and (M_{13}-M_{14}). Mirroring actions between M_5 and M_6, and M_8 and M_9 force equal bias current in Q_1 and Q_2, and Q_3 and Q_4, respectively. By applying the translinear principle to the base-emitter voltages (v_{BE}) of Q_1 and Q_2, the differential input voltage (v_y-v_x) can be derived as :

$$v_y - v_x = v_{BE1} - v_{BE2} = V_T \left(\ln \frac{i_{C1}}{I_S} - \ln \frac{i_{C2}}{I_S} \right) \qquad (2)$$

where $V_T \cong 26$ mV at 27°C is the thermal voltage, I_S is the reverse saturation current, and i_{C1} and i_{C2} are respectively the collector currents of transistors Q_1 and Q_2.

As shown in Fig.2, the relationship of the current flowing through the x-terminal (i_x) is equal to :

$$i_x = i_{C2} - i_{C1} \qquad (3)$$

where
$$i_{C1} = \frac{I_{O1}}{1 + e^{-(v_y - v_x)/V_T}} \qquad (4)$$

and
$$i_{C2} = \frac{I_{O1}}{1 + e^{(v_y - v_x)/V_T}} \quad . \qquad (5)$$

Substituting eqs.(4) and (5) into (3), the current i_x can be rewritten as :

$$i_x = I_{O1} \tanh\left(\frac{v_x - v_y}{2V_T}\right) \tag{6}$$

To simplifying, if we assume that $(v_x\text{-}v_y) << 2V_T$, then the term $\tanh(v_x\text{-}v_y/2V_T)$ can be approximately reduced to $(v_x\text{-}v_y/2V_T)$. Hence, eq.(6) can also be given by :

$$i_x \cong I_{O1}\left(\frac{v_x - v_y}{2V_T}\right) \tag{7}$$

From above expression, when the y-terminal is connected to ground, the parasitic resistance looking into the x-terminal (R_x) of the CCCTA has been derived as :

$$R_x \cong \frac{2V_T}{I_{O1}} \tag{8}$$

It should be noted from eq.(7) that the resistance R_x is controllable electronically by adjusting the bias current I_{O1}.

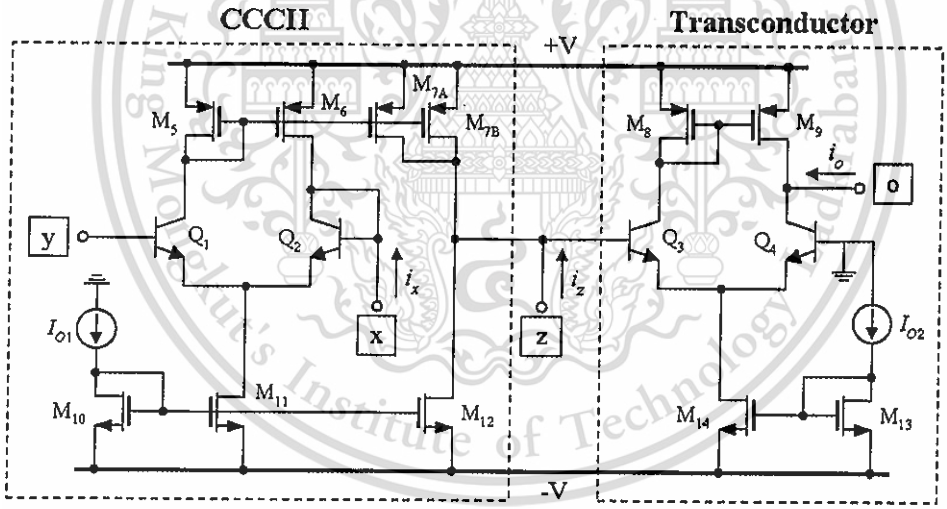


Figure 2. BiCMOS realization of the proposed CCCTA.

Similarly, the small-signal transconductance gain (g_m) of the CCCTA derived from the transconductor Q_3-Q_4 can be expressed as :

$$g_m = \frac{i_o}{v_z} = \frac{I_{O2}}{2V_T} \tag{9}$$

Also note that the g_m-value can be controlled electronically by changing the I_{O2}–value.

4. Simulation Results

To verify the theoretical analysis, the proposed CCCTA structure in Fig.2 has been simulated with PSPICE using standard 0.35-μm BiCMOS process parameters. The circuit was biased with ±1V supply voltages. The transistor aspect ratios (W/L in μm/μm) were chosen as : 7/0.7 and 8.5/0.7 for all the PMOS and NMOS transistors respectively.

In Fig.3, the theoretical and simulated values of the parasitic resistance R_x of the proposed CCCTA against the biasing current I_{O1} are plotted. In the plots, the biasing current I_{O1} was adjusted from 5 **μA to 300 μA**. As shown, the simulated results agree well with the theory. Fig.4 shows the current transfer characteristic from x-terminal to z-terminal as a function of frequency. It can be observed that the bandwidth of the current transfer i_z/i_x has a constant value of about 20 MHz.

The simulated frequency response of the transconductance gain g_m characteristic for three different values of I_{O2}, i.e. I_{O2} = 50 μA, 100 μA and 150 μA, are depicted in Fig.5. The results indicate that the bandwidth in order of megahertz is achieved.

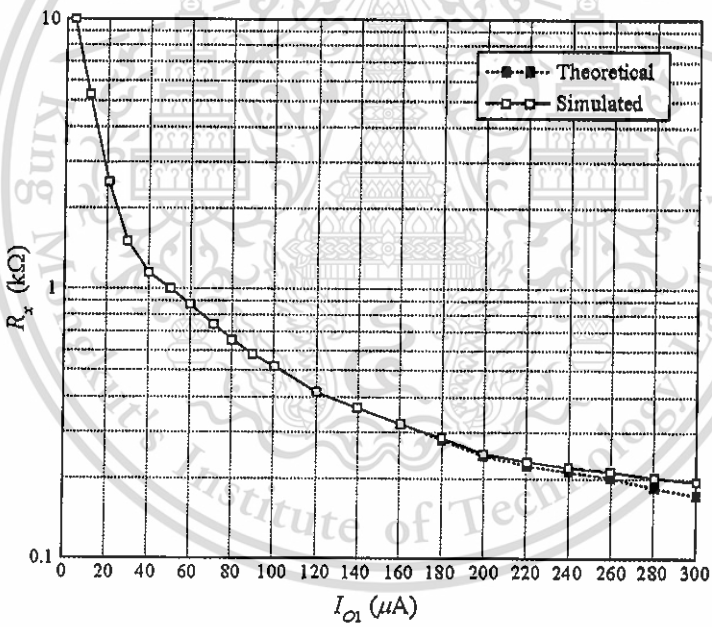


Figure 3. The theoretical and simulated variations of R_x as a function of I_{O1}.

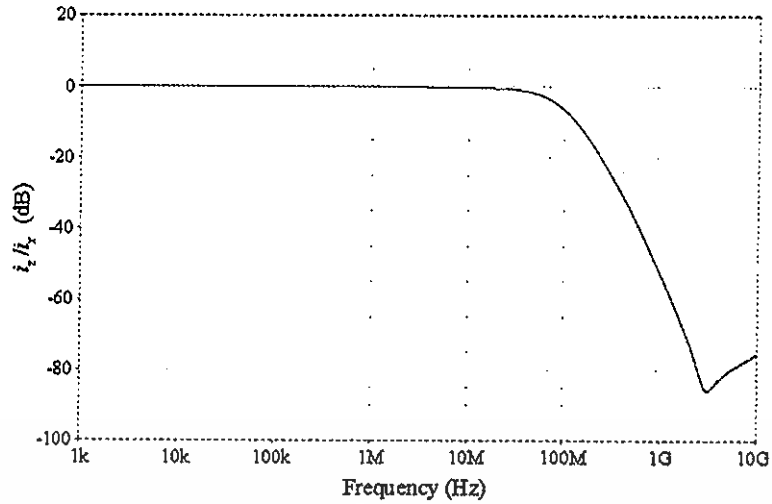


Figure 4. Frequency response of the current transfer i_z/i_x characteristic.

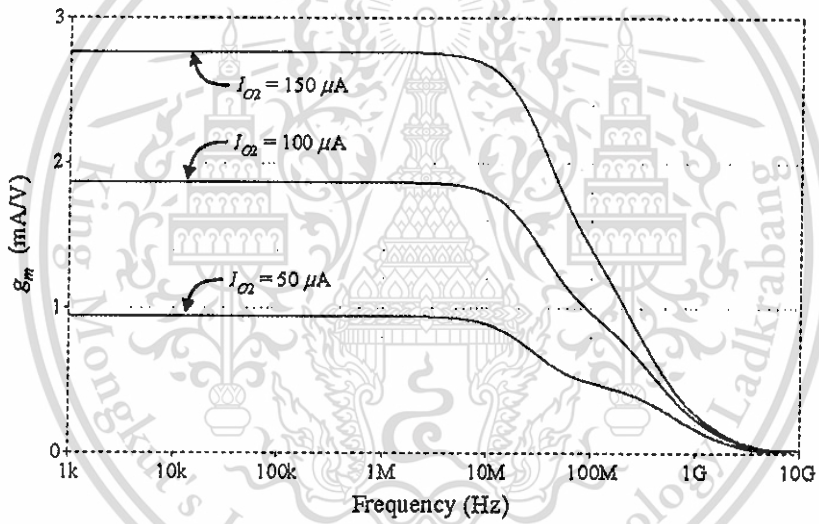


Figure 5. Frequency response of the transconductance gain g_m characteristic.

5. Conclusion

In this paper, a simplified structure of the current-controlled conveyor transconductance amplifier (CCCTA) in BiCMOS technology has been introduced and characterized. The circuit is capable of operate at ±1V supply voltages, and can operate to a frequency about 20 MHz. The proposed CCCTA is implemented with standard 0.35-μm BiCMOS real process parameters. PSPICE simulation results are used to verify the performance of the circuit.

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