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ศึกษาการขนส่งพาหะร้อนในกราฟีนจากความนำไฟฟ้าเชิงอนุพันธ์
Probing Hot-Carrier Transport in Graphene via Differential Conductance

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Research Title: Probing Hot-Carrier Transport in Graphene via Differential-Conductance

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ABSTRACT

In this work we show how differential-conductance mapping, performed as a function of temperature and of the electron or hole density, can be used to identify different contributions to graphene's resistivity. In contrast to previous studies, which have focused largely on the variation of the resistivity in the linear-conductance regime, our studies performed under nonlinear conditions allow us to fully suppress quantum corrections to the resistance. In this way we are therefore able to unambiguously identify the main contributions to scattering over a wide temperature range. Our investigations of the bilayer system show that the resistance exhibits only insulating behavior, decreasing with increasing temperature at all temperatures and carrier densities. This observation cannot be explained within the context of electron-phonon scattering but is consistent with the theory for screening of short-range impurities. As the charge-neutrality point (CNP) is approached an additional contribution to the resistance is observed, which we attribute to electron-hole puddle formation in the presence of long-range Coulomb disorder. On the basis of these observations we therefore suggest that temperature-dependent transport in bilayer graphene is dominated at all temperatures and densities by scattering from long-ranged charged impurities and by short-ranged defects. At least for the graphene-on-SiO_2 device that we study, these sources appear to overwhelm any contribution from phonons.

Keywords: graphene, resistance, phonon scattering, impurity scattering, nonlinear spectroscopy

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Ratchanok Somphonsane

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Chapter 1

Introduction

1.1 Introduction to the Research Problem and Its Significance

With the intense interest that graphene has attracted over the past decade, it seems hard to believe that a clear understanding of the factors governing a quantity as basic as its electrical resistance could remain, even at this stage, elusive. The very two-dimensional nature of this material means, however, that its conduction can be influenced by a variety of different scattering mechanisms (both intrinsic and extrinsic), the interplay of which can result in complicated variations of the resistivity as a function of temperature (T) and carrier density. Phonon-mediated scattering, for example, can arise from the intrinsic acoustic and optical phonons of graphene itself, but can also be caused by the interaction with rippling modes and with surface phonons of the underlying substrate. Impurities are another potentially important source of scattering, and may be both long- and short-ranged in nature. Long-range scattering is generally attributed to Coulomb scattering from charged impurities in the underlying substrate, while short-range scattering arises from neutral defects. Screening of these impurities, and of the electron-phonon interaction, must be taken into account when determining resistivity, resulting in strong density-dependent behavior. Complicating this picture even further, at cryogenic temperatures the resistivity may also be influenced by well-known quantum corrections, most notably weak localization and antilocalization, and electron-electron interactions. Kondo physics has even been invoked to account for some of the resistivity variations observed in this regime. From this discussion it is clear that properly identifying the dominant contributions to graphene's resistivity is a far-from-simple task, and one whose outcome should be particularly sensitive to the level of disorder in the system.

In conventional semiconductors near room temperature, with modest levels of doping, phonon scattering is well known to serve as the dominant process that limits carrier mobility. The situation in graphene is more complicated, not only for the reasons alluded to above. Electrons and holes reside on a two-dimensional Dirac cone, placing significant phase-space restrictions on allowed phonon-scattering events. These restrictions are further compounded by the chiral character of graphene's carriers, which strongly suppresses backscattering. While optical phonons play a role influencing the room-temperature mobility of materials such as silicon and gallium arsenide, in graphene the much larger energy (>160 meV) associated with these modes is generally believed to suppress their importance. Overall, the message is that phonon scattering in graphene is weak, even when the interaction with substrate phonons is taken into account. Room temperature mobility as large as ~20,000 cm^2/Vs is therefore predicted for graphene on SiO_2, while experiment has demonstrated values as large ~200,000 cm^2/Vs for freely-suspended graphene. In many experiments, however, performed with graphene on SiO_2, corresponding mobility values may be smaller than 1000 cm^2/Vs, suggesting that disorder-induced impurity scattering dominates over that produced by phonons.

In this work, we will undertake investigations of the resistivity of monolayer and bilayer graphene transistors, fabricated on SiO_2 substrates. Our studies will be performed over a wide temperature range (3 – 300 K), and for densities that span both the electron and hole branches of the Dirac cone, making use an approach of differential-conductance mapping to explore the separate contributions to graphene's resistivity. The comparison of monolayer and bilayer characteristics is particularly useful here since screening is expected to be very different in these materials due to their linear (monolayer) versus quadratic (bilayer) energy dispersions.

1.2 Objectives

1.2.1 To study current-voltage (I-V) characteristics of monolayer- and bilayer-graphene devices

1.2.2 To study differential conductance of monolayer- and bilayer- graphene in the presence of varying temperature, carrier concentration and magnetic field

1.2.3 To study energy relaxation mechanism of hot carriers in monolayer- and bilayer- graphene

1.3 Scope of Research

1.3.1 Graphene exfoliation & contact formation

1.3.1 I-V characteristic measurement

1.3.2 Transconductance measurement

1.3.3 Differential conductance measurement

1.4 Method

1.4.1 Wafer preparation

We use highly *n*-doped silicon wafers, covered with a 300-nm layer of SiO_2, as the supporting substrate. A coordinate grid is defined on the wafer pieces using photolithography, followed by metal evaporation

1.4.2 Micromechanical exfoliation

Micromechanical exfoliation of HOPG graphite will be used to deposit monolayer and bilayer graphene flakes onto SiO_2 substrates with pre-deposited lithographic markers.

1.4.3 Flake Identification

These flakes are then identified with optical microscopy, the most commonly used techniques to properly determine the number of layers of graphitic flakes.

1.4.4 Contact formation

Electron-beam lithography will then be used to fabricate contact electrodes to preselected graphene flakes, as required for measurement of their electrical properties.

1.4.5 Basic device characterization

Fabricated devices will be subjected to a variety of different electrical characterizations. Current-voltage characteristics will be first of all measured to confirm the quality of the ohmic contacts achieved in this manner. In many cases, I-V characteristic measurement is also used as an *in situ* current annealing for eliminating chemical doping of the graphene and to ensure that the Dirac point to its restored close to its expected position. Transconductance measurements will then be performed in the presence of varying carrier concentration, to allow for proper characterization of the fabricated graphene device. Depending on the amount of chemical doping of the graphene we should expect to see the Dirac point where the resistance of graphene is maximum as the Fermi level is swept from hole band to electron band. These measurements will be undertaken at varying temperatures, to establish the influence of different scattering mechanisms on graphene resistivity. Differential measurement in the presence of varying carrier densities and temperatures will also be performed to identify the various transport regimes for monolayer and bilayer graphene, and to suppress the role of quantum corrections.

More details on these steps will be discussed in Chapter 3.

Chapter 2

Literature Review on Electrical Conductivity in Graphene

There have been many studies on the transport properties of graphene, yet most experiments have focused on the transport of carriers near thermal equilibrium where conduction is controlled by the properties of electrons near the Fermi level. By simply assuming that the transport is linear for the excitations used in the measurements these experiments do not pay much attention to non-linear effects. Important information can be gained, however, by studying the non-linear response of graphene when it is driven by finite external electric fields. Recently, there have been theoretical reports of nonlinear transport in graphene and interestingly they have also been observed in a number of experiments[1-16]. At high bias voltage, electron scattering from phonons tend to reduce the conductivity, which is expected to make the current-voltage curves at high bias sublinear. This has been seen in MLG as a tendency for the current to almost saturate[1,2]. Nonlinearity in conductance at low bias, however, has been shown to result from hot carriers created by Joule heating[3-9] and the mechanisms by which they dissipate heat, namely, by diffusion to electrodes[4,5] (see Figure 2.1) or by transfer to the graphene lattice via the e-p scattering[6,7] (see Figure 2.2). This is, however, less expected in MLG because the conductivity is not very sensitive to temperature[1,2,4,10]. The nonlinearity can also manifest itself as a superlinear behavior as has been discussed by many authors[10-16]. In particular, Zener-Klein tunneling in MLG has been shown to give rise to superlinearities close to CNP, especially in low mobility sample[10-12]. Other possibilities for nonlinearities include the presence of tunnel junctions[13] or contact phenomena[14]. Furthermore, nonlinear current-voltage curves in graphene oxides have been explained with space-charge limited currents[15], but such effects are likely to be negligible in metallic graphene. Nonlinearities are predicted also for vertical transport in misaligned BLG or few-layer systems[16].

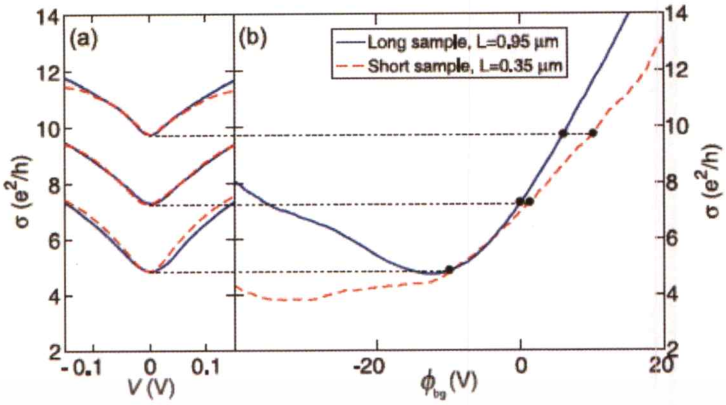

Figure 2.1: The left-hand panel (a) shows the experimentally measured differential conductivity σ(*V*) at finite *V* for the short (dashed line) and the long (solid line) BLG sample at three pairs of gate voltages that are chosen so that the minima at *V* = 0 V for both samples coincide. The right-hand panel (b) shows the corresponding zero-bias conductivity σ(*V* = 0) vs the gate voltage ϕ_{bg} for both samples. The temperature is T_0 = 4.2 K. Adopted from [4].

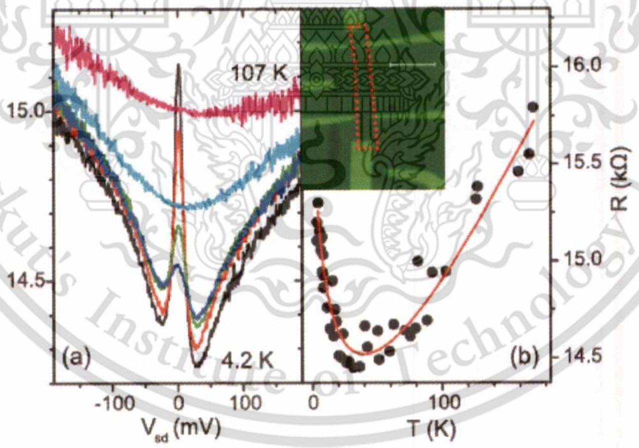

Figure 2.2 (a) Differential resistance as a function of dc source-drain bias measured in graphene sample at different bath temperatures: T_B = 4.2, 17, 26, 35, 83, and 107 K from bottom to top. (b) Dependence of the zero-bias differential resistance on the bath temperature. All measurements are taken at the Dirac point. The solid red line is a guide to the eye. Inset: Optical micrograph of the measured graphene sample, with the flake indicated by a dotted outline; the scale bar is 10 μm. Adopted from [7].

At the same time, it is a well-established fact that quantum effects occur in graphene. Effects such as weak-localization and weak anti-localization have been predicted and also experimentally confirmed in many cases where the experiments are conducted at low temperatures. In fact, it has also been shown that these quantum interference effects are quite robust in graphene and can extend even up to high temperatures, (200 K), due to weak electron-phonon scattering[26]. As a result of this, the weak localization and electron-electron interactions in 2D systems which give rise to a logarithmic correction to the conductivity can be the source for the origin of the nonlinearity in the differential conductance at low bias[17-19] (see Figure 2.3).

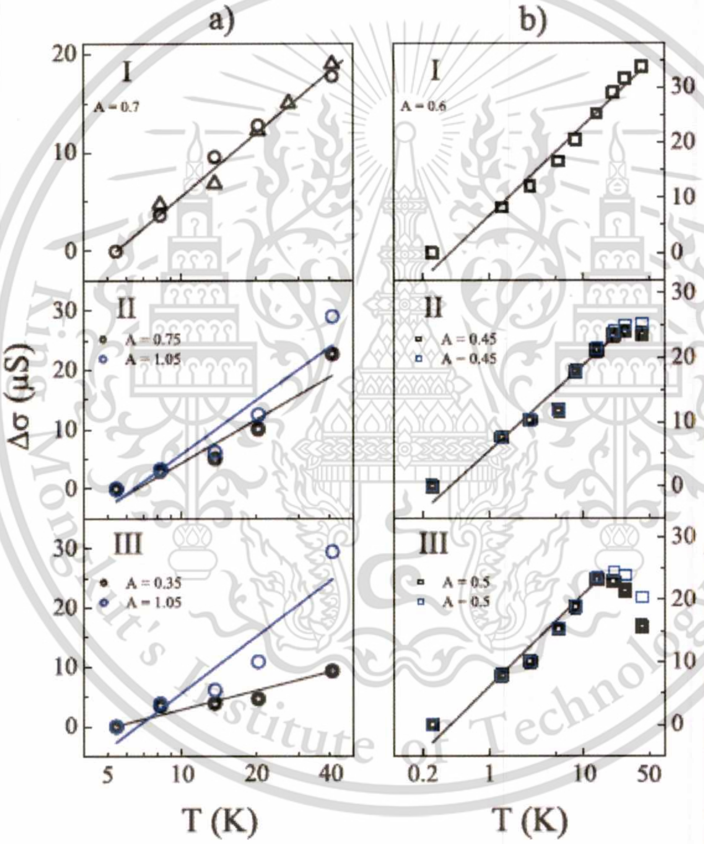

Figure 2.3: The electron-electron interaction correction to the conductivity. (a) The results for three regions of carrier density from two different samples (circles and triangle) are obtained by including WL correction. (b) The WL contribution is suppressed by magnetic field. Solid lines are fits to theory of a logarithmic correction to the conductivity. Black and blue colors correspond to the subtraction of acoustic phonon contribution with different values of deformation potential. Adopted from [19].

Since charge carriers in graphene are chiral and have an additional quantum number (pseudospin), arising from the fact that their wave functions are composed of the contributions from two lattices, the theory of weak localization (WL) in graphene predicts an unusual feature. The Berry phase of the pseudospin incurred by a carrier circumscribing each of the two graphene valleys is π in the case of monolayer. Backscattering in the monolayer (half circumscription of the valley) is therefore effectively suppressed as the two opposing interfering trajectories pick up a phase difference of π, giving rise to a positive correction to the conductivity. Therefore, in monolayer graphene weak anti-localization (WAL) rather than WL is expected to occur[20-22]. The first experiments on WL in monolayer graphene have however produced contradictory results[23-26]. Morozov et al.[23] observed a strong suppression of WL in exfoliated graphene samples and Wu et al.[24] observed WAL in an epitaxial graphene sample. Later on, Tikhonenko et al. showed that WL could be seen in a monolayer graphene[25] and that depending on experimental conditions either WL or WAL is manifested[26] (see Figure 2.4). Moreover, other theoretical studies in fact show that WL will be restored with increasing disordering strength in the sample[27,28]. In bilayer graphene, however, the Berry phase of the carries is 2π, not π as in the monolayer, meaning that the pseudospin turns twice as quickly in the plane as the momentum, while in monolayer it is aligned with the momentum. As a result, backscattering is enhanced in a bilayer leading to a conventional negative correction with a sign of WL[21,29] and this was confirmed by the experiment of Gorbachev et al.[30] (see Figure 2.5).

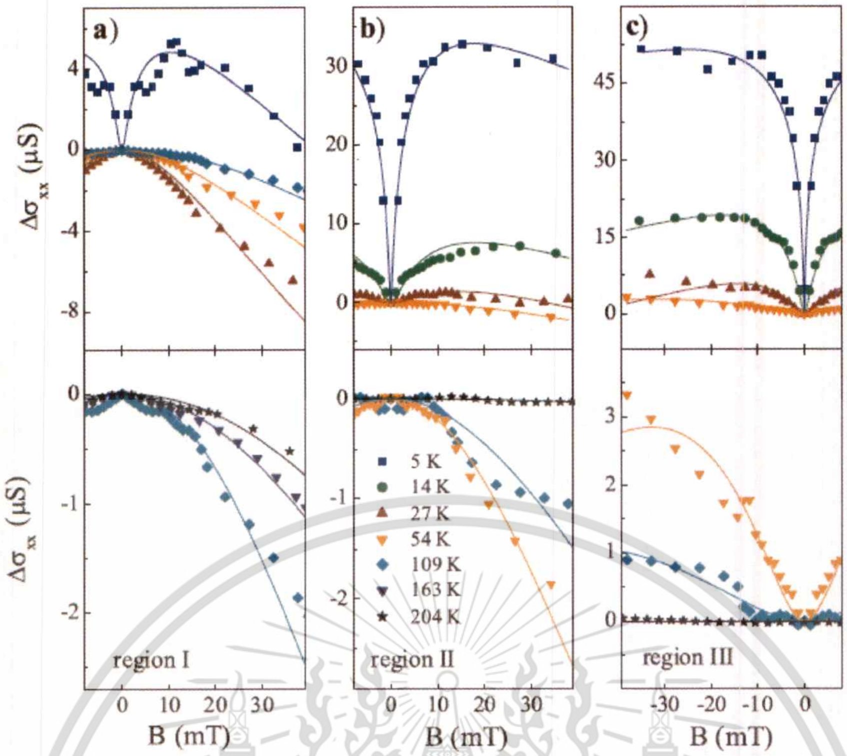

Figure 2.4: (a), (b), (c) Evolution of the magnetoconductance with increasing temperature at three different gate voltages, showing a transition from positive to negative low-field magnetoconductance. Bottom panels show the results at high temperatures. Solid curves are fits to theory of magnetoconductivity due to quantum interference in monolayer graphene. Adopted from [26].

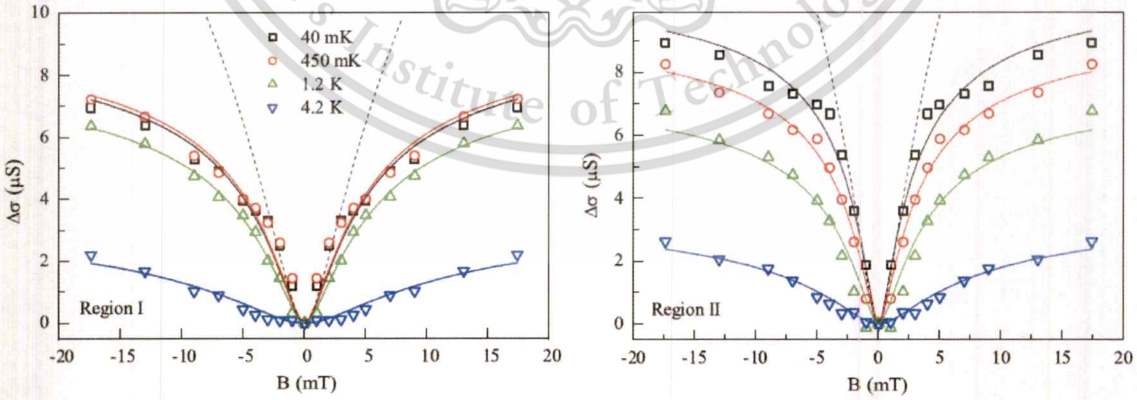

Figure 2.5: Averaged magnetoconductivity for two gate voltages. Dashed and solid curves are the fits using two different theories for the magnetoconductivity due to WL in bilayer graphene. Adopted from [30].

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Chapter 3

Methodology

3.1 Wafer Preparation

We begin by selecting highly *n*-doped silicon wafers covered, with a 300 nm thick dielectric layer of thermally grown SiO_2, as our substrate of choice. The specific oxide thickness of 300 nm is necessary to create the optimum optical contrast necessary to make visible the ultrathin layers of graphene under an optical microscope. The highly doped silicon serves as the back-gate electrode which allows us to apply an external voltage to vary the electric field across the final device structure. The wafers are then cleaved into small squares of approximately 5 x 5 mm^2 using a precise diamond scribe hand tool. In order to remove the micro particles of wafer dust that might have fallen onto the surface during cleaving of the wafer, the cut substrates are immersed in an ultrasonic bath containing acetone. The acetone also helps remove any organic residue that may have been transferred onto the substrate during handling. Following this the substrates are immersed in methanol before finally been blown dry under a strong flow of dry nitrogen. Prior to the exfoliation of graphene onto these substrates it is essential to have a marker grid that will aid in identification of the precise location of the flakes. In order to do this we employ a standard procedure of optical lithography in which a pre-defined set of markers printed on an optical mask is used to transfer the pattern onto the substrates (see Figure 3.1). A metal stack consisting of 3 nm of chromium (Cr) and 45 nm of gold (Au) is deposited onto the substrates using an e-beam evaporator. The Cr acts as an adhesive layer for the main contact material (Au), whose thickness is optimized to provide the high visibility needed when performing subsequent processing steps in an electron microscope. At this stage the wafers are ready for mechanical exfoliation.

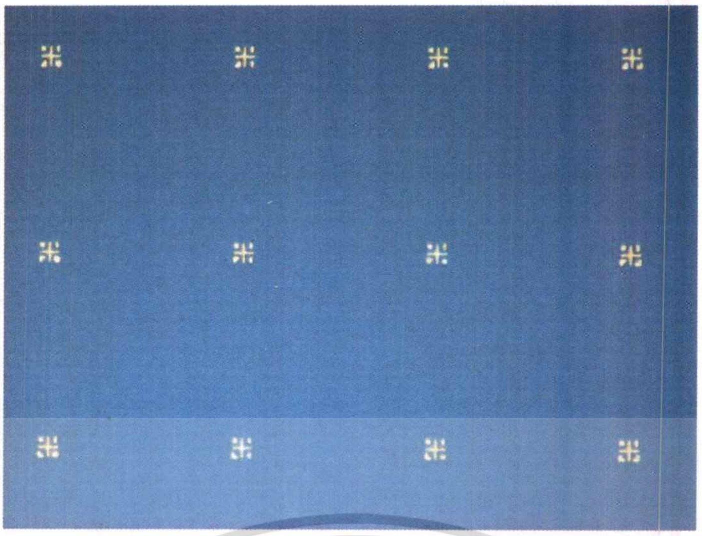

Figure 3.1: Optical image of a clean Si/SiO$_2$ substrate showing the marker grids used for locating graphene flakes deposited by exfoliation (performed later).

3.2 Micromechanical Exfoliation

The micromechanical cleavage or "exfoliation" method used for the isolation of graphene from its parent material (crystalline graphite) has been the backbone for device research since its first demonstration by the Manchester group in 2004. Among the several advantages of this approach, the relative ease of obtaining graphene flakes, and the high crystalline quality that it preserves, remain the main factors responsible for its widespread use to date. If not for this simple innovation, graphene would probably not be so well-known. Indeed, it is quite possible that research in 2D materials in general would not have advanced to its current level, since many of the new materials known today have been obtained primarily by exfoliation. In this work, we employ this approach to obtain the graphene flakes required to make our devices.

To begin with, the marker samples obtained earlier are once again cleaned with acetone and methanol in an ultrasonic bath following which they are dried in a flow of compressed nitrogen gas. In addition to this an ozone cleaning step may also be performed to ensure the removal of any photoresist residue left after processing of the markers. The wafers are then placed on a hot plate at ~150 °C while we simultaneously work on preparing the "transfer" tape. The high temperature ensures two things. Firstly, the substrate remains free of moisture which allows the flake to make good contact to the substrate. Secondly, it enhances the van der Waals interaction between the substrate and the graphene layer in immediate contact with it, relative to the already existing interactions between the different layers of the graphite. This slight difference can aid in the isolation of single flakes which are in direct contact with the substrate and therefore it is possible to increase the yield of potential flakes obtained on a single substrate by following this approach. To begin the process of preparing the transfer tape, we pick a small piece of Kish graphite with a pair of clean tweezers and place it on the sticky side of the blue tape. We then fold the tape on itself, gently pressing the graphite piece between our fingers and reopen the tape. This initial step is performed so as to remove the impurities that are present on the periphery of the graphite piece. Once this is done the clean graphite piece is transferred onto a new piece of blue tape and the folding and unfolding process is repeated until the thick graphite piece is redistributed into significantly thinner flakes across a small region of the tape. Care must be taken to not overdo the peeling process as this will not only result in more glue residue contaminating the flakes, but also more importantly it introduces randomness in the specific cleaving directions which ultimately results in flakes that are too small to use. The best results are often obtained when the initial area imprint of the thick graphite piece is more or less conserved at the end of the cleaving process. The prepared transfer tape in then gently pressed over the heated substrate and a gentle rub with an eraser or the flat end of a Teflon tweezer for about 30 seconds will be sufficient to allow the transfer of flakes onto the substrate. Following this, the tape is gradually peeled off. Extended periods of pressing and/or increase of applied pressure only results in thick graphite flakes being transferred onto the wafer and must therefore be avoided. The transfer tape that we use is generally a low residue tape (Nitto^{TM}) and is preferred over the original 3M^{TM} scotch tape as it significantly reduces the unavoidable transfer of glue residues (along with potential flakes) onto the substrate. The adhesive qualities of the blue tape may be slightly inferior and may make the cleaving process somewhat harder however the tradeoff is justified in lieu of obtaining higher quality samples. In the event that, despite the various precautions described here, significant glue residue is found to be present, the samples can be annealed in a tube furnace at ~250 °C in a controlled (1.5 L/min) flow of Ar (95%)/H2 (5%) gas for approximately 1 hour. Once the transfer steps are completed it is best to store the samples in a portable vacuum box containing packets of silica gel to prevent the absorption of moisture. If kept under ambient conditions for prolonged periods of time, the surface of the substrate can become saturated with moisture and the resultant hydrophobicity will make it impossible to coat the polymers (PMMA) required for subsequent processing steps. To salvage these samples prolonged thermal annealing may be required, however this is achieved while having to sacrifice the inherent properties of as transferred flakes.

3.3 Flake Identification

Some of the most frequently used methods for the identification of graphene flakes are optical microscopy, Raman spectroscopy and atomic force microscopy (AFM). Of these the optical method is most popular as it is comparatively non-invasive and straightforward. The flakes obtained are generally a mix of thick graphite pieces that appear as a bright white color and thinner but multilayered pieces that have a strong blue color. At a low magnification (20x), it is impossible to see any monolayer flakes. However, as we approach a higher magnification (100x) monolayer flakes can be easily detected as they appear as an almost transparent (lowest contrast) layer revealing the substrate behind it. At times it can be tricky to distinguish between monolayer and bilayer samples but this process becomes quite reliable with experience. Figure 3.2 shows an example of monolayer, bilayer and multilayered graphene identified by using optical microscopy. As already mentioned earlier, such distinct optical contrast is made possible by choosing the optimum oxide thickness of 300 nm. However, owing to its near-transparent nature monolayer flakes can be very difficult to find if the raster scanning is not performed very slowly and vigilantly. Once potential flakes that are roughly a few microns in size are identified, optical images of them are recorded from a microscope-mounted camera at different magnifications (2x, 10x, 20x and 100x). This allows us to accurately design contact probes using AutoCAD and help identify the position of the flake relative to the sample edges when viewed under the SEM. Additional standalone verifications for the thickness and properties of the monolayer and bilayer flakes may be obtained from Raman and AFM techniques and can be found in our earlier works. The optical images obtained above are then imported into AutoCAD^{TM} and contacts to the flakes are drawn. This is followed by creating an e-beam writing run file using the Nanolithography Pattern Generation Software (NPGS).

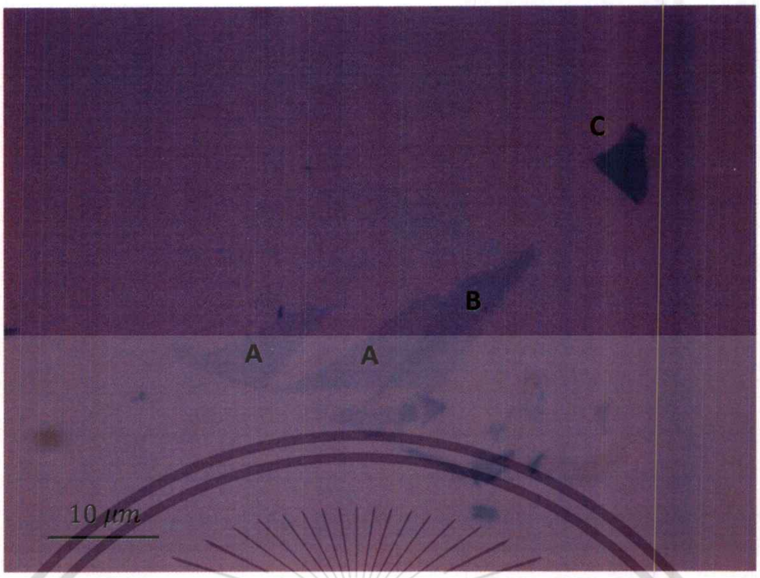

Figure 3.2: A typical result of the exfoliation as seen under an optical microscope. (A) indicates monolayer, (B) bilayer and (C) many-layer. Note the relative contrast of these layers.

3.4 Contact Fabrication

In order to perform electrical measurements of suitable flakes we first need to form source (S) and drain (D) contacts to them. In most experiments pertaining to the analysis of DC small-signal and low-temperature transport properties of graphene, it is the norm to fabricate two-terminal, four-terminal or Hall-bar geometries. The four-terminal measurements are useful when contact resistance need to be characterized while the Hall-bar structures are useful for magneto-transport and for eliminating contact resistance from the measurement. Regardless of the geometry, a standard procedure of electron beam lithography (EBL) is employed to arrive at the desired results. The maximum writing resolution that is achievable depends on the lithography system, and for the JEOL system that we use the resolution can be as low as 50 nm. This allows the fabrication of a wide variety of nanodevices including quantum point contacts and nanowires that have been previously investigated in our research group. However, in the graphene FETs that we fabricate here, the source to drain distance is generally chosen to be greater than 1 μm in order to keep the channel diffusive.

The fabrication process flow for the EBL is depicted in Figure. 3.3(a). To begin evaporate the solvent content of the resist and thereby harden it. This step also improves the adhesion between the PMMA and the substrate thereby minimizing any process-related failures. However, care must be taken to avoid prolonged soft bake times which can result in increased crosslinking in the polymer structure, rendering it unreliable for accurate process characterization. After the soft bake the sample is mounted on an e-beam sample holder and the writing steps are initiated. The graphene flake of interest is found on the SEM/EBL screen by matching the four set of markers surrounding it along with the column and row information that were recorded earlier. Once located, the markers are aligned (using joystick control) to pre-defined markers on the computer screen and the pattern is written.

The e-beam exposes the desired areas of the PMMA, crosslinking the long polymer chains of the PMMA. The crosslinking makes the PMMA in these areas dissolve in a solvent developer such as methylisobutylketone (MIBK), thereby freeing these areas from resist material. The unexposed areas however remain intact as shown in Figure 3.3 (a). As a rule of thumb, it is advisable to slightly overdevelop the sample in order to ensure that the exposed areas are indeed free of resist. This is emphasized further by the fact that in the case of graphene fabrication, standard polymer cleaning techniques such as ozone cleaning or oxygen plasma etching cannot be used. This is because the oxygen atoms are highly reactive with graphene's carbon atoms, leading to their immediate oxidation. The developed samples are then dipped in a solution of isopropyl alcohol (IPA) to quench the development process and blown dry with compressed nitrogen. The samples are viewed under a standard optical microscope at the highest magnification of 100x to confirm successful development time and to also check if the graphene flake(s) was (were) successfully contacted. In case of under-development, which is generally visible as a white residual hue inside the developed areas, the sample can be re-developed for a few more seconds and checked again. However, if the probes were misaligned with the flake and/or failed to contact it, the samples need to be washed in acetone and the EBL step repeated. The latter is highly undesirable because it increases the amount of PMMA residues that stick to the graphene flake and this degrades its otherwise superior electronic qualities. Following the development steps, the samples are loaded into an e-beam evaporator in which metallization of the electrodes is performed. Cr and Au are once again used as the contact materials, with Cr playing the role of a necessary adhesive layer owing to the weak wettability of Au. In addition, we deposit at least 50 nm of Au so that gold wirebonding can be easily performed in the final packaging step. To ensure a good quality of metal deposition, the samples must be pumped down to a vacuum level of at least 10^{-7} torr and the evaporation rate should be set to 0.7 to 1 Angstroms per second. This is important to ensure that the grain size of the deposited metal is small enough to form a good contact on the surface of the sample. After the required metal stacks are deposited, the samples are transferred into a beaker filled with warm acetone (~65 °C, 3 hours) to initiate the lift-off process. Here, the unwanted metal that lies on top of the unexposed PMMA is removed when the latter dissolves in acetone. In order to facilitate the lift-off process, gentle pressure may be applied using a syringe. However, stronger lift-off techniques such as ultrasonic agitation should be avoided at all costs because the high-frequency vibrations can cause the graphene flake to become detached from the surface of the substrate.

Figure 3.3(b) shows an optical image of a flake after lift-off (followed by a methanol rinse and N_2 dry). The source, drain and central voltage probes are seen to make accurate contact with the graphene flake (enclosed within white dotted line). In Figure 3.3(c), an optical image of the overall device is shown. This includes large area contact pads (~200 μm) that are needed for wire bonding. It must be noted that the inner contact probes and the larger connecting pads are both written in a single EBL step by only changing the beam current between the two patterns. The bigger pads need ~10x times larger current while keeping the total writing time under tolerance. The single step EBL avoids multiple exposures and in turn results in better sample quality.

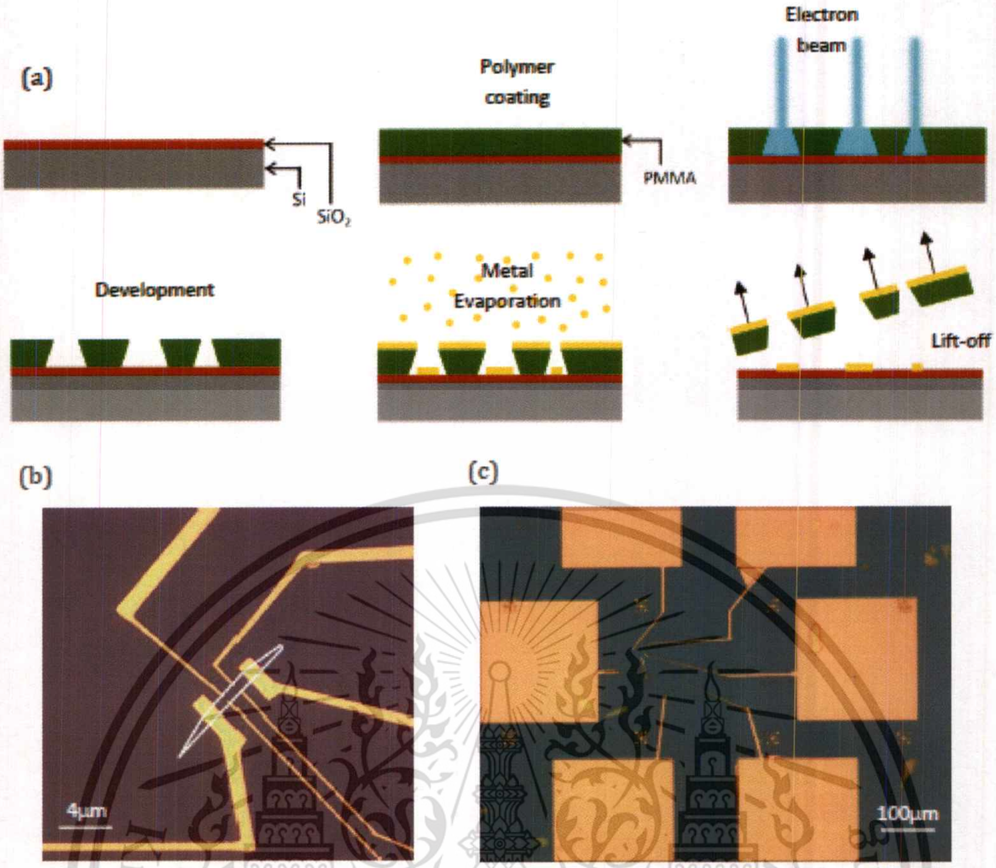

Figure 3.3: (a) Standard process flow employed for contact formation. Cr and Au are used as contact materials while PMMA is used as the e-beam resist. (b) The final device with source drain contacts after metal evaporation and lift-off. The graphene flake is enclosed within the dotted white line. (c) Overall device including wire-bonding pads.

3.5 Basic Electrical Characterization

To obtain DC I-V characterization, we make use of a Keithley source meter (Model 2400). For measurements of the Dirac curves we make use of the low-frequency small-signal (~13 Hz) AC setup such that the applied voltage is small enough to cause negligible heating effects. Figure 3.4 shows a schematic of a 2-probe measurement, in which current and voltage are measured between the same two electrodes. Two Perkin-Elmer^{TM} lock-in amplifiers are used in this setup. One of these supplies the excitation voltage that drives a current through a resistor R_s in series with the sample. The value of this current is determined predominantly by R_s, provided that the condition $R_{device} \ll R_s$ is always satisfied (typical value of R_s is 1 MΩ).

In our measurement, a constant current of 100 nA is used and the current level is adjusted by varying the excitation voltage and/or the size of R_s. The two voltage probes from the second lock-in amplifier, C and D in Figure 3.4, are connected to the electrodes of the graphene device (1 and 4). In contrast, in a 4-probe measurement the lock-in voltage probes (C and D) are connected to a separate pair of electrodes (2 and 3), such that current and voltage are measured separately thus eliminating the contribution from any contact resistance. The oscillator frequency of the lock-in amplifiers is set to 13 Hz to minimize noise pick-up. A Keithley DC source meter is used to provide a gate voltage. R_g acts as a protection resistor to avoid gate leakage and is typically high (100 MΩ). The outputs of the lock-in amplifiers are read out by digital multimeters (Agilent) and recorded by a computer with the aid of a LabView script. All instruments in the setup were thoroughly grounded and connected to the computer via GPIB interface.

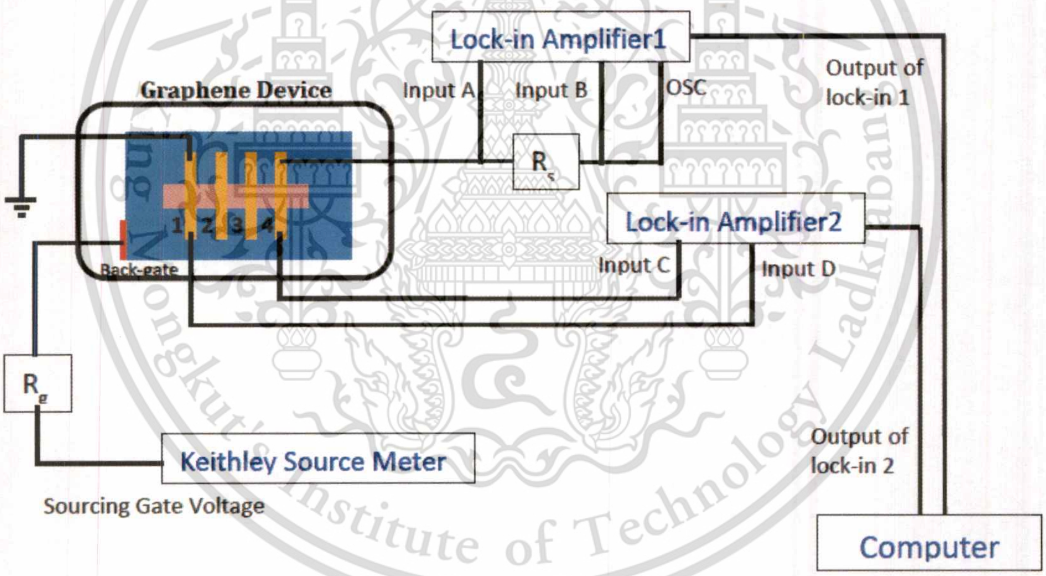

Figure 3.4: Schematics of a low-frequency AC measurement setup for 2-probe measurement.

Chapter 4

Results and Discussions

4.1 Basic Device Characterization

We have investigated the basic characterization of six different graphene devices, two of which were monolayer and four of which were bilayer. Table 1 summarizes the important parameters for these devices, with the notation “M” and “B” referring to monolayer and bilayer graphene, respectively.

Device	L[a] (μm)	W[a] (μm)	μ_h[b] (cm^2/Vs)	μ_e[b] (cm^2/Vs)	σ_{min}[c] (e^2/h)
M1	0.8	0.4	16500	10200	23
M2	1.1	1.3	14200	11600	22
B1	1	4	1100	1070	4.2
B2	4	0.25	1100	1280	4
B3	1.5	1	2300	1800	5.5
B4	1	2	420	450	1.3

Table 4.1: Important parameters for the different devices studied. [a]L, W: channel length, width, measured between voltage probes. [b]μ_e, μ_h: Electron, hole mobility, determined at 4 K, and at density of 10^{12} cm^{-2}. [c]σ_{min}: minimum conductivity, measured at 4 K.

From the Table above it can be seen that the mobility values exhibited by the different types of device are consistent; the monolayer devices show much higher mobility than the bilayer ones, but, for a given device type, the observed mobility values are similar. This is in spite of the different contact geometries employed in the different devices.

4.2 Linear Conductance of Monolayer and Bilayer Graphene

Here we describe the linear conductance measurements of the devices mentioned in Table S1, which consist of measuring their source-drain conductance as a function of back-gate voltage (i.e. their Dirac curves). These measurements were made at a series of different temperatures (while sourcing a fixed current of 100 nA). In Figures 4.1 and 4.2, we show the comparison of these different measurements for the different devices mentioned above.

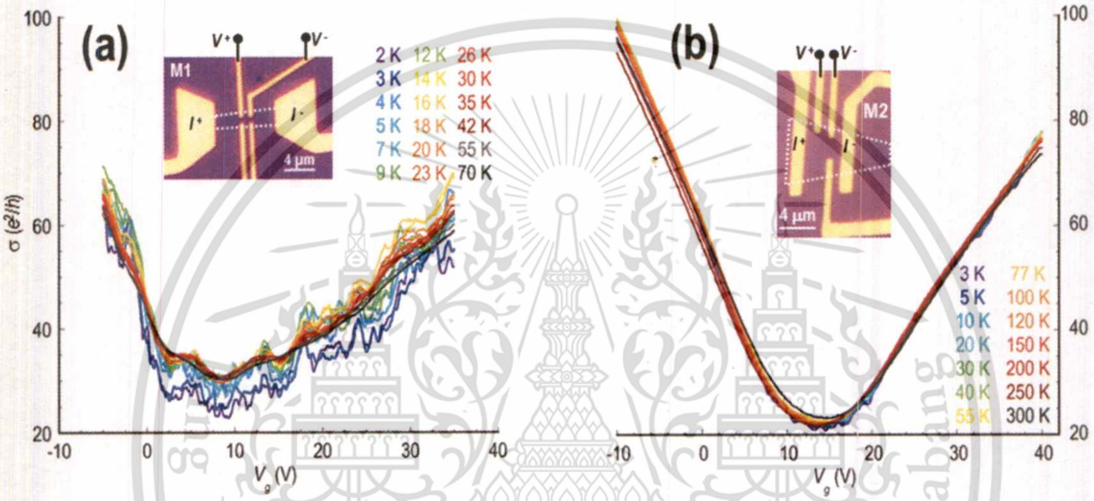

Figure 4.1: Dirac curves at various temperatures for device M1 (a) and M2 (b). The Dirac point can be clearly identified from the high-temperature curves in each panel and occurs at approximately 8 V for device M1 and 14 V for M2. Optical micrographs of these devices are shown in the corresponding insets, in both of which the outline of the graphene flake is indicated by the white dotted line and current and voltage probes are indicated.

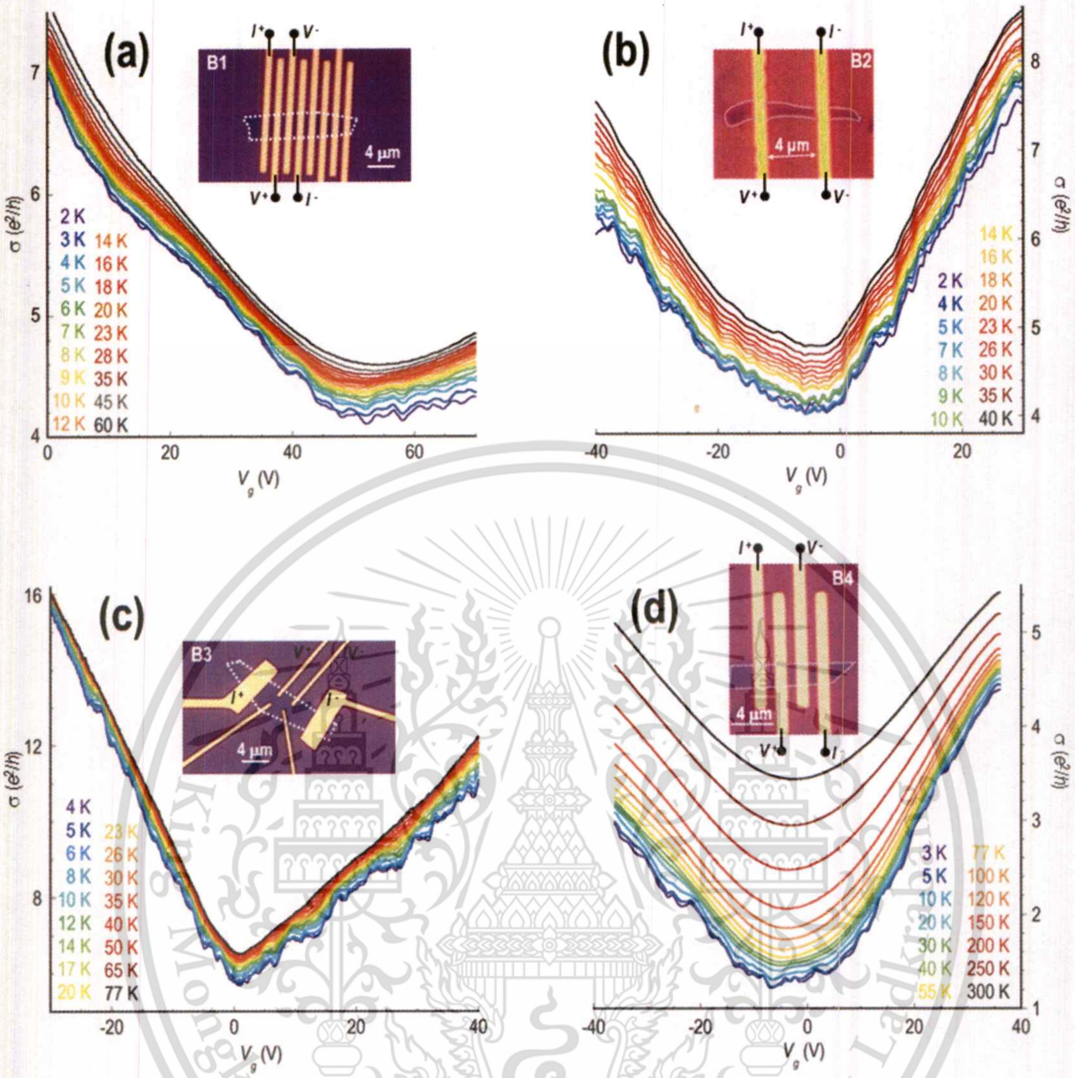

Figure 4.2: Dirac curves at various temperatures for device B1 (a), B2 (b), B3 (c), and B4 (d). The Dirac point can be clearly identified from the high-temperature curves in each panel and occurs at approximately 55 V for device B1, -5 V for B2, 0 V for B3 and -5 V for B4. Optical micrographs of these devices are shown in the corresponding insets, in both of which the outline of the graphene flake is indicated by the white dotted line and current and voltage probes are indicated.

With regards to the similarities between the two monolayer devices in Figure 4.1, it will be apparent that mesoscopic effects are much stronger in Device M1 than in M2, which may be due to the smaller voltage-probe separation in M1. Nonetheless, the mesoscopic features are strongly suppressed in M1 once the temperature is increased to ∼20 K, above which the temperature-dependent variations of the conductance in Figure 4.1(a) resemble those in Figure 4.1(b) (although it should be noted that the variation of conductance with temperature is measured over a wider range in Figure 4.1(b)).

4.3 Carrier-Concentration Analysis

In any analysis of the conductivity mechanisms in graphene, it is necessary to recognize that the conductivity (or resistivity) is determined by the combined influence of two parameters, namely the carrier concentration and the mobility. In graphene, the electron (n) and hole (p) concentrations include contributions from[4] gate-induced (n_g) and thermally-generated (n_{th}) carriers, as well as from the residual puddle density (n^*):

$$n,p \approx \frac{1}{2}\left[\pm\left(n_g + \sqrt{n_g^2 + 4n_0^2}\right)\right] \qquad (1)$$

where the minus (plus) sign corresponds to electrons (holes). Here, $n_g = -C_{ox}V_{g0}/q$, where $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate capacitance per unit area, $\varepsilon_{ox} = 3.9$ is the dielectric constant of SiO_2, q is the elementary charge, and $V_{g0} = V_g - V_0$ is the gate voltage referenced to the Dirac point. The values for n_g calculated for the monolayer and bilayer devices studied in the main paper are shown in the tables below. The residual and thermal concentrations are taken into account through the minimum carrier density $n_0 = [(n^*/2)^2 + n_{th}^2]^{1/2}$, where $n_{th} = (\pi/6)(k_BT/\hbar v_F)^2$ in monolayer graphene (with v_F the Fermi velocity) and $n_{th} = \ln 2(2m^*/\pi\hbar^2)k_BT$ in bilayer[5] (with $m^* = 0.033m_0$ being the electron or hole effective mass).

V_g (V)	14	12	10	8	6	4	2	-2	-6	-10
n_g (10^{12} cm^{-2})	0	0.14	0.29	0.43	0.58	0.72	0.86	1.2	1.4	1.7

Table 4.2 Values of n_g at different values of V_g for the monolayer device (M2). The Dirac point in this device is located at V_{g0} = 14 V.

V_g (V)	-6	-2	2	6	12	18	24	30	36
n_g (10^{12} cm^{-2})	0.13	0.16	0.45	0.73	1.2	1.6	2.0	2.5	2.9

Table 4.3 Values of n_g at different values of V_g for the bilayer graphene (B4). The Dirac point in this device is located at V_{g0} = -5 V.

In Figure 4.4, we use Eq. (1) to analyse the influence of residual and thermal carriers on the total charge concentration in monolayer (Figure 4.4(a)) and bilayer (Figure 4.4(b)) graphene. The graphs actually plot the variation of the total carrier concentration (n or p) as a function of temperature, along with the corresponding contributions from gate-induced (n_g) and residual and thermal (n_0) carriers. To obtain the variations shown in Figure 4.4, n^* was determined[6,7] from the width of the minimum-conductivity plateau in the transconductivity ($\sigma(V_g)$, in units of e^2/h per square), as demonstrated in Figure 4.3. At a reference temperature of 40 K, n^* was thus found to be 3.5×10^{11} cm^{-2} for the monolayer device (with a plateau width of ~ 4.8 V, and a minimum conductivity $\sigma_0 \sim 22e^2/h$, see Figure 4.3(a)) and 7.7×10^{11} cm^{-2} for bilayer graphene (with a plateau width of ~ 10 V and a minimum conductivity $\sigma_0 \sim 1.6e^2/h$, see Figure 4.3(b)). By making use of the self-consistent theory discussed in Refs. 6 & 7, the concentration of charged impurities responsible for such residual carriers could then be calculated to be around 3.1×10^{11} cm^{-2} and 9.3×10^{11} cm^{-2} for the monolayer and bilayer devices, respectively. These values are fairly common for graphene devices formed on SiO_2,[6,7] and are consistent also with the charged-impurity concentration that we infer from the intensity ratio of the Raman peaks,[8,9] $I(G)/I(2D)$.

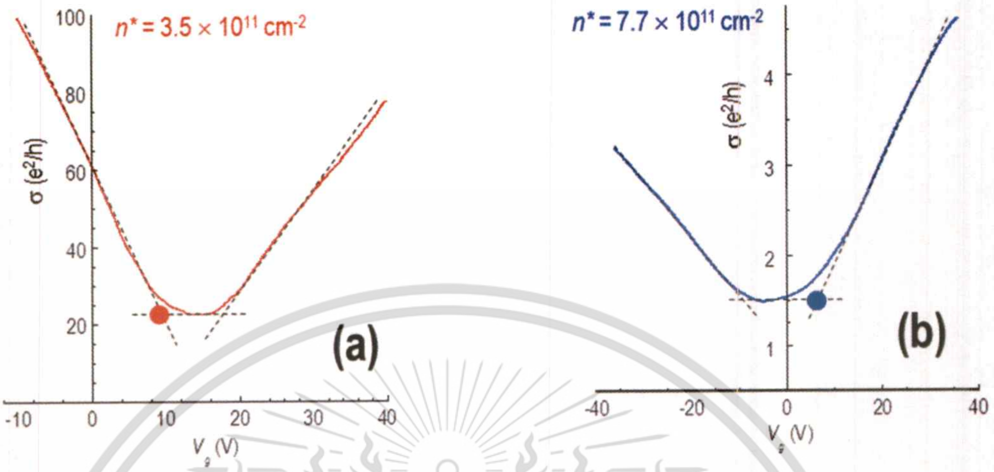

Figure 4.3: The method used to infer the residual charged density (n^*) from the transfer curve at 40 K of the monolayer (a) and (b) bilayer (b) device. Corresponding values of n^* are indicated in each panel.

Turning now to the results of Figure 4.4, in Figure 4.4(a) we indicate the temperature dependence of the hole density (p) in the monolayer device, for different characteristic gating conditions. (A similar analysis could have been performed for electrons in the same device, without significantly changing any of our conclusions). In each of these panels, we plot the variation of $n_0(T)$ by experimentally determining the residual carrier density at each temperature, and then combining this with the calculated thermal-carrier concentration. In the top panel, the gate-induced component of the density is relatively large (~ 1.7 × 10^{12}) and consequently dominates the total concentration at all temperatures. In the bottom panel, in contrast, the device is configured near the Dirac point and the carrier concentration is due entirely to the residual and thermal carriers. In the remaining panels of the figure, the density is adjusted between these two limits, allowing one to appreciate how the residual and thermal concentrations become increasingly important as the Dirac point is approached. An additional feature revealed by each of the panels of Figure 4.4(a) is that the minimum concentration n_0 does not show any significant dependence of temperature. This is due to the fact that residual carriers dominate over the thermal ones in monolayer graphene ($n^* > n_{th}$), at all temperatures considered here.

Turning next to the results of Figure 4.4(b), the four panels of this figure show the results of a carrier-concentration analysis for the bilayer device. Here we are concerned with gate induced variations in the electron concentration, although, again, this analysis could just as equally have been performed for holes. The different panels of this figure follow a similar sequence to Figure 4.4(a), and roughly show analogous behaviour; when the gate-induced concentration is high the role of thermal and residual carriers is minimal, whereas as the Dirac point is neared the latter carriers dominate. A significant difference between these results and those of Figure 4.4(a), however, is that the role of thermal carriers is more prominent in the bilayer than in the monolayer system. Specifically, it is apparent in Figure 4.4(b) that n_0 roughly doubles as the temperature is increased to 300 K, a change that can be attributed almost exclusively to a corresponding increase in $n_{th}(T)$. In the discussion that follows, it will therefore be particularly necessary to pay attention to the influence of thermal carriers when discussing the temperature-dependent conductivity variations in the bilayer system.

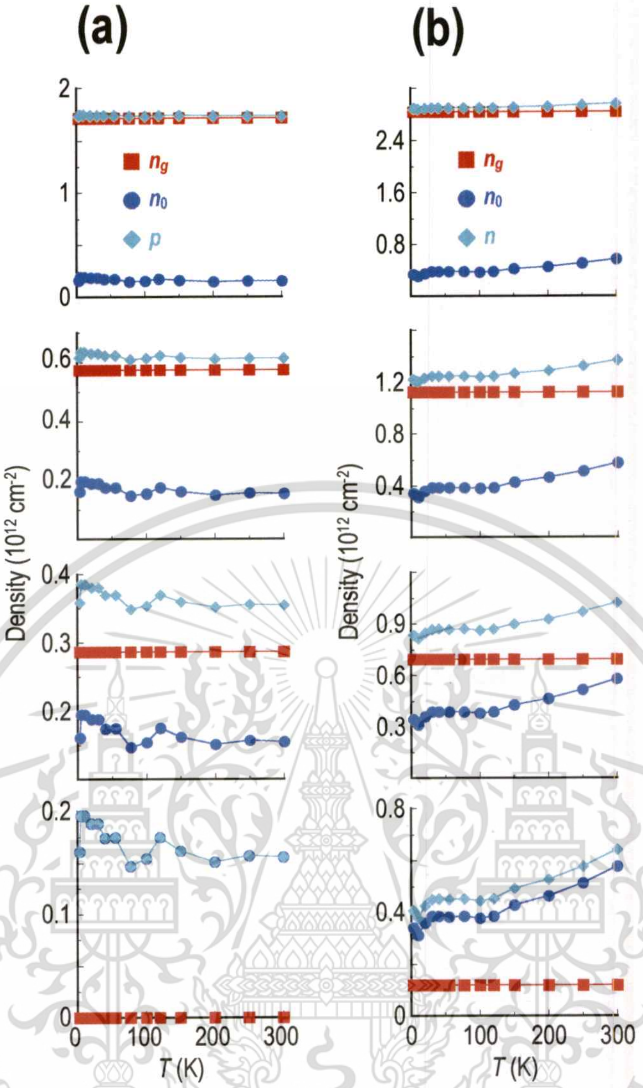

Figure 4.4: (a) Contributions to the total hole density in the monolayer device at various temperatures from 3 – 300 K. The four different panels correspond to four-different values of the gate-induced hole concentration (n_g) and the minimum carrier density (n_0) was determined from the residual charge density (n^*) inferred from the transfer curves (see Figure 4.3) and from the computed thermal concentrations (n_{th}). Moving from the top panel to the bottom one sequentially, the gate voltages (V_g) were -10 V, 6 V, 10 V, and 14 V. (b) Corresponding contributions to the total electron density in the bilayer device at various temperatures from 3 – 300 K. Gate voltages from top to bottom are V_g = 36 V, 12 V, 6 V, and -2 V.

4.4 Analysis of Quantum Corrections Based on Magneto-Conductance Measurements

The zero-bias peak seen in differential resistance g_d^{-1} at low temperatures can be attributed to quantum corrections, most notably to the combined influence of weak localization[10-13] and electron interactions[14,15]. A well-known approach to probe these phenomena involves the application of a perpendicular magnetic field, which breaks time reversal symmetry and suppresses weak localization, while leaving electron interactions largely unaffected[16]. Motivated by this, in Figure 4.5(a) we plot the low-temperature (3-K) magneto-conductance of the monolayer device (at V_d = 0). The first feature we note is the asymmetric character of the magneto-conductance with respect to field reversal, which reflects the fact that our four-terminal geometry does not yield a perfect longitudinal measurement but also contains an admixture of a Hall component. Consequently, in Figure 4.5(b) & 4.5(c) we reconstruct the magneto-conductance in terms of symmetric and antisymmetric components. To do this the magneto-resistance at positive and negative magnetic field was either mirrored symmetrically ($G_{sym}(\pm B) = (G(+B) + G(-B))/2$) or antisymmetrically ($G_{asym}(\pm B) = \pm(G(+B) - G(-B))/2$) around zero field. We found that the antisymmetric component does indeed correspond very well to a linear Hall term. More importantly, the symmetrized component of the magneto-conductance clearly shows a region of positive magneto-conductance that is centered around zero field. The full width of this region is ~50 mT, consistent with previous reports of negative magneto-resistance due to weak localization in graphene[11,13]. Indeed, in Figure 4.5(b) we see that this negative magneto-resistance is suppressed with increase of temperature to ~50 K, where the reproducible magneto-fluctuations that also arise from quantum interference[17,18] are similarly strongly damped. This temperature scale correlates well to that for which the zero-bias peak in differential resistance is suppressed. While these results suggest a strong connection of the zero-bias peak to weak localization, this phenomenon alone is insufficient to account for its full amplitude. From this observation, we infer that the zero-bias peak seen in differential resistance reflects a combination of weak localization and electron interactions, both of which become increasingly important as the temperature is lowered and the phase coherence of the carriers is enhanced[19]. It is well known from the study of conventional metals and semiconductors that, in the presence of weak disorder, the classical (Boltzmann) conductivity exhibits corrections, not only due to weak localization, but also due to electron-electron interactions[19-21]. The interactions influence transport well into the metallic limit ($k_F l \gg 1$)[19-21], and have also been reported for graphene[22]. In terms of the connection of this magneto-resistance feature to the peak in differential resistance, when $|V_d|$ is increased from zero in this regime the ensuing increase in the dephasing rate is then presumably responsible for the drop in differential resistance.

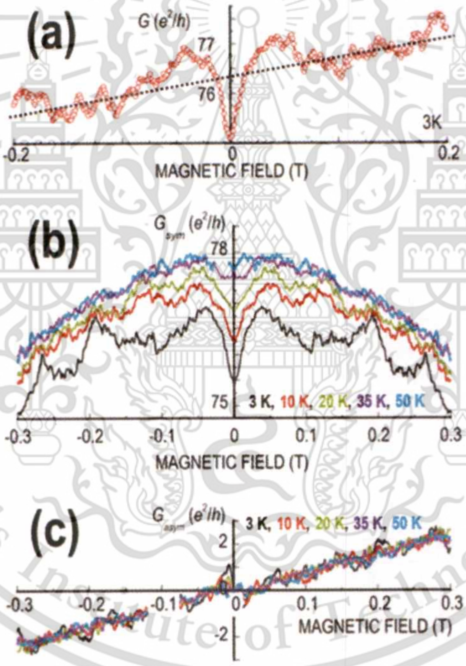

Figure 4.5: (a) The linear magneto-conductance (V_d = 0) measured at the lowest temperature (3 K) for the monolayer device. The black dotted line denotes a linear dependence on magnetic field, indicative of a Hall component. (b) Symmetric and (c) antisymmetric components of the linear magneto-conductance at various temperatures in the range of 3 – 50 K. The zero-magnetic-field conductance dip is washed away at ~50 K, which correlates closely to the temperature scale associated with the quenching of the quench zero-bias peak in differential resistance.

4.5 Differential Conductance of a Bilayer Device

In addition to our studies of the linear conductance presented in Section 4.2, we have also performed an detailed investigation of the differential conductance of a bilayer device (B2). In Figure 4.6, we plot the temperature dependence of the resistance determined for three different gate voltages for this device. The Dirac point in this device occurs at V_g = -5 V, corresponding to the center panel in Figure 4.6, while the the left and right panels of this figure show the resistance variations for hole and electron transport, respectively. In all panels, data are plotted for multiple values of the DC bias (V_d). In fact, we note that a similar insulating behavior for the resistance has also been discussed in an independent study of bilayer graphene transistors[23], although in that work only a narrow range of temperature near 300 K was explored and the microscopic origins of the observed behavior was not considered.

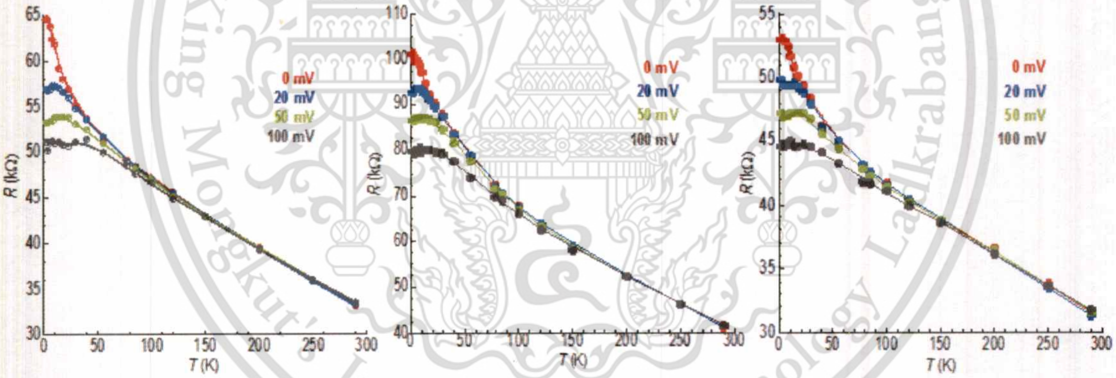

Figure 4.6: Temperature dependent variation of the resistance in bilayer device B2. The centre panel corresponds to the Dirac point, so that the left and right panels of this figure show the resistance variations for hole and electron transport, respectively. In each panel, the variation of resistance with temperature is plotted for several fixed values of V_d.

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Chapter 5

Summary and Outlook

In this work, we have explored the contributions to the resistance of bilayer graphene transistors, realized by exfoliation onto SiO_2 substrates. Our studies have revealed a complex interplay of different scattering mechanisms, both as a function of density and of the material system. The increased importance of short-range impurities in bilayer graphene appears to manifest itself as a "universal" density-independent scaled conductivity, before the role of thermal activation from charge puddles takes over near the Dirac point. This result is in contrast to the result obtained in monolayer graphene where we found that the temperature-dependent variations of the resistance appear to arise predominately from scattering from screened Coulomb impurities near the Dirac point, with an increasing role for acoustic and optical phonons as the density is increased. It is worth commenting that the diversity of mechanisms revealed through these temperature dependent studies is perhaps surprising, when we consider that, at fixed temperature, both monolayer and bilayer graphene show the same linear dependence of their conductance on gate voltage. However, these similar variations arise from completely different scattering mechanisms.

An important feature of our study has been our use of nonequilibrium biasing ($V_d \neq 0$) to suppress the quantum corrections to transport at low temperatures, and to thereby identify the broader mechanisms governing the resistance. Finally, we must mention that we do not claim to be the first to note the very different electrical characteristics of monolayer and bilayer graphene. This was apparent from early studies and has most recently been exploited to implement terahertz bolometers based on these materials. The innovative aspect of the work presented here, however, is the use of differential-conductance mapping to identify the various transport regimes for these materials, and to suppress the role of quantum corrections.

Chapter 6

Output

This grant has been utilized for the study of hot-carrier transport in graphene probing by differential conductance spectroscopy, the result of which is included in several publications and is presented in few international conferences as follows:

1. Publications

1.1) R. Somphonsane, H. Ramamoorthy, G. He, J. Nathawat, C.-P. Kwan, Y.-H. Lee, J. Fransson, and J. P. Bird "Evaluating the Sources of Graphene's Resistivity Using Differential Conductance" Sci. Rep. 7, 10317 (2017)

1.2) H. Ramamoorthy, R. Somphonsane, J. Radice, G. He, J. Nathawat, C. P. Kwan, M. Zhao and J. P. Bird. "Probing Charge Trapping and Joule Heating in Graphene Field-Effect Transistors by Transient Pulsing" Semicon. Sci. Technol. 32, 084005 (2017)

1.3) G. He, J. Nathawat, C.-P. Kwan, H. Ramamoorthy, R. Somphonsane, M. Zhao, K. Ghosh, U. Singisetti, N. Perea-López, C. Zhou, A.L. Elías, M. Terrones, Y. Gong, X. Zhang, R. Vajtai, P. M. Ajayan, D. K. Ferry & J. P. Bird "Negative Differential Conductance & Hot-Carrier Avalanching in Monolayer WS_2 FETs" Sci. Rep. 7, 11256 (2017)

1.4) J. Fransson, R. Somphonsane, H. Ramamoorthy, G. He, and J. P. Bird "Voltage-induced suppression of weak localization in graphene" Phys. Rev. B (2017, under revision)

2. Conference Presentations

2.1) R. Somphonsane, H. Ramamoorthy, and J. P. Bird, "Phonon-induced hot-carrier scattering in graphene: Insight from differential conductance" at: 9th International Conference on Electron Dynamics in Semiconductors, Optoelectronics and Nanostructures (Edison' 19), Salamanca, Spain (2015).

2.2) R. Somphonsane "In-situ current annealing of graphene-metal contacts" at: NanoThailand 2016, Nakhon Ratchasima, Thailand (2016).

2.3) R. Somphonsane, H. Ramamoorthy, and J. P. Bird, “Quenching Weak Localization in Graphene by the Application of a Nonequilibrium Voltage” at: 10th International Conference on Electron Dynamics in Semiconductors, Optoelectronics and Nanostructures (Edison’ 20), Buffalo, New York (2017).

Appendix

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SCIENTIFIC REPORTS

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Evaluating the Sources of Graphene's Resistivity Using Differential Conductance

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We explore the contributions to the electrical resistance of monolayer and bilayer graphene, revealing transitions between different regimes of charge carrier scattering. In monolayer graphene at low densities, a nonmonotonic variation of the resistance is observed as a function of temperature. Such behaviour is consistent with the influence of scattering from screened Coulomb impurities. At higher densities, the resistance instead varies in a manner consistent with the influence of scattering from acoustic and optical phonons. The crossover from phonon-, to charged-impurity, limited conduction occurs once the concentration of gate-induced carriers is reduced below that of the residual carriers. In bilayer graphene, the resistance exhibits a monotonic decrease with increasing temperature for all densities, with the importance of short-range impurity scattering resulting in a "universal" density-independent (scaled) conductivity at high densities. At lower densities, the conductivity deviates from this universal curve, pointing to the importance of thermal activation of carriers out of charge puddles. These various assignments, in both systems, are made possible by an approach of "differential-conductance mapping", which allows us to suppress quantum corrections to reveal the underlying mechanisms governing the resistivity.

In spite of the interest that graphene has attracted over the past decade[1], the manner in which different scattering processes combine to determine its electrical resistance remains a topic of investigation. The reason for this may be traced to the ultrathin structure of this material, which allows its conduction to be influenced by a variety of different scattering mechanisms[1–23]. Phonon-mediated scattering, for example, can be generated by graphene's intrinsic modes[2–9], but can also be due to rippling[4, 10, 11] or the underlying substrate[5, 12, 13]. Impurity scattering, on the other hand, is usually attributed to the presence of long-range charged impurities in the dielectric substrate[13–19], and of short-range neutral defects in the graphene itself[15, 16, 18, 20, 22]. Collectively, these mechanisms may combine to yield complicated variations of the resistance as a function of both temperature (T) and carrier density (n & p for electrons and holes, respectively). A problematic task in experiment is that of separating out the different contributions, a job that is made all the more challenging at low temperatures by the emergence of quantum corrections[24–29]. Most notable of these are those arising from weak (anti) localization[24–27] and electron-electron scattering[28, 29], although Kondo physics has also been invoked to account for the behaviour observed in this regime[30–34].

In conventional semiconductors near room temperature, and with modest levels of doping, phonon scattering is typically the dominant process limiting carrier mobility (μ). The situation in graphene is more complicated, however, not only for the reasons identified above. Electrons and holes reside on a two-dimensional Dirac cone, placing significant phase-space restrictions on electron-phonon scattering[7, 35–37]. The large (>160 meV) energy of the graphene optical modes is additionally understood to suppress their importance, and the overall message is that phonon scattering is weak[35–37]. Room temperature mobility as large as ~20,000 cm^2/Vs is therefore expected for graphene on SiO_2[17, 19], while experiment has demonstrated values an order of magnitude larger for suspended layers[4, 6]. In many other experiments (performed with graphene on SiO_2), however, observed mobility values may

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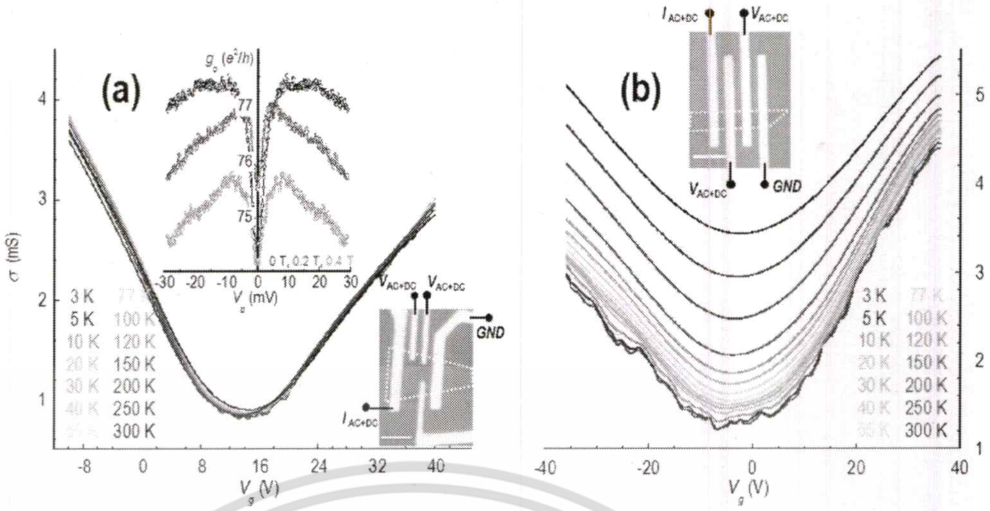

Figure 1. Variation of linear conductivity with gate voltage (V_g) for the monolayer (panel (a)) and bilayer (panel (b)) devices at various temperatures in the range of 3–300 K. Optical micrographs of the two devices are shown in the corresponding insets, in both of which the outline of the graphene flake is indicated by the white dotted line and current and voltage probes are indicated. The scale bar denotes a distance of 4 μm. The upper inset to panel (a) shows the differential conductance of the monolayer device as a function of drain bias at 3 K, and for three different values of magnetic field (indicated).

be smaller than 1000 cm^2/Vs[38, 39], suggesting that the contribution to the resistivity from impurity scattering can be much more important than in conventional semiconductors.

In this article, we study the resistance of graphene/SiO$_2$ transistors over a wide range of temperature (3–300 K), and for densities spanning the electron and hole branches of the Dirac cone. Due to their different energy dispersions, the importance of Coulomb and short-range impurities is expected to be very different in monolayer and bilayer graphene[22]. We therefore perform a comparative study of transistors fabricated with these materials. While prior work has largely focused on the resistance variations exhibited by graphene under linear transport[2–23], far fewer studies[40–44] have applied differential-conductance measurements to this problem. Here we use measurements of differential-conductance, performed as a function of temperature, density and drain bias, to identify the different contributions to graphene's resistance. Crucially, this allows us to identify resistivity contributions, free of the influence of quantum corrections. Our findings in both the monolayer and bilayer systems are in good agreement with the theories[1, 20, 22, 23, 45] proposed by Das Sarma and his colleagues.

Results

Linear Conductance of Monolayer and Bilayer Graphene.

We begin our discussion by first of all addressing the temperature dependence of graphene's linear transport, a problem that has previously been widely investigated[2–23]. To make a direct connection to these earlier works, in Fig. 1 we plot the variation of the conductivity, as a function of gate-voltage (V_g) and temperature. In Fig. 1a we show that the conductivity of monolayer graphene is only weakly dependent on temperature, while in Fig. 1b the bilayer shows a much stronger variation. The weak temperature dependence observed in the monolayer indicates that the dominant source of resistivity in this material, at all densities, is long-range Coulomb disorder. According to ref. 4, the contribution to the resistivity due to this mechanism should not depend on temperature below 300 K. This is in contrast with our results for the bilayer system, which shows a pronounced increase in overall conductivity with increasing temperature. The reason for this much stronger temperature dependence may be attributed to two factors, the first of which is that the thermal carrier concentrations increases much more strongly with increasing temperature in the bilayer. Secondly, due to the very different nature of screening in the two materials, scattering from short range defects, rather than Coulomb impurities, is expected to dominate in the bilayer, and is characterized by a strongly temperature-dependent nature[20, 22].

As a final comment, we note that Fig. 1 shows that, away from the Dirac point, the conductivity in both devices varies linearly with gate voltage (and so with *n* or *p*). While these variations might appear to suggest a common origin, in both materials, this, in fact, is not the case. Rather, the observed behaviour is completely consistent with what one expects when scattering in the monolayer is dominated by screened Coulomb impurities[4, 17–22], and that in the bilayer is governed by unscreened short-range disorder[22].

Differential-Conductance Mapping of Monolayer and Bilayer Graphene.

While linear transport provides a useful tool to reveal the role of different scattering mechanisms, for a more complete picture, offering energy resolution, it is necessary to make use of nonequilibrium studies. It is this approach that we apply here, where we perform differential-conductance mapping of graphene, as a function of drain bias, gate voltage, and temperature. The value of this approach is highlighted in Fig. 2, where we show contour plots of differential conductance (g_d) as a function of these parameters. (More precisely, the plots show differential resistance g_d^{-1}, since it

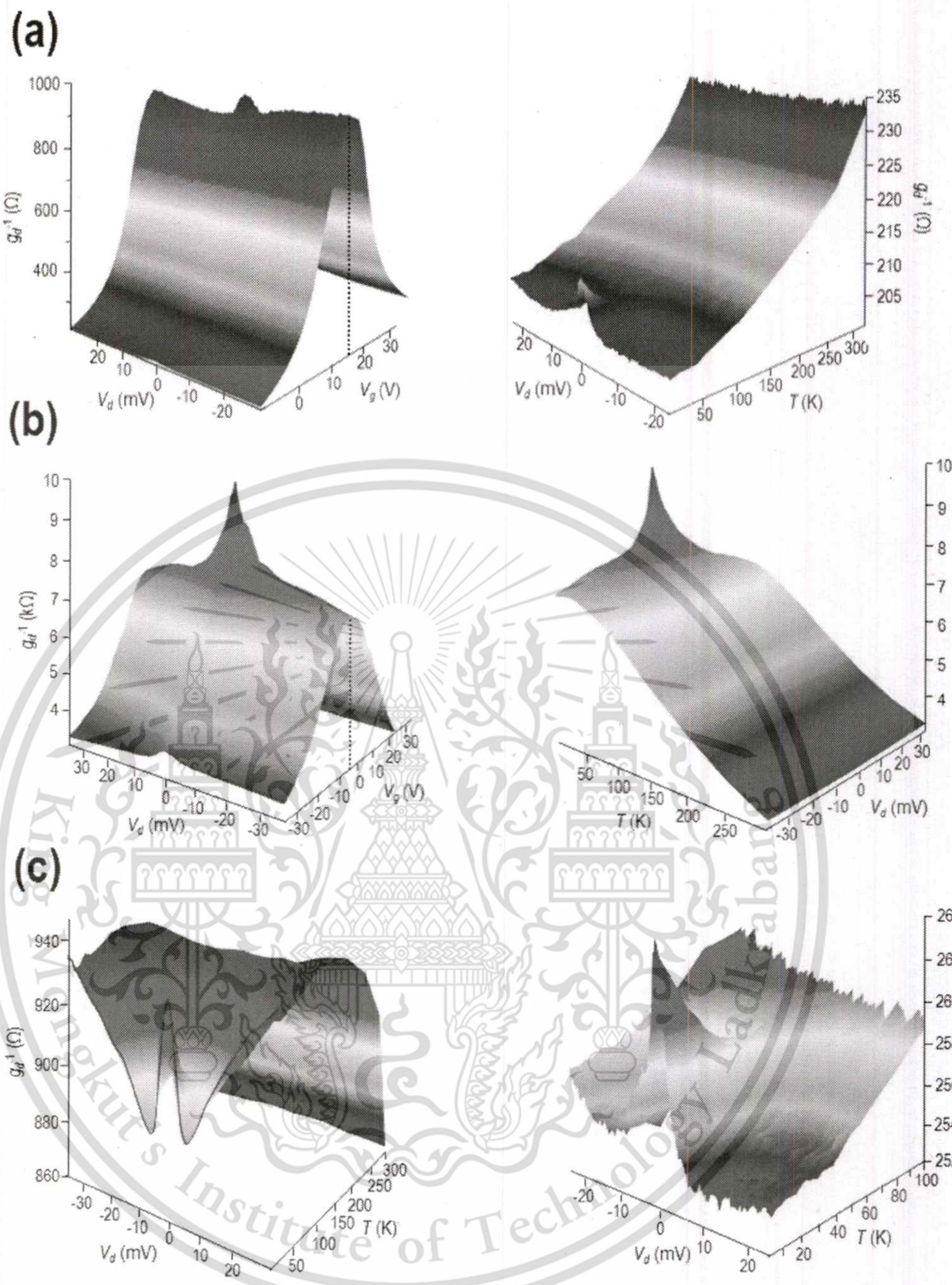

Figure 2. Differential conductance mapping of the monolayer (panel (a)) and bilayer (panel (b)) devices. The contour shown on the left-hand side of each of these two panels plots the full evolution of the differential resistance (g_d^{-1}) as a function of V_d and V_g at $T = 3$ K. The dotted lines indicate the position of the Dirac point. The contours shown on the right-hand side of each panel plot the dependence of differential resistance (g_d^{-1} (V_d)) for fixed gate voltage and as a function of temperature. For the monolayer device the gate voltage was kept at −10 V corresponding to the induced hole density (n_g) of 1.7×10^{12} cm^{-2}, while for the bilayer device the gate voltage was −6 V and the induced hole density was 1.1×10^{11} cm^{-2}. (Note that these values are not the total hole concentrations, p, which were also determined by n^* and n_{th}). Panel (c) show the variation of differential resistance (g_d^{-1}) as a function of drain bias and temperature in the monolayer. The contour on the left is obtained for a gate voltage close to the Dirac point ($V_g = 14$ V), while on the right is obtained away from the same point ($V_g = -10$ V).

is more easy to resolve the different features of the resulting contours in this case.) Fig. 2a,b are for monolayer and bilayer graphene, respectively. While their left panels plot (at the lowest temperature of 3 K) the variation of g_d^{-1} as a function of V_d and V_g, the right-hand panels plot the differential resistance at fixed density (see figure caption)

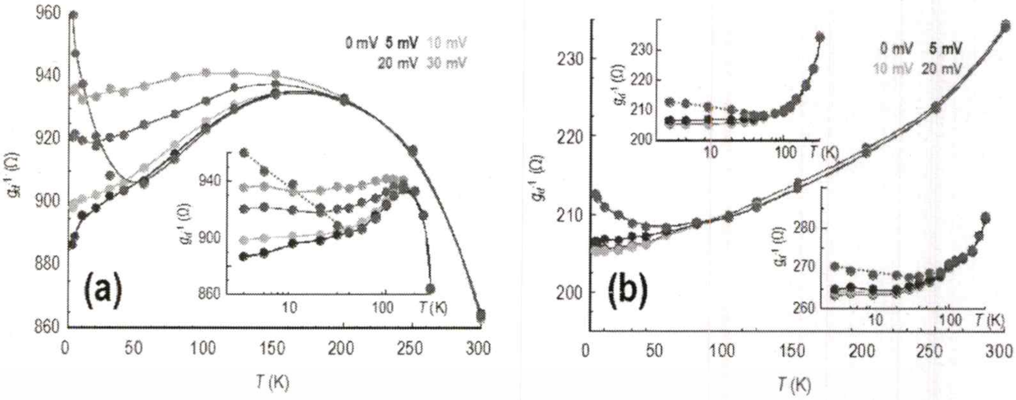

Figure 3. The main panels of (a) and (b) show the temperature dependent variation of the differential resistance ($g_d^{-1}(T)$) of the monolayer device, measured using various fixed values of the drain bias (indicated). Panel (a) is for a hole density close to the Dirac point ($V_g = 14$ V) and in the inset its data are re-plotted on a semi-log scale, highlighting the presence of a logarithmically-increasing contribution to the resistance at low temperatures and zero bias. Panel (b) is for a higher hole density (at $V_g = -10$ V) and its upper inset re-plots the same data of the main panel on a semi-log scale, once again highlighting the presence of a logarithmically-increasing contribution to the resistance at low temperatures and zero bias. In the lower inset we show a similar plot to the upper inset, but in this case obtained on the electron side of the Dirac curve ($V_g = +40$ V).

and as a function of temperature. The Dirac point is identified as a pronounced peak at $V_g = 14$ and $V_g = -5$ V, for monolayer and bilayer graphene, respectively, as indicated by the dotted lines in the left-hand panels. The main features of these contours are: (1) The zero-bias peak in differential resistance that is strongly suppressed with increasing temperature, washing out around 40–50 K; (2) The pronounced temperature-dependent variations of g_d^{-1}, away from the zero-bias peak, which appear to be of opposite sign for the monolayer and bilayer systems.

Zero-Bias Resistance Peak Due to Quantum Corrections. The zero-bias peak (Fig. 2) in the low-temperature differential resistance (g_d^{-1}) is consistent with the influence of quantum corrections, most notably weak localization and electron interactions[46]. As can be seen in the data of Fig. 2, the peak washes out around 40 K or so (this can be seen more clearly in the right panel of Fig. 2c), consistent with its origins in a quantum-coherent effect[46]. Furthermore, in the upper inset to Fig. 1a, we plot the differential conductance of the monolayer device at three magnetic fields. While the largest of these (0.4 T) should be sufficient to fully quench weak localization[28], the amplitude of the zero bias peak is only reduced by ~50% compared to its size at zero magnetic field. This indicates that this feature arises from a combination of weak localization and electron interactions, both of which become increasingly important as the temperature is lowered and carrier coherence is enhanced[46] (see Section S5 of the Supplementary Information).

To observe how the resistance is influenced by semiclassical contributions such as phonon, and charged-impurity, scattering, it is necessary to suppress the quantum corrections by suitable means. We achieve this here by measuring the variation of resistance in the presence of non-zero DC bias, as we demonstrate in Figs 3 & 4. The essential observation here is that, for $V_d = 0$, the resistance of both monolayer (Fig. 3a,b) and bilayer (Fig. 4a,b) graphene increases as a logarithmic function of decreasing temperature below ~40 K. This behavior is well known[46] for quantum corrections and can be quenched by measuring the temperature dependence of the resistance under non-zero DC bias. In Fig. 3a, for example, the zero-bias resistance measured (near the Dirac point) in monolayer graphene shows its logarithmic upturn below 50 K (also see the inset to the main panel). With a DC bias of 10 mV, however, the logarithmic upturn is completely suppressed and the resistance decreases continuously down to 3 K. A similar suppression is apparent for electron and hole densities far from the Dirac point (Fig. 3b, main panel and insets), as well as in bilayer graphene (Fig. 4a,b), and should result from the suppression of carrier phase coherence as the DC bias is increased. The essential point for the study here is that, by suppressing the influence of the quantum corrections, we are able to investigate the underlying sources of graphene's resistance.

Resistance Variations in Monolayer and Bilayer Graphene. Having described how the quantum corrections may be suppressed in our studies, in this section we focus in more detail on the resistance variations exhibited by the monolayer (Fig. 3) and bilayer (Fig. 4) devices. The most striking feature of Fig. 3a, in which we plot the results of measurements obtained with the Fermi level close to the Dirac point, is a nonmonotonic variation of the resistance (also see the contour in the left panel of Fig. 2c). Even with the quantum corrections suppressed at $V_d = 10$ mV, the resistance still exhibits this nonmonotonic character; increasing first as the temperature is lowered below 300 K, before crossing over to a metallic-like variation for which the resistance decreases below 150–200 K. A similar variation is apparent for larger voltages ($V_d > 10$ mV) but the resistance no longer drops at low temperatures, instead showing a tendency to saturation. This is presumably due to self-heating of the graphene carriers under the strongly nonequilibrium voltage[47]; the voltage of 20 mV, for example, corresponds

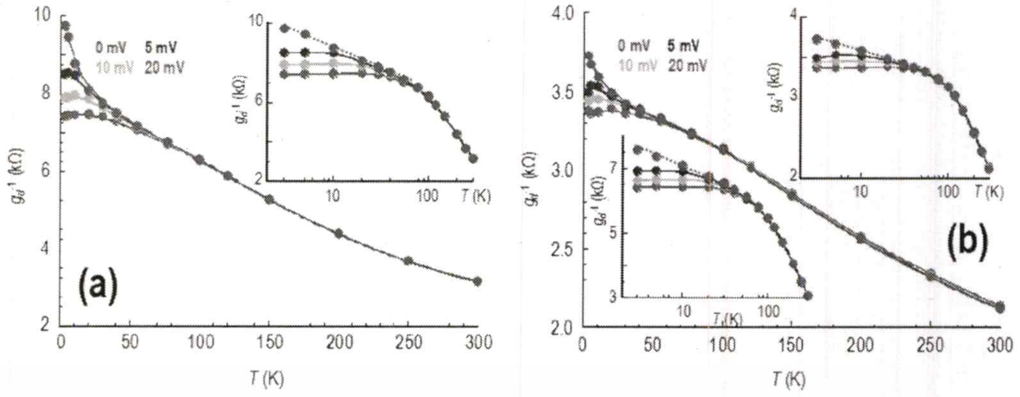

Figure 4. The main panels of (a) and (b) show the temperature dependent variation of the differential resistance ($g_d^{-1}(T)$) of the bilayer device, measured using various fixed values of the drain bias (indicated). In panel (a) the gate voltage is −6 V, while in panel (b) it is −36 V. The upper insets to panels (a) and (b) are plotted on a semi-log scale, highlighting the presence of a logarithmically-increasing contribution to the resistance at low temperatures and zero bias. The lower inset to panel (b) plots the corresponding resistance variation measured for a gate voltage of 6 V.

to an equivalent temperature of 200 K, consistent with the temperature below which the resistance saturates in Fig. 3a.

In Fig. 3b we show the corresponding variations of the resistance, exhibited by the monolayer system once the hole concentration has been adjusted to $n_g = 1.7 \times 10^{12}\,\text{cm}^{-2}$. With the quantum corrections suppressed by the application of the DC bias, the resistance at higher temperatures is characterized by a monotonically-increasing (metallic) variation. Similar behaviour is apparent, also, in the lower inset to Fig. 3b, where we plot the corresponding results obtained for an electron density of $1.9 \times 10^{12}\,\text{cm}^{-2}$.

While we have focused thus far on the behaviour exhibited by monolayer graphene, in panels (a) & (b) of Fig. 4 we plot a series of graphs that are the bilayer counterparts of Fig. 3a,b, respectively. Comparing the monolayer and bilayer devices, we immediately note that (with quantum corrections suppressed) the latter exhibits a much simpler, monotonic, decrease of resistance with increasing temperature. This insulator-like behaviour is observed both close to (Fig. 4a), and away from (Fig. 4b), the Dirac point. Similar results, obtained for another bilayer device, are presented in Section S6 of the Supplementary Information. Critically, the continuous increase of conductance with increasing temperature cannot be explained within any model of phonon-limited conduction in this material.

Discussion

Before discussing the implications of our experimental results it will be helpful to first of all summarize some of the theoretical predictions regarding the sources of resistivity in graphene. Phonons should always give rise to an increasing (metallic) resistivity with increasing temperature, with acoustic phonons providing a linear-in-T contribution over the range of interest here[3,5,7]. With regards to scattering from optical phonons, the large energies associated with these modes is often thought to render them unimportant at or below room temperature. However, recent first-principles calculations[8,9] based on density-functional theory suggest that, above ~200 K, optical-phonon scattering may actually become stronger than that due to the acoustic modes, resulting in a metallic resistivity that shows a more rapid increase than linear-in-T.

Impurity scattering in graphene is typically attributed to Coulombic impurities in the SiO_2 substrate and to neutral defects in the graphene layer. With regards to charged impurities, the influence of these is strongly dependent on the screening generated by carriers in the graphene. Screening enters the matrix element for the scattering process via the dielectric function, which in turn depends upon the polarizability of the material. The key point here is that the dependence of this function on temperature and scattering wavevector is very different in monolayer and bilayer graphene, resulting in very distinct screening properties in these materials[20,22]. Most notably, in monolayer graphene the polarizability shows a nonmonotonic dependence on temperature, which should give rise to a similarly nonmonotonic variation of the resistivity. Hwang and Das Sarma[20] have calculated this behaviour analytically, accounting for the influence of thermal carriers via usual Fermi-Dirac statistics, obtaining asymptotic expressions for the monolayer conductivity:

$$\sigma(T) \approx \sigma_0\left[1 - \frac{2\pi^2 r_s}{3}\frac{I_1}{I_0}\left(\frac{T}{T_F}\right)^2\right](T \ll T_F)\ \& \qquad (1)$$

$$\sigma(T) \approx \sigma_0\left[\frac{16I_0}{\pi}(4(\ln 2)r_s)^2\left(\frac{T}{T_F}\right)^2\right](T \gg T_F), \tag{2}$$

where $\sigma_0 = \sigma(T = 0)$, T_F is the Fermi temperature, r_s is the Wigner-Seitz radius and:

$$I_n = \int_0^1 \frac{x^2\sqrt{1 - x^2}}{(x + 2r_s)^{2+n}}. \tag{3}$$

When the explicit temperature dependence of the finite energy averaging of the scattering time is considered, and by taking $r_s = 0.88$ (for graphene on SiO_2), equation (1) is slightly modified to[20]:

$$\sigma(T) = \sigma_0\left[1 - \frac{\pi^2}{3}0.21\left(\frac{T}{T_F}\right)^2\right]. \tag{4}$$

Das Sarma *et al.* have also considered[22] the influence of temperature-dependent screening in bilayer graphene, and predict a metallic resistivity contribution at low temperatures ($T/T_F \ll 1$). A critical difference with the monolayer, however, is that scattering from short-range impurities is expected to be much more important in bilayer material. The short-range scatterers give rise to a strong insulating temperature dependence of the resistivity in this system, which can overwhelm any signature from charged impurities. (This is to be contrasted with monolayer graphene, in which the influence of short-ranged scatterers is only expected[20, 22] to be significant at very-high densities – $\sim 10^{13}$ cm^{-2} – once screening of the Coulomb impurities become fully effective.) While the resistivity correction arising from short-range scatterers can only be evaluated numerically, the authors of ref. 22. showed that this mechanism should give rise to an insulating variation of the scaled conductivity ($\sigma(T/T_F)/\sigma_0$) that is *independent* of density.

In later work[23, 45] by the Maryland group, the authors addressed explicitly the thermal activation of carriers out of localized puddles arising from the disorder background. Here the authors discussed the puddles as giving rise to a "two-component" model of transport; the first involving usual diffusive transport in the graphene layer, while the second involves the thermal activation of carriers out of the puddles. The activated transport is predicted[23, 45] to give rise to an insulating conductivity near the Dirac point in both monolayer and bilayer graphene systems (equations (5) & (6), respectively, valid when $k_BT < s$):

$$\sigma(T) = \sigma_0\left[1 + \sqrt{\frac{2}{\pi}}\frac{k_BT}{s} + \frac{\pi^2}{3}\left(\frac{k_BT}{s}\right)^2\right], \tag{5}$$

$$\sigma(T) = \sigma_0\left[1 + \sqrt{\frac{2}{\pi}}\frac{k_BT}{s} + \frac{\pi^2}{6}\left(\frac{k_BT}{s}\right)^2\right], \tag{6}$$

where s is the strength of the potential fluctuations in graphene and is typically expected to be in the range of 10–100 meV. The thermal activation is expected to be most significant in the bilayer system, in which the extent of puddle formation should be much stronger, leading to larger characteristic values of s[23, 45]. Nonetheless, evidence for the activation has been found in disordered, CVD-grown, monolayer graphene[48]. Here, the competition between thermal activation, temperature-dependent screening, and phonon scattering was found to result in a nonmonotonic variation of the conductivity, in the crossover regime between insulating and metallic states.

The presence of puddling in typical experiments usually obscures the intrinsic variations of the conductivity that are expected for graphene. Here, the conductivity near its Dirac point is predicted to follow the semiclassical transport theory proposed in ref. 49. According to this theory, which accounts for the influence of thermal excitation, screening, and scattering, the conductivity should be insulating in character, and follow a power-law variation as a function of temperature. While this behaviour is not observed in most experiments, such as those performed here where the graphene is supported on an SiO_2 substrate, there is evidence to suggest that it can be observed at sufficiently low densities in clean, suspended material[6, 50–53].

With this understanding, we now consider the implications of our experimental results in the light of the predictions above. We begin, in Fig. 5, by performing an analysis of the resistance variations observed in monolayer graphene, with a non-zero DC bias ($V_d = 10$ mV) applied to suppress its quantum-corrections. In the inset to Fig. 5a, we plot resistance as a function of temperature for a number of gate voltages on the hole side of the Dirac curve ($V_g \leq 14$ V). These data are re-plotted in the main panel of the figure, by rescaling them relative to their low-temperature resistance (at 3 K). Starting from a gate voltage of -10 V, the Fermi level lies well within the valence band (see Fig. 1a) and the resistance exhibits a metallic variation over the entire temperature range. As the gate voltage is increased towards the Dirac point (at $V_g = 14$ V), however, the resistance develops a nonmonotonic character, the onset of which appears at progressively lower temperatures for larger gate voltages. For $V_g = 6$ V, for example, the crossover to an insulating resistance occurs around 250–300 K; by the time the Dirac point is reached, however, the onset has shifted down to $\sim$150 K.

The data of Fig. 5a support a scenario involving a crossover from phonon-dominated conduction, when the Fermi level lies far from the Dirac point, to one in which transport is governed by scattering from screened Coulomb impurities when the Fermi level is near to this special point. In Section S4 of the Supplementary

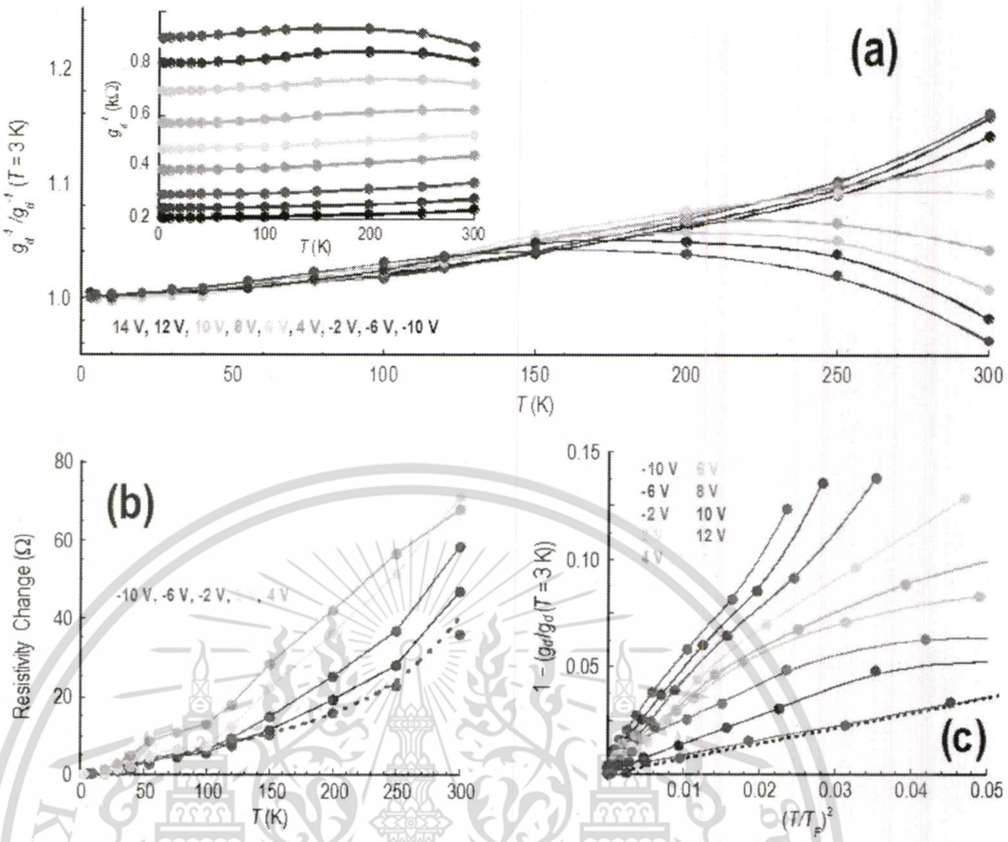

Figure 5. Temperature-dependent variation of the differential resistance ($g_d^{-1}(T)$, $V_d = 10\,\text{mV}$) of the monolayer device. (**a**) The inset shows the variation of differential resistance at several gate voltages (identified in the main panel), while in the main panel these data are re-plotted by normalizing them relative to the low-temperature ($T = 3\,\text{K}$) value. A crossover from monotonic to nonmonotonic behaviour occurs as the Dirac point (at $V_g = 14\,\text{V}$) is approached from the hole band. (**b**) The temperature-dependent change of resistivity (measured relative to the value at 3 K, $V_d = 10\,\text{mV}$, gate voltages indicated) for selected data from panel (a). The dotted line in the figure is an extrapolation of data presented in the theoretical study of refs 8 & 9. (**c**) The data of panel (a) are replotted to reveal the connection to the predictions of equation (4). The dotted line in the figure is the straight-line variation expected from this equation with $r_s = 0.88$.

Information, we include a table relating the different gate voltages to the corresponding electrostatically-induced concentrations (n_g) that they imply. From this table, we see that the data in this figure span a wide range of carrier density, from $n_g \sim 2 \times 10^{12}\,\text{cm}^{-2}$ in the highest case to almost $n_g \sim 0$ near the Dirac point (at $V_g = 14\,\text{V}$). In Fig. 5b, we then address the origins of the resistance variations observed well away from the Dirac point, by plotting the temperature-dependent change of resistivity (relative to its value at 3 K). At these hole concentrations ($>7 \times 10^{11}\,\text{cm}^{-2}$), the gate-induced carrier density is larger than that due to both residual impurities (n^*) and thermal carriers (n_{th}), even at room temperature. (For a further discussion of this point see Section S4 of the Supplementary Information, where we also show how consistent estimates for the residual impurity density can be obtained from a Raman analysis – see Fig. S1 – or from the features of the Dirac curve – see Fig. S4). In this limit we find that the resistance shows purely metallic behaviour, increasing monotonically with increasing temperature. At the same time, as n_g is increased through variation of the gate bias in this figure, the overall resistance level systematically decreases. The dotted line included in the figure represents an extrapolation of the data of Park *et al.*, who have calculated the phonon-limited resistivity for graphene by first-principles methods[8, 9]. Their calculations employ both density-functional theory, and density-functional perturbation theory, to compute all electronic and phononic properties, including the influence of resultant electron-phonon coupling. The dotted line in Fig. 5b clearly agrees well with our experimental data for the gate voltage of −10 V (corresponding to a hole density of $n_g = 1.7 \times 10^{12}\,\text{cm}^{-2}$). According to Park *et al.*, the phonon-limited resistivity is governed by acoustic modes at low temperatures, whereas at temperatures above ~150 K the role of optical phonons becomes more important. It is this crossover in scattering that we attribute to the rapid upturn of the resistivity seen in experiment beyond 150 K. From this analysis we therefore conclude that, when the concentration is dominated by the influence of gate-induced carriers, the resistivity of graphene is essentially determined by phonon scattering. This situation changes when the gate-induced concentration of carriers decreases, however, as we now discuss.

As the gate voltage is increased beyond 6 V in Fig. 5a, the hole concentration drops below $n_g = 5 \times 10^{11}\,\mathrm{cm}^{-2}$ and it is clear that the scaled resistance deviates from a purely metallic variation that is the signature of electron-phonon scattering and develops, instead, a nonmonotonic dependence on temperature. The onset of this behaviour initially occurs near room temperature, but decreases to ~150 K as $n_g \to 0$. A clue as to the origins of this nonmonotonicity, is provided again in Section S4 of the Supplementary Information. This figure shows that, for $n_g < 5 \times 10^{11}\,\mathrm{cm}^{-2}$, one enters a new regime where the full carrier concentration is strongly modified by the contribution from charged-impurity induced residual carriers. On the basis of these observations, we attribute the nonmonotonic variations seen in Fig. 5a to the role of scattering from screened Coulomb impurities, as predicted by Hwang and Das Sarma[20]. To establish this point, in Fig. 5c we have rescaled the data from Fig. 5a to reveal a connection to equation (4). The graph focuses on the low-temperature limit ($T << T_F$), where the prediction of equation (4) is expected to be valid[20], and the dotted line in the figure represents the universal variation this describes (for $r_s = 0.88$). It is clear that good agreement with this line is obtained for the lowest density studied, where the gate-induced concentration ($n_g = 1.4 \times 10^{11}\,\mathrm{cm}^{-2}$) is in fact smaller than that ($\sim 2 \times 10^{11}\,\mathrm{cm}^{-2}$) due to the Coulomb impurities. As the gate voltage is used to produce heavier hole doping, however, the conductance rises rapidly above the dotted line in Fig. 5c. The suggestion of these results is therefore as follows. At the lowest density that we study ($n_g < 5 \times 10^{11}\,\mathrm{cm}^{-2}$), the resistivity data closely follow the universal variation expected[20] for scattering from screened Coulomb impurities, indicating that this mechanism dominates over phonon scattering in this limit. As the density is increased, however, the data in Fig. 5c rise above the universal curve, indicating that an additional mechanism is contributing significantly to the resistivity. This mechanism is presumably due to phonon scattering, which grows to eventually dominate the measured resistance once the density becomes sufficiently large ($n_g > 10^{12}\,\mathrm{cm}^{-2}$).

While in the above discussion we have characterized our results in terms of "metallic" and "insulating" resistivity variations, it must be emphasized that this has nothing to do with a metal-insulator transition. Indeed, even with the nonmonotonic character of the resistance manifested most strongly near the Dirac point, the minimum conductivity achieved in the monolayer is $\sim 20\, e^2/h$ per square (see Sections S1 & S3 of the Supplementary Information). The graphene is therefore metallic at all densities studied, and the observation of "metal-like" and "insulator-like" resistance variations simply reflects the competition between the different scattering mechanisms noted above.

Turning to the variations exhibited by bilayer graphene, these are somewhat easier to analyse since they show no evidence of any metallic variation that would provide a signature of electron-phonon scattering. The first point we note from Fig. 1 is that the overall conductivity in bilayer material is much lower than that in the monolayer, a difference that is commonly observed in experiment and which is attributed to differences in the density of states and screening properties of these materials[54]. The different density of states is also responsible[54] for the increased importance of thermal carriers in the bilayer system, relative to the monolayer (see Section S3 of the Supplementary Information). As we indicate in Fig. 6a, where we plot the variation of resistance with temperature for electrons, the resistance of this material therefore shows insulating variations for all temperatures and densities. This appears consistent with the predictions for scattering from short-range defects in bilayer material[22]. As described above, the signature of such scattering in the bilayer should be a density-independent variation of the scaled conductivity ($\sigma(T/T_F)/\sigma_0$). This behaviour can be clearly seen in the main panel of Fig. 6b, where we plot rescaled differential conductance as a function of T/T_F for a number of electron densities in the range of $n_g = 1.2 - 2.9 \times 10^{12}\,\mathrm{cm}^{-2}$ (see the table included in Section S4 of the Supplementary Information for the correspondence of V_g to n_g for the bilayer). Over this density range, where the contribution from gate-induced carriers dominates the total electron or hole density (see Section S4 of the Supplementary Information), the data clearly fall on a common curve expected for short-range scatterers[22]. This is obviously very different to the behaviour discussed for monolayer graphene, in which the resistivity at higher densities was instead dominated by electron-phonon scattering (Fig. 5b). This may be understood in terms of the different screening properties of monolayer and bilayer graphene[22]. In the inset to Fig. 6b, we extend our analysis by including data for lower electron densities ($n_g = 0.1–1.2 \times 10^{12}\,\mathrm{cm}^{-2}$) than those in the main panel. Here it is clear that the data progressively deviate from the density-independent curve, as n_g is reduced to $1.0 \times 10^{11}\,\mathrm{cm}^{-2}$. Since this concentration corresponds to the situation where $n_g < n^*$, one might expect that the transport should be increasingly limited by puddling behaviour associated with charged background impurities. Consistent with this, in this regime, we find that the temperature dependence of the conductance is well described by the prediction of equation (6) for two-component transport[23,45]. This is shown in Fig. 6c, where we are able to fit the data near the Dirac point with a reasonable[23,45] estimate ($s = 35$ meV) for the potential-fluctuation strength.

In conclusion, in this article we have explored the contributions to the resistance of monolayer and bilayer graphene transistors. Our studies have revealed transitions between different regimes of scattering, as a function of density, temperature, and of the material system, the details of which appear consistent with the predictions of theory[1,20,22,23,45]. In monolayer graphene, the temperature dependence of the resistivity near the Dirac point appears to arise predominately from scattering from screened Coulomb impurities, whereas at higher densities it shows signatures of acoustic and optical phonons. In bilayer graphene, short-range impurities dominate the temperature-dependence of the resistivity for nearly all densities. The exception to this behaviour arises near the Dirac point, where thermal activation out of charge puddles becomes significant. A key approach here has been the application of differential-conductance measurements to suppress the influence of quantum corrections, which has allowed us to identify the various transport regimes relevant to these materials. This approach is expected to be broadly applicable to other low-dimensional materials, and should find application, for example, in the study of transition-metal dichalcogenides and topological insulators.

Methods

Graphene devices were fabricated by exfoliating Kish graphite onto a doped Si substrate with a 300-nm SiO_2 cap layer, and an underlying, heavily-doped, Si layer that served as a back gate[47]. Individual graphene flakes

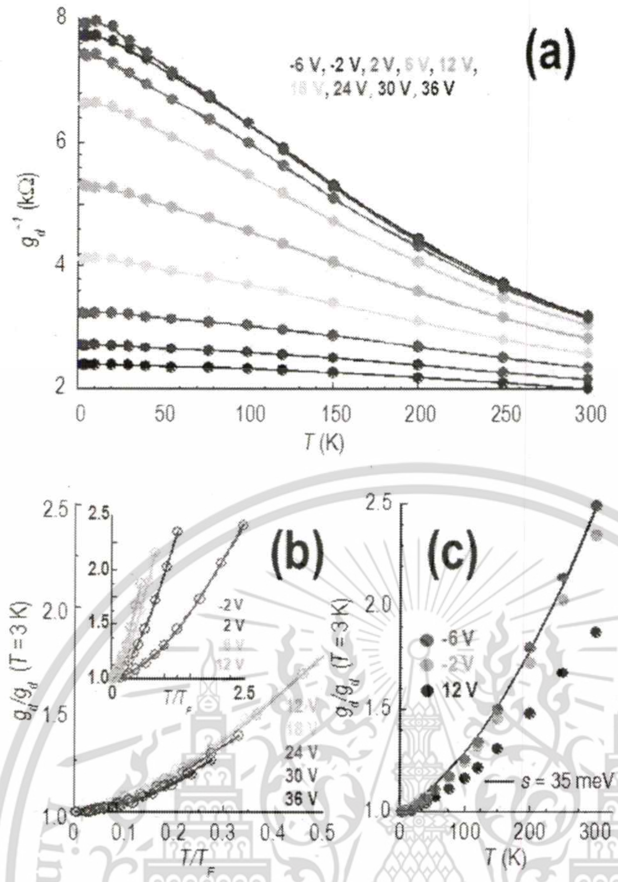

Figure 6. Temperature-dependent variation of the differential resistance ($g_d^{-1}(T)$, $V_d = 10\,\text{mV}$) of the bilayer device. (**a**) g_d^{-1} as a function of T for several gate voltages on the electron side of the Dirac curve. (**b**) Variation of the rescaled differential *conductance* ($g_d/g_d(T = 3\,\text{K})$) as a function of T/T_F for several gate voltages on the electron side of the Dirac curve. Inset: Same as in main panel but for a wider range of V_g. (**c**) Selected data from the inset to Fig. 6b are replotted to compare with the theoretical prediction (solid line) of the two-component transport model of refs 23, 45.

were then contacted with Cr/Au (3-/50-nm) electrodes, defined by electron-beam lithography and lift-off. Layer identification was achieved through a combination of optical microscopy and Raman imaging (see Section S2 of the Supplementary Information). Various devices were fabricated, and characterized electrically, and in the Supplementary Information we show how these exhibited similar and consistent characteristics, independent of the contact configuration used (see Section S1 of the Supplementary Information). In this report, we focus on a detailed study of the differential conductance exhibited by two representative devices, one monolayer and the other bilayer. Optical micrographs of these devices can be seen in the insets to Fig. 1. The various measurements reported here were performed in a four-terminal geometry, thereby eliminating the influence of any contact resistance. In the micrographs of Fig. 1 we indicate how this was achieved, by denoting the two contacts that were used to apply an external (AC and/or DC) voltage(s), and the two internal probes that were then used to measure the resulting voltage drop (v) across a region that then served as our channel. Two different kinds of measurement were made in this study; linear conductance (or resistance) was determined by a low-frequency (13-Hz) AC technique, using a small AC signal ($v_d = 100$-μV RMS) as the externally-applied voltage. For measurements of differential conductance (g_d), a DC voltage (V_d) of varying amplitude was applied on top of this AC component, allowing us to perform differential-conductance spectroscopy as a function of both V_d and gate voltage (V_g). An important point that must be emphasized here is that, in all figures and associated text, indicated values of V_d are those applied *directly* to the graphene region under study. These values are determined by utilising the small-signal AC measurements as a calibration; with a knowledge of v_d, the external-circuit components, and our measurement of the actual AC voltage drop (v) across the graphene channel, we define a ratio (v/v_d) that we use to determine the actual DC voltage drop across the channel ($V_d = V_d^{appl} \times (v/v_d)$). In this expression, V_d^{appl} is the DC voltage applied to the outer contacts of the device. Finally, to suppress the influence of quantum corrections, the differential conductance or resistance (g_d^{-1}) was measured by applying a small, but fixed, value of V_d and subsequently determining the variation of $g_d(T)|_{Vd}$ or $g_d^{-1}(T)|_{Vd}$.

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Author Contributions

R.S., H.R., and G.H. fabricated the graphene transistors, and R.S., H.R., J.N. and C.-P.K. measured their temperature-dependent electrical characteristics. J.N. and N.A. performed Raman microscopy of the devices. R.S., H.R., G.H., J.N., C.-P.K., Y.-H.L., and J.P.B. collaborated on the design of the experiments. R.S., H.R., J.F. and J.B.P. analysed the data and collaborated on the writing of the manuscript.

Additional Information

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Probing charge trapping and joule heating in graphene field-effect transistors by transient pulsing

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Abstract

We use pulsed electrical studies to investigate the various processes that limit the current carrying capacity of graphene high frequency transistors. By investigating the transient response of these devices over a time scale that spans some twelve orders of magnitude, we identify the presence of four distinct processes that degrade the current: (1) charge injection into deep traps within the interior of the oxide; (2) Joule heating of the transistor substrate by hot carriers in the graphene channel; (3) equilibration of interfacial-state filling in response to voltage transients, and; (4) leakage of captured charge from the deep traps, once the pulsed voltage is removed. The time scale associated with these processes ranges from nanoseconds to hours, with process (1) being the fastest and process (4) the slowest. By pulsing the transistors on time intervals as short as a few nanoseconds, we therefore demonstrate how it is possible to obtain output characteristics from them that are essentially free from the influence of these different mechanisms. Under such conditions, the hot-carrier drift velocity is shown to saturate at the large values expected for intrinsic graphene. Beyond graphene, this approach of pulsed characterization of transistor performance should be broadly applicable to studies of other two-dimensional semiconductors, including transition-metal dichalcogenides, black phosphorous, silicene, and topological insulators.

Keywords: graphene, high-field properties, velocity saturation, transient transport

(Some figures may appear in colour only in the online journal)

1. Introduction

The current carrying capacity of semiconductor devices is limited by a number of different processes, whose origins may be either intrinsic or extrinsic [1–13]. The dominant intrinsic effect is due to the scattering of hot carriers by optical phonons, a process that sets the upper attainable limit for the drive current that can be carried by such devices. Typically, however, this optimal performance is not realized in practice, due to the presence of a number of additional, extrinsic mechanisms. Prevalent among these are the injection of energetic ('hot') carriers into the surrounding dielectric layers of the device, and Joule heating of these layers that is driven by energy exchange with the transistor channel. All of these problems are exacerbated as the internal electric fields within small devices are increased through a process of scaling.

The extrinsic degradation of transistor current described above is even more acute in devices formed from emergent two-dimensional (2D) materials, for example those based on graphene [14–16] and the transition-metal dichalcogenides [17, 18]. In such devices, the electrical performance is easily impacted by the interaction of 2D carriers with the underlying substrate [1–9]. In graphene-on-silicon-dioxide back-gated transistors, for example, hot electrons (or holes) may be injected from the transistor channel, into different traps that may be present at the interface between the graphene and the gate oxide, or within this dielectric itself (figure 1(a)) [10–13]. The charging and discharging of these various states can be expected to be characterized by very different time scales, dependent upon the manner in which the transistor is biased. Previous work has highlighted the role that the traps play in generating hysteresis in the electrical characteristics, behavior that arises when hot carriers injected into the traps from the graphene remain localized, even when the drain bias is removed [10].

A completely different issue to that of charge trapping is Joule heating of the device, by which we refer to the process in which heat generated in the graphene channel is transmitted to its surrounding environment (most notably to its underlying substrate). Realistic simulations of the thermal transport in this problem [5] have previously shown that both heating and cooling of the substrate should occur over long time scales, on the order of a hundred to a few hundred nanoseconds (for the types of devices that we study here). Consequently, such Joule heating can be expected to result in pronounced, and undesirable, transients in the electrical response.

The processes of charge trapping and Joule heating described above may be active simultaneously in small devices, making the analysis of their resulting electrical behavior particularly complicated. One way to resolve this problem, however, is to make use of transient measurements, in which controlled electrical pulsing of the device may be used to identify the separate influence of these different processes. Motivated by this idea, there have previously been several reports in which electrical pulsing has been utilized to investigate the transient performance of graphene transistors [4, 10–13]. While these works have provided useful insights into the dynamics of carrier action in graphene transistors, they have generally suffered from limited temporal bandwidth and so have not explored the full spectrum of mechanisms responsible for current degradation. In this article, we therefore present the results of detailed experiments in which we investigate the transient response of graphene transistors over a time scale that ranges from nanoseconds to hours (i.e. over twelve orders of magnitude). Through this approach, we are able to identify the characteristic time scales on which different processes of carrier trapping (and release), and Joule heating, occur. More specifically, our measurements employ a scheme of repetitive pulsing (figure 1(b)), in which control of the pulse duration (τ) and of its repetition frequency allows these distinct processes to be separately manipulated.

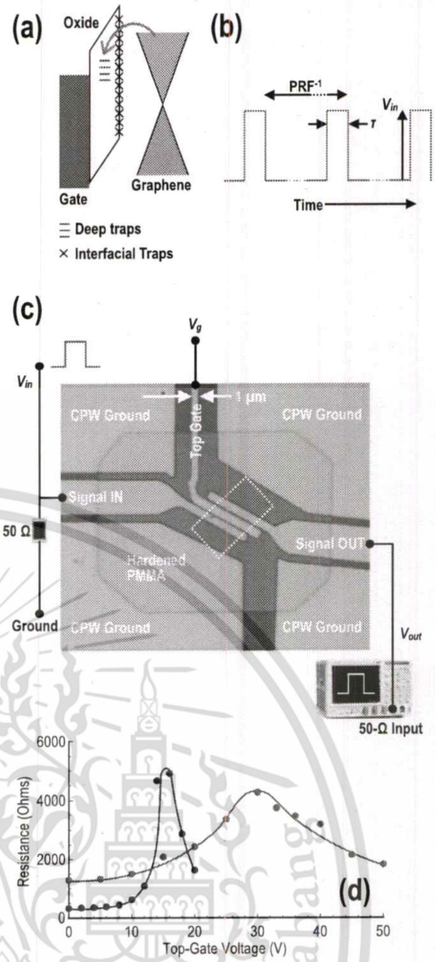

Figure 1. (a) Hot-electron trapping mechanisms in generic graphene-on-SiO$_2$ devices, indicating the separate influence of interfacial states and of deep traps in the oxide itself. (b) Schematic representation of the pulsed measurement scheme, which is based upon a periodic sampling technique. The input pulse is applied repetitively to the sample at a defined pulse repetition frequency (PRF), and the sampling oscilloscope builds up the measured output pulse by acquiring a large number of such pulses. In addition to V_{in} and the PRF, another important parameter that is varied in experiment is the pulse duration (τ). (c) An optical micrograph of one of the studied devices (D2), indicating the methodology of the pulsed measurements utilized here. A voltage pulse (V_{in}) generated by a fast generator is applied to the signal input of the graphene FET, following which it is collected (V_{out}) at the 50 Ω input of a 50 GHz bandwidth digital sampling oscilloscope. As such, V_{out} is proportional to the time-dependent current flowing through the transistor. The rectangle denoted by the white dotted line surround the area inside of which the graphene flake bridges the input and output contacts. The top gate in the figure is isolated from the graphene layer by ~120 nm of electron-beam hardened PMMA (indicated). A DC voltage (V_{g}) applied to the top-gate was used to vary the electron (or hole) density in the graphene channel. (d) Resistance versus V_{g} for two devices (Device D3—blue; Device D4—red), determined from transient measurements under conditions where trapping and self heating are suppressed. Solid lines through the experimental data points are guides to the eye.

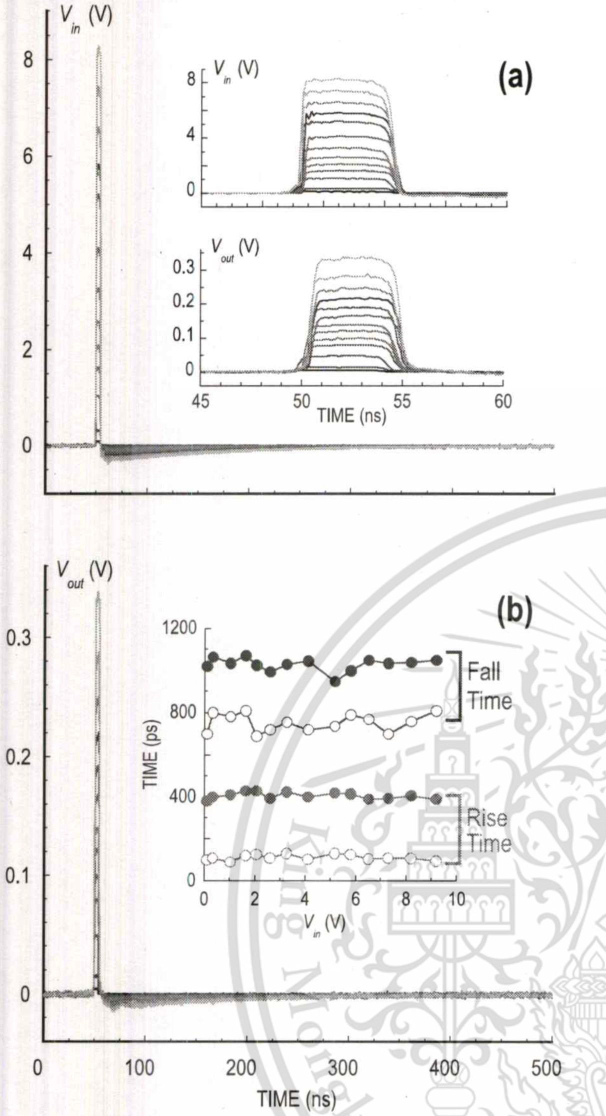

Figure 2. Demonstration of the pulsed measurement capabilities. Panel (a) shows a sequence of input pulses generated by the AVTECH supply, while panel (b) shows the output pulses measured at the oscilloscope after applying the input signal to Device D2. (These pulses therefore represent the time-dependent current flowing through the device.) In the inset to figure 2(a), we compare the input and output pulses over the smaller time range where the pulse is applied. In the inset to figure 2(b), we compare the rise and fall times of the input (open circles) and output (filled circles) pulses. The rise and fall times are defined as the usual 10%–90% times.

The remainder of this article is organized as follows. In the next section we outline the essential experimental methods of this study, including the fabrication and design of the microwave graphene FETs that we study. In section 3 we present our main results, which demonstrate the use of transient pulsing to investigate the dynamics of carrier trapping and Joule heating. We also discuss how, by suitable tailoring of the pulse characteristics, we may drive the devices on time scales faster than those associated with either of these processes. In this way, we are able to investigate the high-field velocity saturation that sets the upper intrinsic limit on the current that can be carried in the graphene channel. The implications of our results are then described in section 4, along with our conclusions.

2. Experimental methods

Rapid pulsing of graphene FETs was performed at room temperature in an impedance-matched setup [19], in which electrical contact to Kish graphene flakes, exfoliated onto 300 nm thick SiO_2 substrates, was provided by an on-chip coplanar waveguide (figure 1(c)) architecture. The carrier density in these devices was varied by means of the voltage (V_g) applied to their aligned top-gate (see also figure 1(c)), which was isolated from the graphene by some 120 nm of (electron-beam) hardened PMMA [19].

Illustrative curves, demonstrating the variation of the small-signal resistance as a function of the gate voltage, are presented in figure 1(d). In our studies of velocity saturation in graphene (see section 3.4 below), various voltages were applied to the top gate in order to vary the carrier density in the channel. For our studies of current degradation due to charge trapping and Joule heating, however, we typically simply observed the behavior with the gate held grounded (i.e. at $V_g = 0$ V). Five different devices (D1–D5) were investigated here, with D2–D5 being monolayer while D1 was realized from bilayer graphene. Room temperature mobility values exhibited by these devices were in the range of 2000–5000 $\mathrm{cm^2\,V^{-1}\,s^{-1}}$ (at a reference carrier density of $\sim 1.5 \times 10^{12}\ \mathrm{cm^{-2}}$), typical of graphene devices deposited on SiO_2. The channel length (L) and width (W) of these devices were as follows: D1 ($L = 1.5\ \mu$m, $W = 3.8\ \mu$m), D2 ($L = 1.1\ \mu$m, $W = 4.0\ \mu$m), D3 ($L = 1.4\ \mu$m, $W = 7.1\ \mu$m), D4 ($L = 0.8\ \mu$m, $W = 3.0\ \mu$m), D5 ($L = 1.4\ \mu$m, $W = 1.8\ \mu$m).

Pulsed I–V studies of the devices performed using a custom-designed setup with full (50 Ω) impedance matching. The system employed semi-rigid coaxial cables to connect a FR-4 laminate carrier, on which the device was mounted, to a pulse generator and broadband oscilloscope [19]. The AVTECH™ generator was used to source repetitive pulses of various amplitude (up to 10 V), width and repetition frequency (10 kHz–1 MHz) to the device. The resulting output pulses were then captured by a TEKTRONIX™ CSA8000B digital sampling oscilloscope, using a 50 GHz bandwidth module. In contrast to a single-shot measurement, in this scheme output pulses are constructed by repetitively capturing transient data while the device is subjected to periodic excitation. For further details on this setup, we refer the reader to [19, 30].

3. Results

A schematic illustration of the broadband setup used to propagate high frequency signals to and from the graphene transistor is indicated in figure 1(c), along with an optical micrograph of one of the measured devices. As noted already, the essential idea of the transient measurement involves applying periodic pulses between the source and drain contacts of the transistor, and measuring the resulting time-dependent variation of the drain current through a process of repetitive sampling [19]. In such experiments, the key parameters governing this variation are therefore the amplitude (V_{in}, see figure 1(c)) and duration (τ) of the input pulse, as well as its PRF. In this article, we focus on exploring how systematic variation of these parameters may be used to investigate phenomena arising from charge trapping and self heating in graphene devices.

To illustrate the capabilities of our measurement setup, in the main panel of figure 2(a) we show a series of input pulses of varying amplitude, which were generated by the AVTECH supply and then fed directly into the 50 Ω input of our oscilloscope. The duration of these pulses is approximately 4 ns, while their waveform is indicated over a time scale of 500 ns to demonstrate the absence of unintended reflections due to parasitic elements. A systematic undershoot (of <10%) can be seen at the end of each pulse, and represents a limitation of the pulse generator. In the main panel of figure 2(b), we show the output pulses detected at the oscilloscope, after connecting the pulse generator to a device-under-test. Inspecting these waveforms over the same wide time base, it is clear that there are no unintended features in the output due to parasitics. The undershoot noted above is reproduced nicely in the outputs, indicating the high degree of integrity of our pulsed setup. This point is further confirmed by the insets to figure 2(a), where we compare the form of the input and output pulses over a time window matching that of the pulses themselves. Once again, it is clear from this comparison that the output pulses clearly capture the key features of the input signals. In the inset to figure 2(b), we quantify this comparison by plotting the rise (open circles) and fall (filled circles) times of the input and output pulses. From these measurements we can see that the measurement setup used to evaluate the devices introduces a delay of order 200 ps. Since this time scale is very much shorter than the pulse durations that we will investigate here, in the discussion that follows we present as-measured output pulses without subjecting them to any additional signal processing.

3.1. Hot-carrier trapping in graphene devices

The first issue we address concerns the use of transient pulsing to explore the dynamics of carrier trapping, which occurs when hot electrons in the graphene channel are unintentionally injected into different localized sites. There are two different types of trap that are expected to be important in these devices [10, 11]; those located at the interface between the graphene and the gate dielectric (the crosses in figure 1(a)), and deep traps within the dielectric itself (the solid lines in figure 1(a)). The different physical nature of these traps is expected to cause them to exhibit very different transient characteristics. Since the deep traps are separated from the graphene channel by a large tunnel barrier, they are unlikely to capture charge while the transistor is unbiased. The pulsed voltage may be used, however, to lower this barrier, and to promote the rapid tunneling of carriers into the deep traps (figure 1(a)). Once this voltage is removed, excess charge stored on the traps will initially remain there, leaking back to the channel only very slowly due to the large barrier that once again blocks their transfer. That is, charging and discharging of the deep traps is expected to be governed by very different time scales (i.e. very fast versus very slow). In the case of the interfacial traps, the situation should be quite different. Since these states are located very close to the graphene channel, without any intervening potential barrier, they are easily accessible under all biasing conditions. Consequently, the filling of these states is determined by a steady-state balance, which arises from a competition between their population and depopulation. When the pulsed voltage is used to instantaneously change the electrochemical potential in the graphene, this balance is momentarily disrupted. Some time is then required for the filling of the interfacial traps to reach a new steady-state, in a process that is once again driven by the competition between population and depopulation. The challenge here is to determine the characteristic time scale on which this re-equilibration is achieved.

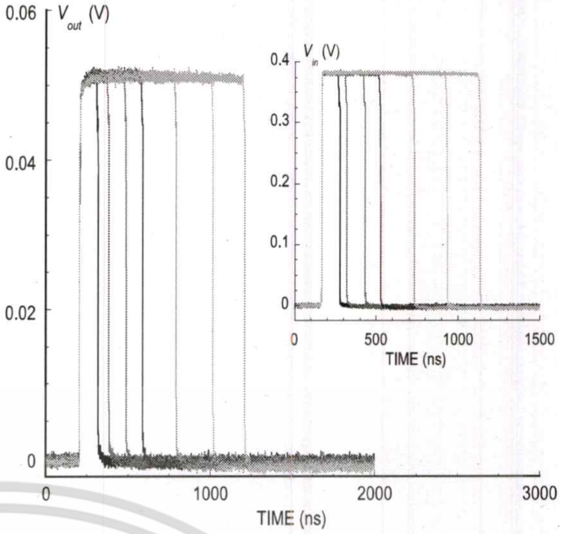

Figure 3. In the main panel we show output pulses obtained for Device D1 by varying pulse duration over the range $100\ \text{ns} \leqslant \tau \leqslant 1000\ \text{ns}$. The input voltage was held fixed at $V_{\text{in}} = 0.38$ V in these measurements, which were obtained using a PRF = 10 kHz. The inset shows the form of the corresponding input pulses applied to the device.

To explore the different processes described above, we begin in figure 3 by considering the transient behavior obtained when subjecting the device to repetitive pulsing with a relatively small input pulse ($V_{\text{in}} = 0.38$ V, corresponding to an electric field of 2.5 kV cm^{-1}; see the inset for the input pulses). The PRF here (and in figure 4) is just 10 kHz, an important point since, as we will shortly see, this minimizes any influence due to Joule heating of the substrate. Under these conditions, the peak voltage detected at the 50 Ω input of the sampling oscilloscope (V_{out} in figure 1(c), which directly is proportional to the current flowing through the device) remains independent of the pulse width, even when the duration is increased to as much as 1 μs. Essentially, this

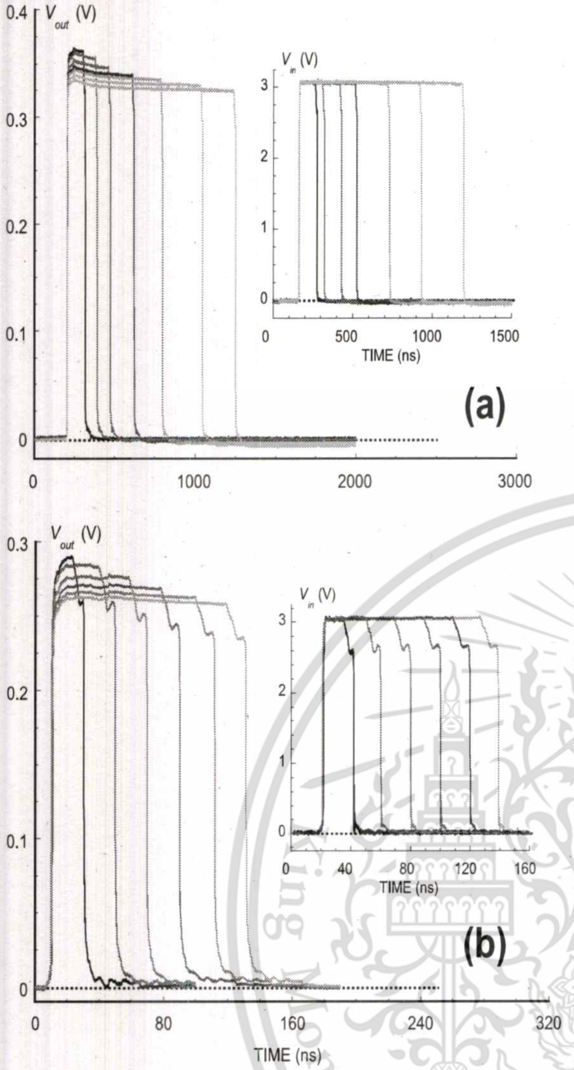

Figure 4. (a) The main panel shows similar measurements to those in figure 3, again for Device D1 but with V_{in} increased to 3.05 V (PRF = 10 kHz). The inset shows the input pulses applied to the device. (b) Corresponding measurements of Device D4 (PRF = 10 kHz), with the inset showing the form of the input pulses.

indicates that the transient current is influenced neither by Joule heating, nor by the influence of charge trapping. Although not shown here, this behavior is maintained for pulse amplitudes up to $V_{\text{in}} \sim 2$ V, corresponding to an (average) field strength of $\sim$13 kV cm^{-1}. For larger pulses, however, quite different behavior is observed, as indicated in figure 4(a) (see the inset for the form of the input pulses). Here, the average field in the channel has been increased to $\sim$20 kV cm^{-1} and we now observe a pronounced dependence of the transient current on pulse duration. More specifically, there are two features of this data that are worthy of further discussion. Firstly, as the pulse duration is increased to 1 μs, the maximum voltage that the output reaches at the end of its initial (rising) edge systematically decreases. (That is, the peak current flowing through the transistor similarly decreases.) At the same time, following the initial rise, each of the output pulses undergoes a slow decay, on a characteristic time scale that appears to be on the order of hundreds of nanoseconds. Both of these behaviors are in marked contrast to the results of figure 3.

The time dependent decay of the current shown in figure 4(a) points to a loss of channel carriers over time, in other words to the influence of trapping. To explain the various aspects of this figure, we must remember that what we actually measure in experiment is not the outcome of a single-shot pulse, but rather the time-dependent current determined from a process of repetitive sampling. Typically, this output pulse is constructed from an average of some 10^5 pulses, with the precise number depending upon the values of τ and the PRF. With this in mind, we propose the following scenario to account for the observations of figure 4(a). Beginning with the successive drop in overall current level that occurs as we increase the pulse duration, this is attributed to charging of the deep traps; with a large pulse applied to the device, the gate barrier will be lowered significantly, allowing these traps to very quickly capture carriers from the channel. As we increase the pulse duration, however, we simultaneously reduce the 'off' time between successive pulses, meaning that there is less time for captured carriers to return to the channel. Consequently, for longer pulse lengths, there will be fewer free carriers in the graphene channel, and it is this effect that should be responsible for the degradation of the maximum output current implied by figure 4(a).

The other aspect of figure 4(a) is a slow time-dependent decay of the output current, which is most clearly seen for the longer pulses. The onset of this decay is not instantaneous, but rather appears some 40 ns after the rising edge of the pulses. A similar effect can also be seen in figure 4(b), in which we show data obtained for a different device (input pulses are again shown in the inset and exhibit an instability on their falling edge; this is actually an artifact due to the pulse generator, but is nicely reproduced in the output curves). The average field in the channel (30 kV cm^{-1}) is somewhat higher here, and the current decay now onsets about 10 ns after the rise of the pulse. Presumably, the shorter time required for the onset of the decay reflects the increased ease with which carriers may be injected into deep traps in the oxide under higher fields. Nonetheless, the nature of the decay of the current is similar to that shown in the main panel, however, and we attribute it to the previously mentioned process in which application of the pulsed voltage leads to a new equilibration between the filling and emptying of the interfacial traps. From the data shown in the main panel, it would appear that this equilibration may take as long as microseconds.

Thus far, we have emphasized that the release of carriers from the deep traps, once the transient voltage has passed, should take place over very long times, due to the presence of a large blocking barrier. This can be demonstrated in experiment, using the approach adopted in figure 5. Here, we monitor the evolution of the device current as the pulse duration is first increased from 20 ns up to 1 μs (figures 5(a) and (b)), following which we steadily reduce it back to 20 ns again (various panels of figure 5(c)). In figure 5(a), it is clear

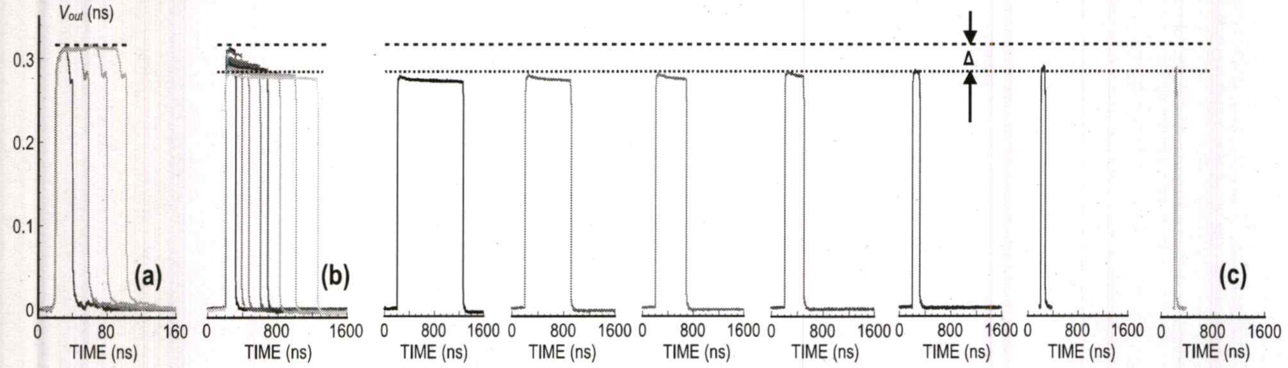

Figure 5 Hysteretic device operation in an experiment performed on Device D2 in which we monitor the evolution of the current (V_{out}) as the pulse duration is first increased from 20 ns up to 1 μs, while maintaining fixed $V_{\mathrm{in}} = 2.72$ V, following which we steadily reduce it back to 20 ns again. (a) As τ is increased from 20 to 80 ns, the output voltage remains fixed, as indicated by the dashed line. (b) τ is further increased up to 1 μs, with the dashed line representing the initial value of V_{out} obtained for the pulses in (a). In panel (c), we demonstrate in sequential order the output pulses measured while returning τ back to 20 ns. Again, the dashed line representing the initial value of V_{out} obtained for the pulses in (a). The dotted line shows the maximum output voltage reached on the return pulses, with Δ representing the difference between V_{out} for these pulses and for the initial ones in (a). Note that for all the measurements shown here, the time lapse between completing any given pulse and starting the next one was 10 s, while the time required to acquire each pulse was 2 s.

that there is no reduction in the output pulse level over the first 100 ns or so. Once again, we associate this delay with the time required for significant charge trapping to onset. Relative to the data of figure 4, the longer time required in figure 5(a) for this onset is likely due to the smaller amplitude of the applied pulse ($V_{\mathrm{in}} = 2.72$ V). For times longer than ~100 ns, the current shows a steady decrease (figure 5(b)). Both of these behaviors are actually reminiscent of those present in figure 4(a). By the time we return back to the 20 ns pulse, at the end of the experiment, it is clear that the amplitude of the output voltage is reduced considerably below its initial value (in panel (a)). Consistent with the discussion in the paragraph above, this 'hysteresis' basically demonstrates that the detrapping times associated with the deep traps must be considerably longer than the time interval between successive pulses. As a result, there is insufficient time during these periods to allow the trapped charges to all return back to the 2D channel, and it is this effective accumulation of trapped charges that causes a steady decrease in the channel current over time. After reaching the end of the experiment, we have found that it may take as long as 40 min for the current to return to its original value (i.e. for $\Delta \rightarrow 0$). It is this long-time retention of charge that is responsible for the observation of the widely-reported hysteretic characteristics [10–13, 20–24] found for graphene devices.

3.2. Joule heating of graphene devices

When graphene is subjected to an instantaneous excitation, such as that which can be supplied by an ultra-short laser pulse [25–29], its carriers undergo rapid thermalization, followed by a loss of their excess energy to the lattice, on time scales of tens to hundreds of femtoseconds, and picoseconds, respectively [31–35]. While the time-dependent dynamics of such processes is inaccessible in our transient studies, we are able to probe the thermal time constants associated with a slower process, namely that in which heat is conducted from the excited graphene channel to the underlying substrate. As noted already, a computational study of thermal transport in graphene-on-SiO_2 devices has shown how the transmission of heat from the 2D graphene channel to the underlying oxide should be slowed (significantly) by the large thermal mismatch between these materials [5]. Indeed, for a typical oxide thickness of ~300 nm, this mismatch is such that the time constant associated with the heating of this layer should be as long as 100 ns [5]. Even longer yet is the time required for heat to diffuse through the thick silicon substrate, on top of which the graphene-on-SiO_2 system is formed. Based on a standard substrate thickness of 0.5 mm, this time is expected to reach as much as a 100 μs [5].

One means by which the dynamics of substrate heating may be explored is by suitable control of the PRF. Typically, this is adjusted to be sufficiently low (10 kHz) that successive pulses may be viewed as truly independent of one another, with all thermal transients associated with any given pulse fully decaying before the next one is initiated. In figure 6, we illustrate the effect of increasing the PRF so that this condition is no longer satisfied. In both of these measurements, the PRF has been increased to 1 MHz, for which condition the triggering of successive pulses is separated by a time interval of 1 μs. An example of the form of the input pulses is provided in figure 6(a). In figure 6(b), we show output pulses obtained in response to an input of relatively small amplitude ($V_{\mathrm{in}} = 0.38$ V); successive pulses rise to the same output voltage, independent of the pulse duration. Very different behavior is seen in figure 6(c), however, which was obtained after increasing the amplitude of the pulsed voltage to $V_{\mathrm{in}} = 3.05$ V. For this larger input voltage, the peak current exhibited during each transient pulse increases as τ is increased. We attribute this latter behavior to Joule heating of the underlying substrate, which is exacerbated as both τ and the PRF are increased. As noted earlier, the combined effect of increasing these two parameters is to reduce the 'off' time between successive pulses, with this time becoming as small as 700 ns for the longest pulses used in the insets. This is

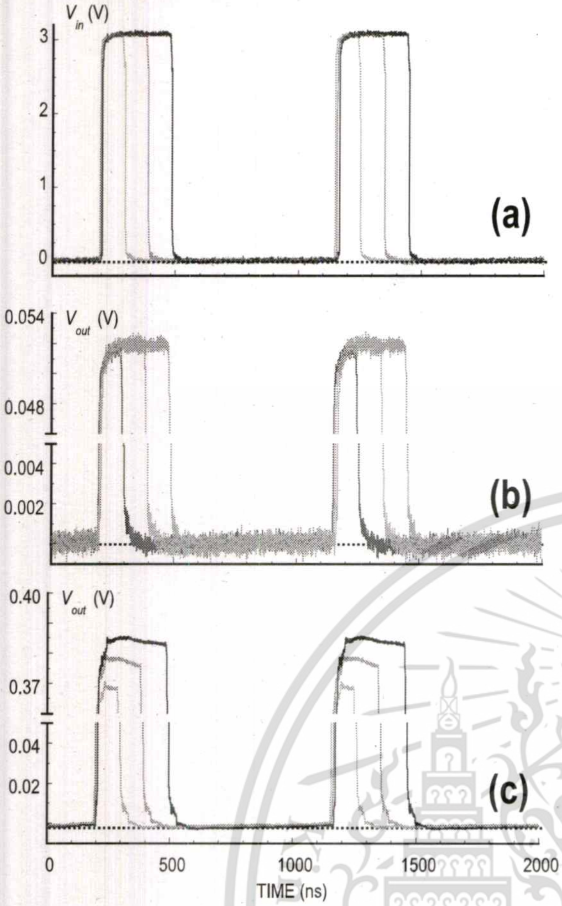

Figure 6. Influence of PRF on the transient measurements. The experiments were performed on Device D1 for a PRF of 1 MHz, and for two different input voltages ($V_{\text{in}} = 0.38$ and 3.05 V). (a) Form of the input pulses for $V_{\text{in}} = 3.05$ V (although not shown here, the input pulses were of similar form for $V_{\text{in}} = 0.38$ V. (b) Output pulses measured with $V_{\text{in}} = 0.38$ V. There is no significant dependence on the pulse duration. (c) Output pulses measured with $V_{\text{in}} = 3.05$ V. Here, there is a clear dependence of V_{out} on the pulse duration. Note the break in the vertical axis in panels (b) and (c).

comparable to the time constants associated with heating of the SiO_2 and Si layers of the substrate, implying that the device has insufficient time to cool completely between successive pulses. Longer pulses should instead lead to an increase in the steady-state temperature of the device, generating increased thermal carriers that give rise to the increased currents apparent in figure 6(c).

3.3. Interaction of charge trapping and joule heating

While we have thus far explored the influence of charge trapping and substrate heating separately, through appropriate manipulation of the pulse amplitude, duration and repetition frequency, for large enough V_{in} both effects may be present simultaneously. In such cases, however, we are often able to take advantage of the fact that these processes typically occur on very different time scales. An example of this is provided in figure 7(b), the data of which were obtained for a large input pulse of $V_{\text{in}} = 4$ V (corresponding to a peak electric field of 50 kV cm^{-1}, see figure 7(a) for the applied pulses). For pulse durations shorter than ~100 ns, it can be seen that V_{out} decreases systematically with increasing pulse duration, reminiscent of the trapping-related behavior discussed earlier in relation to figure 4. As in our discussion of that figure, we attribute this behavior to the filling of deep traps under the influence of strong pulsed biasing. Coexisting with this effect is a slower overall decay of the current that is most conveniently discussed by considering the behavior exhibited by the three longest pulses (i.e. those for which $150\text{ ns} \leqslant \tau \leqslant 450\text{ ns}$). These appear to collapse on top of one another, indicating that they decay with essentially the same time constant, the value of which should be of order 10^2 ns. Significantly shorter than the microsecond time scale that we have previously associated with interfacial-state filling (figure 4), we suggest that the decay in figure 7(b) most likely arises from Joule heating [5] of the underlying substrate. In the case considered here, the Joule heating results in a loss of heat from the graphene channel, which should therefore reduce the instantaneously generated thermal carrier concentrations. As the carrier concentration decays, the current should similarly decrease, as we observe in figure 7(b). This behavior is therefore distinct from that described in relation to

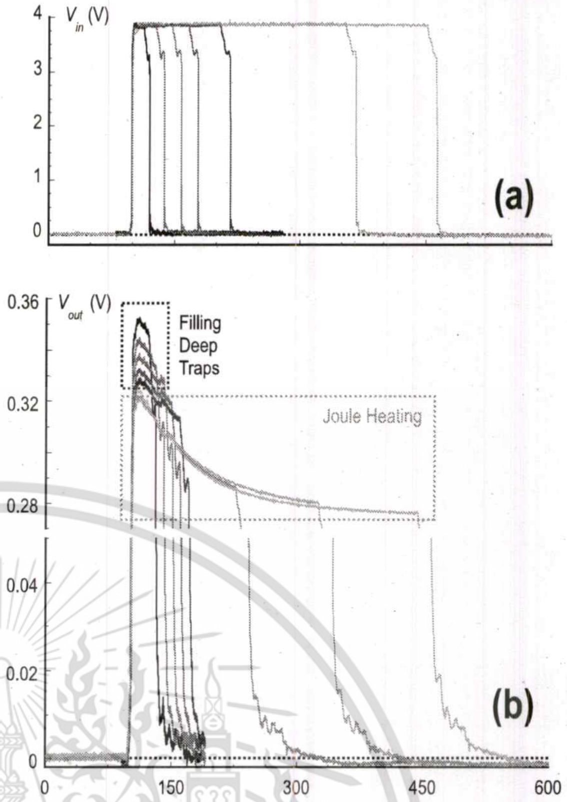

Figure 7. Measurement showing the influence of both the filling of deep traps and Joule heating, in an experiment performed on Device D4 using a large input pulse of $V_{\text{in}} = 4$ V. The PRF in this measurement was 10 kHz. (a) Some examples of the input pulses applied to the device. (b) Output pulses measured at the oscilloscope. The boxes enclosed by dotted lines identify current variations arising from filling deep traps and from Joule heating. Note the break in the vertical axis.

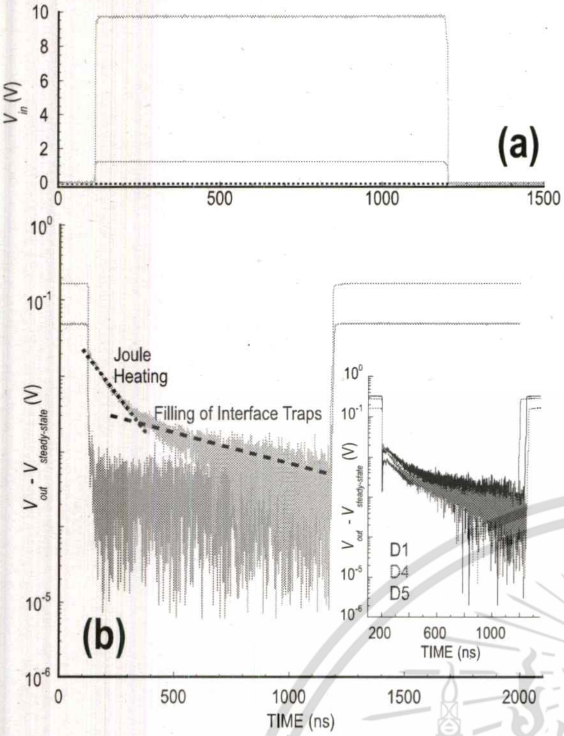

Figure 8. Additional measurements revealing the joint influence of deep traps and Joule heating. (a) Form of the applied voltage pulses. (b) Time dependent variation of the output voltage exhibited by Device D5 in response to the pulses of panel (a). Data show the variation of $V_{\mathrm{out}}(t) - V_{\mathrm{steady\text{-}state}}$, where $V_{\mathrm{steady\text{-}state}}$ is the steady-state output voltage reached at the end of the pulse, for an input voltage $V_{\mathrm{in}} = 1.2$ V (blue) and 9.5 V (green). The inset shows similar behavior for three different devices (D1, D4 and D5). The PRF in these measurements was 10 kHz.

figure 6, where the PRF was increased to cause thermal overburdening of the device. The overburdening reduces the overall efficiency with which the graphene channel is able to dissipate heat via the substrate, thereby *increasing* the concentration of thermal carriers in the graphene. In this case one obtains an *increase* of the transient current, behavior that is opposite to that shown in figure 7(b).

For a further example of the interplay of different transient processes, in figure 8 we compare the time dependent variation of the output voltage exhibited by Device D5 under conditions of both high- and low-field biasing. Figure 8(b) actually shows the time-dependent variation of $V_{\mathrm{out}}(t) - V_{\mathrm{steady\text{-}state}}$, where $V_{\mathrm{steady\text{-}state}}$ is the steady-state output voltage reached at the end of the pulse. The pulse duration has moreover been increased to the maximum possible value of 1.1 μs, and the low-field pulse exhibits no noticeable time dependence across this entire range, Very different behavior is seen in the high-field data, however, which appear to exhibit two different regimes of exponential decay, a rapid initial decay with a time constant of $\tau_1 \sim 125$ ns, followed by a much slower decrease with $\tau_2 \sim 600$ ns (the values of $\tau_{1,2}$ were determined simply by fitting the current decay to an exponential form, over the two appropriate time ranges). As we indicate in the inset to figure 8(b), we have studied these time constants in three different devices (D1, D4 and D5), both monolayer and bilayer, and find them to be very similar. Based on our discussions above, we attribute the initial decay with time constant τ_1 to the influence of heat dissipation though the substrate. The slower decay, with the much longer time constant τ_2, is then attributed to the release of trapped carriers from interface states. While an alternative interpretation, which cannot be ruled out completely, could be that the two time scales result from interface states with different characteristic energies, this would in turn imply that the measurements reveal no signature due to substrate heating. This would contradict the theoretical expectations of [5], which actually lead to time scales for substrate heating in accordance with our observed value for τ_1.

3.4. Observing intrinsic drift velocity saturation in graphene

As noted already in the introduction, the key factor that sets the upper limit on the ultimate drive current that can be carried by transistors is the value of the saturated drift velocity of their hot carriers. Associated with the spontaneous emission of optical phonons by hot carriers, the large energies of these phonons (160–200 meV) in graphene are expected to result in similarly large saturated velocities [36–39]. Experiments, on the other hand, have widely been found to yield significantly lower velocities than expected [1–8], an anomaly that is usually attributed to the interaction of graphene's hot carriers with the surface optical phonons of the $\mathrm{SiO_2}$ substrate. Since the energy of the latter (~55 meV) is very much lower than that of graphene's own optical phonons, drift velocity saturation may occur at much lower values than expected. This result may be understood quantitatively in terms of the (approximate) relation for the saturation velocity (v_{sat}) in graphene [1]:

$$v_{\mathrm{sat}} = \frac{2}{\pi}\frac{\omega_{\mathrm{OP}}}{\sqrt{\pi n}}. \tag{1}$$

Here, n is the 2D carrier density in the graphene channel and $\hbar\omega_{\mathrm{OP}}$ is the energy of the specific optical phonon responsible for velocity saturation. Using the surface optical phonon energy of 55 meV, as opposed to graphene's intrinsic phonon energies, equation (1) yields a saturated velocity of just 30% of its expected upper (intrinsic) value. This situation has been confirmed in a number of different experiments [1–8].

To avoid the influence of substrate-induced interactions, we have recently shown how it is possible to make use of extremely short-duration (nanosecond) electrical pulsing to observe the intrinsic mechanisms for velocity saturation in graphene [19]. In this approach, one essentially drives the graphene on time scales much faster than those on which substrate heating or trapping or can occur. An example of such rapid (4 ns) pulsing was presented already in figure 3. Typical current-voltage characteristics obtained by transient pulsing are indicated in the inset to figure 9. Away from the charge-neutrality point at $V_{\mathrm{g}} \sim +15$ V, these curves exhibit a common behavior; a linear increase at low fields that crosses over to a saturation at fields beyond ~40 kV cm^{-1}. Closer to the charge-neutrality point, however, the devices exhibit the

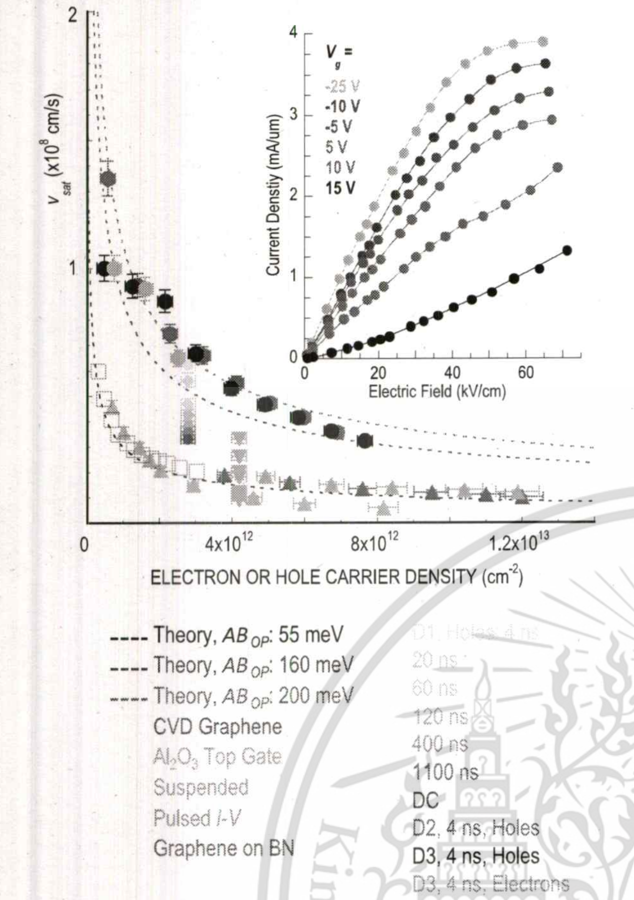

Figure 9. The main panel shows the variation of the saturated drift velocity with carrier density, inferred for the different devices. The different symbols are identified in the inset to the plot. Dashed lines correspond to the predictions of equation (1), using different characteristic phonon energies (also indicated). Filled triangles and open squares represent the results of prior experiments reported in the literature (see [19] for further details). The inset shows current-field characteristics determined for Device D3 by transient pulsing. A top-gate voltage close to +15 V corresponds to the charge-neutrality point so that these data are obtained for hole doping.

'kink' behavior reported previously [1], which arises from the influence of the pulsed voltage on the effective gate voltage within the channel; the kink indicates the onset of an inversion of the majority carrier type near the source of the device, whose effective doping becomes opposite to that near the drain.

By repeating the pulsed current-field measurements at different gate voltages that span from the electron to the hole spectrum, we are able to construct the pulsed current-voltage characteristic of the device and confirm the presence of velocity saturation [19]. In the main panel of figure 9, we show the density-dependent variation of v_{sat}, determined for both electrons and holes in three of our devices. The velocity data obtained by rapid pulsing clearly follow the variation expected from equation (1), assuming that graphene's intrinsic optical phonons ($\hbar\omega_{\mathrm{OP}} = 160$–$200\,\mathrm{meV}$) are the source of the velocity saturation. These results should be contrasted with the data (plotted as filled triangles and open squares) from prior (quasi-DC) experiments [1, 3, 4, 40, 41]. The latter clearly follow the variation expected for scattering from the lower-energy ($\hbar\omega_{\mathrm{OP}} = 55\,\mathrm{mV}$) surface optical phonons of $\mathrm{SiO_2}$. In fact, our values for v_{sat} even exceed those obtained for freely-suspended graphene [40] (inverted triangles), and for graphene isolated on a BN substrate [41] (open squares). Based on these observations we conclude that rapid pulsing of graphene can indeed be used to probe its intrinsic velocity saturation, free of the impact of Joule heating and charge trapping. This point is made clear by the data plotted as solid blue circles in the main panel of figure 5, which show the systematic degradation of v_{sat} as the pulse duration is increased.

4. Discussion and conclusions

In this article, we have made used of pulsed electrical studies to investigate the various processes that limit the current carrying capacity of (top-gated) graphene devices. When graphene is subjected to an instantaneous excitation, its carriers undergo rapid thermalization, followed by a loss of their excess energy to the lattice, on time scales of tens to hundreds of femtoseconds, and picoseconds, respectively [31–35]. In our experiments, we investigate the consequences of this excitation over a time scale that ranges from nanoseconds to hours (i.e. over twelve orders of magnitude), a dynamic range that allows us to investigate various phenomena due to charge trapping and to heat transfer from the graphene channel to its substrate. In this work, we have seen how a number of key parameters of the applied electrical pulse, namely its amplitude, duration, and repetition frequency, are important to determining the resulting transient performance. For pulses of sufficiently small amplitudes, corresponding to average channel fields of a few $\mathrm{kV\,cm^{-1}}$, the output characteristics were found to be independent of these parameters. By increasing these parameters, either independently or in combination with one another, the transient current was found to develop a significant time-dependent nature, associated with four different processes. (1) The fastest process was attributed to the filling of deep traps, which appears to be activated once the average channel field exceeds $\sim 10\,\mathrm{kV\,cm^{-1}}$, allowing for enhanced tunneling across the gate dielectric (figure 4). (2) Following this, a time constant with a characteristic value of 100–200 ns was observed and was attributed to a process of Joule heating, in which heat is transferred from the graphene channel to the underlying substrate (figure 6). As mentioned already, the value of this time constant was found to be consistent with predictions for such a mechanism [5]. (3) A slow decay of current on a characteristic time scale of around 1 μs (figures 4 and 8) was associated with a mechanism of interfacial-state equilibration, in which a dynamic competition between the population and depopulation of these states was responsible for the approach to a steady state subsequent to the application of a voltage pulse. (4) Finally, the slowest process was attributed to the release of captured charge from the deep traps, once the voltage pulse was removed. In this situation, a large potential barrier blocks the release of charge

Table 1. Identification of different current mechanisms and their associated time scales.

Mechanism	Time scale
Injection into deep traps	Depends on electric field strength; most likely varying from sub-ns scale—below the time resolution of our measurements—to tens of, or even a hundred, ns as the pulse amplitude is decreased
Joule heating of substrate	$\sim 10^2$ ns
Interface trap equilibration	~ 1 μs
Escape from deep traps	Minutes to hours

from the traps, resulting in the manifestation of hysteresis in the electrical characteristics over a time scale of hours (figure 5). (We note here that a similar idea has recently been discussed in the analysis of memory effects in MoS_2 FETs [17].) These different regimes are summarized in table 1.

A word of caution that must be emphasized at this point concerns the possibility of an interplay among some of the different mechanisms identified above. Most notably, as the environment is heated by the current flow through the graphene channel, the excess thermal energy may lead to detrapping of charge from the interfacial and deep traps [42]. While this possibility cannot be ruled out here, we believe nonetheless that the general picture that we have developed should be correct. Specifically, if dominant, such detrapping would be expected to lead to an increase in current over time, opposite to the behavior that we observe in our transient studies. Nonetheless, based on observations from the literature [42], it would appear that a more careful treatment of thermal detrapping should be considered in future studies.

By making use of a nanosecond-duration pulsing scheme, we have shown how it is possible to suppress the influence of both charge trapping and substrate heating. In this way, we were able to observe the intrinsic drift velocity behavior predicted by theory for graphene transistors. The expected dependence of the drift velocity on carrier density (equation (1)) was also reproduced nicely in our experiments (figure 9), which showed that the saturated drift velocity may approach the Fermi velocity of graphene ($\sim 10^8$ cm s^{-1}) when the Fermi level is driven sufficiently close to the Dirac point. We note here that this conclusion contradicts the results of a recent numerical study of velocity saturation, based upon an ensemble Monte Carlo approach [43]. In that work, the value of the saturated velocity was found to be largely independent of density, in marked contrast to the behavior shown in figure 9. We note, however, that Ferry did not consider the energy transfer processes in a realistic device structure, and so may have overestimated the effective carrier temperature in his calculations. This in turn would lead to an underestimate in the value of the drift velocity.

The various experimental results demonstrated here are not only of relevance for the device physics of graphene, but should also be important for studies of other 2D semiconductors, including atomically-thin transition-metal dichalocogenides, black phosphorous, silicene, and various topological insulators.

Acknowledgments

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SCIENTIFIC REPORTS

Negative Differential Conductance & Hot-Carrier Avalanching in Monolayer WS2 FETs

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The high field phenomena of inter-valley transfer and avalanching breakdown have long been exploited in devices based on conventional semiconductors. In this Article, we demonstrate the manifestation of these effects in atomically-thin WS_2 field-effect transistors. The negative differential conductance exhibits all of the features familiar from discussions of this phenomenon in bulk semiconductors, including hysteresis in the transistor characteristics and increased noise that is indicative of travelling high-field domains. It is also found to be sensitive to thermal annealing, a result that we attribute to the influence of strain on the energy separation of the different valleys involved in hot-electron transfer. This idea is supported by the results of ensemble Monte Carlo simulations, which highlight the sensitivity of the negative differential conductance to the equilibrium populations of the different valleys. At high drain currents (>10 μA/μm) avalanching breakdown is also observed, and is attributed to trap-assisted inverse Auger scattering. This mechanism is not normally relevant in conventional semiconductors, but is possible in WS_2 due to the narrow width of its energy bands. The various results presented here suggest that WS_2 exhibits strong potential for use in hot-electron devices, including compact high-frequency sources and photonic detectors.

The emergence, in recent years, of monolayer transition-metal dichalcogenides has opened up broad possibilities for the realization of functional electronic and optoelectronic devices[1,2] In contrast to graphene, many of these materials (including MoS_2, WS_2, and WSe_2) are semiconducting and exhibit a significant forbidden gap (>1 eV), making them well suited for use in various transistor schemes. This has driven a concerted effort to characterize the operational characteristics of such devices, with particular emphasis being placed on evaluating the efficiency (ON/OFF ratio) and sharpness (sub-threshold slope) of transistor switching, and on identifying the different scattering mechanisms that limit the channel mobility[1] Much less attention appears to have been paid, however, to a potentially exciting application of these materials, namely the idea of using them to realize active mm-wave/terahertz sources, which derive their functionality from the dynamic transfer of hot electrons between different regions of their band structure.

Transferred-electron effects have long been exploited in conventional semiconductors, with the most well-known example being provided by the Gunn effect[3,4] In this phenomenon, the scattering of hot electrons from a central, high-mobility, valley, to a nearby one with heavier effective mass, gives rise to negative differential conductance and to the formation of traveling high-field domains. The domains are injected from the cathode of

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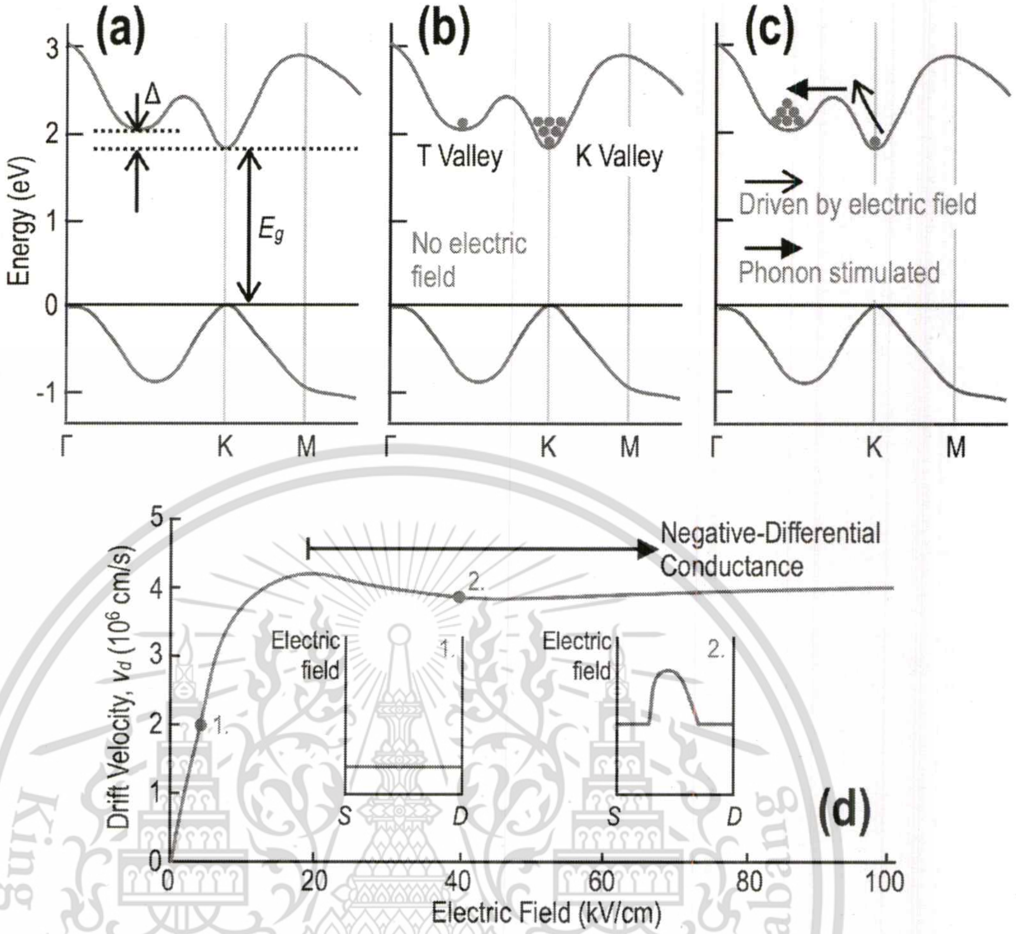

Figure 1. Bandstructure of WS2 and the mechanism for its negative differential conductance. (**a**) Band structure of monolayer WS_2. The T valley is located between the Γ and K points, and is separated from the K valley by an amount Δ. (**b**) Relative populations of the K and T valleys is indicated schematically for monolayer WS_2 at thermal equilibrium. (**c**) The populations of the K and T valleys change significantly under the application of an electric field. (**d**) Anticipated form of the velocity-field characteristic of monolayer WS_2, indicating a region of negative differential velocity/conductance. The insets are schematics that represent the electric-field distribution within the sample at very-different electric fields. 1. At low fields, the electric field is approximately constant throughout the conductor. 2. In the region where negative differential conductance occurs, a high-field domain is formed and travels repeatedly through the conductor.

the device and drift towards the anode, at which point they collapse, allowing a new domain to again be injected from the cathode. The periodic repetition of this process, on a time scale determined by the saturated drift velocity and by the anode-cathode separation, results in the emission of (microwave) radiation from the device, a phenomenon that has been exploited for some five decades in compact, inexpensive microwave sources[4]

The purpose of this Article is to demonstrate the possibility of exploiting the specific features of the band structure of transition-metal dichalcogenides, to realize novel transferred-electron effects. The material that we chose to focus on for this purpose is WS_2, which, when isolated in monolayer form, exhibits a band structure that suggests the strong potential for hot-electron transfer[5] This form of this structure is shown in Fig. 1(a), which reveals the presence of a direct gap ($E_g \sim 1.8\,\text{eV}$) at the K point (and, thus, at its equivalent K′ point[5]), and of a satellite valley that is located at the "T" point between the Γ and K points. The energy separation (Δ) of these two valleys is around 80 meV (dependent upon mechanical strain, see the discussion below), and the electron mass in the satellite valley ($m_T^* = 0.75m_o$, where m_o is the free-electron mass) is heavier than that near the K point ($m_K^* = 0.32m_o$). (In reciprocal space, the primitive Brillouin zone cell encloses six such T valleys, in addition to a single K and a single K′ point.) This bandstructure is therefore reminiscent of that found in GaAs, the prototypical "Gunn material", thus suggesting the possibility of achieving novel transferred-electron effects in WS_2. More specifically, in thermal equilibrium at room temperature, we expect most of the conduction-band carriers to populate the K (K′) valleys, with a much smaller number of electrons being present in the T valleys (Fig. 1(b)). By applying a sufficiently large electric field, however, it should be possible to drive carriers up the K valleys, allowing them to eventually scatter into the lower-mobility T valleys (Fig. 1(c)). This should give rise to a region of negative slope (Fig. 1(d)) in the

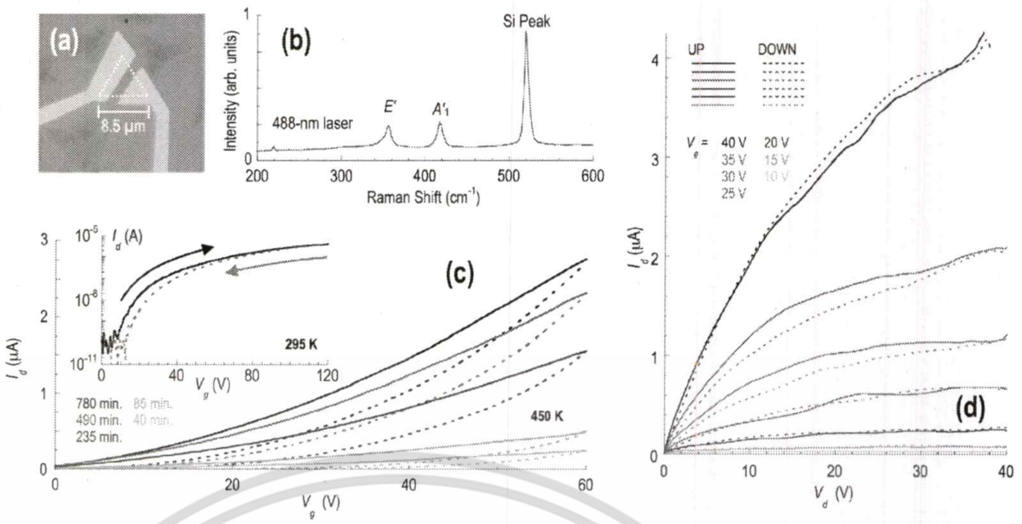

Figure 2. Raman spectroscopy and essential electrical characterization of the WS2 FETs. (**a**) Example of a monolayer WS_2 transistor (Device A). The outline of the WS_2 crystal is indicated by the white dotted line. (**b**) Raman spectrum of Device A, measured with 488-nm wavelength excitation. (**c**) The main panel plots transfer curves, measured for Device A at 450 K, after holding for that temperature for various times (indicated). The solid lines correspond to up sweeps of the gate voltage, while the dotted lines represent the corresponding down sweeps. The inset shows the transfer curve measured near room temperature, after completing the annealing process indicated in the main panel. Solid and dashed lines correspond to different sweep directions (indicated). (**d**) Transistor curves measured for Device A, after completing an annealing process similar to that indicated in Fig. 2(c). Solid and dashed lines correspond to different sweep directions (indicated).

velocity-fiel$_d$ (v_d-ε) characteristic, and lead in turn to negative differential conductance and to high-field domain formation (see the insets to Fig. 1(d)). In this Article, we present evidence of such behavior in monolayer WS_2, which we find exhibits clear signatures of negative differential conductance and of domain-induced current instabilities. Our experimental observations are confirmed by simulations of high-field transport, implemented via a Monte Carlo approach that includes all relevant scattering processes, both within the WS_2 and the (SiO_2) substrate. The calculations reveal how the relative populations of the two types of valley (K & T) evolve with electric field, and capture the characteristic features of the negative differential conductance observed in our experiments. We moreover demonstrate a novel form of high-field avalanching in these devices, which we attribute to a trap-assisted inverse-Auger process. Overall, our results represent a promising first step towards the realization of compact photonic sources based on two-dimensional (2D) transition-metal dichalcogenides. The high saturation velocity associated with this material (and with other transition-metal dichalcogenides[6, 7]) bodes well for the prospect of extending the operation of these sources to frequencies approaching the terahertz range (i.e. $\geq$10 GHz).

Results

WS_2 crystals (Fig. 2(a)) were grown on commercial Si/SiO_2 wafers by chemical vapor deposition (CVD) (for further details see refs 8 and 9). The monolayer character of these triangular-shaped single crystals was confirmed by Raman spectroscopy. An example is shown in Fig. 2(b), in which we plot the Raman spectrum of the device of Fig. 2(a) and find behavior consistent with previous reports for monolayer WS_2[10–12] The crystals were incorporated as the active channel of field-effect transistor (FET) structures, in which the variation of drain current (I_d) could be measured as a function of the drain (V_d) and gate (V_g) voltages. The gating was achieved by biasing a heavily-doped Si substrate, separated from the WS_2 crystals by a 300-nm thick SiO_2 dielectric layer. The fabricated devices were installed in a sample chamber with a base vacuum $\geq 10^{-6}$ mbar, and which allowed for control of temperature over the range of 300–500 K. Some twenty different transistors were fabricated for the purpose of this study, with channel lengths in the range of 1–2 µm (please refer to the Supplementary Information for more details on the most heavily-studied devices, including the nomenclature that we use here to identify them). The results included in this paper have been selected for representative purposes, being typical of the behavior exhibited by the different devices.

Negative Differential Conductance in Partially-Annealed WS2 Transistors.

Recent studies of the electrical characteristics of WS_2 FETs have focused on understanding the essential aspects of transistor operation[13–23], and on enhancing this functionality through targeted strategies for doping[24–28]. The drive currents supported by these transistors have also been found to be significantly enhanced by thermal annealing[19], which improves contact transparency and should also relax residual strain in the channel. In Fig. 2(c), we confirm the importance of thermal annealing by plotting various transfer curves, measured for Device A at an annealing temperature of 450 K. The annealing was performed while holding the sample chamber under vacuum, and the results of Fig. 2(c) were obtained by holding at that temperature for various times (indicated). Consistent with

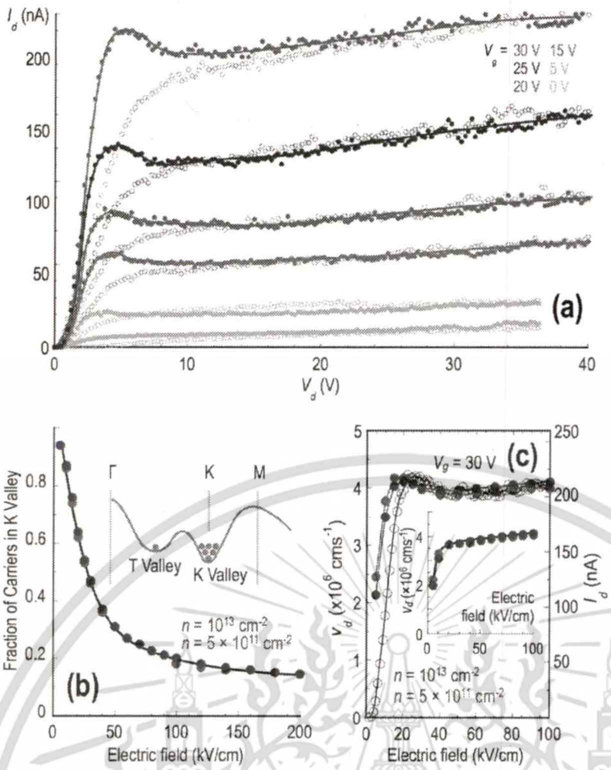

Figure 3. Negative differential conductance in the WS2 FETs. (**a**) Negative differential conductance in the room-temperature transistor curves (gate voltages indicated) of Device C. The filled and open symbols represent measurements taken while sweeping the drain voltage up and down from zero, respectively. The solid lines are guides to the eye that are drawn through the up sweeps to highlight the increased current noise that onsets on entering the region of negative differential conductance. (**b**) The main panel plots the carrier population in the K valley, at room temperature and at two different densities (indicated), as a function of electric field. The population decreases rapidly with increasing field, as the population of the T valley correspondingly increases. The inset indicates schematically the populations of the two valleys at thermal equilibrium. (**c**) In the main panel we compare the form of the calculated velocity-field curves, at two different densities (indicated) and for $\Delta = 110$ meV, with the I_d-V_d characteristic of Device C (the V_g = 30-V curve from Fig. 3(a)). Filled symbols correspond to the electron density, while the open symbols denotes the drain current. The inset shows the calculated velocity-field characteristics, for the same densities as considered in the main panel and for unstrained WS_2 with $\Delta = 80$ meV. Note the absence of any negative differential conductance in this case.

ref. 19, we observe a large increase in drive current when annealing over a time scale of many hours. Prior to the annealing, the current level remained in the range of 10^{-9}–10^{-8} A, over the entire range of gate voltage studied. With sustained annealing, however, the current could be increased to the μA level, representing a significant improvement in performance. During annealing, the transfer curves exhibit significant hysteresis, indicating that the channel current is degraded by the influence of charge trapping. As described previously in the literature (see, for example, the discussions in ref. 29), the traps responsible for this behavior are predominantly believed to be interfacial states, present at the boundary between the channel and the gate oxide, and deep traps within gate dielectric itself. In addition to providing a pathway for the loss of carriers from the channel, the traps may also function as localized scattering sites, suppressing the drive current of the FET[1, 2] In our experiments, the hysteresis in the transfer curves is significantly reduced at room temperature (see the inset to Fig. 2(c)), where the WS_2 transistors exhibit an ON/OFF ratio close to 10^5. In Fig. 2(d), we show transistor curves measured at room temperature, for another transistor (Device B) that has also been subjected to extended annealing. Consistent with the data of Fig. 2(c), we observe that the current level here rises to exceed 10 μA, at which point it approaches the saturation regime. Once again, there is a small amount of hysteresis as the drain voltage is cycled, consistent with the bias-induced excitation of carriers into/out of localized states. Importantly, however, the magnitude of this effect is small, a point that will be important to our subsequent discussions of the negative differential conductance effect.

It is quite clear that the transistor curves of Fig. 2(d) exhibit no evidence of negative differential conductance, in spite of the fact that the electric field in the channel reaches as much as 40 kV/cm. In Fig. 3(a), however, we show a very clear example of negative differential conductance that we have observed in these devices. While these data were obtained for Device C, under conditions that are described in the following paragraph, similar examples of negative differential conductance were obtained in all devices studied (see the Supplementary

Information for further examples). There are a number of aspects of the data in Fig. 3(a) that suggest that they are indeed associated with negative differential conductance arising from the influence of inter-valley transfer. The first feature that we note is the *clear region of negative differential conductance* itself, which is only observed when increasing the drain voltage, and which onsets at around $V_d = 5\,\mathrm{V}$ (corresponding to a channel field of 20–30 kV/cm). Crucially, the *onset of the negative differential conductance is accompanied by a marked increase in the noise level* in the drain current, a characteristic that commonly signals the formation of a traveling high-field domain in the channel[3, 4, 30] Finally, we note the *significant hysteresis in the drain current*, the value of which is significantly suppressed when returning from large drain voltage, compared to sweeping up. The nature of this hysteresis is very different to that exhibited by the fully-annealed devices (see Fig. 2(d)), being most pronounced over the very range of drain voltage for which the region of negative differential conductance emerges, and almost completely absent at larger V_d. This should be contrasted with the hysteresis seen in Fig. 2(d), which is less prominent in nature, persists over a wider voltage range, and shows no systematic variation with drain voltage. The hysteresis in Fig. 3(a) is instead consistent with transferred-electron phenomenology; as the voltage is lowered back from its maximal extent, a significant number of carriers may remain trapped in the lower-mobility valley (see the discussion that follows below), so that it is only by fully reducing the voltage to zero that the carriers may be returned to their original valley. Collectively, these three distinct observations provide strong evidence for a Gunn effect, arising from hot-electron transfer between the T- and K-valleys[3, 4]

While the evidence of negative differential conductance in Fig. 3(a) is convincing, an apparent contradiction arises from the fact that no such behavior is present whatsoever in Fig. 2(d). The critical difference between these results comes from the fact that the various curves of Fig. 2(d) were obtained after fully annealing the device, until no further significant increase in its current level could be achieved (a process that typically required as much as 12 hours, as suggested by the data of Fig. 2(c)). In this fully annealed state, transistor currents in the range of μA/μm could reliably be achieved for appropriate gate and drain biasing. The data exhibiting negative differential conductance (Fig. 3(a)), on the other hand, were obtained by subjecting the device to only modest annealing (anneal times of around an hour or less), resulting in smaller drain currents (~10 nA) for the same biasing conditions; this point may be appreciated by noting the lower current levels reached in Fig. 3(a) than in Fig. 2(d). In the discussion that follows, we propose a reconciliation of these very different behaviors, which considers the influence of mechanical strain on the band structure of WS_2, and the manner in which this affects the negative differential conductance.

In the normal (unstrained) crystalline state of monolayer WS_2, the energy separation between its T and K valleys is thought to be around 80 meV. With this relatively small difference, carriers are transferred to the T valleys at vanishingly-small fields and we consequently obtain no negative differential conductance. This point is demonstrated in the inset to Fig. 3(c), which shows the velocity-field characteristic calculated for unstrained monolayer WS_2. (The calculations are based on an ensemble Monte Carlo approach, in which scattering between the K and T valleys is generated by T-point LO phonons, see Supplementary Information for further details.) Data are plotted for two different densities, neither of which exhibit any evidence of negative differential velocity. In contrast, it has recently been shown that biaxial strain raises the energy of the T valleys relative to that the K valleys[31, 32] The resulting energy shift is relatively linear in the strain, and reduces the number of carriers in the T valley at thermal equilibrium. This in turn provides favorable conditions for the observation of negative differential conductance, by suppressing the likelihood of carriers being transferred into the T valleys at low fields[4] In our simulations, we have systematically raised the T valleys and find that negative differential conductance begins when the inter-valley separation (Δ) is as little as 100 meV (i.e. when it is increased by just 25% relative to the unstrained case), corresponding to a strain level of just 1%[31, 32] This estimate is consistent with recent scanning-microscopy studies of MoS_2 FETs, which have revealed the presence of unintended strain in their channels, introduced during nanofabrication[33] By assuming $\Delta = 110\,\mathrm{meV}$, in Fig. 3(b) we compute the fraction of the carriers that remain in the K valley as a function of the electric field. Near zero bias, virtually all of the carriers are in the K valley, with a much smaller fraction accessing the T valley (as indicated schematically in Fig. 1(b)). With increasing electric field, however, the population of the K valley decreases rapidly (Fig. 3(b)), as carriers are driven into the T valley (as in Fig. 1(c)). This results in the emergence of pronounced negative differential velocity, as shown in the main panel of Fig. 3(c). Here, we overlay the velocity-field characteristics, calculated for two different carrier densities and for $\Delta = 110\,\mathrm{meV}$, on top of one of the experimentally-measured transistor curves from Fig. 3(a). The data for both densities overlap well with the high-field portion of the experimental curve, consistent with the fact that appearance of negative differential conductance in Fig. 3(a) appears to be independent of the gate voltage. (Note that, since we do not know the carrier concentrations in the FET channel *per se*, it is not possible for us to infer a drift velocity from our transistor curves. Nonetheless, we note that the general shape of these curves is consistent with the expected variation of the drift velocity in Fig. 3(c) The negative differential conductance in the computed curves sets in beyond 20 kV/cm, again consistent with the experiment. While the peak-to-valley ratio of the negative differential conductance in Fig. 3(a) is considerably smaller than that found in GaAs[4], it nonetheless appears sufficient to lead to instability and to domain propagation, as indicated by the relatively large hysteresis, and by the accompanying current noise, in the transistor curves.

Avalanching Breakdown Under High Current Biasing. Negative differential conductance is just one example of a hot-carrier phenomenon that may be exhibited by semiconductor devices. Another well-known such effect is current breakdown due to avalanching, which can arise in the presence of large electric fields, once the drive current reaches an appropriate level. As noted already, the negative differential conductance discussed here was observed while the channel current in the FETs remained relatively low (<1 μA). By fully annealing the devices to optimize their current-carrying capacity, and utilizing both large drain and gate voltages, however, we are able to observe strong evidence of current avalanching. This phenomenon can be seen in Fig. 4, and occurs once the two bias voltages are increased such that the current rises to around 50–100 μA. (The avalanching is

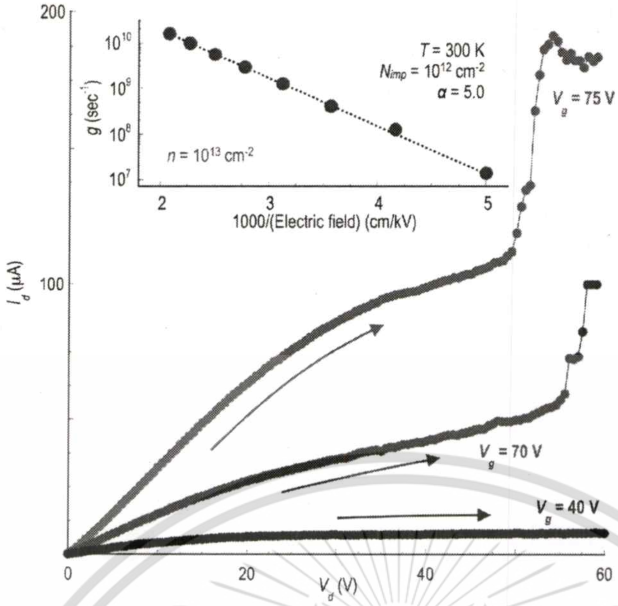

Figure 4. Avalanching breakdown in the WS2 FETs under strong electrical biasing. The main panel shows examples of current avalanching under high-current conditions. In these measurements, performed on Device A, a combination of thermal annealing and strong gate biasing is used to attain a large drain current (~10 μA), allowing the onset of avalanching. The inset to the figure plots the carrier generation rate (*g*) as a function of inverse electric field, calculated for Device A using the approach described in the Supplementary Information. The dotted line is a guide to the eye.

thus restricted to well-annealed devices, since these are the only ones capable of supporting the required current levels.) Focusing on the transistor curves obtained for $V_g = 70$ & 75 V in this figure, these do not exhibit current saturation but rather cross over to a slower increase as the drain bias is increased beyond the linear regime. With further increase of the bias, a sudden increase in the current is eventually observed, behavior that is indicative of avalanching. The capacity of the avalanching to destroy the device has meant that we have only been able to study its essential aspects, but it is clear already from Fig. 4 that it onsets at smaller drain bias as the gate voltage (and so the carrier density in the channel) is increased. A similar breakdown to that shown in Fig. 4 was also observed in other devices, for consistent values of the drain and gate voltages, once annealing had been used to maximize the current-carrying capacity of these transistors (see Supporting Information for additional examples).

We have studied the details of carrier generation in WS_2 using our ensemble Monte Carlo simulations, and find that the origin of the generation is very different to that in more-conventional semiconductors. The latter are characterized by relatively wide bands, which allow hot carriers to reach an energy several times that of the band gap. The impact ionization responsible for avalanching then occurs via a so-called "inverse Auger" process, in which a single hot electron interacts with a valence-band electron via the Coulomb interaction. (Another possibility, of course, is inter-band tunneling, but this is considered unlikely here since it generally produces a softer breakdown than the sharp current rise seen in our experiments. This is not altogether surprising, if we consider the long channel length of our devices, which is typically greater than 1 μm, and the large bandgap of monolayer WS_2; these factors should combine to suppress the role of inter-band tunneling.) Providing that the conduction-band electron has sufficient energy, it is then able to excite the valence electron into the conduction band, creating an additional electron and a hole[34] In the transition-metal dichalcogenides, however, the conduction band (as well as the valence band) is typically quite narrow, comparable to the size of the band gap itself[5] Consequently, hot electrons are unable to gain sufficient energy for the inverse Auger process. It is known, however, that transition-metal dichalcogenides typically have a large number of mid-gap traps, which arise from defects (such as chalcogenide vacancies[35, 36]) that can mediate electron-hole recombination. One possible mechanism that we hypothesize as the source of the breakdown is the inverse of this process, in which an energetic electron initially excites a valence electron into a mid-gap trap, following which it is excited into the conduction band through its interaction with a second hot electron. While the exact distribution of the mid-gap states involved in this second-order process is not known for these devices, the carrier ionization should ultimately be determined by an integration over all intermediate energies. For this reason we feel that the breakdown should not depend crucially upon the density of traps, although it would, of course, disappear if there were no such traps. The essential point is that this two-step process, which we refer to as trap-assisted inverse Auger scattering, has the same effect of creating a new electron-hole pair (see Fig. 5). Since two electrons are required to initiate the process, we assume that the ionization is second-order and construct a scattering process similar to that in normal 2D materials (see the Supplementary Information for further details). By associating the experimentally observed breakdown in Fig. 4 with the avalanching threshold, we are able to calculate the electron-hole pair generation rate (*g*) and its dependence on electric field. This dependence is plotted in the inset to Fig. 4, where we have

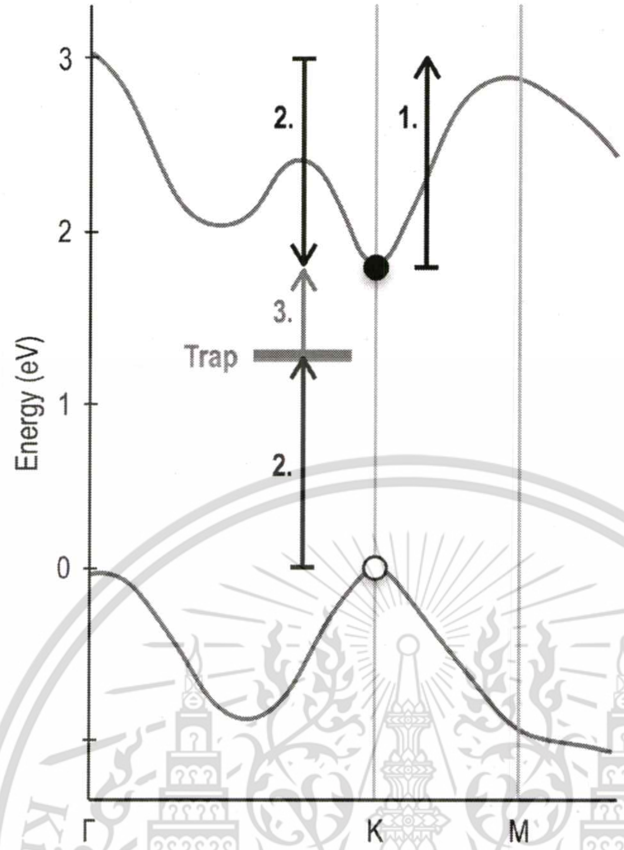

Figure 5. Schematic of the trap-assisted inverse Auger scattering process proposed for impact ionization. In Step 1, a carrier is driven up the conduction band by the strong electric field in the channel of the FET. In Step 2, the excited electron scatters from another electron in the valence band, losing its excess energy. This energy is transferred to the valence-band electron, which is excited into a mid-gap trap. Next, in Step 3, a second hot electron in the conduction band collides with the trapped electron, exciting it from the trap into the conduction band. At the end of this two-step process, the net result is the creation of an additional electron in the conduction band and a hole in the valence band (both indicated).

assumed an impurity concentration at the SiO_2 interface of $N_{imp} = 10^{12}\,\mathrm{cm}^{-2}$, and an equilibrium electron density of $10^{13}\,\mathrm{cm}^{-2}$. According to these calculations, the trap-assisted breakdown gives rise to a behavior in which the log of the generation rate varies linearly with the inverse electric field. This behavior corresponds to the "lucky" electron model suggested by Shockley[37, 38], and gives rise to the soft breakdown behavior that is apparent in the main panel of Fig. 4. According to the calculations in the inset, the exponential growth in the generation rate occurs in the field range of 200–500 kV/cm. This should be compared with the results of our experiment, which show that the breakdown occurs at a drain bias close to 50 V (when $V_g = 75\,\mathrm{V}$), corresponding to an average field in the channel of around 230 kV/cm. Since the device is operated in saturation when the breakdown occurs, however, the peak field near the drain will likely be much higher than this, further promoting the trap-assisted avalanching.

Discussion

In this Article, we have demonstrated important manifestations of hot-carrier transport in monolayer WS_2 FETs. Negative differential conductance was observed, and was found to exhibit characteristics typical of the Gunn effect in more-traditional semiconductors. Reminiscent of those materials, the negative differential conductance was accompanied by the observation of pronounced hysteresis in the transistor characteristics, behavior that is consistent with the excitation of hot carriers from the lighter-mass K valleys into the heavier-mass T valleys. Simultaneous with the emergence of the negative differential conductance, the noise level in the drain current was also found to increase, a feature that suggests the formation of travelling, high-field domains within the FET channel. Overall, observation of the negative differential conductance was found to be sensitive to thermal annealing, a result that we have explained within a scenario in which the annealing relaxes unintentional strain within the transition-metal dichalcogenide channel. By reducing the K-T valley separation (Δ), this suppresses the negative differential conductance, as larger numbers of carriers populate the T valleys at thermal equilibrium, and thereby mask the influence of any transferred carriers at high electric fields. By fully annealing the transistors, and by employing strong gate biasing, we were ultimately able to achieve drive currents in excess of 10 μA/μm, under which conditions an avalanching breakdown of the drain current was observed. Since the narrow (conduction- and valence-) band width in this material is unable to support avalanching via the usual inverse Auger process, we have proposed instead a mechanism based on a two-stage, trap-assisted inverse Auger scattering. The results presented here suggest the strong potential of WS_2 for use in various active devices. While further work still needs to be carried out, the instabilities associated with the negative differential conductance in this material may find application in compact microwave or terahertz sources, while the high-field breakdown may be useful in different photonic sensors.

Methods

WS_2 crystals were grown by CVD on commercial Si/SiO_2 wafers (as described in refs. 8 and 9), featuring pre-defined Cr/Au (5-nm/45-nm) markers that allowed alignment to individual WS_2 crystals to be performed in subsequent electron-beam lithography steps. Ambient Raman spectra of the crystals were obtained using a Renishaw inVia Raman Microscope, using a laser excitation of wavelength 488-nm and providing access to Raman shift in the range of 100–4000 cm^{-1}. Electrical measurements of the WS_2 FETs were performed after first wire bonding them into a ceramic DIP package, which was then mounted into the enclosed vacuum space of a variable-temperature system, capable of heating the devices to 500 K. This system allowed thermal annealing of the samples to be performed under the temperature conditions described in the main text, during which time the sample space was maintained at a vacuum of approximately 10^{-5} mbar. Transistor curves of the devices were recorded using a Keithley 2400 source-measure unit, with a second, similar, instrument being used to source the gate voltage. In measurements of the avalanching breakdown in these devices, a programmed compliance level was used to ensure that the drain current did not exceed 1 mA, thereby limiting irreversible damage to them.

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Author Contributions

J.P.B., M.T., R.V., and P.M.A. conceived and directed the experiments. G.H., J.N., C.-P.K., H.R., R.S., M.Z., N.P.-L., C. Z., A.L.E., Y.G., and X.Z. performed the experimental work. J.P.B., G.H., K.G., U.S., and D.K.F. analyzed the data. J.P.B., G.H., and D.K.F. wrote the manuscript.

Additional Information

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Competing Interests: The authors declare that they have no competing interests.

บันทึกรายการรับ-จ่ายเงิน โครงการวิจัย สัญญาเลขที่ ....2559-01-05-036......... ตั้งแต่วันที่ ......1 ต.ค. 2558..... ถึงวันที่ ....30 ก.ย. 2559.....

แหล่งทุน : แหล่งเงินรายได้

ชื่อโครงการ : ศึกษาการขนส่งพาหะร้อนในกราฟีนจากความนำไฟฟ้าเชิงอนุพันธ์

ชื่อหัวหน้าโครงการ : ดร. รัชนก สมพรเสน่ห์

ว/ด/ป	รายการ	เลขที่อ้างถึง	รายการรับ - จ่าย			รายรับ	รายจ่าย						รวม รายจ่าย
			รับ	จ่าย	คงเหลือ	ดอกเบี้ยรับ	งบบุคลากร	งบดำเนินงาน				งบลงทุน	
							ค่าจ้างชั่วคราว	ค่าตอบแทน	ค่าใช้สอย	ค่าวัสดุ	ค่าสาธารณูปโภค	ค่าครุภัณฑ์	
	งบประมาณที่ได้รับการอนุมัติ (ตามแผน)		50,000.00										-
26/1/16	จำนวนเงินที่ได้รับ (งวดที่ 1 = 85%)		42,500.00										
14/7/16	จำนวนเงินที่ได้รับ (งวดที่ 2 = 15%)		7,500.00										
	จำนวนเงินที่ได้รับ (งวดที่ 3)												
	หัก ค่าใช้จ่าย (ครั้งที่ 1)			42,500.00			-	-	18,500.00	34,500.00	-	-	53,000.00
	ค่าใช้จ่าย (ครั้งที่ 2)			7,500.00					-	-			
	งบประมาณคงเหลือ		50,000.00		-	0.00							
	รายละเอียดค่าใช้จ่าย												
ครั้งที่ 1													
15/2/16	ค่าจ้างวิเคราะห์ (I-V characteristics, Raman spectrum, AFM)	แบบ พ. 5							8,500.00				8,500.00
14/3/16	ค่าจ้างเหมาบริการ (ค่าจ้าง machine shop สำหรับ design cryostat parts)	แบบ พ. 5							10,000.00				10,000.00
21/3/16	10 MHz to 6 GHz SMA Bias Tee Rated To 2500 mA And 100 Volts DC Double Binding Post to 50 Ohm BNC Male Adapter	PSIN701010								13,400.00			13,400.00
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แหล่งทุน : แหล่งเงินรายได้

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ชื่อหัวหน้าโครงการ : ดร. รัชนก สมพรเสน่ห์

ว/ด/ป	รายการ	เลขที่อ้างถึง	รายการรับ - จ่าย			รายรับ	รายจ่าย						รวม
			รับ	จ่าย	คงเหลือ	ดอกเบี้ยรับ	งบบุคลากร	งบดำเนินงาน				งบลงทุน	รายจ่าย
25/3/16	Bias Tee 50 ohm Wideband 0.2 to 12000 MHz RoHS	590619								9,850.00			9,850.00
	รวมครั้งที่ 1		-	-	-	-	-	-	18,500.00	34,500.00	-	-	53,000.00

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4. Major Prize / Award / Honor

Year	Award	Institute
2015	Best Senior Poster Award of EDISON'19	Edison'19 Conference
2011	Best Poster Award	SEAS, The State University of New York, at Buffalo, USA
2011	Best Poster Award	EE Department, The State University of New York, at Buffalo, USA

5. Scholarships/Fellowships

Year	Scholarships/Fellowships	Institute
2016-2017	Grant for new researcher	Ministry of Science and Technology, Thailand
2016-2017	Grant for new researcher	King Mongkut's Institute of Technology Ladkrabang
2015-2017	Grant for new researcher	Thailand research funding
2015-2017	Grant for new researcher	King Mongkut's Institute of Technology Ladkrabang
2015-2016	Grant for new researcher	King Mongkut's Institute of Technology Ladkrabang
2007-2012	Scholarship for Ph.D. study	Ministry of Science and Technology, Thailand
2004-2005	Scholarship for Graduate study in Teaching profession	The Insitute for the Promotion of Teaching Science and Technology, Thailand
2000-2004	Scholarship for undergraduate study	The Insitute for the Promotion of Teaching Science and Technology, Thailand

6. Publications

1. H. Ramamoorthy, R. Somphonsane, J. Radice, G. He, J. Nathawat, C. P. Kwan, M. Zhao and J. P. Bird. *"Probing Charge Trapping and Joule Heating in Graphene Field-Effect Transistors by Transient Pulsing"* Semicon. Sci. Technol. 32, 084005 (2017)
2. R. Somphonsane, H. Ramamoorthy, G. He, J. Nathawat, C.-P. Kwan, Y.-H. Lee, J. Fransson, and J. P. Bird "Evaluating the Sources of Graphene's Resistivity Using Differential Conductance" Sci. Rep. 7, 10317 (2017)
3. G. He, J. Nathawat, C.-P. Kwan, H. Ramamoorthy, R. Somphonsane, M. Zhao, K. Ghosh, U. Singisetti, N. Perea-López, C. Zhou, A.L. Elías, M. Terrones, Y. Gong, X. Zhang, R. Vajtai, P. M. Ajayan, D. K. Ferry & J. P. Bird "*Negative Differential Conductance & Hot-Carrier Avalanching in Monolayer* WS_2 *FETs*" Sci. Rep. 7, 11256 (2017)
4. G. He, H. Ramamoorthy, C.-P. Kwan, Y.-H. Lee, J. Nathawat, R. Somphonsane, M. Matsunaga, A. Higuchi, N. Aoki, Y. Gong, X. Zhang, R. Vajtai, P. M. Ajayan, and J. P. Bird "*Thermally-Assisted Nonvolatile Memory in Monolayer* MoS_2 *Transistors*" Nano Lett. 16, 6445-6451 (2016)
5. H. Ramamoorthy, R. Somphonsane, J. Radice, G. He, C.-P. Kwan, and J. P. Bird "*"Freeing" Graphene from its Substrate: Observing Intrinsic Velocity Saturation with Rapid Electrical Pulsing*" Nano Lett. **16**, 399–403 (2016)
6. B. Liu, R. Akis, D. K. Ferry, G. Bohra, R. Somphonsone, H. Ramamoorthy, and J. P. Bird, "*Conductance fluctuations in graphene in the presence of long-range disorder*" J. Phys.: Condens. Matter **28**, 135302 (2016)

7. D. K. Ferry, R. Somphonsone, H. Ramamoorthy, and J. P. Bird, "*Energy relaxation of hot carriers in graphene via plasmon interactions*" J. Comput. Electron. **15**, 144-153 (2016)
8. D. K. Ferry, R. Somphonsone, H. Ramamoorthy, and J. P. Bird, "*Plasmon-mediated energy relaxation in graphene*" Appl. Phys. Lett. **107**, 262103 (2015)
9. G. He, K. Ghosh, U. Singisetti, H. Ramamoorthy, R. Somphonsane, G. Bohra, M. Matsunaga, A. Higuchi, N. Aoki, S. Najmaei, Y. Gong, X. Zhang, R. Vajtai, P. M. Ajayan, and J. P. Bird, "*Conduction Mechanisms in CVD-Grown Monolayer MoS_2 Transistors: From Variable-Range Hopping to Velocity Saturation*" Nano Lett. 15, 5052 (2015)
10. H. Ramamoorthy, R. Somphonsane, G. He, D. K. Ferry, Y. Ochiai, N. Aoki, and J. P. Bird, "*Reversing hot-carrier energy-relaxation in graphene with a magnetic field*", Appl. Phys. Lett. 104, 193115 (2014)
11. R. Somphonsane, H. Ramamoorthy, G. Bohra, G. He, D. K. Ferry, Y. Ochiai, N. Aoki, and J. P. Bird, "*Fast energy relaxation of hot carriers near the Dirac point of graphene*", Nano Lett. 13, 4305 (2013)
12. G. Bohra, R Somphonsane, N. Aoki , Y. Ochiai, R. Akis, D. K. Ferry, and J. P. Bird, "*Nonergodicity and microscopic symmetry breaking of the conductance fluctuations in disordered mesoscopic graphene*", Phys. Rev. B 86, 161405(R) (2012)
13. G. Bohra, R. Somphonsane, N. Aoki , Y. Ochiai, D. K. Ferry, and J. P. Bird, "*Robust mesoscopic fluctuations in disordered graphene*", Appl. Phys. Lett. 101, 093110 (2012)
14. J. Fransson, R. Somphonsane, H. Ramamoorthy, G. He, and J. P. Bird "*Voltage-induced suppression of weak localization in graphene*" *Phys. Rev. B* (2017, under revision)

7. Presentations

Oral Presentations

1. Gave a talk on "*Relaxation Dynamics of Hot Carriers in Graphene Revealed by Current-Induced Heating Measurements*" at NanoThailand 2014 (The 4th Thailand International Nanotechnology Conference), at Phatumthani, Thailand on Nov 26-28, 2014
2. Gave a talk on "Reversing Hot-Carrier Energy Relaxation with a Magnetic field" at IEEE NMDC 2014 (IEEE Nanotechnology Materials and Devices Conference) at Sicily, Italy on Oct 12-15, 2014
3. Gave a talk on on "Hot-Carrier Relaxation in Graphene and Its Dependence on a Magnetic Field" at GRPR 2014 (The 6th International Conference on Recent Progress in Graphene Research) at Taipei, Taiwan on Sep 21-25, 2014

Poster Presentations

1. R. Somphonsane, H. Ramamoorthy, G. He, J. Nathawat, C.-P. Kwan, N. Arabchigavkani, Y.-H. Lee, J. Fransson & J.P. Bird, "*Quenching weak localization in graphene by application of a nonequilibrium voltage*" at: 20th International Conference on Electron Dynamics in Semiconductors, Optoelectronics and Nanostructures (Edison' 20), Buffalo, NY, USA (2017)
2. R. Somphonsane, "*In-situ current annealing of graphene-metal contacts*" at NanoThailand 2016 (The 5th Thailand International Nanotechnology Conference), at Nakhon Ratchasima, Thailand on Nov 27-29, 2016
3. R. Somphonsane, H. Ramamoorthy, and J. P. Bird, "*Phonon-induced hot-carrier scattering in graphene: Insight from differential conductance*" at: 19th International Conference on Electron Dynamics in Semiconductors, Optoelectronics and Nanostructures (Edison' 19), Salamanca, Spain (2015)
4. H. Ramamoorthy, R. Somphonsane, G. He, D. K. Ferry, N. Aoki, Y. Ochiai and J. P. Bird, "*Hot-Carrier Relaxation in Graphene in a Magnetic Field*" at: 21st International Conference on "High Magnetic Fields in Semiconductor Physics"(HMF-21), Panama City Beach, Florida (2014)
5. R. Somphonsane, H. Ramamoorthy, D. K. Ferry, and J. P. Bird, "*Magnetic-field dependence of hot-carrier relaxation in graphene*", Poster presentation at: The International Symposium on Advanced Nanodevices and Nanotechnology (ISANN), Kauai, Hawaii (2013)
6. H. Ramamoorthy, R. Somphonsane, and J. P. Bird, "*Current-induced cleaning of graphene and graphene-metal contacts*" The International Symposium on Advanced Nanodevices and Nanotechnology (ISANN), Kauai, Hawaii (2013)
7. R. Somphonsane, H. Ramamoorthy, G. Bohra, G. He, D. K. Ferry, Y. Ochiai, N. Aoki, and J. P. Bird, "*Hot-carrier energy relaxation near the Dirac point of graphene*", International Workshop on Recent Progress in Nonequilibrium Quantum Many-Body Theory, Buffalo, NY (2013)
8. R. Somphonsane, H. Ramamoorthy, G. Bohra, G. He, D. K. Ferry, Y. Ochiai, N. Aoki, and J. P. Bird, "*Energy relaxation in mesoscopic graphene*", 3rd International Symposium on Terahertz Nanoscience (TeraNano III), Honolulu, Hawai (2012)