# COMMON-MODE FEEDBACK AND FEEDFORWARD TECHNIQUES FOR LOW-VOLTAGE CMOS OPERATIONAL TRANSCONDUCTANCE AMPLIFIER


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## บทคัดย่อ


วิทยานิพนธ์ฉบับนี้ นำเสนอเทคนิคการป้อนกลับโหมดร่วมและการป้อนไปหน้าสำหรับวงจรขยายซีมอสทรานส์คอนดักแตนซ์แบบโอเปอเรชันนัลที่ใช้แรงดันต่ำ วงจรขยายทรานส์คอนดักแตนซ์ที่นำเสนอเป็นแบบผลต่างเสมือนมีทั้งหมด 3 วงจร ซึ่งได้รับการออกแบบให้มีช่วงสวิงสัญญาณกว้างและสามารถทำงานภายใต้ไฟเลี้ยงต่ำ วงจรที่หนึ่งใช้วงจรป้อนกลับสัญญาณโหมดร่วมทำงานในโหมดกระแสที่มีช่วงสวิงกว้างซึ่งสามารถนำมาเชื่อมต่อกับวงจรขยายทรานส์คอนดักแตนซ์แรงดันต่ำได้อย่างอิสระโดยไม่ต้องมีการเปลี่ยนแปลงวงจรที่มีอยู่ วงจรป้อนกลับสัญญาณโหมดร่วมโหมดกระแสที่นำเสนอประกอบด้วย วงจรสะท้อนกระแสซึ่งทำหน้าที่เป็นวงจรตรวจจับสัญญาณโหมดร่วม และวงจรขยายกระแสเพื่อเพิ่มอัตราขยายของวงจร หลักการป้อนกลับแบบบวกถูกนำมาใช้เพื่อเพิ่มความต้านทานที่เอาต์พุตและเพิ่มอัตราขยาย วงจรที่นำเสนอถูกออกแบบโดยใช้เทคโนโลยีซีมอสขนาดเท่ากับ 0.18 ไมโครเมตร วงจรทำงานภายใต้แหล่งจ่ายไฟเลี้ยงเท่ากับ 1 โวลต์ การจำลองการทำงานวงจรที่นำเสนอด้วยโปรแกรม HSPICE โดยผลการจำลองการทำงานแสดงให้เห็นว่าวงจรมีช่วงสวิงเอาต์พุตกว้างเท่ากับ 0.7 โวลต์ มีอัตราขยายสัญญาณโหมดร่วมต่ำเท่ากับ -36 เดซิเบล และมีกำลังงานสูญเสียเท่ากับ 390 ไมโครวัตต์ วงจรที่นำเสนอวงจรที่สองเป็นวงจรขยายผลต่างเสมือนแบบคลาสเอบีโดยอาศัยวงจรซีมอสอินเวอร์เตอร์เป็นวงจรพื้นฐาน และวงจรป้อนกลับสัญญาณโหมดร่วมคอมพลีเมนทารีที่มีช่วงสวิงกว้างซึ่งประกอบด้วยวงจรตรวจจับสัญญาณโหมดร่วมแบบกระแส และวงจรทรานส์อิมพิแดนซ์ วงจรถูกออกแบบโดยใช้เทคโนโลยีซีมอสขนาด 0.18 ไมโครเมตร ภายใต้ไฟเลี้ยง 1 โวลต์ และผลการจำลองการทำงานเห็นได้ว่าวงจรมีเอาต์พุตสวิงกว้าง อัตราขยายสัญญาณโหมดร่วมมีค่าต่ำเท่ากับ -15 เดซิเบล แรงดันเอาต์พุตสวิงของวงจรมีค่าเท่ากับ 0.7 โวลต์ และมีกำลังงานสูญเสียเท่ากับ 102.5 ไมโครวัตต์ วงจรที่สามเป็นวงจรขยายผลต่างเสมือนแรงดันต่ำโดยใช้การป้อนสัญญาณอินพุตเข้าที่ขาบอดี้ของทรานซิสเตอร์เกตเลยเสมือน เพื่อให้วงจรสามารถมีช่วงสวิงอินพุตได้กว้างขณะเดียวกันก็สามารถทำงานได้ที่แรงดันต่ำเท่ากับ 0.5 โวลต์ เทคนิคการป้อนไปหน้าถูกนำมาใช้เพื่อลดอัตราขยายโหมดร่วมและวงจรป้อนกลับแบบบวกใช้เพื่อเพิ่มความต้านทานเอาต์พุตและอัตราขยายโหมดผลต่าง วงจรถูกจำลองการทำงานด้วยโปรแกรม CADENCE โดยใช้เทคโนโลยีซีมอสที่มีขนาดเท่ากับ 0.18 ไมโครเมตร ผลการจำลองการทำงานแสดงให้เห็นว่าอินพุตและเอาต์พุตมีช่วงสวิงกว้าง อัตราขยายโหมดผลต่างและอัตราขยายโหมดร่วมร่วมที่ได้มีค่าต่ำเท่ากับ 57 เดซิเบล และ -41 เดซิเบล ตามลำดับ และกำลังงานสูญเสียของวงจรมีค่าเท่ากับ 48 ไมโครวัตต์

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## ABSTRACT

This thesis presents the common-mode feedback (CMFB) and feedforward techniques for low-voltage CMOS operational transconductance amplifier (OTA). There are three different proposed low voltage rail-to-rail OTAs. The first circuit presents a current-mode CMFB circuit with rail-to-rail operation. The CMFB is a stand-alone circuit, which can be connected to any low voltage transconductor without changing or upsetting the existing circuit. The proposed CMFB employs current mirrors to operate as a common-mode detector and a current amplifier to enhance the loop gain of the CMFB. The circuit employs a positive feedback to enhance the output impedance and gain. The circuit has been designed by using a 0.18 μm CMOS technology (1V supply voltage) and analyzed by using HSPICE with BSIM3V3 device models. The simulation results shows a rail to rail output swing (±0.7 V) with a low common-mode (CM) gain (-36 dB) and a power dissipation of 390 μW. The second circuit presents a CMOS inverter-based class-AB OTA comprising current- mode CMFB. The circuit employs two CMOS inverters and a complementary CMFB consisting of a current-mode CM detector and a transimpedance amplifier. The circuit has been designed by using a 0.18 μm CMOS technology and operates at 1 V supply voltage. The simulation results demonstrate a rail-to-rail operation with low CM gain (-15 dB). The power dissipation of the circuit is 102.5 μW. The third circuit presents a low-voltage OTA. Bulk-driven quasi-floating gate (BD-QFG), feed-forward and positive-feedback techniques are employed in this amplifier. BD-QFG technique allows the circuit to operate at a supply voltage as low as 0.5 V, while feed-forward technique is used to suppress CM gain. Positive feedback is used to increase the output impedance and differential-mode (DM) gain. The circuit performance was verified by using CADENCE with process parameters of a standard 0.18 μm CMOS technology. The results demonstrated wide input and output signal swings. The DM and CM gains are 57 dB and -41 dB, respectively. The power dissipation is 48 μW.

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July 2017

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# CHAPTER 1
# INTRODUCTION

## 1.1 Background and Motivation

Nowadays, a high-performance analog circuit operating at low voltages becomes increasingly important due mainly to the advance of the large scale integration with complicated circuit systems and the demand for battery-operated portable equipment. However, supply voltage reduction in analog circuits causes several performance degradations such as degraded intrinsic gain, limited voltage swing and less dynamic range. As a result, new circuit techniques become mandatory to design analog circuits having sufficiently large gain with rail-to-rail capability.

The operational transconductance amplifier (OTA) is one of the most frequently used basic cells. OTA finds many applications in many analog circuits such as voltage comparators, analog-to-digital (ADC) and digital-to-analog (DAC) converters, and high frequency filters [1–16]. At present, differential OTAs are often used in industry products, since they provide improved dynamic range over their single-ended counterparts. In addition, they can reject common-mode noise, contain no even-order nonlinearities and increase output voltage swing. Several approaches have been proposed to design low voltage OTA using both fully differential (FD) and pseudo-differential (PD) configurations. FD is typically based on a differential pair with a tail current source, while PD is based on two independent inverters without tail current source. It is known that avoiding the voltage drop across the tail current source, in a PD structure, allows wider input and output ranges, making the architecture attractive for low power-supply applications. However, PD structure requires common-mode feedback (CMFB) circuit which serves two purposes: 1) to stabilize the common-mode voltage at high impedance nodes and 2) to suppress the common-mode signal components. In general, CMFB senses the common-mode (CM) output voltage, compares the result with a reference voltage and uses negative feedback to set the CM output voltage to the value that optimizes the output voltage swing.

In addition, OTA is required to operate with wide operating range under low supply voltage [17–19]. Basically, key important characteristics of OTA include high differential-mode (DM) gain, low common-mode (CM) gain, wide input and output voltage swings, large bandwidth, and low power consumption. All these conditions are the main goal of this thesis.

## 1.2 Purpose and Scope of the Study

According to the topology of a PD structure shown in Figure 1.1, $G_{miA}$ and $G_{miB}$ are two input transconductors and $Z_{outA}$ and $Z_{outB}$ are the equivalent output impedances of $G_{miA}$ and $G_{miB}$, respectively. Unlike FD structure, PD structure is based on two transconductors without tail current source, making the PD structure suitable for low voltage applications. However, removing the tail current source results in large common-mode gain ($A_{cm}$).

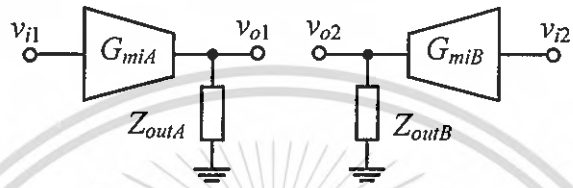



Figure 1.1 Basic structure of pseudo-differential amplifier (PDA)

In this thesis, two main designs based on pseudo differential amplifier are proposed which are 1) PDA using current-mode common-mode feedback (CMFB) and 2) PDA using feed-forward amplifier (FFA).

### 1.2.1 PDA using current-mode CMFB circuit

The conceptual implementation of the proposed pseudo-differential amplifier (PDA) with current-mode CMFB is illustrated in Figure 1.2. The proposed PDA consists of two input transconductors ($G_{miA}$ and $G_{miB}$) and a current-mode common-mode feedback (CMFB) network. In the design, the CMFB network comprises a common-mode amplifier (CMA) and two output transconductors ($G_{moA}$ and $G_{moB}$). In addition, the CMA consists of two matched resistors, two matched current mirrors, and transimpedance amplifier (TA). The detail of this current-mode CMFB is described in chapter 3.

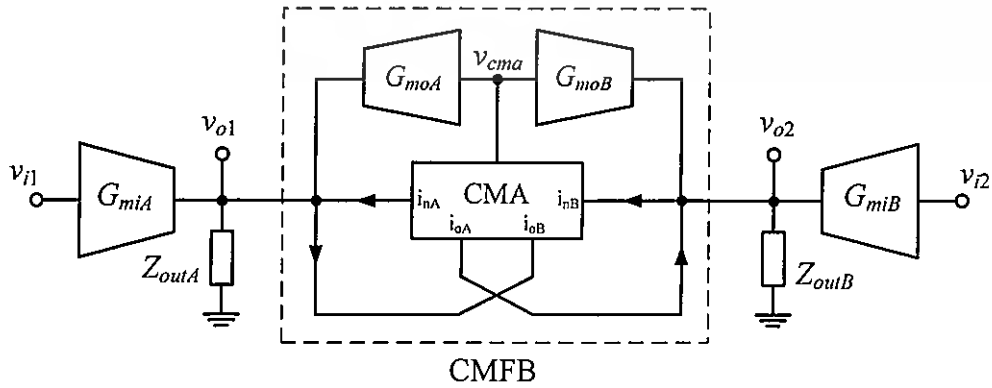



Figure 1.2 Structure of PDA using common-mode feedback (CMFB)

1.2.2 PDA using feed-forward amplifier (FFA)

Figure 1.3 illustrates the proposed structure of a feed-forward PDA. As can be seen, a feed-forward amplifier (FFA) has been added to the PDA. The FFA consists of two matched inverting amplifiers, that have a voltage gain of $-\alpha$, and two matched feed-forward transconductors ($G_{mffA}$ and $G_{mffB}$). The FFA serves two purposes: reduces the common-mode transconductance ($G_{cm}$) and raises the differential transconductance ($G_{dm}$).

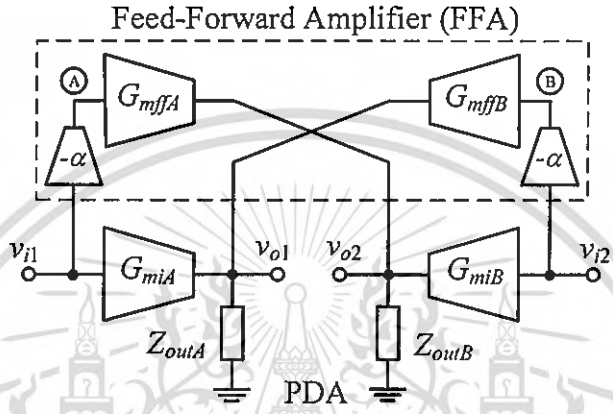



Figure 1.3 Structure of PDA using feed-forward amplifier (FFA)

Based on the two aforementioned concepts, three proposed low voltage rail-to-rail pseudo differential amplifiers (PDA) and their applications are presented in this thesis.

The first circuit is a class-A PDA using a current mode common-mode feedback (CMFB) circuit and its application to an oscillator. HSPICE and BSIM3V3 is used to simulate the proposed circuit using a 0.18 μm CMOS process to verify the circuit performance.

The second circuit is a CMOS inverter-based class-AB PDA with CMFB and its application to an active bandpass filter. The circuit has been designed and simulated using a standard 0.18 μm CMOS technology and the Cadence Spectre is used to prove the performance and robustness of the circuit.

The third circuit is a bulk-driven quasi floating gate (BD-QFG) PDA using feed-forward technique. Feed-forward path is used to suppress the common-mode gain and increase the differential mode gain. The circuit is suitable for low voltage application. Its application to multiple feedback filter (MFB) has been verified using Cadence Spectre and a standard 0.18 μm CMOS technology to evaluate the circuit performance.

## 1.3 Thesis outline

This thesis consists of five chapters presenting the theory, operation detail, design and simulation of pseudo differential amplifiers (PDAs) using common-mode feedback and feed forward technique. The organization of the thesis is outlined as follows:

Chapter 1 gives a motivation and historical perspective of the low voltage pseudo differential amplifier (PDA) and the purpose of the research. The framework and objective of conducting this research work are also included.

Chapter 2 reviews various techniques used in the design of low voltage analog circuit. The literature reviews on fully differential (FD) vs. pseudo differential (PD) amplifiers, common-mode circuits, and feed-forward techniques are also summarized.

Chapter 3 presents a design of pseudo differential amplifier (PDA) with common-mode feedback (CMFB) and its operation. Their performance analysis and simulation results of the proposed PDA are verified via HSPICE and Cadence Spectre.

Chapter 4 presents a design of a low voltage BD-QFG PDA. Its principle of operation and performance analysis is also included. Cadence Spectre is used to simulate the circuit and the simulation results and discussion is provided.

Finally, Chapter 5 contains a summary of the research presented and discusses the possible directions for future research of the PDA using common-mode feedback and feed-forward techniques.

Appendix A The differential mode and common-mode output impedance of the PDA

Appendix B The differential mode and common-mode transconductance of the PDA

Appendix C Frequency response of the PDA

Appendix D Noise analysis of the PDA

Appendix E Transfer function of bandpass-based oscillator

Appendix F Transfer function of MFB filter

Appendix G List of publications

# CHAPTER 2
# LOW VOLTAGE ANALOG CIRCUIT DESIGN TECHNIQUES: A LITERATURE REVIEW

## 2.1 Introduction

Large scale integration in large complex system and increasing demand for battery-operated portable equipment necessitate the use of high performance analog circuit that can operate at a lower supply voltage. Unfortunately, reduction of supply voltage especially in an analog circuit causes performance degradation such as degraded intrinsic gain, limited voltage swing and narrow dynamic range. As a result, new circuit techniques must be employed so that an analog circuit can operate under such stringent conditions, yet maintain good performance.

In the past, CMOS circuits operated at relatively high power supply levels. Analog designers were able to use the large voltage headroom which was given to develop circuit techniques in order to meet the increasing demand for high performance electronic applications. Increasing the speed and accuracy of CMOS circuits was the first priority, while power consumption can be compromised. Over the past several years, the CMOS design has changed and analog designers must contend with shrinking power supplies and the need to reduce the power consumption.

The reduction in power supply voltage and the need for less power hungry circuits come from two main reasons. The first is the increase in demand for system-on-chip (SoC) applications where an entire system is integrated on a single chip. While most of the signal processing in SoC applications will be handled by digital circuits, analog circuits will always be needed to interface with the real world [20]. The main push in developing new CMOS processes is to decrease the size of the devices so that the functional density of the digital chips increases. The decrease in device size has the added benefit of reducing capacitances and increasing the intrinsic speed of the transistors. However as MOS transistor size is scaled down, the thickness of the gate oxide is reduced. As a MOS transistor has a thinner gate oxide, in order to prevent the transistor from a breakdown due to higher electrical field across the gate oxide, and to ensure its reliability, the supply voltage needs to be reduced.

A second reason for the decrease in power supply voltage has been the increased demand for portable electronic devices as well as remote wireless sensors and implantable biomedical devices. Electronic equipment such as hearing aids, cell phones, and multimedia players all run off batteries and require low power

consumption in order to increase the time before the battery must be recharged [20]. Lower power consumption would also allow for smaller and lighter batteries, which make up a relatively large portion of the area and weight of portable devices. The easiest and often most effective way to decrease the power consumption in a circuit is to decrease the power supply voltage.

While reducing the power supply of submicron processes has improved the performance of digital circuits, it has caused difficulties for analog designers due to the reduction in available signal swing. This problem is magnified due to the fact that the threshold voltage ($V_{TH}$) of the transistors has been reduced at a slower rate than the power supply voltage. The $V_{TH}$ has been kept high in order to maintain a good on/off current ratio, as well as to reduce the static leakage current in digital circuits. A plot of the power supply voltage ($V_{DD}$) and threshold voltage ($V_{TH}$) of CMOS processes down to the 90 nm node is shown in Figure 2.1 [21]. The reduction in available signal swing has made it difficult for analog designers to meet design specifications such as dynamic range, gain, linearity, signal-to-noise ratio (SNR), etc. If standard analog design techniques from the past are used in the new low voltage processes, the dynamic range and SNR will degrade due to the decreased signal swing and relatively constant noise floor [22]. The gain of devices such as amplifiers will also decrease because cascode transistors can no longer be used due to the large voltage they require to keep their transistors in saturation. The reduced signal swing will also make it difficult to design rail-to- rail input circuits due to the large $V_{TH}$ which must be overcome. In order for analog designers to continue to meet ever increasing performance specifications, they must invent new low voltage design techniques to overcome all these obstacles [20–23].

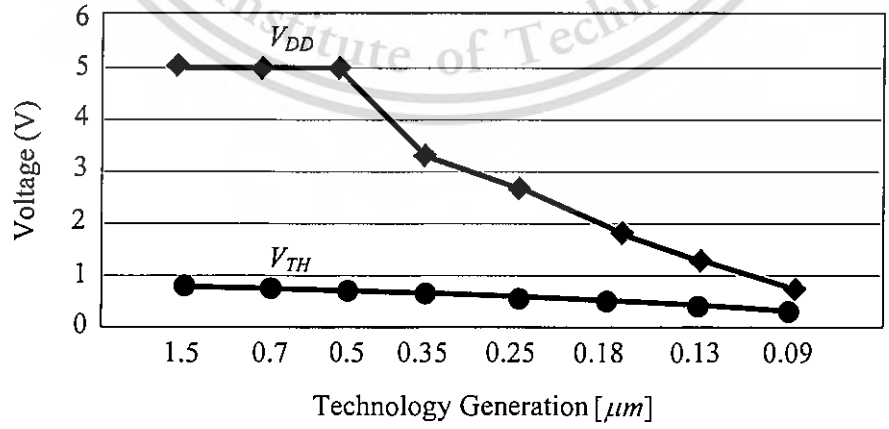



Figure 2.1 Supply voltage ($V_{DD}$) and threshold voltage ($V_{TH}$) vs. technology generation

Obviously, low–voltage (LV) low–power (LP) analog circuits have received significant attention and have become increasingly important in the electronic industry. Since the threshold voltages of standard CMOS technologies are not expected to be decreased much below what is available today, several design techniques exist for LV LP analog circuit design. However, only a few of them have found their way in modern designs, for instance, transistor operating in the sub threshold (weak inversion) region, level shifter techniques, self cascode structures, BD (Bulk-Driven) technique, Floating-Gate (FG) approach and Quasi-Floating-Gate (QFG) [20–48].

It is well known that the lower transconductance value of BD, FG and QFG leads not only to lower bandwidth but also to higher input referred noise in comparison to Gate-Driven (GD) transistor. Another issue is that the FG and QFG techniques cannot process DC signals, since their input terminals are capacitively connected to the floating gate and quasi floating gate, respectively. Also, due to the input capacitors the silicon area requirements of FG and QFG are increased. A new circuit technique has come up in order to combine the advantages and eliminate the disadvantages of the BD and QFG techniques. This interesting technique is Bulk-Driven Quasi-Floating-Gate (BD-QFG) [49–50] and they are created by combining the BD with either the QFG techniques.

## 2.2 Low Voltage Analog Design Techniques

### 2.2.1 Bulk-Driven MOSFET (BD-MOSFET) [21 – 34]

Bulk–driven MOSFET (BD-MOSFET) concept was first proposed by A. Guzinski et al in 1987 [34]. After that, BD technique has been adopted to implement a number of analog building blocks such as operational amplifiers, current mirrors, current conveyors, operational transconductance amplifiers, voltage followers, voltage to current converters, buffers, voltage–controlled oscillators, and phase–locked loops. The Bulk-Driven PMOS symbol and its cross–section are shown in Figure 2.2.

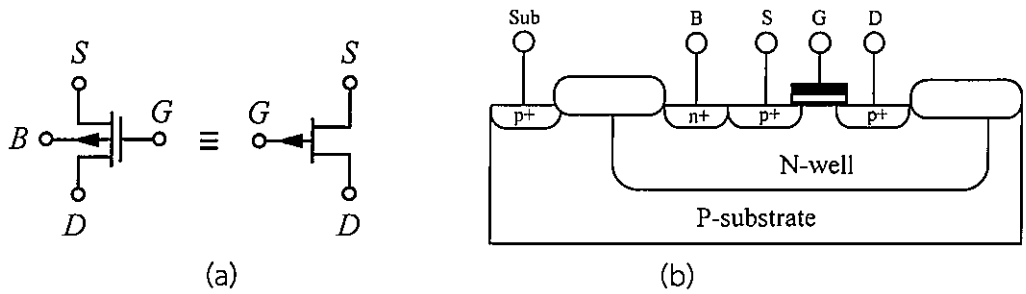



Figure 2.2 Bulk–driven PMOS: (a) symbol and (b) cross–section

Since the bulk contact serves the function of the gate of JFET and modulates the channel width according to the voltage applied to the bulk (see Figure 2.2(b)), BD-MOSFET is considered as a depletion type device. For *P*–channel (*N*–channel), BD-MOSFET can work in positive (negative), zero or slightly negative (positive) biasing condition.

In BD technique, a bias voltage is applied to the gate of the MOS Transistor so a channel is established between the source and the drain. This channel remains constant as long as the gate bias voltage is still the same, as the case for BD technique. On the other hand, the signal is applied to the bulk contact. By this way, the limitation of threshold voltage on the signal pathway is eliminated; consequently, the applicability of any analog cell to a very low supply voltage is possible to be extended.

The practical effect of forward biasing the bulk-source junction is to reduce the $V_{TH}$ of the transistor, which is given by

$$V_{TH} = V_{TO} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \tag{2.1}$$

where $V_{TH}$ is the threshold voltage, $V_{BS}$ is the bulk–source voltage, $V_{TO}$ is the threshold voltage at zero bulk–source voltage, $\gamma$ and $\phi_F$ are the bulk–threshold parameter and the surface potential, respectively.

In the Gate-Driven MOSFET, the signal is applied to the gate terminal. The threshold voltage requirement appears as an obstacle facing the input signal. BD-MOSFET is based on a different method, where the signal is applied to the bulk terminal after biasing the gate terminal to sufficient voltage, thus the threshold voltage in this set up is removed from the signal path. In other words, in a conventional GD-MOSFET, the current is acquired when the gate source voltage overcomes the threshold voltage, while in BD-MOSFET, gate source voltage remains constant and the input signal is applied at the bulk terminal.

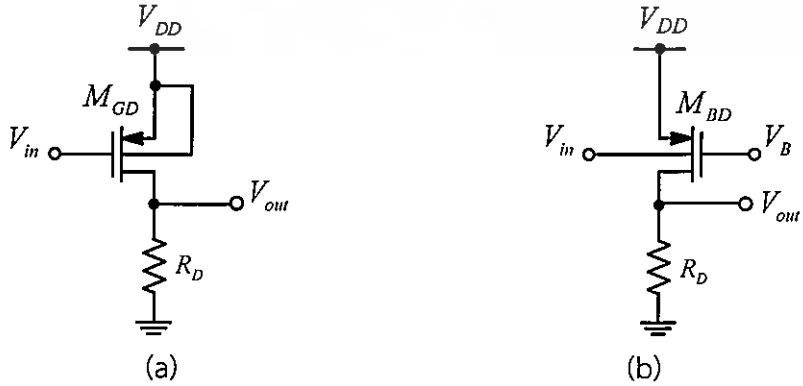



Figure 2.3 CS amplifier based on (a) BD-MOSFET and (b) GD-MOSFET

Figure 2.3 shows the common-source (CS) amplifier based on GD and BD-MOSFET where the input signal is applied to the gate and the bulk of transistor $M_{GD}$ and $M_{BD}$, respectively.

To study the small signal equivalent circuit of BD-MOSFET in comparison with the small signal equivalent circuit of gate–driven MOSFET (GD-MOSFET), BD and GD common–source (CS) amplifiers are shown in Figure 2.4 (a) and (b), and the small signal equivalent circuits at high frequencies of the CS amplifiers are shown in Figure 2.5 (a) and (b).

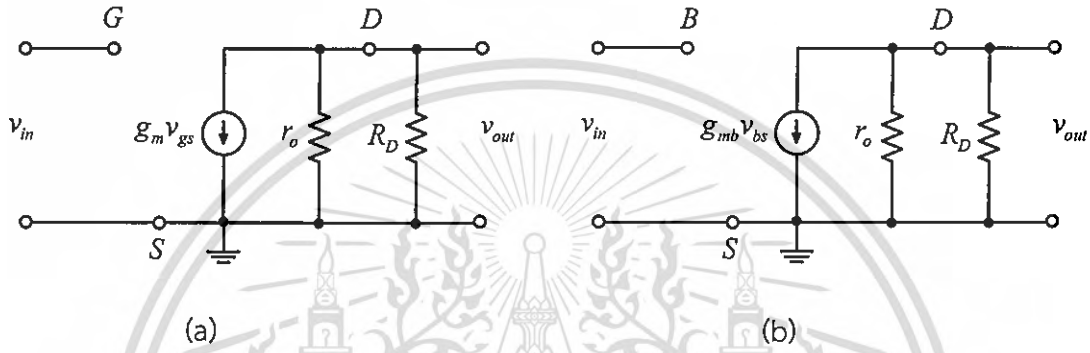



Figure 2.4 Small signal equivalent circuits of the CS amplifier based on: a) GD-MOSFET and b) BD-MOSFET

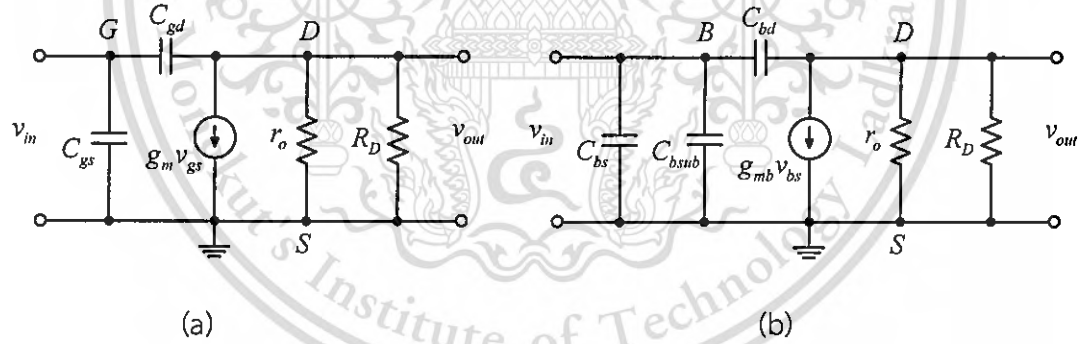



Figure 2.5 Small signal equivalent circuit at high frequencies of the CS amplifier based on: a) GD-MOSFET and b) BD-MOSFET

The transconductance ($g_m$) of GD-MOSFET which operates in strong inversion is given by

$$g_m = k\frac{W}{L}(V_{GS} - V_T) \tag{2.2}$$

where $k$ is the current gain factor of the used process. However, the bulk transconductance of MOSFET is given by

$$g_{mb} = \frac{C_{bc}}{C_{gc}} g_m = \frac{\gamma}{2\sqrt{|2\phi_F - V_{BS}|}} g_m = \eta g_m \approx (0.2 \to 0.4) g_m \quad (2.3)$$

where $C_{bc}$, $C_{gc}$ and $\eta$ are the total bulk channel capacitance, the total gate channel capacitance and the specific parameter, respectively.

The total bulk channel capacitance $C_{bc}$ of the MOSFET is given by

$$C_{bc} = WLC_j \quad (2.4)$$

where $C_j$ is the zero bias junction capacitance

The total gate channel capacitance $C_{gc}$ of the MOSFET is given by

$$C_{gc} = WLC_{ox} \quad (2.5)$$

where $C_{ox}$ is the oxide capacitance per unit area

The $f_T$ (transition frequency) is defined as the frequency where the magnitude of the short circuit, common source current gain falls to unity. However, the $f_T$ for GD and BD-MOSFET is respectively given by

$$f_{T,GD} = \frac{g_m}{2\pi C_{gs}} \quad (2.6)$$

where $C_{gs}$ is the gate source capacitance, and

$$f_{T,BD} = \frac{g_{mb}}{2\pi (C_{bs} + C_{bsub} + C_{bd})} \quad (2.7)$$

where $C_{bs}$ is the bulk-source capacitance, $C_{bd}$ is the bulk-drain capacitance, and $C_{bsub}$ is the bulk-substrate parasitic capacitance, respectively.

From (2.6) and (2.7) the relation between both unity gain frequencies is given by

$$f_{T,BD} = \frac{g_{mb}}{g_m} \frac{C_{gs}}{C_{bs} + C_{bsub} + C_{bd}} f_{T.GD} = \eta \frac{C_{gs}}{C_{bs} + C_{bsub} + C_{bd}} f_{T.GD} \approx (0.3 \to 0.5) f_{T.GD} \quad (2.8)$$

From (2.8) it is obvious that the transition frequency of BD-MOSFET is smaller than the transition frequency of GD-MOSFET, since the transition frequency is proportional to the transconductance, as well as the effect of the parasitic capacitances.

The input referred noise power spectral density of GD-MOSFET is expressed by

$$v_{noise,GD}^2 = \frac{i_{ni}^2}{g_m^2} \tag{2.9}$$

where $i_{ni}^2$ is the total drain current generated by noise sources and its unit is $A^2$. The input referred noise power spectral density of BD-MOSFET can be expressed by:

$$v_{noise,BD}^2 = \left(\frac{g_m}{g_{mb}}\right)^2 v_{noise,GD}^2 \tag{2.10}$$

From (2.10) it is obvious that the BD-MOSFET suffer from the higher value of input referred noise, since $g_{mb}$ is inherently smaller than $g_m$.

The output resistance $r_o$ for GD-MOSFET and BD-MOSFET are identical and given by

$$r_o = \frac{1}{g_o} = \frac{1}{\lambda I_{DSAT}} \tag{2.11}$$

where $\lambda$ is the channel length modulation coefficient and $I_{DSAT}$ is the drain source current in saturation.

Advantages

- As mentioned, bulk–driven PMOS works in positive, zero or slightly negative bias voltage also. This can lead to larger input common mode voltage range and voltage swing.
- Depletion characteristics avoid $V_{TH}$ requirement in the signal path. Voltage swing for low voltage supply is increased, and minimum operational supply voltage is pushed to its limit.
- This technique offers a possibility of using the conventional gate to modulate the BD-MOSFET since the transfer characteristic changes greatly with different $V_{GS}$, because $I_D$ is more sensitive to $V_{GS}$ than to $V_{BS}$.
- Better linearity and smaller power supply requirements because of the small value of the bulk transconductance ($g_{mb}$) of the MOSFET.
- Suitable for rail–to–rail applications.
- Can be modeled using the conventional MOS transistor.

Disadvantages

- The transconductance of the bulk ($g_{mb}$) is typically 20–40% of the transconductance of a conventional gate–driven ($g_m$) based on long–channel theory. This as shown in equations limits both the intrinsic gain and the cut–off frequency of the device, and increases the equivalent input noise voltage.

- The polarity of the BD-MOSFETs is process related; only BD-NMOSs are available for P-well process, and on the other hand, only BD-PMOSs are available for N-well process. This limits the applicability of this technique since we cannot use BD-MOSFET transistors in some circuit structures which require both NMOS and PMOS.

- Bulk terminals of all BD-MOSFETs usually have to be isolated, so it is necessary for each BD-MOSFETs to reside within its own separate well for many applications. Accordingly, the BD-MOSFET consumes more area than its GD counterpart does and further suffers from a degraded frequency response due to the added input capacitance from its well structure. More than that, the matching between BD-MOSFETs in differential wells suffers. Thus analog circuits with tight matching between MOSFETs are difficult to fabricate.

- When $V_{BS}$ is critically large (more than the turn–on voltage of the bulk–channel PN junction diode), latch–up incurs.

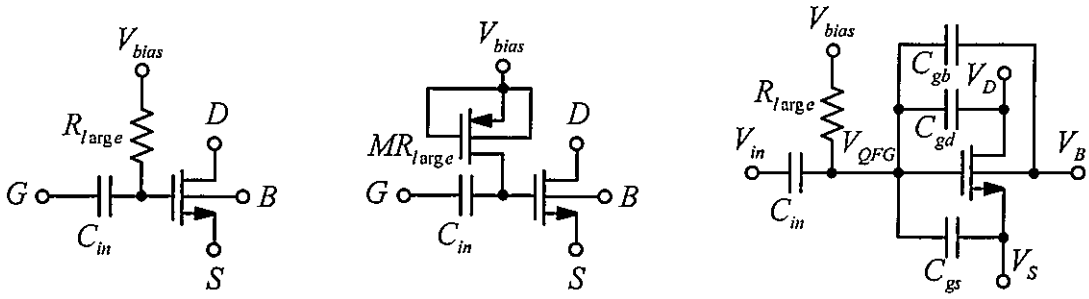
### 2.2.2 Quasi Floating Gate MOSFET (QFG-MOSFET) [35 – 48]

The quasi-floating-gate MOS (QFG-MOSFET) transistor is a device that operates in a very similar way to the FG-MOSFET, but it allows biasing the floating gate at a specific dc voltage while maintaining all the ac properties of the FG-MOSFET. Unlike the FG-MOSFET device, the QFG-MOSFET does not have issues with trapped charge, simulation or new technologies.

Several low voltage circuit applications have been designed utilizing the QFG-MOSFET, such as the differential OTA, current mirror, transconductors, current conveyors, filters, and linear MOS resistors.

The symbol of single input terminal QFG-MOSFET shown in Figure 2.6 (a). The input terminals are capacitively coupled to the quasi-floating-gate, but the DC gate voltage is set to $V_{bias}$ without requiring a large capacitor.

The floating gate of the QFG-MOSFET is weakly connected to a proper bias voltage using a large value resistor $R_{large}$, which is usually implemented by a large resistance of a reverse biased junction of a diode connected MOS transistor ($MR_{large}$) operating in the cutoff region as shown in Figure 2.6 (b). The equivalent circuit of Figure 2.6 (b) is shown in Figure 2.6 (c).




(a) (b) (c)

Figure 2.6 Single input QFG-MOSFET a) symbolic with $R_{large}$, b) symbolic with $MR_{large}$, c) equivalent circuit of (b)

Similarly to FG-MOSFET, the QFG-MOSFET can also be fabricated in all CMOS technologies, nevertheless, the double poly technology is recommended to acquire better results.

The input terminal ($V_{in}$) is capacitively coupled to the QFG just like in the FG-MOSFET case, but the DC gate voltage is set to $V_{bias}$ independently of the DC level of the input voltage. A simple analysis reveals that the AC voltage at the QFG is given by

$$V_{QFG} = \frac{sR_{large}}{1+sR_{large}C_{total}}\left(C_{in}V_{in} + C_{gd}V_D + C_{gs}V_S + C_{gb}V_B\right) \tag{2.12}$$

where $C_{total}$ is the total capacitance, and is given by

$$C_{total} = C_{in} + C_{gd} + C_{gs} + C_{gb} + C_R \tag{2.13}$$

As can be observed from (2.12), the input is a high pass filter with cut-off frequency:

$$f_c = \frac{1}{2\pi R_{large}C_{total}} \tag{2.14}$$

The value of the cut-off frequency is very low, in the range of sub-hertz, as long as $R_{large}$ remains large enough (in the order of Giga-Ohms); in order not to influence the circuit operation at the lowest required frequency [45, 49]. However, this equation confirms the incapability of QFG to process DC signals.

Note from (2.12) that inputs are high–pass filtered with a cutoff frequency $1/2\pi R_{large}C_{total}$, which can be made very low. Note also that the exact value of $R_{large}$ or its temperature and voltage dependence are unimportant, provided that

$R_{large}$ remains large enough not to influence the circuit operation at the lowest frequency required. The exact value of $C_{total}$ is also unimportant.

Due to a large value of $R_{large}$, even at low frequencies, (2.12) can be simplified as follows:

$$V_{QFG} = \frac{1}{C_{total}}\left(C_{in}V_{in} + C_{gd}V_D + C_{gs}V_S + C_{gb}V_B\right) \tag{2.15}$$

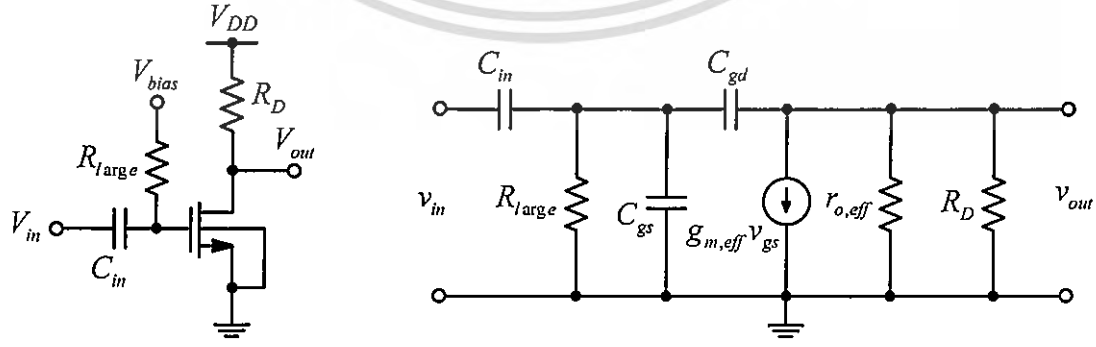
Note from (2.15) that the voltage at the floating gate becomes a weighted averaging of the AC input voltages determined by capacitance ratios when the parasitical capacitance is negligible.

For NMOS (PMOS), the pull–up (pull–down) resistor $R_{large}$ sets the gate to a DC voltage equal to the positive (negative) rail, to which an AC voltage given by (2.12) is superimposed. Hence, the gate voltage can become more (less) than $V_{bias}$. This does not pose a problem as long as the amplitude of the signals is (approximately) limited to 0.5 V in order to avoid forward biasing of the junction implementing $R_{large}$, so that it never becomes forward–biased. For larger signal amplitudes, utilization of two reverse–biased junctions in series can increase the maximum signal amplitude.

The relation between the effective transconductance ($g_{m,eff}$) of the QFG-MOSFET and the transconductance ($g_m$) of GD-MOSFET is given by:

$$g_{m,eff} = \frac{C_{in}}{C_{total}} g_m \approx (0.5 - 0.6) g_m \tag{2.16}$$

However, the $g_{m,eff}$ of QFG-MOSFET is larger than the $g_{m,eff}$ of floating gate transistor, but still smaller than the transconductance of conventional GD-MOSFET.




(a) (b)

Figure 2.7 Quasi floating gate MOSFET: (a) common source amplifier with single input terminal, (b) small signal model equivalent of (a).

Figure 2.7 shows the common source amplifier based on QFG-MOSFET in (a) and its small signal equivalent circuit in (b), where the previous capacitors are shown, however the floating gate–bulk capacitance is ignored, because it has no influence on signal path. The operation principle of the QFG-MOSFET is similar to the FG-MOSFET.

The effective output conductance of QFG -MOSFET is greater than the output conductance of GD-MOSFET, and it is given by

$$g_{o,eff} = \frac{C_{gd}}{C_{total}} g_m + g_o \tag{2.17}$$

The effective transconductance of QFG-MOSFET is larger than the effective transconductance of FG–MOSFET but, it is still smaller than the transconductance of conventional GD-MOSFET. It is given by

$$g_{m,eff} = \frac{C_{in}}{C_{total}} g_m \tag{2.18}$$

The transition frequency ($f_T$) of QFG can be expressed as

$$f_{T,QFG} = \frac{g_{m,eff}}{2\pi(C_{gd} + C_{gs})} \approx (0.5 \rightarrow 0.6) f_T \tag{2.19}$$

The relationship between the input referred noise power spectral density of QFG-MOSFET and GD-MOSFET is given by

$$v^2_{noise,QFG} = \left(\frac{C_{total}}{C_{in}}\right)^2 v^2_{noise,GD} \tag{2.20}$$

It is obvious from this equation that the relation between QFG-MOSFET and GD-MOSFET in term of (input referred noise power spectral density) is the similar to FG-MOSFET and GD-MOSFET since the input signal path in both MOSFETs is the same. However, QFG-MOSFET suffers from higher input referred noise than GD-MOSFET but still smaller than FG-MOSFET since $C_{total,QFG} < C_{total,FG}$.

Advantages

- No initial charge trapped at the floating gate.
- Does not need a programming technique as FG-MOSFET does.
- Consumes smaller occupied chip area than FG-MOSFET does.

- Higher effective transconductance and transition frequency than the FG-MOSFET.

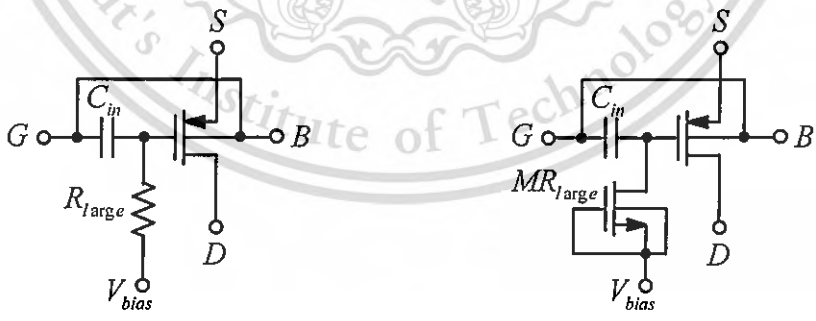
Disadvantages

- Larger effective output conductance than the effective output conductance of FG-MOSFET and the output conductance of GD-MOSFET.
- Floating gate voltage must not exceed the cut-in voltage of the p-n junction of the diode connected transistor $MR_{large}$.
- High-pass filters the applied signal.

### 2.2.3 Bulk-Driven Quasi-Floating-Gate MOSFET (BD-QFG-MOSFET) [49-50]

The bulk-driven (BD) and quasi-floating-gate (QFG) techniques are quite suitable for ultra LV LP applications mainly battery-powered implantable and wearable medical devices. Although they offer design simplicity and good performance, they still suffer from several drawbacks. The QFG MOS transistors have lower transconductances and transient frequency values than the conventional gate-driven (GD) MOS Transistor. Regarding the BD technique, it has much lower transconductance and transient frequency values than the conventional GD-MOSFET.

Therefore, novel techniques BD-QFG MOSFET were introduced by Khateb, these techniques appear as attractive approaches to overcome the above mentioned drawbacks of the BD, and QFG techniques. To illustrate the principle of the BD-QFG MOSFET using N-well technology, Figure 2.8 shows its symbol and the realization in MOS technology.




(a) (b)

Figure 2.8 BD-QFG MOSFET: (a) symbol and (b) realization in MOS technology

As shown in Figure 2.8 (a), the input-gate ($G$) is also connected to the bulk-terminal (B) of the QFG MOSFET and the bias-gate ($V_{bias}$) is connected to a suitable bias voltage through a large resistor ($R_{large}$) which is practically realized by MOSFET operating in the cutoff region ($MR_{large}$) as shown in Figure 2.8 (b). The input terminal ($G$) is capacitively coupled via $C_{in}$ to the QFG terminal from one side and

directly coupled to the bulk terminal from other side. As a result the total transistor transconductance ($g_{m,BD\text{-}QFG}$) is increased.

Assuming that the source (S) terminals of BD-QFG-MOSFETs at Figure 2.8 is grounded then their small-signal model is presented in Figure 2.9.

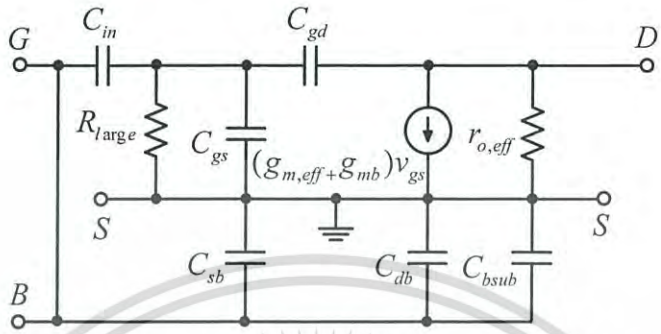



Figure 2.9 Small signal model for BD-QFG MOSFET

The output conductance of BD–QFG MOSFET is given by

$$g_{o,eff} \approx \frac{C_{gd}}{C_{total}} g_m + g_o \tag{2.21}$$

The transconductance of BD–QFG MOSFET is expressed by

$$g_{m,BD-QFG} = g_{mb} + g_{m,QFG} \tag{2.22}$$

Accordingly, the transition frequency of BD–QFG MOSFET is also increased

$$f_{T,BD-QFG} = \frac{g_{m,BD-QFG}}{2\pi(C_{bs} + C_{bsub} + C_{gs})} \tag{2.23}$$

where $g_{m,QFG}$ is the effective transconductance of the BD-QFG MOSFET.

From (2.22) and (2.23), it is clear that the BD–QFG MOSFETs offer better parameters than the BD, and QFG MOSFETs. Both transconductance and transition frequency are increased. However, the parasitic capacitance between the bulk and substrate terminal ($C_{bsub}$) degrades the transition frequency of the BD–QFG MOSFETs.

It is worth mentioning here that the total capacitance seen from the floating-gate MOSFET is higher than the one seen from quasi–floating–gate, because the value of $C_{bias}$ in FG is usually larger than gate–drain parasitic capacitance of the $MR_{large}$ in QFG. This results in the transconductance of the QFG MOSFET being larger

than FG-MOSFET, also the transconductance of the BD-QFG MOSFET is larger than QFG-MOSFET.

Advantages

- Higher transconductance ($g_m$) and transition frequency ($f_T$) than BD, QFG techniques.
- Can process DC and AC signals.
- Low supply voltage requirements and power consumption.
- Threshold voltage requirement is completely removed from the signal path.
- Rail-to-rail voltage swing capability.

Disadvantages

- Lower transconductance, transient frequency and output impedance than GD-MOSFET.
- When $V_{BS}$ is critically large (more than the turn-on voltage of the bulk-channel PN junction diode), latch-up incurs.
- BD-QFG MOSFET consumes larger silicon area compared with the MOS transistor due to the added input capacitors.
- In BD-QFG, the FG voltage must not exceed the cut-in voltage of the p-n junction of the diode connected transistor $MR_{large}$.

## 2.3 Pseudo Differential Amplifier (PDA) and Common-Mode Control Methods

In analog and mixed signal processing, fully-differential (FD) structures are often used due to their better dynamic range (larger signal swing, better distortion performance, and better common-mode rejection) over single-ended (SE) structures. For applications of low power supply voltages and large signal swings, pseudo-differential (PD) structures become attractive since they avoid the voltage drop across the tail current source. But PD structures have the same low frequency transconductance for both differential and common-mode signals. Therefore, the use of PD structures requires a careful and efficient control over the common-mode behavior of the circuits.

In this section, discusses and literature reviews of the pseudo differential amplifier (PDA) and the CM control methods which includes: 1) common-mode feedback (CMFB) and 2) common-mode feedforward (CMFF).

### 2.3.1 Pseudo Differential Amplifier (PDA) Structure [51 – 53]

The topology of a generic fully-differential transconductor is presented in Figure 2.10 (a). On the two branches of transconductor are represented the two active devices, having the transconductance $G_m$. The two input signals $v_{i1}$ and $v_{i2}$ can be expressed as

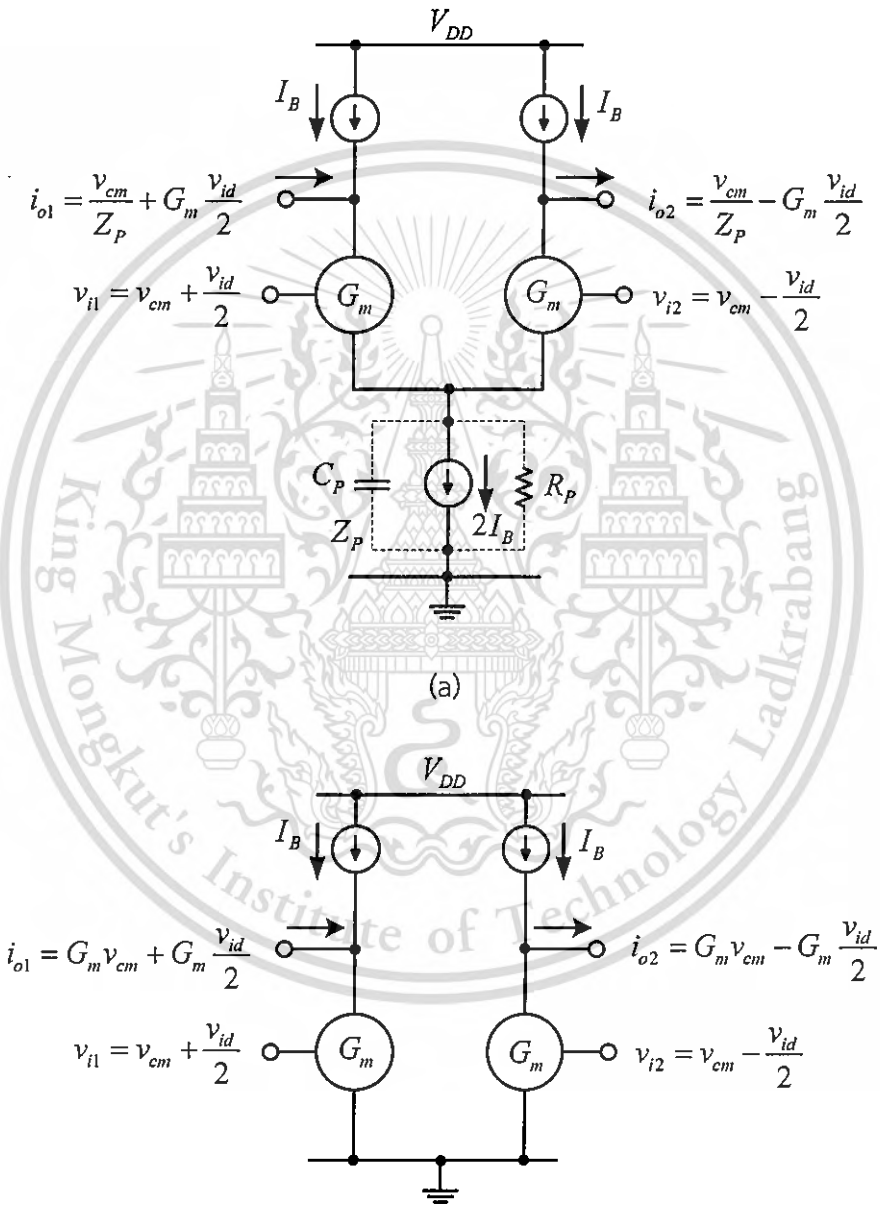



Figure 2.10 (a) Fully differential amplifier (FDA) (b) Pseudo differential amplifier (PDA)

$$v_{i1} = v_{icm} + \frac{v_{id}}{2} \tag{2.24}$$

$$v_{i2} = v_{icm} - \frac{v_{id}}{2} \tag{2.25}$$

where $v_{icm}$ is the input common-mode signal, and $v_{id}$ is the input differential-mode signal. In the fully-differential configuration, the rejection of the common-mode signal is achieved by the large output impedance $Z_P$ ($Z_P=R_P||C_P$) of the tail current source, especially at relatively low frequencies.

Pseudo differential (PD) structure is used at low supply voltages because PD structure avoids the voltage drop across the tail current source as shown in Figure 2.10 (b) [51-53]. It achieves large signal swing by avoiding the voltage drop across tail current source, but it needs efficient common-mode control circuitry to reject common-mode signal.

In the design of pseudo differential transconductor, one of the important characteristics is linearity. The PD transconductor shown in Figure 2.10 (b) can be seen as a combination of two parallel single-ended branches. If we consider the nonlinear voltage-to-current conversion, the drain currents of two stages ($I_1$ and $I_2$) can be generally expressed as

$$I_1 = I_B + g_m(v_{i1}) + g_2(v_{i1})^2 + g_3(v_{i1})^3 \tag{2.26}$$

$$I_2 = I_B + g_m(v_{i2}) + g_2(v_{i2})^2 + g_3(v_{i2})^3 \tag{2.27}$$

where $I_B$ is the bias current, and $v_{i1}$ and $v_{i2}$ are the input signals as expressed in equations (2.26) and (2.26). $g_2$ and $g_3$ are used to represent the transconductor non-linearity. Notice that higher order harmonics (greater than third-order) are neglected here.

The output differential current ($i_{o,PD}$) for the PD structures can then be calculated as

$$i_{o,PD} = g_m v_{id} + 2g_2 v_{id} v_{icm} + g_3(3v_{id}v_{icm}^2 + v_{id}^3/4) \tag{2.28}$$

If the same expression is derived for the FD structure ($I_1$ + $I_2$ = const.), the output differential current ($i_{o,FD}$) is

$$i_{o,FD} = g_m v_{id} - \left(\frac{g_2^2}{g_m} - \frac{g_3}{4}\right) v_{id}^3 \tag{2.29}$$

By comparing the above two output differential current equations, PD structure presents an additional distortion term due to common-mode signal. In particular, even-order terms can appear due to the product of the differential and

common-mode signals. To minimize this effect, the transconductance of the PD structure should be designed as linear as possible. Also an efficient common-mode control circuitry is essential to cancel the effect of common-mode signal on its output response. Especially, common-mode feedback (CMFB) and common-mode feedforward (CMFF) circuitry is essential.

### 2.3.2 Common-Mode Feedback (CMFB) Circuits [54 – 82]

Figure 2.11 illustrates conceptual architecture of the use of common-mode feedback (CMFB). The basic idea is to sense the level of the output CM voltage, compare it with a reference voltage and feedback the CM correction signal to the differential amplifier. The correction signal is the difference between output CM signal and the reference voltage ($V_{CM}$). There are two approaches to design CMFB circuits. One is the continuous-time and the other is the switched-capacitor. Although switched-capacitor CMFB (SC-CMFB) circuits [54–56] do not impose any limitation on the output swing of the differential amplifier and have enough accuracy and low static power consumption, they reduce amplifier's unity gain frequency and slew rate and also occupy large area. Moreover, SC-CMFBs suffer from clock feed-through and channel charge injection errors and increase amplifier's load capacitance. Hence, SC-CMFBs are usually used in switched-capacitor applications rather than continuous-time applications. In spite of the lower linearity and output swing of the continuous-time CMFB (CT-CMFB) circuits compared to the SC-CMFBs, do not load differential amplifier considerably and they are faster and occupy smaller area.

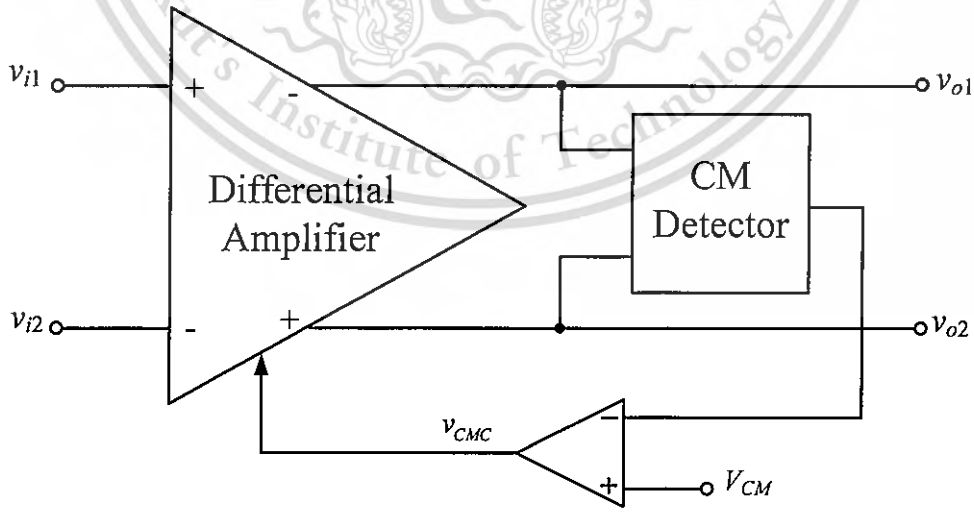



Figure 2.11 Conceptual architecture of CMFB circuit

Several approaches have been proposed to achieve CMFB [54–82]. Simple resistive divider CMFB circuits use resistors to average the voltages of the two

differential nodes and send the result to a differential pair to compare with $V_{CM}$ [57–61], (as shown in Figure 2.12). This technique reduces the common-mode voltage error caused by the nonlinearity of the differential pair. The voltage swing ranges are not limited by the differential pair, and hence, more voltage swing is allowed without a significant offset of common-mode voltage. The disadvantage of the resistive divider CMFB is the requirement of large-valued resistors. Not only do these resistors require more silicon area, but they also load down the output and cause a reduction of the gain. Moreover, they affect output impedances, which are very critical in current-mode systems since they influence the pole and zero locations.

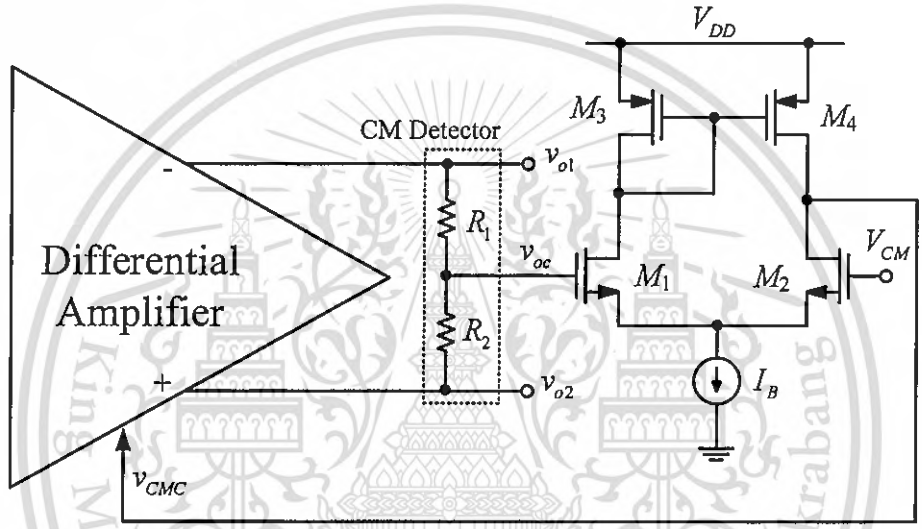



Figure 2.12 Simple resistive-divider CMFB circuit

Figure 2.13 illustrates the schematic of a folded cascade amplifier with MOS resistive network CMFB circuit [62]. The input transistors ($M_1$-$M_2$) and the active load transistors ($M_3$-$M_4$) are biased in the saturation region. Therefore, it is necessary to adjust the current of the transistor $M_{11}$ to twice that of the current passing through $M_3$ or $M_4$. Any variation in biasing voltages $V_{B1}$ or $V_{B2}$ causes a large voltage change at the output ($v_{o1}$ and $v_{o2}$). In order to compensate bias voltage variations, often CMFB circuits are used. Since the tail current transistor ($M_{11}$) is a PMOS transistor, it is possible to apply feedback voltage to its body to counter the biasing voltage variations. Two PMOS transistors ($M_9$-$M_{10}$) are employed to detect the common mode voltage. These two transistors act as two resistors and are of the same size. The feedback voltage ($v_{CMC}$) is constant for differential voltages and changes only if the output common mode voltage changes. Feedback voltage ($v_{CMC}$) is applied to change the body voltage of the tail current source transistor $M_{11}$. However, the circuit has quite low output impedance and high common gain.

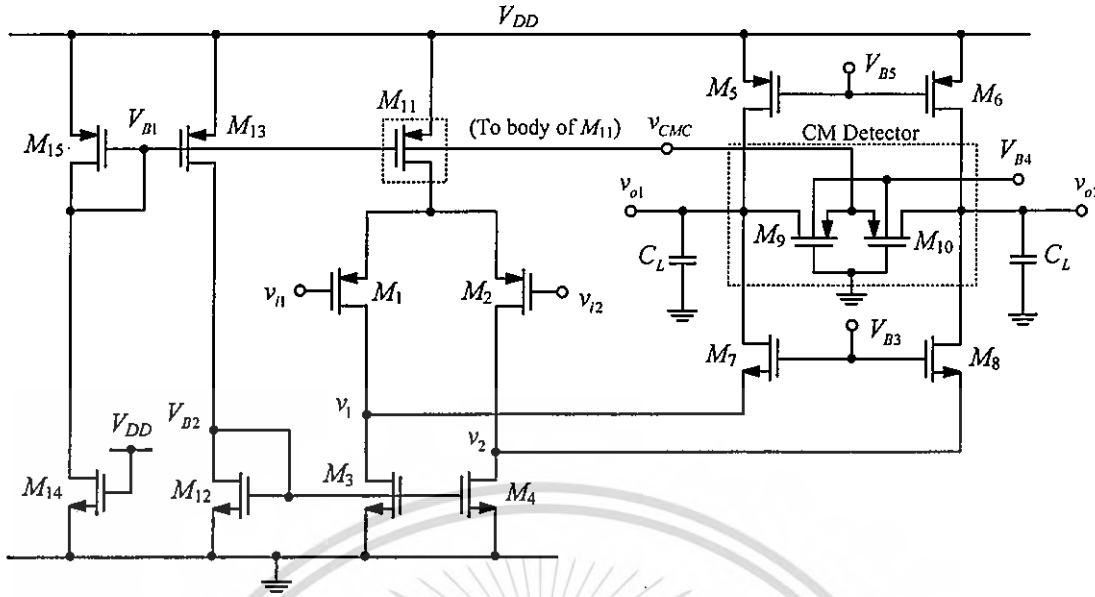



Figure 2.13 Schematic of the folded cascode amplifier with embedded CMFB

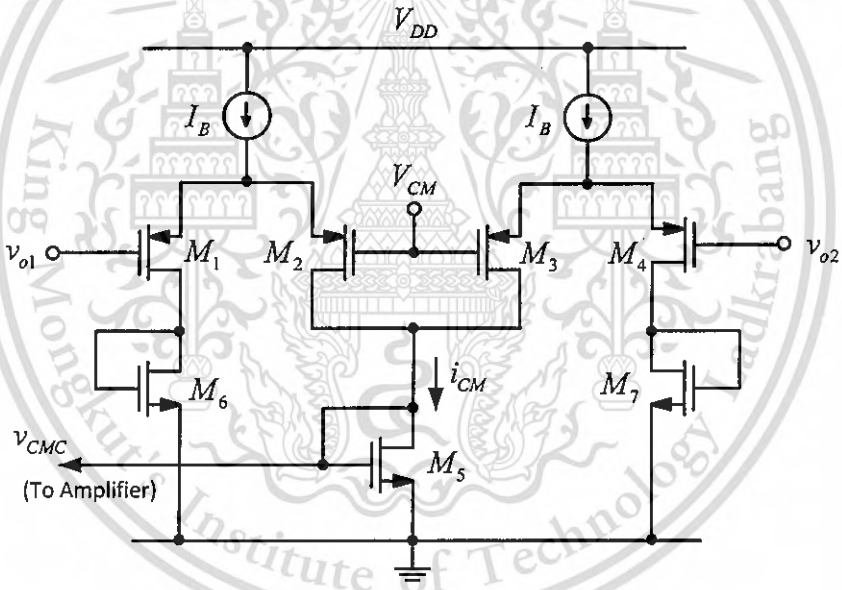



Figure 2.14 MOS transistor as a common-mode feedback circuit

To solve previous problem, Methods of employing MOS transistors as CMFBs were proposed in [63–71]. The CMFBs consist of common-mode (CM) detector and one stage amplifier. For the conventional CMFB circuit shown in Figure 2.14 [70], the matched differential pairs $M_{1\text{-}2}$ and $M_{3\text{-}4}$ connect to the amplifier output $v_{o1}$ and $v_{o2}$, sense the CM output voltage [$v_{oc}$= ($v_{o1}$+$v_{o2}$)/2] of the amplifier, and compare $v_{oc}$ with the desired CM output voltage ($V_{CM}$). A negative feedback loop sets $v_{oc}$ to be about equal to $V_{CM}$ by adjusting a bias current in the amplifier that is related to the CM control signal output of the CMFB circuit, which is $i_{CM}$ [$i_{CM}$=$I_B$+$g_m$($v_{oc}$-$V_{CM}$)] in Figure

2.14. Nevertheless, the CM gain of the circuit is quite high and, in addition, the output swing is limited.

The proposed CMFB circuits in [71–77] are the two-stage common-mode amplifiers as shown in Figure 2.15. The first stage is composed of $M_1$–$M_7$ and current sinks. The second stage is composed of $M_8$–$M_{11}$. By using a two-stage structure, the difference differential amplifier (DDA) CMFB design is not forced to trade-off between gain and input voltage range. The first stage can be optimized to have a wide range to accommodate the input voltage swing, while the second stage can be optimized to have a large gain. A cascode output stage design ($M_8$–$M_{11}$) enables this CMFB to have a very high output impedance, retaining the high-impedance property of the two differential nodes. This two-stage structure, however, introduces two low-frequency poles and has a stability problem. These two poles are introduced by node A (the two differential nodes) and node B (connection between first stage and second stage). A special compensation scheme is required to stabilize the loop (not shown in Figure 2.15). The resulting common-mode gains are quite low. The problem with this structure is the limited output swing and potential oscillation problem. In addition, bipolar transistor technology in [72] is not compatible with the well-known CMOS technology.

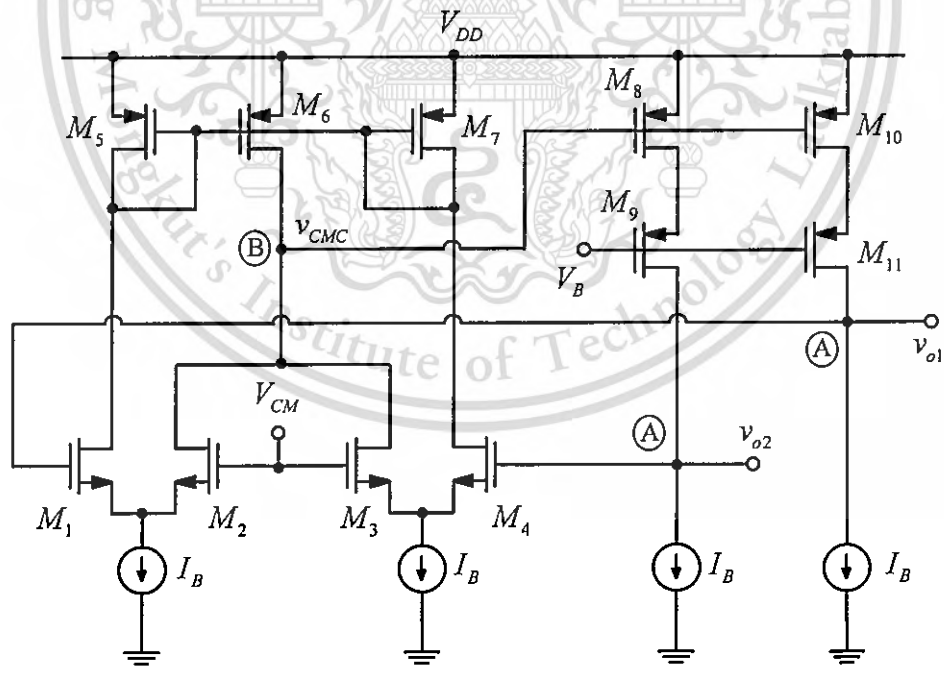



Figure 2.15 Two-stage MOS CMFB circuit for fully differential OTA

Low common mode gains with good output swings were obtained using the complementary CMFB [78–81]. Figure 2.16 shows the schematic of the CMFB circuit

and part of the main amplifier. Both NMOS and PMOS differential pairs are used so that the CMFB circuit still works properly with a large differential input. The common-mode feedback (CMFB) circuit has two gain stages. The first one is from the input to node $v_{CMC}$ and the second one is from node $v_{CMC}$ to the main amplifier output ($v_{o1}$ and $v_{o2}$). Thus, the loop gain of the CMFB circuit is much higher than that of a previous single-stage CMFB circuit. Miller capacitors are used to stabilize the CMFB circuit (not shown in Figure 2.16). However, the circuits are complex and require high power consumption. Additionally, NMOS and PMOS with the same threshold voltage and transconductance are required, which may not be true in general.

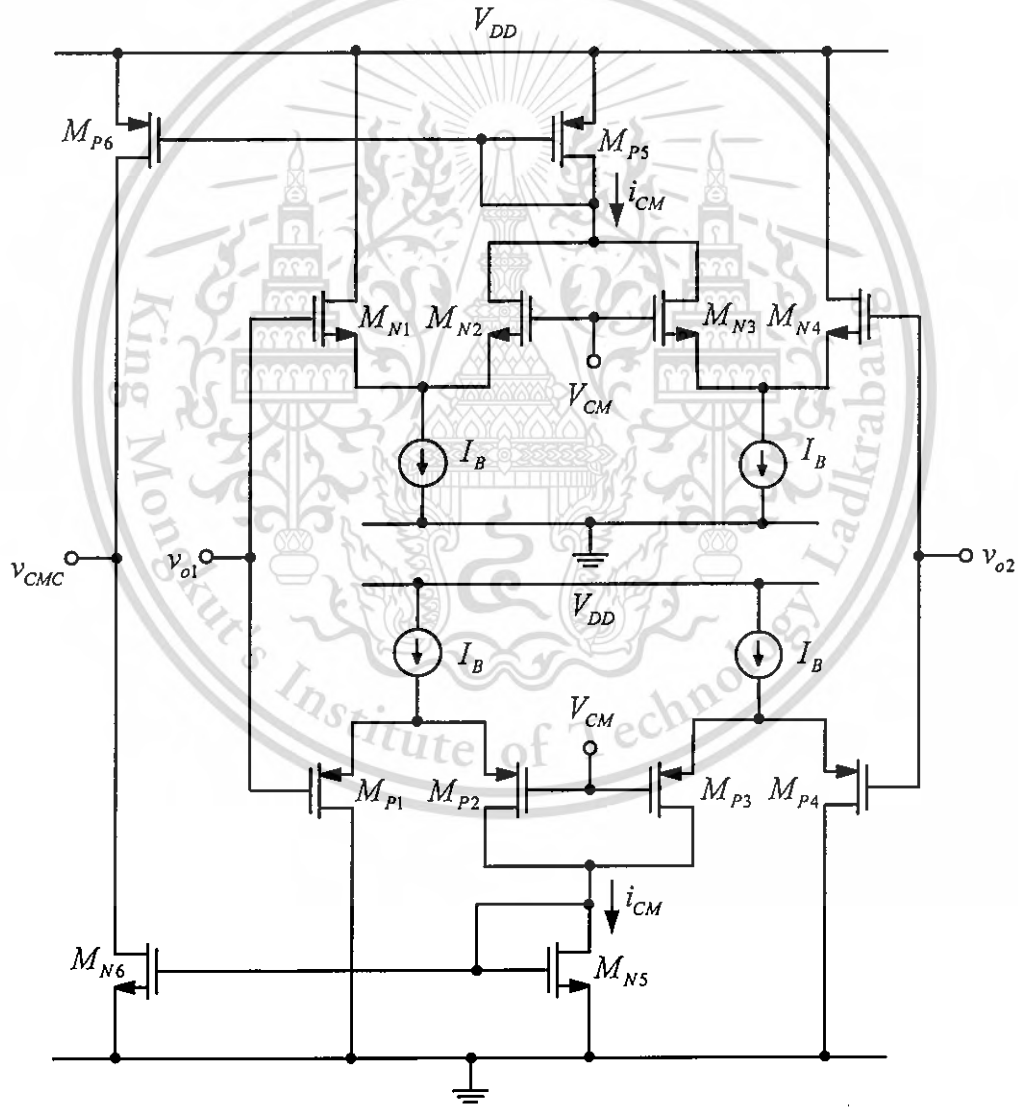



Figure 2.16 Schematic of the complementary CMFB circuit

The transconductor with positive feedback was used in [82–84]. Figure 2.17 shows the schematic of the Nauta transconductor [83]. It consists of six CMOS

inverters, which has no internal nodes and has a good linearity in *V-I* conversion if the factors of the NMOS and PMOS transistors are perfectly matched. The signal amplification is performed by two matched inverters Inv1 and Inv2 both with $\beta_n \approx \beta_p$. The common-mode level of the output voltages $v_{o1}$ and $v_{o2}$ is controlled by the four matched inverters Inv3–Inv6. For simplicity the transconductances ($g_m$) of these inverters are assumed for the moment to be constant ($\beta_n=\beta_p$). The output current of the single CMOS inverter with $\beta_n=\beta_p=\beta_{inv}$ can be given by

$$i_{out} = g_m\left(v_{id} - V_C\right) \tag{2.30}$$

where

$$g_m = \beta_{inv}\left(V_{DD} + V_{TP} - V_{SS} - V_{TN}\right) \tag{2.31}$$

$$V_C \approx \frac{V_{DD} + V_{SS} + V_{TP} + V_{TN}}{2} \tag{2.32}$$

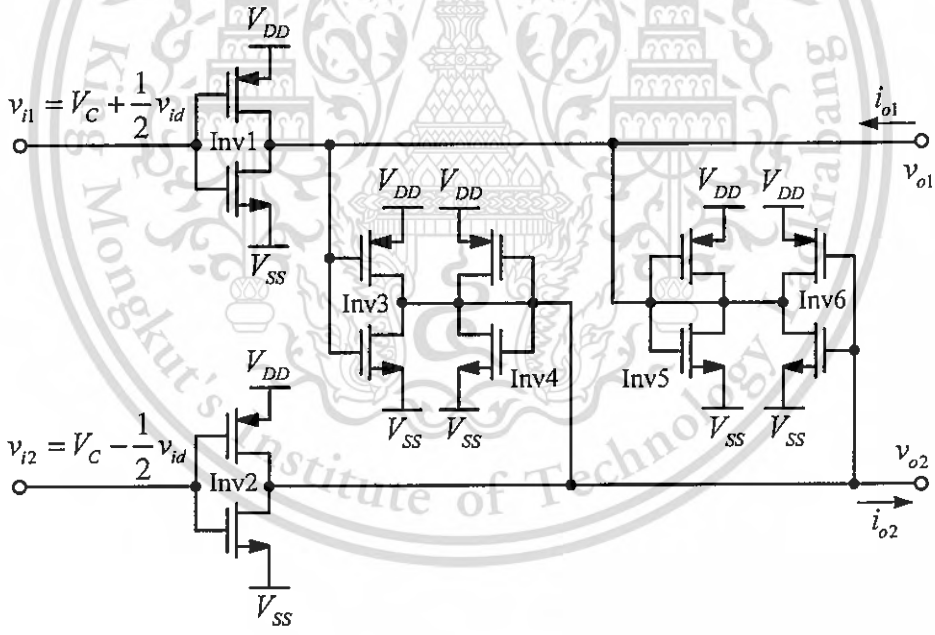



Figure 2.17 Nauta transconductor circuit

The Inverters Inv4 and Inv5 are shunted as resistances connected between the output nodes and the common-mode voltage level $V_C$. The values of these resistances are $1/g_{m4}$ and $1/g_{m5}$. Inv3 and Inv6 inject currents $g_{m3}(V_C-v_{o1})$ and $g_{m6}(V_C-v_{o2})$, respectively, into these resistances.

The result for common-mode output signals is that the output node $v_{o1}$ is virtually loaded with a resistance $1/(g_{m5}+g_{m6})$ and the output node $v_{o2}$ with a virtual resistance $1/(g_{m3}+g_{m4})$. For differential output signals the output node $v_{o1}$ is loaded

with a resistance $1/(g_{m5}-g_{m6})$ and the output node $v_{o2}$ is loaded with a resistance $1/(g_{m4}-g_{m3})$. If the four inverters have the same supply voltage and are perfectly matched, all the transconductance ($g_m$) are equal. Thus the network Inv3-Inv6 forms a low-resistance load for common signals and a high-resistance load for differential signals, resulting in a controlled common-mode voltage level of the outputs. The circuit shows quite high common-mode gain ($A_{cm} \cong -6$ dB).

### 2.3.3 Common-Mode Feedforward (CMFF) Circuits [85 – 86]

A common-mode feedforward (CMFF) circuit was first proposed in [51]. The configuration of pseudo-differential amplifier (PDA) with CMFF uses a separate transconductance ($G_m$) for common-mode (CM) detection, as show Figure 2.18 [51, 86]. This technique consists of adding a parallel replica transconductor whose CM transconductance is equal in magnitude to that of the main transconductor but whose differential transconductance is zero. If the output current of this CM transconductor is subtracted at the output nodes of the PDA, a feedforward cancellation of the CM input signal is performed while preserving the overall differential transconductance. Provided that the CM response of the two parallel paths match perfectly, the structure exhibits an ideally infinite CM rejection.

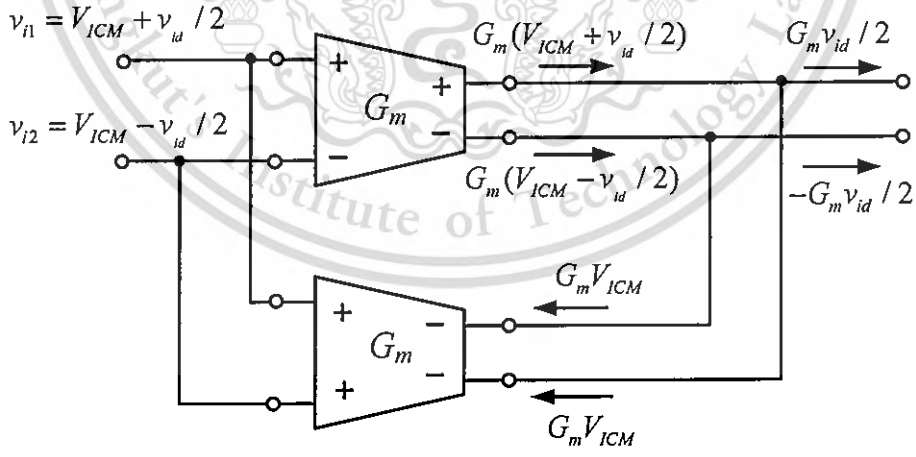



Figure 2.18 Common mode feedforward configuration

A circuit implementation of the PDA with CMFF reported in [53, 86] is shown in Figure 2.19. The currents through the two branches of the differential pair can be written as

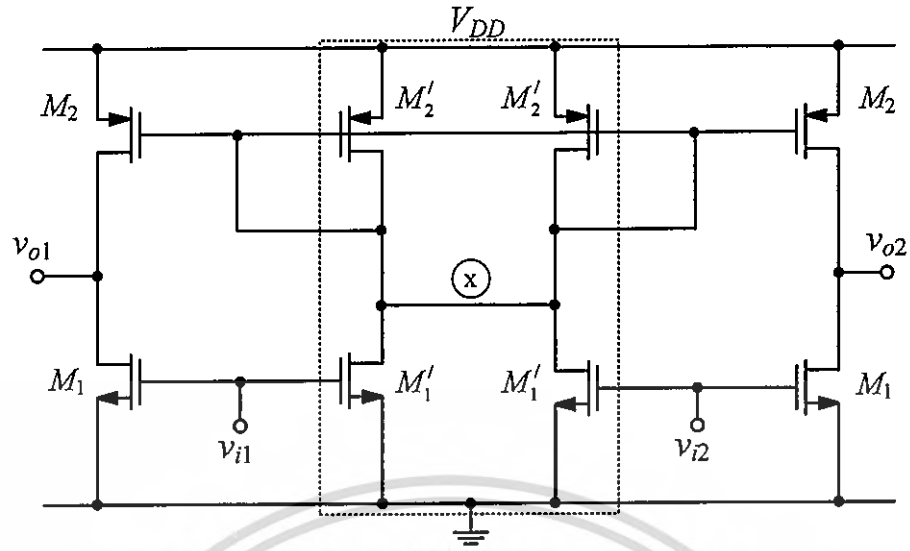



Figure 2.19 Circuit implementation of the PDA with CMFF

$$i_1 = i_{cm} + \frac{i_{od}}{2} = g_m v_{i1} \tag{2.33}$$

$$i_2 = i_{cm} - \frac{i_{od}}{2} = g_m v_{i2} \tag{2.34}$$

where the input voltages $v_{i1}$ and $v_{i2}$ are given by

$$v_{i1} = V_{ICM} + \frac{v_{id}}{2} \tag{2.35}$$

$$v_{i2} = V_{ICM} - \frac{v_{id}}{2} \tag{2.36}$$

From Eqs. (2.33)–(2.36), the differential and common-mode currents are given by

$$i_{od} = i_1 - i_2 = g_m \left( v_{i1} - v_{i2} \right) = g_m v_{id} \tag{2.37}$$

$$i_{cm} = \frac{i_1 + i_2}{2} = g_m V_{ICM} \tag{2.38}$$

where

$$g_m = \mu C_{ox} \frac{W}{L} \left( V_{CM} - V_{TH} \right) \tag{2.39}$$

Using CMFF, the currents at the two differential outputs of the circuit shown in Figure 2.19 are

$$i_{o1} = i_{cm} - i_2 = \frac{i_{od}}{2} \tag{2.40}$$

$$i_{o2} = i_{cm} - i_1 = -\frac{i_{od}}{2} \tag{2.41}$$

Therefore,

$$i_{o1} - i_{o2} = i_{od} = g_m v_{id} \tag{2.42}$$

According to (2.42) the differential transconductance of the circuit presented in Figure 2.19 can be expressed as: $G_m = g_m$ where $g_m$ represent the transconductance of the each transistor which form the input differential pair.

From Figure 2.19, $M_1$ and $M_2$ are the core of the transconductor. $M_1'$ is used to detect the input common-mode signal and convert it into common-mode current. This current flows through $M_2'$ and is mirrored into the main transconductor. The resulting current then cancels the common-mode current generated by $M_1$ and as a result suppresses the common-mode gain. Straightforward circuit analysis shows that the current flowing into the output nodes of the transconductor is

$$i_{ocm} = g_{m1} v_{icm} - g_{m1} v_{icm} \cdot \frac{g_{m2}}{g_{m2} + g_{o1} + g_{o2}} \tag{2.43}$$

$$= v_{icm} \cdot \frac{g_{m1}(g_{o1} + g_{o2})}{g_{m2} + g_{o1} + g_{o2}} \tag{2.44}$$

The common-mode gain $A_{cm}$ is

$$A_{cm} = \frac{v_{ocm}}{v_{icm}} = \frac{g_{m1}(g_{o1} + g_{o2})}{g_{m2} + g_{o1} + g_{o2}} \cdot \frac{1}{g_{o1} + g_{o2}} \tag{2.45}$$

It can be seen from (2.43) that the output common-mode current $i_{ocm}$ is nonzero, which is mainly due to finite output transconductance of the transistors. The common-mode gain can be derived and shown as

$$A_{cm} = \frac{g_{m1}}{g_{m2} + g_{01} + g_{02}} \approx 1 \tag{2.46}$$

It is clearly seen that the common-mode feedforward reduces the common-mode gain to approximately equal to one.

The schematic of the pseudo differential OTA in Figure 2.20 is proposed by [85]. The currents at the two differential outputs of the circuit can be expressed as

$$i_{o1} = i_1 - i_2 = i_d \tag{2.47}$$

$$i_{o2} = i_2 - i_1 = -i_d \tag{2.48}$$

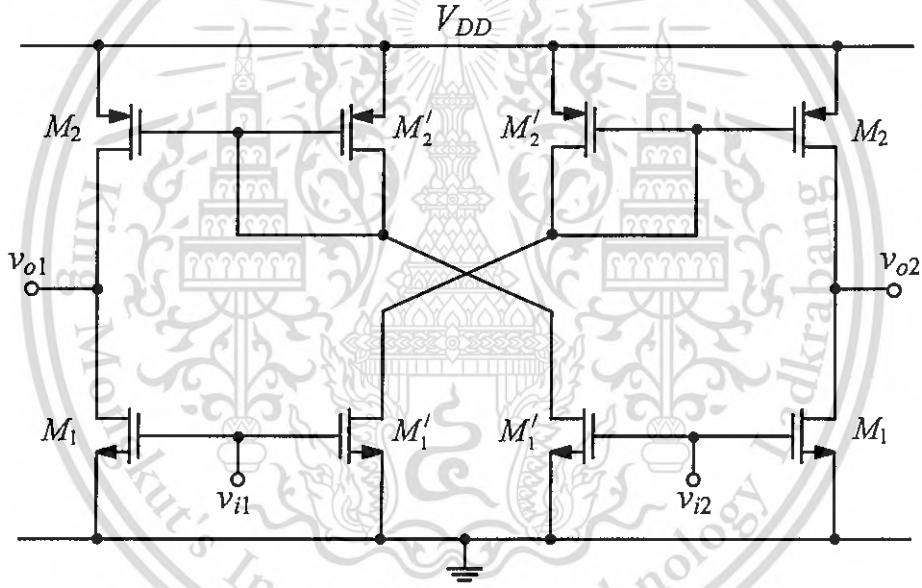



Figure 2.20 Pseudo differential OTA proposes by Edgar [85]

From Eqs. (2.47)-(2.48), the difference between two output current is given by

$$i_{o1} - i_{o2} = 2i_{od} = 2g_m v_{id} \tag{2.49}$$

According to Eq. (2.49), the differential transconductance of the circuit presented in Figure 2.20 can be expressed as

$$G_m = 2g_m \tag{2.50}$$

where $g_m$ represents the transconductance of the each transistor which form the input differential pair. It is obviously that the differential transconductance value of the circuit is twice higher than that of the circuit presented in Figure 2.19, both circuit having the same number of identical transistors.

### 2.3.4 Common-Mode Control Circuit Using Both CMFF and CMFB [87–90]

The combination of a CMFB and a CMFF for the CM control is one interesting technique for pseudo-differential architectures as shown in Figure 2.21. This configuration includes the common-mode feedforward (CMFF) circuit required to reject the input CM signals and supply noise, while a conventional common-mode feedback (CMFB) circuit to fix the common-mode output voltage.

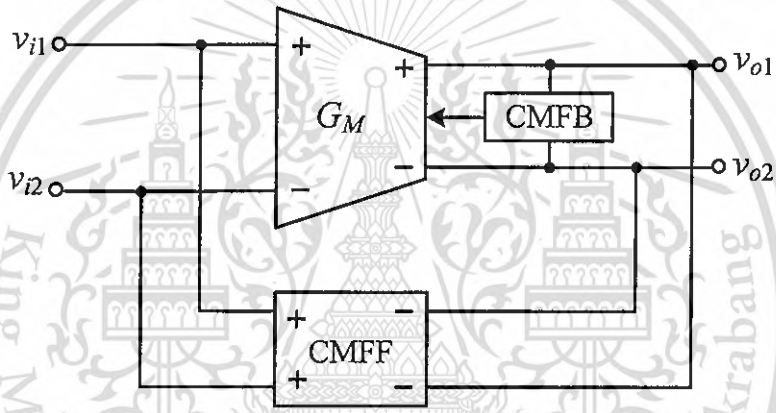



Figure 2.21 CM control using separate CMFB and CMFF

As reported in [87–90], a common-mode control circuit based on CMFF scheme combines CMFF and CMFB. A simplified CMOS version shown in Figure 2.22 is used for explanation. Transistors $M_1$ and $M_2$ compose the main transconductor. The right most part of the transconductor is the CMFF circuit, while the left most part of the main transconductor is the CMFB circuit. An assumption is made here that transistors $M_1$ and $M_1'$ operate in triode region. Transistors $M_1'$ have the half dimensions as $M_1$. The CMFF used here is very similar to the proposed circuit in [90], except that a common-mode reference current $I_{CM}$ is added. The left side CMFB is the same as the CMFF, with the exception that the gates of transistors $M_1'$ are connected to the outputs of the main transconductor.

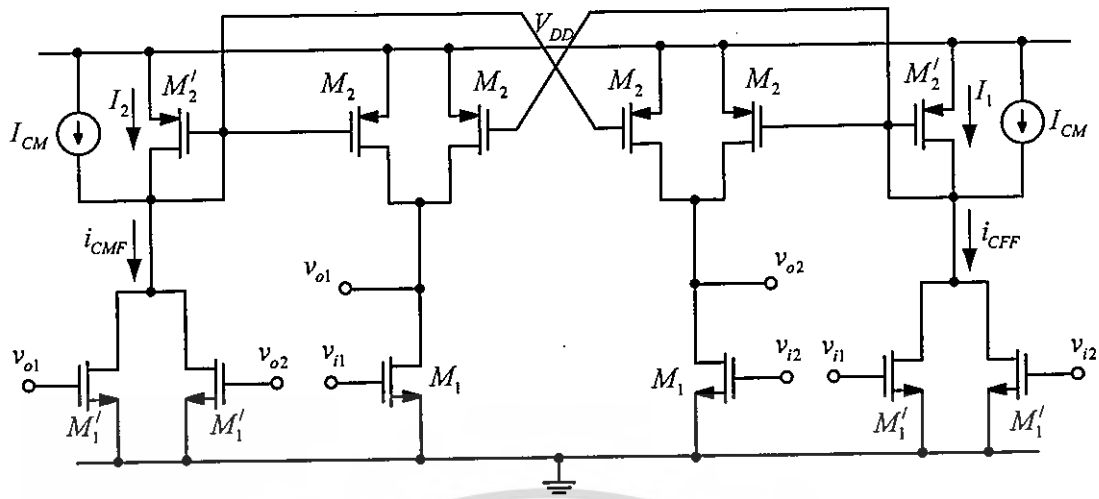



Figure 2.22 the circuit implementation of PD-OTA with CMFF and CMFB

The common-mode reference current $I_{CM}$ shown in Figure 2.22 is

$$I_{CM} = \frac{\beta}{2}\left[V_{CM} - V_{TH} - \frac{1}{2}V_{DS}\right]V_{DS} \tag{2.51}$$

where $V_{CM}$ is the reference common-mode voltage and it is generated by a bias circuit.

The currents $I_1$ and $I_2$ generated by the CMFF and CMFB circuits can be expressed as

$$I_1 = i_{CFF} + I_{CM} = \beta\left[v_{icm} - V_{TH} - \frac{1}{2}V_{DS}\right]V_{DS} \tag{2.52}$$

$$I_2 = i_{CMF} + I_{CM} = \beta\left[v_{ocm} - V_{TH} - \frac{1}{2}V_{DS}\right]V_{DS} \tag{2.53}$$

Currents $i_{CFF}$ and $i_{CMF}$ generated respectively by the CMFF and CMFB are fed back into the main transconductor via two PMOS devices, resulting the following bias current is

$$I_B = i_{CFF} + i_{CMF} \tag{2.54}$$

$$= \beta\left[v_{icm} - V_{TH} - \frac{1}{2}V_{DS}\right]V_{DS} + \beta V_{DS}(v_{ocm} - V_{CM}) \tag{2.55}$$

where the first term corresponds to the current required to reject the input CM signal and the second term corresponds to the current used to set the transconductor output CM voltage $v_{ocm}$ to CM reference voltage $V_{CM}$.

Although, the combination of both CMFF and CMFB will increases the CMRR of the proposed differential OTA topology. However, the OTA consumes high power and requires good-matching MOSFETs to achieve the cancellation of the CM components.

## 2.4 Conclusions

Various low voltage circuit techniques are discussed in this chapter. Bulk–driven circuit technique offers better linearity and larger input common mode range but suffers from limited gain and cut–off frequency. Quasi-floating-gate (QFG) MOSFETs do not take much larger silicon area and they have high–pass filter characteristic. Bulk–driven quasi-floating-gate (BD-QFG) MOSFETs combine the most advantages of BD, and QFG technique, but share some disadvantages of them.

At lower supply voltage, pseudo-differential (PD) OTAs become an interesting choice since they avoid the voltage drop across the bias current source. Since a pseudo-differential structure has the same transconductance for both differential and common mode (CM) signals, the use of this solution requires a careful control of the common-mode behavior. The PD transconductor with CM control techniques presented in this chapter employed the common-mode feedback (CMFB) and common-mode feedforward (CMFF) topologies. The CMFB method is used to set the output voltage of the OTA and suppress the common-mode signal. Nevertheless, the CMFB circuits are still complex, consume large power consumption, and have limited output swing. Furthermore, the CMFF method can also be used to reduce the common-mode signal of the OTA. However, CMFF fails at setting the DC output voltage. Combinations of CMFF and CMFB are combined to suppress the CM signal.

# CHAPTER 3
# PSEUDO DIFFERENTIAL AMPLIFIER (PDA) USING COMMON-MODE FEEDBACK CIRCUITS AND ITS APPLICATIONS

In this chapter, two CMOS pseudo-differential amplifiers (PDAs) using new current-mode common-mode feedback (CMFB) technique with rail-to-rail operation are presented. The CMFB consists of current mirrors and resistors operating as a common-mode detector. The current amplifier, which consists of transimpedance and transconductance, is employed to enhance the loop gain of the CMFB, resulting in minimized relative gain error. The positive feedback is also employed to increase the differential-mode gain of the system. The organization of this chapter is as follows: Section 3.1 introduces the proposed CMOS PDA with current-mode CMFB structure, operating principle, performance analysis, and its application to an oscillator. In Section 3.2, presents the CMOS Inverter-based PDA with CMFB, performance analysis, simulation results and its application as a bandpass filter. Conclusions is discussed in Section 3.3.

## 3.1 CMOS PDA with current-mode common-mode feedback

### 3.1.1 Proposed PDA Architecture and Circuit Implementation

Figure 3.1 illustrates the architecture of the proposed PDA. As seen, the PDA consists of an input transconductor $G_{M(IN)}$ and CMFB. The proposed CMFB consists of two matched resistors ($R_1$=$R_2$), two matched current mirrors and two stage current amplifier (transimpedance and transconductance amplifiers). When the output voltages from $G_{M(IN)}$ are differential signals, these voltages are converted to the currents through resistors $R_1$ and $R_2$ (see solid signal). These currents, which have the same magnitude but opposite phase, flow to each resistor and are mirrored to the $Out_{1A}$ and $Out_{1B}$ terminals (with the current gain of $\beta$). Because these currents have the same magnitude but opposite phase, there will be no input current flowing into the transimpedance amplifier ($R_{MO}$) and, thus no voltage variation at node C. In addition, the currents through resistors $R_1$ and $R_2$ are mirrored to the $Out_{2A}$ and $Out_{2B}$ terminals (with the current gain of $\alpha$), and positively fed back to the output of the input transconductor $G_{M(IN)}$, thus enhancing the output impedance (at node $v_{o1}$ and $v_{o2}$) and differential gain of the system.

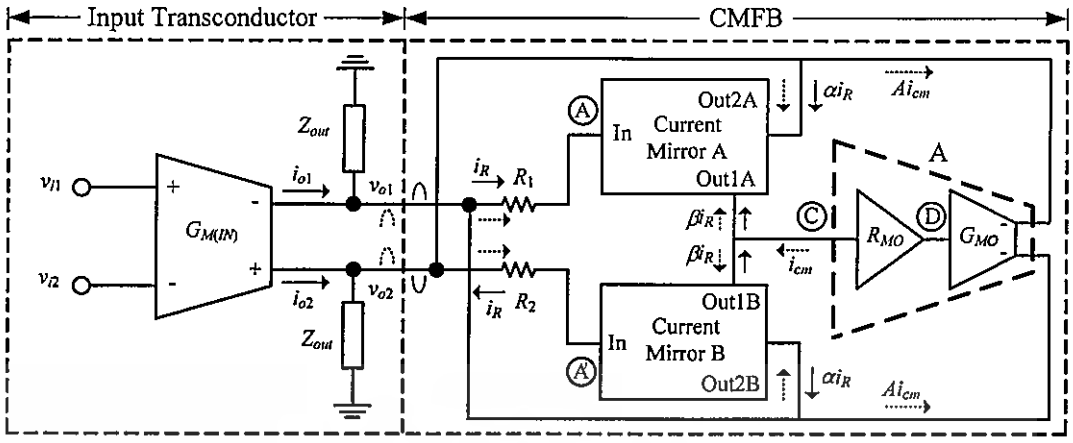



Figure 3.1 Block diagram of the proposed pseudo-differential amplifier (PDA)

When the output voltages from the $G_{M(IN)}$ are common-mode signals, the common-mode current will flow through $R_1$ and $R_2$ (see dash signal) to nodes A and A′ with the same magnitude and phase. As a result, the summation of these two currents at the $Out_{1A}$ and $Out_{1B}$ terminals are added constructively ($i_{cm}$) and passed to the current amplifier ($A$), which consists of the transimpedance ($R_{MO}$) and transconductance ($G_{MO}$) amplifiers. The output current ($Ai_{cm}$) is then negatively fed back to the output node of input transconductor $G_{M(IN)}$, resulting in the reduced output impedance and common-mode gain of the system.

From, Figure 3.1 it can be easily shown that the differential ($Z_{dm}$) and common-mode ($Z_{cm}$) output impedances at nodes $v_{o1}$ and $v_{o2}$ are (see appendix A)

$$Z_{dm} = \frac{Z_{out}}{1+(1-\alpha)Z_{out}/R_{1,2}} \tag{3.1}$$

$$Z_{cm} = \frac{Z_{out}}{1+(1+\alpha+2A\beta)Z_{out}/R_{1,2}} \tag{3.2}$$

where $Z_{out}$ is the output impedance of the input transconductor, $\alpha$ and $\beta$ are current mirror ratios, and $A$ is the current gain and equal to $R_{MO}G_{MO}$.

From Eqs. (3.1) – (3.2), the differential-mode gain ($A_{dm}$) can be derived and shown as

$$A_{dm} = -G_{M(IN)}Z_{dm} = -G_{M(IN)}\left[\frac{Z_{out}}{1+(1-\alpha)Z_{out}/R_{1,2}}\right] \tag{3.3}$$

Similarly, the common-mode gain ($A_{cm}$) can be shown as

$$A_{cm} = -G_{M(IN)}Z_{cm} = -G_{M(IN)}\left[\frac{Z_{out}}{1+(1+\alpha+2A\beta)Z_{out}/R_{1,2}}\right] \quad (3.4)$$

From Eqs. (3.3) and (3.4), the common-mode rejection ratio (*CMRR*) is given by

$$CMRR = \frac{A_{dm}}{A_{cm}} = \left[\frac{1+(1+\alpha+2A\beta)Z_{out}/R_{1,2}}{1+(1-\alpha)Z_{out}/R_{1,2}}\right] \quad (3.5)$$

Obviously, *CMRR* can be increased, if $A=R_{MO}G_{MO}$ is large. In addition, the current mirror ratios $\alpha$ and $\beta$ play roles in determining $A_{dm}$, $A_{cm}$ and *CMRR* of the system.

The circuit implementation of Figure 3.1 is shown in Figure 3.2. $M_{1A,B}$–$M_{2A,B}$ realize the input transconductor $G_{M(IN)}$, while $M_{3A,B}$–$M_{6A,B}$ and $M_7$–$M_9$ realize a current-mode CMFB circuit. As seen, $M_{3A}$–$M_{6A}$ form the current mirror A, while $M_{3B}$–$M_{6B}$ form the current mirror B. Since the impedances at node A (and A′) is very small, the signal swing at node $v_{o1}$ (and $v_{o2}$) is therefore limited by the output swing of the input transconductor ($G_{M(IN)}$). The ratios of $\alpha$ and $\beta$ (in Eqs.(3.1)-(3.5)) can be set by adjusting the aspect rations of $M_{3A,B}$, $M_{6A,B}$ ($\alpha=(W/L)_{6A,B}/(W/L)_{3A,B}$) and $M_{3A,B}$, $M_{5A,B}$ ($\beta=(W/L)_{5A,B}/(W/L)_{3A,B}$), respectively. It is noted that positive-feedback term $\alpha$ can be used to enhance the differential gain of the system. However, it is instructive to note that improper value of $\alpha$ can also drive the system unstable. In practice, $\alpha$ should be set a little bit larger than one to compensate for the loss as a result of the current mirror, which is unable to mirror the input current to the output perfectly. In this work, $\alpha$ is set to 1.5 to enjoy both differential gain and stability.

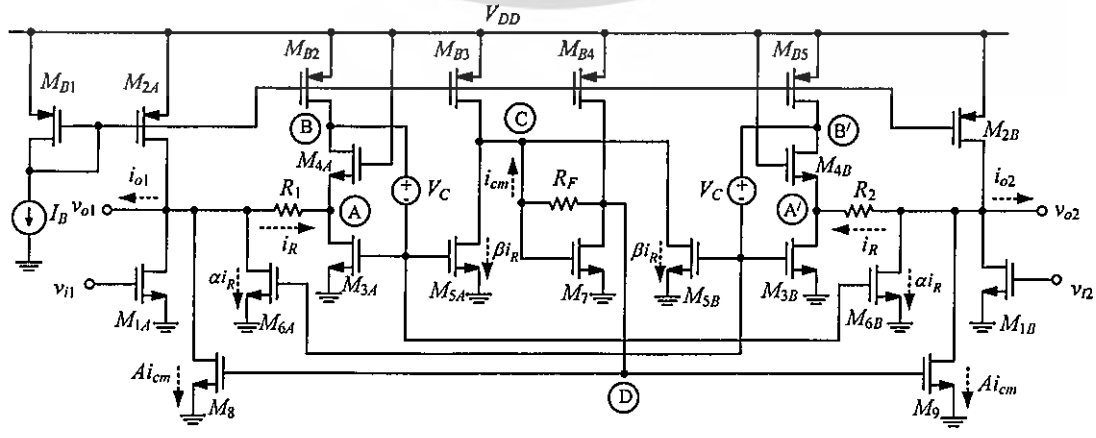



Figure 3.2 The proposed CMOS PDA

The value of $\beta$ plays role in determining the common-mode gain. As seen in Eq.(3.4), large value of $\beta$ results in low common-mode gain. However, it is noted that large $\beta$ requires large transistors, thus large standby current and parasitic capacitors, which can degrade frequency performance of the system. In this work, $\beta$ is set to ten. The dc common-mode voltage of the system can be designed and is equal to $V_{DD}-V_{GS4(A,B)}$. In this work, we set the dc common-mode voltage to $V_{DD}/2$ for the maximum output swing.

One among important factors used to determine the bias current and sizes of $M_{3A,B}$–$M_{6A,B}$ is the impedances at nodes A and A′. Bias current and dimension of these transistors should be chosen, such that the impedances at both nodes are much lower than $R_{1,2}$. As a result, nodes A and A′ can be considered as ac grounds.

The current gain ($A$) of the CMFB depends on the gain of the transimpedance and transconductance amplifiers. Here, transistor $M_7$ and resistor $R_F$ consist to be the transimpedance amplifier ($R_{MO}$), while $M_8$–$M_9$ form the output transconductor ($G_{MO}$). Straightforward analysis shows that $R_{MO}$ and $G_{MO}$ are given by

$$R_{MO} = -R_F \frac{g_{m7}\left(r_{O7} \| r_{O(B4)}\right)}{1+g_{m7}\left(r_{O7} \| r_{O(B4)}\right)} \cong -R_F \tag{3.6}$$

$$G_{MO} = g_{m8,9} \tag{3.7}$$

As mentioned earlier, $A = R_{MO}G_{MO}$ is an important parameter. Gain of CMFB should be sufficiently large so as to obtain the common-mode voltage within the desired accuracy. From Eqs. (3.6) and (3.7), one can increase the value of $A$ by increasing $R_F$ and $g_{m8,9}$. In the design, however, the choice of $R_F$ requires some consideration, because $R_F$ also affects the impedances at node C and node D, thus the time constant of the CMFB. It is known that CMFB should contain minimum number of poles to ensure the stability, and speed of the overall system. Similarly, the value of $G_{MO}$ in Eq. (3.7) needs some consideration, since $g_{m8,9}$ depends on the device dimension and bias current, which affects direclty parasitic capacitances and power consumption, respectively. In fact, the choice of $R_F$ and $g_{m8,9}$ strongly depends on the application for which CMFB is being applied.

### 3.1.2 Performance Analysis

#### 3.1.2.1 Tuning Circuitry

As mentioned earlier, $\alpha$ indicates the amount of the current feedback to the output node, and can be used to adjust the differential mode gain. However, we

have found that $\alpha$ is quite sensitive to the stability of the system. Deviation of $\alpha$ from the desired value could result in a reduced differential gain or even cause system unstable. Since the value of $\alpha$ depends on the matching of transistors, the performance of the system could suffer from process fluctuations. One solution to this problem is to design $\alpha$ with tuning ability.

In this work, we have developed a circuitry, which allows us to tune $\alpha$ electronically. Figure 3.3(a) shows such circuit (see dashed line). As seen, the circuit consists of low voltage current mirror ($M_{T1}$-$M_{T5}$). $M_{T1}$-$M_{T2}$ are used to set the bias voltage at the gates of $M_{T2}$ and $M_{6B}$. The bias current of $M_{T4}$ is mirrored to $M_{T5}$, and cause the bias current of $M_{T2}$ and $M_{6B}$ to be equal. When the signal current $i_R$ flows into the circuit, the variation of the voltage signal at node X will pass through the capacitor $C_X$, and becomes the gate voltage of $M_{6B}$, which is further converted to the signal current $i_{o2}$. Since the $i_{o2}=g_{m6B}V_X$, and $g_{m6B}$ is given by $(2\mu C_{ox}(W/L)I_{Btune})^{1/2}$, one can therefore express the relationship between the output current and input current as

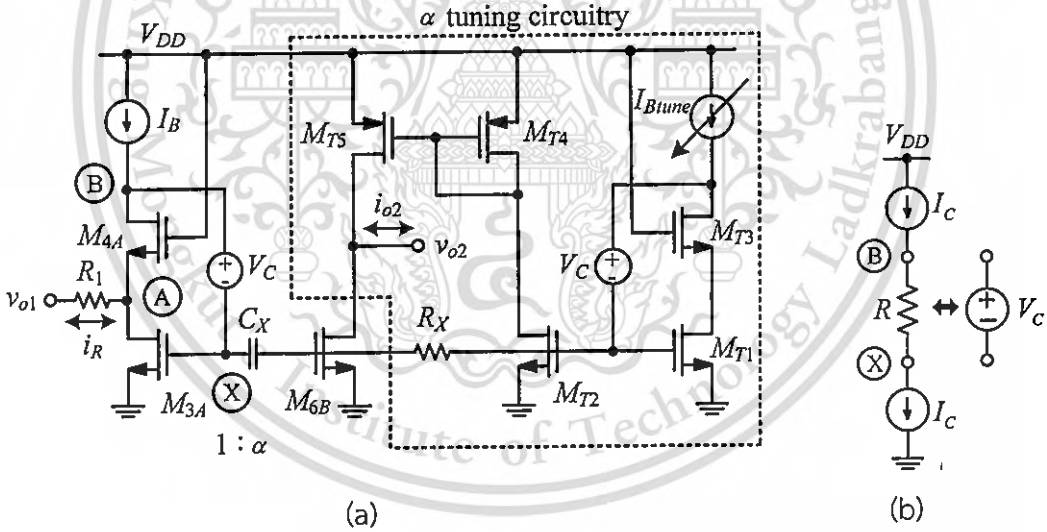



Figure 3.3 (a) An electronically $\alpha$ tuning circuitry and (b) The DC level shifter ($V_C$)

$$\frac{i_{o2}}{i_R} = \alpha = \sqrt{\frac{(W/L)_{6B}}{(W/L)_{3A}}\frac{I_{Btune}}{I_B}} \tag{3.8}$$

From Eq. (3.8), it is obvious that the current gain $\alpha$ can be electronically tuned via the bias current $I_{Btune}$.

The DC level shifters ($V_C$) in Figure 3.2 are designed by using a simple resistor

and the constant current source/sink ($I_C$) as shown in Figure 3.3(b) [91].

### 3.1.2.2 Compensation

Since CMFB introduces additional poles to the system, common-mode stability needs to be investigated. By using small signal analysis, one can find the impedances associated with nodes A (and A′), B (and B′), C and D as

$$R_{A(A')} \approx \frac{1}{g_{m3A,B} g_{m4A,B} \left(r_{OB2}\right)} \tag{3.9}$$

$$R_{B(B')} \approx \frac{1}{g_{m3A,B}} \tag{3.10}$$

$$R_C \approx \frac{R_F + \left(r_{OB4} \| r_{O7}\right)}{1 + g_{m7}\left(r_{OB4} \| r_{O7}\right)} \tag{3.11}$$

$$R_D \approx \frac{R_F + \left(r_{O5A} \| r_{O5B} \| r_{OB3}\right)}{1 + g_{m7}\left(r_{O5A} \| r_{O5B} \| r_{OB3}\right)} \tag{3.12}$$

where $g_m$ and $r_O$ denote transconductance and output resistance of transistor, respectively.

### 3.1.2.3 Geometric and Parametric Mismatches

Since resistor and transistor mismatches may occur due to process gradients, the circuit performance is therefore of concern. We have investigated and found that transistor mismatches in the current mirrors A and B will not affect system performance as long as the impedances at node A and A′ are much smaller than $R_1$ and $R_2$. Since the impedances at node A and A′ are designed to be small, the aforementioned condition can be met.

In case of the mismatch between $R_1$ and $R_2$, this could result in an undesired output voltage. To explain this, let's assume that $R_1=R+\Delta R$ and $R_2=R-\Delta R$, one can show that this mismatch can cause the common-mode output impedances at nodes $v_{o1,o2}$ ($Z_{cm(Vo1)}$ and $Z_{cm(Vo2)}$) to be different.

Straight forward small signal analysis shows these output impedances given by

$$Z_{cm(v_{o1})} = \frac{Z_{out}}{1+\left(\frac{1+\alpha+A\beta}{R+\Delta R}+\frac{A\beta}{R-\Delta R}\right)Z_{out}} \tag{3.13}$$

$$Z_{cm(v_{o2})} = \frac{Z_{out}}{1+\left(\frac{1+\alpha+A\beta}{R-\Delta R}+\frac{A\beta}{R+\Delta R}\right)Z_{out}} \tag{3.14}$$

Since $v_{o1}$ and $v_{o2}$ are $-G_{M(IN)}Z_{cm(Vo1)}v_{ic}$ and $-G_{M(IN)}Z_{cm(Vo2)}v_{ic}$, respectively, one can show that

$$v_{o1}-v_{o2} \cong -G_{M(IN)}\Delta R\frac{2}{\left(1+\alpha+2A\beta\right)^2}v_{ic} \tag{3.15}$$

This differential output voltage, as a result of the resistor mismatch, behaves indistinguishably from the differential output signal, and could propagate to the next stage. From (3.15), one can reduce this undesired output voltage by having large $\alpha$ and large $A\beta$.

In addition to the resistor mismatch, the ratio mismatches in parameters of $\alpha$ and $\beta$, as a result of mismatches in $M_{3A,B}$, $M_{6A,B}$ and $M_{3A,B}$, $M_{5A,B}$ can also cause differential output voltage. If we assume that these ratio mismatches are $\alpha \pm \Delta\alpha$ and $\beta \pm \Delta\beta$, one can easily show that the undesired output voltages are given by (3.16) and (3.17), respectively.

$$v_{o1}-v_{o2} = -G_{M(IN)}\Delta\alpha\frac{R}{2A^2\beta}v_{ic} \tag{3.16}$$

$$v_{o1}-v_{o2} = -G_{M(IN)}\Delta\beta\frac{R}{A\beta}v_{ic} \tag{3.17}$$

Similarily, these output voltage can be reduced if $A\beta$ is large.

### 3.1.2.4 Minimum Supply Voltage and Output Swing

Based on the proposed circuit topology, the minimum supply voltage is given by

$$V_{DD(\min)} = Max\left[\left(V_{GS3,5}+V_C+V_{DSAT(B2,B5)}\right),\left(V_{GS7}+V_{DSAT(B3)}\right),\left(V_{GS4}+V_{DSAT3}\right)\right] \tag{3.18}$$

where $V_{GSx}$ and $V_{DSATx}$ are the gate-source voltage and drain-source saturation voltage of transistor $M_{xA,B}$, respectively. According to Eq. (3.18), it is obvious that the minimum supply voltage strongly depends on the threshold voltage. Therefore, process with low value of $V_{TH}$ can lead to CMFB, which can operate at lower supply voltage.

As previously mentioned, the impedances of the input current mirrors at node A and A′ are very small, thus causing both nodes to operate as virtual ground. As a result, the output swing of PDA (Figure 3.2) is only limited by the output swing of the input transconductor ($G_{M(IN)}$), which is given by

$$V_{DSAT(M1A,B)} \le V_{OUT(Swing)} \le V_{DD} - V_{DSAT(M2A,B)} \tag{3.19}$$

### 3.1.3 RC-Bandpass Filter-Based Oscillator

Figure 3.4 shows an RC bandpass filter-based oscillator using our proposed OTA [92]. In this type of oscillator, the oscillation frequency depends on the bandpass filter, which is made of passive resistors and capacitors, the oscillator frequency is therefore less susceptible to power supply noise. The transfer function of a single-ended simplified circuit of the oscillator (see in Figure 3.4a) can be expressed as

$$H(s) = \frac{v_{out}}{i_{in}} = \frac{\frac{1}{C_1}s}{s^2 + \frac{1 + C_1/C_2 + R_2/R_1}{R_2 C_1}s + \frac{1}{R_1 C_1 R_2 C_2}} \tag{3.20}$$

The center frequency $\omega_o$, the quality factor $Q$ of the filter and the minimum requirement for $G_m$ are given by

$$\omega_o = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}} \tag{3.21}$$

$$Q = \frac{\sqrt{(C_1/C_2).(R_2/R_1)}}{1 + C_1/C_2 + R_2/R_1} \tag{3.22}$$

$$G_{m,\min} \geq \frac{1+C_1/C_2+R_2/R_1}{R_2} \tag{3.23}$$

From Eqs. (3.21)-(3.23) if resistors and capacitors are chosen as $R_1$=$R_2$ =$R$ and $C_1$= $C_2$ = $C$ then $\omega_o$ = 1/($RC$), $G_{m,min}$= 3/$R$ and $Q$ = 1/3.

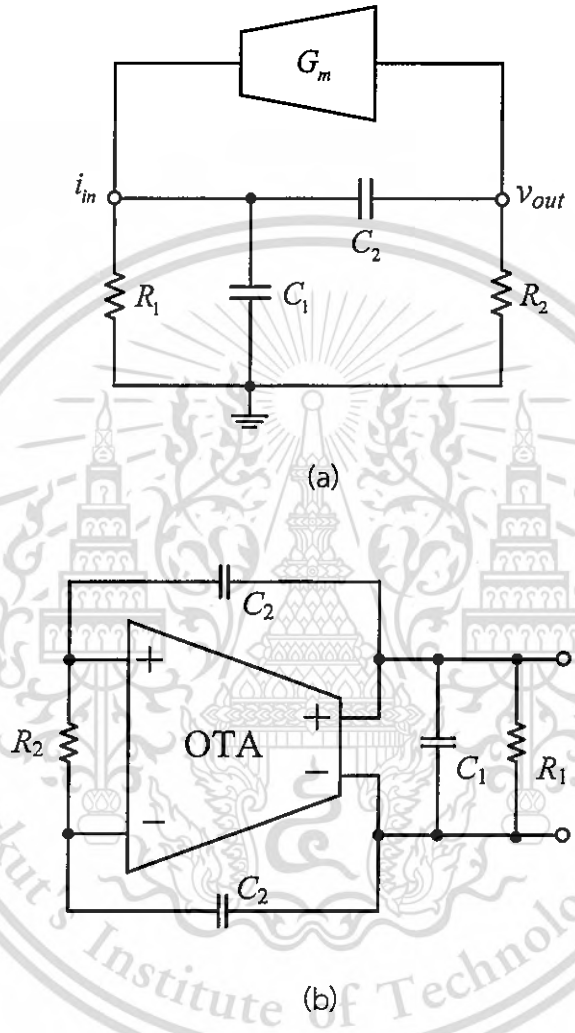



Figure 3.4 Basic structure of proposed oscillator a) Single-ended b) Fully-differential

### 3.1.4 Simulation Results

To verify the circuit performance, HSPICE with BSIM3V3 is used to simulate the proposed circuit using a 0.18 μm CMOS process under 1 V supply voltage. Bias current ($I_B$) is set to 20 μA. This bias current value is chosen to optimize both gain and power dissipation of the circuit. In this work, $R_{1,2}$ and the impedance at node A (and A′) are 50kΩ and 180Ω, respectively. The current consumption of the CMFB and total power dissipation of proposed PDA are 280 μA and 390 μW, respectively. The aspect ratios of the transistors are summarized in Tables 3.1.

Figure 3.5 shows DC transfer characteristic of the PD with the proposed CMFB. As seen, the output swing shows rail-to-rail operation. Figure 3.6 shows the output current ($i_{o2}$) of the circuit in Figure 3.3 for different value of $I_{Btune}$, when the input current ($i_R$) is 10 $\mu A_{pp}$. The circuit demonstrates the current gains ($\alpha$) of 1, 1.3, 1.5 and 1.7, when $I_{Btune}$ are 10 $\mu A_{pp}$, 13 $\mu A_{pp}$, 15 $\mu A_{pp}$ and 17 $\mu A_{pp}$, respectively.

Figure 3.7 shows how DC differential mode gain ($A_{dm}$) varies with $\alpha$. As discussed in Section 3.1, $\alpha$ can be used to enhance the output impedance, and thus differential mode gain of the system. From Figure 3.7 it reveals that as $\alpha$ increases, the differential mode gain increases. It is noted, however, that an increase in $\alpha$ causes bandwidth to decrease. This is because an increase in $\alpha$ will increase the output impedance, and thus the time constant associated with the output nodes.

Figure 3.8 shows the DC common-mode gain for different values of $\beta$ and $R_F$, while Figure 3.9 shows common-mode bandwidth for different values of $\beta$ and $R_F$. As seen, large value of $\beta$ and $R_F$ can cause common-mode gain ($A_{cm}$) to decrease as discussed in Section 3.1. Obviously, the choice of $\beta$ and $R_F$ needs careful consideration. It is noted that large value of $\beta$ also causes more standby current, and thus more power dissipation, while large $R_F$ causes impedances at nodes C and D to increase, and thus degrading the bandwidth of the system. In fact, large $\beta$ results in large parasitic capacitances, and large time constant, which then also causes the common-mode bandwidth of the system to decrease. However, we have observed that an increase in $R_F$ causes common-mode gain bandwidth to decrease more rapidly than an increase in $\beta$, for the same value of common-mode gain. Therefore, power dissipation, chip area and common-mode gain bandwidth are important factors used to justify the value of $\beta$ and $R_F$.

Figure 3.10 shows the transient response of the output voltages for both differential mode ($v_{od}=v_{o1}-v_{o2}$) and common-mode ($v_{oc}=(v_{o1}+v_{o2})/2$), when the differential and common-mode inputs are 17 mV at 10 KHz and $\alpha$, $\beta$ and $R_F$ are 1.5, 10 and 500kΩ, respectively. As seen, the differential output voltage reads ± 0.7 V, while the output common-mode voltage shows only 0.03 mV variation. Figure 3.11 shows frequency response of the proposed PDA for differential mode input signals. The DC gain is found to be 35.6 dB with the –3 dB and unity gain frequency of 10.4 MHz and 1.25 GHz (no load capacitor $C_L$), respectively while the phase margin is 83°. Figure 3.12 shows gain and phase for the common-mode case. As seen, the common-mode gain is small and found to be -36 dB.

Figure 3.13 shows the output waveform. The oscillation frequency is found to be 4 MHz, which is close to the calculated result $R_1=R_2=45k\Omega$, and $C_1=C_2=1pF$ ($f_{osc}=1/2\pi RC\approx$ 3.5 MHz).

Table 3.1 Aspect ratio of MOS transistors

| Transistor | $W$ (μm) | $L$ (μm) |
|---|---|---|
| $M_{1A,B}$ | 9 | 0.3 |
| $M_{2A,B}$ | 33 | 0.5 |
| $M_{3A,B}$, $M_8$, $M_9$, $M_{T1}$ | 6 | 0.3 |
| $M_{4A,B}$, $M_{T3}$ | 8.5 | 0.3 |
| $M_{5A,B}$ | 60 | 0.3 |
| $M_{6A,B}$, $M_{T2}$ | 9 | 0.3 |
| $M_7$ | 18 | 0.3 |
| $M_{B1}$, $M_{B2}$, $M_{B4}$, $M_{B5}$ | 22 | 0.5 |
| $M_{B3}$ | 220 | 0.5 |
| $M_{T4}$, $M_{T5}$ | 17 | 0.5 |

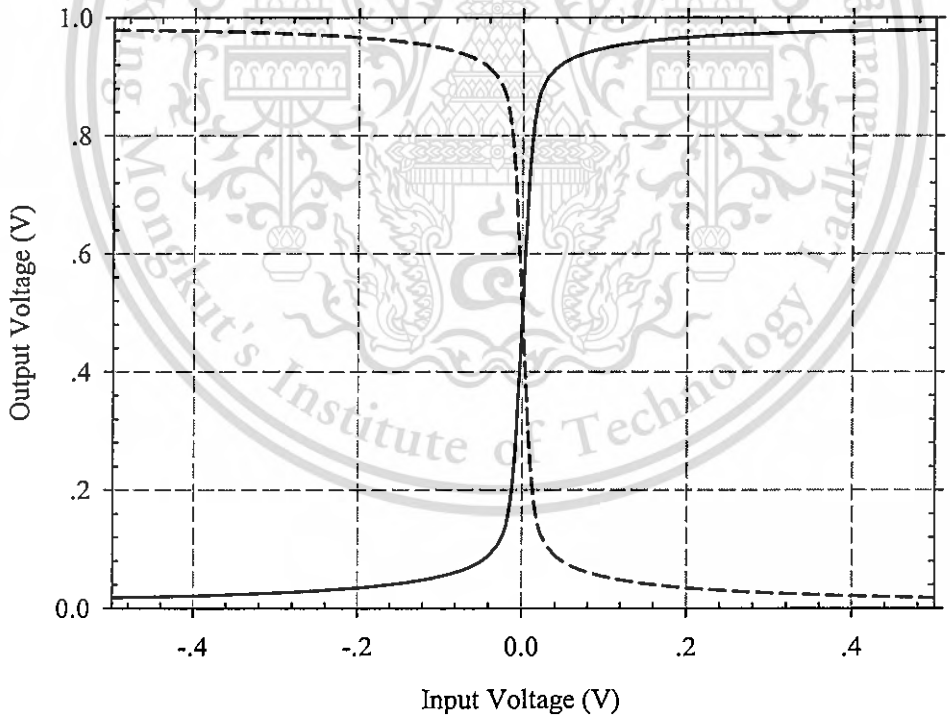



Figure 3.5 DC transfer characteristic

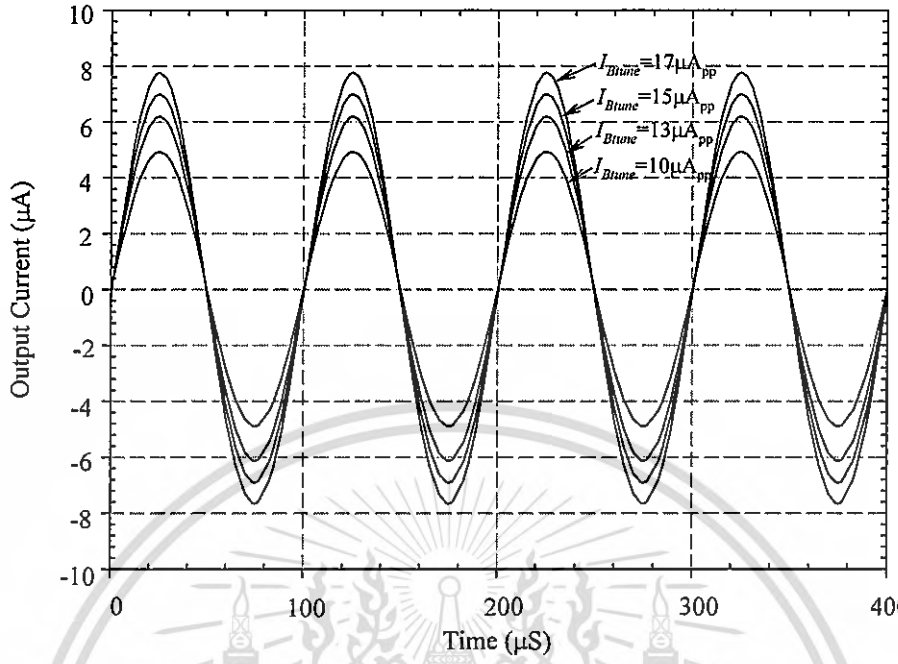



Figure 3.6 Output current ($i_{o2}$) of the circuit in Figure 3.3 for different values of $I_{Btune}$

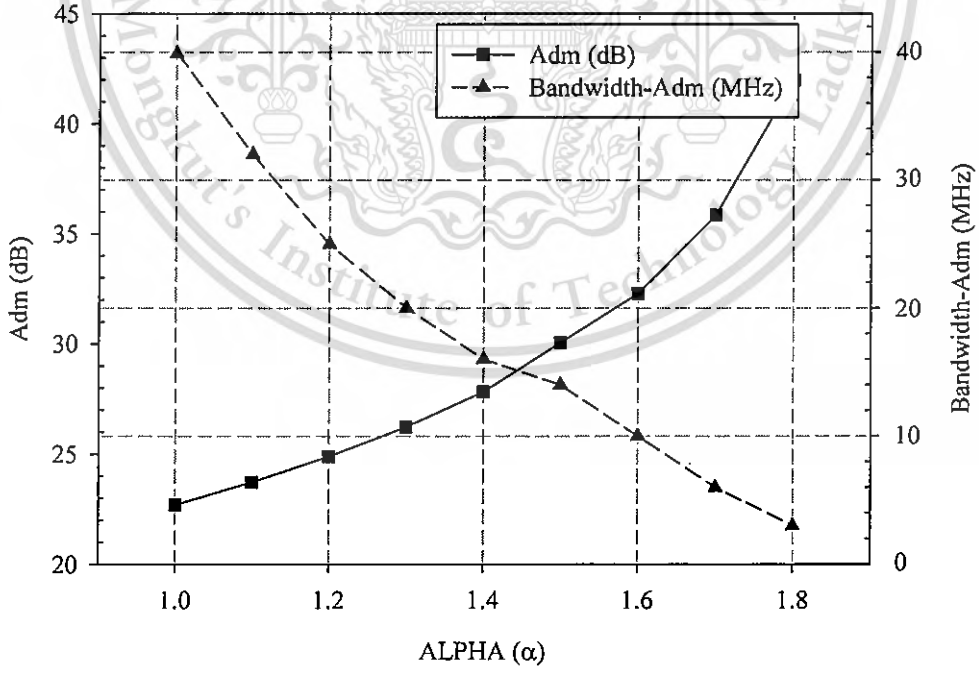



Figure 3.7 Differential-mode gain ($A_{dm}$) versus alpha ($\alpha$)

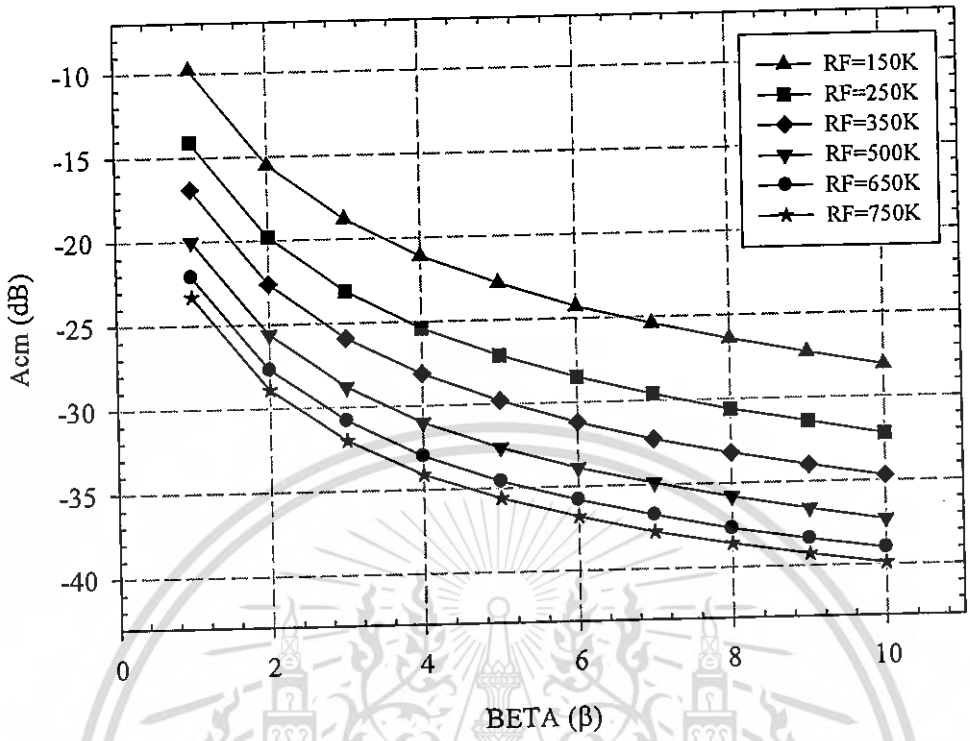



Figure 3.8 Common-mode gain ($A_{cm}$) versus beta ($\beta$)

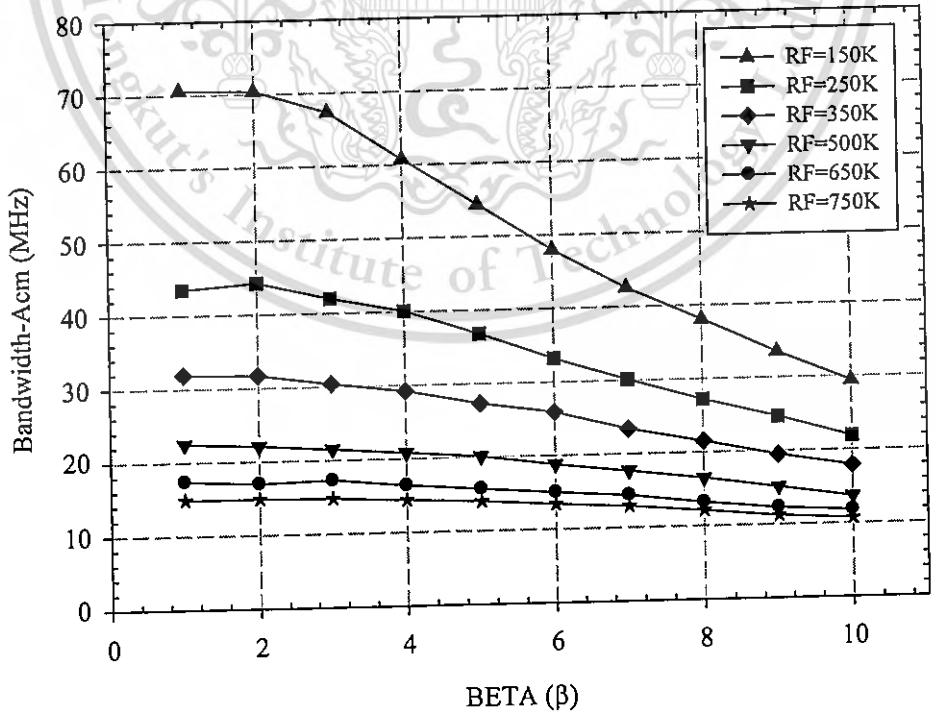



Figure 3.9 Bandwidth of the common-mode gain versus beta ($\beta$)

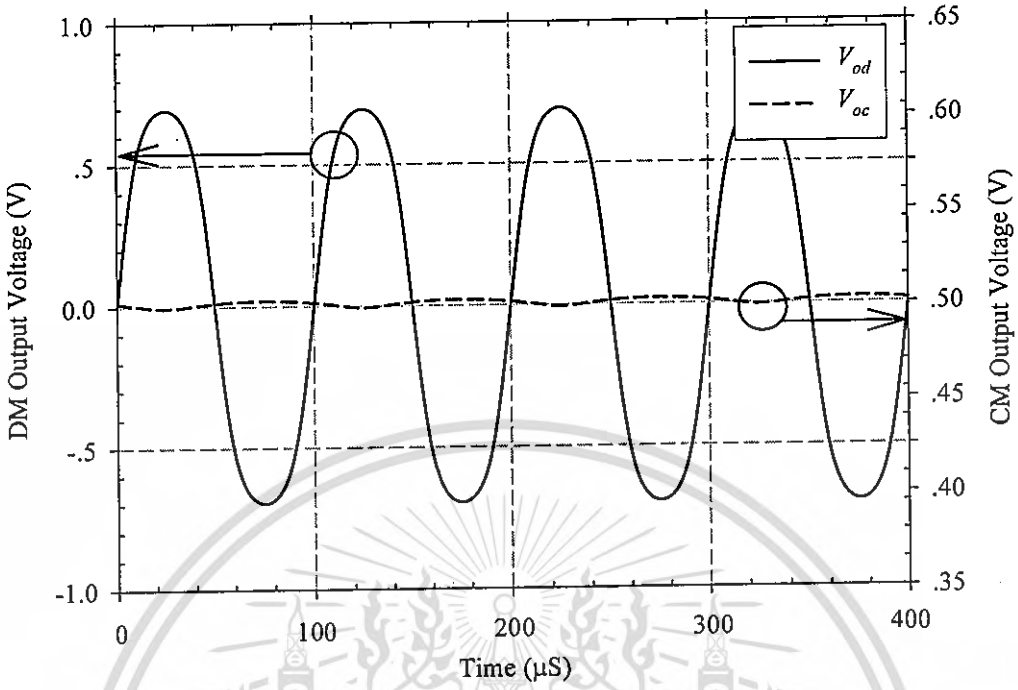



Figure 3.10 Differential-mode and common-mode output voltages

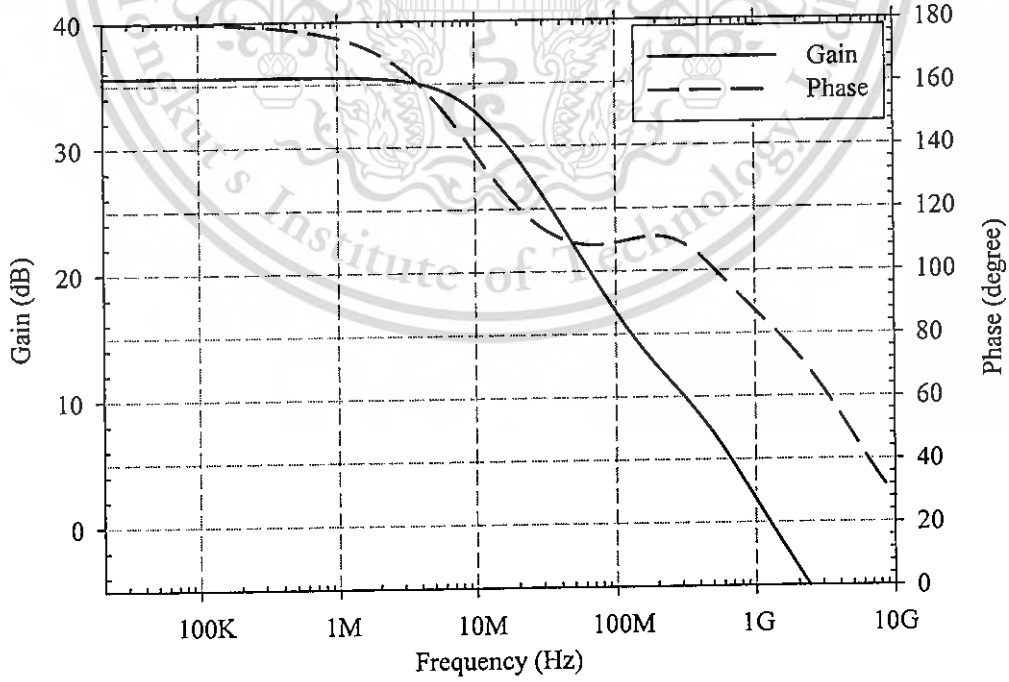



Figure 3.11 Differential-mode gain and phase

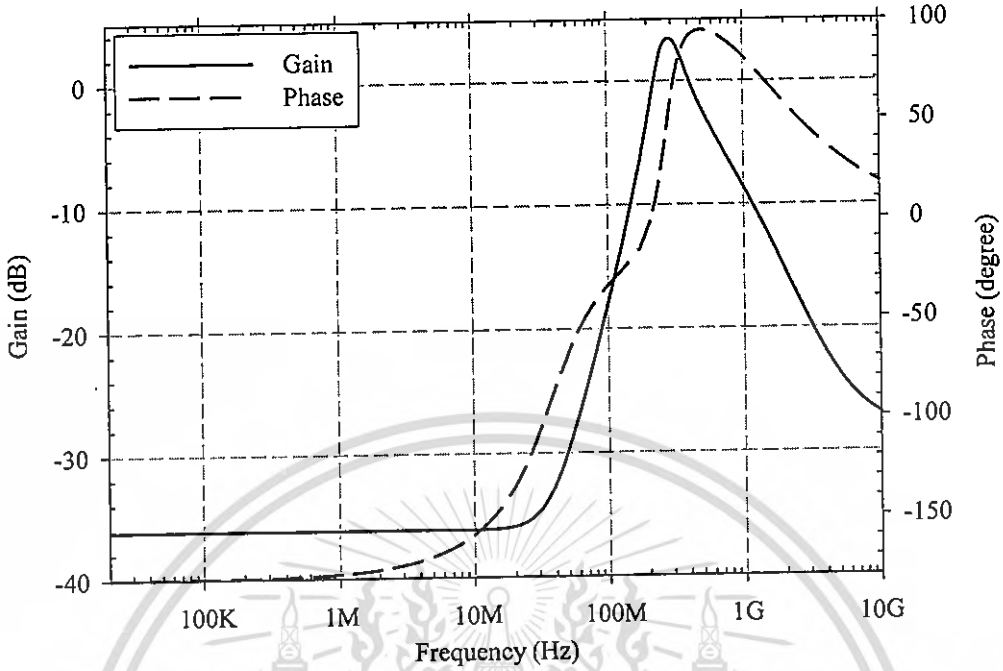



Figure 3.12 Common-mode gain and phase

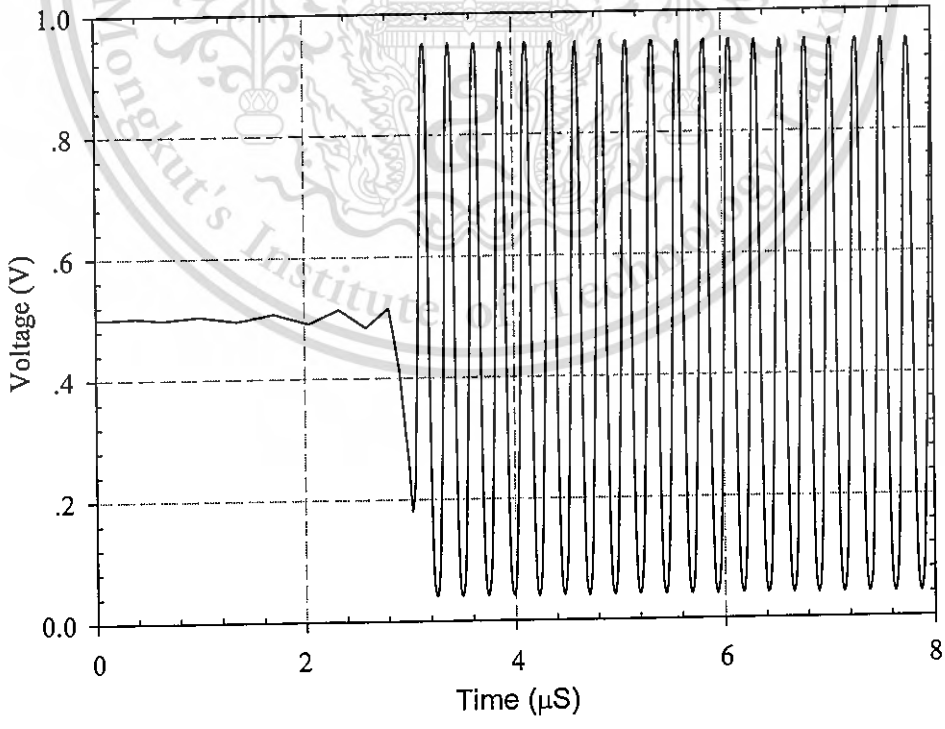



Figure 3.13 Output waveform of the sinusoidal oscillator circuit (see Figure 3.4a)

## 3.2 CMOS Inverter-Based PDA with Common-Mode Feedback

### 3.2.1 Proposed PDA Topology and Circuit Implementation

The topology of a PD structure is shown in Figure 3.14 $G_{m(in)A}$ and $G_{m(in)B}$ are two input transconductors and $Z_{outA}$ and $Z_{outB}$ are the equivalent output impedances of $G_{m(in)A}$ and $G_{m(in)B}$, respectively. Unlike FD structure, PD structure is based on two transconductors without tail current source, making the PD structure suitable for low voltage applications. However, removing the tail current source results in large common-mode gain ($A_{cm}$).

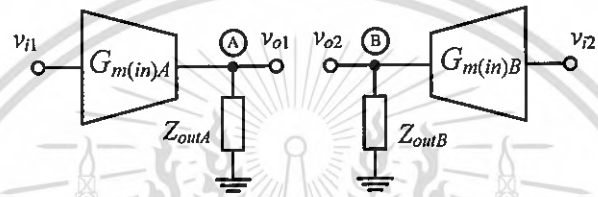



Figure 3.14 Pseudo-differential amplifier topology

From Figure 3.14 the common-mode gain ($A_{cm}$) and the differential-mode gain ($A_{dm}$) are expressed as:

$$A_{cm} = G_{m(in)A(B)} Z_{outA(B)} \tag{3.24}$$

$$A_{dm} = G_{m(in)A(B)} Z_{outA(B)} \tag{3.25}$$

As shown in Eqs. 3.24 and 3.25, the common-mode gain ($A_{cm}$) is the same as the differential-mode gain ($A_{dm}$), resulting in the unity common-mode rejection ratio ($CMRR=A_{dm}/A_{cm}=1$). Since large value of $A_{cm}$ can lead to large common-mode variation at the output [53], common-mode feedback (CMFB) circuit is required.

The conceptual implementation of the proposed pseudo-differential amplifier (PDA) is illustrated in Figure 3.15(a). The proposed PDA consists of two input transconductors ($G_{m(in)A}$ and $G_{m(in)B}$) and a common-mode feedback (CMFB) network. In our design, the CMFB network comprises a common-mode amplifier (CMA) and two output transconductors ($G_{m(out)A}$ and $G_{m(out)B}$). To explain the operation of the proposed PDA, the operation of the CMA, whose topology is shown in Figure 3.15(b), is first examined. The CMA consists of two matched resistors ($R_1 = R_2 = R$), two matched current mirrors (current mirrors A and B), and transimpedance amplifier (TA).

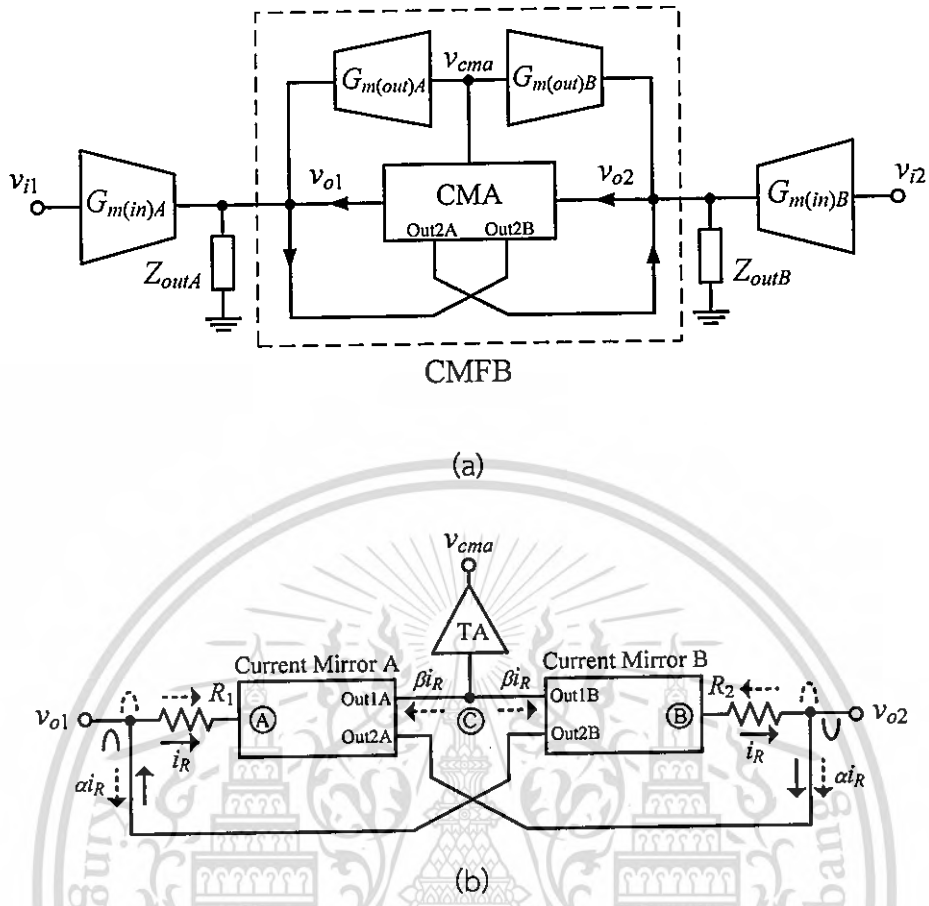



Figure 3.15 Circuit topology of the proposed PDA and b) the common-mode amplifier

When the output voltages ($v_{o1}$ and $v_{o2}$) are common-mode signals ($v_{o1}$=$v_{o2}$) (see dotted line), these voltages are converted into currents through $R_1$ and $R_2$. These common-mode currents with the same magnitude and phase flow through nodes A and B, and are mirrored to Out1A and Out1B terminals with the current gain of $\beta$. These currents are incrementally combined at node C and passed to the transimpedance amplifier (TA). The amplified output voltage $v_{cma}$ is then negatively fed back to the output of the input transconductors ($G_{m(in)A}$ and $G_{m(in)B}$) via the output transconductors ($G_{m(out)A}$ and $G_{m(out)B}$) to suppress the common-mode voltage. In addition, the common-mode currents are mirrored to Out2A and Out2B terminals (with the current gain of $\alpha$) and cross-fed back to the output nodes such that the common-mode gain is further suppressed.

From Figure 3.15, the equivalent common-mode output impedance ($Z_{out(cm)A(B)}$) and common-mode gain ($A_{cm}$) are derived and shown as

$$Z_{out(cm)A(B)} = \frac{Z_{out}}{1+\left(1+\alpha+2G_{m(out)}\beta Z\right)Z_{out}/R} \tag{3.26}$$

$$A_{cm} = G_{m(in)}\left[\frac{Z_{out}}{1+\left(1+\alpha+2G_{m(out)}\beta Z\right)Z_{out}/R}\right] \tag{3.27}$$

where $Z_{out} = Z_{(out)A(B)}$, $G_{m(in)} = G_{m(in)A(B)}$, $G_{m(out)} = G_{m(out)A(B)}$, and $Z$ is the transimpedance gain of the TA.

$Z_{out(cm)A(B)}$ and $A_{cm}$ depend on $\alpha$, $G_{m(out)}$, $\beta$ and $Z$. Obviously, $A_{cm}$ of the proposed PDA can be reduced if the common-mode loop gain $2G_{m(out)}\beta Z(Z_{out}/R)$ is large. It is also worth noting that the proposed topology of CMA allows rail-to-rail operation at the output nodes $v_{o1(2)}$ since input impedances of the current mirrors are relatively small, resulting in small signal variation at nodes A and B.

Let us consider the output voltages as differential signals ($v_{o1} = -v_{o2}$) (see solid signal). These voltages are similarly converted into currents through $R_1$ and $R_2$. However, unlike the previous case, these currents have opposite phase resulting in no current flowing into (and out of) node C and the TA. As a result, the feedback signal $v_{cmo}$ remains constant. It is noticed that the differential currents are also mirrored to Out2A and Out2B terminals and then positively cross-fed back to the output terminals. This positive feedback mechanism enhances the equivalent differential output impedance ($Z_{out(dm)A(B)}$) and, thus, the differential gain ($A_{dm}$) of the system.

$Z_{out(dm)A(B)}$ and $A_{dm}$ are derived and expressed as

$$Z_{out(dm)A(B)} = \frac{Z_{out}}{1+(1-\alpha)Z_{out}/R} \tag{3.28}$$

$$A_{dm} = G_{m(in)}\left[\frac{Z_{out}}{1+(1-\alpha)Z_{out}/R}\right] \tag{3.29}$$

$Z_{out(dm)A(B)}$ and $A_{dm}$ depend on $\alpha$. If $\alpha$ is equal to one, $Z_{out(dm)A(B)}$ and $A_{dm}$ will become very large. This is the direct result of the positive feedback of the differential currents as previously mentioned.

The proposed topology of PDA shown in Figure 3.15 can suppress the common-mode response by the negative feedback mechanism, while the differential-mode gain is enhanced via the positive feedback mechanism. It is noted that, since the voltage signal variations at nodes A and B are small, the output swing of PDA is therefore only limited by the output swing capability of the input transconductors. Furthermore, the CMFB topology contains only low impedance node, thus allowing the PDA to operate at high frequency.

The circuit implementation of the topology in Figure 3.15 is illustrated in Figure 3.16 Transistors $M_{1NA,B}$ and $M_{1PA,B}$ form the input transconductors, while $M_{2NA(B),2PA(B)}$–$M_{4NA(B),4PA(B)}$ and $M_{5N,P}$ form the CMFB circuit. $M_{2N(P)A}$–$M_{4N(P)A}$ form the current mirror A while $M_{2N(P)B}$–$M_{4N(P)B}$ form the current mirror B. The current gains $\alpha$ and $\beta$ are obtained by properly sizing the aspect ratios of the transistors in both current mirrors. It is noted that $M_{1PA(B)}$ and $M_{1NA(B)}$ also serve as the output transconductor ($G_{m(out)A(B)}$) with the transconductance equal to the bulk transconductance of $M_{1PA(B)}$. This efficient design in which a single transconductor is employed as both input and output transconductors simplifies and compacts the circuit. Moreover, the loading effect and power dissipation are minimized.

Transistors $M_{5N,P}$ and resistor $R_F$ form the transimpedance amplifier (TA). The transimpedance gain ($Z$) of the circuit is set by the resistor $R_F$. The transimpedance amplifier helps to increase the gain of the common-mode amplifier (CMA) and simultaneously reduce the impedances at nodes C and D such that the time constants associated with these nodes are low. The body bias voltage $V_{BP}$ is set to reduce the threshold voltage of PMOS transistors, allowing the circuit to operate at low supply voltage.

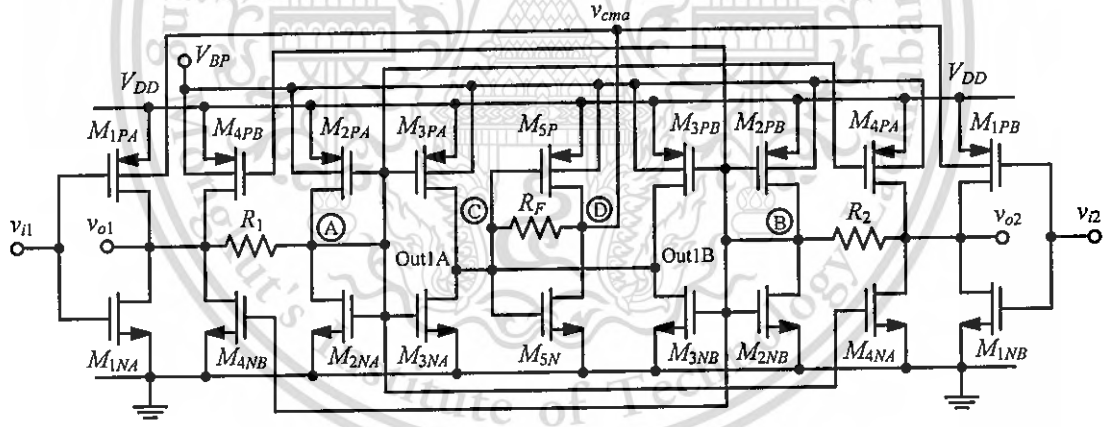



Figure 3.16 Circuit implementation of Figure 3.15

By comparing Figure 3.15 and Figure 3.16, the input transconductance ($G_{m(in)}$), output transconductance ($G_{m(out)}$), equivalent output impedances at node $v_{o1(2)}$ ($Z_{out}$), and transimpedance gain ($Z$) can be expressed as

$$G_{m(in)} = g_{m1N} + g_{m1P} \tag{3.30}$$

$$G_{m(out)} = g_{mb1P} \tag{3.31}$$

$$Z_{out} = r_{O1N} \parallel r_{O1P} \parallel r_{O4N} \parallel r_{O4P} \tag{3.32}$$

$$Z = -R_F \tag{3.33}$$

where $g_{mi}$, $g_{mbi}$ and $r_{Oi}$ are the transconductance, bulk transconductance and drain-to-source resistance of the transistor $M_{iA(B)}$, respectively.

By substituting Eqs.(3.30)-(3.33) in Eqs. (3.26)-(3.29), $Z_{out(cm)}$, $Z_{out(dm)}$, $A_{cm}$ and $A_{dm}$ can be expressed as

$$Z_{out(cm)} = \frac{R}{1+\alpha-2g_{mb1P}\beta R_F + R\left(r_{O1N} \| r_{O1P} \| r_{O4N} \| r_{O4P}\right)^{-1}} \tag{3.34}$$

$$Z_{out(dm)} = \frac{R}{1-\alpha+R\left(r_{O1N} \| r_{O1P} \| r_{O4N} \| r_{O4P}\right)^{-1}} \tag{3.35}$$

$$A_{cm} = \left(g_{m1N}+g_{m1P}\right)\frac{R}{1+\alpha-2g_{mb1P}\beta R_F + R\left(r_{O1N} \| r_{O1P} \| r_{O4N} \| r_{O4P}\right)^{-1}} \tag{3.36}$$

$$A_{dm} = \left(g_{m1N}+g_{m1P}\right)\frac{R}{1-\alpha+R\left(r_{O1N} \| r_{O1P} \| r_{O4N} \| r_{O4P}\right)^{-1}} \tag{3.37}$$

From Eqs. (3.36) and (3.37), the common-mode rejection ratio (*CMRR*) can be derived as

$$CMRR = \frac{A_{dm}}{A_{cm}} = \frac{\left(1+\alpha-2g_{mb1P}\beta R_F\right)\left(r_{O1N} \| r_{O1P} \| r_{O4N} \| r_{O4P}\right)+R}{\left(1-\alpha\right)\left(r_{O1N} \| r_{O1P} \| r_{O4N} \| r_{O4P}\right)+R} \tag{3.38}$$

It is noticed that *CMRR* can be increased if $R_F$ is large. In addition, $\alpha$ and $\beta$ also play a role in determining the *CMRR*.

It is noted that the choice of $\alpha$ requires precaution. A large value of $\alpha$ can result in a large differential gain; however, such a large value of $\alpha$ can drive the circuit unstable. In practice, $\alpha$ should be set slightly larger than one to compensate for the loss, due to the imperfection of the current mirror not being able to perfectly mirror the current from the input to the output. In this work, $\alpha$ is set to 1.3 to enjoy both differential gain and stability. The value of $\beta$ plays a role in the determination of the common-mode gain as it is part of the CMFB circuit. From Eq. (3.36), large value of $\beta$ results in low common-mode gain. Nevertheless, large $\beta$ requires large transistors; thus large standby current and parasitic capacitors, which can degrade the frequency performance of the system. In this work, $\beta$ is set to 5.

The output common-mode voltage ($V_{out(cm)}$) is equal to the voltages at nodes A and B, which is given by [93]

$$V_{out(cm)} = \frac{V_{DD} - V_{TN2A(B)} + V_{TP2A(B)}}{1+\sqrt{\beta_{N2A(B)}/\beta_{P2A(B)}}} + V_{TN2A(B)} \tag{3.39}$$

where $\beta_{N2A(B)}=\mu_n C_{OX}(W/L)_{2A(B)}$ and $\beta_{P2A(B)}=\mu_p C_{OX}(W/L)_{2A(B)}$

For maximum output swing, $\beta_{N2A(B)}$ and $\beta_{P2A(B)}$ should be such that $V_{out(cm)}$ is equal to $V_{DD}/2$.

### 3.2.2 Performance Analysis

#### 3.2.2.1 Loop Gain and Frequency Response

The frequency compensation of the common-mode loop is accomplished by adding a resistor $R_C$ and capacitor $C_C$ in series between nodes C and D (not shown in Figure 3.16). The small-signal equivalent circuit with $R_C$ and $C_C$ can be shown in Figure 3.17, where $r_{oC(D)}$ and $C_{oC(D)}$ are the total parasitic resistance and capacitance at node C(D), $r_{oL}$ (= $r_{O1N} \| r_{O1P} \| r_{O4N} \| r_{O4P}$) and $C_{oL}$ (= $C_{DBN1}+C_{DBP1}+C_{DBN4}+C_{DBP4}$) are the equivalent resistance and capacitance at the output of the PDA, respectively.

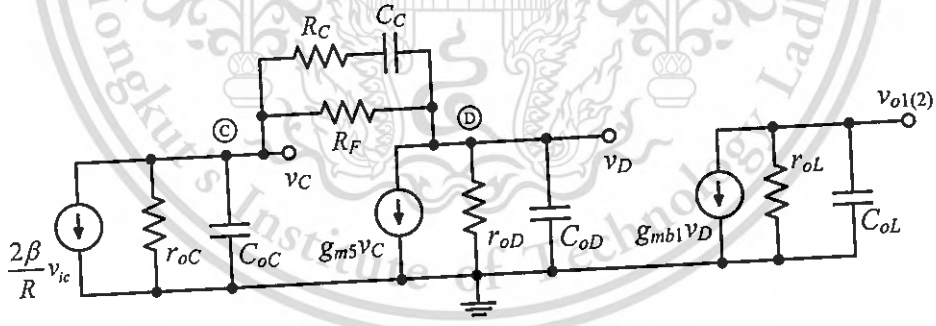



Figure 3.17 Simplified small-signal CMFB loop

By using typical circuit analysis, the open-loop gain of the proposed CMFB is

$$A_{CMFB}(s) = \frac{A_{CMFB}(0)\left(1+\frac{s}{\omega_{Z1}}\right)}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)\left(1+\frac{s}{\omega_{P3}}\right)\left(1+\frac{s}{\omega_{P4}}\right)} \tag{3.40}$$

where $A_{CMFB}(0)$ is the small-signal DC gain of the CMFB loop expressed as

$$A_{CMFB}(0) \approx -\frac{2\beta g_{mb1P} r_{oL} R_F}{R} \tag{3.41}$$

From Eq. (3.40), there are one dominant LHP pole, three non-dominant LHP poles and one LHP zero, each of which is determined by:

$$\omega_{Z1} \approx -\frac{1}{C_C R_C} \text{ (LHP ZERO)} \tag{3.42}$$

$$\omega_{P1} \approx -\frac{1}{r_{oL} C_{oL} + C_C (R_C + R_F)} \text{ (LHP POLE)} \tag{3.43}$$

$$\omega_{P2} \approx -\frac{r_{oL} C_{oL} + C_C (R_F + R_C)}{C_{oL} C_C r_{oL} (R_F + R_C)} \text{ (LHP POLE)} \tag{3.44}$$

$$\omega_{P3} \approx -\frac{g_{m5}}{(C_{oC} + C_{oD})} \text{ (LHP POLE)} \tag{3.45}$$

$$\omega_{P4} \approx -\frac{C_{oC} C_{oD} + C_C (C_{oC} + C_{oD})}{C_{oC} C_{oD} C_C R_C} \text{ (LHP POLE)} \tag{3.46}$$

From Eqs. (3.41) and (3.43), the gain bandwidth product (*GBW*) of the CMFB loop is

$$GBW = A_{CMFB}(0) \cdot \omega_{P1} = \frac{2\beta g_{mb1P} r_{oL} R_F}{R} \cdot \frac{1}{r_{oL} C_{oL} + C_C (R_C + R_F)} \tag{3.47}$$

The first non-dominant pole is $\omega_{P2}$. Since $\omega_{P3}$ and $\omega_{P4}$ are far away from the unity-gain frequency, the overall phase margin can be determined as

$$PM \approx 180° - tan^{-1}\left(\frac{GBW}{\omega_{P1}}\right) - tan^{-1}\left(\frac{GBW}{\omega_{P2}}\right) + tan^{-1}\left(\frac{GBW}{\omega_{Z1}}\right) \tag{3.48}$$

According to Eq. (3.48) and Figure 3.17, $\omega_{Z1}$ is the left half-plane zero and lower frequency than $\omega_{P3}$ and $\omega_{P4}$. This zero will add positive phase margin to the frequency response of the CMFB, simplifying design of stable amplifier for unity gain in differential mode.

### 3.2.2.2 Noise Analysis

The input-referred noise voltage of MOSFET is dominated by flicker noise at low frequency and by thermal noise at high frequency. The input-referred noise spectral density of the PDA can be calculated and shown as (see appendix D)

$$\overline{V_n^2} \approx \overline{V_{n,(1/f)}^2} + \overline{V_{n,th}^2} \tag{3.49}$$

where $V_{n,(1/f)}$ is the input-referred flicker noise determined by

$$\overline{V_{in(1/f)}^2} = \frac{2}{C_{OX} f}\left(\frac{K_N}{(WL)_{1N}} + \frac{K_P}{(WL)_{1P}}\right) \tag{3.50}$$

and $V_{n,th}$ is the input-referred thermal noise determined by

$$\overline{V_{in,th}^2} = 8\frac{k_B T}{\left(g_{m1N} + g_{m1P}\right)^2}\left[\frac{2}{3}\left(g_{m1N} + g_{m1P} + g_{m4N} + g_{m4P}\right) + \frac{1}{R}\right] \tag{3.51}$$

where parameters $K_N$ and $K_P$ are the flicker noise process-dependent constants of NMOS and PMOS, respectively. $k_B$ is the Boltzmann constant, $T$ is the absolute temperature, $f$ is frequency, and other parameters have their usual meanings.

From Eqs. (3.50) and (3.51), the input-referred noise can be lowered by increasing ($g_{m1N}$+$g_{m1P}$) and/or sizes of $M_{1NA(B)}$ and $M_{1PA(B)}$. Obviously, the amplifier suffers from a fundamental tradeoff between its noise performance and frequency response.

### 3.2.2.3 Geometric and Parametric Mismatches

Since resistor and transistor mismatches are practically unavoidable, the circuit performance accounting for mismatches is therefore of concern. It is found that system performance is unaffected by transistor mismatches in the current mirrors A and B as long as the impedances at nodes A and B are much smaller than those of $R_1$ and $R_2$. Since the impedances at nodes A and B are designed to be small, the aforementioned condition can be readily met.

In case of the mismatch between $R_1$ and $R_2$, this could result in an undesired output voltage. To clarify this point, it is assumed that $R_1$=$R$+$\Delta R$ and $R_2$=$R$–$\Delta R$ and the results reveal that this mismatch can cause the common-mode output impedances at nodes $v_{o1}$ and $v_{o2}$ (i.e., $Z_{out(cm)A}$ and $Z_{out(cm)B}$) to be different.

The straightforward small signal analysis shows $Z_{out(cm)A}$ and $Z_{out(cm)B}$ are determined by

$$Z_{out(cm)A} = \frac{1}{\frac{1+\alpha-g_{mb1P}\beta R_F}{R+\Delta R} - \frac{g_{mb1P}\beta R_F}{R-\Delta R} + \left(r_{O1N} \| r_{O1P} \| r_{O4N} \| r_{O4P}\right)^{-1}} \tag{3.52}$$

$$Z_{out(cm)B} = \frac{1}{\frac{1+\alpha-g_{mb1P}\beta R_F}{R-\Delta R} - \frac{g_{mb1P}\beta R_F}{R+\Delta R} + \left(r_{O1N} \| r_{O1P} \| r_{O4N} \| r_{O4P}\right)^{-1}} \tag{3.53}$$

Since $v_{o1}$ and $v_{o2}$ are respectively $G_{m(in)}Z_{out(cm)A}\, v_{ic}$ and $G_{m(in)}Z_{out(cm)B}\, v_{ic}$, one can show that

$$v_{o1} - v_{o2} \cong \left(g_{m1N} + g_{m1P}\right)\Delta R \frac{2}{\left(1+\alpha-2g_{mb1P}\beta R_F\right)^2} v_{ic} \tag{3.54}$$

This differential output voltage behaves indistinguishably from the differential output signal and could propagate to the subsequent stage. From Eq. (3.54), the undesired output voltage can be reduced by increasing $g_{mb1P}\beta R_F$.

In addition to the resistor mismatch, the ratio mismatches in $\alpha$ and $\beta$, as a result of mismatches in $M_{2A(B)}$, $M_{4A(B)}$ and $M_{2A(B)}$, $M_{3A(B)}$, can cause differential output voltage. If these ratio mismatches are assumed to be $\alpha \pm \Delta\alpha$ and $\beta \pm \Delta\beta$, the undesired output voltages can be readily derived as

$$v_{o1} - v_{o2} = \left(g_{m1N} + g_{m1P}\right)\Delta\alpha \frac{R}{2\beta\left(g_{mb1P}R_F\right)^2} v_{ic} \tag{3.55}$$

$$v_{o1} - v_{o2} = \left(g_{m1N} + g_{m1P}\right)\Delta\beta \frac{R}{g_{mb1P}\beta R_F} v_{ic} \tag{3.56}$$

Similarly, these output voltages can be suppressed if $g_{mb1P}\beta R_F$ is large.

### 3.2.2.4 Minimum Supply Voltage and Output Swing

Based on the proposed circuit topology, the minimum supply voltage is determined by

$$V_{DD(\min)} = V_{TH2N} + V_{DSAT2N} + V_{TH2P} + V_{DSAT2P} \tag{3.57}$$

where $V_{TH2N(P)}$ and $V_{DSAT2N(P)}$ are the threshold voltage and saturation voltage of $M_{2NA(B)}$ and $M_{2PA(B)}$, respectively. Obviously, the minimum supply voltage depends heavily

upon the threshold voltage. Therefore, process with low threshold voltage can lead to the CMFB, which can operate at lower supply voltage.

As previously mentioned, the impedances of the input current mirrors at nodes A and B are very small, thus causing both nodes operating as virtual ground. As a result, the output swing of the PDA is limited by the output swing of the input transconductor ($G_{m(in)}$) (see Figure. 3.16) and is determined by

$$V_{DSAT(M_{1NA(B)})} \leq V_{OUT(swing)} \leq V_{DD} - V_{DSAT(M_{1PA(B)})} \tag{3.58}$$

### 3.2.3 Transimpedance-Capacitor ($R_m$-C) Bandpass Filter

To demonstrate the performance of the proposed circuit, a transimpedance-Capacitor ($R_m$-$C$) bandpass filter based on single PDA as illustrated in Figure 3.18(a) [94] is employed. The capacitor $C_{BF}$ is connected in series with the transimpedance amplifer ($R_m$) formed by the proposed PDA and feedback resistor $R_{BF}$. Since the input impedance of the transimpedance amplifier is very low, nodes $E$ and $E'$ can be considered as ac ground. Hence, differentiator can be obtained by cascading $C_{BF}$ before the transimpedance amplifier and the low-frequency transfer function is equal to $sC_{BF}R_{BF}$.

The small-signal equivalent circuit of Figure 3.18(a) is depicted in Figure 3.18(b), where $g_m$ is the transconductance and $C_X$, $C_Y$ and $C_Z$ are the parasitic capacitances determined by

$$g_m = g_{m1N} + g_{m1P} \tag{3.59}$$

$$C_X = C_{GS1N} + C_{GS1P} + C_{GB1N} + C_{GB1P} \tag{3.60}$$

$$C_Y = C_{GD1N} + C_{GD1P} \tag{3.61}$$

$$C_Z = C_{oL} + C_L \tag{3.62}$$

The transfer function of the bandpass filter can be expressed as

$$H(s) = \frac{v_o}{v_i} \cong \frac{sC_{BF}D}{As^2 + Bs + C} \tag{3.63}$$

where

$$A \approx (C_{BF} + C_X)(C_Y + C_Z) + C_Y C_Z \tag{3.64}$$

$$B \approx \frac{g_m C_Y r_{oL} R_{BF} + (C_{BF} + C_X + C_Y) R_{BF} + (C_Y + C_Z) r_{oL}}{r_{oL} R_{BF}} \tag{3.65}$$

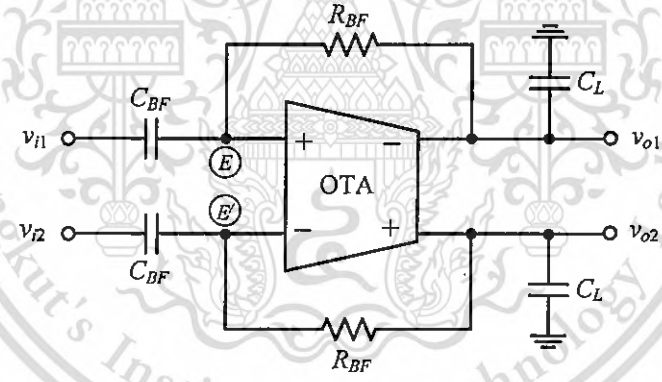
$$C \approx \frac{g_m r_{oL} + 1}{r_{oL} R_{BF}} \tag{3.66}$$

$$D \approx \frac{1 - g_m R_{BF}}{R_{BF}} \tag{3.67}$$

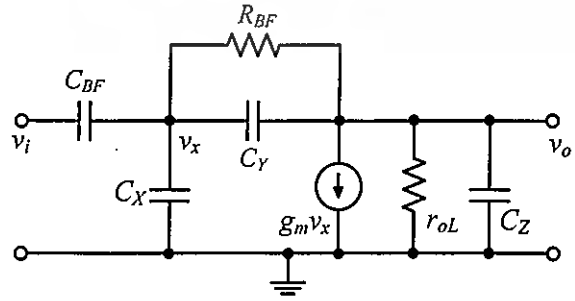
The centre frequency $\omega_o$ and the quality factor $Q$ of the filter can be expressed as

$$\omega_o = \sqrt{\frac{C}{A}} = \sqrt{\frac{g_m r_{oL} + 1}{r_{oL} R_{BF} \left[ (C_{BF} + C_X)(C_Y + C_Z) + C_Y C_Z \right]}} \tag{3.68}$$

$$Q = \sqrt{\frac{AC}{B}} = \sqrt{\frac{\left[ (C_{BF} + C_X)(C_Y + C_Z) + C_Y C_Z \right](g_m r_{oL} + 1)}{g_m C_Y r_{oL} R_{BF} + (C_{BF} + C_X + C_Y) R_{BF} + (C_Y + C_Z) r_{oL}}} \tag{3.69}$$




(a)




(b)

Figure 3.18 (a) Basic structure of $R_m$-$C$ bandpass filter and (b) Simplified small signal equivalent circuit

### 3.2.4 Simulation results

To prove the performance and robustness of the proposed PDA, the circuit has been designed and simulated in a standard 0.18 μm CMOS technology using the Cadence Spectre. The threshold voltages are 0.45 V and -0.5 V for NMOS and PMOS, respectively. The supply voltage is 1 V and the input and output common-mode voltages are biased at $V_{DD}/2$, i.e., 0.5 V. The body bias voltage $V_{BP}$ is set to 0.5 V to reduce the threshold voltage of PMOS transistors. The total current drawn from the supply is 102.5 μA. The bias currents of all transistors are chosen to optimize both gain and power dissipation. Resistors $R_{1,2}$ and the impedance at nodes A and B are 50kΩ and 7kΩ, respectively. The dimensions of transistors are listed in Table 3.2.

Table 3.2 Dimensions of Transistors

| Transistors | $W$ (μm) | $L$ (μm) |
|---|---|---|
| $M_{1NA(B)}$ | 5.2 | 0.5 |
| $M_{1PA(B)}$ | 11 | 0.5 |
| $M_{2NA(B)}$ | 0.8 | 0.24 |
| $M_{2PA(B)}$ | 2.6 | 0.24 |
| $M_{3NA(B)}$ | 4.2 | 0.24 |
| $M_{3PA(B)}$ | 13 | 0.24 |
| $M_{4NA(B)}$ | 1.1 | 0.24 |
| $M_{4PA(B)}$ | 3.5 | 0.24 |
| $M_{5NA(B)}$ | 2.5 | 0.24 |
| $M_{5PA(B)}$ | 7.3 | 0.24 |

Figure 3.19 shows the DC transfer characteristic of the proposed PDA with and without CMFB. The output swing of the PDA demonstrates rail-to-rail operation, while Figure 3.20 shows the transient response of the output voltages, when a CM sinusoidal signal with a peak-to-peak value of 10 $mV_{pp}$ (10 kHz) is applied to the inputs. In case of no CMFB circuit, the CM signal is amplified to 0.6 $V_{pp}$. However, the CM signal decreases to 0.4 $mV_{pp}$, when the CMFB is employed; this leads to a CM attenuation of -15 dB and a *CMRR* of 53 dB. Figure 3.21 shows the open-loop frequency response of the CMFB circuit with stability compensation. The DC open-loop gain is found to be 40 dB, while the unity gain frequency is 70 MHz. The circuit is stable and the phase margin is $50^{\circ}$.

Figure 3.22 shows the frequency response of the PDA when the differential-mode signal is applied to the inputs. The DC gain is 38 dB, while the –3 dB and unity gain frequency are 13.7 MHz and 1.42 GHz (no load $C_L$), respectively. The phase

margin is 86°. Figure 3.23 illustrates the frequency response of the PDA when the common-mode input is applied. The common-mode gain is relatively much smaller (-15 dB), while the bandwidth is almost the same as that of the differential-mode case.

The input referred noise spectral density is shown in Figure 3.24. The input referred noise is less than 16.35nV/√Hz at 10 MHz while integrated noise is 66.93μV(rms) in a range from 1MHz to 20MHz.

Monte Carlo simulations have been performed so as to check how the process variation and device mismatch affect the *CMRR*. A 1000-iteration Monte Carlo analysis is carried out using statistical models provided by the foundry. Figure 3.25 shows the Monte Carlo statistical results of the *CMRR* in the presence of the process variation. The mean value of *CMRR* is 51.8 dB, while the standard deviation is 4.25. The minimum and maximum *CMRRs* are 38 dB and 58 dB, respectively. The maximum number of occurrences is at 52.45 dB. Monte Carlo simulation of the *CMRR* with device mismatches is shown in Figure 3.26. The mean value is 49.3 dB, while the standard deviation is 8.87. The Monte Carlo statistical results give the minimum and maximum *CMRRs* of 35 dB and 69 dB, respectively. The maximum number of occurrences is at 40.3 dB. From Figure 3.25 and 3.26, it is apparent that the device mismatch plays a greater important role than the process variation. Obviously, the use of layout techniques to improve matching becomes mandatory.

Impact of temperature variation on the DC common-mode voltage is also studied and shown in Figure 3.27. The DC common-mode voltage shows small variation (6 %) when temperature is varied from 0°C to 70°C.

Table 3.3 shows the performance comparison with recently published transconductors. It is noted that the proposed transconductor operates with rail-to-rail output swing and at low supply voltage. The circuit proposed in [84] is developed based on CMOS inverter-based amplifier. Since the circuit has no internal node, the circuit can operate at high frequencies. The transconductor proposed in [15] is also based on CMOS inverter. The double CMOS pair is biased in the subthreshold region resulting in low power consumption. Both circuits demonstrate low CMRR mainly due to their low loop gains.

This work is based on the CMOS inverter-based PDA and novel current mode CMFB, allowing the circuit to operate at higher frequencies, yet maintain relatively large CMRR. Table 3.3 also shows the results obtained from theoretical equations and they are in good agreement with those obtained from the simulations.

Figure 3.28 shows the frequency response of the $R_m$-$C$ bandpass filter ($C_{BF}$ = 0.25 pF, $C_L$ = 0.5 pF and $R_{BF}$ = 50 kΩ). The centre frequency $f_o$ and quality factor $Q$ are

31.62 MHz and 1.66, respectively. Figure 3.29 shows the variation of the center frequency for various values of $R_{BF}$ and $C_L$ ($R_{BF}$ = 30 kΩ–120 kΩ, $C_L$ = 0.5 pF and $C_L$ = 0.3 pF–2.1 pF, $R_{BF}$ = 50 kΩ). The power dissipation of the proposed PDA and its application are 102.5 μW.

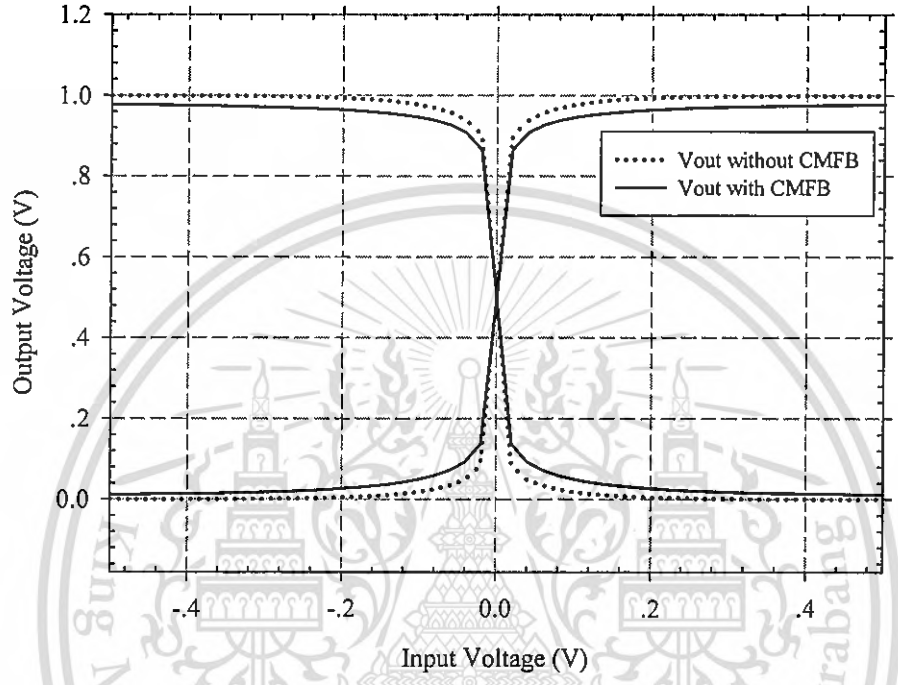



Figure 3.19 DC transfer characteristic

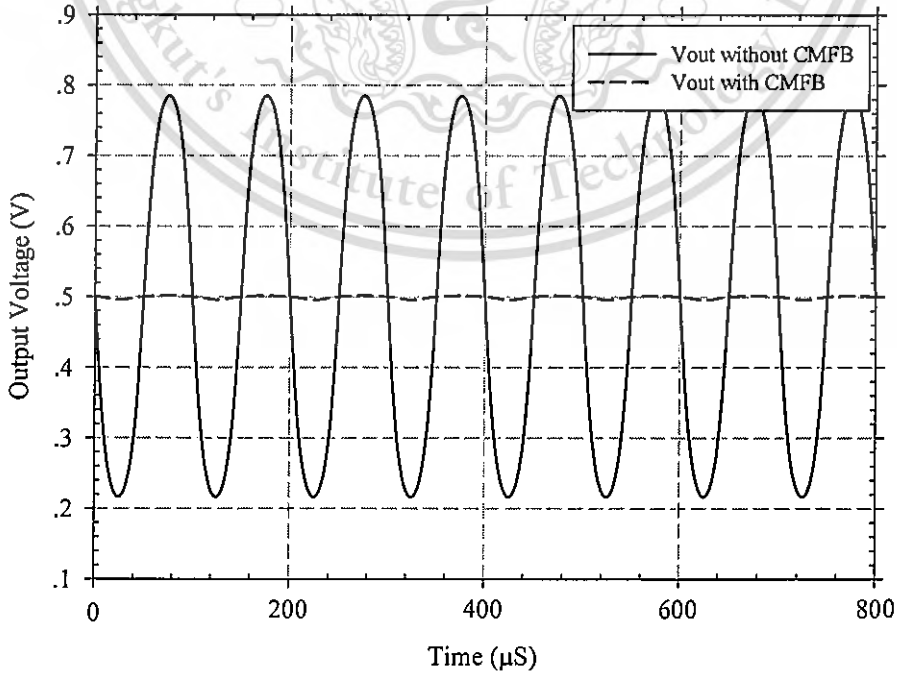



Figure 3.20 Output voltages with and without CMFB

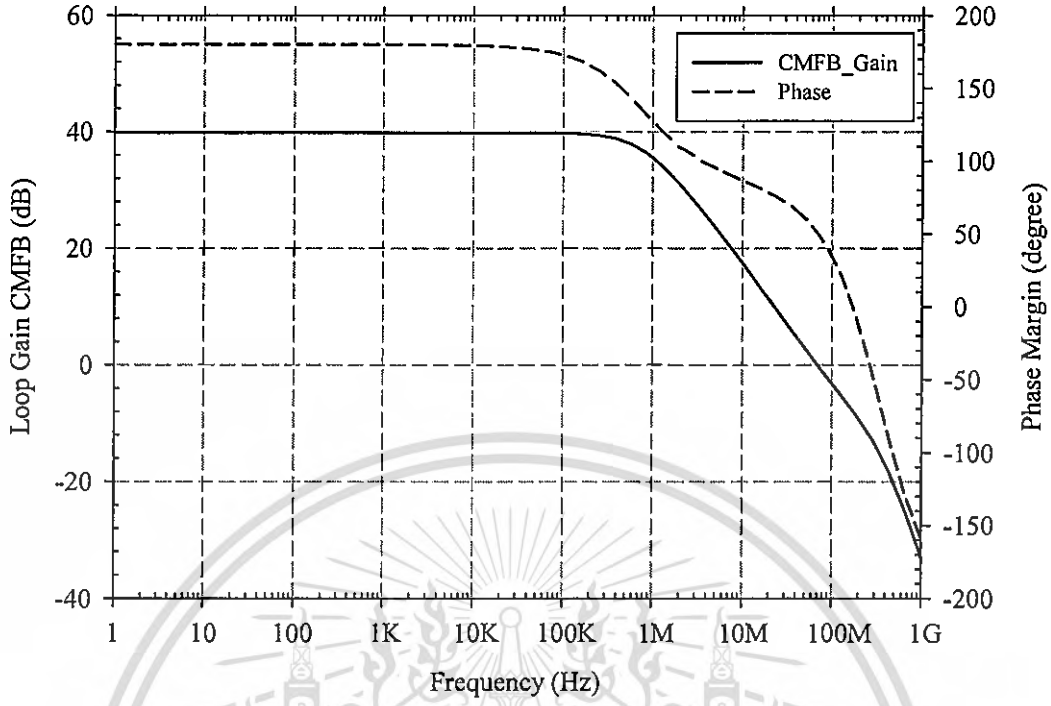



Figure 3.21 Open-loop frequency response of the CMFB circuit

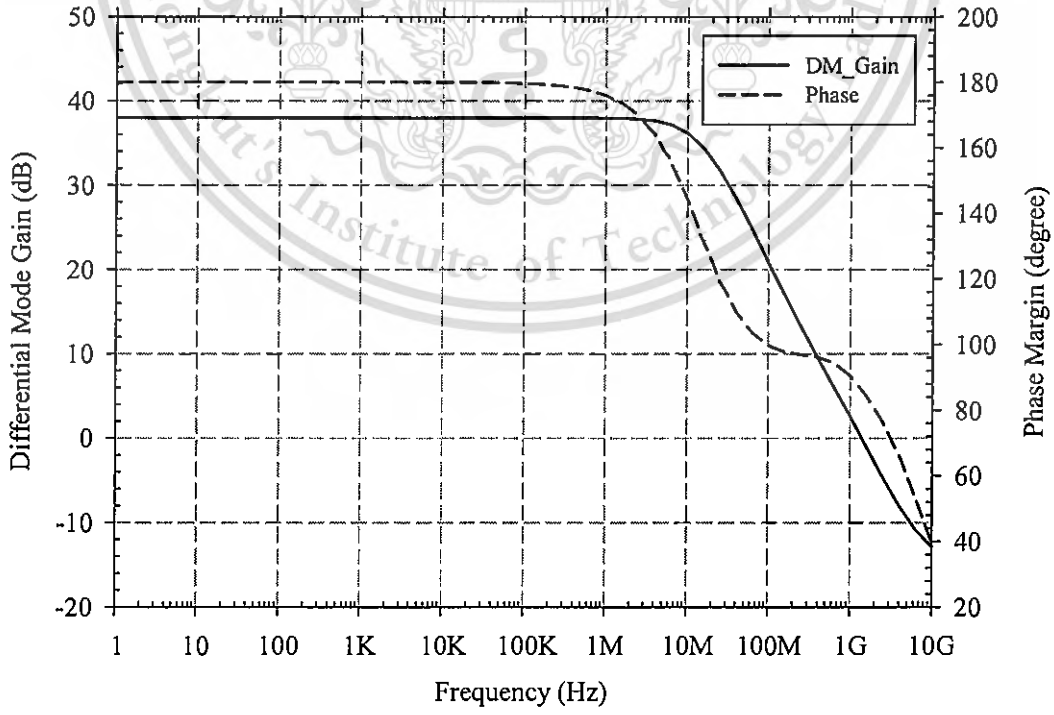



Figure 3.22 Differential-mode gain and phase

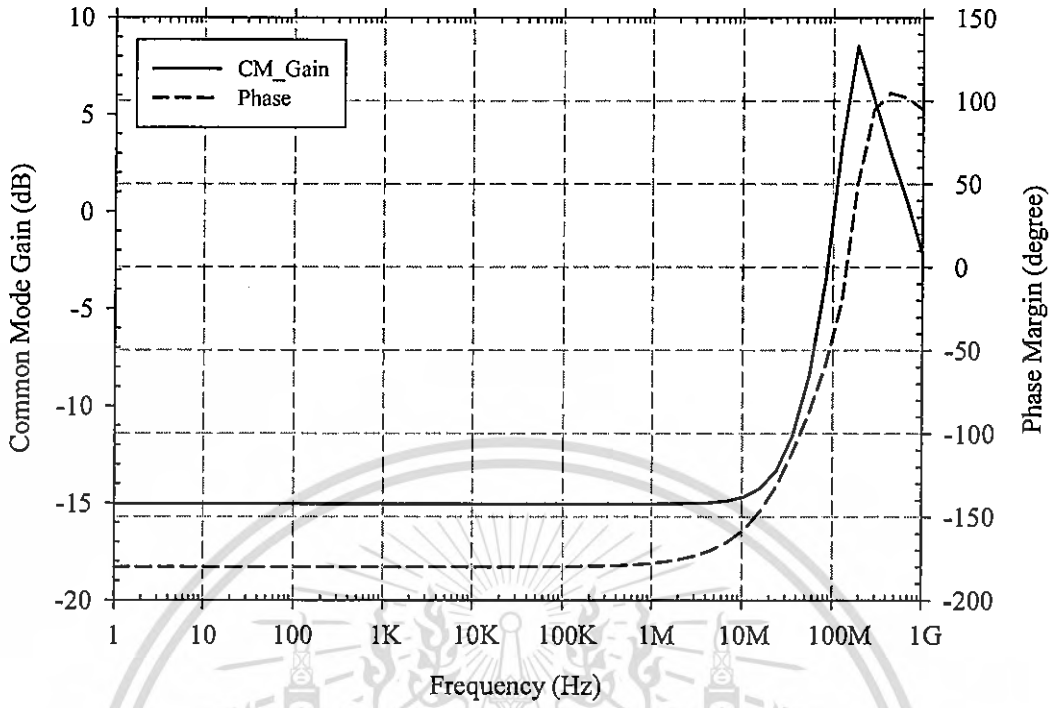



Figure 3.23 Common-mode gain and phase

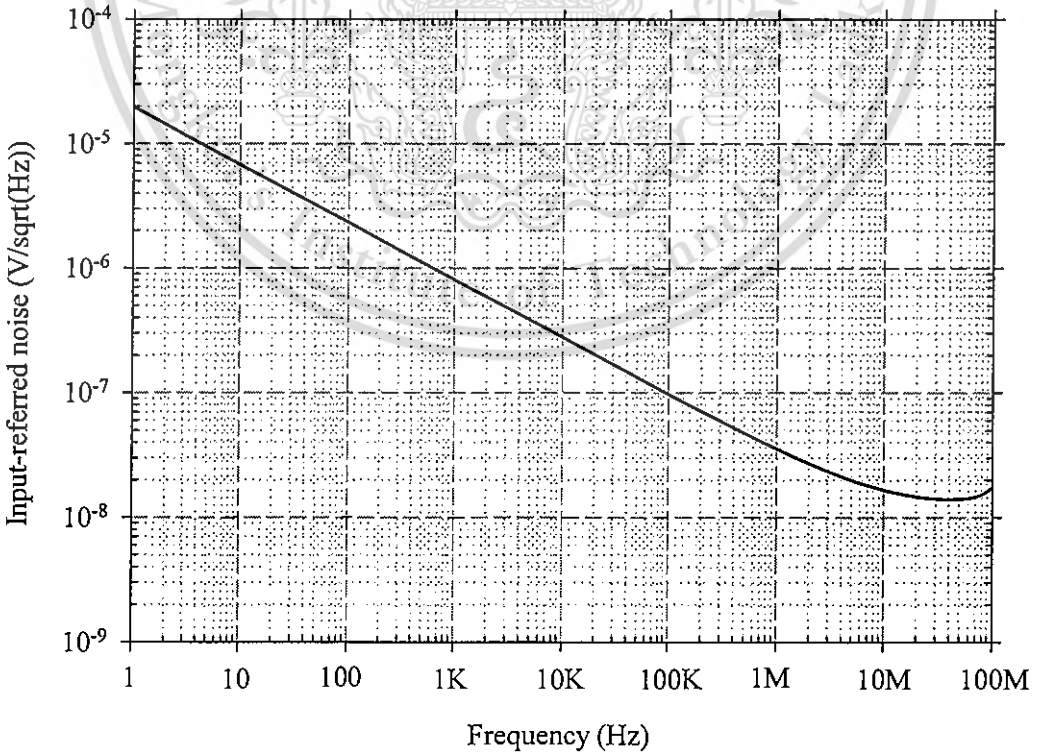



Figure 3.24 PDA input-referred noise

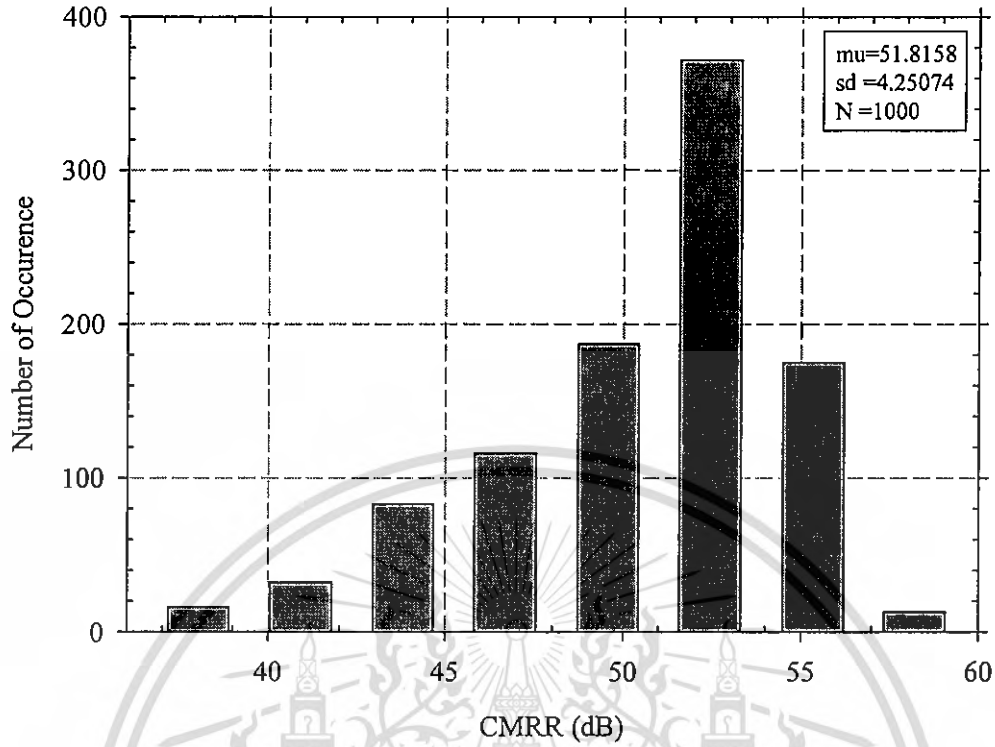



Figure 3.25 Monte Carlo simulation results for *CMRR* with process variation (1000 runs)

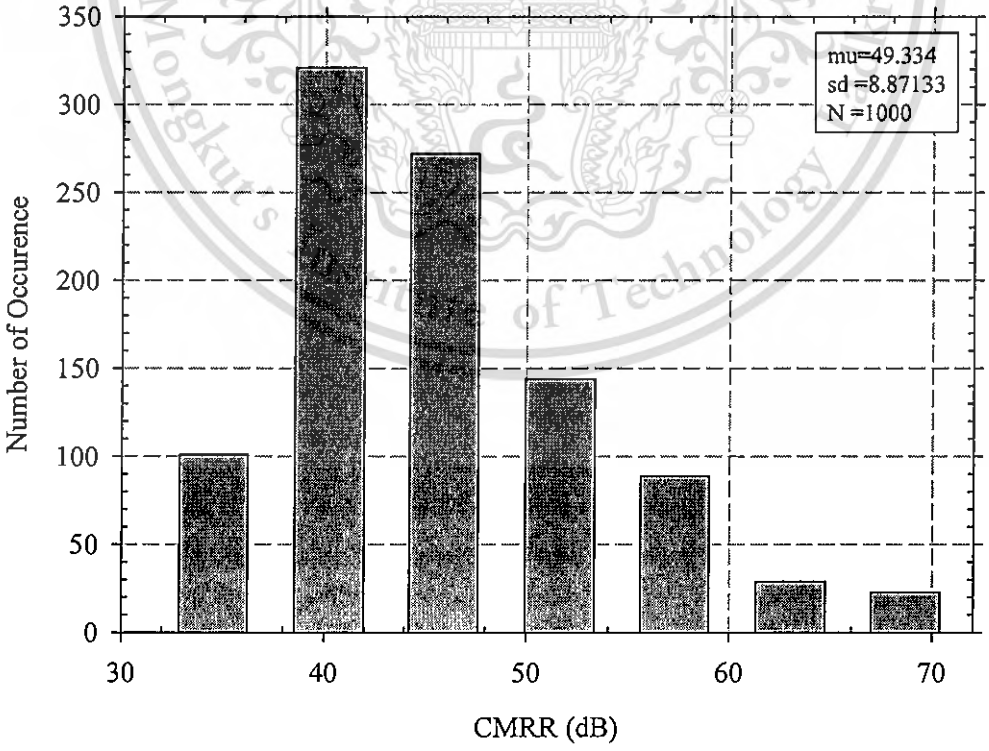



Figure 3.26 Monte Carlo simulation results for *CMRR* with mismatch (1000 runs)

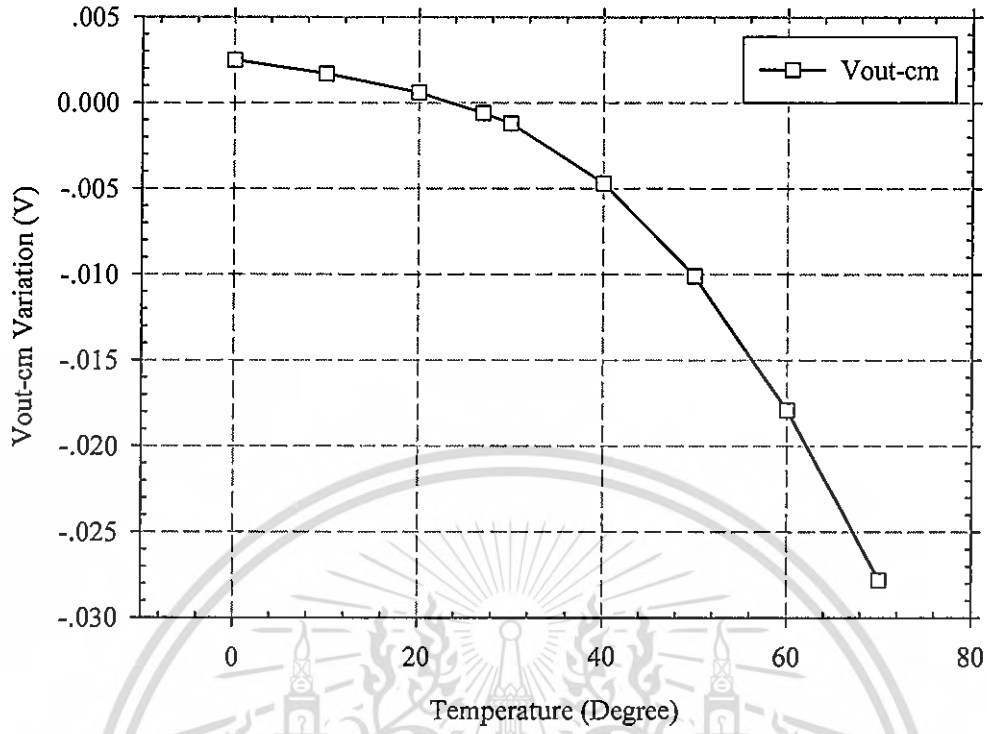



Figure 3.27 DC common-mode voltage variation with temperature

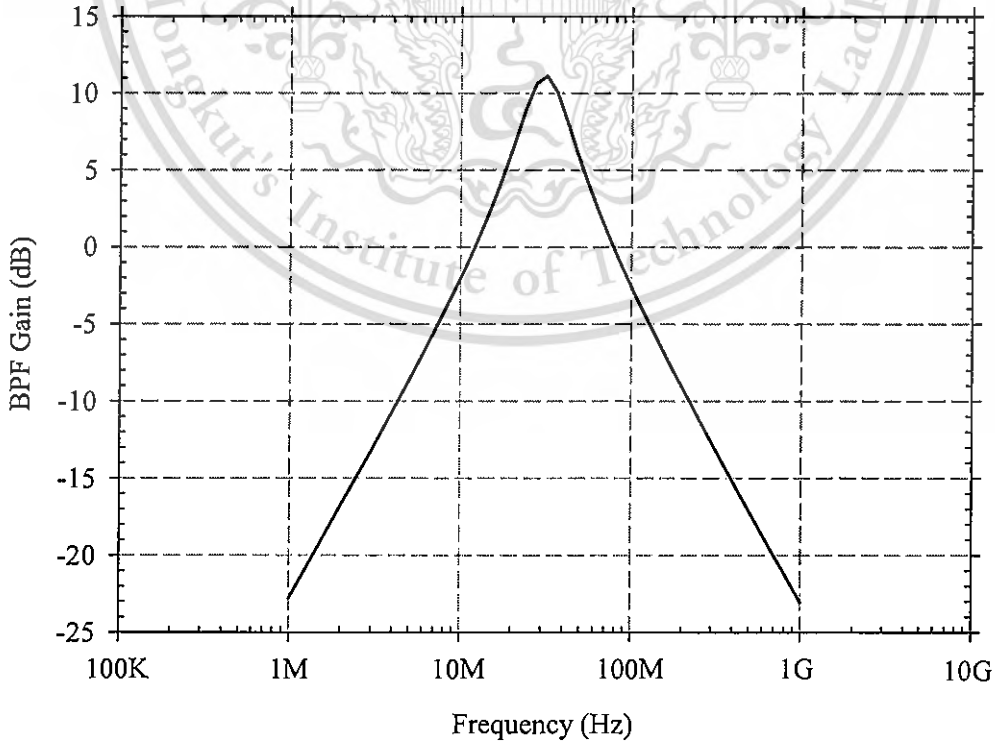



Figure 3.28 Frequency responses of the simple $R_m$-$C$ bandpass filter

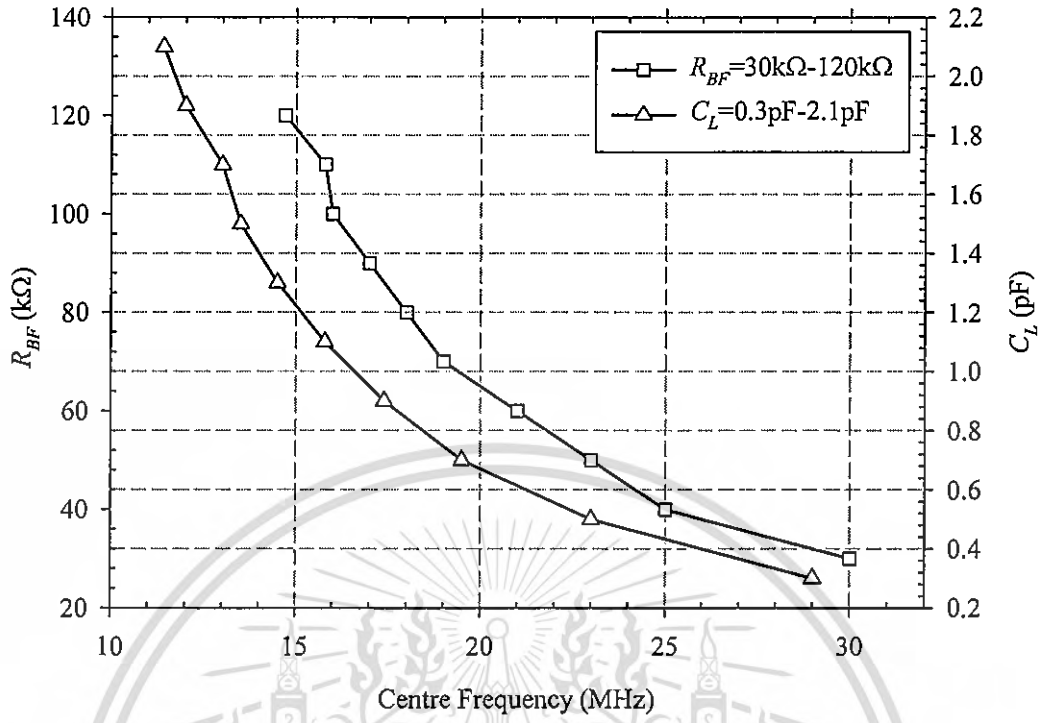



Figure 3.29 Center frequency as a function of $R_{BF}$ and $C_L$

Table 3.3 Performance evaluation

| Parameters | [15] | [84] | This work |
|---|---|---|---|
| Technology | 0.35μm | 0.35μm | 0.18μm |
| Supply voltage | 3.3V | 2.5V | 1V |
| DC gain | 29.3dB | 31.3dB | 38dB |
| Phase margin | 82.8° | 77° | 86° |
| GBW (no load $C_L$) | 28.97MHz | 3.56GHz | 1.42GHz |
| CMRR | 35.19dB | 31dB | 53dB |
| Maximum Output Swing | 0.88 V | 2.27 V | 0.72 V |
| Linearity | THD=-40dB @0.3Vp-p | THD=-46dB @1Vp-p | THD=-40dB @0.5Vp-p |
| Transconductance | 49.6nS-12.5μS | 108.4μS | 305μS |
| Input referred noise | 113nV/√Hz | 85nV/√Hz | 16.35nV/√Hz |
| Power dissipation | 44.53μW | 800μW | 102.5μW |

## 3.3 Conclusions

In this chapter, The first CMOS pseudo differential amplifier (PDA) using current-mode common-mode feedback (CMFB) circuit with rail-to-rail operation is explained. The CMFB converts the output voltage signals into currents, which is then applied to two current mirrors, operating as a common-mode detector. The current amplifier is used to enhance the loop gain, resulting in minimized gain error. The positive feedback is also employed to enhance the differential gain of the system. The advancetage of the proposed CMFB shows low common-mode gain and rail-to-rail capability.

The second circuit presents the design of a CMOS inverter-based class-AB pseudo differential amplifier (PDA) using current-mode common-mode feedback (CMFB). The circuit is designed based on a CMOS inverter and low-voltage wide-swing CMFB circuit. The proposed PDA demonstrates rail-to-rail operation. The simulation results show that the circuit can operate at low supply voltage with high differential and low common-mode gains. The unity gain frequency is quite high and the power dissipation is relatively low.

# CHAPTER 4

# A 0.5 V BULK-DRIVEN QUASI-FLOATING-GATE PSEUDO-DIFFERENTIAL AMPLIFIER USING FEEDFORWARD TECHNIQUES AND ITS APPLICATION

In this chapter, a low voltage pseudo-differential amplifiers (PDA) using bulk-driven (BD) and quasi-floating gate (QFG) technique is presented. Section 4.1 presents the basic structure of a bulk-driven pseudo-differential amplifier (BD-PDA) and the proposed PDA that uses a simple feed-forward network to boost and suppress differential-mode and common-mode gains. An output stage using feedback amplifier (FBA) is also proposed to enhance the pseudo-differential amplifier's output impedance and set its DC common-mode voltage. In addition, an improved version of the PDA incorporating a gain-enhancement network (GEN) to increase effective input transconductance, yet maintaining the same power dissipation, is also presented. The improved version has an increased open loop gain and lower input referred noise. The PDAs can operate at rail-to-rail input and output signal swings with a supply voltage close to the transistor's threshold voltage. Section 4.2 provides the performance analysis of the proposed PDA consisting of frequency response, noise analysis, and minimum supply voltage and output swing. Section 4.3 presents an application of the proposed BD-PDA as a multiple-feedback (MFB) filter. Section 4.4 demonstrates the simulation results and Section 4.5 concludes the research.

## 4.1 Proposed BD-QFG Pseudo Differential Amplifier

### 4.1.1 Conventional BD-PDA Topology

Figure 4.1 a) depicts the structure of a conventional pseudo-differential Amplifier (PDA). As can be seen, the PDA consists of two matched transconductors ($G_{miA}$ and $G_{miB}$). $Z_{outA}$ and $Z_{outB}$ represent the output impedances of the input transconductors A and B, respectively. The operation of the PDA is simple and can be explained as follows. When input voltage signals ($v_{i1}$ and $v_{i2}$) are applied, the signals are converted to output current signals via the input transconductors ($G_{miA}$

and $G_{miB}$). The output voltages ($v_{o1}$ and $v_{o2}$) are then equal to the output currents multiplied by the output impedances.

Figure 4.1 b) shows a basic low-voltage bulk-driven pseudo-differential amplifier. Its circuit is composed of two bulk-driven PMOS transistors ($M_{1P}$ and $M_{2P}$) and two current sources ($M_{1N}$ and $M_{2N}$). One can think of transistors $M_{1P}$ and $M_{1N}$ as operating as the input transconductor $G_{miA}$ while $M_{2P}$ and $M_{2N}$ as operating as the input transconductor $G_{miB}$. It should be noted that, for a conventional gate-driven MOSFET, input voltage signal is applied to the gate and therefore it has to be greater than the threshold voltage. However, this constraints is removed in bulk-driven MOSFET since its input voltage signal is applied to the bulk terminal, eliminating threshold voltage from the signal path. As a result, wide-voltage swing at the input is obtainable provided that the forward bias of the parasitic p-n junctions inside $M_{1P}$ and $M_{2P}$ is kept low.

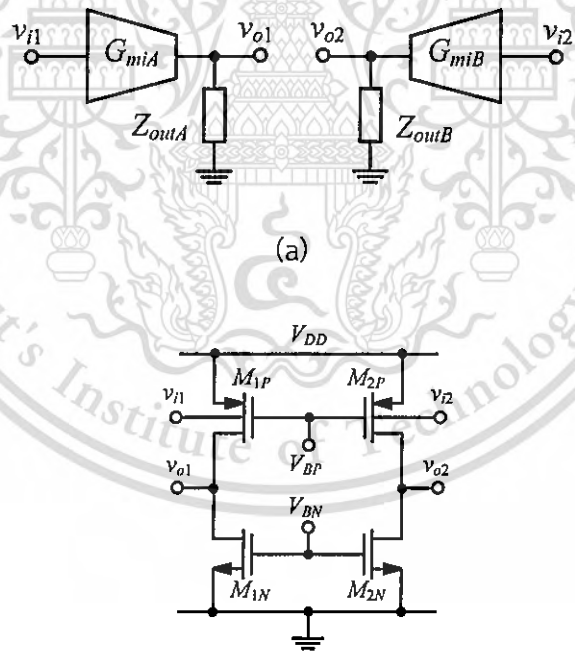



Figure 4.1 a) Basic structure of pseudo-differential amplifier and b) bulk-driven PDA

Derived from the schematic in Figure 4.1, the expressions for differential-mode ($G_{dm}$) and common-mode transconductances ($G_{cm}$) are

$$G_{dm} = G_{cm} = g_{mb1P(2P)} \tag{4.1}$$

where $g_{mb1P(2P)}$ is the bulk transconductance of $M_{1P(2P)}$.

According to Eq. (4.1), $G_{dm}$ is the same as $G_{cm}$. As a result, PDA with large $G_{dm}$ unavoidably has large $G_{cm}$ as well. Since large $G_{cm}$ makes a circuit susceptible to interference and supply noise, a good technique for reducing $G_{cm}$ is needed.

### 4.1.2 BD-PDA with Feed-Forward Structure

Figure 4.2 illustrates the proposed structure of a feed-forward PDA. As seen, a feed-forward amplifier (FFA) has been added to the PDA. The FFA consists of two matched inverting amplifiers, that have a voltage gain of $-\alpha$, and two matched feed-forward transconductors ($G_{mffA}$ and $G_{mffB}$). The FFA is used to serve two purposes: reduce the common-mode transconductance ($G_{cm}$) and raise the differential transconductance ($G_{dm}$).

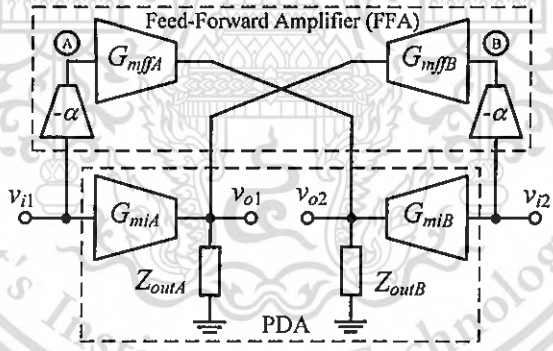



Figure 4.2 PDA and feed-forward amplifier (FFA)

The operation of the proposed amplifier can be explained as follows. Let us first consider the common-mode input signals (i.e., $v_{i1(2)}=v_{icm}$). The input signals are first converted to currents via the input transconductors $G_{miA}$ and $G_{miB}$. The signals are also amplified at a voltage gain of $-\alpha$. The amplified signals ($v_A$ and $v_B$) are then converted to currents by the feedforward transconductors ($G_{mffA}$ and $G_{mffB}$). These currents are then fed forward to the output of the input transconductor $G_{miB}$ and $G_{miA}$, respectively. Since the output currents of $G_{miA}$ and $G_{miB}$ and the output currents of $G_{mffA}$ and $G_{mffB}$ have an opposite phase, the total output currents combine destructively, and thus the common-mode transcoductance ($G_{cm}$) is suppressed.

However, if the input signals are differential ($v_{i1}=-v_{i2}$), the output currents of $G_{miA}$ and $G_{miB}$ and the output currents of $G_{mffA}$ and $G_{mffB}$ are in phase, thus the differential-mode output currents and the differential transconductance ($G_{dm}$) are boosted.

$G_{dm}$ and $G_{cm}$ are derived and shown below.

$$G_{dm} = G_{miA(B)} + \alpha \cdot G_{mffA(B)} \tag{4.2}$$

$$G_{cm} = G_{miA(B)} - \alpha \cdot G_{mffA(B)} \tag{4.3}$$

According to Eqs. (4.2) and (4.3), if $\alpha$ is set to $G_{miA(B)}/G_{mffA(B)}$, $G_{dm}$ and $G_{cm}$ become $2G_{miA(B)}$ and zero, respectively. Obviously, the proposed FFA can boost $G_{dm}$ and at the same time suppress $G_{cm}$.

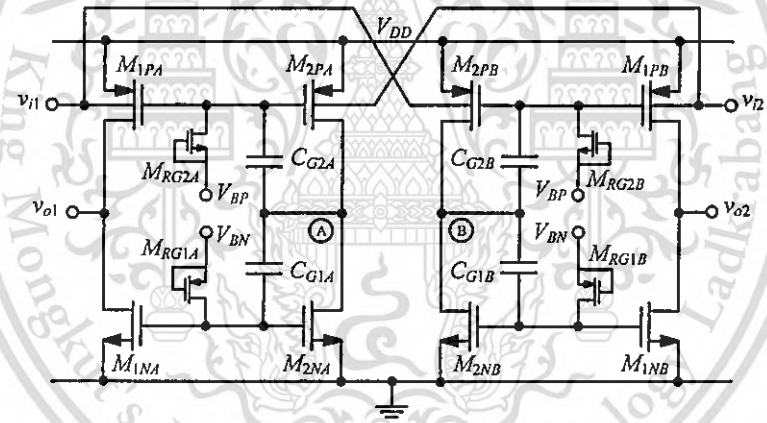



Figure 4.3 Transistor-level implementation

Figure 4.3 illustrates a transistor-level implementation of the proposed PDA. Transistors $M_{1PA}$ and $M_{1PB}$ make up the two matched input transconductors (i.e., $G_{miA}$ and $G_{miB}$). Transistors $M_{P2A}$ and $M_{P2B}$ make up the amplifiers that have the voltage gain of $-\alpha$. The amplified signals ($v_A$ and $v_B$) are converted to currents by the feedforward transconductors $G_{mffA}$ and $G_{mffB}$ which are made up from $M_{1NA-1PB}$ and $M_{1PA-1PB}$. It should be noted here that $M_{1PA-1PB}$ makes up both the input transconductor and the feedforward transconductors. This efficient design simplifies and compacts the circuit. Moreover, the loading effect and power dissipation are minimized.

As can be seen, quasi-floating gate (QFG) transistors are used so that the circuit can operate from a supply equal to threshold voltage. Their gate voltages are set to one of the supply rails (i.e., $V_{DD}$ and $G_{ND}$) via very large resistors which are implemented using transistors (i.e., $M_{RG1A,B}$ and $M_{RG2A,B}$) operating in the cutoff region. Signals inside the circuit are coupled through the gate via capacitors and large resistors hence making the gate terminals behaving as the floating terminals for the signal frequencies as small as a few hertz up to gigahertz range [36].

Derived from the schematics in Figure 4.2 and Figure 4.3, $G_{miA}$, $G_{miB}$ and $\alpha$ can be expressed as

$$G_{miA(B)} = g_{mb1PA(B)} \tag{4.4}$$

$$G_{mffA(B)} = g_{m1NA(B)} + g_{m1PA(B)} \tag{4.5}$$

$$\alpha = \frac{g_{mb2PA(B)}}{g_{m2NA(B)} + g_{m2PA(B)}} \tag{4.6}$$

By substituting Eqs. (4.4)-(4.6) into Eqs. (4.2) and (4.3), $G_{dm}$ and $G_{cm}$ can be expressed as

$$G_{dm} = g_{mb1A(B)P} + \frac{g_{mb2PA(B)}}{g_{m2NA(B)} + g_{m2PA(B)}}\left(g_{m1NA(B)} + g_{m1PA(B)}\right) \tag{4.7}$$

$$G_{cm} = g_{mb1A(B)P} - \frac{g_{mb2PA(B)}}{g_{m2NA(B)} + g_{m2PA(B)}}\left(g_{m1NA(B)} + g_{m1PA(B)}\right) \tag{4.8}$$

According to Eqs. (4.7) and (4.8), if the gate and bulk transconductances of $M_{1(2)NA(B)}$, and $M_{1(2)PA(B)}$ are set such that $g_{m1NA(B)}+g_{m1PA(B)} = g_{m2NA(B)}+g_{m2PA(B)}$ and $g_{mb1PA(B)} = g_{mb2PA(B)}$, $G_{dm}$ and $G_{cm}$ will be $2g_{mb1A(B)P}$ and zero, respectively.

### 4.1.3 Improved BD-QFG PDA with Gain-Enhancement Network (GEN)

The proposed PDA in the previous section has three main drawbacks: (1) the PDA still has a low effective input transconductance (i.e., $G_{md} \approx 2g_{mb1A(B)P}$) which leads to a small differential-mode gain, (2) the output impedance is low (i.e., $R_{out} \approx r_{o1NA(B)} \| r_{o1PA(B)}$) especially for modern deep submicron MOSFETs and (3) the output

common-mode voltage is undetermined. This section presents a method for solving the aforementioned problems.

The transcondutance of the feed-forward PDA as previously described is enhanced by incorporating a gain-enhancement network (GEN) as depicted in Figure 4.4 The topology is similar to Figure 4.2 except that the gain-enhancement network (GEN), which are made up of cross-coupled transconductors $G_{mf3A)}$ and $G_{mf3B}$, is augmented at nodes A and B. The purpose of the GEN is to enhance the impedances at nodes A and B via a partial positive feedback mechanism, thus the differential voltages at nodes A and B are boosted. Transcoductors $G_{mf1A(B)}$ and $G_{mf2A(B)}$ operate as the inverting amplifier that has the voltage gain of $-\alpha$.

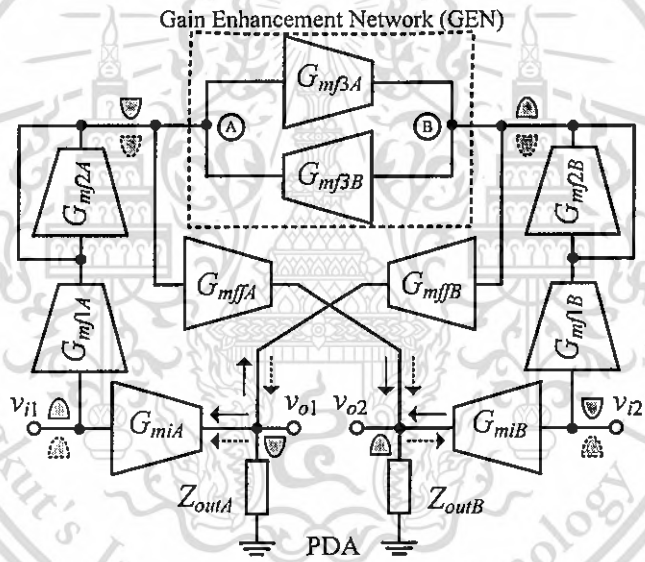



Figure 4.4 Gain Enhancement PDA

The circuit operation can be explained as follows. Let us assume that the input voltages are differential signals (i.e., $v_{i1} = -v_{i2} = v_i$) (see solid line). The input voltages are converted into currents through $G_{miA}$ and $G_{miB}$, and also converted into currents through $G_{mf1A}$ and $G_{mf1B}$ which lead to a large decrease and increase of the voltages at the high impedance nodes A and B, respectively. The voltages at nodes A and B are then converted into large currents through $G_{mffA}$ and $G_{mffB}$ which are finally combined constructively with the currents from $G_{miA}$ and $G_{miB}$.

However, if the input signals are common ($v_{i1}=-v_{i2}$), the impedances at nodes A and B are relatively much smaller than that of the differential-mode case. The

output currents of $G_{miA}$ and $G_{miB}$ and the output currents of $G_{mffA}$ and $G_{mffB}$ are out of phase, thus the common-mode output currents and common-mode transconductance ($G_{cm}$) are suppressed. This property of the PDA that is able to generate large differential-mode and small common-mode output currents allows the proposed topology to have a large common-mode rejection ratio (CMRR).

The differential-mode ($G_{dm}$) and common-mode ($G_{cm}$) transconductances can be derived as shown below.

$$G_{dm} = G_{miA(B)} + \frac{G_{mf1A(B)}}{G_{mf2A(B)} - G_{mf3A(B)}} \cdot G_{mffA(B)} \tag{4.9}$$

$$G_{cm} = G_{miA(B)} - \frac{G_{mf1fA(B)}}{G_{mf2A(B)} + G_{mf3A(B)}} \cdot G_{mffA(B)} \tag{4.10}$$

In comparing Eqs. (4.2) to (4.9), the expressions of $G_{dm}$ are similar. The only difference lies in the second term where the multiplication factor of $G_{mffA(B)}$ in Eq. (4.9) is $G_{mf1A(B)}/(G_{mf2A(B)}-G_{mf3A(B)})$. Large $G_{dm}$ is realizable by designing $G_{mf2A(B)}$ to be slightly larger than $G_{mf3A(B)}$. It is also noticed that small $G_{cm}$ in Eq. (4.10) is also realizable by properly choosing $G_{mf1A(B)}$, $G_{mf2A(B)}$ and $G_{mf3A(B)}$. Since a condition of having large $G_{dm}$ and small $G_{cm}$ can be satisfied simultaneously, a large common-mode rejection ratio (CMRR) can be readily achieved.

A transistor-level implementation of the topology in Figure 4.4 is illustrated in Figure 4.5 Transistors $M_{1PA}$ and $M_{1PB}$ implement the two matched input transconductors $G_{miA}$ and $G_{miB}$. $M_{1PA}$ and $M_{1PB}$ together with $M_{1NA}$ and $M_{1NB}$ implement the feed-forward transconductors $G_{mffA}$ and $G_{mffB}$. A cross-coupled transistor pair $M_{2NA}$ and $M_{2NB}$ make up the gain-enhancement network (GEN). $M_{sub}$, which operates as an adjustable resistor via a control voltage $V_C$, and $R_{AB}$ ensure that the impedances at nodes A and B are positive and large. $M_{P2A}$ and $M_{P2B}$ implement the transconductors $G_{mf1A}$ and $G_{mf1B}$ and, at the same time, $G_{mf2A}$ and $G_{mf2B}$, respectively. This efficient design, in which $M_{1PA(B)}$ implements $G_{miA(B)}$ and part of $G_{mffA(B)}$ while $M_{P2A(B)}$ implement both $G_{mf1A(B)}$ and $G_{mf2A(B)}$, simplifies and compacts the circuit. Moreover, the loading effect and power dissipation are minimized.

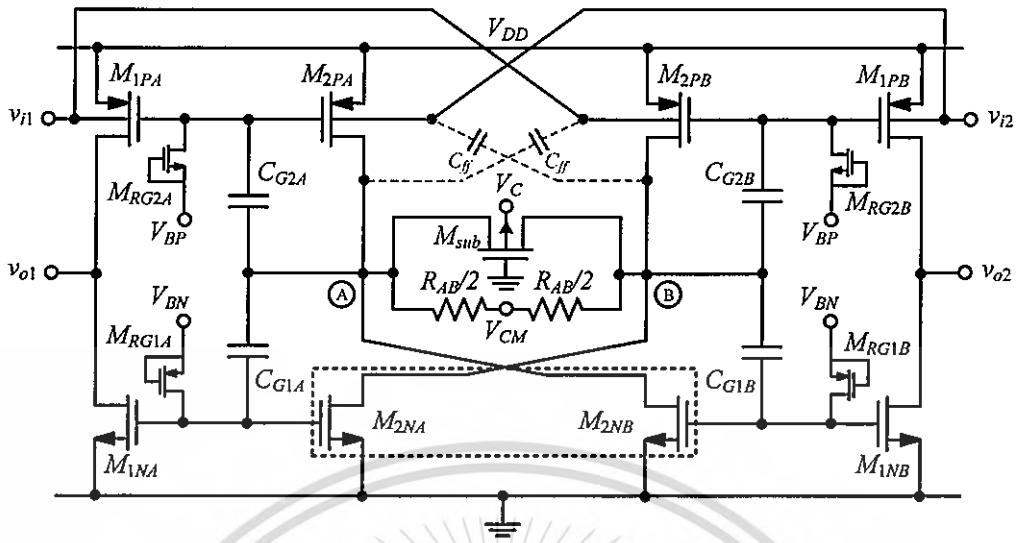



Figure 4.5 Transistor-level implementation

Derived from the schematics in Figure 4.4 and Figure 4.5, the transconductances $G_{miA}$, $G_{miB}$, $G_{mf1A(B)}$, $G_{mf2A(B)}$, and $G_{mf3A(B)}$ and $G_{mffA(B)}$, can be expressed as

$$G_{miA(B)} = g_{mb1PA(B)} \tag{4.11}$$

$$G_{mf1A(B)} = g_{mb2PA(B)} \tag{4.12}$$

$$G_{mf2A(B)} = g_{m2PA(B)} \tag{4.13}$$

$$G_{mf3A(B)} = g_{m2NA(B)} \tag{4.14}$$

$$G_{mffA(B)} = g_{m1PA(B)} + g_{m1NA(B)} \tag{4.15}$$

By substituting Eqs. (4.11)-(4.15) into Eqs. (4.9) and (4.10), $G_{dm}$ and $G_{cm}$ can be expressed as

$$G_{dm} = g_{mb1PA(B)} + \frac{g_{mb2PA(B)}}{g_{m2PA(B)} - g_{m2NA(B)} + 2\left(R_{AB} \parallel R_{sub}\right)^{-1}}\left(g_{m1PA(B)} + g_{m1NA(B)}\right). \tag{4.16}$$

$$G_{cm} = g_{mb1PA(B)} - \frac{g_{mb2PA(B)}}{g_{m2PA(B)} + g_{m2NA(B)}}\left(g_{m1PA(B)} + g_{m1NA(B)}\right) \tag{4.17}$$

According to Eqs. (4.16) and (4.17), if $g_{m2PA(B)}-g_{m2NA(B)} = -2(R_{AB}||R_{sub})^{-1}$ and $g_{m1PA(B)}+g_{m1NA(B)} = g_{m2PA(B)}+g_{m2NA(B)}$, the differential-mode and common-mode transconductances become very large and zero respectively. Practically, $g_{m2NA(B)}-g_{m2PA(B)}$ should be designed to be smaller than $2(R_{AB}||R_{sub})^{-1}$ so that the stability of the PDA is maintained. This condition can be satisfied by properly choosing $R_{AB}$, $V_C$ and dimensions of $M_{2PA,B}$ and $M_{2NA,B}$. Note that a bias voltage $V_{CM}$ is used to set the DC voltages at high resistance nodes A and B.

### 4.1.4 Output Impedance Enhancement and Common-Mode Voltage Setup

Output impedance enhancement and common-mode voltage setup can be achieved by connecting an output stage as depicted in Figure 4.6 to the PDA. The output stage is configured in both positive and negative feedbacks. The positive feedback uses cross-coupled transistors $M_{4PA}$ and $M_{4PB}$ to enhance the output impedance and thus the open-loop gain. In addition, the negative feedback configuration implemented by $M_{3PA,B}$ and $R_C$ is used to set the common-mode voltage. As can be seen, the output stage is simple since there is no need for a complicated common-mode detector as conventionally done in most CMFB circuits.

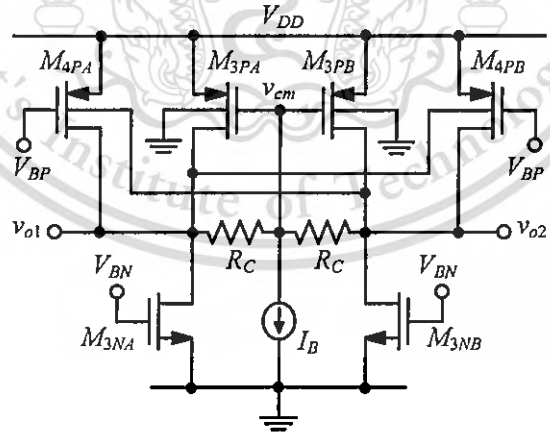



Figure 4.6 Output stage

The differential-mode ($Z_{out(dm)}$) and common-mode ($Z_{out(cm)}$) output impedances can be determined by analyzing the small signal equivalent circuits of the output stage and shown as below.

$$Z_{out(dm)} = \frac{1}{\left(R_O \parallel R_C\right)^{-1} - g_{mb4PA(B)}} \tag{4.18}$$

$$Z_{out(cm)} = \frac{1}{R_O^{-1} + g_{m3PA(B)} + g_{mb4PA(B)}} \tag{4.19}$$

where $R_O$ is $r_{O1PA(B)} \| r_{O1NA(B)} \| r_{O3PA(B)} \| r_{O4PA(B)} \| r_{O3NA(B)}$.

According to Eqs. (4.18)-(4.19), $Z_{out(dm)}$ can become large if $R_O \| R_C$ is set to be slightly larger than $g_{mb4PA(B)}$.

By setting the drain current of $M_{4PA,B}$ equal to that of $M_{3NA,B}$, a common-mode voltage ($V_{out(cm)}$) can be determined as

$$V_{out(cm)} = V_{DD} - \left|V_{TP3}\right| - \sqrt{\frac{I_B}{\mu_p C_{ox}\left(W/L\right)_{3PA(B)}}} + R_C I_B \tag{4.20}$$

where $V_{TP3}$ is the threshold voltage of $M_{3PA(B)}$.

Practically, $V_{out(cm)}$ should be set equal to $V_{DD}/2$ for a maximum output swing, From Eqs. (4.16)-(4.17) and Eqs. (4.18)-(4.19), $A_{dm}$ and $A_{cm}$ can be derived as

$$A_{dm} = \left[ g_{mb1PA(B)} + \frac{g_{mb2PA(B)}}{g_{m2PA(B)} - g_{m2NA(B)} + 2\left(R_{AB} \parallel R_{sub}\right)^{-1}} \left(g_{m1PA(B)} + g_{m1NA(B)}\right) \right] \left( \frac{1}{\left(R_O \parallel R_C\right)^{-1} - g_{mb4PA(B)}} \right) \tag{4.21}$$

$$A_{cm} = \left[ g_{mb1PA(B)} - \frac{g_{mb2PA(B)}}{g_{m2PA(B)} + g_{m2NA(B)}} \left(g_{m1PA(B)} + g_{m1NA(B)}\right) \right] \left( \frac{1}{R_O^{-1} + g_{m3PA(B)} + g_{mb4PA(B)}} \right) \tag{4.22}$$

The common-mode rejection ratio (*CMRR*) can be derived as

$$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right|$$

$$= \left[ \frac{g_{mb1PA(B)} + \frac{g_{mb2PA(B)}}{g_{m2PA(B)} - g_{m2NA(B)} + 2\left(R_{AB} \parallel R_{sub}\right)^{-1}} \left(g_{m1PA(B)} + g_{m1NA(B)}\right)}{g_{mb1PA(B)} - \frac{g_{mb2PA(B)}}{g_{m2PA(B)} + g_{m2NA(B)}} \left(g_{m1PA(B)} + g_{m1NA(B)}\right)} \right] \left[ \frac{R_O^{-1} + g_{m3PA(B)} + g_{mb4PA(B)}}{\left(R_O \parallel R_C\right)^{-1} - g_{mb4PA(B)}} \right] \tag{4.23}$$

## 4.2 Performance Analysis

### 4.2.1 Frequency Response

The frequency response of the circuit can be analyzed from the small-signal equivalent circuits of Figs. 4.5 and 4.6, which is depicted in Figure 4.7 where $C_{A(B)}$ and $C_{outA(B)}$ are the total parasitic capacitance at node A(B) and output node respectively, their capacitance given by $C_{A(B)} = C_{gsn1} + C_{gsp1} + C_{gsn2} + C_{gsp2} + C_{dbn2}$ and $C_{outA(B)} = C_{dbn1} + C_{gdn1} + C_{gdp1} + C_{dbn3} + C_{dbp3} + C_{gdn3} + C_{gdp3} + C_{gdp4} + C_L$.

The frequency compensation is accomplished by incorporating two feed-forward capacitors $C_{ff}$ at the nodes A and B which act like a short circuit at high frequency.

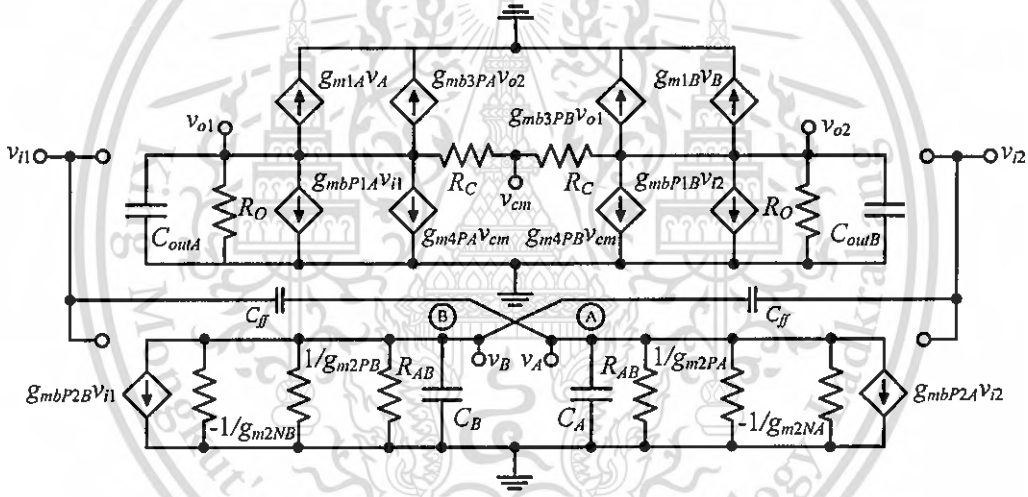



Figure 4.7 Small signal equivalent circuits of Figure. 4.5 and 4.6

By using typical circuit analysis, the open-loop gain of the PDA can be derived as below.

$$A_{dm}(s) = \frac{A_{dm}\left(1+\frac{s}{\omega_{Z1}}\right)}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)} \tag{4.24}$$

where $A_{dm}$ is the low-frequency gain given by Eq. (4.21)

According to Eq. (4.24), there are one LHP zero ($\omega_{Z1}$), one dominant LHP pole ($\omega_{P1}$) and one non-dominant LHP pole ($\omega_{P2}$), which are as follows.

$$\omega_{Z1} \approx -\frac{g_{mb2PA(B)}\left(g_{m1PA(B)}+g_{m1NA(B)}\right)}{\left(g_{mb1PA(B)}+g_{m1PA(B)}+g_{m1NA(B)}\right)C_{ff}} \tag{4.25}$$

$$\omega_{P1} \approx -\frac{\left(R_O \parallel R_C\right)^{-1}-g_{mb4PA(B)}}{C_{outA(B)}} \tag{4.26}$$

$$\omega_{P2} \approx -\frac{2\left(R_{AB} \parallel R_{sub}\right)^{-1}+g_{m2PA(B)}-g_{m2NA(B)}}{C_{A(B)}+C_{ff}} \tag{4.27}$$

From Eqs. (4.21) and (4.26), the gain-bandwidth product (*GBW*) is

$$GBW \approx A_{dm}(0)\cdot\omega_{P1} \approx \frac{g_{mb2PA(B)}\left(g_{m1PA(B)}+g_{m1NA(B)}\right)}{g_{m2PA(B)}-g_{m2NA(B)}+2\left(R_{AB} \parallel R_{sub}\right)^{-1}}\cdot\frac{1}{C_{outA(B)}} \tag{4.28}$$

The overall phase margin can be determined as

$$PM \approx 180°-tan^{-1}\left(\frac{GBW}{\omega_{P1}}\right)-tan^{-1}\left(\frac{GBW}{\omega_{P2}}\right)+tan^{-1}\left(\frac{GBW}{\omega_{Z1}}\right) \tag{4.29}$$

It should be noted that $\omega_{Z1}$ is located in the left half plane. This zero will add positive phase margin to the frequency response, thus simplifying the design of the amplifier.

### 4.2.2 Noise Analysis

Input-referred noise voltage of MOSFET is dictated by flicker and thermal noises at low and high frequency, respectively. At low frequency, the input-referred flicker noise $V_{n,(1/f)}$ of the proposed PDA can be derived and shown as below.

$$\overline{V_{n,(1/f)}^2}=\frac{2}{C_{ox}G_{dm}^2}\cdot\frac{1}{f}\left[\begin{array}{l}K_P\left(\frac{g_{m1P}^2}{(WL)_{1P}}+\frac{g_{m3P}^2}{(WL)_{3P}}+\frac{g_{m4P}^2}{(WL)_{4P}}\right)+K_N\left(\frac{g_{m1N}^2}{(WL)_{1N}}+\frac{g_{m3N}^2}{(WL)_{3N}}\right)\\+\left(1+\frac{g_{m2N}^2}{g_{m2P}^2}\right)\left(\frac{K_P g_{m2P}^2}{(WL)_{2P}}+\frac{K_N g_{m2N}^2}{(WL)_{2N}}\right)\end{array}\right] \tag{4.30}$$

where the parameters $K_N$ and $K_P$ are the flicker noise process-dependent constants of NMOS and PMOS, respectively. $C_{ox}$ is the gate capacitance and other parameters have their usual meanings.

At high frequency, the input-referred thermal noise $V_{n,th}$ can be derived and shown as below.

$$\overline{v_{n,th}^2} = \frac{8k_B T\gamma}{G_{dm}^2}\left[g_{m1P} + g_{m1N} + \left(1+\frac{g_{m2N}^2}{g_{m2P}^2}\right)\left(g_{m2P} + g_{m2N} + \frac{1}{\gamma R_{AB}} + \frac{1}{\gamma R_{Msub}}\right) + g_{m3P} + g_{m3N} + g_{m4P} + \frac{1}{\gamma R_C}\right] \quad (4.31)$$

where $k_B$ and $T$ are the Boltzmann constant and absolute temperature, respectively

According to Eqs. (4.30) and (4.31), the input-referred noises are inversely proportional to $G_{dm}$. As a result, appropriate bias condition and transistor dimensions should be arranged so as to maximize $G_{dm}$, e.g., using large transistors and/or large bias current. Obviously, the PDA suffers from a fundamental tradeoff between its noise performance, chip area, frequency response and power consumption.

### 4.2.3 Minimum Supply Voltage and Output Swing

Based on the proposed PDA, the minimum supply voltage can be determined as

$$V_{DD(\min)} = Max(V_{TN} + V_{DSATN}, |V_{TP}| + V_{DSATP}) \quad (4.32)$$

where $V_{TN}$ and $V_{TP}$ are the threshold voltages of NMOS and PMOS, respectively.

According to Eq. (4.32), $V_{DD(min)}$ depends on the threshold voltages and saturation voltages. Apparently, a CMOS process with lower threshold voltage leads to the PDA that can operate at a lower supply voltage.

It is noted that bulk-driven MOS transistor has a parasitic bipolar junction transistor which can cause latch-up. Nevertheless, latch-up will not occur if its bulk voltage is limited to a low voltage level. For the supply voltage as low as 0.5 V, rail-to-rail input common-mode range can be achieved without latch-up.

The output voltage swing is limited by the output voltage swing of the input transconductors $G_{miA,B}$ and feedforward transconductors $G_{mffA,B}$, and it can be expressed as below.

$$V_{DSAT(M_{1NA(B)})} \leq V_{out(swing)} \leq V_{DD} - V_{DSAT(M_{1PA(B)})} \tag{4.33}$$

where $V_{DSAT}$ stands for saturation voltage.

## 4.3 Multiple-Feedback (MFB) Filter Application

To demonstrate the circuit performance, the proposed PDA is used to build a fully-differential multiple-feedback (MFB) filter topology [95] as shown in Figure 4.8

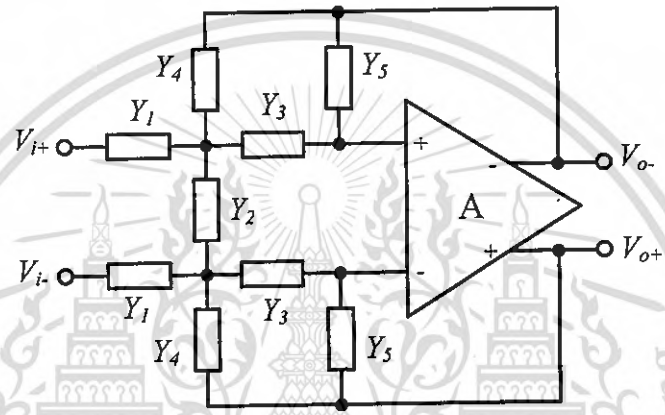



Figure 4.8 Multiple-Feedback (MFB) Filter Topology

From the circuit topology in Figure 4.8, its transfer function can be derived as

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{Y_1 Y_3}{Y_5\left(Y_1 + Y_2 + Y_3 + Y_4\right) + Y_3 Y_4} \tag{4.34}$$

Table 4.1 Passive component of the MFB filter

| Filters | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ |
|---|---|---|---|---|---|
| LP | $R_1$ | $C_2$ | $R_3$ | $R_4$ | $C_5$ |
| HP | $C_1$ | $R_2$ | $C_3$ | $C_4$ | $R_5$ |
| BP | $R_1$ | $R_2$ | $C_3$ | $C_4$ | $R_5$ |

By replacing the passive components $Y_1$-$Y_5$ with either $R$ or $C$ as shown in table 4.1, different types of filter can be achieved. The transfer functions of the MFB as low-pass filter $H_{LP}(s)$, high-pass filter $H_{HP}(s)$, and band-pass filter $H_{BP}(s)$ are summarized in Table 4.2

Table 4.2 Transfer functions of filters

| Filter | Transfer function | $K$ | $\omega_o$ | $Q$ |
|---|---|---|---|---|
| $H_{LP}(s)$ | $-K\dfrac{\omega_o^2}{s^2+\frac{\omega_o}{Q}s+\omega_o^2}$ | $\dfrac{R_4}{R_1}$ | $\sqrt{\dfrac{1}{R_3R_4C_5C_2}}$ | $\sqrt{\dfrac{C_2}{R_3R_4C_5}}(R_1 \parallel R_3 \parallel R_4)$ |
| $H_{HP}(s)$ | $-K\dfrac{s^2}{s^2+\frac{\omega_o}{Q}s+\omega_o^2}$ | $\dfrac{C_1}{C_4}$ | $\sqrt{\dfrac{1}{R_2R_5C_3C_4}}$ | $\sqrt{\dfrac{R_5C_3C_4}{R_2}}\left(\dfrac{1}{C_1+C_3+C_4}\right)$ |
| $H_{BP}(s)$ | $-K\dfrac{\frac{\omega_o}{Q}s}{s^2+\frac{\omega_o}{Q}s+\omega_o^2}$ | $\dfrac{R_5}{R_1}\left(\dfrac{C_3}{C_3+C_4}\right)$ | $\sqrt{\dfrac{1}{R_5C_3C_4}\left(\dfrac{1}{R_1}+\dfrac{1}{R_2}\right)}$ | $\sqrt{R_5C_3C_4\left(\dfrac{1}{R_1}+\dfrac{1}{R_2}\right)}\left(\dfrac{1}{C_3+C_4}\right)$ |

## 4.4 Simulation results

To evaluate the circuit performance and robustness, the proposed PDA has been verified using Cadence Spectre and a standard 0.18 μm CMOS technology with nominal threshold voltages $V_{TN}$ and $V_{TP}$ of 0.45 V and −0.5 V, respectively. A 0.5 V supply was used and the input and output common-mode voltages were set to $V_{DD}/2$, i.e., 0.25 V. The transistor dimensions are listed in Table 4.3. The resistors $R_{AB}$ and $R_C$ were 9 kΩ and 50 kΩ, respectively. The bias current ($I_B$) of the output stage was 6 μA.

Figure 4.9 shows the transient response when a 10 $mV_{pp}$ (10 kHz) sinusoidal differential-mode and common-mode inputs were applied to the PDA. The differential-mode ($v_{od}=v_{o1}-v_{o2}$) and common-mode output voltages ($v_{oc}=(v_{o1}+v_{o2})/2$) read 200 mV and 0.3 mV, respectively.

Figure 4.10 and 4.11 show the differential-mode ($A_{dm}$) and common-mode ($A_{cm}$) frequency characteristics, respectively. The differential mode gain was 57 dB and the common mode gain was −41 dB, resulting in a common-mode rejection ratio of 98 dB. The bandwidth (BW) and unity gain frequency ($f_T$) of $A_{dm}$ and $A_{cm}$ were around the same (i.e., BW ≈ 1 MHz and $f_T$ ≈ 100 MHz). The phase margin was 83°.

Figure 4.12 shows the DC transfer characteristic of the PDA connected in a unity gain configuration. The PDA demonstrated large output swing. Figure 4.13 shows the transient response when an input square wave of 100 KHz with an amplitude of +/- 0.35 V was applied to the PDA, which is connected in the unity gain configuration.

Clearly, a good settling behavior is observed. The slew rate was 2.9 V/μS. The input referred noise as a function of frequency was illustrated in Figure 4.14 which showed 86.39 nV/√Hz at 1 MHz and read integrated noise of 378 μV(rms) in a range from 100kHz to 10 MHz.

To investigate how the process variation and device mismatch influence the *CMRR*, Monte Carlo simulations have been carried out. A one thousand iteration Monte Carlo analysis was performed. The Monte Carlo statistical result of the *CMRR* that accounts for the presence of the process variation was depicted in Figure 4.15. The smallest and largest *CMRRs* were 69.67 dB and 98.43 dB, respectively. The mean value was 85.98 dB and the standard deviation was 7.44. The maximum number of occurrences was at 82.45 dB. Monte Carlo simulation of the *CMRR* that accounts for device mismatches was depicted in Figure 4.16. The smallest and largest *CMRRs* were 48.86 dB and 91.89 dB, respectively. The mean value was 70.51 dB, while the standard deviation was 9.24. The maximum number of occurrences was at 72.76 dB. Obviously, the device mismatch plays more significant role than the process variation and, therefore, appropriate layout techniques is essential.

The layout of the proposed PDA was illustrated in Figure 4.17. It occupied the chip area of 154 x 138 $\mu m^2$. The performances of the circuit from a post-layout simulation were summarized in Table 4.4. As can be seen, the performances were in good agreement with those from the pre-layout simulation.

Figure 4.18 shows the frequency response of the MFB filter. The components of the LP filter were $R_1$=10kΩ, $R_3$=10kΩ, $R_4$=31kΩ, $C_2$=5pF and $C_5$=2.5pF, while the components of the HP filter were $R_2$=60kΩ, $R_5$=15kΩ, $C_1$=30pF, $C_3$=50pF, $C_4$=20pF. Finally, the components of the BP filter were $R_1$=10kΩ, $R_2$=10kΩ, $R_5$=80kΩ, $C_3$=10pF, $C_4$=3.5pF. The quality factor Q was 0.34.

Table 4.4 compared the performance characteristics of the proposed PDA and the others reported in the literature. To achieve a fair comparison, a figure of merit (FOM) as defined in Eq. (4.35) was utilized [61]. This FOM includes four key parameters, namely, gain bandwidth product (*GBW*), power dissipation ($P_D$) and load capacitor ($C_L$).

$$FOM = \frac{GBW\,(MHz) \times C_L(\mathrm{pF})}{P_D\,(\mu W)} \tag{4.35}$$

It can be seen in the last row of Table 4.4 that the FOM of the proposed PDA is higher than most of the PDAs

Table 4.3 Dimensions of Transistors

| Transistors | $W$ (μm) | $L$ (μm) |
|---|---|---|
| $M_{1NA(B)}$ | 10.4 | 0.5 |
| $M_{1PA(B)}$ | 38 | 0.5 |
| $M_{2NA(B)}$ | 10.4 | 0.5 |
| $M_{2PA(B)}$ | 38 | 0.5 |
| $M_{3NA(B)}$ | 2.4 | 0.5 |
| $M_{3PA(B)}$ | 14.8 | 0.5 |
| $M_{4PA(B)}$ | 23.1 | 0.5 |

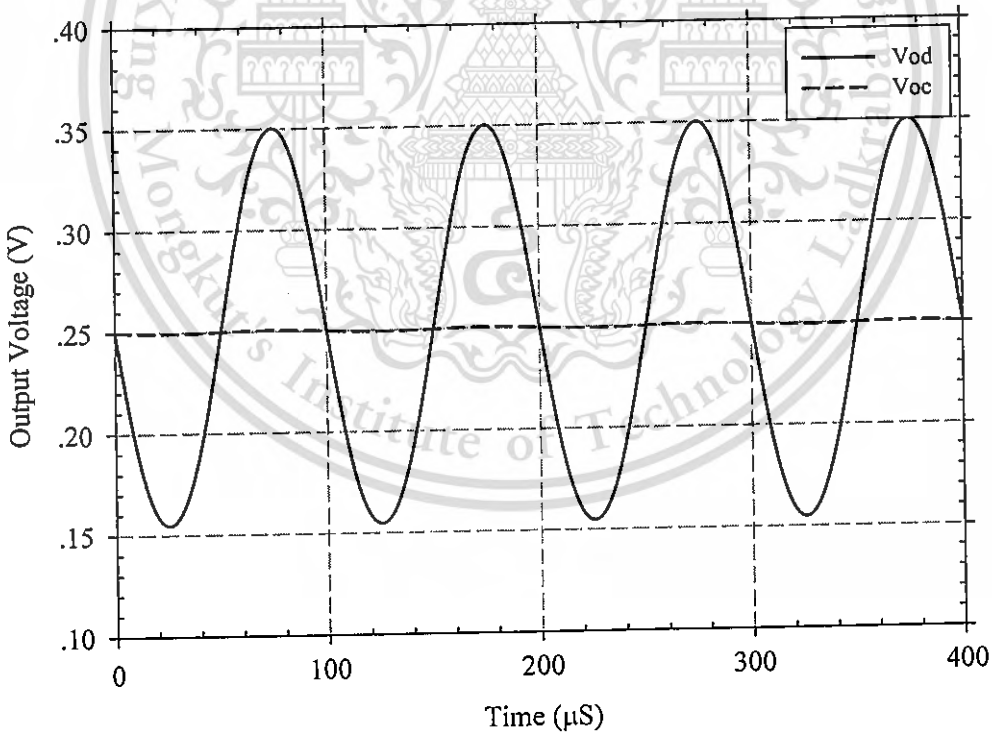



Figure 4.9 Differential-mode and common-mode output voltages

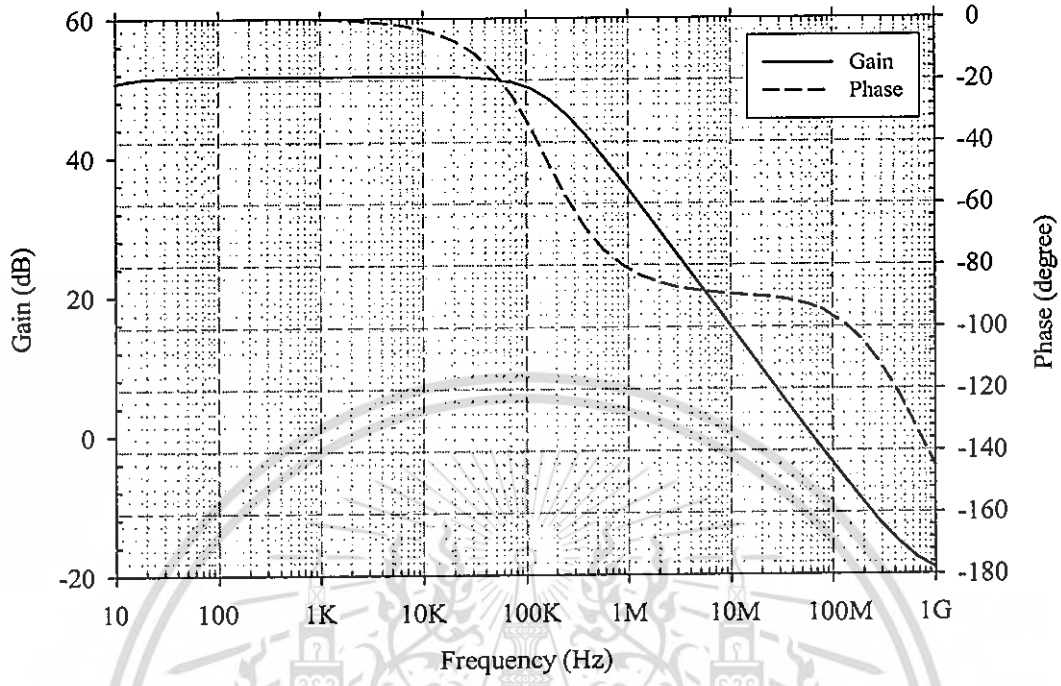



Figure 4.10 Differential-mode gain and phase

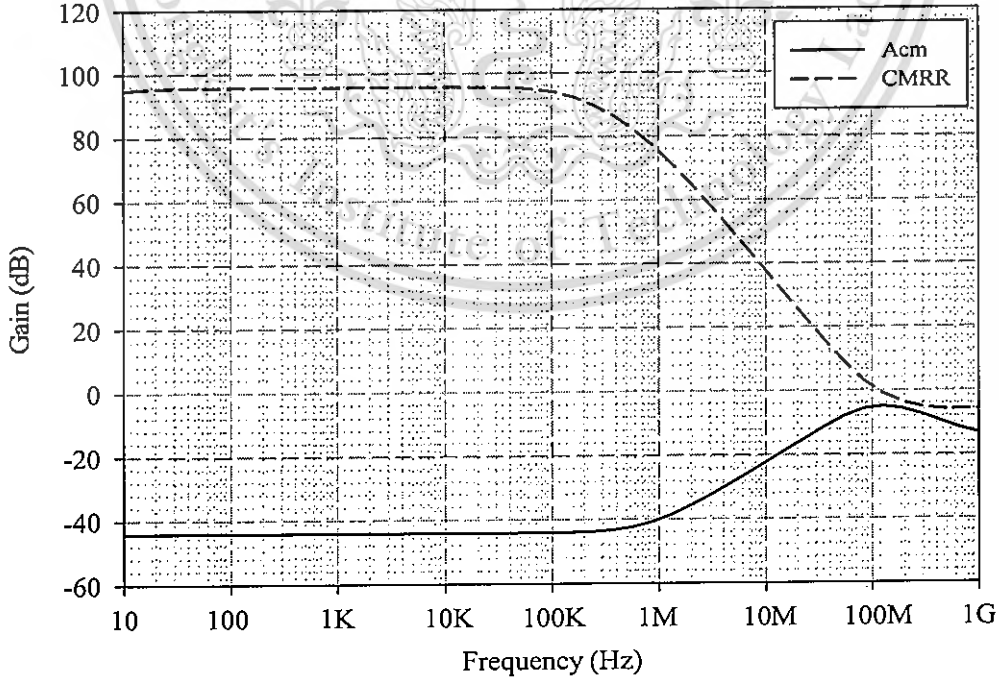



Figure 4.11 Common-mode gain and CMRR

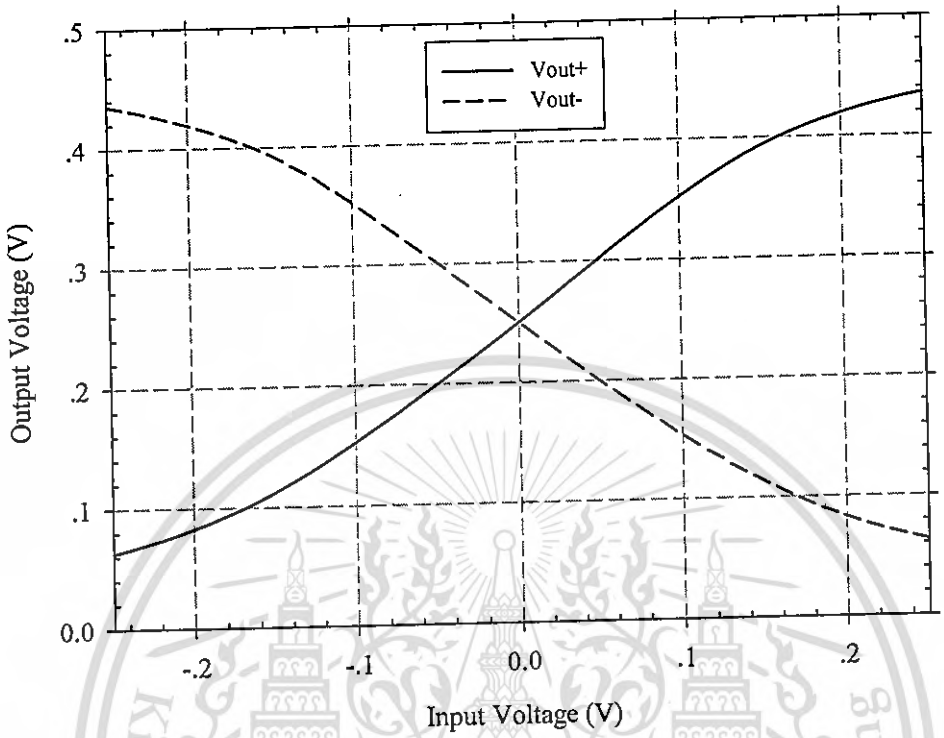



Figure 4.12 Voltage transfer characteristic in closed-loop configuration

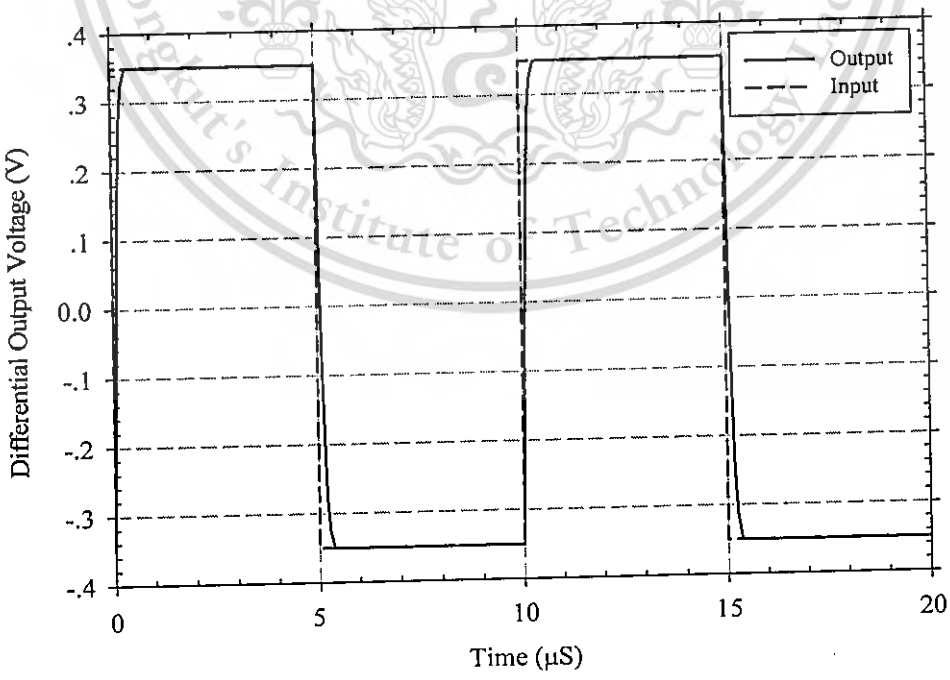



Figure 4.13 Transient response in closed-loop configuration

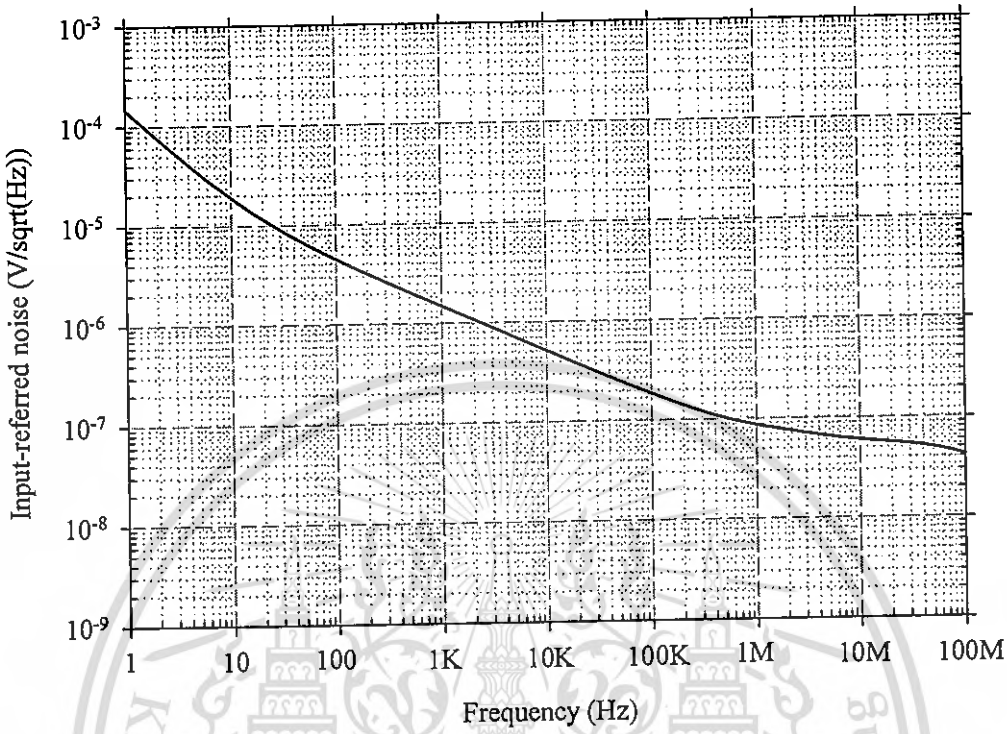



Figure 4.14 Input-referred noise

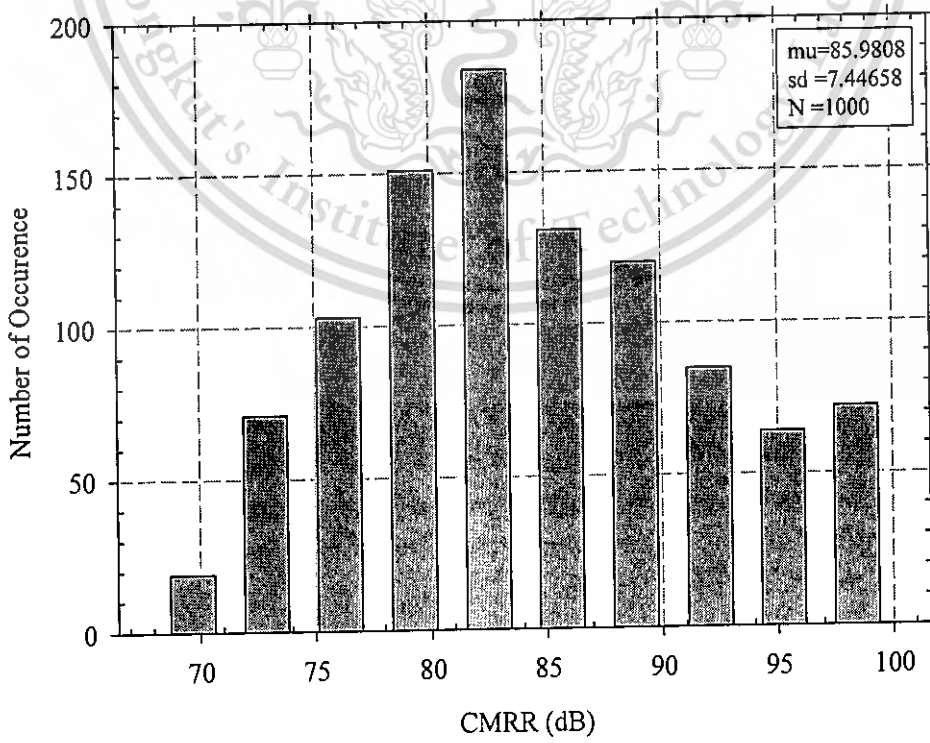



Figure 4.15 Monte Carlo simulation results for *CMRR* with process variation (1000 runs)

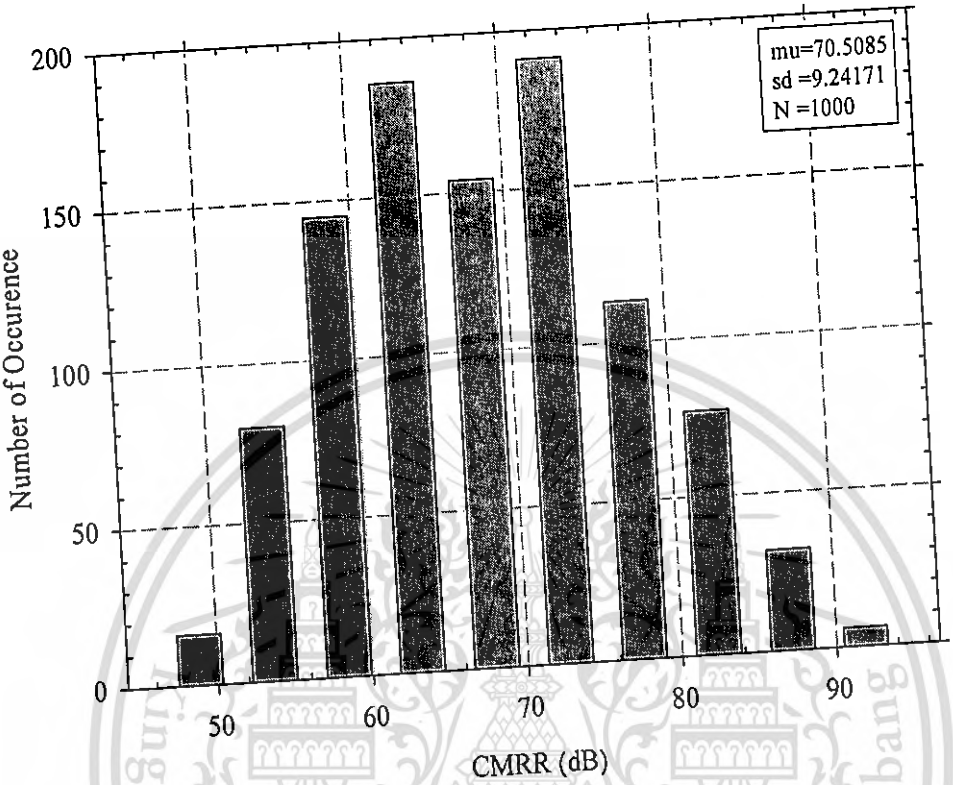



Figure 4.16 Monte Carlo simulation results for *CMRR* with mismatch (1000 runs)

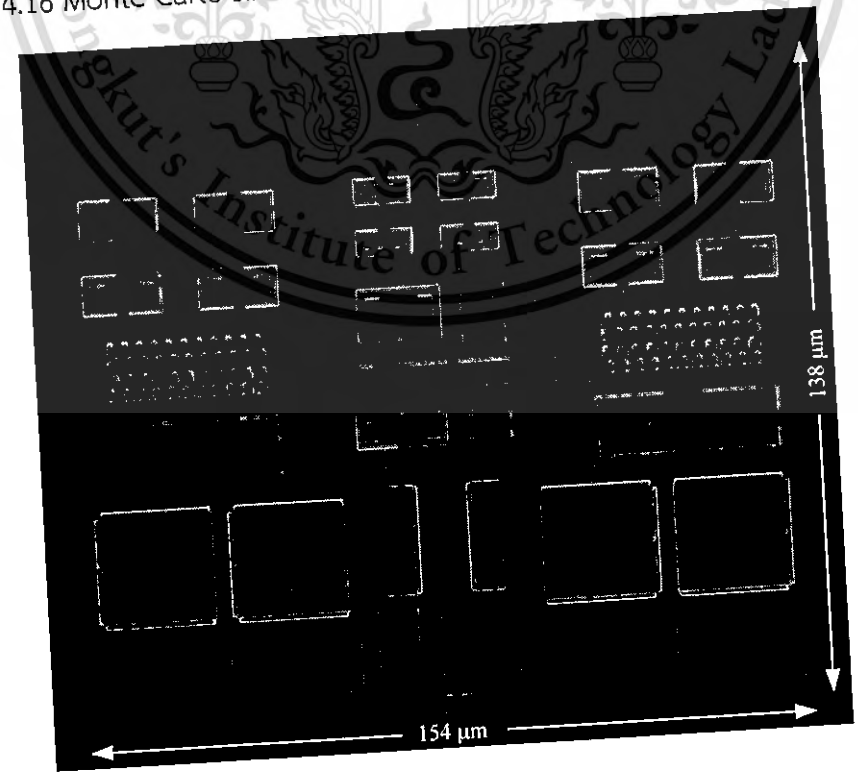



Figure 4.17 Layout of the proposed circuit

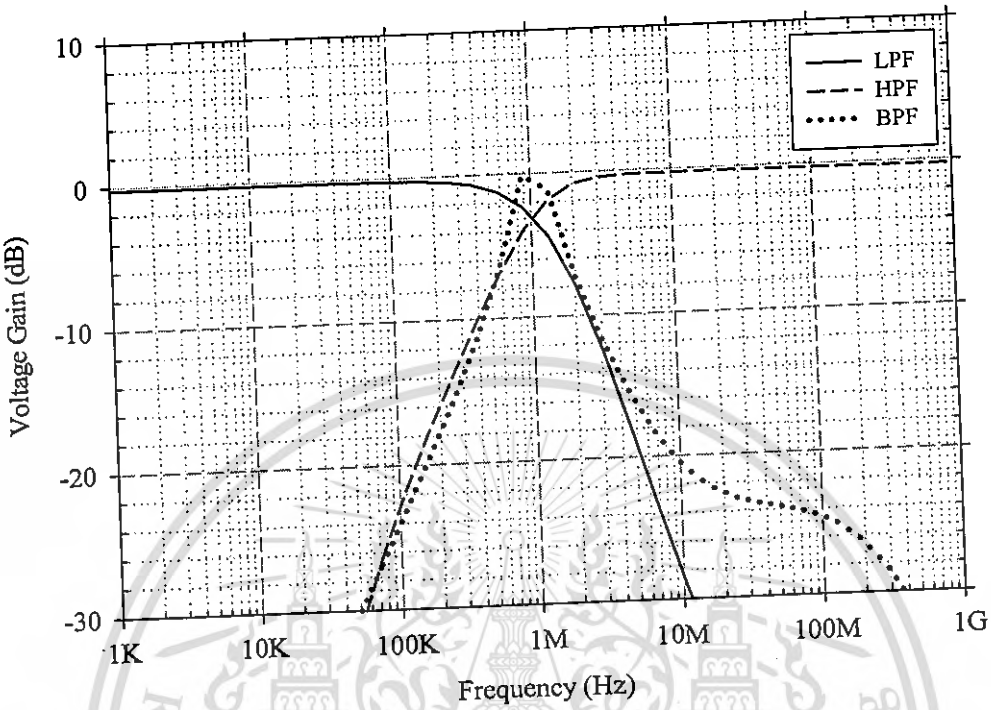



Figure 4.18 Frequency response of filters

Table 4.4 Performances of the proposed circuit and other reported OTAs

| Parameters | [23] | [24] | [28] | This work |
|---|---|---|---|---|
| Technology | 0.18 µm (N-well) | 0.18 µm (Triple-well) | 0.18 µm (N-well) | 0.18 µm (N-well) |
| Power supply | 0.5 V | 0.5 V | 0.5 V | 0.5 V |
| DC Gain | 48 dB | 65 dB | 56 dB | 57 dB |
| GBW ($C_L$=20pF) | 2.4 MHz | 550 KHz | 3.2 MHz | 1 MHz |
| Phase margin | 45° | 50° | 58° | 86° |
| CMRR | 78 dB | 86 dB | 73 dB | 98 dB |
| PSRR | 76 dB | 76 dB | 93 dB | 82 dB |
| Input ref. noise | 90 nV/$\sqrt{Hz}$ | 432 nV/$\sqrt{Hz}$ | 74 nV/$\sqrt{Hz}$ | 86.39 nV/$\sqrt{Hz}$ |
| Linearity | HD3@0.4Vp-p =-40 dB | HD3@0.5Vp-p =-57 dB | THD@0.17Vp-p =-40dB | THD@0.5Vp-p =-40 dB |
| Slew rate | 2.92 V/µS | 0.23 V/µS | 1.34 V/µS | 2.9 V/µS |
| $C_L$ | 20pF | 20pF | 1pF | 20pF |
| Power consumption | 110 µW | 28 µW | 45 µW | 48 µW |
| FOM (x100) | 43.6 | 39 | 7 | 41.7 |

## 4.5 Conclusion

This chapter presents a low-voltage bulk-driven quasi-floating-gate pseudo-differential amplifier (BD-QFG PDA). The feedforward technique using simple circuitry was introduced to suppress the common-mode signals. The gain-enhancement network and output stage were developed to enhance the differential-mode gain and set the common-mode voltage. Both input and output stages operate in class AB. The circuit was simulated at 0.5 Volt supply using a standard CMOS technology process. The results demonstrated wide input and output signal swings, relatively large differential-mode gain and small common-mode gain.

# CHAPTER 5
# CONCLUSIONS

## 5.1 Summary and Discussions

This thesis deals with the design of pseudo differential amplifiers (PDAs) which are important parts of analog signal processing circuit. PDAs find several applications in numerous analog circuits such as $G_m$-C filter, current feedback amplifier, instrument amplifier, oscillator, and data converter. As a result, numerous approaches have been proposed to design PDAs. In this thesis, the author utilized existing analog circuit design techniques to implement OTAs which can operate at low supply voltage with rail-to-rail capability and also their applications using standard CMOS technologies.

The summary of the thesis can be discussed as follow:

First of all, the design and application of PDA using a current-mode common-mode feed-back (CMFB) circuit is presented in the section 3.1. The CMFB converts the output voltage signals into currents, which is then applied to two current mirrors, operating as a common-mode detector. The current amplifier is used to enhance the loop gain, resulting in minimized gain error. The positive feedback is also employed to enhance the differential gain of the system. The proposed CMFB shows low common-mode gain and rail-to-rail capability.

Additionally, the design and application of a CMOS inverter-based class-AB PDA is proposed in section 3.2. The circuit is designed based on a CMOS inverter and low-voltage wide-swing CMFB circuit. The proposed PDA demonstrates rail-to-rail operation. The simulation results show that the circuit can operate at the supply voltage of 1 V with the differential and CM gains of 38 and -15 dB, respectively. The unity-gain frequency is 1.42 GHz and the power dissipation is 102.5 μW.

Finally, the design and application of the low-voltage pseudo-differential amplifiers (PDA) is presented in chapter 4. The feedforward technique using simple circuitry was introduced to suppress the common-mode signals. The gain-enhancement network and output stage were developed to enhance the differential-mode gain and set the common-mode voltage. Both input and output stages operate in class AB. The circuit was simulated at 0.5 Volt supply using a standard CMOS technology process. The results demonstrated wide input and output signal swings, relatively large differential-mode gain and small common-mode gain.

## 5.2 Suggestions for Future Work

In the future, it will be necessary to investigate in more detail the benefits and drawbacks of the proposed PDAs. Two issues which have not been yet thoroughly investigated are the performance of these circuits in the presence of process variations as well as mismatch by using both gate-driven and bulk-driven quasi-floating-gate transistors. A more in-depth characterization of the noise performance of PD circuits is also needed. It will also be necessary to develop more low-voltage and low-power analog applications such as $G_m$-C filter, and analog-to-digital converters in the future, so that eventually a complete system can be developed which runs off of a sub-volt power supply.

Furthermore, it is evident that the bulk-driven quasi-floating-gate (BD-QFG) approach as a research topic is increasingly popular. The author recommends looking into other new application areas using the BD-QFG approach and developing the improved versions of the above author's circuit blocks.

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# APPENDIX A
# THE DIFFERENTIAL-MODE AND COMMON-MODE OUTPUT IMPEDANCE OF THE PDA

- In case of output common-mode current

Based on the proposed PDA in Figure A.1, the output current ($i_{o1}$ and $i_{o2}$) can be shown as

$$i_{o1} = \frac{v_{o1}}{Z_{out}} + (1+\alpha) i_R + A i_{cm} = \frac{v_{o1}}{Z_{out}} + (1+\alpha)\frac{v_{o1}}{R_{1,2}} + \frac{2A\beta}{R_{1,2}} v_{oc} \tag{A.1}$$

$$i_{o2} = \frac{v_{o2}}{Z_{out}} + (1+\alpha) i_R + A i_{cm} = \frac{v_{o2}}{Z_{out}} + (1+\alpha)\frac{v_{o2}}{R_{1,2}} + \frac{2A\beta}{R_{1,2}} v_{oc} \tag{A.2}$$

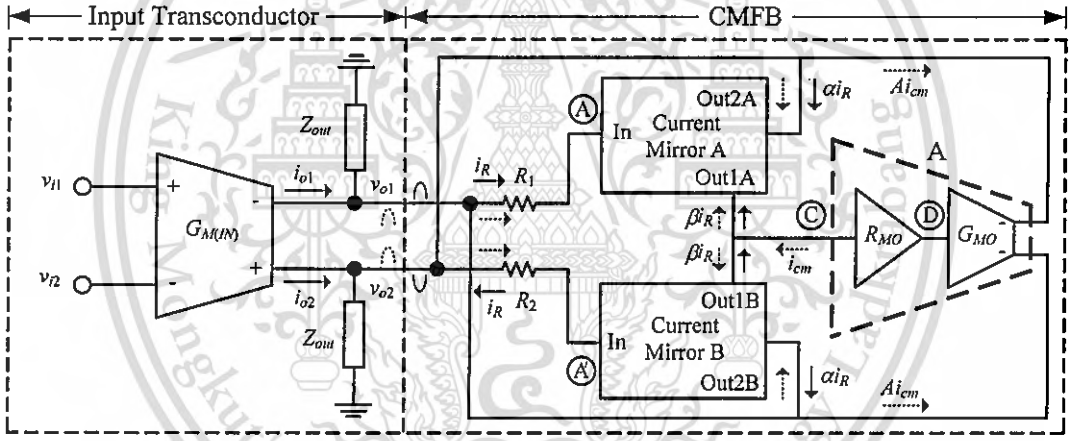



Figure A.1 Conceptual structure of PDA with proposed CMFB

Since the output common-mode current is $i_{oc} = (i_{o1} + i_{o2})/2$, we have

$$i_{oc} = \frac{\dfrac{v_{o1} + v_{o2}}{Z_{out}} + \dfrac{(1+\alpha+2A\beta)}{R_{1,2}} v_{oc}}{2} \tag{A.3}$$

By substituting $v_{oc} = (v_{o1} + v_{o2})/2$ into equation (A.3), we obtain

$$i_{oc} = \frac{\dfrac{2v_{oc}}{Z_{out}} + \dfrac{2(1+\alpha+2A\beta)}{R_{1,2}}}{2}$$

$$= \left[ \frac{1}{Z_{out}} + \frac{(1+\alpha+2A\beta)}{R_{1,2}} \right] v_{oc}$$

$$= \left[ \frac{1+(1+\alpha+2A\beta) Z_{out} / R_{1,2}}{Z_{out}} \right] v_{oc} \quad \text{(A.4)}$$

Thus, the common-mode output impedance ($Z_{cm}$) is

$$Z_{cm} = \frac{v_{oc}}{i_{oc}} = \left[ \frac{Z_{out}}{1+(1+\alpha+2A\beta) Z_{out} / R_{1,2}} \right] \quad \text{(A.5)}$$

- In case of output differential-mode current

the output current ($i_{o1}$ and $i_{o2}$) can be shown as

$$i_{o1} = \frac{v_{o1}}{Z_{out}} + (1-\alpha) i_R = \frac{v_{o1}}{Z_{out}} + (1-\alpha) \frac{v_{o1}}{R_{1,2}} \quad \text{(A.6)}$$

$$i_{o2} = \frac{v_{o2}}{Z_{out}} + (1-\alpha) i_R = \frac{v_{o2}}{Z_{out}} + (1-\alpha) \frac{v_{o2}}{R_{1,2}} \quad \text{(A.7)}$$

From equations (A.6) and (A.7), $i_{od}$ is

$$i_{od} = i_{o1} - i_{o2} = \frac{1+(1-\alpha) Z_{out} / R_{1,2}}{Z_{out}} v_{od} \quad \text{(A.8)}$$

Since $v_{od} = (v_{o1} - v_{o2})$, the differential-mode output impedance ($Z_{dm}$) is

$$Z_{dm} = \frac{v_{od}}{i_{od}} = \frac{Z_{out}}{1+(1-\alpha) Z_{out} / R_{1,2}} \quad \text{(A.9)}$$

# APPENDIX B

# THE DIFFERENTIAL-MODE AND COMMON-MODE TRANSCONDUCTANCE OF THE PDA

When the input signal is differential ($v_{i1}$=-$v_{i2}$), the output currents of the circuit in Figure B.1 are given as

$$i_{o1} = g_{mb1P}v_{i1} + \frac{g_{mb2P}v_{i1}}{g_{m2P} - g_{m2N} + g_{o2N} + g_{o2P} + 2R_{AB}^{-1}}\left(g_{m1P} + g_{m1N}\right) \tag{B.1}$$

$$i_{o2} = g_{mb1P}v_{i2} + \frac{g_{mb2P}v_{i2}}{g_{m2P} - g_{m2N} + g_{o2N} + g_{o2P} + 2R_{AB}^{-1}}\left(g_{m1P} + g_{m1N}\right) \tag{B.2}$$

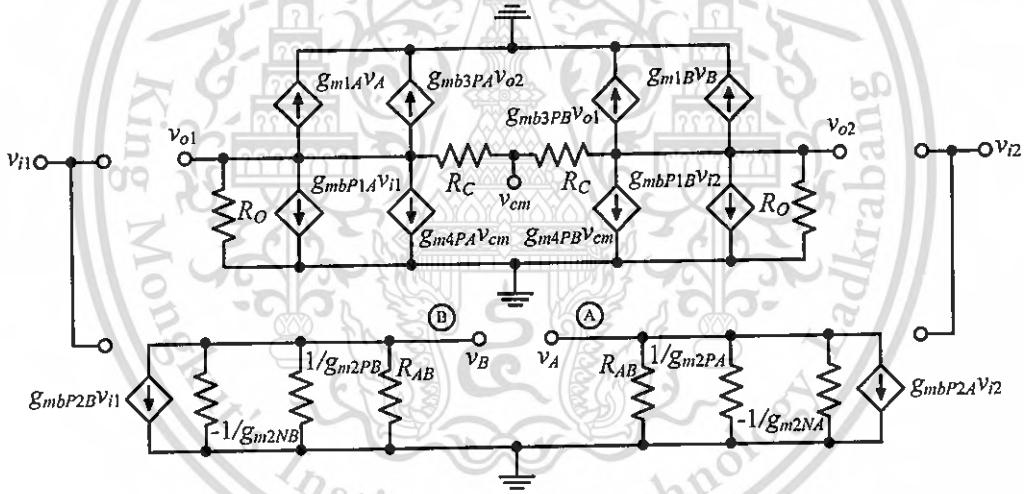



Figure B.1 Small signal equivalent circuit of the feedforward PDA

The differential output current $i_{od}$ is thus given by

$$i_{od} = i_{o1} - i_{o2} = g_{mb1P}\left(v_{i1} - v_{i2}\right) + \frac{g_{mb2P}\left(g_{m1P} + g_{m1N}\right)}{g_{m2P} - g_{m2N} + g_{o2N} + g_{o2P} + 2R_{AB}^{-1}}\left(v_{i1} - v_{i2}\right) \tag{B.3}$$

$$i_{od} = \left[g_{mb1P} + \frac{g_{mb2P}\left(g_{m1P} + g_{m1N}\right)}{g_{m2P} - g_{m2N} + g_{o2N} + g_{o2P} + 2R_{AB}^{-1}}\right]\left(v_{i1} - v_{i2}\right) \tag{B.4}$$

From Eqs. (B.4), the differential-mode transconductance ($G_{dm}$) can be expressed as

$$G_{dm} = g_{mb1P} + \frac{g_{mb2P}}{g_{m2P} - g_{m2N} + g_{o2N} + g_{o2P} + 2R_{AB}^{-1}}\left(g_{m1PA} + g_{m1N}\right) \tag{B.5}$$

In the case of common-mode signals ($v_{i1}$=$v_{i2}$), the output currents are

$$i_{o1} = g_{mb1P}v_{i1} - \frac{g_{mb2P}v_{i1}}{g_{m2P} + g_{m2N} + g_{o2N} + g_{o2P}}\left(g_{m1P} + g_{m1N}\right) \tag{B.6}$$

$$i_{o2} = g_{mb1P}v_{i2} - \frac{g_{mb2P}v_{i2}}{g_{m2P} + g_{m2N} + g_{o2N} + g_{o2P}}\left(g_{m1P} + g_{m1N}\right) \tag{B.7}$$

Since, $i_{oc} = (i_{o1} + i_{o2})/2$, thus the output current is given by

$$i_{oc} = g_{mb1P}\left(\frac{v_{i1} + v_{i2}}{2}\right) - \frac{g_{mb2P}\left(g_{m1P} + g_{m1N}\right)}{g_{m2P} + g_{m2N} + g_{o2N} + g_{o2P}}\left(\frac{v_{i1} + v_{i2}}{2}\right) \tag{B.8}$$

$$i_{oc} = \left[g_{mb1P} - \frac{g_{mb2P}\left(g_{m1P} + g_{m1N}\right)}{g_{m2P} + g_{m2N} + g_{o2N} + g_{o2P}}\right]\left(\frac{v_{i1} + v_{i2}}{2}\right) \tag{B.9}$$

By substituting $v_{ic} = (v_{i1} + v_{i2})/2$ into equation (B.9), the common-mode transconductance ($G_{cm}$) is

$$G_{cm} = g_{mb1P} - g_{mb2P}\frac{\left(g_{m1PA} + g_{m1N}\right)}{g_{m2P} + g_{m2N} + g_{o2N} + g_{o2P}} \tag{B.10}$$

# APPENDIX C
# FREQUENCY RESPONSE OF THE PDA

Based on the small signal equivalent circuit in Figure C.1, the transfer function is given by

$$F(s)=\frac{A+Bs}{C+Ds+Es^2+Fs^3+Gs^4} \tag{C.1}$$

where

$$A=\frac{2\beta}{R}g_{mb1}r_{oC}r_{oD}r_{oL}\left(1-g_{m5}R_F\right) \tag{C.2}$$

$$B=\frac{2\beta}{R}g_{mb1}r_{oC}r_{oD}r_{oL}C_C\left(R_F+R_C-g_{m5}R_FR_C\right) \tag{C.3}$$

$$C=g_{m5}r_{oC}r_{oD}+r_{oC}+r_{oD}+R_F \tag{C.4}$$

$$\begin{aligned}D=\;&C_{oC}r_{oC}R_F+C_{oC}r_{oC}r_{oD}+C_{oD}r_{oD}R_F+C_{oD}r_{oC}r_{oD}+g_{m5}r_{oC}r_{oD}r_{oL}C_{oL}+C_{oL}r_{oL}R_F+C_{oL}r_{oC}r_{oL}+C_{oL}r_{oD}r_{oL}\\&+g_{m5}r_{oC}r_{oD}R_CC_C+g_{m5}r_{oC}r_{oD}R_FC_C+R_CR_FC_C+r_{oC}R_CC_C+r_{oC}R_FC_C+r_{oD}R_CC_C+r_{oD}R_FC_C\end{aligned} \tag{C.5}$$

$$\begin{aligned}E=\;&C_{oC}C_{oD}r_{oC}r_{oD}R_F+C_{oC}C_{oL}r_{oC}r_{oL}R_F+C_{oC}C_{oL}r_{oC}r_{oD}r_{oL}+C_{oC}C_Cr_{oC}R_CR_F+C_{oC}C_Cr_{oC}r_{oD}R_C+C_{oC}C_Cr_{oC}r_{oD}R_F\\&+C_{oD}C_{oL}r_{oD}r_{oL}R_F+C_{oD}C_{oL}r_{oC}r_{oD}r_{oL}+C_{oD}C_Cr_{oD}R_CR_F+C_{oD}C_Cr_{oC}r_{oD}R_C+C_{oD}C_Cr_{oC}r_{oD}R_F+g_{m5}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_C\\&+g_{m5}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_F+C_{oL}C_Cr_{oL}R_CR_F+C_{oL}C_Cr_{oC}r_{oL}R_C+C_{o3}C_Cr_{o1}r_{o3}R_F+C_{o3}C_Cr_{o2}r_{o3}R_C+C_{oL}C_Cr_{oD}r_{oL}R_F\end{aligned} \tag{C.6}$$

$$\begin{aligned}F=\;&C_{oC}C_{oD}C_{oL}r_{oC}r_{oD}r_{oL}R_F+C_{oC}C_{oD}C_Cr_{oC}r_{oD}R_CR_F+C_{oC}C_{oL}C_Cr_{oC}r_{oL}R_CR_F+C_{oC}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_C\\&+C_{oC}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_F+C_{oD}C_{oL}C_Cr_{oD}r_{oL}R_CR_F+C_{oD}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_C+C_{oD}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_F\end{aligned} \tag{C.7}$$

$$G=C_{oC}C_{oD}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_FR_C \tag{C.8}$$

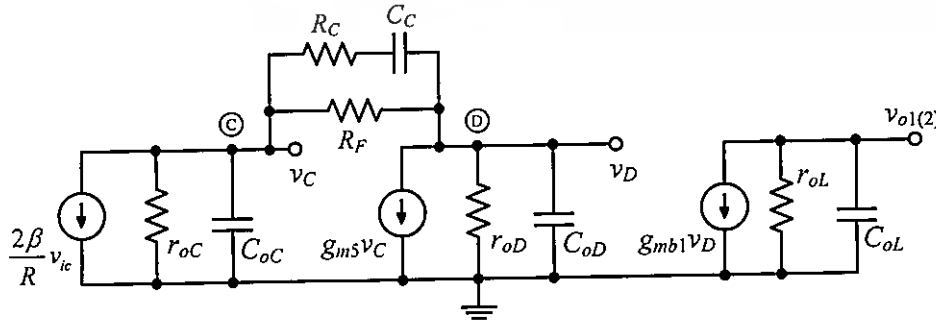



Figure C.1 Simplified small signal CMFB loop (see in chapter 3)

The generic pole-zero transfer function can be written as

$$F(s)=\frac{K\left(1+\frac{s}{\omega_{Z1}}\right)}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)\left(1+\frac{s}{\omega_{P3}}\right)\left(1+\frac{s}{\omega_{P4}}\right)} \tag{C.9}$$

The poles in the denominator term can be derived using the following equality:

$$D(s)=1+K_1s+K_2s^2+K_3s^3+K_4s^4=\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)\left(1+\frac{s}{\omega_{P3}}\right)\left(1+\frac{s}{\omega_{P4}}\right)$$

$$=1+s\left(\frac{1}{\omega_{P1}}+\frac{1}{\omega_{P2}}+\frac{1}{\omega_{P3}}+\frac{1}{\omega_{P4}}\right)+s^2\left(\frac{1}{\omega_{P1}\omega_{P2}}+\frac{1}{\omega_{P1}\omega_{P3}}+\frac{1}{\omega_{P2}\omega_{P3}}+\frac{1}{\omega_{P1}\omega_{P4}}+\frac{1}{\omega_{P2}\omega_{P4}}+\frac{1}{\omega_{P3}\omega_{P4}}\right) \tag{C.10}$$
$$+s^3\left(\frac{1}{\omega_{P1}\omega_{P2}\omega_{P3}}+\frac{1}{\omega_{P1}\omega_{P2}\omega_{P4}}+\frac{1}{\omega_{P1}\omega_{P3}\omega_{P4}}+\frac{1}{\omega_{P2}\omega_{P3}\omega_{P4}}\right)+s^4\left(\frac{1}{\omega_{P1}\omega_{P2}\omega_{P3}\omega_{P4}}\right)$$

If $|\omega_{P4}|\gg|\omega_{P3}|\gg|\omega_{P2}|\gg|\omega_{P1}|$ then,

$$D(s)=1+K_1s+K_2s^2+K_3s^3+K_4s^4\approx1+\frac{s}{\omega_{P1}}+\frac{s^2}{\omega_{P1}\omega_{P2}}+\frac{s^3}{\omega_{P1}\omega_{P2}\omega_{P3}}+\frac{s^4}{\omega_{P1}\omega_{P2}\omega_{P3}\omega_{P4}} \tag{C.11}$$

$$\omega_{P1}\approx-\frac{1}{K_1} \tag{C.12}$$

$$\omega_{P2}\approx-\frac{K_1}{K_2} \tag{C.13}$$

$$\omega_{P3}\approx-\frac{K_2}{K_3} \tag{C.14}$$

$$\omega_{P4}\approx-\frac{K_3}{K_4} \tag{C.15}$$

By comparing equations (C.1) and (C.11), the pole-zero can be express as

$$\omega_{Z1}\approx-\frac{A}{B}\approx-\frac{\frac{2\beta}{R}g_{mb1}r_{oC}r_{oD}r_{oL}\left(1-g_{m5}R_F\right)}{\frac{2\beta}{R}g_{mb1}r_{oC}r_{oD}r_{oL}C_C\left(R_F+R_C-g_{m5}R_FR_C\right)}\approx-\frac{1}{C_CR_C} \tag{C.16}$$

$$\omega_{P1}\approx-\frac{C}{D} \tag{C.17}$$

$$\approx -\frac{g_{m5}r_{oC}r_{oD}+r_{oC}+r_{oD}+R_F}{\begin{array}{l}C_{oC}r_{oC}R_F+C_{oC}r_{oC}r_{oD}+C_{oD}r_{oD}R_F+C_{oD}r_{oC}r_{oD}+g_{m5}r_{oC}r_{oD}r_{oL}C_{oL}+C_{oL}r_{oL}R_F+C_{oL}r_{oC}r_{oL}+C_{oL}r_{oD}r_{oL}\\ +g_{m5}r_{oC}r_{oD}R_CC_C+g_{m5}r_{oC}r_{oD}R_FC_C+R_CR_FC_C+r_{oC}R_CC_C+r_{oC}R_FC_C+r_{oD}R_CC_C+r_{oD}R_FC_C\end{array}} \quad (C.18)$$

$$\approx -\frac{g_{m5}r_{oC}r_{oD}}{C_{oL}r_{oL}\left(R_F+r_{oC}+r_{oD}\right)+g_{m5}r_{oC}r_{oD}\left(r_{oL}C_{oL}+R_CC_C+R_FC_C\right)+C_CR_F\left(R_C+r_{oC}+r_{oD}\right)} \quad (C.19)$$

$$\omega_{P1}\approx -\frac{1}{r_{oL}C_{oL}+C_C\left(R_C+R_F\right)} \quad (C.20)$$

$$\omega_{P2}\approx -\frac{D}{E} \quad (C.21)$$

$$\approx -\frac{\begin{array}{l}C_{oC}r_{oC}R_F+C_{oC}r_{oC}r_{oD}+C_{oD}r_{oD}R_F+C_{oD}r_{oC}r_{oD}+g_{m5}r_{oC}r_{oD}r_{oL}C_{oL}+C_{oL}r_{oL}R_F+C_{oL}r_{oC}r_{oL}+C_{oL}r_{oD}r_{oL}\\ +g_{m5}r_{oC}r_{oD}R_CC_C+g_{m5}r_{oC}r_{oD}R_FC_C+R_CR_FC_C+r_{oC}R_CC_C+r_{oC}R_FC_C+r_{oD}R_CC_C+r_{oD}R_FC_C\end{array}}{\begin{array}{l}C_{oC}C_{oD}r_{oC}r_{oD}R_F+C_{oC}C_{oL}r_{oC}r_{oL}R_F+C_{oC}C_{oL}r_{oC}r_{oD}r_{oL}+C_{oC}C_Cr_{oC}R_CR_F+C_{oC}C_Cr_{oC}r_{oD}R_C+C_{oC}C_Cr_{oC}r_{oD}R_F\\ +C_{oD}C_{oL}r_{oD}r_{oL}R_F+C_{oD}C_{oL}r_{oC}r_{oD}r_{oL}+C_{oD}C_Cr_{oD}R_CR_F+C_{oD}C_Cr_{oC}r_{oD}R_C+C_{oD}C_Cr_{oC}r_{oD}R_F+g_{m5}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_C\\ +g_{m5}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_F+C_{oL}C_Cr_{oL}R_CR_F+C_{oL}C_Cr_{oC}r_{oL}R_C+C_{o3}C_Cr_{o1}r_{o3}R_F+C_{o3}C_Cr_{o2}r_{o3}R_C+C_{oL}C_Cr_{oD}r_{oL}R_F\end{array}} \quad (C.22)$$

$$\approx -\frac{\begin{array}{l}C_{oC}r_{oC}\left(R_F+r_{oD}\right)+C_{oD}r_{oD}\left(R_F+r_{oC}\right)+C_{oL}r_{oL}\left(R_F+r_{oC}+r_{oD}\right)\\ +g_{m5}r_{oC}r_{oD}\left(r_{oL}C_{oL}+R_CC_C+R_FC_C\right)+C_C\left(R_F\left(R_C+r_{oC}+r_{oD}\right)+R_C\left(r_{oC}+r_{oD}\right)\right)\end{array}}{\begin{array}{l}C_{oC}C_{oL}r_{oC}r_{oL}\left(R_F+r_{oD}\right)+C_CR_CR_F\left(C_{oC}r_{oC}+C_{oL}r_{oL}\right)+C_{oD}C_{oL}r_{oD}r_{oL}\left(R_F+r_{oC}\right)\\ +C_{oD}C_Cr_{oD}R_CR_F+C_{oC}C_{oD}r_{oC}r_{oD}R_F\\ +\left(R_F+R_C\right)\left(g_{m5}C_{oL}C_Cr_{oC}r_{oD}r_{oL}+C_{oL}C_Cr_{oC}r_{oL}+C_{oL}C_Cr_{oD}r_{oL}+C_{oD}C_Cr_{oC}r_{oD}+C_{oC}C_Cr_{oC}r_{oD}\right)\end{array}} \quad (C.23)$$

$$\approx -\frac{+g_{m5}r_{oC}r_{oD}\left(r_{oL}C_{oL}+R_CC_C+R_FC_C\right)+C_C\left(R_F\left(R_C+r_{oC}+r_{oD}\right)+R_C\left(r_{oC}+r_{oD}\right)\right)}{\left(R_F+R_C\right)\left(g_{m5}C_{oL}C_Cr_{oC}r_{oD}r_{oL}+C_{oL}C_Cr_{oC}r_{oL}+C_{oL}C_Cr_{oD}r_{oL}+C_{oD}C_Cr_{oC}r_{oD}+C_{oC}C_Cr_{oC}r_{oD}\right)} \quad (C.24)$$

$$\approx -\frac{g_{m5}r_{oC}r_{oD}\left(r_{oL}C_{oL}+R_CC_C+R_FC_C\right)+C_C\left(R_F\left(R_C+r_{oC}+r_{oD}\right)\right)}{g_{m5}C_{oL}C_Cr_{oC}r_{oD}r_{oL}\left(R_F+R_C\right)} \quad (C.25)$$

$$\approx -\frac{g_{m5}r_{oC}r_{oD}\left(r_{oL}C_{oL}+C_C\left(R_F+R_C\right)\right)+C_C\left(R_F\left(r_{oC}+r_{oD}\right)\right)}{g_{m5}C_{oL}C_Cr_{oC}r_{oD}r_{oL}\left(R_F+R_C\right)} \quad (C.26)$$

$$\omega_{P2}\approx -\frac{r_{oL}C_{oL}+C_C\left(R_F+R_C\right)}{C_{oL}C_Cr_{oL}\left(R_F+R_C\right)} \quad (C.27)$$

$$\omega_{P3}\approx -\frac{E}{F} \quad (C.28)$$

$$\approx -\frac{\begin{array}{l} C_{oC}C_{oD}r_{oC}r_{oD}R_F + C_{oC}C_{oL}r_{oC}r_{oL}R_F + C_{oC}C_{oL}r_{oC}r_{oD}r_{oL} + C_{oC}C_Cr_{oC}R_CR_F + C_{oC}C_Cr_{oC}r_{oD}R_C + C_{oC}C_Cr_{oC}r_{oD}R_F \\ +C_{oD}C_{oL}r_{oD}r_{oL}R_F + C_{oD}C_{oL}r_{oC}r_{oD}r_{oL} + C_{oD}C_Cr_{oD}R_CR_F + C_{oD}C_Cr_{oC}r_{oD}R_C + C_{oD}C_Cr_{oC}r_{oD}R_F + g_{m5}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_C \\ +g_{m5}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_F + C_{oL}C_Cr_{oL}R_CR_F + C_{oL}C_Cr_{oC}r_{oL}R_C + C_{o3}C_Cr_{o1}r_{o3}R_F + C_{o3}C_Cr_{o2}r_{o3}R_C + C_{oL}C_Cr_{oD}r_{oL}R_F \end{array}}{\begin{array}{l} C_{oC}C_{oD}C_{oL}r_{oC}r_{oD}r_{oL}R_F + C_{oC}C_{oD}C_Cr_{oC}r_{oD}R_CR_F + C_{oC}C_{oL}C_Cr_{oC}r_{oL}R_CR_F + C_{oC}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_C \\ +C_{oC}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_F + C_{oD}C_{oL}C_Cr_{oD}r_{oL}R_CR_F + C_{oD}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_C + C_{oD}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_F \end{array}} \quad \text{(C.29)}$$

$$\approx -\frac{\begin{array}{l} C_{oC}C_{oL}r_{oC}r_{oL}\left(R_F + r_{oD}\right) + C_CR_CR_F\left(C_{oC}r_{oC} + C_{oL}r_{oL}\right) + C_{oD}C_{oL}r_{oD}r_{oL}\left(R_F + r_{oC}\right) \\ +C_{oD}C_Cr_{oD}R_CR_F + C_{oC}C_{oD}r_{oC}r_{oD}R_F \\ +\left(R_F + R_C\right)\left(g_{m5}C_{oL}C_Cr_{oC}r_{oD}r_{oL} + C_{oL}C_Cr_{oC}r_{oL} + C_{oL}C_Cr_{oD}r_{oL} + C_{oD}C_Cr_{oC}r_{oD} + C_{oC}C_Cr_{oC}r_{oD}\right) \end{array}}{\begin{array}{l} C_{oC}C_{oD}r_{oC}r_{oD}R_F\left(C_{oL}r_{oL} + C_CR_C\right) + C_{oL}C_Cr_{oL}R_CR_F\left(C_{oC}r_{oC} + C_{oD}r_{oD}\right) \\ +C_{oL}C_Cr_{oC}r_{oD}r_{oL}\left(C_{oC} + C_{oD}\right)\left(R_F + R_C\right) \end{array}} \quad \text{(C.30)}$$

$$\approx -\frac{\left(R_F + R_C\right)\left(g_{m5}C_{oL}C_Cr_{oC}r_{oD}r_{oL} + C_{oL}C_Cr_{oC}r_{oL} + C_{oL}C_Cr_{oD}r_{oL} + C_{oD}C_Cr_{oC}r_{oD} + C_{oC}C_Cr_{oC}r_{oD}\right)}{\begin{array}{l} C_{oC}C_{oD}r_{oC}r_{oD}R_F\left(C_{oL}r_{oL} + C_CR_C\right) + C_{oL}C_Cr_{oL}R_CR_F\left(C_{oC}r_{oC} + C_{oD}r_{oD}\right) \\ +C_{oL}C_Cr_{oC}r_{oD}r_{oL}\left(C_{oC} + C_{oD}\right)\left(R_F + R_C\right) \end{array}} \quad \text{(C.31)}$$

$$\approx -\frac{g_{m5}C_{oL}C_Cr_{oC}r_{oD}r_{oL}\left(R_F + R_C\right)}{C_{oL}C_Cr_{oC}r_{oD}r_{oL}\left(C_{oC} + C_{oD}\right)\left(R_F + R_C\right)} \quad \text{(C.32)}$$

$$\omega_{P3} \approx -\frac{g_{m5}}{\left(C_{oC} + C_{oD}\right)} \quad \text{(C.33)}$$

$$\omega_{P4} \approx -\frac{F}{G} \quad \text{(C.34)}$$

$$\approx -\frac{\begin{array}{l} C_{oC}C_{oD}C_{oL}r_{oC}r_{oD}r_{oL}R_F + C_{oC}C_{oD}C_Cr_{oC}r_{oD}R_CR_F + C_{oC}C_{oL}C_Cr_{oC}r_{oL}R_CR_F + C_{oC}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_C \\ +C_{oC}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_F + C_{oD}C_{oL}C_Cr_{oD}r_{oL}R_CR_F + C_{oD}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_C + C_{oD}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_F \end{array}}{C_{oC}C_{oD}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_FR_C} \quad \text{(C.35)}$$

$$\approx -\frac{C_{oC}C_{oD}r_{oC}r_{oD}R_F\left(C_{oL}r_{oL} + C_CR_C\right) + C_{oL}C_Cr_{oL}R_CR_F\left(C_{oC}r_{oC} + C_{oD}r_{oD}\right) + C_{oL}C_Cr_{oC}r_{oD}r_{oL}\left(C_{oC} + C_{oD}\right)\left(R_F + R_C\right)}{C_{oC}C_{oD}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_FR_C} \quad \text{(C.36)}$$

$$\approx -\frac{C_{oC}C_{oD}r_{oC}r_{oD}R_F\left(C_{oL}r_{oL} + C_CR_C\right) + C_{oL}C_Cr_{oL}\left(R_CR_F\left(C_{oC}r_{oC} + C_{oD}r_{oD}\right) + r_{oC}r_{oD}\left(C_{oC} + C_{oD}\right)\left(R_F + R_C\right)\right)}{C_{oC}C_{oD}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_FR_C} \quad \text{(C.37)}$$

$$\approx -\frac{C_{oC}C_{oD}C_{oL}r_{oC}r_{oD}r_{oL}R_F + C_{oL}C_Cr_{oL}\left(R_CR_F\left(C_{oC}r_{oC} + C_{oD}r_{oD}\right) + r_{oC}r_{oD}\left(C_{oC} + C_{oD}\right)\left(R_F + R_C\right)\right)}{C_{oC}C_{oD}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_FR_C} \quad \text{(C.38)}$$

$$\approx -\frac{C_{oC}C_{oD}C_{oL}r_{oC}r_{oD}r_{oL}R_F + C_{oL}C_Cr_{oL}R_F\left(R_C\left(C_{oC}r_{oC} + C_{oD}r_{oD}\right) + r_{oC}r_{oD}\left(C_{oC} + C_{oD}\right)\right)}{C_{oC}C_{oD}C_{oL}C_Cr_{oC}r_{oD}r_{oL}R_FR_C} \quad \text{(C.39)}$$

$$\approx -\frac{C_{oC}C_{oD}C_{oL}r_{oC}r_{oD}r_{oL}R_F + C_{oL}C_C r_{oC}r_{oD}r_{oL}R_F\left(C_{oC}+C_{oD}\right)}{C_{oC}C_{oD}C_{oL}C_C r_{oC}r_{oD}r_{oL}R_F R_C} \tag{C.40}$$

$$\approx -\frac{C_{oL}r_{oC}r_{oD}r_{oL}R_F\left(C_{oC}C_{oD}+C_C\left(C_{oC}+C_{oD}\right)\right)}{C_{oC}C_{oD}C_{oL}C_C r_{oC}r_{oD}r_{oL}R_F R_C} \tag{C.41}$$

$$\omega_{P4} \approx -\frac{C_{oC}C_{oD}+C_C\left(C_{oC}+C_{oD}\right)}{C_{oC}C_{oD}C_C R_C} \tag{C.42}$$

The transfer function of CMFB is

$$A_{CMFB}(s) = \frac{A_{CMFB}(0)\left(1+\frac{s}{\omega_{Z1}}\right)}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)\left(1+\frac{s}{\omega_{P3}}\right)\left(1+\frac{s}{\omega_{P4}}\right)} \tag{C.43}$$

where the DC open-loop CMFB gain is equal to

$$A_{CMFB}(0) = \frac{\frac{2\beta}{R}g_{mb1}r_{oC}r_{oD}r_{oL}\left(1-g_{m5}R_F\right)}{g_{m5}r_{oC}r_{oD}+r_{oC}+r_{oD}+R_F} \approx -\frac{2\beta}{R}g_{mb1}r_{oL}R_F \tag{C.44}$$

From Eqs. (C.20) and (C.44), the gain bandwidth product (*GBW*) is

$$GBW = A_{CMFB}(0)\cdot\omega_{P1} = \frac{2\beta g_{mb1P}r_{oL}R_F}{R}\cdot\frac{1}{r_{oL}C_{oL}+C_C\left(R_C+R_F\right)} \tag{C.45}$$

Since $\omega_{P3}$ and $\omega_{P4}$ are far away from the unity-gain frequency, the overall phase margin can be determined as

$$PM \approx 180° - tan^{-1}\left(\frac{GBW}{\omega_{P1}}\right) - tan^{-1}\left(\frac{GBW}{\omega_{P2}}\right) + tan^{-1}\left(\frac{GBW}{\omega_{Z1}}\right) \tag{C.46}$$

According to Eq. (C.46), the left half-plane zero $\omega_{Z1}$ will add positive phase margin to the frequency response of the CMFB.

# APPENDIX D
# NOISE ANALYSIS OF THE PDA

The voltage and current thermal noises of resistor ($R$) are

$$\overline{v_n^2} = 4kTR \tag{D.1}$$

$$\overline{i_n^2} = \frac{4kT}{R} \tag{D.2}$$

The flicker noise (1/f) at low frequency and thermal noise at high frequency of the transistor are

-Flicker Noise (1/f)

$$\overline{v_n^2} = \frac{K_f}{C_{OX}WL}\cdot\frac{1}{f} \tag{D.3}$$

-Thermal Noise

$$\overline{i_n^2} = 4kT\gamma g_m \cong 4kT\frac{2}{3}g_m \tag{D.4}$$

The open loop gain of the PDA is

$$A_V = \left(g_{m1N} + g_{m1P} + g_{m8N} + g_{m8P}\right)\left(r_{oN} \| r_{oP}\right) \tag{D.5}$$

By using (D.1)-(D.4), the thermal output noise of the circuit shown in Figure D.1 is

$$\overline{v_{o1}^2} = \frac{8}{3}kT\left(g_{m1N} + g_{m1P} + g_{m8N} + g_{m8P}\right)\left(r_{oN} \| r_{oP}\right)^2 + \frac{4kT}{R}\left(r_{oN} \| r_{oP}\right)^2 \tag{D.6}$$

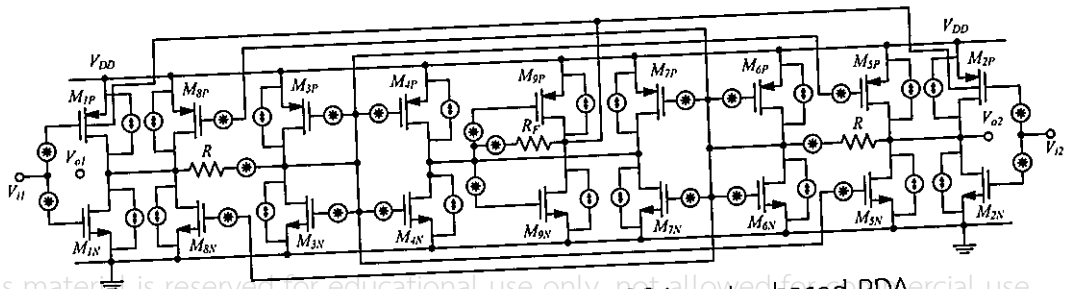



Figure D.1 Noise analysis of the CMOS inverter-based PDA

We can find the input referred noise spectral density of the PDA as

$$\overline{V_{in,th}^2} = \frac{2}{A_V^2}\left(\frac{8}{3}kT\left(g_{m1N}+g_{m1P}+g_{m8N}+g_{m8P}\right)\left(r_{oN}\parallel r_{oP}\right)^2+\frac{4kT}{R}\left(r_{oN}\parallel r_{oP}\right)^2\right) \quad \text{(D.7)}$$

By substituting equation (D.5) into (D.7), the input referred thermal noise can be expressed as

$$\overline{V_{in,th}^2} = \frac{2}{\left(g_{mN}+g_{mP}\right)^2\left(r_{oN}\parallel r_{oP}\right)^2}\left(\frac{8}{3}kT\left(g_{m1N}+g_{m1P}+g_{m8N}+g_{m8P}\right)\left(r_{oN}\parallel r_{oP}\right)^2+\frac{4kT}{R}\left(r_{oN}\parallel r_{oP}\right)^2\right) \quad \text{(D.8)}$$

$$\overline{V_{in,th}^2} = \frac{2}{\left(g_{m1N}+g_{m1P}\right)^2}\left(\frac{8}{3}kT\left(g_{m1N}+g_{m1P}+g_{m8N}+g_{m8P}\right)+\frac{4KT}{R}\right) \quad \text{(D.9)}$$

The input referred flicker noise is

$$\overline{V_{in(1/f)}^2} = 2\left(\frac{K_f}{C_{OX}\left(WL\right)_N}\cdot\frac{1}{f}+\frac{K_f}{C_{OX}\left(WL\right)_P}\cdot\frac{1}{f}\right) \quad \text{(D.10)}$$

The total input referred noise of the PDA is determined by

$$\overline{V_n^2} \approx \overline{V_{n,(1/f)}^2}+\overline{V_{n,th}^2} \quad \text{(D.11)}$$

$$\overline{V_{in}^2} = 2\left[\frac{1}{\left(g_{m1N}+g_{m1P}\right)^2}\left(\frac{8}{3}kT\left(g_{m1N}+g_{m1P}+g_{m8N}+g_{m8P}\right)+\frac{4KT}{R}\right)+\frac{K_f}{C_{OX}\left(WL\right)_{1N}}\cdot\frac{1}{f}+\frac{K_f}{C_{OX}\left(WL\right)_{1P}}\cdot\frac{1}{f}\right] \quad \text{(D.12)}$$

# APPENDIX E
# TRANSFER FUNCTION OF THE BANDPASS-BASED OSCILLATOR

Figure E.1 shows the block diagram of a single-ended version of the proposed oscillator. The open loop gain is determined by

$$A(0)=\frac{i_{in}}{v_{out}}=G_m \tag{E.1}$$

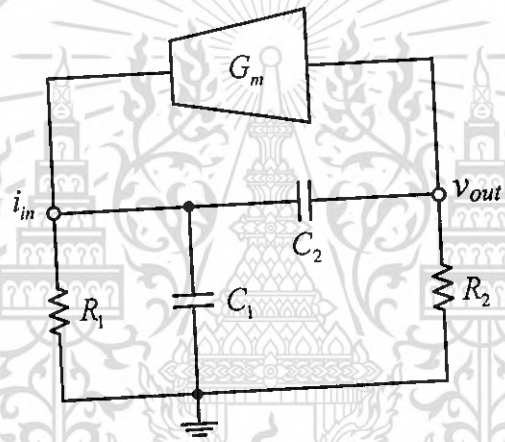



Figure E.1 Basic structure of proposed oscillator

The transfer function of the band pass filter (BPF) is

$$B(s)=\frac{v_{out}}{i_{in}}=\frac{\frac{1}{C_1}s}{s^2+\frac{1+C_1/C_2+R_2/R_1}{R_2C_1}s+\frac{1}{R_1C_1R_2C_2}} \tag{E.2}$$

The loop gain according to Barkhausen Criterion has to be equal to one:

$$A.B=\frac{\frac{G_m}{C_1}s}{s^2+\frac{1+C_1/C_2+R_2/R_1}{R_2C_1}s+\frac{1}{R_1C_1R_2C_2}}=1 \tag{E.3}$$

The oscillation frequency ($\omega_o$) is given by

$$(j\omega_o)^2 + \frac{1}{R_1 C_1 R_2 C_2} = 0 \tag{E.4}$$

$$-\omega_o^2 + \frac{1}{R_1 C_1 R_2 C_2} = 0 \tag{E.5}$$

$$\omega_o = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}} \tag{E.6}$$

The transconductance ($G_m$) has to meet the following condition:

$$\frac{G_m}{C_1} s \geq \frac{1 + C_1/C_2 + R_2/R_1}{R_2 C_1} s \tag{E.7}$$

$$G_m \geq \frac{1 + C_1/C_2 + R_2/R_1}{R_2} \tag{E.8}$$

# APPENDIX F
# TRANSFER FUNCTION OF THE MFB FILTER

From Figure F.1, summing the currents at node $V_x$ gives

$$I_1 = Y_1(V_i - V_x) = I_2 + I_3 + I_4 = Y_2V_x + Y_3V_x + Y_4(V_x - V_o) \quad \text{(F.1)}$$

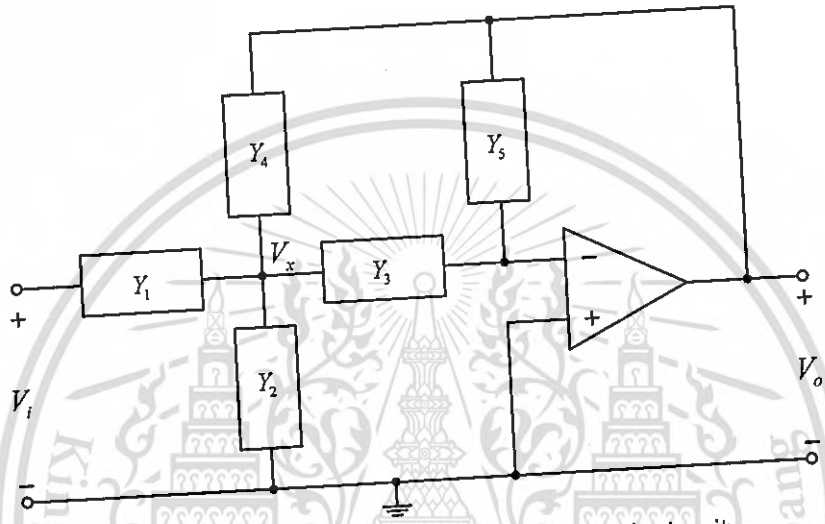



Figure F.1 Generalised multiple feedback circuit

Re-arranging (F.1) leads to

$$Y_1V_i = V_x(Y_1 + Y_2 + Y_3 + Y_4) - Y_4V_o \quad \text{(F.2)}$$

and

$$Y_3V_x = -Y_5V_o \quad \text{(F.3)}$$

$$V_x = -\frac{Y_5}{Y_3}V_o \quad \text{(F.4)}$$

$$Y_1Y_3V_i = V_o\left[-Y_5(Y_1 + Y_2 + Y_3 + Y_4) - Y_3Y_4\right] \quad \text{(F.5)}$$

Rearranging equation (F.5) yields

$$\frac{V_o}{V_i} = \frac{-Y_1Y_3}{Y_5(Y_1 + Y_2 + Y_3 + Y_4) + Y_3Y_4} \quad \text{(F.6)}$$

Table F.1 summary of the passive components of MFB filter

| Filter Types | Passive Components (Z=1/Y) | | | | |
|---|---|---|---|---|---|
| | $Z_1$ | $Z_2$ | $Z_3$ | $Z_4$ | $Z_5$ |
| LP | $R_1$ | $C_2$ | $R_3$ | $R_4$ | $C_5$ |
| HP | $C_1$ | $R_2$ | $C_3$ | $C_4$ | $R_5$ |
| BP | $R_1$ | $R_2$ | $C_3$ | $C_4$ | $R_5$ |

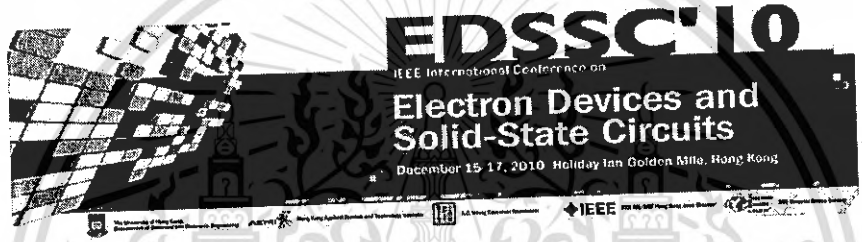
# APPENDIX G
# LIST OF PUBLICATIONS

1. Apirak Suadet and Varakorn Kasemsuwan "A CMOS Inverter-Based Class-AB Pseudo Differential Amplifier for HF Applications", in proceedings of the 2010 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC'10), pp.1-4, 2010.

2. Apirak Suadet, Thawatchai Thongleam, Varakorn Kasemsuwan, Kasin Vichienchom, "A 0.5 V volt rail-to-rail CMOS pseudo-differential OTA using simple feed-forward technique", in proceedings of the 2010 International Conference on Electrical Engineering/Electronics,Computer, Telecommunications and Information Technology (ECTI-CON'11), pp. 106-109, 2011.

3. Apirak Suadet and Varakorn Kasemsuwan, "A Current-Mode Common-Mode Feedback Circuit (CMFB) with Rail-to-Rail Operation", Journal of RF-Engineering and Telecommunications (FREQUENZ), vol. 65, pp.47-54, 2011. (ISSN 0016-1136, IF2016=0.462)

4. Apirak Suadet and Varakorn Kasemsuwan, "A CMOS inverter-based class-AB pseudo-Differential amplifier with current-mode common-mode feedback (CMFB)", Analog Integrated Circuits and Signal Processing, vol. 74, pp. 387-398, 2013. (ISSN 0925-1030, IF2016=0.623)



2010 IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC)

# A CMOS Inverter-Based Class-AB Pseudo Differential Amplifier for HF Applications

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*Abstract*— **This paper presents a CMOS inverter-based class-AB pseudo differential amplifier for HF applications using new simple rail-to-rail CMFB circuit. The proposed circuit employs two CMOS inverters and the complementary common-mode feedback (CMFB) consisting of current mode common-mode detector and transimpedance amplifiers. The circuit has been designed using 0.18 $\mu$m CMOS technology under 1 V supply, and the simulation results shows that the rail to rail output swing is achieved with low common-mode gain (-15 dB). The output swing of the circuit is 0.7 V. The power dissipation of the circuit is 96 $\mu$W.**

***Keywords-pseudo-differential amplifier; common-mode feedback; class-AB; CMOS inverter***

## I. INTRODUCTION

Nowadays, a high performance analog circuit using low voltage becomes essential mainly due to the advance of the large scale integration with complicated circuit systems and the demand for battery-operated portable equipments. However, supply voltage reduction in analog circuit causes several performance degradations and, therefore, new approaches in the design are needed to obtain analog circuits with enough bandwidth, gain and linearity.

Operational transconductance amplifier (OTA) is one of the most basic cells as OTA finds many applications in many analog circuits such as operational amplifier, voltage comparators, A-D and D-A converters and high frequency filters. Several approaches have been proposed to design low voltage OTA [1-14] using both fully differential (FD) and pseudo-differential (PD) configurations. FD is typically based on a differential pair with a tail current source while PD is based on two independent inverters without tail current source. It is known that avoiding the voltage drop across the tail current source, in a PD structure, allows wider input and output ranges, and makes the architecture attractive for low power-supply applications. However, PD structure requires an extra common-mode feedback (CMFB) circuit, which serves two purposes: 1) to fix the common-mode voltage at high impedance nodes and 2) to suppress the common-mode signal components. Several approaches have been proposed to achieve CMFB [1-10]. Switched-capacitor circuit was proposed to build a CMFB [1], and the resulting circuit shows small power consumption. However, the CMFB circuits introduces clock-feed through error and load capacitance, [2-3] used simple resistive divider to sense the voltage of two differential nodes. As a result, the voltage swing of the CMFB is not limited. However, not only do these resistors require large silicon area, they load down the output impedances. [4] used MOS resistive network with bulk-driven CMFB technique. However, the circuit has quite low output impedance and high common gain. To solve the problem, methods of employing MOS transistor as CMFB circuit have been proposed [5-6]. The CMFB consists of CM detector and one stage amplifier. As a result, the common-mode gains are quite high and, in addition, the output swings are limited. [7-8] employs transistors with two stage common-mode amplifiers. The resulting common-mode gain is low. The problem with this structure is that the circuit has limited output swing and potential oscillation problem. [9-10] proposed the complementary CMFB, which can achieve both low common-mode gains with good output swings. However, the circuits are complex and show high power consumption. [11-12] proposed positive feedback technique to increase the differential gain. However, the circuit shows quite high common-mode gain ($A_{cm} \cong -6$ dB).

In this paper, a CMOS inverter-based class-AB pseudo differential amplifier (PDA) using a new common-mode feedback (CMFB) is proposed. The CMFB consists of a current mirror (CM) and transimpedance amplifier (TA). The common-mode gain is found to be low (-15 dB). The positive feedback is also employed to increase the differential-mode gain. The output swing of the circuit is 0.7 V.

## II. THE PROPOSED PSEUDO-DIFFERENTIAL AMPLIFIER

### A. Conventional Class-AB OTA

A conventional class-AB OTA is shown in Fig. 1(a). As seen, the circuit is based on CMOS inverter. It is well known that CMOS inverter has high gain and less power consumption. In addition, it contains no internal nodes and, as a result, the performance of the circuit will not be much degraded by the extra parasitic poles at high frequency.

The PD structure using CMOS inverter is shown in Fig. 1(b). It can be easily seen that the differential-mode gain ($A_{dm}$) is the same as the common-mode gain ($A_{cm}$), resulting in the unity common-mode rejection ratio ($CMRR=A_{dm}/A_{cm}$). Since



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large $A_{cm}$ can lead to large common-mode variation at the output [13], therefore common-mode feedback (CMFB) circuit is required.

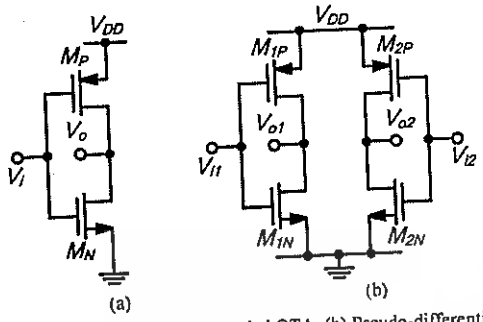


Figure 1. (a) Inverter-based single-ended OTA (b) Pseudo-differential OTA.

### B. *The Proposed PDA Structure*

The proposed PDA is based on the configuration shown in Fig. 2(a). As seen, PDA consists of the two independent CMOS inverters ($M_{1N,P}$ -$M_{2N,P}$) and common-mode amplifier (CMA), which serves two purposes: 1) to detect the common-mode signal at the output nodes ($V_{o1}$ and $V_{o2}$), and 2) to provide positive feedback (see dash line) to enhance the output impedance and differential gain.

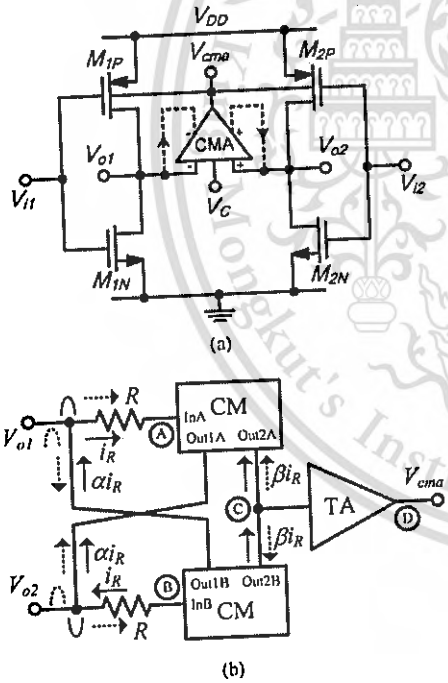


Figure 2. The proposed PDA (a) Circuit configuration (b) Structure of CMA.

The operation can be explained as follows. In case of the common-mode output signal ($V_{o1,2}$=$V_{oc}$), CMA will amplify $V_{o1,2}$ and negatively fed back the result ($V_{cma}$) to the bulk terminals of $M_{1P,2P}$ such that the common-mode output voltage is suppressed. On the contrary, CMA will not respond to the differential-mode signal ($V_{o1}$= $-V_{o2}$), namely, the output of CMA ($V_{cma}$) stays constant. The DC common-mode voltage is set by $V_C$. It is noted that the common-mode gain can be further suppressed if $V_{cma}$ is also fed back to the bulk terminals of $M_{1N,2N}$. This can be made possible in the triple-well process.

Fig. 2(b). illustrates the architecture of the proposed CMA. As seen, CMA consists of two matched resistors ($R$), two current mirrors (CM) and transimpedance amplifier (TA). The operation of the CMA can be explained as follows. When the output voltages from PDA are differential signals (see solid signal), these voltages are converted to the currents through resistors $R$. These currents, which have the same magnitude but opposite phase, flow to each resistor and are mirrored to the $Out_{2A}$ and $Out_{2B}$ terminals (with the current gain of $\beta$). Because these currents have the same magnitude but opposite phase, there will be no input current flowing into the transimpedance amplifier (TA) and, thus no voltage variation at node C. In addition, the currents through resistors $R$ are mirrored to the $Out_{1A}$ and $Out_{1B}$ terminals (with the current gain of $\alpha$), and positively fed back to the output of the PDA, thus enhancing the output impedance (at nodes $V_{o1}$ and $V_{o2}$) and differential gain of the system.

When the outputs from PDA are common-mode signals (see dotted line), the common-mode current flows through nodes A and B with the same amplitude and phase. As a result, the summation of these two currents are added constructively and passed to transimpedance amplifier (TA). The amplified output voltage $V_{cma}$ is negatively fed back to the bulk terminals of $M_{1P,2P}$ to suppress the common-mode voltage, as discussed previously.

Straight forward small signal analysis shows that $A_{dm}$ and $A_{cm}$ can be derived and shown as

$$A_{dm} = -G_{M(IN)}\left[\frac{Z_{out}}{1+(1-\alpha)Z_{out}/R}\right] \quad (1)$$

$$A_{cm} = -G_{M(IN)}\left[\frac{Z_{out}}{1+(1+\alpha-2g_{mb}\beta R_F)Z_{out}/R}\right] \quad (2)$$

where $G_{M(IN)}$ is the transconductance of the CMOS inverter ($G_{M(IN)}$=$g_{mIN,2N}$+$g_{mIP,2P}$), $Z_{out}$ is the output impedance of the PDA ($Z_{out}$=$r_{OIN,2N}$//$r_{OIP,2P}$), $\alpha$ and $\beta$ are the current gains of the current mirror (CM), $g_{mb}$ is the bulk transconductance of $M_{1P,2P}$, and $R_F$ is the transimpedance gain of the transimpednace amplifier (TA).

From Eqs. (1) and (2), one can find the common-mode rejection ratio as

$$CMRR = \frac{A_{dm}}{A_{cm}} = \left[\frac{1+(1+\alpha-2g_{mb}\beta R_F)Z_{out}/R}{1+(1-\alpha)Z_{out}/R}\right] \quad (3)$$

From Eq. (3), one can notice that CMRR can be increased if the transimpedance gain ($R_F$) is large. In addition, the current gain $\alpha$ and $\beta$ of current mirrors A and B also play roles in determining the *CMRR*.

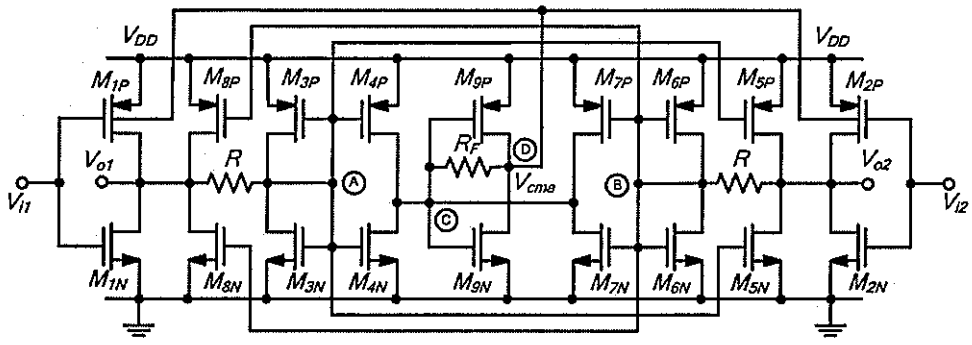


Figure 3. The proposed class-AB pseudo-differential amplifier (PDA).

### C. *Circuit Implementation*

The circuit implementation of Fig. 2 is illustrated in Fig. 3. $M_{1N,P}$-$M_{2N,P}$ consist to be the input pseudo-differential amplifier, while $M_{3N,P}$-$M_{9N,P}$ consist to be a wide swing CMFB circuit. $M_{3N,P}$-$M_{5N,P}$ form the current mirror A while $M_{6N,P}$-$M_{8N,P}$ are used to form the current mirror B. The current gain with the ratios of $\alpha$ and $\beta$ can be achieved by adjusting the aspect rations of $M_{3N,P}$, $M_{5N,P}$ ($M_{6N,P}$, $M_{8N,P}$) and $M_{3N,P}$, $M_{4N,P}$ ($M_{6N,P}$, $M_{7N,P}$), respectively.

It is noted that the choice of $\alpha$ requires precaution. A large value of $\alpha$ can result in a large differential gain. However, large value of $\alpha$ can drive the circuit unstable. In practice, $\alpha$ should be set a little bit larger than one to compensate for the loss, due to the imperfection of the current mirror not being able to perfectly mirror the current from the input to the output. In this work, $\alpha$ is set to 1.3 to enjoy both differential gain and stability. The value of $\beta$ plays role in determining the common-mode gain, because it is part of the CMFB circuit. As seen in Eq. (2), large value of $\beta$ results in low common-mode gain. However, it is noted that large $\beta$ requires large transistors, thus large standby current and parasitic capacitors, which can degrade frequency performance of the system. In this work, $\beta$ is set to 3.

Transistor $M_{9N,P}$ and $R_F$ consist to be the transimpedance amplifier (TA). The transimpedance gain of the circuit is set by the resistor $R_F$. The transimpedance amplifier is employed here to enhance the gain of the common-mode amplifier (CMA) and, at the same time, to reduce both input and output impedances (at nodes C and D), so that the time constants associated with these nodes are low.

The dc common-mode voltage level ($V_C$) is equal to the voltages at nodes A and B, which is given by [14]

$$V_C = \frac{V_{DD} - V_{TN(3N,6N)} + V_{TP(3P,6P)}}{1+\sqrt{\beta_{N(3N,6N)}/\beta_{P(3P,6P)}}} + V_{TN(3N,6N)} \qquad (4)$$

where $\beta_{N(3N,6N)}=\mu_n C_{OX}(W/L)_{3N,6N}$ and $\beta_{P(3P,6P)}=\mu_P C_{OX}(W/L)_{3P,6P}$

For maximum output swing, we have set $\beta_{N(3N,6N)}$ and $\beta_{P(3P,6P)}$ such that $V_C$ is equal to $V_{DD}/2$.

## III. Simulation Results

To verify the circuit performance, Spectre is used to simulate the proposed circuit, using a 0.18 $\mu$m CMOS process under the supply voltage of 1 V. In this work, the bias currents of all transistors are chosen to optimize both gain and power dissipation.

Fig. 4 shows the DC transfer characteristic of the proposed PDA. As seen, the output swing shows rail-to-rail operation. Fig. 5 shows the transient response of the output voltages for both differential-mode ($V_{o1}$, $V_{o2}$) and common-mode ($V_{oc}$), when the input signals are differential and common-mode voltages with the amplitude of 10 $mV_{pp}$ at 10 kHz. As seen, the differential-mode output voltage reads 0.7 $V_{pp}$, while the common-mode output voltage reads only 0.4 $mV_{pp}$.

Fig. 6 shows the frequency response of the proposed PDA in case of the differential-mode input signal. The DC gain is found to be 36 dB, while the –3 dB and unity gain frequency are 8.5 MHz and 800 MHz, respectively. The phase margin is 85°. Fig. 7 shows the frequency response of the PDA in case of the common-mode input signal. As seen, the common-mode gain is relatively much smaller (-15 dB), while the bandwidth is almost the same as in the differential-mode case. The power dissipation of the proposed PDA is 96 µW.

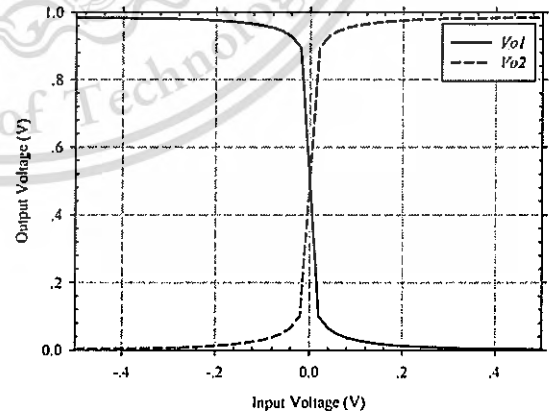


Figure 4. DC transfer characteristic.

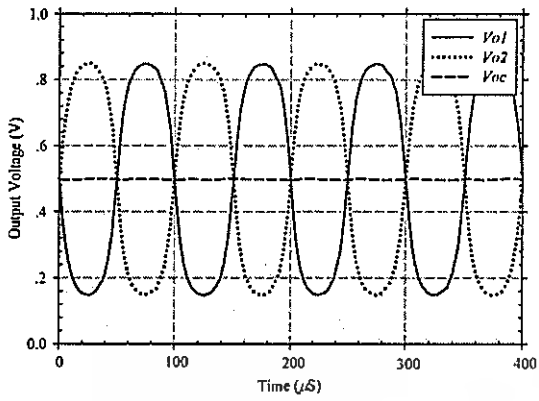


Figure 5. Differential and common-mode output voltages.

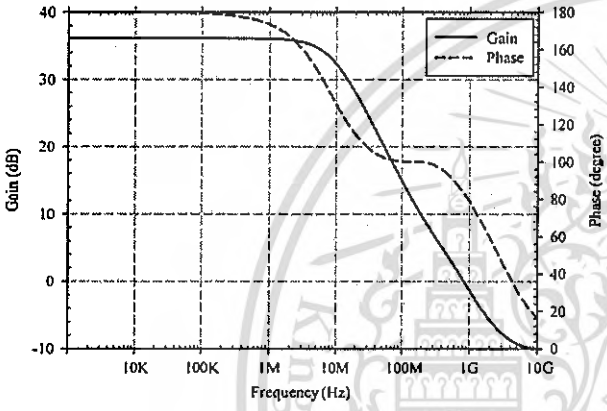


Figure 6. Differential-mode gain and phase margin.

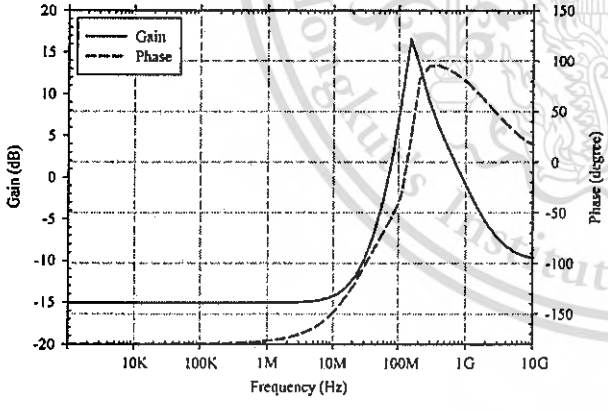


Figure 7. Common-mode gain and phase margin.

## IV. Conclusions

In this paper, a CMOS inverter-based class-AB pseudo differential amplifier for HF applications is proposed. The circuit is based on CMOS inverter, and low-voltage wide-swing CMFB circuit. The proposed PDA has been designed using 0.18 $\mu$m CMOS process. The simulation results show that the circuit can operate under the supply voltage of 1 V with the differential and common-mode gains of 36 dB and -15 dB, respectively. The unity gain frequency is 800 MHz, and the power dissipation is 96 $\mu$W.

## Acknowledgment

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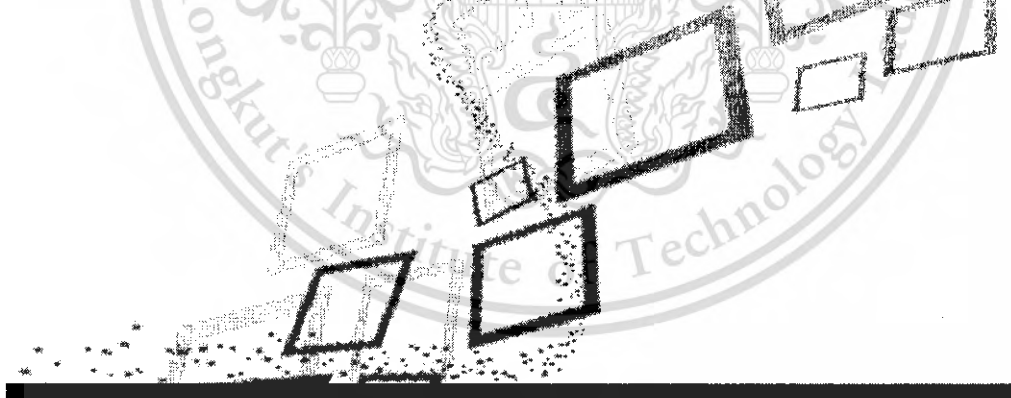

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# A 0.5 Volt Rail-to-Rail CMOS Pseudo-Differential OTA Using Simple Feed-forward Technique

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***Abstract*- This paper presents a low voltage CMOS pseudo differential OTA using simple feed-forward technique. The circuit employs feed-forward technique to suppress the common-mode gain, and positive feedback to enhance the output impedance. The circuit is designed using 0.18 $\mu$m CMOS technology under 0.5 V supply. The simulation results show rail-to-rail input/output swing, achieved with low common-mode gain (-35 dB). The output swing of the circuit is 0.3 Vpp. The power dissipation of the circuit is 50 $\mu$W.**

## I. INTRODUCTION

In recent years, the scaling of CMOS technologies as well as the increasing use of portable equipments has forced the reduction of the supply voltage to subvolt regime. The analog circuitry must be adapted in order to operate under such stringent conditions in order not to degrade the signal-to-noise ratio (SNR). It is well known that supply voltage reduction in analog circuitry causes several performance degradations and, therefore, new approaches in the design are needed to achieve enough bandwidth, gain and good linearity.

Operational transconductance amplifier (OTA) is one of the most basic cells as OTA finds many applications in many analog circuits such as operational amplifier, continuous-time $G_m$-C filters, oscillators and data converters. There have been several proposed circuit techniques to realize OTA [1]-[14] using both fully differential (FD) and pseudo-differential (PD) configurations. FD is typically based on a differential pair with a tail current source while PD is based on two independent inverters without tail current source. It is known that avoiding the voltage drop across the tail current source, in a PD structure, allows wider input and output swings, making the structure attractive for low voltage applications. However, PD structure requires an extra common-mode feedback (CMFB) circuit to suppress the common-mode signal, thus degrading the PD performance, since CMFB behaves as an additional load. Furthermore, CMFB circuit has to be carefully designed to avoid stability problems, resulting in complex circuitry and more power consumption. Another alternative is to use common-mode feed-forward (CMFF) technique [1-2]. Although CMFF fails to fix the DC output voltage [3], stable DC output voltage can still be obtained for the OTA configured in the cascade configuration, e. g. filter, where the DC output voltage is set by the input common-mode level of next stage. [4] proposed the feed-forward technique, which achieved enhanced differential-mode gain and suppressed common-mode gain. However, the circuit has limited input common-mode range and low cutoff frequency operated in weak inversion.

Several techniques have been proposed to achieve OTA with rail-to-rail operation. The N-P differential pairs are employed [5]. However, this approach is restricted for supply voltages greater than two threshold voltages. The dynamic level shifters have been proposed to provide a rail-to-rail operation at low supply voltage [6]. Unfortunately, this approach requires complicated circuit, which then increases the silicon area and power consumption. [7] proposed the transconductor with resistor input technique. Although the circuit achieved rail-to-rail input swing, the input impedance was quite low, and depended on the resistor employed.

The use of bulk-driven MOS transistors in the input stage was proposed as a useful alternative to design amplifiers able to operate with a supply voltage in the order of the threshold voltage [8-10]. In this manner, the threshold voltage of a MOSFET can be removed from the signal path, and rail-to-rail operation can be achieved. The main drawback of bulk-driven method is the bulk transconductance ($g_{mb}$), which is 4 to 5 times smaller than the gate transconductance ($g_m$), resulting in relatively low DC gain and higher input referred noise [11]. Furthermore, a quasi floating gate (QFG) technique has also been employed to design amplifiers. In this technique, input signal is capacitively coupled to the transistor gate, while a very large-valued resistor weakly connects this gate to one of the supply rails. As a result, the dc gate-source voltage is set to the supply voltage, thus enabling the QFG circuit to operate under a low voltage environment [12]-[13].

In this work, a low voltage pseudo differential OTA using a bulk-driven (BD) and quasi floating gate CMOS inverter (QFG-inverter) is proposed. The circuit uses novel feed-forward circuitry to simultaneously suppress common-mode signals and enhance the differential-mode signals. Positive feedback is employed to enhance the output impedance. The resulting circuit exhibits large input/output swing.

## II. THE PROPOSED PSEUDO-DIFFERENTIAL OTA

### *A. Bulk Input Pseudo-Differential OTA*

A basic low voltage bulk input PD-OTA is shown in Fig. 1. As seen, the circuit consists of two independent bulk input PMOS transistors ($M_{1P}$ and $M_{2P}$) and two active load NMOS transistors ($M_{1N}$ and $M_{2N}$). Rail-to-rail input swing is achieved

as long as the value of the forward current through the bulk terminal is maintained at a low level. The minimum supply voltage of the circuit is approximately equal to the threshold voltage of the MOSFET employed.

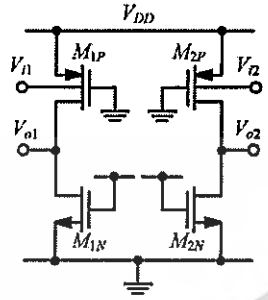


Figure 1. Basic bulk input PD-OTA.

### B. Proposed PD-OTA Structure

From Fig. 1, it can be easily seen that the differential-mode gain ($A_{dm}$) of the basic bulk input PD-OTA is the same as the common-mode gain ($A_{cm}$), making the circuit prone to interferences and supply noises [14]. To suppress the common-mode response, a newly developed feed-forward circuitry has been proposed as shown in Fig. 2. As seen, PD-OTA consists of two independent bulk-driven CMOS inverters ($M_{1(2)N}$ – $M_{1(2)P}$) and two feed-forward inverting attenuators (FFA) with an attenuation factor of $-\alpha$. The feed-forward attenuator serves two purposes: 1) to suppress the common-mode signals at the output nodes ($V_{o1}$ and $V_{o2}$), and 2) to enhance the differential transconductance ($G_{dm}$) of the system.

The operation can be explained as follows. In case of the common-mode input signals ($v_{i1,2}=v_{icm}$), FFA will attenuate $v_{i1,2}$ and negatively feed forward the attenuated signals to the gate terminals of $M_{1N(P)}$ and $M_{2N(P)}$. Since the input signals and attenuated signals have opposite phase, the common-mode output current is then suppressed. On the contrary, in case of the differential-mode signals ($v_{i1}=-v_{i2}$), the input signals at the bulk and attenuated signals at the gate are in phase, thereby increasing the differential-mode output currents and differential transconductance ($G_{dm}$).

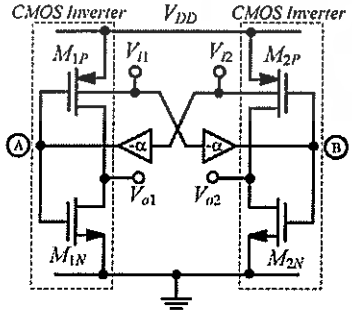


Figure 2. The proposed PD-OTA configuration.

From Fig. 2, the differential-mode transconductance ($G_{dm}$) and common-mode transconductance ($G_{cm}$) can be derived and shown as

$$G_{dm} = g_{mbP1(2)} + \alpha \cdot g_{m1(2)} \tag{1}$$

$$G_{cm} = g_{mbP1(2)} - \alpha \cdot g_{m1(2)} \tag{2}$$

where $g_{mbP1(2)}$ is the bulk transconductance of $M_{1P(2P)}$, $g_{m1(2)} = g_{mn1(2)}+g_{mp1(2)}$, $g_{mn1(2)}$ and $g_{mp1(2)}$ are the gate transconductance of $M_{1(2)N}$ and $M_{1(2)P}$, respectively.

From Eqs. (1) and (2), if $\alpha$ is set to $g_{mbP1(2)}/g_{m1(2)}$, $G_{dm}$ and $G_{cm}$ will be equal to $2g_{mbP1(2)}$ and zero, respectively.

### C. Circuit Implementation

The circuit implementation of the proposed OTA is illustrated in Fig. 3(a). As seen, the circuit consists of two bulk-input QFG-inverters ($M_{1A(B)N}$-$M_{1A(B)P}$) operating as PD-OTA, and feed-forward attenuator (FFA) ($M_{2A(B)N}$-$M_{2A(B)P}$) with an attenuation factor $\alpha$ of $g_{mb2A(B)P}/(g_{m2A(B)P}+g_{m2A(B)N})$. The dc operating point at the quasi-floating gate is set to $V_{B1}$ and $V_{B2}$ through large pull-up and pull-down resistors ($R_G$) realized by PMOS and NMOS operating in the cutoff region, respectively. Since $R_G$ is very large, the cutoff frequency can be very low (below 1 Hz) and, as a result, very low input frequency can be passed and processed by the QFG transistors.

The output impedance enhancement technique using positive feedback is shown in Fig. 3(b). As seen, the bulk inputs of transistors $M_{3AP}$ and $M_{3BP}$ form a cross coupled pair. The differential-mode ($Z_{O(dm)}$) and common-mode ($Z_{O(cm)}$) output impedances at the output nodes ($V_{o1}$ and $V_{o2}$) can be easily analyzed using straight forward small signal analysis and shown as

$$Z_{O(dm)} = \frac{1}{(Z_O \,//\, R_C)^{-1} - g_{mb3A(B)P}} \tag{3}$$

$$Z_{O(cm)} = \frac{1}{(Z_O \,//\, R_C)^{-1} + g_{mb3A(B)P}} \tag{4}$$

where $Z_O$ is $r_{O1A(B)P}//r_{O1A(B)N}//r_{O3A(B)P}//r_{O3A(B)N}$.

Similarly, the differential-mode transconductance ($G_{dm}$) and common-mode transconductance ($G_{cm}$) can be derived and shown as

$$G_{dm} = g_{mb1A(B)P} + g_{mb2A(B)P}\left(\frac{g_{m1A(B)P}+g_{m1A(B)N}}{g_{oA(B)}+g_{m2A(B)P}+g_{m2A(B)N}}\right) \tag{5}$$

$$G_{cm} = g_{mb1A(B)P} - g_{mb2A(B)P}\left(\frac{g_{m1A(B)P}+g_{m1A(B)N}}{g_{oA(B)}+g_{m2A(B)P}+g_{m2A(B)N}}\right) \tag{6}$$

where $g_{oA(B)}$ is $(r_{o2A(B)P}//r_{o2A(B)N})^{-1}$.

From Fig. 3, the bias voltage at the body terminal of $M_{1A(B)N}$ is zero, while the body bias voltage of $M_{1A(B)P}$ is set to $V_{DD}/2$ so as to maximize the input swing. The difference of the body voltages results in mismatch on the threshold voltages of $M_{1A(B)N}$ and $M_{1A(B)P}$, i.e., $V_{DD}/2$ causes the threshold voltage of

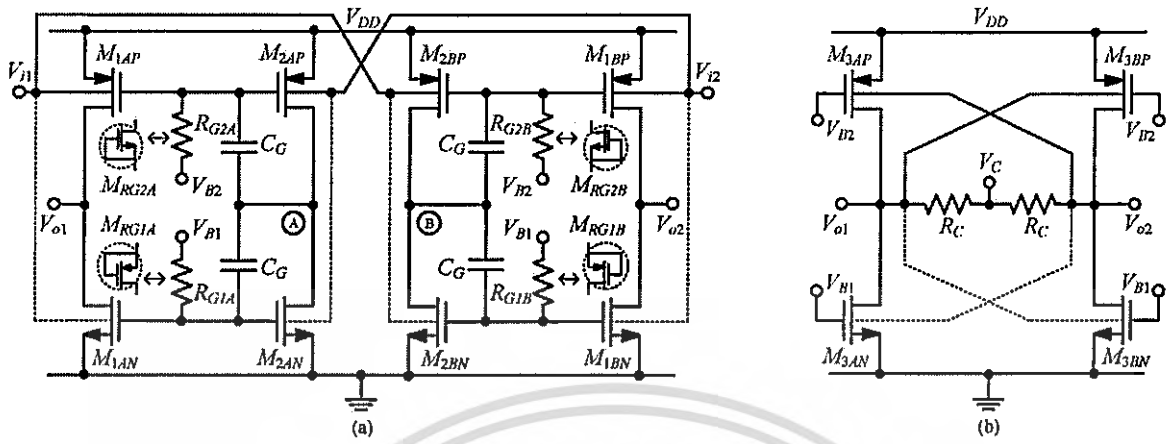


Figure 3. The proposed PD-OTA (a) circuit implementation (b) output impedance enhancement.

$M_{1A(B)P}$ to decrease due to the body effect, and hence, unsymmetrical output swing. In this work, $V_{B2}$ is set to 60 mV in order that symmetrical output swing is achieved. It is noted that $V_{B2}$ could be set to ground, and the input signal can be connected to the bodies of $M_{1A(B)P}$ and $M_{1A(B)N}$ (see dash line) if NMOS and PMOS have separated wells. We have found that the performance of the circuit is improved in doing so.

The dc common-mode output voltage ($V_{OCM}$) is set by the bias voltage ($V_C$) through resistor $R_C$ as shown in Fig. 3(b). In our design, $V_C$ is set to $V_{DD}/2$ to maximize the output swing.

## III. Simulation Results

To verify the circuit performance, Cadence Spectre is used to simulate the proposed circuit, using a standard 0.18 $\mu$m CMOS process ($V_{THN} \cong |V_{THP}| \cong 0.45$ Volt) to operate under the supply voltage of 0.5 V. In this work, the bias currents of all transistors are chosen to optimize both gain and power dissipation.

Fig. 4 shows the open-loop frequency response of the proposed PD-OTA in case of the differential-mode input signal. The DC differential-mode gain is found to be 35 dB, while the –3 dB and unity gain frequency are 1 MHz and 100 MHz, respectively. The phase margin of the proposed circuit is 80°. It is noted that the open-loop gain is increased up to 40 dB if input signal is connected to both body terminals. Fig. 5 shows the common-mode gain of the PD-OTA with (solid line) and without (dashed line) the feed-forward attenuator circuits. As seen, the common-mode gain with FFA (-35 dB) is relatively much smaller than that of the PD-OTA without FFA (13 dB).

Fig. 6 shows the transient responses of the output voltages for both differential-mode ($V_{o1}$, $V_{o2}$) and common-mode ($V_{oc}$), when the inputs are differential and common-mode voltages with the amplitude of 10 $mV_{pp}$ at 10 kHz. As seen, the differential-mode output voltage reads 0.3 $V_{pp}$, while the common-mode output voltage reads only 0.05 $mV_{pp}$.

Fig. 7 shows the proposed PD-OTA configured as a closed-loop inverting amplifier with the unity gain configuration ($R_1 = R_2$) and Fig. 8 shows the voltage transfer characteristic of the closed-loop amplifier. As seen, the output signal shows rail-to-rail operation. The power dissipation of the proposed PD-OTA is 50 µW.

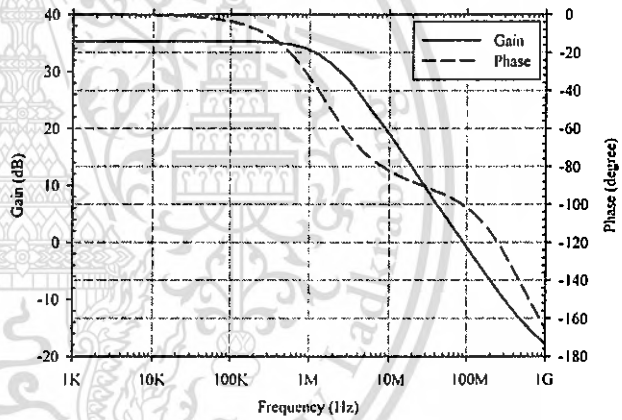


Figure 4. Differential-mode gain and phase margin.

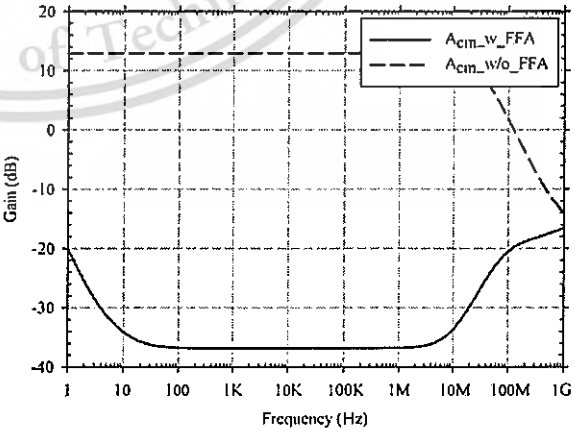


Figure 5. Comparisons of common-mode gain with and without FFA.

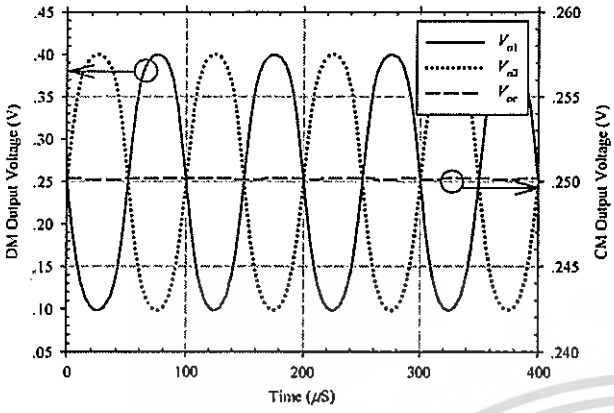


Figure 6. Differential and common-mode output voltages.

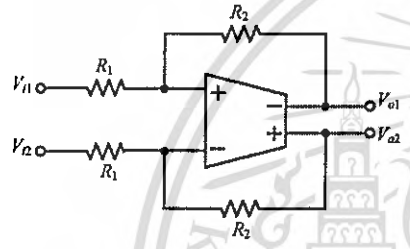


Figure 7. PD-OTA configured as an inverting amplifier.

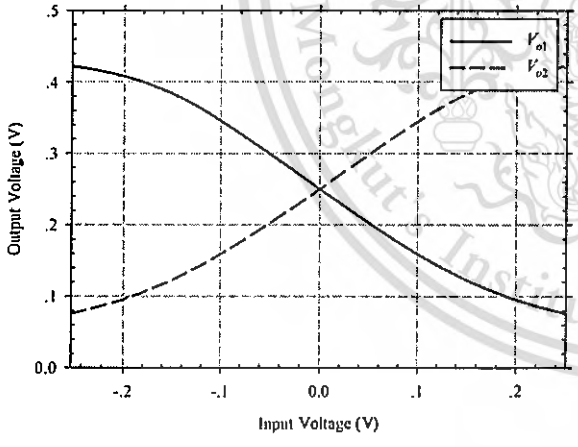


Figure 8. Voltage transfer charecteristic.

## IV. Conclusions

In this paper, a low voltage rail-to-rail CMOS pseudo differential OTA using simple feed-forward technique is proposed. The circuit employs QFG-inverter, enabling the circuit to operate under a low voltage supply. Feed-forward technique is used to suppress the common-mode response. The proposed OTA has been designed using 0.18 $\mu$m CMOS process. The simulation results shows rail-to-rail operation. The differential-mode gain is increased, while the common-mode gain is suppressed.

## Acknowledgment

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# A Current-Mode Common-Mode Feedback Circuit (CMFB) with Rail-to-Rail Operation

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**Abstract.** This paper presents a current-mode common-mode feedback (CMFB) circuit with rail-to-rail operation. The CMFB is a stand-alone circuit, which can be connected to any low voltage transconductor without changing or upsetting the existing circuit. The proposed CMFB employs current mirrors, operating as common-mode detector and current amplifier to enhance the loop gain of the CMFB. The circuit employs positive feedback to enhance the output impedance and gain. The circuit has been designed using a 0.18 $\mu$m CMOS technology under 1 V supply and analyzed using HSPICE with BSIM3V3 device models. A pseudo-differential amplifier using two common sources and the proposed CMFB shows rail to rail output swing ($\pm$ 0.7 V) with low common-mode gain (−36 dB) and power dissipation of 390 $\mu$W.

**Keywords.** Common-Mode Feedback, Pseudo-Differential Amplifier, Common-Mode Detector.

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## 1 Introduction

At present, a high performance analog circuit using low voltage is strongly demanded. This is mostly due to the advance of the large scale integration with complicated circuit systems, and the increase of the demand for battery-operated portable equipments. However, supply voltage reduction in analog circuits causes several performance degradations such as degraded intrinsic gain, limited voltage swing and less dynamic range. As a result, circuit techniques become mandatory to design analog circuits having sufficiently large gain with rail-to-rail capability.

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Current mode circuits, whose input/out signals are primarily currents, contain low impedance nodes resulting in small voltage swings. As a result, the circuits are not restricted by the supply voltage and large input and output current swings can be attained. In addition, low impedance nodes imply low time constant, enabling the circuits to operate with high bandwidth.

The operational transconductance amplifier (OTA) is one of the most frequently used basic cells. OTA finds many applications in many analog circuits such as operational amplifier, voltage comparators, analog-to-digital and digital-to-analog converters, and high frequency filters. At present, differential OTAs are often used in industry products, since they provide improved dynamic range over their single-ended counterparts. In addition, they can reject common-mode noise, contain no even-order nonlinearities and increase output voltage swing. Several approaches have been proposed to design low voltage OTA [1–16] using both fully differential (FD) and pseudo-differential (PD) configurations. FD is typically based on a differential pair with a tail current source, while PD is based on two independent inverters without tail current source. It is known that avoiding the voltage drop across the tail current source, in a PD structure, allows wider input and output ranges, making the architecture attractive for low power-supply applications. However, PD structure requires common-mode feedback (CMFB) circuit which serves two purposes: 1) to stabilize the common-mode voltage at high impedance nodes and 2) to suppress the common-mode signal components. In general, CMFB senses the common-mode (CM) output voltage, compares the result with a reference voltage and uses negative feedback to set the CM output voltage to the value that optimizes the output voltage swing.

Several approaches have been proposed to achieve CMFB [1–17]. [1,2] used the switched-capacitor (SC) technique, resulting in lower power consumption. However, the SC-CMFB circuits introduce clock-feed through error noise and increase load capacitance, making circuits not appropriate for low voltage continuous time applications. [3–5] used simple resistive divider to sense and average the voltage of two differential nodes. As a result, the voltage swing of the CMFB is not limited. However, not only do these resistors require large silicon area, these resistors load down the output impedances, thus affecting gain of the system. To solve this problem, methods of employing MOS transistor as CMFB have been proposed ([6–10]). The CMFB

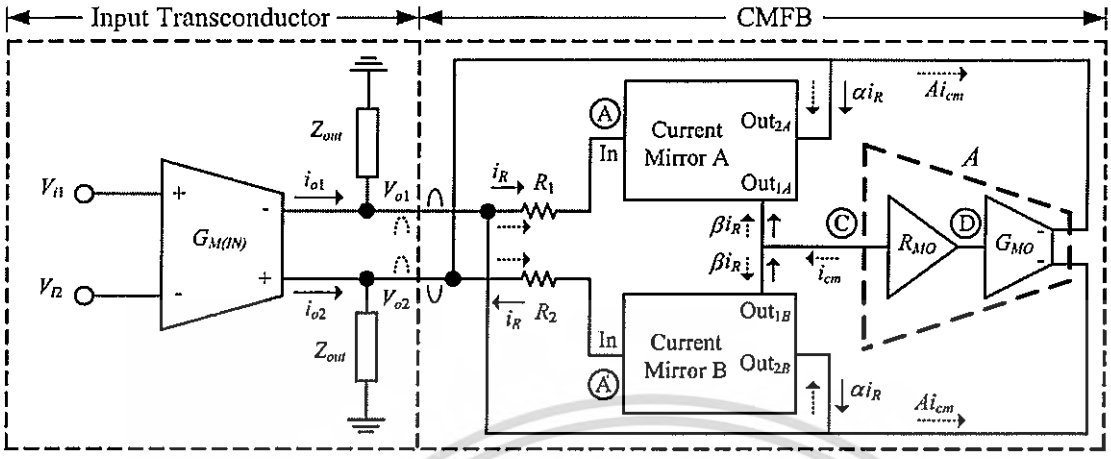


**Figure 1.** Block diagram of the proposed pseudo-differential amplifier (PDA).

consists of CM detector and one stage amplifier. Unfortunately, output swings are limited. [11–14] employed transistors with two stage common-mode amplifiers. The resulting common-mode gains are quite low. The problem with this structure is the limited output swing and potential oscillation problem. In addition, the bipolar transistor technology in [12] is not compatible with the well-known CMOS technology. [15, 16] proposed the complementary CMFB, which can achieve both low common-mode gains with good output swings. However, NMOS and PMOS with the same threshold voltage and transconductance are required, which may not be true in general. [17] proposed a positive feedback technique to increase the differential gain. However, the circuit shows quite high common-mode gain ($A_{cm} \cong -6\,dB$).

In this paper, a current-mode common-mode feedback (CMFB) circuit with rail-to-rail operation is proposed. The CMFB is a stand-alone circuit, and can be connected to low voltage transconductor, without changing or upsetting the existing circuit. The CMFB consists of current mirrors and resistors operating as a common-mode detector. The current amplifier, which consists of transimpedance and transconductance, is employed to enhance the loop gain of the CMFB, resulting in minimized relative gain error. The positive feedback with tunable current mirror is employed to enhance the differential gain of the system. The proposed CMFB shows low common-mode gain (−36 dB) and rail-to-rail capability.

## 2 Proposed Common-Mode Feedback

### 2.1 Common-Mode Feedback Architecture

Figure 1 illustrates the architecture of the proposed PD. As seen, the PD consists of an input transconductor $G_{M(IN)}$ and CMFB. The proposed CMFB consists of two matched resistors ($R_1 = R_2$), two matched current mirrors and two stage current amplifier (transimpedance and transconductance amplifiers). When the output voltages from $G_{M(IN)}$ are differential signals, these voltages are converted to the currents through resistors $R_1$ and $R_2$ (see solid signal). These currents, which have the same magnitude but opposite phase, flow to each resistor and are mirrored to the $Out_{1A}$ and $Out_{1B}$ terminals (with the current gain of $\beta$). Because these currents have the same magnitude but opposite phase, there will be no input current flowing into the transimpedance amplifier ($R_{MO}$) and, thus no voltage variation at node C. In addition, the currents through resistors $R_1$ and $R_2$ are mirrored to the $Out_{2A}$ and $Out_{2B}$ terminals (with the current gain of $\alpha$), and positively fed back to the output of the input transconductor $G_{M(IN)}$, thus enhancing the output impedance (at node $V_{o1}$ and $V_{o2}$) and differential gain of the system.

When the output voltages from the $G_{M(IN)}$ are common-mode signals, the common-mode current will flow through $R_1$ and $R_2$ (see dash signal) to nodes A and A′ with the same magnitude and phase. As a result, the summation of these two currents at the $Out_{1A}$ and $Out_{1B}$ terminals are added constructively ($i_{cm}$) and passed to the current amplifier ($A$), which consists of the transimpedance ($R_{MO}$) and transconductance ($G_{MO}$) amplifiers. The output current ($Ai_{cm}$) is then negatively fed back to the output node of input transconductor $G_{M(IN)}$, resulting in the reduced output impedance and common-mode gain of the system.

From Figure 1, it can be easily shown that the differential ($Z_{dm}$) and common-mode ($Z_{cm}$) output impedances at nodes $V_{o1}$ and $V_{o2}$ are

$$Z_{dm} = \frac{Z_{out}}{1 + (1-\alpha)Z_{out}/R_{1,2}}, \tag{1}$$

$$Z_{cm} = \frac{Z_{out}}{1 + (1+\alpha+2A\beta)Z_{out}/R_{1,2}} \tag{2}$$

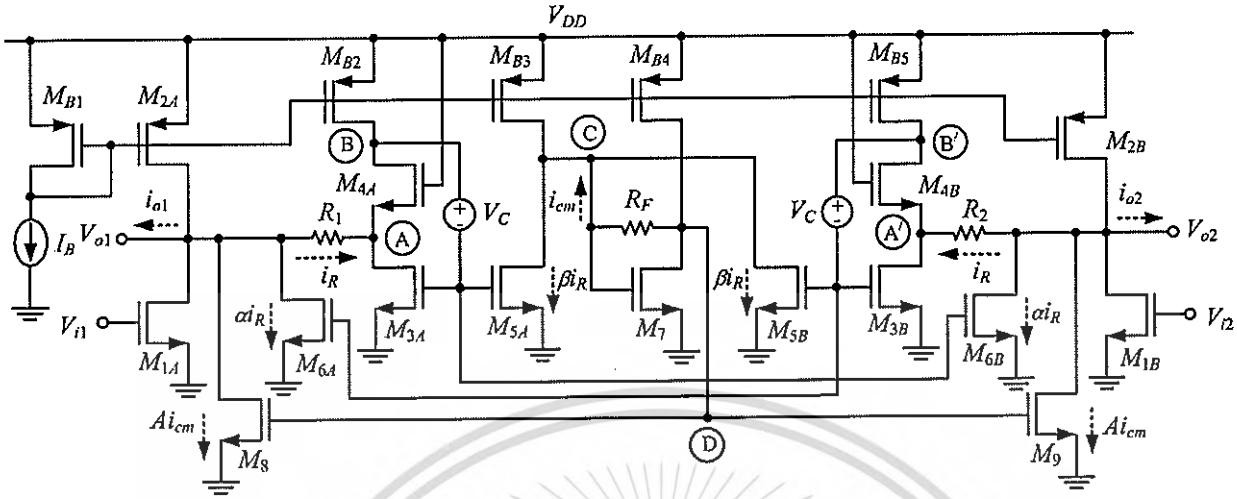


**Figure 2.** The proposed CMOS PDA.

where $Z_{out}$ is the output impedance of the input transconductor, $\alpha$ and $\beta$ are current mirror ratios, and $A$ is the current gain and equal to $R_{MO}G_{MO}$.

From equations (1)–(2), the differential-mode gain ($A_{dm}$) can be derived and shown as

$$A_{dm} = -G_{M(IN)}Z_{dm} = -G_{M(IN)}\left[\frac{Z_{out}}{1+(1-\alpha)Z_{out}/R_{1,2}}\right]. \quad (3)$$

Similarly, the common-mode gain ($A_{cm}$) can be shown as

$$A_{cm} = -G_{M(IN)}Z_{cm} = -G_{M(IN)}\left[\frac{Z_{out}}{1+(1+\alpha+2A\beta)Z_{out}/R_{1,2}}\right]. \quad (4)$$

From equations (3) and (4), the common-mode rejection ratio (CMRR) is given by

$$\text{CMRR} = \frac{A_{dm}}{A_{cm}} = \left[\frac{1+(1+\alpha+2A\beta)Z_{out}/R_{1,2}}{1+(1-\alpha)Z_{out}/R_{1,2}}\right]. \quad (5)$$

Obviously, CMRR can be increased, if $A = R_{MO}G_{MO}$ is large. In addition, the current mirror ratios $\alpha$ and $\beta$ play a role in determining $A_{dm}$, $A_{cm}$ and CMRR of the system.

### 2.2 Circuit Implementation

The circuit implementation of Figure 1 is shown in Figure 2. $M_{1A,B}$–$M_{2A,B}$ form the input transconductor $G_{M(IN)}$, while $M_{3A,B}$–$M_{6A,B}$ and $M_7$–$M_9$ form a current-mode CMFB circuit. As seen, $M_{3A}$–$M_{6A}$ form the current mirror A, while $M_{3B}$–$M_{6B}$ form the current mirror B. Since the impedance at node A (and A′) is very small, the signal swing at node $V_{o1}$ (and $V_{o2}$) is therefore limited by the output swing of the input transconductor ($G_{M(IN)}$). The ratios of $\alpha$ and $\beta$ (in equations (1)–(5)) can be set by adjusting the aspect ratios of $M_{3A,B}$, $M_{6A,B}$ ($\alpha = (W/L)_{6A,B}/(W/L)_{3A,B}$) and $M_{3A,B}$, $M_{5A,B}$ ($\beta = (W/L)_{5A,B}/(W/L)_{3A,B}$), respectively. It is noted that the positive-feedback term $\alpha$ can be used to enhance the differential gain of the system. However, it is instructive to note that an improper value of $\alpha$ can also drive the system unstable. In practice, $\alpha$ should be set a little bit larger than one, to compensate the loss as a result of the current mirror, which is unable to mirror the input current to the output perfectly. In this work, $\alpha$ is set to 1.5 to enjoy both differential gain and stability.

The value of $\beta$ plays a role in determining the common-mode gain. As seen in (4), a large value of $\beta$ results in low common-mode gain. However, it is noted that a large $\beta$ requires large transistors, thus large standby current and parasitic capacitors, which can degrade frequency performance of the system. In this work, $\beta$ is set to 10. The dc common-mode voltage of the system can be designed and is equal to $V_{DD} - V_{GS4(A,B)}$. In this work, we set the dc common mode voltage to $V_{DD}/2$ for the maximum output swing.

Important factors used to determine the bias currents and sizes of $M_{3A,B}$–$M_{6A,B}$ are the impedances at nodes A and A′. Bias current and dimension of these transistors should be chosen such that the impedances at both nodes are much lower than $R_{1,2}$. As a result, nodes A and A′ can be considered as ac grounds.

The current gain (A) of the CMFB depends on the gain of the transimpedance and transconductance amplifiers. Here,

transistor $M_7$ and resistor $R_F$ form the transimpedance amplifier ($R_{MO}$), while $M_8$–$M_9$ form the output transconductor ($G_{MO}$). Straightforward analysis shows that $R_{MO}$ and $G_{MO}$ are given by

$$R_{MO} = -R_F \frac{g_{m7}\left(r_{O7} /\!/ r_{O(B4)}\right)}{1 + g_{m7}\left(r_{O7} /\!/ r_{O(B4)}\right)} \cong -R_F, \quad (6)$$

$$G_{MO} = g_{m8,9}. \quad (7)$$

As mentioned earlier, $A = R_{MO}G_{MO}$ is an important parameter. Gain of CMFB should be sufficiently large so as to obtain the common-mode voltage within the desired accuracy. From equations (6) and (7), one can increase the value of $A$ by increasing $R_F$ and $g_{m8,9}$. In the design, however, the choice of $R_F$ requires some consideration, because $R_F$ also affects the impedances at node C and node D, thus the time constant of the CMFB. It is known that CMFB should contain the minimum number of poles to ensure the stability and speed of the overall system. Similarly, the value of $G_{MO}$ in equation (7) needs some consideration, since $g_{m8,9}$ depends on the device dimension and bias current, which affects directly parasitic capacitances and power consumption, respectively. In fact, the choice of $R_F$ and $g_{m8,9}$ strongly depends on the application for which CMFB is being applied.

### 2.3 Alpha (α) Tuning Circuitry

As mentioned earlier, α indicates the amount of the current feedback to the output node, and can be used to adjust the differential mode gain. However, we have found that α is quite sensitive to the stability of the system. Deviation of α from the desired value could result in a reduced differential gain or even cause the system to become unstable. Since the value of α depends on the matching of transistors, the performance of the system could suffer from process fluctuations. One solution to this problem is to design α with tuning ability.

In this work, we have developed a circuitry, which allows us to tune α electronically. Figure 3 shows such circuit (see the dashed line). As seen, the circuit consists of low voltage current mirror ($M_{T1}$–$M_{T5}$). $M_{T1}$–$M_{T2}$ are used to set the bias voltage at the gates of $M_{T2}$ and $M_{6B}$. The bias current of $M_{T4}$ is mirrored to $M_{T5}$, and causes the bias current of $M_{T2}$ and $M_{6B}$ to be equal. When the signal current $i_R$ flows into the circuit, the variation of the voltage signal at node X will pass through the capacitor $C_X$, and become the gate voltage of $M_{6B}$, which is further converted to the signal current $i_{o2}$. Since $i_{o2} = g_{m6B}v_x$ and $g_{m6B}$ is given by $(2\mu C_{ox}(W/L)I_{\text{Btune}})^{1/2}$, one can express the relationship between the output current and input current as

$$\frac{i_{o2}}{i_R} = \alpha = \sqrt{\frac{(W/L)_{6B}}{(W/L)_{3A}}\frac{I_{\text{Btune}}}{I_B}}. \quad (8)$$

From (8), it is obvious that the current gain α can be electronically tuned via the bias current $I_{\text{Btune}}$.

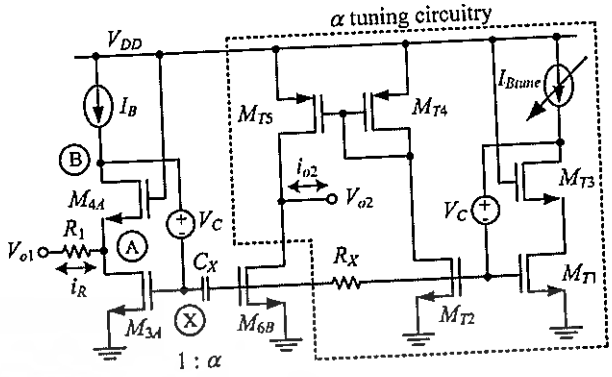


Figure 3. An electronically α tuning circuitry.

### 2.4 Compensation

Since CMFB introduces additional poles to the system, common-mode stability needs to be investigated. By using small signal analysis, one can find the impedances associated with nodes A (and A′), B (and B′), C and D as

$$R_{\text{A(A')}} = \frac{1}{g_{m3A,B}g_{m4A,B}\left(r_{OB2}\right)}, \quad (9)$$

$$R_{\text{B(B')}} = \frac{1}{g_{m3A,B}}, \quad (10)$$

$$R_{\text{C}} = \frac{R_F + (r_{OB4} /\!/ r_{O7})}{1 + g_{m7}\left(r_{OB4} /\!/ r_{O7}\right)}, \quad (11)$$

$$R_{\text{D}} = \frac{R_F + (r_{O5A} /\!/ r_{O5B} /\!/ r_{OB3})}{1 + g_{m7}(r_{O5A} /\!/ r_{O5B} /\!/ r_{OB3})}, \quad (12)$$

where $g_m$ and $r_O$ denote transconductance and output impedance of transistor, respectively.

### 2.5 Geometric and Parametric Mismatches

Since resistor and transistor mismatches may occur due to process gradients, the circuit performance is of concern. We have investigated and found that transistor mismatches in the current mirrors A and B will not affect system performance as long as the impedances at node A and A′ are much smaller than $R_1$ and $R_2$. Since the impedances at node A and A′ are designed to be small, the aforementioned condition can be met.

In case of the mismatch between $R_1$ and $R_2$, this could result in an undesired output voltage. To explain this, let us assume that $R_1 = R + \Delta R$ and $R_2 = R - \Delta R$. One can show that this mismatch can cause the common-mode output impedances at nodes $V_{o1,o}(Z_{\text{cm}(Vo1)}$ and $Z_{\text{cm}(Vo2)})$ to be different.

Straightforward small signal analysis shows that these output impedances are given by

$$Z_{\mathrm{cm}(Vo1)} = \frac{Z_{\mathrm{out}}}{1 + \left(\frac{1+\alpha+A\beta}{R+\Delta R} + \frac{A\beta}{R-\Delta R}\right) Z_{\mathrm{out}}}, \quad (13)$$

$$Z_{\mathrm{cm}(Vo2)} = \frac{Z_{\mathrm{out}}}{1 + \left(\frac{1+\alpha+A\beta}{R-\Delta R} + \frac{A\beta}{R+\Delta R}\right) Z_{\mathrm{out}}}. \quad (14)$$

Since $v_{o1}$, $v_{o2}$ are $-G_{M(IN)} Z_{\mathrm{cm}(Vo1)} v_{ic}$, $-G_{M(IN)} Z_{\mathrm{cm}(Vo2)} v_{ic}$, respectively, one can show that

$$v_{o1} - v_{o2} \cong -G_{M(IN)} \Delta R \frac{2}{(1+\alpha+2A\beta)^2} v_{ic}. \quad (15)$$

This differential output voltage, as a result of the resistor mismatch, behaves indistinguishably from the differential output signal, and could propagate to the next stage. From (15), one can reduce this undesired output voltage by having large $\alpha$ and large $A\beta$.

In addition to the resistor mismatch, the ratio mismatches in parameters $\alpha$ and $\beta$ – as a result of the mismatches in $M_{3A,B}$, $M_{6A,B}$ and $M_{3A,B}$, $M_{5A,B}$ – can also cause differential output voltage. If we assume that these ratio mismatches are $\alpha \pm \Delta\alpha$ and $\beta \pm \Delta\beta$, one can easily show that the undesired output voltages are given as

$$v_{o1} - v_{o2} = -G_{M(IN)} \Delta\alpha \frac{R}{2A^2\beta} v_{ic}, \quad (16)$$

$$v_{o1} - v_{o2} = -G_{M(IN)} \Delta\beta \frac{R}{A\beta} v_{ic}, \quad (17)$$

respectively.

Similarly, these output voltages can be reduced if $A\beta$ is large.

### 2.6 Minimum Supply Voltage and Output Swing

Based on the proposed circuit topology, the minimum supply voltage is given by

$$V_{DD(\min)} = V_{GS7} + V_{DSAT(MB3)} \quad (18)$$

where $V_{GS7}$ and $V_{DSAT(MB3)}$ are the gate-source voltage of $M_7$ and drain-source saturation voltage of $M_{B3}$, respectively. According to equation (18), it is obvious that the minimum supply voltage strongly depends on the threshold voltage. Therefore, process with low value of $V_{TH}$ can lead to CMFB, which can operate at lower supply voltage.

As previously mentioned, the impedances of the input current mirrors at node A and A′ are very small, thus causing both nodes to operate as virtual ground. As a result, the output swing of PDA (Figure 2) is only limited by the output swing of the input transconductor ($G_{M(IN)}$), which is given by

$$V_{DSAT(M1A,B)} \le V_{\mathrm{OUT(Swing)}} \le V_{\mathrm{DD}} - V_{\mathrm{DSAT(M2A,B)}}. \quad (19)$$

| Transistor | $(W/L)$ |
|---|---|
| $M_{1A,B}$ | 9/0.3 |
| $M_{2A,B}$ | 33/0.5 |
| $M_{3A,B}$, $M_8$, $M_9$, $M_{T1}$ | 6/0.3 |
| $M_{4A,B}$, $M_{T3}$ | 8.5/0.3 |
| $M_{5A,B}$ | 60/0.3 |
| $M_{6A,B}$, $M_{T2}$ | 9/0.3 |
| $M_7$ | 18/0.3 |
| $M_{B1}$, $M_{B2}$, $M_{B4}$, $M_{B5}$ | 22/0.5 |
| $M_{B3}$ | 220/0.5 |
| $M_{T4}$, $M_{T5}$ | 17/0.5 |

**Table 1**

## 3 Simulation Results

To verify the circuit performance, HSPICE with BSIM3V3 is used to simulate the proposed circuit using a 0.18 $\mu$m CMOS process under 1 V supply. Bias current ($I_B$) is set to 20 $\mu$A. This bias current value is chosen to optimize both gain and power dissipation of the circuit. In this work, $R_{1,2}$ and the impedance at node A (and A′) are 50 k$\Omega$ and 180 $\Omega$, respectively. The aspect ratios of the transistors are summarized in Table 1. The DC level shifters ($V_C$) in Figure 2 are designed using a simple resistor and current sources as suggested by [18].

Figure 4 shows the DC transfer characteristic of the PD with the proposed CMFB. As seen, the output swing shows rail-to-rail operation. Figure 5 shows the output current ($i_{o2}$) of the circuit in Figure 3 for different values of $I_{\mathrm{Btune}}$, when the input current ($i_R$) is 10 $\mu$ A$_{pp}$. The circuit demonstrates the current gains ($\alpha$) of 1, 1.3, 1.5 and 1.7, when $I_{\mathrm{Btune}}$ are 10 $\mu$ A$_{pp}$, 13 $\mu$ A$_{pp}$, 15 $\mu$ A$_{pp}$ and 17 $\mu$ A$_{pp}$, respectively.

Figure 6 shows how the differential mode gain ($A_{\mathrm{dm}}$) varies with $\alpha$. As discussed in Section 2, $\alpha$ can be used to enhance the output impedance and thus differential mode gain of the system. From Figure 6, it reveals that as $\alpha$ increases, the differential mode gain increases. It is noted, however, that an increase in $\alpha$ causes bandwidth to decrease. This is because an increase in $\alpha$ will increase the output impedance, and thus the time constant associated with the output nodes.

Figure 7 shows the common-mode gain for different values of $\beta$ and $R_F$, while Figure 8 shows common-mode bandwidth for different values of $\beta$ and $R_F$. As seen, large value of $\beta$ and $R_F$ can cause common-mode gain ($A_{\mathrm{cm}}$) to decrease as discussed in Section 2. Obviously, the choice of $\beta$ and $R_F$ needs careful consideration. It is noted that a large value of $\beta$ also causes more standby current, and thus more power dissipation, while large $R_F$ causes impedances at nodes C and D to increase, and thus degrading the band-

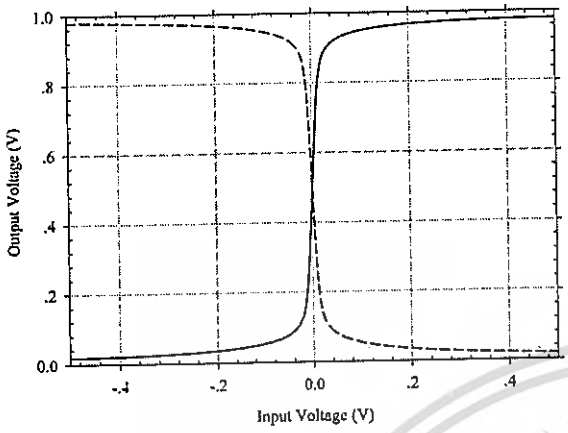


**Figure 4.** DC transfer characteristic.

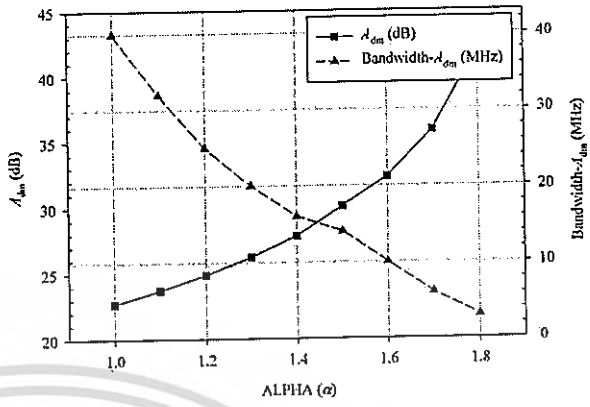


**Figure 6.** Differential-mode gain ($A_{dm}$) versus alpha ($\alpha$).

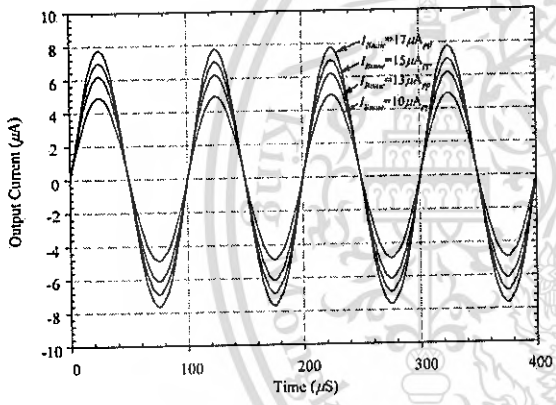


**Figure 5.** Output current ($I_{o2}$) of the circuit in Figure 3 for different values of $I_{Btune}$.

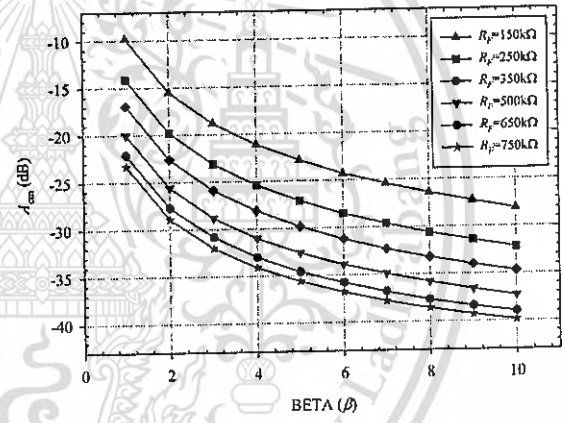


**Figure 7.** Common-mode gain ($A_{cm}$) versus beta ($\beta$).

width of the system. In fact, large $\beta$ results in large parasitic capacitances, and large time constant, which then also causes the common-mode bandwidth of the system to decrease. However, we have observed that an increase in $R_F$ causes common-mode gain bandwidth to decrease more rapidly than an increase in $\beta$, for the same value of common-mode gain. Therefore, power dissipation, chip area and common-mode gain bandwidth are important factors used to justify the value of $\beta$ and $R_F$.

Figure 9 shows the transient response of the output voltages for both differential mode ($V_{od} = V_{o1} - V_{o2}$) and common-mode ($V_{oc} = (V_{o1} + V_{o2})/2$), when the differential and common-mode inputs are 17 mV at 10 KHz and $\alpha = 1.5$, $\beta = 10$ and $R_F = 500\,\text{k}\Omega$. As seen, the differential output voltage reads $\pm$ 0.7 V, while the output common-mode voltage shows only 0.03 mV variation. Figure 10 shows frequency response of the proposed PDA for differential mode input signals. The DC gain is found to be 35.6 dB with the –3 dB and unity gain frequency of 10.4 MHz and 1.25 GHz, respectively, while the phase margin is 83°. Figure 11 shows gain and phase for the common-mode case. As seen, the common-mode gain is small and found to be –36 dB.

Figure 12 (a) shows an RC bandpass filter-based oscillator using our proposed PD ([19]). In this type of oscillator, the oscillation frequency depends on the bandpass filter, which is made of passive resistors and capacitors, the oscillator frequency is therefore less susceptible to power supply noise. Figure 12 (b) shows the output waveform. The oscillation frequency is found to be 4 MHz, which is close to the calculated result $R_1 = R_2 = 45\,\text{k}\Omega$ and $C_1 = C_2 = 1\,\text{pF}$ ($f_{osc} = 1/2\pi RC = 3.5\,\text{MHz}$). The power dissipation of the proposed PDA is 390 $\mu$W.

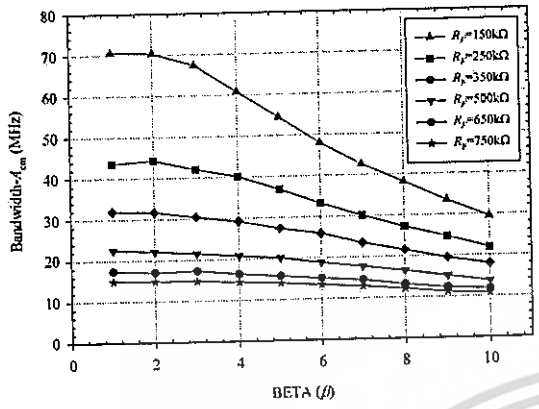


**Figure 8.** Bandwidth of the common-mode gain versus beta ($\beta$).

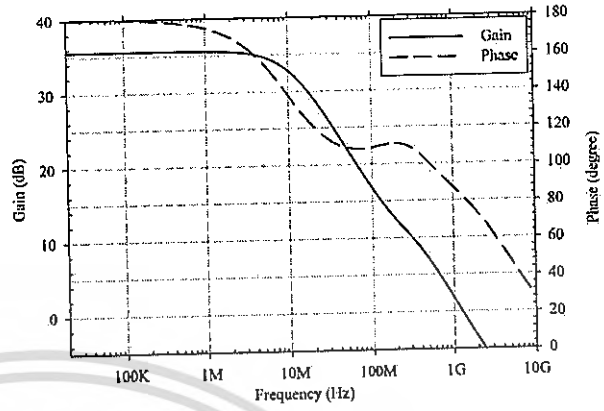


**Figure 10.** Differential gain and phase margin.

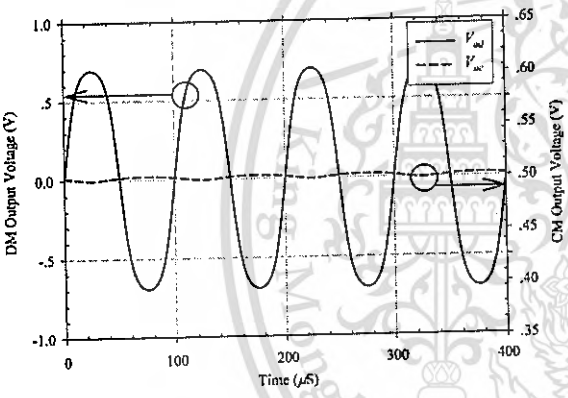


**Figure 9.** Differential-mode and common-mode output voltages.

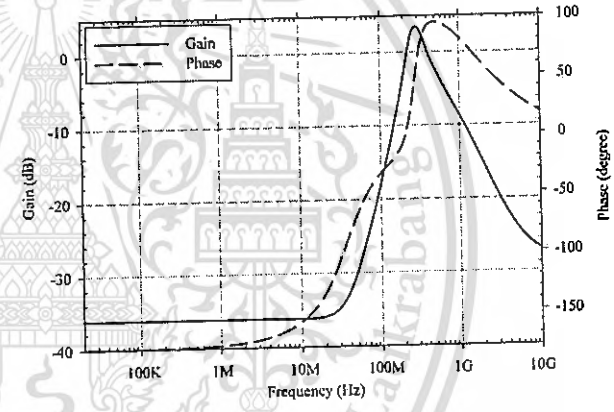


**Figure 11.** Common-mode gain and phase margin.

## 4 Conclusions

This paper presents a current-mode common-mode feedback (CMFB) circuit with rail-to-rail operation. The CMFB converts the output voltage signals into currents, which is then applied to two current mirrors, operating as a common-mode detector. The current amplifier is used to enhance the loop gain, resulting in minimized gain error. The positive feedback is also employed to enhance the differential gain of the system. The proposed CMFB shows low common-mode gain and rail-to-rail capability.

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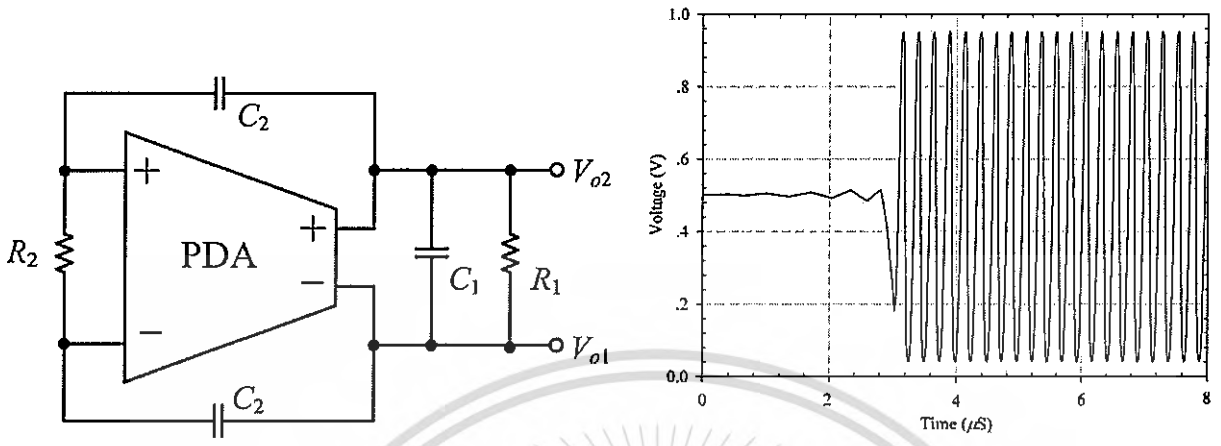


**Figure 12.** (a) Sinusoidal oscillator circuit using our proposed PD and (b) output waveform.

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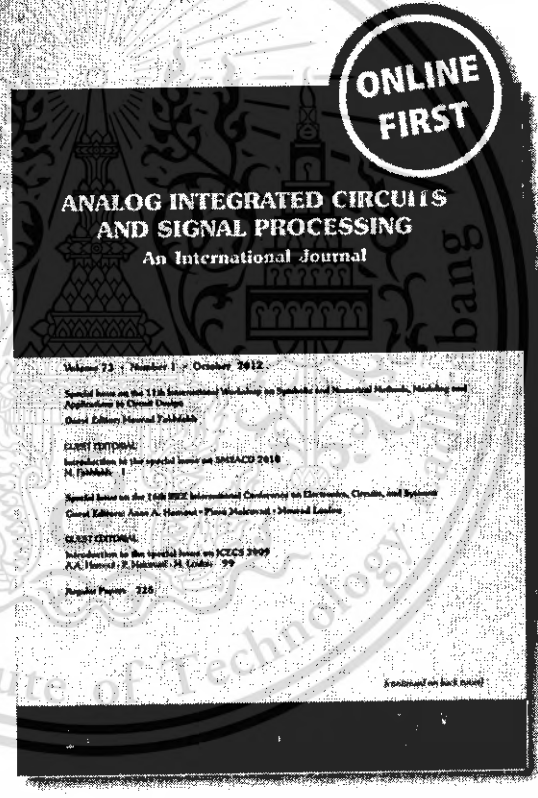


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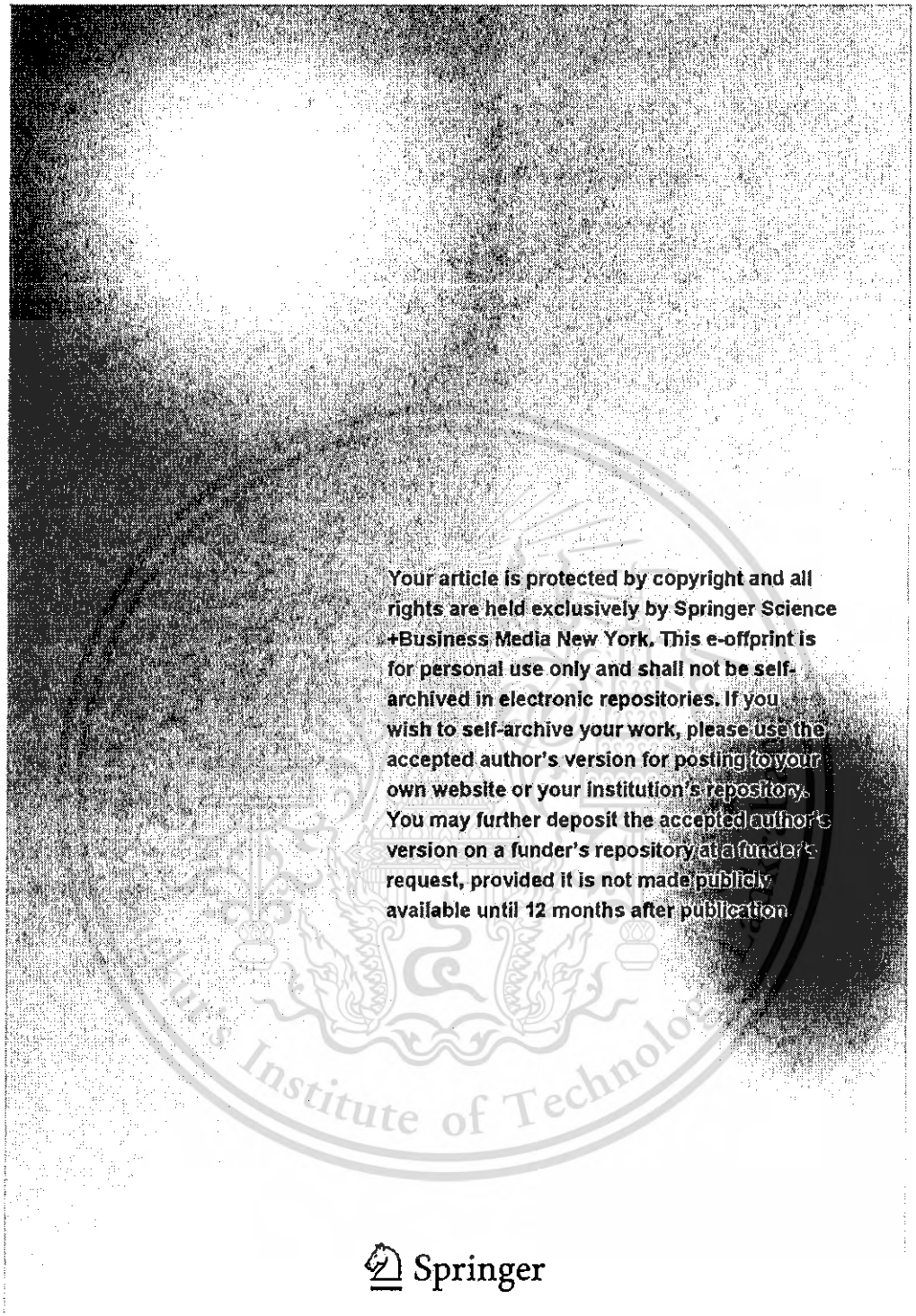

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# A CMOS inverter-based class-AB pseudo-differential amplifier with current-mode common-mode feedback (CMFB)

**Apirak Suadet · Varakorn Kasemsuwan**

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**Abstract** This paper presents a CMOS inverter-based class-AB pseudo-differential amplifier comprising current-mode common-mode feedback (CMFB). The circuit employs two CMOS inverters and the complementary CMFB consisting of current-mode common-mode (CM) detector and transimpedance amplifier. The circuit has been designed using 0.18 μm CMOS technology and operates at 1 V supply. The simulation results demonstrate rail-to-rail operation with low CM gain (−15 dB). The power dissipation of the circuit is 102.5 μW.

**Keywords** Pseudo-differential amplifier · Common-mode feedback · Class-AB · CMOS inverter

## 1 Introduction

Nowadays, a high-performance analog circuit operating at low voltages becomes increasingly important due mainly to the advance of the large scale integration with complicated circuit systems and the demand for battery-operated portable equipment. However, supply voltage reduction in analog circuit causes several performance degradations and, therefore, new design approaches are required to obtain analog circuits with sufficient bandwidth, gain, and linearity.

Current mode circuits, whose input and output signals, are primarily currents contain low impedance nodes resulting in small voltage swings. As a result, the circuits are not restricted by the supply voltage and large input and output current swings can be attained. In addition, low impedance nodes imply low time constants, enabling the circuits to operate with high bandwidth.

The operational transconductance amplifier (OTA) is an important analog building block. OTA finds many applications in many analog circuits, such as sample and hold stages, comparators, data converters and high frequency filters [1–6]. Differential OTA is usually employed since this approach entails a number of well-known advantages, such as dynamic range extension, even-order harmonics cancellation, and noises reduction. Many approaches have been proposed in the design of differential OTA [1–30] using both fully differential (FD) and pseudo-differential (PD) configurations. FD is typically based on a differential pair with a tail current source, while PD is based on two independent inverters without a tail current source. It is known that avoiding the voltage drop across the tail current source allows wider input and output ranges and makes the architecture attractive for low power-supply applications. However, PD structure requires an extra common-mode feedback (CMFB) circuit, which serves two purposes: (1) to fix the common-mode (CM) voltage at high impedance nodes and (2) to suppress the CM signal components.

A number of approaches have been proposed to realize CMFBs [7–28]. Switched-capacitor circuits were proposed to build CMFBs [7, 8] with small power consumption. However, this approach introduces clock-feed through error and load capacitance. The CMFBs in [9, 10] used simple resistive divider to sense the voltage between two differential nodes, thus enabling the CMFBs to have rail-to-rail operation capability. However, not only do these resistors require large silicon area, they load down the output impedances. MOS resistive network with bulk-

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driven CMFB technique was proposed in [11]. The circuit has quite low output impedance and high common gain. Methods of employing MOS transistors as CMFBs were proposed in [12–14]. The CMFBs consist of CM detector and one stage amplifier. As a result, the CM gains are quite high and, in addition, the output swing is limited. Two-stage CM amplifiers were proposed in [15–18] and the resulting CM gain is low. This structure suffers from limited output swing. Low CM gains with good output swings were obtained using the complementary CMFB [19–21]. However, the circuits are complex and require high power consumption. Positive feedback was used in [22–24] to increase the differential-mode gain. The circuit demonstrates high CM gain ($A_{cm} \cong -6$ dB). Combinations of CM feedforward and CMFB were proposed in [25–27] to suppress the CM signal. Nevertheless, by using the same topology in both CMFF and CMFB, the proposed differential OTA consumes high power and requires good-matching MOSFETs to achieve the cancellation of the CM components. An adaptive bias CMFB to suppress the CM gain was proposed in [28]. Nonetheless, this technique demands large CM loop gain and limits the signal swing.

In this paper, a CMOS inverter-based class-AB pseudo-differential amplifier (PDA) using a new CMFB is proposed. The CMFB consists of current mirrors and transimpedance amplifier (TA). The resulting circuit demonstrates low CM gain (−15 dB) and rail-to-rail operation. The positive feedback is also employed to increase the differential-mode gain. The organization of this paper is as follows: Sect. 2 introduces the proposed PDA structure and operating principle of the proposed CMFB. Section 3 discusses the circuit implementation and transfer characteristics. Section 4 presents the performance analysis and its application of the proposed PDA as bandpass filter is demonstrated in Sect. 5. Simulation results are given in Sect. 6 followed by conclusions in Sect. 7.

## 2 The proposed PDA structure

The topology of a PD structure is shown in Fig. 1. $G_{m(in)A}$ and $G_{m(in)B}$ are two input transconductors and $Z_{outA}$ and $Z_{outB}$ are the equivalent output impedances of $G_{m(in)A}$ and $G_{m(in)B}$, respectively. Unlike FD structure, PD structure is based on two transconductors without tail current source, making the PD structure suitable for low-voltage applications. However, removing the tail current source results in large CM gain ($A_{cm}$).

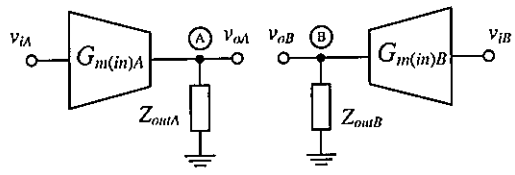


Fig. 1 PDA topology

From Fig. 1, the CM gain ($A_{cm}$) and the differential-mode gain ($A_{dm}$) are expressed as:

$$A_{cm} = G_{m(in)A(B)} Z_{outA(B)} \tag{1}$$

$$A_{dm} = G_{m(in)A(B)} Z_{outA(B)} \tag{2}$$

As shown in Eqs. (1) and (2), the CM gain ($A_{cm}$) is the same as the differential-mode gain ($A_{dm}$), resulting in the unity common-mode rejection ratio ($CMRR = A_{dm}/A_{cm} = 1$). Since large value of $A_{cm}$ can lead to large CM variation at the output [29], CMFB circuit is required.

The conceptual implementation of the proposed PDA is illustrated in Fig. 2(a). The proposed PDA consists of two input transconductors ($G_{m(in)A}$ and $G_{m(in)B}$) and a CMFB network. In our design, the CMFB network comprises a common-mode amplifier (CMA) and two output transconductors ($G_{m(out)A}$ and $G_{m(out)B}$). To explain the operation of the proposed PDA, the operation of the CMA, whose topology is shown in Fig. 2(b), is first examined. The CMA consists of two matched resistors ($R_1 = R_2 = R$), two matched current mirrors (current mirrors A and B), and TA.

When the output voltages ($v_{oA}$ and $v_{oB}$) are CM signals ($v_{oA} = v_{oB}$) (see dotted line), these voltages are converted into currents through $R_1$ and $R_2$. These CM currents with the same magnitude and phase flow through nodes A and B, and are mirrored to Out1A and Out1B terminals with the current gain of $\beta$. These currents are incrementally combined at node C and passed to the TA. The amplified output voltage $v_{cma}$ is then negatively fed back to the output of the input transconductors ($G_{m(in)A}$ and $G_{m(in)B}$) via the output transconductors ($G_{m(out)A}$ and $G_{m(out)B}$) to suppress the CM voltage. In addition, the CM currents are mirrored to Out2A and Out2B terminals (with the current gain of $\alpha$) and cross-fed back to the output nodes such that the CM gain is further suppressed.

From Fig. 2, the equivalent CM output impedance ($Z_{out(cm)A(B)}$) and CM gain ($A_{cm}$) are derived and shown as

$$Z_{out(cm)A(B)} = \frac{Z_{out}}{1 + \left(1 + \alpha - 2G_{m(out)}\beta Z\right) Z_{out}/R} \tag{3}$$

$$A_{cm} = G_{m(in)} \left[ \frac{Z_{out}}{1 + \left(1 + \alpha - 2G_{m(out)}\beta Z\right) Z_{out}/R} \right], \tag{4}$$

where $Z_{out} = Z_{(out)A(B)}$, $G_{m(in)} = G_{m(in)A(B)}$, $G_{m(out)} = G_{m(out)A(B)}$, and $Z$ is the transimpedance gain of the TA.

$Z_{out(cm)A(B)}$ and $A_{cm}$ depend on $\alpha$, $G_{m(out)}$, $\beta$ and Z. Obviously, $A_{cm}$ of the proposed PDA can be reduced if the

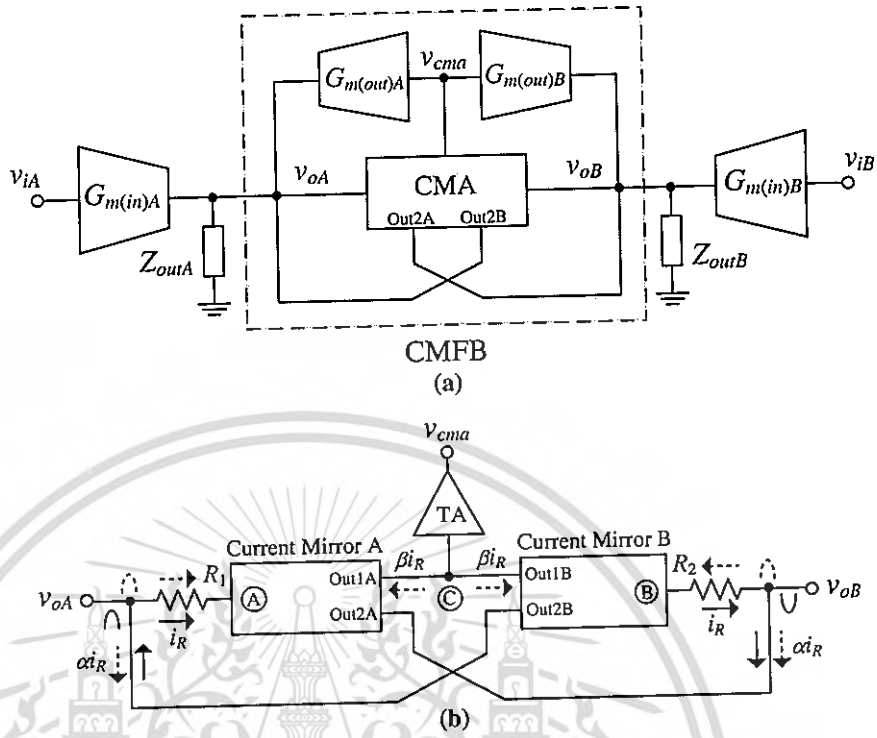


Fig. 2 Circuit topology of **a** the proposed PDA and **b** the CMA

CM loop gain $2G_{m(out)}\beta Z(Z_{out}/R)$ is large. It is also worth noting that the proposed topology of CMA allows rail-to-rail operation at the output nodes $v_{oA(B)}$ since input impedances of the current mirrors are relatively small, resulting in small-signal variation at nodes A and B.

Let us consider the output voltages as differential signals ($v_{oA} = -v_{oB}$) (see solid signal). These voltages are similarly converted into currents through $R_1$ and $R_2$. However, unlike the previous case, these currents have opposite phase resulting in no current flowing into (and out of) node C and the TA. As a result, the feedback signal $v_{cma}$ remains constant. It is noticed that the differential currents are also mirrored to Out2A and Out2B terminals and then positively cross-fed back to the output terminals. This positive feedback mechanism enhances the equivalent differential output impedance ($Z_{out(dm)A(B)}$) and, thus, the differential gain ($A_{dm}$) of the system.

$Z_{out(dm)A(B)}$ and $A_{dm}$ are derived and expressed as

$$Z_{out(dm)A(B)} = \frac{Z_{out}}{1 + (1-\alpha)Z_{out}/R} \tag{5}$$

$$A_{dm} = G_{m(in)}\left[\frac{Z_{out}}{1 + (1-\alpha)Z_{out}/R}\right]. \tag{6}$$

$Z_{out(dm)A(B)}$ and $A_{dm}$ depend on $\alpha$. If $\alpha$ is equal to one, $Z_{out(dm)A(B)}$ and $A_{dm}$ will become very large. This is the direct result of the positive feedback of the differential currents as previously mentioned.

The proposed topology of PDA shown in Fig. 2 can suppress the CM response by the negative feedback mechanism, while the differential-mode gain is enhanced via the positive feedback mechanism. It is noted that, since the voltage signal variations at nodes A and B are small, the output swing of PDA is therefore only limited by the output swing capability of the input transconductors. Furthermore, the CMFB topology contains only low impedance node, thus allowing the PDA to operate at high frequency.

## 3 Circuit implementation

The circuit implementation of the topology in Fig. 2 is illustrated in Fig. 3. Transistors $M_{1NA,B}$ and $M_{1PA,B}$ form the input transconductors, while $M_{2NA(B),2PA(B)}$–$M_{4NA(B),4PA(B)}$ and $M_{5N,P}$ form the CMFB circuit. $M_{2N(P)A}$–$M_{4N(P)A}$ form the current mirror A while $M_{2N(P)B}$–$M_{4N(P)B}$ form the current mirror B. The current gains $\alpha$ and $\beta$ are obtained by properly sizing the aspect ratios of the transistors in both current mirrors. It is noted that $M_{1PA(B)}$ and $M_{1NA(B)}$ also serve as the output transconductor ($G_{m(out)A(B)}$) with the transconductance equal to the bulk transconductance of $M_{1PA(B)}$. This efficient design in which a single transconductor is employed as both input and output transconductors simplifies and compacts the circuit. Moreover, the loading effect and power dissipation are minimized.

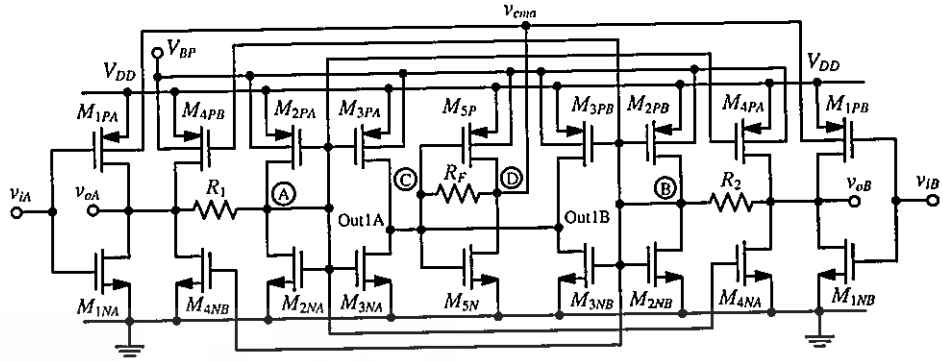


**Fig. 3** Circuit implementation of Fig. 2

Transistors $M_{5N,P}$ and resistor $R_F$ form the TA. The transimpedance gain ($Z$) of the circuit is set by the resistor $R_F$. The TA helps to increase the gain of the CMA and simultaneously reduce the impedances at nodes C and D such that the time constants associated with these nodes are low. The body bias voltage $V_{BP}$ is set to reduce the threshold voltages of PMOS transistors, allowing the circuit to operate at low supply voltages.

By comparing Figs. 2 and 3, the input transconductance ($G_{m(in)}$), output transconductance ($G_{m(out)}$), equivalent output impedances at node $v_{oA(B)}$ ($Z_{out}$), and transimpedance gain ($Z$) can be expressed as

$$G_{m(in)} = g_{m1N} + g_{m1P} \tag{7}$$

$$G_{m(out)} = g_{mb1P} \tag{8}$$

$$Z_{out} = r_{O1N} \parallel r_{O1P} \parallel r_{O4N} \parallel r_{O4P} \tag{9}$$

$$Z = R_F, \tag{10}$$

where $g_{mi}$, $g_{mbi}$ and $r_{Oi}$ are the transconductance, bulk transconductance and drain-to-source resistance of the transistor $M_{iA(B)}$, respectively.

By substituting Eqs. (7)–(10) in Eqs. (3)–(6), $Z_{out(cm)}$, $Z_{out(dm)}$, $A_{cm}$ and $A_{dm}$ can be expressed as

$$Z_{out(cm)} = \frac{R}{1+\alpha-2g_{mb1P}\beta R_F + R(r_{O1N} \parallel r_{O1P} \parallel r_{O4N} \parallel r_{O4P})^{-1}} \tag{11}$$

$$Z_{out(dm)} = \frac{R}{1-\alpha+R(r_{O1N} \parallel r_{O1P} \parallel r_{O4N} \parallel r_{O4P})^{-1}} \tag{12}$$

$$A_{cm} = (g_{m1N}+g_{m1P})\frac{R}{1+\alpha-2g_{mb1P}\beta R_F + R(r_{O1N} \parallel r_{O1P} \parallel r_{O4N} \parallel r_{O4P})^{-1}} \tag{13}$$

$$A_{dm} = (g_{m1N}+g_{m1P})\frac{R}{1-\alpha+R(r_{O1N} \parallel r_{O1P} \parallel r_{O4N} \parallel r_{O4P})^{-1}} \tag{14}$$

From Eqs. (13) and (14), the $CMRR$ can be derived as

$$CMRR = \frac{A_{dm}}{A_{cm}} = \frac{(1+\alpha-2g_{mb1P}\beta R_F)(r_{O1N} \parallel r_{O1P} \parallel r_{O4N} \parallel r_{O4P})+R}{(1-\alpha)(r_{O1N} \parallel r_{O1P} \parallel r_{O4N} \parallel r_{O4P})+R}. \tag{15}$$

It is noticed that $CMRR$ can be increased if $R_F$ is large. In addition, $\alpha$ and $\beta$ also play a role in determining the $CMRR$.

It is noted that the choice of $\alpha$ requires precaution. A large value of $\alpha$ can result in a large differential gain; however, such a large value of $\alpha$ can drive the circuit unstable. In practice, $\alpha$ should be set slightly larger than one to compensate for the loss, due to the imperfection of the current mirror not being able to perfectly mirror the current from the input to the output. In this work, $\alpha$ is set to 1.3 to enjoy both differential gain and stability. The value of $\beta$ plays a role in the determination of the CM gain as it is

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part of the CMFB circuit. From Eq. (4), large value of $\beta$ results in low CM gain. Nevertheless, large $\beta$ requires large transistors; thus large standby current and parasitic capacitors, which can degrade the frequency performance of the system. In this work, $\beta$ is set to 5.

The output CM voltage ($V_{out(cm)}$) is equal to the voltages at nodes A and B, which is given by [30]

$$V_{out(cm)} = \frac{V_{DD} - V_{TN2A(B)} + V_{TP2A(B)}}{1 + \sqrt{\beta_{N2A(B)} / \beta_{P2A(B)}}} + V_{TN2A(B)}, \quad (16)$$

where $\beta_{N2A(B)} = \mu_n C_{OX}(W/L)_{2A(B)}$ and $\beta_{P2A(B)} = \mu_p C_{OX}(W/L)_{2A(B)}$

For maximum output swing, $\beta_{N2A(B)}$ and $\beta_{P2A(B)}$ should be such that $V_{out(cm)}$ is equal to $V_{DD}/2$.

## 4 Performance analysis

### 4.1 Loop gain and frequency response of the proposed CMFB

The frequency compensation of the CM loop is accomplished by adding a resistor $R_C$ and capacitor $C_C$ in series between nodes C and D (not shown in Fig. 3). The small-signal equivalent circuit with $R_C$ and $C_C$ can be shown in Fig. 4, where $r_{oC(D)}$ and $C_{oC(D)}$ are the total parasitic resistance and capacitance at node C(D), $r_{oL}(= r_{O1N} \parallel r_{O1P} \parallel r_{O4N} \parallel r_{O4P})$ and $C_{oL}(= C_{DBN1} + C_{DBP1} + C_{DBN4} + C_{DBP4})$ are the equivalent resistance and capacitance at the output of the PDA, respectively.

By using typical circuit analysis, the open-loop gain of the proposed CMFB is

$$A_{CMFB}(s) = \frac{A_{CMFB}(0)\left(1 + \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)\left(1 + \frac{s}{\omega_{P2}}\right)\left(1 + \frac{s}{\omega_{P3}}\right)\left(1 + \frac{s}{\omega_{P4}}\right)}, \quad (17)$$

where $A_{CMFB}(0)$ is the small-signal DC gain of the CMFB loop expressed as

$$A_{CMFB}(0) \approx -\frac{2\beta g_{mb1P} r_{oL} R_F}{R}. \quad (18)$$

From Eq. (17), there are one dominant LHP pole, three non-dominant LHP poles and one LHP zero, each of which is determined by:

$$\omega_{Z1} \approx -\frac{1}{C_C R_C} (\text{LHP ZERO}) \quad (19)$$

$$\omega_{P1} \approx -\frac{1}{r_{oL} C_{oL} + C_C(R_C + R_F)} (\text{LHP POLE}) \quad (20)$$

$$\omega_{P2} \approx -\frac{r_{oL} C_{oL} + C_C(R_F + R_C)}{C_{oL} C_C r_{oL}(R_F + R_C)} (\text{LHP POLE}) \quad (21)$$

$$\omega_{P3} \approx -\frac{g_{m5}}{(C_{oC} + C_{oD})} (\text{LHP POLE}) \quad (22)$$

$$\omega_{P4} \approx -\frac{C_{oC} C_{oD} + C_C(C_{oC} + C_{oD})}{C_{oC} C_{oD} C_C R_C} (\text{LHP POLE}). \quad (23)$$

From Eqs. (18) and (20), the gain bandwidth product ($GBW$) of the CMFB loop is

$$GBW = A_{CMFB}(0) \cdot \omega_{P1} = \frac{2\beta g_{mb1P} r_{oL} R_F}{R} \cdot \frac{1}{r_{oL} C_{oL} + C_C(R_C + R_F)} \quad (24)$$

The first non-dominant pole is $\omega_{P2}$. Since $\omega_{P3}$ and $\omega_{P4}$ are far away from the unity-gain frequency, the overall phase margin can be determined as

$$PM \approx 180° - \tan^{-1}\left(\frac{GBW}{\omega_{P1}}\right) - \tan^{-1}\left(\frac{GBW}{\omega_{P2}}\right) + \tan^{-1}\left(\frac{GBW}{\omega_{Z1}}\right) \quad (25)$$

According to Eq. (25) and Fig. 4, $\omega_{Z1}$ is the left half-plane zero and of lower frequency than $\omega_{P3}$ and $\omega_{P4}$. This zero will add positive phase margin to the frequency response of the CMFB, simplifying the design of stable amplifier for unity gain in differential mode.

### 4.2 Noise analysis

The input-referred noise voltage of MOSFET is dominated by flicker noise at low frequency and by thermal noise at

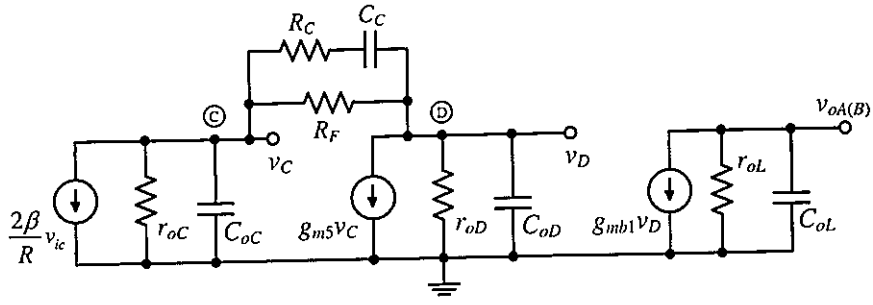



**Fig. 4** Simplified small-signal CMFB loop

high frequency. The input-referred noise spectral density of the PDA can be calculated and shown as

$$\overline{V_n^2} \approx \overline{V_{n,(1/f)}^2} + \overline{V_{n,th}^2}, \tag{26}$$

where $V_{n,(1/f)}$ is the input-referred flicker noise determined by

$$\overline{V_{in(1/f)}^2} = \frac{2}{C_{OX}f}\left(\frac{K_N}{(WL)_{1N}} + \frac{K_P}{(WL)_{1P}}\right), \tag{27}$$

and $V_{n,th}$ is the input-referred thermal noise determined by

$$\overline{V_{in,th}^2} = 8\frac{k_B T}{(g_{m1N} + g_{m1P})^2}\left[\frac{2}{3}(g_{m1N} + g_{m1P} + g_{m4N} + g_{m4P}) + \frac{1}{R}\right], \tag{28}$$

where parameters $K_N$ and $K_P$ are the flicker noise process-dependent constants of NMOS and PMOS, respectively. $k_B$ is the Boltzmann constant, $T$ is the absolute temperature, $f$ is the frequency, and other parameters have their usual meanings.

From Eqs. (27) and (28), the input-referred noise can be lowered by increasing $(g_{m1N} + g_{m1P})$ and/or sizes of $M_{1NA(B)}$ and $M_{1PA(B)}$. Obviously, the amplifier suffers from a fundamental tradeoff between its noise performance and frequency response.

### 4.3 Geometric and parametric mismatches

Since resistor and transistor mismatches are practically unavoidable, the circuit performance accounting for mismatches is therefore of concern. It is found that system performance is unaffected by transistor mismatches in the current mirrors A and B as long as the impedances at nodes A and B are much smaller than those of $R_1$ and $R_2$. Since the impedances at nodes A and B are designed to be small, the aforementioned condition can be readily met.

In case of the mismatch between $R_1$ and $R_2$, this could result in an undesired output voltage. To clarify this point, it is assumed that $R_1 = R + \Delta R$ and $R_2 = R - \Delta R$ and the results reveal that this mismatch can cause the CM output impedances at nodes $v_{oA}$ and $v_{oB}$ (i.e., $Z_{out(cm)A}$ and $Z_{out(cm)B}$) to be different.

The straightforward small-signal analysis shows $Z_{out(cm)A}$ and $Z_{out(cm)B}$ are determined by

$$Z_{out(cm)A} = \frac{1}{\frac{1+\alpha-g_{mb1P}\beta R_F}{R+\Delta R} - \frac{g_{mb1P}\beta R_F}{R-\Delta R} + (r_{O1N} \parallel r_{O1P} \parallel r_{O4N} \parallel r_{O4P})^{-1}} \tag{29}$$

$$Z_{out(cm)B} = \frac{1}{\frac{1+\alpha-g_{mb1P}\beta R_F}{R-\Delta R} - \frac{g_{mb1P}\beta R_F}{R+\Delta R} + (r_{O1N} \parallel r_{O1P} \parallel r_{O4N} \parallel r_{O4P})^{-1}}. \tag{30}$$

Since $v_{oA}$ and $v_{oB}$ are respectively $G_{m(in)}Z_{out(cm)A}\, v_{ic}$ and $G_{m(in)}Z_{out(cm)B}\, v_{ic}$, one can show that

$$v_{oA} - v_{oB} \cong (g_{m1N} + g_{m1P})\Delta R\frac{2}{(1+\alpha-2g_{mb1P}\beta R_F)^2} v_{ic}. \tag{31}$$

This differential output voltage behaves indistinguishably from the differential output signal and could propagate to the subsequent stage. From Eq. (31), the undesired output voltage can be reduced by increasing $g_{mb1P}\beta R_F$.

In addition to the resistor mismatch, the ratio mismatches in $\alpha$ and $\beta$, as a result of mismatches in $M_{2A(B)}$, $M_{4A(B)}$ and $M_{2A(B)}$, $M_{3A(B)}$, can cause differential output voltage. If these ratio mismatches are assumed to be $\alpha \pm \Delta\alpha$ and $\beta \pm \Delta\beta$, the undesired output voltages can be readily derived as

$$v_{oA} - v_{oB} = (g_{m1N} + g_{m1P})\Delta\alpha\frac{R}{2\beta(g_{mb1P}R_F)^2} v_{ic} \tag{32}$$

$$v_{oA} - v_{oB} = (g_{m1N} + g_{m1P})\Delta\beta\frac{R}{g_{mb1P}\beta R_F} v_{ic}. \tag{33}$$

Similarly, these output voltages can be suppressed if $g_{mb1P}\beta R_F$ is large.

### 4.4 Minimum supply voltage and output swing

Based on the proposed circuit topology, the minimum supply voltage is determined by

$$V_{DD(\min)} = V_{TH2N} + V_{DSAT2N} + V_{TH2P} + V_{DSAT2P}, \tag{34}$$

where $V_{TH2N(P)}$ and $V_{DSAT2N(P)}$ are the threshold voltage and saturation voltage of $M_{2NA(B)}$ and $M_{2PA(B)}$, respectively. Obviously, the minimum supply voltage depends heavily upon the threshold voltage. Therefore, process with low threshold voltage can lead to the CMFB, which can operate at lower supply voltage.

As previously mentioned, the impedances of the input current mirrors at nodes A and B are very small, thus causing both nodes operating as virtual ground. As a result, the output swing of the PDA is limited by the output swing of the input transconductor ($G_{m(in)}$) (see Fig. 3) and is determined by

$$V_{DSAT(M_{1NA(B)})} \le V_{OUT(swing)} \le V_{DD} - V_{DSAT(M_{1PA(B)})}. \tag{35}$$

## 5 $R_m$–$C$ bandpass filter application

To demonstrate the performance of the proposed circuit, a transimpedance-Capacitor ($R_m$–$C$) bandpass filter based on single PDA as illustrated in Fig. 5(a) [31] is employed. The capacitor $C_{BF}$ is connected in series with the transimpedance amplifier ($R_m$) formed by the proposed PDA and feedback resistor $R_{BF}$. Since the input impedance of the TA is very low, nodes $E$ and $E'$ can be considered as ac ground.

Hence, differentiator can be obtained by cascading $C_{BF}$ before the TA and the low-frequency transfer function is equal to $sC_{BF}R_{BF}$.

The small-signal equivalent circuit of Fig. 5(a) is depicted in Fig. 5(b), where $g_m$ is the transconductance and $C_X$, $C_Y$ and $C_Z$ are the parasitic capacitances determined by

$$g_m = g_{m1N} + g_{m1P} \tag{36}$$

$$C_X = C_{GS1N} + C_{GS1P} + C_{GB1N} + C_{GB1P} \tag{37}$$

$$C_Y = C_{GD1N} + C_{GD1P} \tag{38}$$

$$C_Z = C_{oL} + C_L \tag{39}$$

The transfer function of the bandpass filter can be expressed as

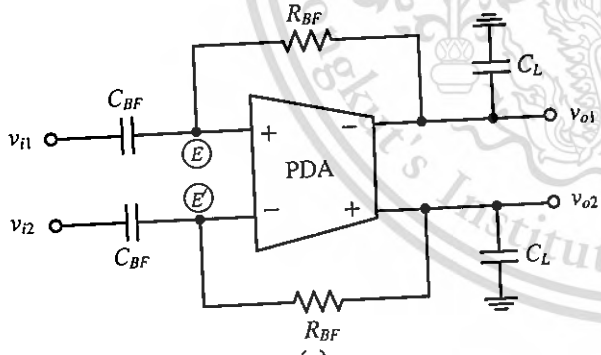
$$H(s) = \frac{v_o}{v_i} \cong \frac{sC_{BF}D}{As^2 + Bs + C} \tag{40}$$

where

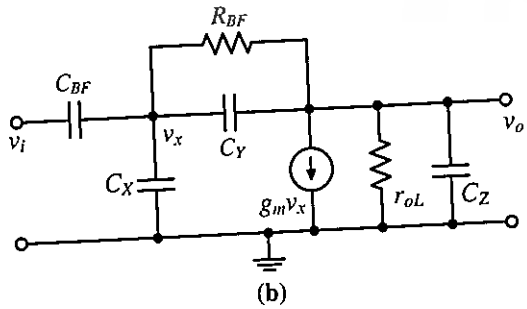
$$A \approx (C_{BF} + C_X)(C_Y + C_Z) + C_Y C_Z \tag{41}$$

$$B \approx \frac{g_m C_Y r_{oL} R_{BF} + (C_{BF} + C_X + C_Y)R_{BF} + (C_Y + C_Z)r_{oL}}{r_{oL}R_{BF}} \tag{42}$$

$$C \approx \frac{g_m r_{oL} + 1}{r_{oL}R_{BF}} \tag{43}$$




(a)




(b)

**Fig. 5** **a** Basic structure of $R_m$–$C$ bandpass filter and **b** simplified small-signal equivalent circuit

$$D \approx \frac{1 - g_m R_{BF}}{R_{BF}}. \tag{44}$$

The centre frequency $\omega_o$ and the quality factor $Q$ of the filter can be expressed as

$$\omega_o = \sqrt{\frac{C}{A}} = \sqrt{\frac{g_m r_{oL} + 1}{r_{oL}R_{BF}[(C_{BF} + C_X)(C_Y + C_Z) + C_Y C_Z]}} \tag{45}$$

$$Q = \sqrt{\frac{AC}{B}} = \sqrt{\frac{[(C_{BF} + C_X)(C_Y + C_Z) + C_Y C_Z](g_m r_{oL} + 1)}{g_m C_Y r_{oL} R_{BF} + (C_{BF} + C_X + C_Y)R_{BF} + (C_Y + C_Z)r_{oL}}}. \tag{46}$$

## 6 Simulation results

To prove the performance and robustness of the proposed PDA, the circuit has been designed and simulated in a standard 0.18 μm CMOS technology using the Cadence Spectre. The threshold voltages are 0.45 and −0.5 V for NMOS and PMOS, respectively. The supply voltage is 1 V and the input and output CM voltages are biased at $V_{DD}/2$, i.e., 0.5 V. The body bias voltage $V_{BP}$ is set to 0.5 V to reduce the threshold voltage of PMOS transistors. The total current drawn from the supply is 102.5 μA. The bias currents of all transistors are chosen to optimize both gain and power dissipation. Resistors $R_{1,2}$ and the impedance at nodes A and B are 50 and 7 kΩ, respectively. The dimensions of transistors are listed in Table 1.

### 6.1 CMFB performance

Figure 6 shows the DC transfer characteristic of the proposed PDA with and without CMFB. The output swing of the PDA demonstrates rail-to-rail operation, while Fig. 7 shows the transient response of the output voltages, when a CM sinusoidal signal with a peak-to-peak value of 10 $mV_{pp}$ (10 kHz) is applied to the inputs. In case of no CMFB circuit, the CM signal is amplified to 0.6 $V_{pp}$. However, the CM signal decreases to 0.4 $mV_{pp}$, when the CMFB is employed; this leads to a CM attenuation of −15 dB and a *CMRR* of 53 dB.

Figure 8 shows the open-loop frequency response of the CMFB circuit with stability compensation. The DC open-loop gain is found to be 40 dB, while the unity-gain frequency is 70 MHz. The circuit is stable and the phase margin is 50°.

### 6.2 Frequency response

Figure 9 shows the frequency response of the PDA when the differential-mode signal is applied to the inputs. The

Table 1 Dimensions of transistors

| Transistors | W (μm) | L (μm) |
|---|---|---|
| $M_{1NA(B)}$ | 5.2 | 0.5 |
| $M_{1PA(B)}$ | 11 | 0.5 |
| $M_{2NA(B)}$ | 0.8 | 0.24 |
| $M_{2PA(B)}$ | 2.6 | 0.24 |
| $M_{3NA(B)}$ | 4.2 | 0.24 |
| $M_{3PA(B)}$ | 13 | 0.24 |
| $M_{4NA(B)}$ | 1.1 | 0.24 |
| $M_{4PA(B)}$ | 3.5 | 0.24 |
| $M_{5NA(B)}$ | 2.5 | 0.24 |
| $M_{5PA(B)}$ | 7.3 | 0.24 |

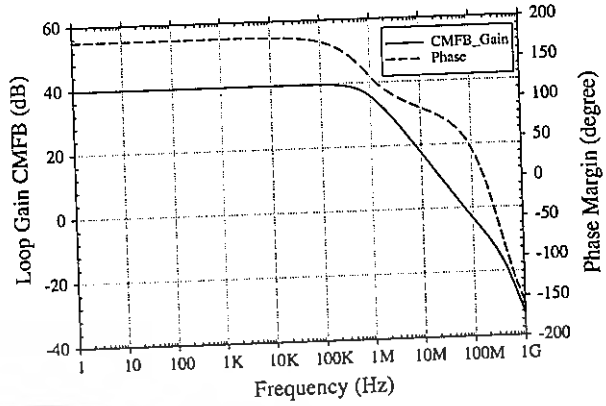



Fig. 8 Open-loop frequency response of the CMFB circuit

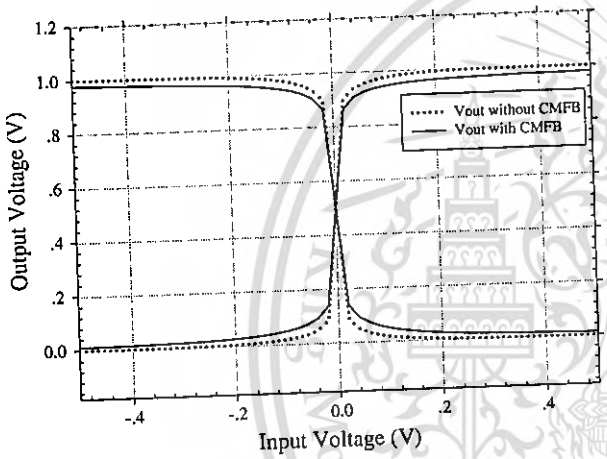



Fig. 6 DC transfer characteristic

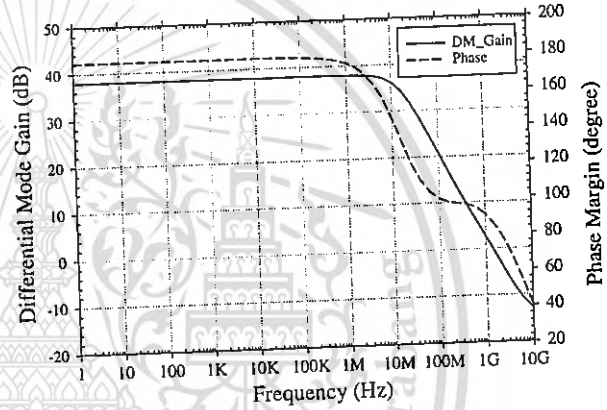



Fig. 9 Differential-mode gain and phase

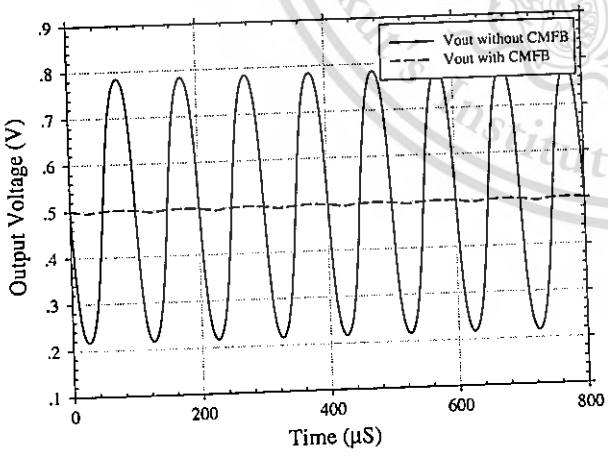



Fig. 7 Output voltages with and without CMFB

DC gain is 38 dB, while the −3 dB and unity-gain frequency are 13.7 MHz and 1.42 GHz, respectively. The phase margin is 86°. Figure 10 illustrates the frequency response of the PDA when the CM input is applied. The CM gain is relatively much smaller (−15 dB), while the bandwidth is almost the same as that of the differential-mode case.

### 6.3 Noise

The input referred noise spectral density is shown in Fig. 11. The input referred noise is less than 1 pV/$\sqrt{\text{Hz}}$ at 10 MHz.

### 6.4 Effect of process and temperature variations on the CM performance

Monte Carlo simulations have been performed so as to check how the process variation and device mismatch affect the *CMRR*. A 1,000-iteration Monte Carlo analysis is carried out using statistical models provided by the foundry. Figure 12 shows the Monte Carlo statistical results of the *CMRR* in the presence of the process variation. The mean value of *CMRR* is 51.8 dB, while the standard deviation is 4.25. The minimum and maximum *CMRRs* are 38 and 58 dB, respectively. The maximum number of

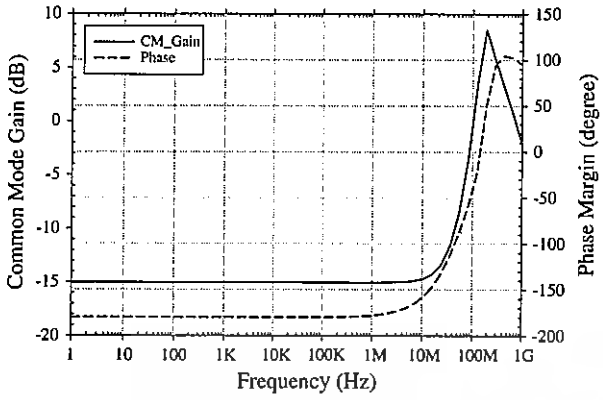



**Fig. 10** CM gain and phase

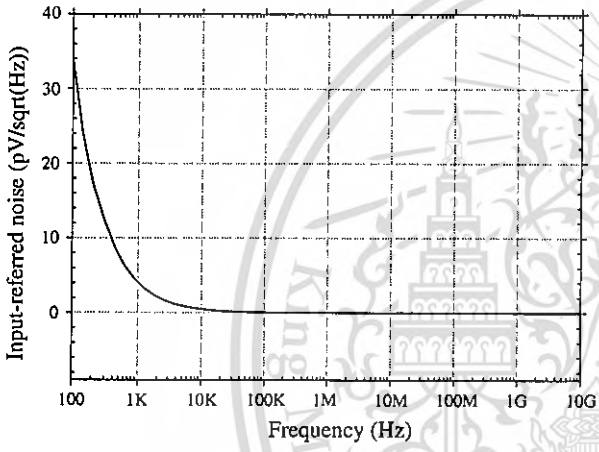



**Fig. 11** PDA input-referred noise

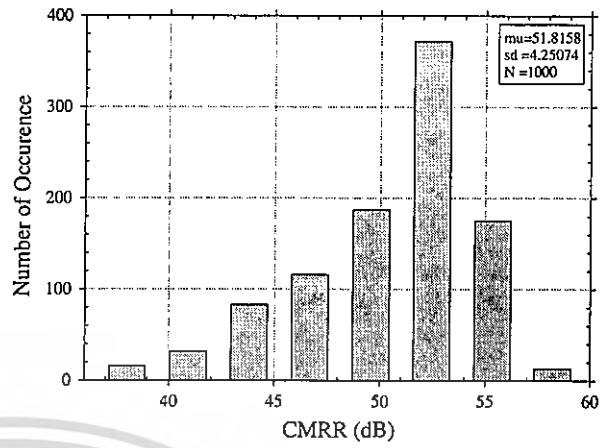



**Fig. 12** Monte Carlo simulation results for *CMRR* with process variation (1,000 runs)

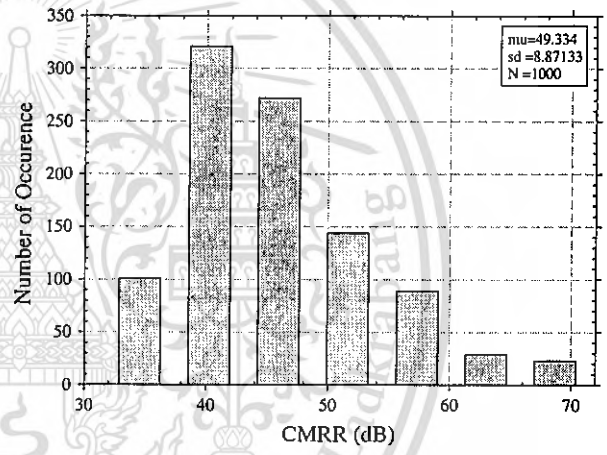



**Fig. 13** Monte Carlo simulation results for *CMRR* with mismatch (1,000 runs)

occurrences is at 52.45 dB. Monte Carlo simulation of the *CMRR* with device mismatches is shown in Fig. 13. The mean value is 49.3 dB, while the standard deviation is 8.87. The Monte Carlo statistical results give the minimum and maximum *CMRRs* of 35 and 69 dB, respectively. The maximum number of occurrences is at 40.3 dB. From Figs. 12 and 13, it is apparent that the device mismatch plays a greater important role than the process variation. Obviously, the use of layout techniques to improve matching becomes mandatory.

Impact of temperature variation on the DC CM voltage is also studied and shown in Fig. 14. The DC CM voltage shows small variation (6 %) when temperature is varied from 0 to 70 °C.

Table 2 shows the performance comparison with recently published transconductors. It is noted that the proposed transconductor operates with rail-to-rail output swing and at low supply voltage. The circuit proposed in [24] is developed based on CMOS inverter-based amplifier. Since the circuit has no internal node, the circuit can operate at high frequencies. The transconductor proposed in [5] is also based on CMOS inverter. The double CMOS pair is biased in the subthreshold region resulting in low-power consumption. Both circuits demonstrate low CMRR mainly due to their low loop gains.

Loop gain is increased in [18] by using two-stage voltage mode amplifier in the CMFB and additional adaptive biasing circuitry. Consequently, high CMRR is achieved. Note that the bandwidth of the circuit is lower than the other implementations because two-stage voltage mode amplifier contains low-frequency poles. This work is based on the CMOS inverter-based PDA and novel current mode CMFB, allowing the circuit to operate at higher frequencies, yet maintain relatively large CMRR. Table 2 also shows the results obtained from theoretical equations and they are in good agreement with those obtained from the simulations.

### 6.5 Application

Figure 15 shows the frequency response of the $R_m$–$C$ bandpass filter ($C_{BF} = 0.25$ pF, $C_L = 0.5$ pF and $R_{BF} = 50$ kΩ). The centre frequency $f_o$ and quality factor $Q$ are 31.62 MHz and 1.66, respectively. Figure 16 shows the variation of the center frequency for various values of $R_{BF}$ and $C_L$ ($R_{BF} = 30$–$120$ kΩ, $C_L = 0.5$ pF and $C_L = 0.3$–$2.1$ pF, $R_{BF} = 50$ kΩ). The power dissipation of the proposed PDA and its application are 102.5 μW.

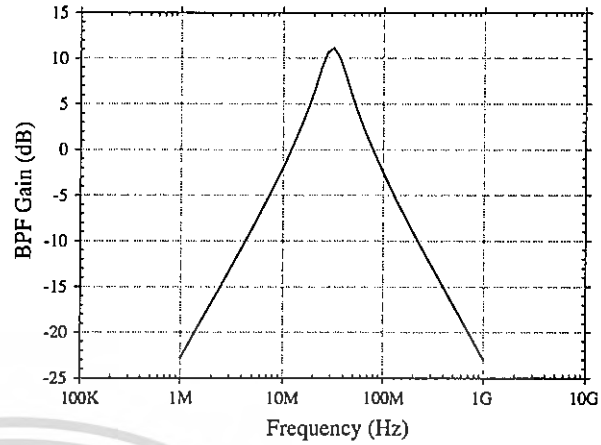



Fig. 15 Frequency responses of the simple $R_m$–$C$ bandpass filter

## 7 Conclusions

In this paper, a CMOS inverter-based class-AB PDA is proposed. The circuit is designed based on a CMOS inverter and low-voltage wide-swing CMFB circuit. The proposed PDA demonstrates rail-to-rail operation. The

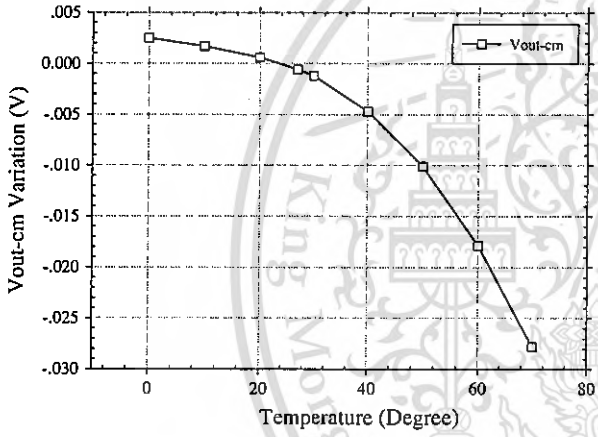



Fig. 14 DC CM voltage variation with temperature

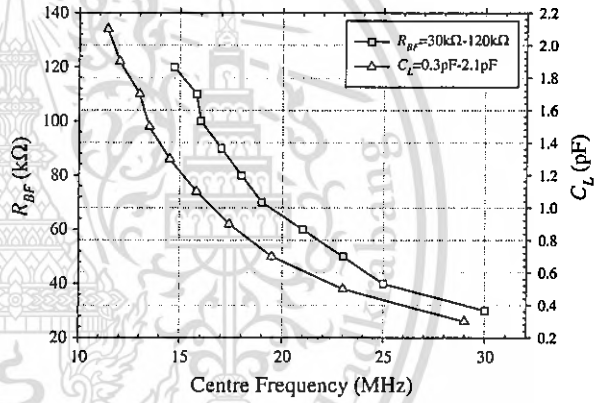



Fig. 16 Center frequency as a function of $R_{BF}$ and $C_L$

Table 2 Performance evaluation

| Parameters | [5] | [18] | [24] | This work (simulation) | This work (calculation) |
|---|---|---|---|---|---|
| Technology (μm) | 0.35 | 0.18 | 0.35 | 0.18 | 0.18 |
| Supply voltage (V) | 3.3 | ±0.9 | 2.5 | 1 | 1 |
| DC gain (dB) | 29.3 | 42 | 31.3 | 38 | 39.9 |
| Phase margin (°) | 82.8 | 90 | 77 | 86 | 90 |
| UGBW | 28.97 MHz | 3.2 MHz | 3.56 GHz | 1.42 GHz | 1.39 GHz |
| CMRR (dB) | 35.19 | 169 | 31 | 53 | 57.36 |
| Maximum output swing (V) | 0.88 | – | 2.27 | 0.72 | 0.8 |
| Linearity | THD = −40 dB @0.3 $V_{pp}$ | HD3 = −65 dB @0.6 $V_{pp}$ | THD = −46 dB @1 $V_{pp}$ | THD = −40 dB @0.5 $V_{pp}$ | – |
| Transconductance | 49.6 nS–12.5 μS | 76 μS | 108.4 μS | 305 μS | 300 μS |
| Input referred noise | 113 nV/√Hz | – | 85 nV/√Hz | 1 pV/√Hz | – |
| Power dissipation (μW) | 44.53 | 250 | 800 | 102.5 | 98 |

simulation results show that the circuit can operate under the supply voltage of 1 V with the differential and CM gains of 38 and −15 dB, respectively. The unity-gain frequency is 1.42 GHz and the power dissipation is 102.5 μW.

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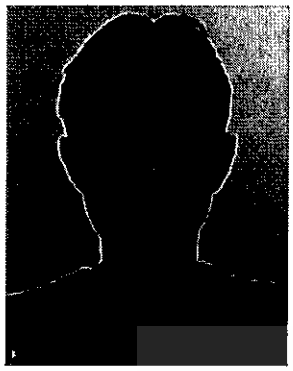

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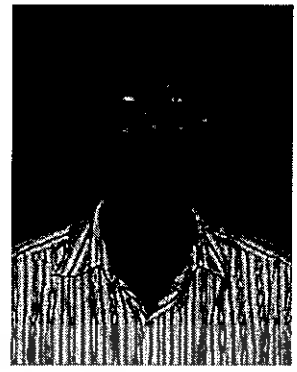

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