INTEGRABLE ELECTRONIC CIRCUITS

ชัยพงษ์ วัฒนไชยประทีป วศ.บ.

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ปีการศึกษา ๒๕๒๖

สารบัญ

กิตติกรรมประกาศ

ขอขอบพระคุณอย่างสูงต่อรองศาสตราจารย์ ดร.สิทธิชัย โภไคยอุดม ในการให้คำปรึกษาและแนะนำในการทำวิทยานิพนธ์นี้ และขอขอบคุณต่อ กอบชัย เดชหาญ

ชัยพงษ์ วัฒนไชยประทีป

บทคัดย่อ

การศึกษาคุณสมบัติต่าง ๆ ของวงจรอีเล็กทรอนิกส์ ซึ่งประกอบไปด้วยอุปกรณ์ชิ้นส่วนเป็นจำนวนมาก และเพื่อให้ได้คุณสมบัติของวงจรเป็นไปตามที่ต้องการ จึงได้ทำการออกแบบวงจรนั้น ๆ ด้วยชิ้นส่วนประกอบดรีสครีท แล้วทำการวิเคราะห์หาข้อมูลต่าง ๆ เพื่อใช้ในการปรับปรุง ซึ่งวงจรที่ได้ออกแบบไว้นี้สามารถนำไปสร้างเป็นวงจรรวมได้ ในวิทยานิพนธ์นี้ได้ออกแบบวงจรเปลี่ยนอุณหภูมิให้เป็นผลต่างของกระแส วงจรดักขนาดสูงสุดของสัญญาณซายน์ และวงจรทรานซิส-เตอร์ตัวเดียวสำหรับทำหน้าที่เป็นเรคติไฟร์

Abstract

Having designed the discrete circuits in order to obtain the desired characteristics. Both the theory and experimental results are demonstrated for improving to be the integrable circuits. Three novel circuits are treated in this thesis, namely, a linear temperature-to-differential-current converter, peak-amplitude detector for sinusoidal signals and a single transistor full-wave rectifier.

where α is a constant conversion rate factor, T and T_0 are absolute temperatures, and I_0 is a constant current. The synthetic resistance magnitude of the circuit in [1] is given by

$$R = \pm R_0(I_1/I_0) \tag{2}$$

where R_0 is a given resistance and I_1/I_0 is a ratio of two biasing currents, and I_1 can possess the form as given in (1). If we further assume that R_0 possesses a low-temperature coefficient, then it can be readily seen from (1) and (2) that the rate of change of R with respect to T is constant and equal to

$$\frac{dR}{dT} = \pm \alpha R_0/I_0. \tag{3}$$

Therefore, by properly choosing α, it is possible to realize general resistances with precisely prescribed temperature coefficients of either positive or negative type, depending upon whether I_1 is increasing or decreasing with temperature.

It is the purpose of this letter to describe a simple and elegant circuit for converting temperature to differential currents linearly, where the conversion rate is programmable and constant over a substantial temperature range.

Slightly simpler circuits for converting temperature to current linearly exist in the literature [2], [3]. However, only increasing current with temperature is readily available. Decreasing current with temperature can be obtained only with additional circuits, resulting in roughly equal overall circuit complexities as the present circuit. However, the circuit method reported in this letter will offer higher conversion rate for the same value of conversion resistance, as well as being a more elegant approach.

Circuit Description

Fig. 1 shows the proposed linear temperature-to-differential-current converter. Let the ratios of the emitter areas of Q_2 to Q_1 and Q_4 to Q_3 be λ. The current mirrors Q_7, Q_8, Q_9 and Q_{10}, Q_{11}, Q_{12} force equal emitter currents to flow through Q_1, Q_2, Q_3 and Q_4, resulting in voltages V_a and V_b equal to

$$V_a = -mV_T \ln \lambda \tag{4}$$

$$V_b = mV_T \ln \lambda \tag{5}$$

where m is a relatively temperature-independent parameter to account for certain nonlinearities in the p-n junction I–V characteristic, having a value in the range from unity to two [4], and $V_T = kT/q$ is the usual thermal voltage associated with a p-n junction. Therefore, the differential current flowing through R' will be equal to

$$i_T = (2mV_T \ln \lambda)/R' \tag{6}$$

where it is seen that if R' possesses a low-temperature coefficient, then i_T is increasing approximately linearly with absolute temperature. The differential temperature-dependent output currents are $(I_2 - i_T)$ and $(I_3 + i_T)$, respectively, where I_2 and I_3 should be chosen such that at a given operating temperature T_0, we have

$$(I_2 - i_T)|_{T_0} = (I_3 + i_T)|_{T_0} = I_0 \tag{7}$$

where I_0 is the required operating current at T_0.

Comparing (6) and (7) to (1), it is seen that the conversion factor is given by

$$\alpha = di_T/dT = (2mV_T \ln \lambda)/TR' \tag{8}$$

which is relatively independent of temperature.

บทที่ 1

วงจรเปลี่ยนอุณหภูมิให้เป็นผลต่างของกระแส

A Linear Temperature-to-Differential-Current Converter

Abstract—A simple circuit is proposed as a linear temperature-to-differential-current converter. Large and accurate conversion rate can be easily obtained. An immediate application has also been proposed.

Introduction

In some applications, it is desirable to have linear temperature-dependent differential currents; for example, in a recently proposed integrable circuit for synthesizing general voltage-variable resistances [1], it is desirable to have a biasing current of the form

$$I_1 = I_0 \pm \alpha(T - T_0) \tag{1}$$

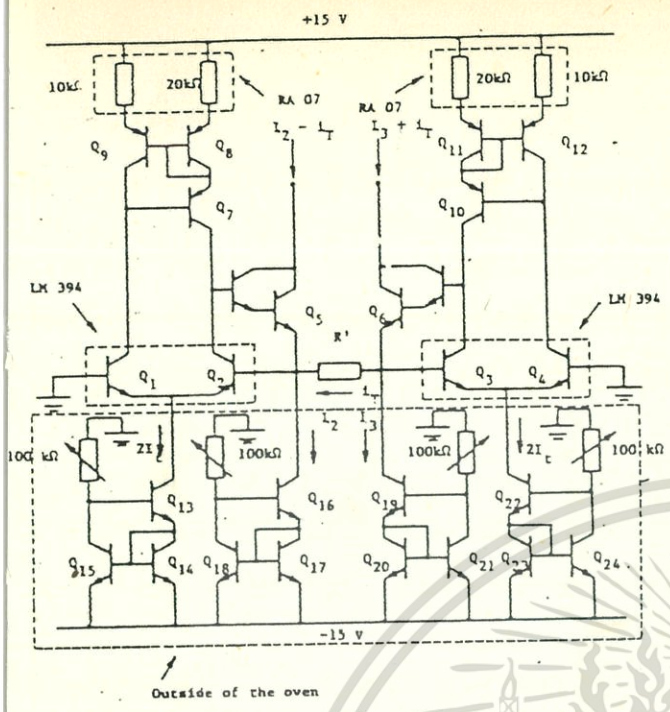

Fig. 2. Actual experimental circuit.

he base currents in their respective circuits do not exactly cancel. However, due to the large β's of the discrete p-n-p transistors used ($\beta > 100$), this effect is relatively unimportant. In practical monolithic circuits, nonunity emitter area ratios would have been employed. Thus the current mirror reflecting ratio can be set to unity and the aforementioned problems can be avoided. The whole circuit, except the bias current sources, was placed in a temperature-controlled oven.

Fig. 3 shows the plots of the differential current versus temperature, for the cases of 50- , 100- , and 200-Ω conversion resistances, respectively. These resistances were of the metal film type, which possess low absolute temperature coefficients of the order of 50 ppm/°C. The vertical axis of Fig. 3 is the difference between the actual current and the current at 30°C. It is clearly seen that very good linearities and accuracies have been achieved, even with a conversion resistance as low as 50 Ω. The measured slopes were approximately 2.5, 1.28, 0.61 μA/°C for 50- , 100- , and 200-Ω conversion resistance, respectively, which is accurately equal to a ratio of 4.0:2.0:1.0 as expected. The maximum measured absolute error was less than ±4 percent in the temperature range of 0 to 100°C.

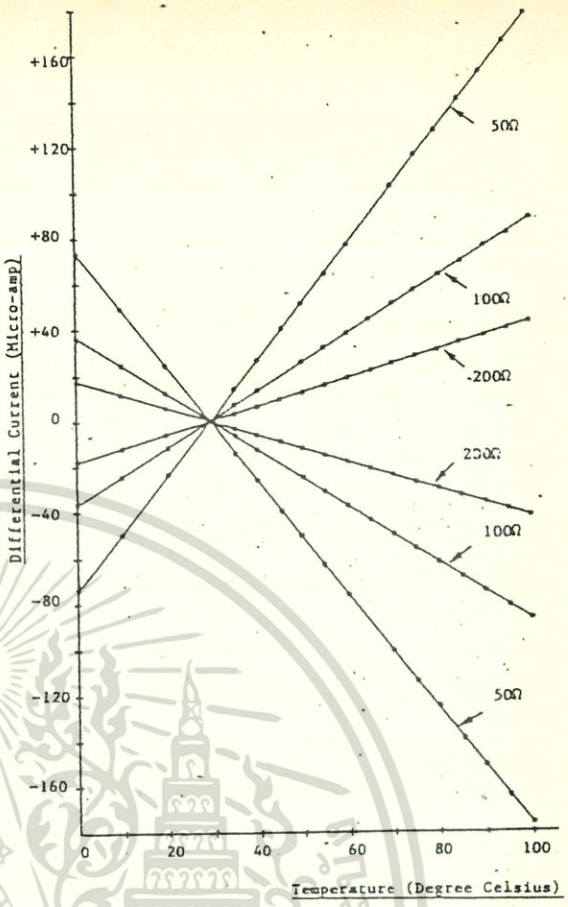

Fig. 3. Experimental results of the linear temperature-to-differential-current converter, with conversion resistances of 50 and 100 Ω.

Conclusions

We have described and experimentally demonstrated a simple and elegant circuit for linear temperature to differential current conversion. The circuit can be employed as part of the previously proposed general resistance converter [1] to obtain general resistances with precisely prescribed temperature coefficients of either positive or negative type.

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บทที่ 2

วงจรดักขนาดสูงสุดของสัญญาณซายน์

PEAK-AMPLITUDE DETECTOR FOR SINUSOIDAL SIGNALS

A circuit technique is proposed for detecting the peak amplitude of a sinusoidal signal using Pythagoras's law without requiring a simultaneous equal-amplitude quadrature signal. The number of four-quadrant multipliers required is only two.

Introduction: Recently, Doorenbosch *et al.*[1] proposed a method of peak-amplitude dete

signals, resulting in the square of the peak amplitude only, in accordance with the following trigonometric identity:

$$(A \sin \omega t)^2 + (A \cos \omega t)^2 = A^2 \tag{1}$$

Doorenbosch *et al.*[1] used the circuit in the automatic volume control of a two-integrator oscillator,[2] whereby the required approximately equal-amplitude quadrature signals can be readily tapped from the closed feedback loop. The various advantages of using this method of amplitude detection over other methods, which involve rectification or peak detection, have already been discussed in Reference 1 and will not be repeated here.

In using the identity in eqn. 1 to detect the peak amplitude of a general sinusoidal signal, a frequency-independent unity-gain quadrature phase shifter will be needed. Simple differentiators or integrators are not useful, since the gain is frequency-dependent. Other conventional methods using network approximations are usually narrow-band and not very accurate. Recently, Barker[3] proposed a wide-band 90° phase shifter without using any reactive element; however, the peak amplitude of the signal must be known beforehand in using the circuit. Surface-acoustic-wave devices[4] can be designed to yield true quadrature taps; however, the method is narrow-band and is applicable only at high frequencies. It appears that there remains the problem of realising a quadrature phase shifter with an accurate 90° phase shift over a wide bandwidth with unity gain.

In this letter we propose a method of overcoming this problem by generating $(A \sin \omega t)^2$ and $(A \cos \omega t)^2$ signals directly, thus avoiding the need for a true wide-band unity-gain quadrature phase shifter.

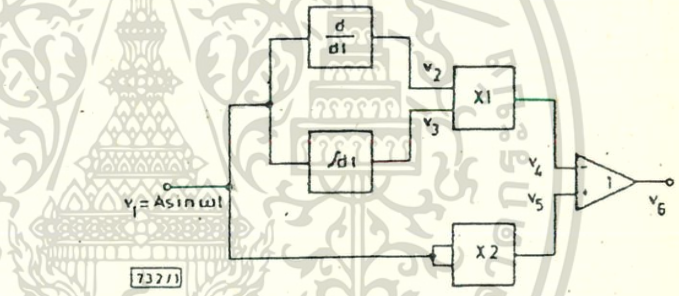

Fig. 1 *Basic circuit diagram of peak-amplitude detector*

Circuit description: Fig. 1 shows the basic circuit blocks of the amplitude detector. Let v_1 be the input sinusoidal signal, with peak amplitude A, and v_2, v_3 be the output signals of the differentiator and integrator, respectively, with equal time constants τ. Therefore, v_2 and v_3 can be written as

$$v_2 = (A\tau\omega) \cos \omega t \tag{2}$$

$$v_3 = -(A/\tau\omega) \cos \omega t \tag{3}$$

v_2 and v_3 are further multiplied by multiplier 1 and the input signal v_1 is squared by multiplier 2. Thus the respective output signals from the two multipliers are:

$$v_4 = -A^2 \cos^2 \omega t \tag{4}$$

$$v_5 = A^2 \sin^2 \omega t \tag{5}$$

v_4 and v_5 are substracted by the unity-gain difference amplifier, resulting in

$$v_6 = A^2(\sin^2 \omega t + \cos^2 \omega t) = A^2 \tag{6}$$

which is the square of the peak amplitude. The peak amplitude itself can be obtained, if required, by using a square-root circuit.

Any deparure from ideality will give rise to distortions in v_6. Important sou[illegible] of nonidealities are:

(*a*) The integrator pole cannot be exactly located on the $j\omega$ axis. Owing to the inevitable presence of offset current charging the integrating capacitor, a parallel resistor is needed

(*b*) The time constants of both the differentiator and the integrator are not exactly equal.

(*c*) The accuracies of the analogue multipliers are limited.

(*d*) The offset voltages from the integrator, the differentiator, the multipliers and the difference amplifier are nonzero.

(*e*) The gains of the difference amplifier are not exactly equal for both signals.

(*f*) Feedthrough exists at the multiplier output.

We will first consider the effect of non-$j\omega$ pole location for the integrator. Usually a large-value resistor R' is needed in parallel with the integrating capacitor. If we let $\tau = RC$ be the integrator and the differentiator time constants, then it can be readily shown that the effect of R' upon the output signal of multiplier 1 can be written as

$$v_4 = \frac{-A^2}{(1+\varepsilon^2/\omega^2\tau^2)^{1/2}} (\cos\gamma\cos^2\omega t - \tfrac{1}{2}\sin\gamma\sin 2\omega t) \qquad (7)$$

where $\varepsilon = R/R' \ll 1$, and $\gamma = 90° - \tan^{-1}(\omega\tau/\varepsilon)$ is a very small angle. Thus the main effects are the introduction of small second-harmonic distortions and a slight frequency dependence of the output-signal amplitude.

Error sources 2, 3 and 5 result in unequal magnitudes of the terms $\cos^2\omega t$ and $\sin^2\omega t$, resulting also in slight second-harmonic distortions.[3] The offset signals from the outputs of the integrator and the differentiator will cause fundamental feedthrough at the output of integrator 1 as well as an increased d.c. offset voltage. Any fundamental feedthrough signal at the multiplier outputs will be simply transmitted by the difference amplifier. Further error will result if a square-root circuit is employed to obtain the peak amplitude signal instead of the square of the peak amplitude.

The bandwidth of the practical circuit, with fixed time constants for both the differentiator and the integrator, will be primarily determined by the dynamic ranges and the noise levels of both circuits. At very low frequencies, the differentiator output signal can become too low and the integrator output signal can become saturated. At high frequencies, the reverse is true.

Experimental results and discussions: The circuit of Fig. 1 has been constructed and the operation has been experimentally verified. LF351 f.e.t. input operational amplifiers have been employed for the differentiator, integrator and difference amplifier. The output offset voltages of these functional circuits have been nulled to values smaller than $\pm 0{\cdot}5$ mV. MC1595s have been employed in the four quadrant multipliers, where care has been taken to ensure that the conversion gains of both multipliers are identical to each other. The output offset voltage of each multiplier has also been nulled to a value smaller than $\pm 0{\cdot}5$ mV. The time constants of the integrator and differentiator have been adjusted, such that they are within $\pm 5\%$ of each other. The total system gain has been set at 1/100. Therefore, for a peak input amplitude of 10 V, the expected output voltage will be 1 V.

Fig. 2 shows the plot of the output voltage of the difference amplifier against the peak amplitude of the input sinusoidal signal, with fixed frequency at 1 kHz. It is seen that the slope of the output voltage versus the input voltage is accurately equal to 2 as expected. The accuracy, however, deteriorated when the signal amplitude is low. This is due to the fact that the output signal level is of the same order of magnitude as the output offset voltage. The amplitude flatness with respect to frequency has been checked by keeping the input signal amplitude fixed at 2 V and varying the signal frequency. We have measured an amplitude deviation of less than $\pm 2\%$ within the frequency range where the peak output signals from the integrator or the differentiator are greater than 10 mV, up to just before saturation. In the present experimental circuit, fundamental feedthrough and second-harmonic distortion also deteriorated as the input signal amplitude decreased. At 100 mV peak input-signal amplitude, the peak-peak second-harmonic distortion was approximately 30% of the average output-voltage level, whereas in the range 1–10 V peak input-signal amplitude these distortions decreased to less than 1% of the average output voltage.

We are investigating the practical possibility of employing the described peak-amplitude detector in the automatic volume control of Wien bridge oscillators.

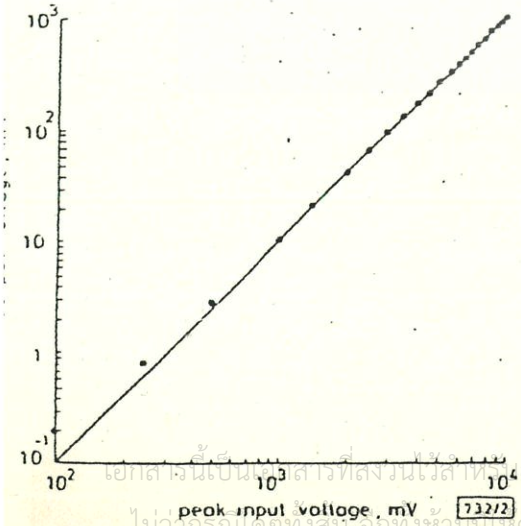

Fig. 2 *Plot of output voltage against input peak voltage of 1 kHz sinusoidal signal*

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บทที่ 3

วงจรทรานซิสเตอร์ตัวเดียวสำหรับทำหน้าที่เป็นเรคติไฟร์

A Single-Transistor Full-Wave Rectifier

Abstract—A simple full-wave rectifier using only a single transistor with two matched resistors has been proposed and the basic performances have been experimentally demonstrated.

I. Introduction

Full-wave rectifiers, which are also referred to as absolute value circuits, are widely useful in various electronic systems, for example, in the compander [1] and expander [2] circuits in telephone systems. Several methods of designing precision full-wave rectifiers can be found in [1]–[5]. However, all these existing circuits are rather complicated; for example, in the circuits of [1] and [2], the full-wave rectifiers actually occupy a substantial area of the silicon chips.

In this letter, a very simple full-wave rectifier using only a single transistor and two matching resistors will be described. The circuit is capable of precise rectification with reasonably large amplitude signal and it is suitable to be employed both in the discrete and integrated applications.

II. Circuit Operation

Fig. 1 shows the circuit of the proposed full-wave rectifier. The two resistors are assumed to be closely matched. The base bias voltage V_B is assumed to be just high enough to drive the transistor into saturation, where in the case of symmetrical V_{cc} and V_{EE}, the required V_B is approximately equal to V_{BE} of the transistor. For a first-order description of the circuit operation, we further assume that the collector-emitter saturation voltage ($V_{CE\,sat}$) and the base-emitter voltage (V_{BE}) of Q_1 are constant. Now as the signal voltage v_{in} goes negative, Q_1 is out of saturation and the output signal voltage is equal to

$$v_o|_{v_{in}\ \text{negative}} \simeq (R/R)|v_{in}| \simeq |v_{in}|. \tag{1}$$

When the signal voltage v_{in} goes positive, Q_1 is driven further into saturation; and, since $V_{CE\,sat}$ and V_{BE} are assumed to be constant, then

$$v_o|_{v_{in}\ \text{positive}} \simeq v_{in}. \tag{2}$$

From (1) and (2), it is clearly seen that the circuit operates as a full-wave rectifier.

Departure from ideality in the actual circuit leads to inaccuracy in the output signal. The major cause of inaccuracy is due to the variation of $V_{CE\,sat}$ with signal amplitude at low-signal level. Other secondary causes of inaccuracy are due to mismatches in the two resistors, effects of finite β of Q_1 resulting in unequal collector and emitter currents, as well as the variation of V_{BE} with signal amplitude. At high frequencies, further distortion results from the finite delay time for the transistor to come out of saturation. In addition, both $V_{CE\,sat}$ and V_{BE} are strongly temperature dependent, which further contributes to the output inaccuracy.

It can be readily shown that the cumulative distortions due to all secondary causes can be easily made less than ±1 percent. In integrated form, the required unity ratio tolerance of the matching resistors of better than ±0.5 percent can be easily achieved [6]. The inaccuracy due to finite β is negligible, provided that β is greater than 300, while the inaccuracy due to V_{BE} variation can also be made less than ±0.5 percent, for input voltage swings between $V_{cc}/2$ and $V_{EE}/2$. Therefore, the major cause of distortion, particularly at low-signal level, is due to variation of $V_{CE\,sat}$.

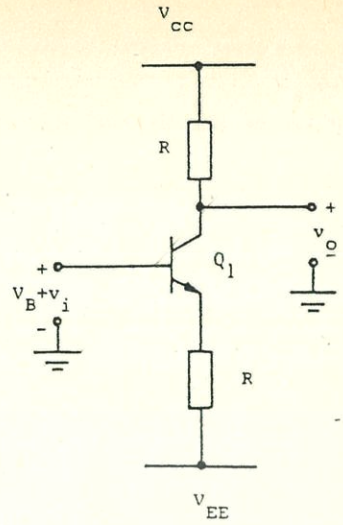

Fig. 1. The basic single transistor full-wave rectifier.

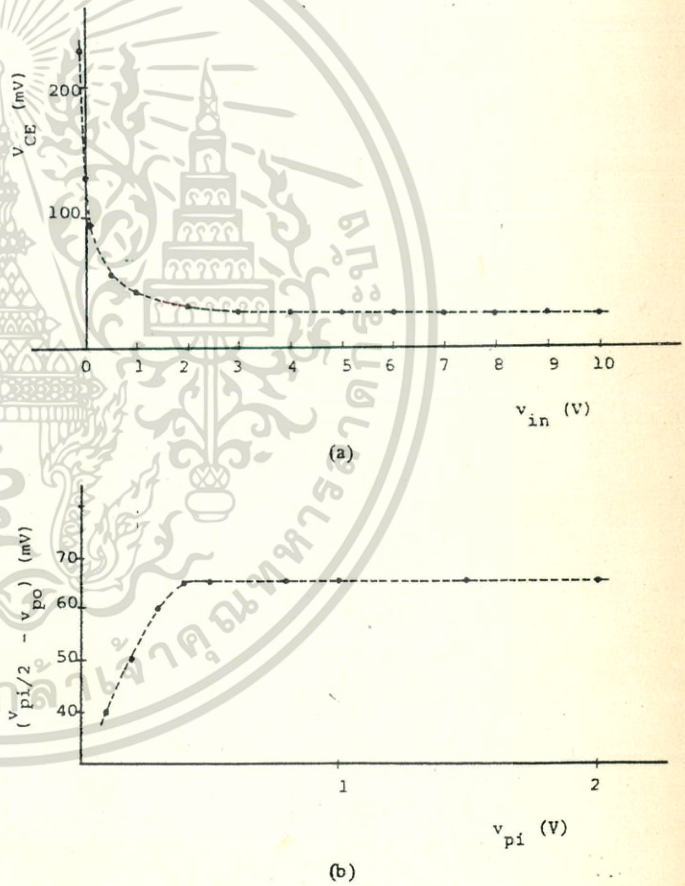

Fig. 2. (a) Plot of V_{CE} versus v_i. (b) Plot of $(V_{pi}/2 - V_{po})$ versus v_{pi}.

Fig. 2(a) shows the experimental plot of $V_{CE\,sat}$ versus v_{in}, when V_B is set such that the circuit gives the best full-wave rectified sinusoidal waveform. An estimate of the variation of $V_{CE\,sat}$ with input signal level can also be made analytically using the idealized Ebers–Moll model, resulting in an equation similar to (1.9b) of [7]. It is seen

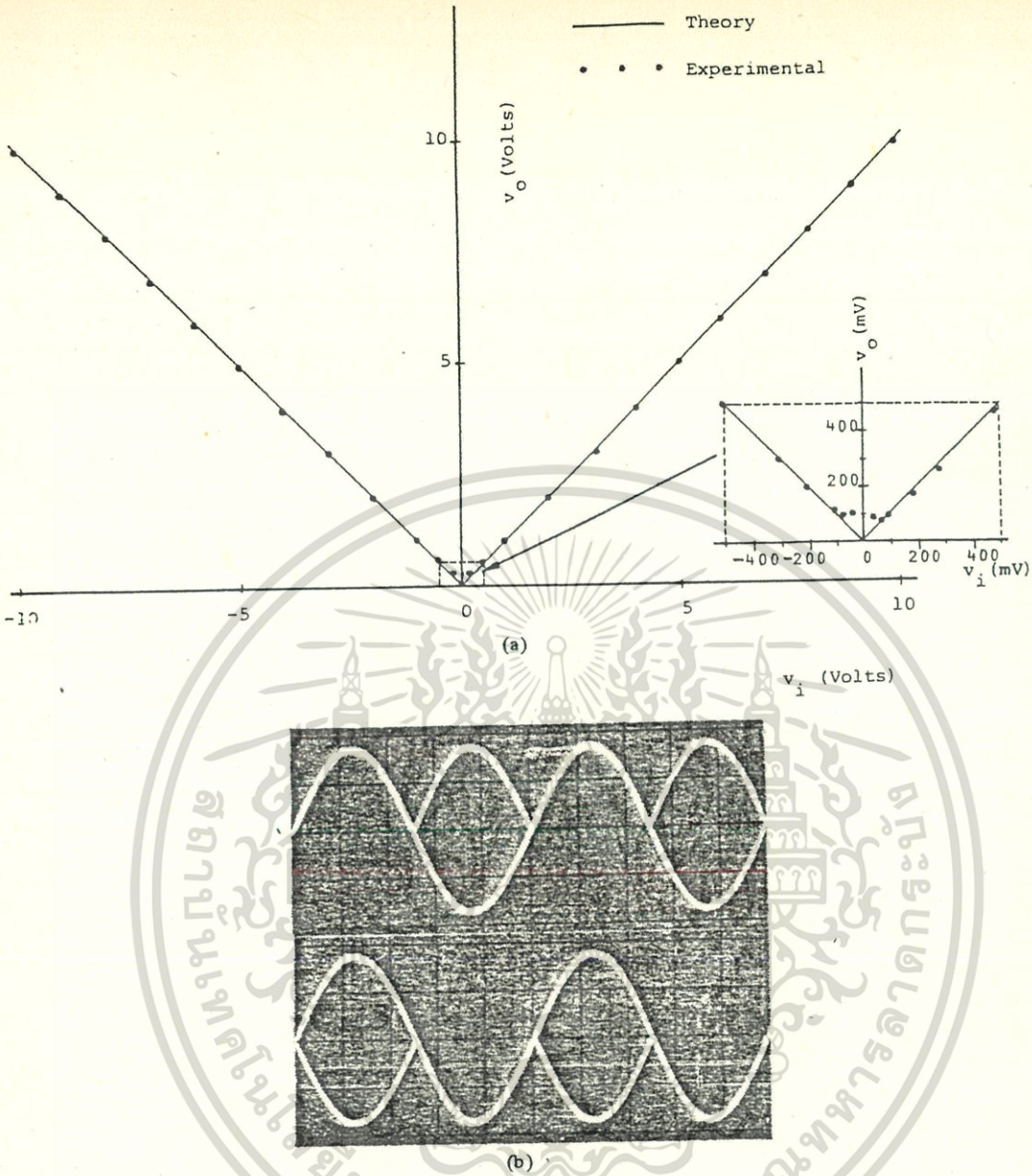

Fig. 3. (a) Plot of v_o versus v_i. (b) Oscilloscope traces of v_o versus v_i.

from Fig. 2(a) that the transition between the saturated and the unsaturated regions of the transistor is gradual, resulting in rapid $V_{CE\,sat}$ variation with v_{in} of less than +500 mV, such that the bottom peaks of full-wave rectified waveform are rounded. Therefore, the peak voltage of output waveform (v_{po}) is less than half of the peak-to-peak voltage (v_{pi}) of the sinusoidal input signal. Fig. 2(b) shows the plot of ($v_{pi}/2 - v_{po}$) versus the peak of the input voltage (v_{pi}). It is seen that this difference voltage remains relatively constant at 65 mV for peak input voltage of greater than 500 mV. Therefore, for large input signal, with peak voltage of several volts, the effect of nonzero ($v_{pi}/2 - v_{po}$) is negligible.

III. Experimental Performance

Fig. 3(a) shows the plot of the output voltage (v_o) versus the input voltage (v_i), where it is seen that both the accuracy and linearity are good for v_i greater than ±100 mV. The exploded view of the plot for v_i less than ±500 mV exhibits relatively large amount of distortions, particularly when v_i is less than ±50 mV. Therefore, in its present simple form, the circuit is useful only for relatively large input signal. Fig. 3(b) shows the superpositioned traces of the sinusoidal input signal with the full-wave rectified output signal, where the peak-to-peak amplitude of the input signal is 5 V. It is seen that the circuit performance is very good as a full-wave rectifier, when the peak signal amplitude is relatively large.

Distortions due to saturation delay time begin to be noticable only when the input frequency is several tens of kilohertz or higher.

The basic circuit performance can be improved by using additional circuits; for example, a relatively straightforward additional integrable circuit can be employed to keep the collector current constant, so that $V_{CE\,sat}$ becomes less dependent upon the input signal amplitude. Distortions due to the variation in V_{BE} can also be virtually eliminated by employing additional differential-pair voltage follower. Although improved performances can be obtained, the resulting overall circuit become rather complicated, and the advantage of single transistor simplicity is lost.

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บทที่ 4

บทสรุป

ได้ทำการออกแบบทดสอบวงจรต่าง ๆ ซึ่งก็ได้ให้ผลดีแต่อย่างไรก็ดี ในอนาคตก็ควรจะปรับปรุงให้ดีกว่านี้ยิ่ง ๆ ขึ้นไปอีก แน่นอนว่าวงจรต่าง ๆ เหล่านี้จำเป็นต้องพิจารณาเป็นอย่างยิ่งต่อสภาวะแวดล้อม วงจรที่สร้างและออกแบบเป็นลักษณะดีสครีท แต่เมื่อได้มีการออกแบบเป็นวงจรรวมแล้วผลของการชดเชยต่อสภาวะแวดล้อมจะมีพอ ๆ กันเป็นการเฉลี่ยกันออกไป แน่นอนว่าผลที่ได้ย่อมดีขึ้นไปอีก

บทความและหนังสืออ้างอิง

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An Integrable Electronically Variable Phase Shifter

S. POOKAIYAUDOM, K. DEJHAN, AND
C. WATANACHAIPRATEEP

Abstract—An easily integrable electronically variable phase shifter is proposed and experimentally demonstrated. The circuit operation is in the current mode, and it can be directly employed as a subsystem of monolithic circuit. A temperature compensated biasing circuit has also been suggested.

I. Introduction

Phase shifters, having constant frequency independent gains, with electronically variable phase shifts, are widely useful in many applications, for example, they can be employed as the frequency determining elements in electronically tunable oscillators, or they can be directly employed as phase modulators in communication systems. Many phase shifting circuits exist in the literature. However, the majority of them have been designed using one or more operational amplifiers in conjunction with passive RC elements [1], [2]. Hence they are not easily tunable electronically. In addition, they usually operate in voltage mode. Thus, it is inconvenient to employ these existing circuits as subsystems of monolithic circuits, since additional current-to-voltage and voltage-to-current converters will usually be needed.

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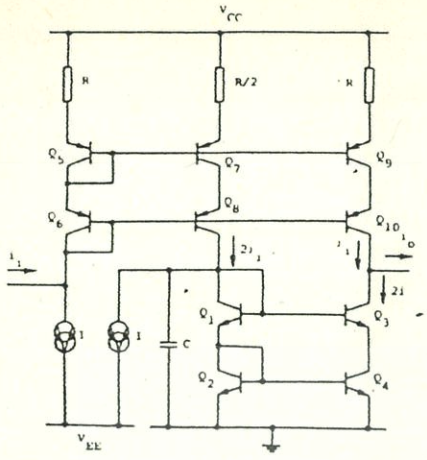

Fig. 1. Practical circuit implementation of the basic phase shifter.

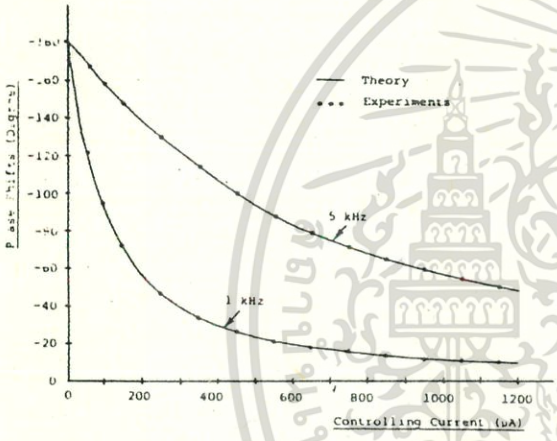

Fig. 2. Experimental results of the basic phase shifter of Fig. 1.

In this letter, a simple integrable electronically variable phase shifter will be presented, where the phase shift is controlled by a current. The circuit also operate in current mode. Thus it can be directly employed in many monolithic circuits without extra conversion stages.

II. Theory

Let r_e be the small-signal forward-biased diode resistance, and i_i be the input signal current of the phase shifter. Suppose, for the moment, that i_i passes through a single pole low-pass filter with a time constant of $2r_eC$, then we have:

$$i = i_i/(1 + s2r_eC). \tag{1}$$

Let the output signal current of the phase shifter be:

$$i_0 = 2i - i_i \tag{2}$$

where upon substituting (1) into (2), we have:

$$i_0/i_i = (1 - s2r_eC)/(1 + s2r_eC) \tag{3}$$

which possesses unity amplitude independent of frequency.

The phase of the transfer function (3) is given by:

$$\phi = -2 \tan^{-1} (\omega C 2r_e). \tag{4}$$

Let I be the diode forward biased current and V_T be the usual thermal voltage associated with a p–n junction, we can then write (4) as:

$$\phi = -2 \tan^{-1} (2\omega C V_T/I) \tag{5}$$

where it is seen that for $0 < I < \infty$, we have $-\pi < \phi < 0$. Therefore, in principle, phase shifts of close to 0 and $-\pi$ can be obtained with very large and very small biasing current; respectively. However, in practice the uppper biasing current limit is around 10 mA due mainly to excessive current drifts of current sources at higher current level, while the lower bound is limited by the level of acceptable signal distortions generated by the diode nonlinearities. Thus, the practical range of obtainable phase shift from a single stage phase shifter is substantially smaller than the maximum range of 0 to $-\pi$. However, a phase shift range of greater than $\pi/2$, centered around $-\pi/2$, can always be obtained for a given frequency with judicious choice of the capacitance C.

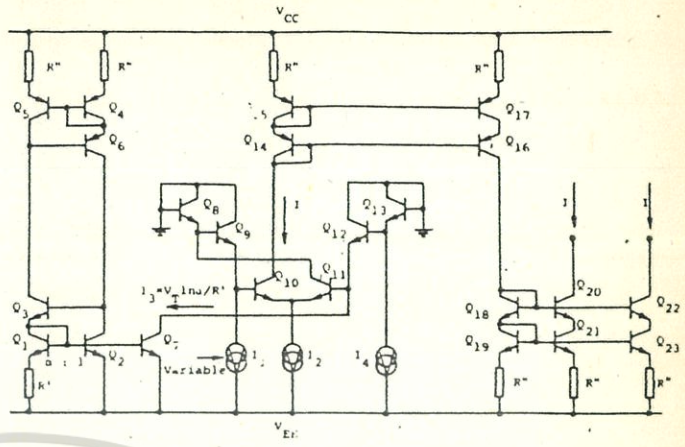

Fig. 3. Improved biasing circuit for temperature compensation.

III. Practical Circuit Implementation

Fig. 1 shows a practical realization of integrable circuit which will give a transfer function of the form given by (3). Many other variations are also possible. Basically transistors Q_1 to Q_4, with C shunting Q_1 and Q_2, perform as a low-pass cascode current mirror filter, having its pole location controllable by the magnitude of the bias current I. The output signal current $2i$ is related to the input signal current $2i_i$ by (1). Transistors Q_9 and Q_{10} also reflect input current i_i to the collector of Q_3, giving an output current i_0 as defined in (2).

Fig. 2 shows the experimental results of the circuit of Fig. 1, which has been simulated with n-p-n transistor array (LM3046) and selectively matched discrete p-n-p transistors. It is readily seen that the experimental results agree well with the theory of previous section. It has also been experimentally confirmed that for a fixed amplitude input signal current, distortions which are primarily second harmonic increase as the diode bias current decreases. Therefore, to ensure reasonably large signal current amplitude dynamic range, the diode bias current should not be lower than 200 μA. At this current level, a signal current amplitude of 10–15 μA does not produce any appreciable distortion.

IV. Circuit Improvements

Two disadvantages are apparent in the phase shift expression of (5). First, it is strongly temperature dependent due to the presence of the thermal voltage V_T. Secondly, the phase shift decreases with increasing controlling current, which can become inconvenient in actual applications, where increasing phase shift with controlling current characteristic is usually preferred. Fig. 3 shows a biasing circuit which reduces both the aforementioned disadvantages. Transistors Q_1 to Q_7 generate a temperature dependent current I_3 given by [3]:

$$I_3 = V_T \ln \alpha / R' \tag{6}$$

where α is the ratio of the emitter areas of Q_1 to Q_2, while transistors Q_8 to Q_{13} generate a current I given by [4]:

$$I = I_3 I_4 / I_1 = V_T I_4 \ln \alpha / I_1 R' \tag{7}$$

where I_1 is a variable current. The current I is then reproduced into two tracking currents by transistors Q_{14} to Q_{22}, which are then employed to bias the two diode branches of Fig. 1. Upon substituting (7) into (5), we have:

$$\phi = -2 \tan^{-2} \{\omega (2CR'/I_4 \ln \alpha) I_1\} \tag{8}$$

where it is seen that, provided that $CR'/I_4 \ln \alpha$ possesses low temperature coefficient, the resulting phase shift ϕ is relatively temperature independent, and is increasing with I_1, which is now the controlling current.

Conclusions

We have proposed and experimentally demonstrated a simple integrable electronically variable phase shifter. A temperature compensated biasing circuit, which also inverts the phase shift controlling current relationship, has also been described.

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Electronically tunable filter blocks

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Circuit blocks, suitable for integrated circuits, for realizing electronically tunable high-pass and low-pass filters, where the relationship between the controlling signal and the cut-off frequency can be both linear and inverse, are presented.

1. Introduction

Filters with electronically tunable characteristics are very useful in many applications, for example in adaptive filtering. Electronic tunability can be easily realized by varying the bias currents of pn-junction diodes, which form parts of the *RC* circuit. Grimbleby (1977) described one such approach using a capacitively emitter-coupled differential quartet (Pookaiyaudom and Kuhanont 1977). Recently, Pookaiyaudom *et al.* (1979) also described another circuit, relying upon the same basic principle of varying the pn-junction forward biased diode resistance, to obtain an electronically tunable all-pass network. The use of a capacitively emitter-coupled differential quartet in the approach of Grimbleby (1977) resulted in a great deal of difficulty with instability. In the second approach of Pookaiyaudom *et al.* (1979), a capacitively loaded current mirror has been employed, resulting in a circuit free from potential instability.

In this paper, we shall propose and experimentally demonstrate electronically tunable low-pass and high-pass filter blocks, also relying upon the principle of variation of the forward biased resistances of pn-junction diodes. These filter blocks can be cascaded to form a tunable band-pass filter, where the centre-frequency and the bandwidth can be independently tuned. The circuit principle as will be proposed here is suitable for integrated circuits. A biasing circuit to obtain temperature insensitivity will also be described.

2. The basic circuit blocks

Figure 1 shows the basic low-pass filter. Transistors Q_1 to Q_4 form a cascode current mirror, with capacitor C_1 connected parallel to the mirror input. It can be readily shown that the circuit transfer function is given by:

$$i_o/i_i = 1/(1 + S2r_eC_1) \tag{1}$$

where the cut-off frequency is given by

$$\omega_{3dB} = 1/2r_eC_1 = I_1/2mV_TC_1 \tag{2}$$

where V_T is the usual thermal voltage associated with a pn-junction and I_1 is the diode bias current, r_e is the small-signal forward biased diode resistance; and m is the

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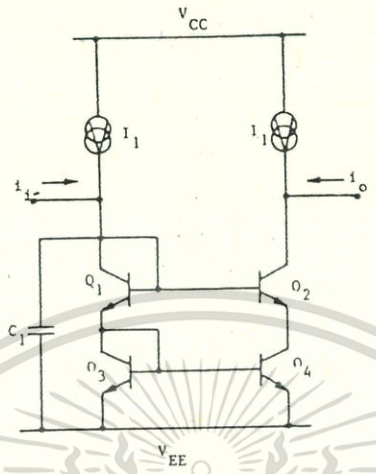

Figure 1. The tunable low-pass circuit.

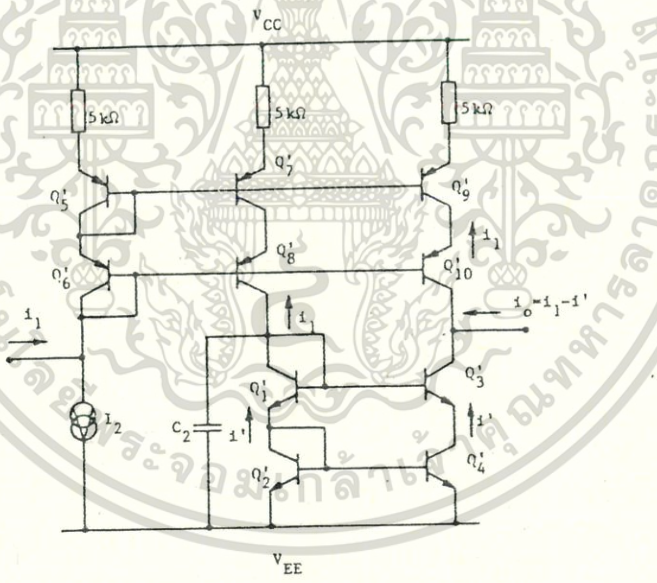

Figure 2. The basic high-pass circuit.

usual parameter accounting for certain non-linearities in the diode characteristic, having its value lie in the range between 1 and 2.

Figure 2 shows the basic high-pass filter, where it can be easily shown that the transfer function, in the case of perfect current mirror matching, is given by

$$i_o/i_i = S2r_eC_2/(1+S2r_eC_2) \tag{3}$$

The cut-off frequency is again given by

$$\omega_{3dB} = 1/2r_eC_2 = I_2/2mV_TC_2 \tag{4}$$

It is seen that in both cases of eqns. (2) and (4), the lower and upper cut-off frequencies are linearly related to the bias currents I_1 and I_2 respectively. The signal currents in both cases should also be considerably smaller than the biasing currents, so that the non-linearities resulting from the exponential forward bias characteristics of diodes are small. Therefore, the minimum biasing current will be determined by the magnitude of the peak signal current. In practice, the biasing current should be kept at least an order of magnitude greater than the maximum peak signal current. The upper limit of the biasing current is primarily limited by the increased inaccuracy in eqns. (1) to (4), since at high current levels r_es are small and various series contact and semiconductor bulk resistances are becoming more significant. From our experiments using integrated transistor arrays (CA3046), a practical upper limit of the biasing current is around 5 mA. If the maximum peak signal current is limited to 10 μA, then a practical variation range in the biasing current is from 100 μA to 5 mA, resulting in a dynamic range of 50, which is adequate for most applications.

The effect of current mirror mismatches in the circuit of Fig. 1 will result in an equation of the form

$$i_o/i_i = (1+\varepsilon_1)/(1+S2r_eC_1) \tag{5}$$

where ε_1 is a small number, resulting from the mismatches associated with Q_1 to Q_4 and also between the two biasing current sources.

In the circuit of Fig. 2, if ε_2 be a small number associated with the mismatches in Q_1' to Q_4' and Q_5' to Q_8', and ε_3 be a small number associated with the mismatches in Q_5', Q_6', Q_9' and Q_{10}', then

$$i_o/i_i = [(\varepsilon_3-\varepsilon_2)+S2r_eC_2(1+\varepsilon_3)]/[1+S2r_eC_2] \tag{6}$$

where it is seen that the main effect due to mismatches is that the current gain approaches a finite value $(\varepsilon_3-\varepsilon_2)$ as the frequency decreases towards zero.

3. Experimental results

Figures 3 (*a*) and (*b*) show the experimental plots of the current transfer functions of the circuits in Figs. 1 and 2 respectively. The theoretical plots of perfect matching cases in eqns. (2) and (4) have also been displayed for comparison. In both circuits all npn transistors are in the form of array (CA3046), while selectively matched discrete pnp transistors have been used for the negative current mirrors. The V_{BE} matching of these discrete pnp transistors have been selected to be better than ± 1 mV. The emitter balancing resistors in the circuit of Fig. 2 have 1% tolerances. It is seen from Fig. 3 that in the case of the low-pass filter the measured performance agreed well with theory even at frequencies well beyond the cut-off point, while in the case of the high-pass filter current mirror mismatches limit the attenuation factor as the frequency decreases. In our calculations, an m value of 1·15 has been used.

Figures 4 (*a*) and (*b*) show the plot of the measured 3 dB cut-off frequencies versus the biasing current for both cases of the low-pass and high-pass filters respectively. The results clearly show that the 3 dB cut-off frequency varies linearly with the biasing current, having both positive slope and origin intercept, as expected from eqns. (2) and (4) respectively.

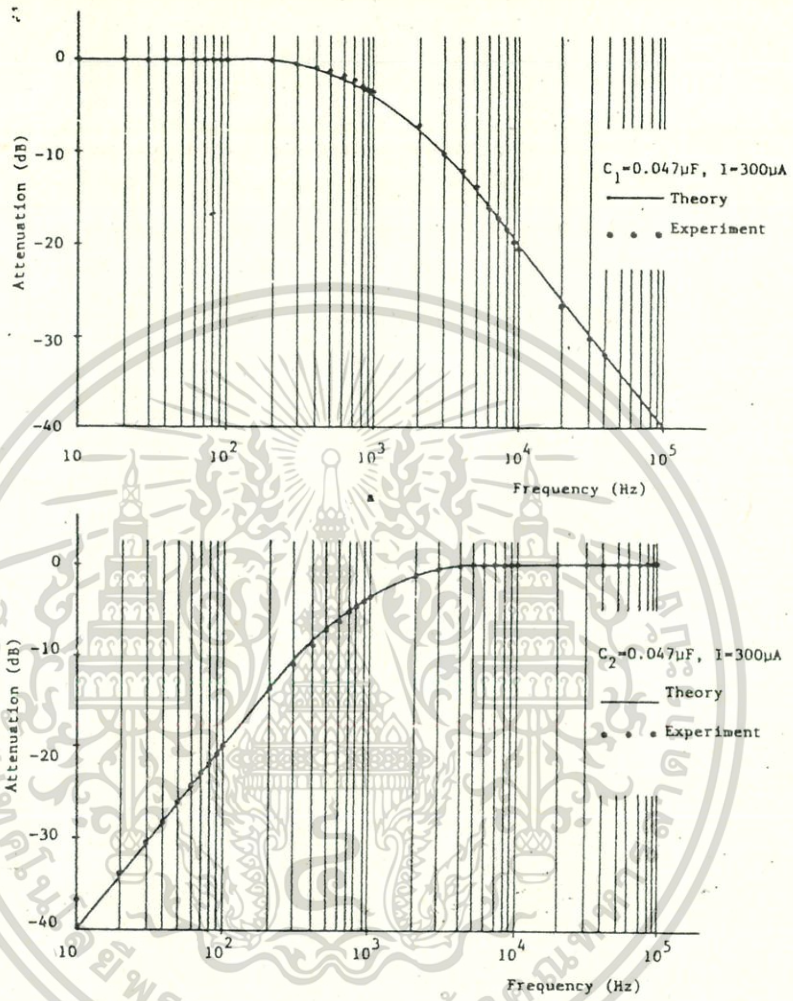

Figure 3. (*a*) Plot of the amplitude characteristic of the low-pass circuit. (*b*) Plot of the amplitude characteristic of the high-pass circuit.

4. Temperature compensation

From eqns. (2) and (4), it is seen that the 3 dB cut-off frequencies are inversely proportional to the thermal voltage V_T, which is itself linearly related to the absolute temperature T. Therefore, the 3 dB cut-off frequencies, at the moment, show a strong inversely related relationship with the absolute temperature. This apparent disadvantage can be readily corrected by using temperature-dependent current sources. Figure 5 shows such a suitable biasing circuit, generating a linearly variable current as well as being directly related to the absolute temperature. Transistors Q_1 to Q_7 generates a temperature dependent current (van Kessel and van de Plassche 1971) of the form

$$I_3 = (V_T \ln \alpha)/R' \tag{7}$$

where α is the emitter area ratio of Q_1 to Q_2. The emitter balancing resistors R's are used to help balance the current ratio of the negative current mirror, where in our

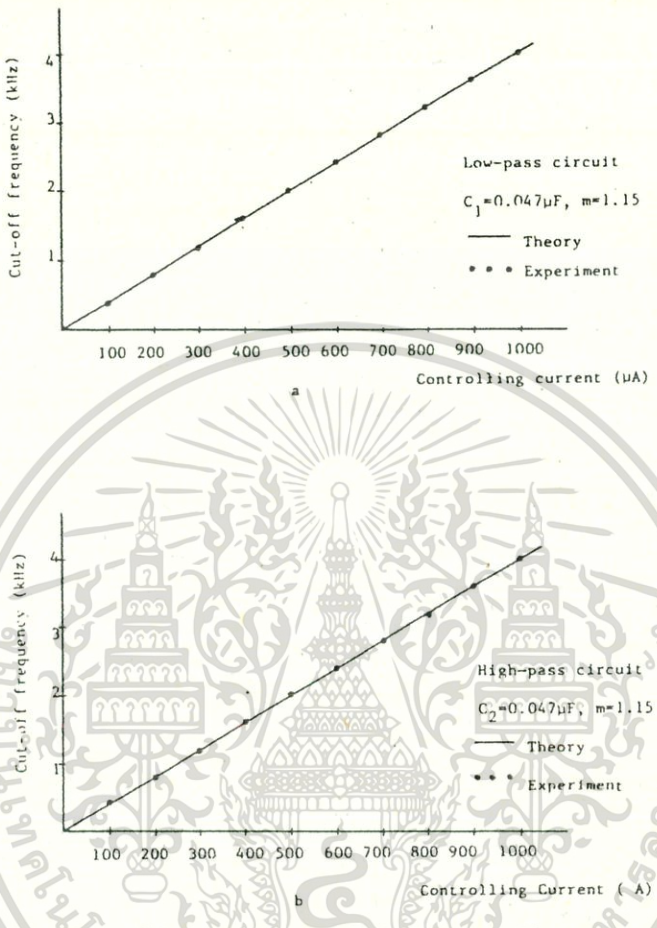

Figure 4. Plots of the cut-off frequencies versus the controlling current for (*a*) the low-pass circuit and (*b*) the high-pass circuit.

experimental circuit we have employed discrete pnp transistors, while in an actual monolithic circuit low performance lateral pnp transistors would be employed instead. Both cases would require emitter balancing resistors to obtain adequate unity current ratio accuracy.

Transistors Q_8 to Q_{13} generate an output current I of the form (Gilbert 1968)

$$I = I_4 I_3 / I_5 = V_T (\ln \alpha) I_4 / I_5 R' \tag{8}$$

Upon substituting (8) into (2) and (4),

$$\omega_{3dB}\Big|_{LP} = (\ln \alpha) I_4 / (2m I_5 R' C_1) \tag{9}$$

and

$$\omega_{3dB}\Big|_{HP} = (\ln \alpha) I_4 / (2m I_5 R' C_2) \tag{10}$$

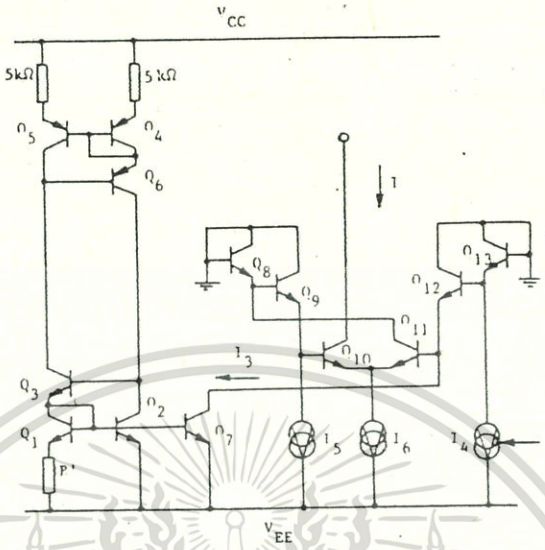

Figure 5. The biasing circuit for temperature compensation.

Now provided that the terms $I_5R'C_1$ or $I_5R'C_2$ possess low temperature coefficients, the 3 dB cut-off frequencies for both cases of the low-pass and high-pass circuits should also be relatively independent of the temperature.

In addition, instead of letting I_4 be a variable current source, we can alternatively let I_5 be the variable controlling current, so that the cut-off frequency is inversely related to the controlling current.

5. Tunable band-pass filter

The basic low-pass and high-pass circuits can be readily cascaded to form a very versatile electronically tunable band-pass filter, where the upper and lower cut-off frequencies can be independently varied electronically. Such a circuit could be useful in various electronic systems, for example, in adaptive filtering applications in high quality audio systems. As an example, we will consider the following possibility; in the absence of a high frequency audio signal, the upper cut-off frequency of the filter can be set low, so that high-frequency noise and scratch sound are reduced. Upon detecting the presence of a high-frequency signal, the upper cut-off frequency can be automatically increased so that the high frequency audio signal is unattenuated.

6. Discussion and conclusions

In this paper we have described and experimentally demonstrated circuit blocks for realizing electronically tunable low-pass and high-pass filters, where both linear and inverse relationships between the controlling signal and cut-off frequency can be obtained, which are suitable for integrated circuits.

One salient feature which should be pointed out is that the circuits operate in the current mode, having low input resistance and high output resistance. Therefore, they are eminently suitable as subsystems of a larger monolithic circuit. However, in stand-alone applications a single-ended voltage to current converter will usually be needed at the front end. Such a circuit can also be directly integrated into the same chip, but is left internally non-connected, so that either the voltage or current mode of operation is available.

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Synthesis of Current-Controlled Nonlinear Impedances

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C. WATANACHAIPRATEEP

Abstract—An integrable circuit technique is employed to obtain a class of current-controlled nonlinear impedances which is complementary to the recently proposed voltage-controlled class of nonlinear impedances.

Introduction

Recently, Pookaiyaudom *et al.* [1] proposed an integrable circuit principle for synthesizing voltage-controlled nonlinear impedances, where the words nonlinear impedances are used to denote certain circuit elements having the ratios of terminal voltages to currents dependent upon both the magnitudes and the frequencies of these quantities. Owing to the voltage-controlled nature of the circuit, the class of nonlinear impedances obtainable is restricted. There exists also a complementary class of current-controlled nonlinear impedances, where some of the elements cannot be realized by the voltage-controlled class of circuits. As an example, we will consider the synthesis of nonlinear resistances. The class of nonlinear resistances obtainable, using the voltage-controlled circuits, is restricted to cases where for each given terminal voltage, there corresponds only one terminal current. However, two or more distinct terminal voltages can correspond to a common terminal current. On the other hand, the complementary class of nonlinear current-controlled resistances is restricted to cases, where for each given terminal current, there corresponds only one terminal voltage, whereas two or more distinct terminal currents can correspond to a common terminal voltage.

It is the purpose of this letter to propose an integrable circuit to rotate a given nonlinear voltage-controlled impedance, as synthesized by the method of reference [1], to its complementary current-controlled version.

Circuit Description

Fig. 1(a) shows a modified circuit principle of reference [1], where for the sake of simplicity, only two differential pairs (Q_1, Q_2) and (Q_3, Q_4) will be employed as voltage to current converters to provide nonlinear characteristic. More complicated nonlinear characteristic can be realized by employing more differential pairs in parallel with the existing ones. The dynamic ranges of the differential currents passing through Z_1 and Z_2 are $\pm I_1$ and $\pm I_2$, respectively. The active load Q_5 to Q_7 injects current $i_3 = 2(i_1 - i_2)$ into the current mirror Q_8 to Q_{10}, which functions as a voltage level shifter. The output current of the current mirror will flow through R_2 in the direction as shown in Fig. 1(a), which will be denoted as $i_4 = -2(i_1 - i_2)$. Therefore, the ratio of the differential change in the output voltage across R_2 to the differential change in the input voltage is given by

$$(\delta v_2/\delta v_1) \simeq \begin{cases} -2R_2(Y_1 - Y_2), & v_1/|Z_1| \leqq I_1,\ v_1/|Z_2| \leqq I_2 \\ 2R_2Y_2, & v_1/|Z_1| > I_1,\ v_1/|Z_2| \leqq I_2 \\ -2R_2Y_1, & v_1/|Z_1| \leqq I_1,\ v_1/|Z_2| > I_2 \\ 0, & v_1/|Z_1| > I_1,\ v_1/|Z_2| > I_2 \end{cases} \quad (1)$$

The actual circuit performance will be accurately represented by (1) if high-performance differential voltage-to-current converters [2] are used instead of the simple differential pairs.

Fig. 1(b) shows the additional circuit, which will inject the input current i_i through R_1, while the output voltage across R_2 will be reflected to the input node by the differential pair Q'_2, Q'_3. The differential input resistance looking into the emitter of Q'_1 will be approximately equal to $r'_{e1} = V_T/I$, where I is the bias current of Q'_1, and V_T is the usual thermal voltage associated with a p-n junction. The voltage appears across R_1 will be equal to

$$v_1 = R_1 i_i \quad (2)$$

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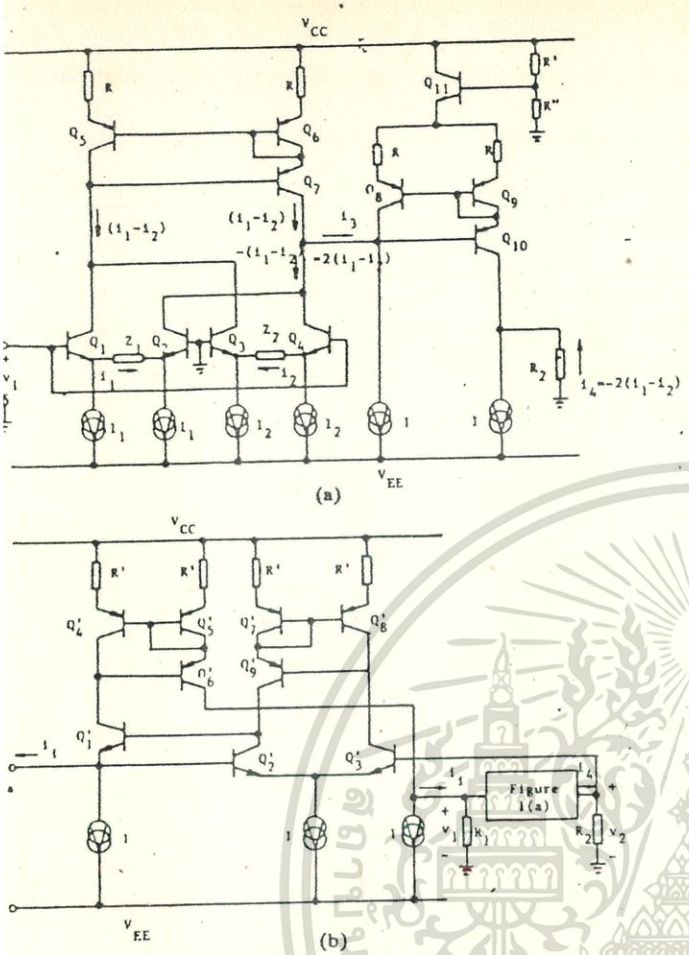

Fig. 1. (a) The circuit to generate nonlinear impedance characteristic. (b) The current-controlled nonlinear impedance generator.

where it has been assumed that the input current i_i is flowing out of the input node.

The voltage at the input node will be simply given by

$$v_i = v_2. \tag{3}$$

From equations (1), (2), and (3), it is seen that the differential input impedance at the input node will be approximately given by

$$Z_i = (\delta v_i/\delta i_i) = \begin{cases} -2R_1R_2(Y_1 - Y_2), & v_1/|Z_1| \leq I_1, v_1/|Z_2| \leq I_2 \\ 2R_1R_2Y_2, & v_1/|Z_1| > I_1, v_1/|Z_2| \leq I_2 \\ -2R_1R_2Y_1, & v_1/|Z_1| \leq I_1, v_1/|Z_2| > I_2 \\ 0, & v_1/|Z_1| > I_1, v_1/|Z_2| > I_2 \end{cases} \tag{4}$$

The circuit as shown in Fig. 1(b) will give a grounded current-controlled nonlinear impedance. The floating version can be readily realized with additional circuit to eject i_2 from the output node, while the voltage difference between the input and the output nodes is equal to the voltage drop across R_2. Very similar circuit has been employed in reference [3] to realize a current-controlled floating negative impedance converter. Since the extension from the circuit of reference [3] to the present circuit will be relatively straightforward, we will not discuss it further here.

The function of the circuit of Fig. 1(b), excluding the Fig. 1(a) portion, can be considered a special case of the "reflector" as proposed by Chua [3]. However, in using (4) or its more complicated versions using more than two differential pairs in Fig. 1(a), current-controlled nonlinear impedances can be realized in a more direct manner than using the concept of "reflector."

As with the case of voltage-controlled nonlinear impedance synthesis, care must be taken to prevent the circuit from self-instabilities. It has been pointed out in reference [4] that purely negative capacitance can be stably realized in current-controlled negative impedance converter. It has also been found in our present nonlinear impedance circuit that negative capacitance can be realized as part of the nonlinear impedance without self-instability problem. However, negative inductance cannot be stably realized as part of the nonlinear impedance.

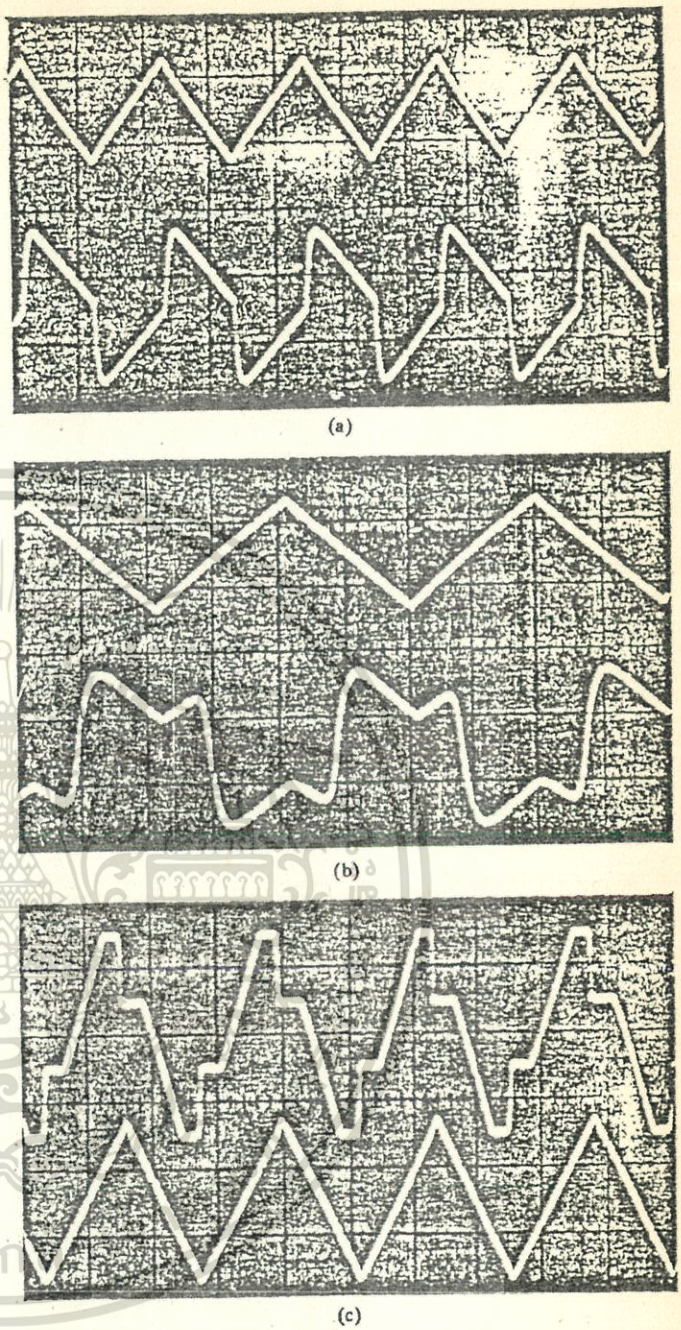

Fig. 2. (a) The synthesis impedance of series resistor and negative impedance, where the vertical scales are 0.5 V/div and 0.1 V/div for the upper and lower traces, respectively, and the horizontal scale is 0.05 ms/div. (b) The series negative inductance is saturated for part of the cycle. The vertical scale is the same as case (a), while the horizontal scale is 0.05 ms/div. (c) The series resistance is saturated for part of the cycle. The vertical scales for the upper and the lower traces are 2 V/div and 0.2 V/div, respectively, while the horizontal scale is 0.002 s/div.

Experimental Results and Discussions

The validity of the circuits of Fig. 1(a) and (b) have been experimentally verified by using transistor arrays to breadboard the circuit. Fig. 2 shows the oscillograms of a particular experiment, where the triangular traces represent the input voltage of a single ended voltage-to-current converter, having a conversion resistance of 20 kΩ. The converted current is then injected into the input node a. The lower traces show the voltage appearing across node a for different input current conditions. The impedances Z_1 and Z_2 of the differential pairs (Q_1, Q_2) and (Q_3, Q_4) of Fig. 1(a) are purely capacitive and purely resistive, respec-

tively, where the capacitance and resistance magnitudes are respectively equal to 0.027 μF and 11 kΩ. The current sources I_1 and I_2 are set at 50 μA and 100 μA, respectively, while all other current sources are set at 500 μA. The voltage conversion resistances R_1 and R_2 are both equal to 10 kΩ.

Fig. 2(a) shows the case when the impedance is equal to $2R_1R_2(1/R - SC)$, that is, a resistance in series with a negative inductance. Fig. 2(b) shows the case in which the negative inductance part is saturated when the input triangular current reaches the upper and lower peak regions, while Fig. 2(c) shows the case in which the resistance is saturated at the upper and lower peak regions of the input current.

In conclusion, it is seen that the present current-controlled nonlinear impedance synthesis method can be employed to generate highly complex nonlinear impedances which are complementary to the class of nonlinear impedances generated by the voltage-controlled circuit as given in reference [1].

References

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