OPTIMIZATION OF THIN-FILM FABRICATION PROCESSES FOR ORGANIC FIELD EFFECT TRANSISTOR

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A THESIS SUBMITTED IN FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF ENGINEERING IN ELECTRICAL ENGINEERING
FACULTY OF ENGINEERING
KING MONGKUT'S INSTITUTE OF TECHNOLOGY LADKRABANG
2013

KMITL-2013-EN-D-018-194

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บทคัดย่อ

วิทยานิพนธ์ฉบับนี้ นำเสนอกระบวนการพัฒนาชั้นฟิล์มบางในการสร้างทรานซิสเตอร์เทคโนโลยีสารอินทรีย์ เพื่อลดมูลค่าการสร้างต่อหน่วยที่สามารถสร้างบนฐานรองแบบยืดหยุ่น ในการยกระดับการใช้งานเมื่อสร้างเป็นอุปกรณ์อิเล็กทรอนิกส์ กระบวนการพัฒนาจะประกอบด้วย ลำดับแรกคือกระบวนการสร้างชั้นไดอิเล็กตริกด้วยพอลิเมอร์ ในระดับความหนา 95 นาโนเมตร การลดการเกิดรูพรุนและการแตกร้าวของชั้นฟิล์มที่ทำให้มีการรั่วไหลของกระแสผ่านชั้นฟิล์มต่ำ ด้วยการเลือกตัวทำละลายและฐานรองที่เหมาะสม ลำดับต่อมาคือกระบวนการสร้างชั้นสารกึ่งตัวนำ ด้วยกระบวนการพัฒนาอุปกรณ์และวิธีการให้สามารถควบคุมเงื่อนไขการปลูกฟิล์มบางเพนทาซีนเพื่อควบคุมคุณสมบัติทางกายภาพ จากการเรียงตัวของโมเลกุลจนถึงคุณลักษณะโครงสร้างของเกรนจนทำให้เกิดฟิล์มบางที่มีคุณลักษณะสนับสนุนต่อการเกิดประจุพาหะในสภาวะถูกกระตุ้นและมีการเคลื่อนตัวได้ดี ลำดับดับสุดท้ายคือการพัฒนากระบวนการสร้างหน้ากาก เพื่อใช้ขึ้นรูปทรานซิสเตอร์ด้วยเทคนิคการระเหิดด้วยความร้อนในการสร้างชั้นขั้วเกต ขั้วซอส-เดรน และสารกึ่งตัวนำนั้น ซึ่งกระบวนการสร้างหน้ากากนั้นสามารถพัฒนาได้ด้วยการลดความหนาของฟิล์มไวแสงที่ใช้สร้างพีซีบีบอร์ดเพื่อเพิ่มขีดความสามารถในการใช้งาน และพัฒนากระบวนการขึ้นรูปหน้ากาก

แบบสองขั้นตอน จนสามารถสร้างหน้ากากที่มีความละเอียดในระดับ 18 ไมโครเมตร จากการพัฒนากระบวนการสร้างฟิล์มบางทั้งหมดมีความสำคัญแต่จะจะพบว่า การสร้างชั้นไดอิเล็กตริกจากสารละลายโพลิเมทิลเมทาคริเลตในไดเมทิลฟอร์มาไมด์ทำให้สามารถลดความหนาในการใช้งานในระดับ 95 นาโนเมตร จะช่วยเพิ่มคุณสมบัติทางไฟฟ้าของทรานซิสเตอร์ได้ดีที่สุด โดยค่าความคล่องตัวของพาหะ 0.16 ซม^2/โวลต์.วินาที ค่าแรงดันขีดเริ่ม -3.6 โวลท์ อัตราการเปิดปิดกระแส 10^{-6} และค่าความชันในย่านแรงดันขีดเริ่ม 1.5 โวลท์/เดคเคด

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Program	Electrical Engineering
Year	2013
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Abstract

This thesis describes a study on the optimized processes uniformity of thin film layers for the fabrication of organic thin film transistor (OTFT) with a low-cost and large area application in electronic devices. For the dielectric layer, uniform, pinhole and crack-free films of Poly(methyl methacrylate) (PMMA) could be obtained by spin-coating, with a minimum thickness of about 95 nm. The effect of the insulator thickness on the performance of the devices has been investigated. Leakage currents, which are usually significant in many devices using polymeric gate dielectrics, were reduced by selecting a suitable solvent for each dielectric and the substrate materials. For the semiconductor layer, effects of the deposition conditions on molecular orientation, thin-film morphology and electrical characteristics of the active pentacene layer were throughly investigated. For patterning the OTFT structures by the thermal evaporation, the shadow masks were used for fabrication the gate electrode, the source-drain electrode and the semiconductor layer. In the shadow mask fabrication process a commercial photoresist film with an optimized thickness was used and optimized electroplating process to improve the resolution of the shadow mask up to 18 μm. Optimizing the fabrication process for all layers, is the key to improve the electrical performance of the OTFTs. However, the most significant improvement regarding the electrical performance of our fabricated OTFTs was achieved for the dielectric layer. The fabricated dielectric layer was prepared by solution of PMMA in dimethylformamide. The OTFT with the improved

dielectric layer showed a field-effect mobility of 0.16 $cm^2 V^{-1}s^{-1}$, a threshold voltage of -3.6 V, an on/off current ratio of 10^6 and a subthreshold slope of 1.5 V per decade.

Acknowledgment

I would like to give grateful acknowledgements to the following people and institutions that have enabled me to pursue and complete this work. This thesis would not have been possible without the funding provided by the Thailand Research Fund through the Royal Golden Jubilee, with its Ph.D. Program (grant No. PHD/0190/2547) for the scholarship throughout the thesis, the Deutscher Akademischer Austauschdienst (German Academic Exchange service) (DAAD) (grant No. D/08/04908) for the scholarship to conduct the experiments in Germany, the National Metal and Materials Technology Center (MTEC) for the support with the needed materials and the National Science and the Technology Development Agency (NSTDA), for the financial support provided during the research (Project MT-B-52-CER-07-240-I). I am profoundly indebted to my supervisors, Assoc. Prof. Dr. Apinunt Thanachayanont and Dr. Chanchana Thanachayanont, for all their time, advice, constant encouragement spend and the support provided, concerning not only my research, but also introducing me to the scientific community. I would like to show my gratitude to Prof. Michael Hietschold, Dr. Steffen Schulze and Dr. Somboon Sahasithiwat, for their kind advice and guidance during the experiments and sharing their knowledge of experimental techniques. I really thank them from my heart.

My gratitude goes to all my current and former colleagues in the Faculty of engineering at the King Mongkut's Institute of Technology Ladkrabang, Thailand, not to forget the ones at the National Metal and Materials Technology Center Thailand Science Park and the Institute of Physic, at the Chemnitz University of Technology, Germany. I would like to particularly thank Krokchi Inpore, Chabaiporn Junin, Narin Jantaping and Pennapa Muthitamongkol for their assistance and support during this thesis. In particular, special thanks to the best friend I have met in Germany, Piyapong Yountong, for his firm friendship and kind help with various tasks during my stay in Germany. It is my pleasure to thank those who made this thesis possible by allowing me access to their facilities and sharing their knowledge, in particular Assoc. Prof. Dr. Prayoon Songsiriritthigul and Dr. Hideki Nakajima at the Synchrotron Light Research Institute, Thailand and Dr.Sirapat Pratontep at the National Nano Technology Center, Thailand Science Park.

Most importantly, I am deeply indebted to my parents, in particular my mother, Suwanee Tippo for encouraging and inspiring me all the time. Finally, I want to especially thank my loving girlfriend, Nida Yampuang, for her understanding, patience and encouragement, without which I would not have succeeded this far.

Tossapol Tippo

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Chapter 1

Introduction

Organic electronic devices can, according to their current performance be used for existing or new applications which require large-area coverage, some structural flexibility, a low-temperature processing and a low-cost manufacture [1]. Among these devices, the organic thin-film transistor (OTFT) could evolve into an important element for the microelectronics technologies future. Two key advantages over devices deriving from inorganic semiconductors possessed by the OTFTs are its mechanical flexibility and the low-cost manufacture. These advantages contribute to OTFTs being promising candidates for chemical sensors, information displays and radio frequency identification tags. Different materials for organic semiconductors have been used as the active layer in the OTFTs. These include molecular crystals such as pentacenes which can be deposited by thermal evaporation in form of a thin film. Also playing a crucial role for the determination of the OTFTs performance is the gate dielectric layer [2]. The benefits provided by OTFTs can easily be lost when inappropriate insulators are used. The inorganic insulators silicon dioxide and silicon nitride, for example, both commonly used for gate dielectrics in the OTFTs, are formed at high temperature. Therefore the use of many organic substrates is precluded. On the other hand certain organic insulators, such as benzocyclobutene (BCB), need a very high curing temperature. This thesis is concerned with organic electronic devices based on pentacenes in combination with a polymer gate insulator. In this thesis, three strategies have been used to achieve low voltage organic electronic devices having a high performance and low-cost manufacture. In the first step, spin-coated polymer gate dielectrics were investigated regarding their ability to be used as electrical dielectrics under operation on devices. Here the solvents and substrates were optimized for PMMA gate dielectrics and the low voltage operating devices were studied. In the second step, the development of highly ordered thin films deriving from pentacenes, were studied. At present the research on pentacenes is concentrating on the semiconducting electrical properties. This is because charge mobility and injection in organic crystals depend strongly on molecular orientation and packing. Thus controlling the structure and the morphology of the organic thin films can lead to useful applications [3]. In the third step, the development process for

the shadow mask fabrication in order to pattern the structure on the OTFTs was optimized. This patterning process was carried out by thermal evaporation. This thesis is organized as follows:

Chapter 2 a general introduction to organic electronics is given. The historical background and various applications of organic electronics are briefly discussed and special attention is given to OTFTs. Charge transport mechanisms in organic semiconductors are reviewed and the various structures and electrical characteristics of OTFTs are discussed.

Chapter 3 begins with an overview of film formation techniques for OTFTs. The experimental details of this thesis and the techniques used in it, to characterize thin films and OTFTs are described. Details of the organic materials which are used in this thesis are also given.

Chapter 4 shows the results and focuses on, the formation of the thin film polymers on glass substrates, the use of PMMA with various solvents on glass substrate, as the supporting substrate for a PMMA gate dielectric, the fabrication and optimization of the pentacene thin film semiconductors and the fabrication of the shadow mask for pattern the OTFTs structure in the thermal evaporation process. The properties of PMMA films deposited by spin coating and their performance as PMMA gate dielectrics for low voltage operating devices are described, The device characteristics of a pentacene-based OTFT using PMMA as the gate dielectric are reported. In particular, the saturated field-effect mobility as a function of the thickness of the gate dielectric is explained in detail.

In Chapter 5 is focusing on the modeling of the fabricated OTFTs. Their performance is then tested in an inverter simulation to find out more about its possible use as an electronic circuit application.

Finally, Chapter 6 provides the conclusions deriving from the experiments and some suggestions for further research work.

Chapter 2

A Literature Review of Organic Electronics

2.1 Historical Background

In the late 1940s organic semiconductors were identified [4]. But it took another forty years until organic light-emitting diodes (OLEDs) [5],[6], organic photovoltaic cells (OPVCs) [7] and OTFTs [8] came in to view. In the beginning organic devices were based on either small molecules, 8-hydroxyquinoline aluminium (Alq3), for example, for the emitting layer in OLEDs [5], or conjugated polymers, such as poly (p-phenylenevinylene) (PPV) [6] and polythiophene (PT) for the active layer in the OTFTs [8].

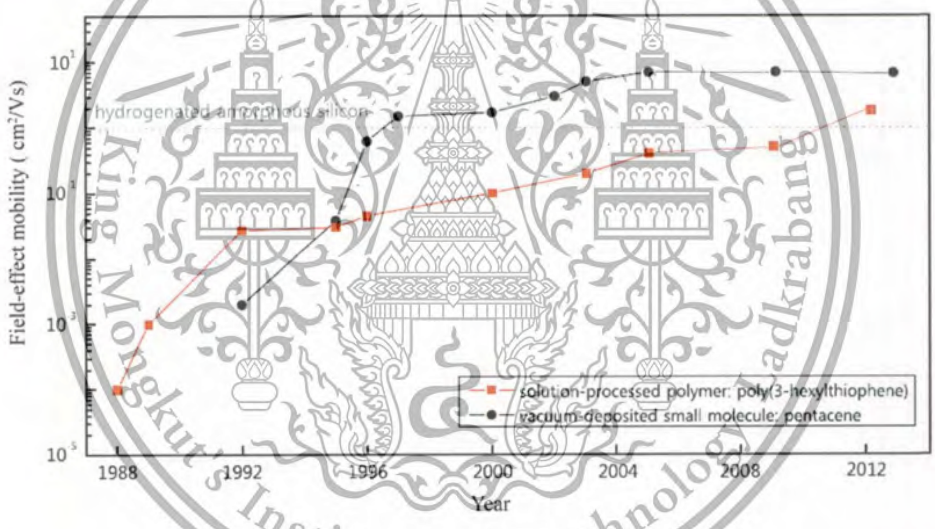

Figure 2.1 Improvement in organic semiconductor mobility since the 1980s [4], [9]-[12].

Over the last 20 years the performance of organic electronic devices was continuously improved, and OLEDs have now been introduced to the display market. Looking at OPVCs, power conversion efficiencies have reached over 5% [13]. These efficiencies are significantly lower than those of their inorganic counterparts (10~20%). But considering cheap production methods, such as roll-to-roll or printing processes, OPVCs will develop further in a dynamic way. OTFTs and their progress have been less intense but are now competing with amorphous silicon thin film

transistors (TFTs) which are used in active-matrix (AM) liquid crystal displays (LCDs), as shown in figure 2.1 [4],[9]-[12]. From now on, this review will focus on OTFTs.

2.2 Applications

For existing or novel TFT applications, requiring large-area coverage, structural flexibility, low temperature processing and low-cost manufacture, OTFTs, as shown by their processing characteristics and performance, could be used. As shown in the following sections AM flat panel displays (FPDs) based on liquid crystal pixels, organic light emitting diodes and electronic ink, low-end smart cards, electronic identification tags, sensors and perhaps all-flexible electronics are included in the applications of organic semiconductors.

2.2.1 Flat Panel Displays

OTFTs in backplanes for displays, is one of their important potential applications. According to the latest results in the "Quarterly Worldwide FPD Shipment and Forecast Report" from Austin, Texas-based Display Search [14], the worldwide growth of FPDs sales revenues has stagnated. But they are forecasted to increase from 82.6 billion US dollars in 2009 to 111.5 billion US dollars by 2016. Each year from 2008 to 2016, OLED television (TV) and e-Book sales revenues may rise up to 140% and 49%, respectively [14]. Still most backplanes of AM LCDs and AM OLED displays depend on TFTs having an active layer consisting of hydrogenated amorphous silicon (a-Si:H) or low temperature poly silicon (LTPS). However OTFTs have several advantages compared to structures fabricated from inorganic semiconductors: flexibility, large-area coverage and low-cost manufacture. That is why OTFTs are a promising candidate for flexible and inexpensive displays. For example, because of the relatively high processing temperature needed for a-Si:H deposition, it is not possible to produce AM LCDs based on a-Si:H TFTs on a transparent plastic substrate. But OTFTs can be processed at room temperature and thus are compatible with temperature-sensitive substrates. Also low-cost large-area manufacturing approaches, such as those based on inkjet-printing and roll-to-roll processing, for large-area AM LCD of TVs could be enabled by solution-processed OTFTs.

In the year 2000 Philips Research [15] reported the first AM display based on organic semiconductors. In 2001, Rogers et al. reported an electrophoretic flexible

display using a backplane based on OTFTs [16]. Following Rogers's report, many research groups have described OTFT backplanes in combination with electrophoretic display media and simple OLED pixels. Arias et al. have also shown the possibility of an OTFT backplane with fairly large size and high resolution for AM LCDs in 2010 [17].

2.2.2 Low-end smart cards and electronic identification tags

Organic semiconductors and the devices based on them are still in their infancy. It is obvious that certain parameters such as field-effect mobility, uniformity of threshold voltage and dark currents are far inferior to those of silicon field-effect transistors (FETs). But the performance of today's organic semiconductor technology is enough and adequate to develop low-cost circuits for applications such as card games, intelligent electronic tickets and product packaging.

A promising candidate for organic electronics has become an integrated radio frequency identification (RFID) tag, which normally operates at 13.56 MHz (high-frequency, HF). It is used for providing power to the tag via inductive coupling. It is used in smart cards, tickets, library book labels, passports, laundry tags and many other applications. The cost of, by solution processing produced organic RFID tags could be low enough to compete with that of barcodes, and in addition providing a lot of the advantages offered by the silicon-based RFID tags. Also being made of plastics, organic RFID tags, are thinner and more flexible than those based on silicon. In 2003 pentace based RFID circuits were demonstrated by Baude et al. [18]. Without a rectification stage, they were powered directly by RF and operated at 125 kHz. Subramanian et al. reported in 2004 of 135 kHz, all-printed organic RFID tags using novel pentacene and oligothiophene precursors for p-type semiconductors and ZnO nanoparticles for the n-type semiconductor [19]. Blache et al. described the first working 4 bit transponder in 2009. It was based on an organic complementary metal-oxide-semiconductor (CMOS) operating at a carrier frequency of 13.56 MHz [20]. Being fabricated on flexible polyester substrates, all the active layers of the device consisted of soluble organic molecules deposited by spin coating.

2.2.3 Sensors

Sensors used for food safety, environmental monitoring, medical diagnostics and home security have been intensively studied in recent years. Many advantages offered by organic semiconductors compared to their inorganic counterparts, make them particularly attractive for sensor applications. First, organic sensors can be

manufactured on flexible substrates at room temperature using low-cost processes, which is an important attribute for disposable sensors and other applications. Second, their properties are tunable via chemical synthesis. Included in this are not only electronic characteristics such as energy band gap and electron affinity but also the surface energy. The ability to covalently attach biologically relevant moieties to organic semiconductor molecules is of particular interest for sensors [21]. These hybrid materials can lead to the fabrication of sensors with high sensitivity and specificity. In 2002 Bartic et al. described ion-selective (IS) field effect transistors for pH monitoring using a proton sensitive OTFT as a transducer [22]. Someya et al. reported a large-area, flexible pressure sensor with OTFTs in 2004 [23]. These OTFTs were integrated with a graphite-containing rubber pressure sensor layer in order to form a very wide area structure, used to realize a flexible AM which was used to read out pressure images from the sensors. When it was wrapped around a cylindrical bar with a 2-mm radius the device was still electrically functional. OTFTs for biological and chemical sensors, capable of detecting parts per billion (ppb) concentrations analyst in water, were demonstrated with reliable operation by Roberts et al. in 2008 [24]. Based on a thin, cross-linked gate dielectric and a stable organic semiconductor, OTFTs could detect changes in pH and low concentrations of chemicals, such as trinitrobenzene, cysteine and glucose in water.

2.3 Organic thin-film transistors

The core technology in modern-day microelectronics is the metal-insulator-semiconductor (MIS) structure. The energy-band diagram for an ideal MIS device, based on a p-type semiconductor, is shown in figure 2.2 [25].

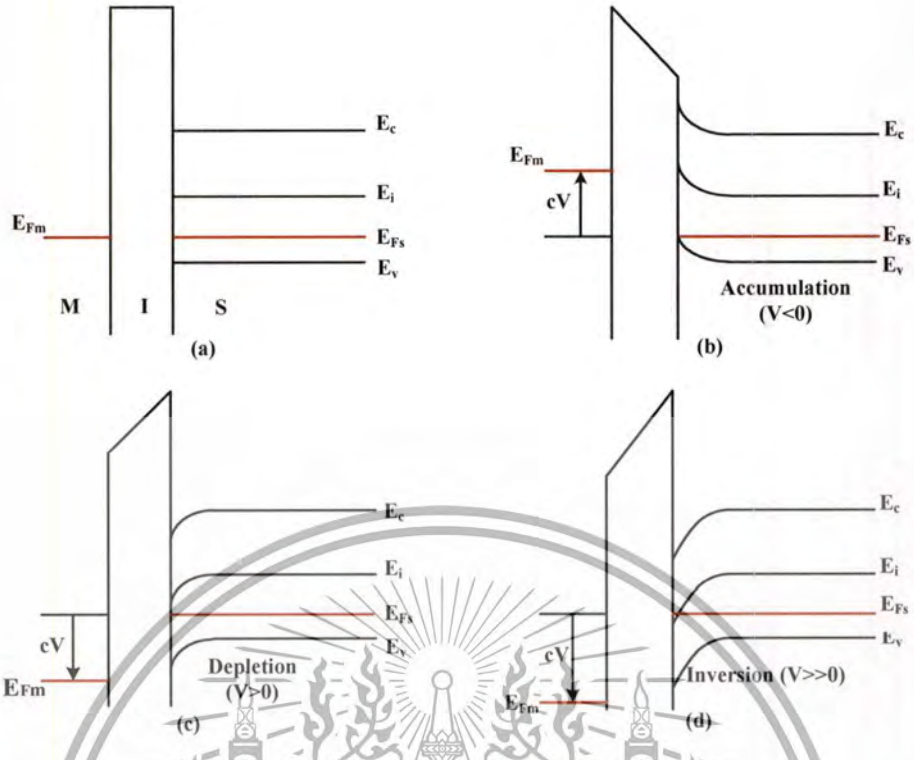

Figure 2.2 Energy band diagrams for an ideal p-type MIS device under (a) flat band, (b) accumulation, (c) depletion and (d) inversion conditions.

The Fermi levels of the metal and semiconductor align with no external bias. The various bands are flat throughout the MIS structure (Figure 2.2(a)). When a negative voltage is applied to the metal with respect to the semiconductor (Figure 2.2(b)), the bands bend upward and the valence band moves closer to the Fermi level, causing an accumulation of holes near the insulator-semiconductor's interface. A depletion of holes occurs when a positive voltage is applied to the metal (Figure 2.2(c)). If the positive voltage is increased further (Figure 2.2(d)), the bands bend down more strongly and the intrinsic level at the surface eventually becomes lower than the Fermi level.

Under this condition, the density of electrons exceeds that of 10 holes, and an inversion layer forms at the insulator-semiconductor's interface. In the case of a MISFET, the inversion layer provides a conducting channel between the source and drain electrodes. One of the main advantages of the MISFET is that the depletion region between the p-type substrate and both the n-type and the n regions below source and drain electrodes provide isolation from any other device fabricated on the same substrate. In addition, very low off currents can be achieved because both n+ regions

act as reverse-biased diodes. In 1962 the concept of a TFT was proposed by Weimer [26] and this led to the first a-Si:H TFT in 1979 by Le Comber [27]. The important difference between the TFT and the MISFET is that the channel is formed by the accumulation of charge carriers near the dielectric-semiconductor's interface. Inversion of charge carriers in the channel as with MISFETs does not occur. When a positive voltage is applied to the gate electrode of a p-type semiconductor, it operates in the depletion mode. The channel region is depleted of charge carriers resulting in a high channel resistance. This is called the off-state. That is why, low off currents are only guaranteed by the low conductivity of the semiconductor. For the duration, when a negative voltage is applied to the gate electrode, it operates in the accumulation mode. A large concentration of charge carriers is accumulated in the channel, resulting in low channel resistance, the so called on-state.

2.3.1 Charge transport in organic semiconductors

A narrow bandwidth and strong interactions between free charge carriers and the lattice is the result of the weak intermolecular interaction forces, normally van der Waals bonds. This creates a polaron formation, a self-localized charge. These polarons might be responsible for the low charge carrier mobilities in organic semiconductors. The bonding energies in inorganic single-crystalline semiconductors are strong, as a result of covalent or ionic bonding. So the charge carriers move in highly delocalized states in a wide bandwidth and have very high charge carrier mobility. In common single-crystalline inorganic semiconductors, charge transport, known as band transport, occurs in delocalized states. Its limitations are lattice vibrations, phonons which scatter the charge carriers. Such a mechanism is not applicable to disordered materials such as polymers. Charge transport might take place by hopping between the localized states. Phonons and the charge carrier mobility assist hopping, which increases with temperature is given by the equation:

$$\mu = \mu_0 e^{-\left(\frac{T_0}{T}\right)^{\frac{1}{\alpha}}} \tag{2.1}$$

Where μ_0 represent the trap-free mobility, α is the ratio of the effective density of states at the delocalized band edge to the concentration of traps in range from 1 to 4 [28]. However the temperature dependence of the charge carrier mobility is significantly affected by trapping, which is attributed to grain boundaries and other

structural defects in the polycrystalline films [29]. Hopping is appropriate to describe charge transport in disordered materials, while the multiple trapping and thermal release model (MTR) applies to well-ordered materials such as pentacenes and oligothiophenes. Charge carriers interact with the localized levels, which work as traps. The effective field-effect mobility, μ_{eff} will be given by

$$\mu_{eff} = \mu_0 \alpha e^{\left[\frac{(E_0 - E_t)}{k_B T}\right]} \tag{2.2}$$

E_o is the energy of the transport level and k_B the Boltzmann's constant. In the case of a single trap level, E_t is the energy difference between the trap level and the transport level. It is the ratio of the effective density of states (DOS) at transport level regarding the concentration of traps [28]. The gate voltage dependence of the field-effect mobility can be explained by an energy distributed DOS, which is an important outcome of the MTR model. In section 2.3.6 this will be discussed in more detail. Band-like transport in delocalized states becomes on the other hand the dominant charge transport mechanism in single crystals of organic semiconductors. Normally the boundary between band transport (delocalized process) and hopping (localized process) is defined by materials having charge carrier mobilities around 1 $cm^2\ V^{-1}s^{-1}$ at room temperature. But it is not possible to guarantee that the mean free path, l does not exceed the intermolecular distance, which is, except at very low temperatures, the necessary condition for the diffusive band-like transport. To distinguish between the charge transport in delocalized 1, 2 states and thermally activated hopping between localized states, which occur because of defects and impurities, by measuring the Hall effect on single crystals of rubrene has been made possible by Podzorov et al. [30]. Their results suggest a band-like transport in delocalized states as a possible charge transport mechanism in highly ordered organic semiconductors. Allowing independent measurements of the density of charge carriers is an advantage of the Hall experiment. Being temporarily trapped in shallow traps, the charge carriers do not make a contribution to the Hall voltage. Therefore, the mobility extracted from the Hall experiments should coincide with the intrinsic, trap-free mobility. Furthermore, band-like transport was not only reported in single crystals of rubrene but also in polycrystalline films of pentacene by measuring the thermopower. This was reported by Pernstich et al. and is defined by the Seebeck coefficient [31]. The Seebeck

coefficient S is given by the thermoelectric voltage V_{therm} when two ends of a sample are held at different temperatures (ΔT).

$$S = \frac{V_{therm}}{\Delta T} \tag{2.3}$$

The general expression for the electronic contribution to the Seebeck coefficient is

$$S = \frac{k_B}{e} \int \frac{E_F - E}{k_B T} \bullet \frac{\sigma(E)}{\sigma} dE \tag{2.4}$$

where $\sigma(E)$ is the electrical conductivity, it includes terms describing the DOS and energy-dependent scattering mechanisms, σ is the total conductivity and T is the temperature [31]. By rewriting equations (2.3) and (2.4) the thermoelectric voltage can be given for p-type semiconductors, as shown in the equation in terms of valence band edge E_v and a weighted average w as

$$V_{therm} = \frac{k_B}{e} \left(\frac{E_F - E_V}{k_B T} + w \right) \Delta T \tag{2.5}$$

where, with respect to the valence band edge, E_F–E_V is the Fermi level position. The rate at which E_F changes with the gate voltage is depending on the semiconductor's trap density. The quantity w accounts for carriers distributed beyond E_v. The 1, 3 values of w in single crystals of rubrene (2.1~3.6) have been found to be within the range of the electronic contribution in conventional single-crystalline inorganic semiconductors (2~4). In single crystals of organic and conventional single-crystalline inorganic semiconductors, this depends on the nature of the scattering mechanisms, which are depending on the room temperature, indicating the similarity of transport mechanisms. The values found in the polycrystalline films of pentacene transistors are slightly smaller (1.7~2.2) compared to those in amorphous inorganic semiconductors. There the n-values are in the range of -7 to -11 [31].

2.3.2 Organic semiconductors

For the active layer in OTFTs various organic semiconductor materials have been used, including molecular crystals such as pentacenes. They can be deposited in thin film form by thermal evaporation. Also included are conductive polymers, which can be easily processed by solution-based methods, such as inkjet-printing and spin-coating [32].

2.3.2.1 Small molecules

Pentacenes, oligothiophenes, named nT where n stands for the number of thiophene units, and phthalocyanines (Pcs) are the most representative p-type semiconductor materials based on small molecules. The normal process for producing thin films of these materials is by vacuum deposition. But some compounds can be processed by solution-based methods where a soluble precursor molecule is used. This may lead to certain advantages in device fabrication.

Not only pentacene a promising candidate for the active layer in OTFTs because high field-effect mobility, is as shown in figure 2.3(a), the molecule is a polycyclic aromatic hydrocarbon consisting of five aligned condensed benzene rings, called linear acenes or oligoacenes. Pentacene is one of the polyacenes, which were broadly studied as organic semiconductors during the 1960s and the 1970s. Oligothiophenes are small molecule p-type semiconductors for OTFTs are either substituted at both ends by a linear alkyl group, or non-substituted (Figure 2.3(b)). The outstanding performance of these small molecules is based on their ability to form well-ordered polycrystalline films in a herringbone pattern.

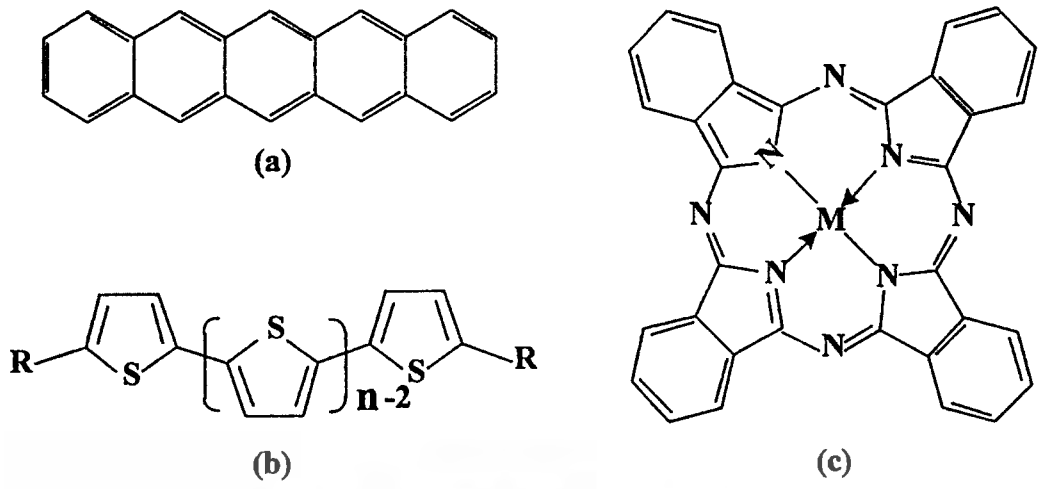

Figure 2.3 Chemical structure of (a) pentacene, (b) unsubstituted (R=H) and alkyl end-substituted (R=C*n*H2*n*+1) oligothiophenes and (c) metal phthalocyanine (Pc), where the central hydrogen atom is changed to the metal atom ($M=H_2$), it is named α-6T.

Another of the first reported families of small molecule p-type semiconductors are phthalocyanines. Their structure is a molecular cage, into which various metals can be introduced (figure 2.3 (c)). Many devices based on Pcs are fabricated by vacuum deposition, i.e. thermal evaporation. Also the solution-based Langmuir-Blodgett (LB) technique has been used. In addition Pcs could be substituted at their periphery with electrons drawing groups, such as hexadecafluoro-substituted copper Pc (R=F, M=Cu). These materials, can under ambient conditions, exhibit n-type field-effect mobilities, as high as 0.03 $cm^2 V^{-1} s^{-1}$ with excellent stability [32].

2.3.2.2 Polymers

In polymers, as indicated in figure 2.3, the carrier mobilities are still one order of magnitude lower than those in the smaller molecules. An explanation could be the fact that solution-processed materials, such as polymers provide poorer ordering than evaporated small molecules. This can be associated with the addition of soluble precursors (e.g. alkyl chains) or soluble groups.

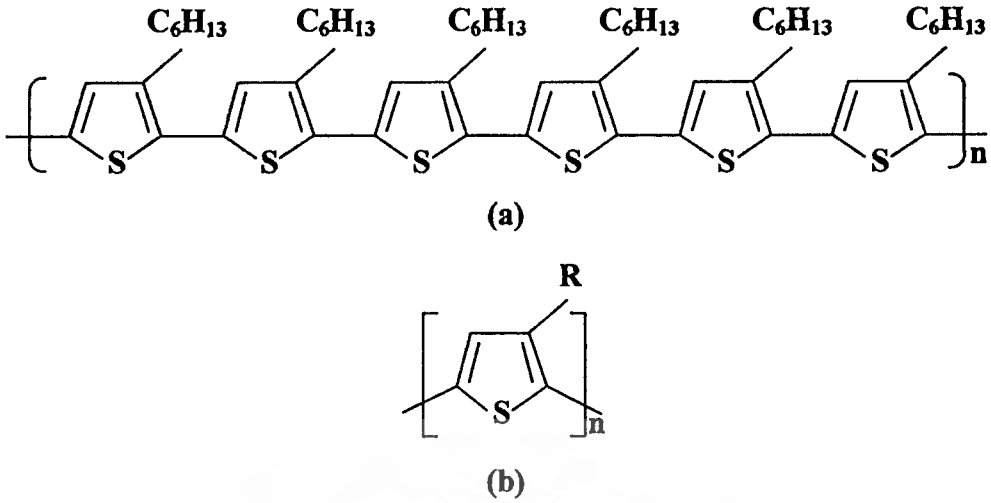

Figure 2.4 Chemical structure of (a) poly(3-hexylthiophene) (P3HT) and (b) poly(3-alkylthiophene) (P3AT) (R=C_4H_9, C_8H_{17}, $C_{10}H_{21}$ and $C_{12}H_{25}$).

The first solution-processed semiconductors used for OTFTs were Polythiophenes (PTs). To impact functionality, increase solubility and induce self-assembly now various derivatives have been incorporated on the polymer backbone. The alkyl derivatives can be incorporated with two types of arrangement into a PT-based polymer chain, either head-to-tail (HT) or head-to-head (HH). Regiorandom describes a polymer with a mixture of HH and HT linkages in PTs, while one with only HT linkages is called regioregular [32]. The most widely studied p-type semiconductor material among PT-based polymers, is Poly(3-hexylthiophene) (P3HT). Here the addition of alkyl side-chains enhances the solubility of the polymer chains (Figure 2.4(a)). Also Poly (3-alkylthiophene)s (P3ATs), thiophene-based polymers with side chains ranging from butyl to dodecyl, are important (Figure 2.4(b)).

2.3.2.3 n-type semiconductors

The fabrication of complementary logic circuits will be enabled by the development of n-type organic semiconductors, which have many advantages; such as high robustness, low noise and low power consumption. But most of the organic semiconductors studied until now are p-type. Some molecules like unsubstituted pentacene or oligothiophenes are more conducive to the injection of holes than electrons. On the contrary, in n-type semiconductors electrons are more easily injected than holes.

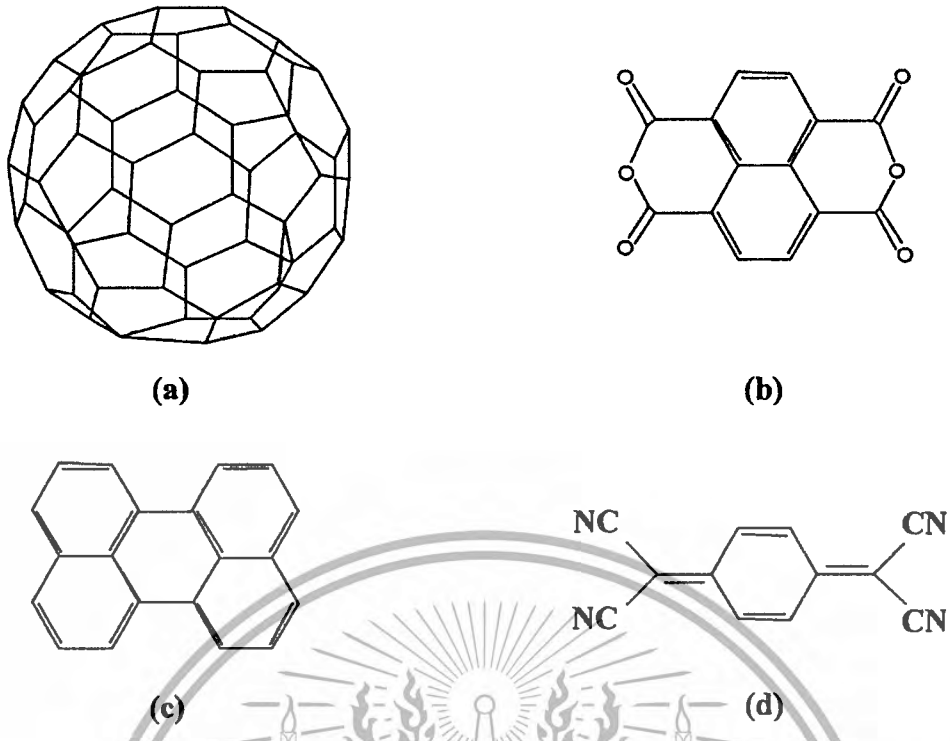

Figure 2.5 Chemical structure of (a) buckminsterfullerene (C60), (b) naphthalene-tetracarboxylic-dianhydride (NTCDA), (c) perylene and (d) tetracyanoquinodimethane.

As aforementioned substituted Pcs containing R=F or Cl, M=Cu, Zn, Co or Fe have exhibited n-type behavior. Also ambipolar mobility has been reported from water soluble copper Pcs substituted with sulfonic acid and methyl pyridinium groups. In 1993 Fullerenes (e.g. C_{60}) and their derivatives were reported as n-type organic semiconductors, which are molecules composed entirely of carbon in the form of a hollow sphere, ellipsoid or tube as shown in figure 2.5(a). Since then, mobilities as high as 0.56 $cm^2\ V^{-1}\ s^{-1}$ have been reported for C_{60} films, which were fabricated by molecular beam deposition without breaking the vacuum [33]. Their strong instability with respect to oxygen is a major problem of these materials, which acts as an electron trap within the C_{60} lattice. In figure 2.5 the chemical structure of Naphthalene-tetracarboxylic-dianhydride (NTCDA), perylene and tetacyanoquinodomethane (TCNQ) are shown. They have been studied as n-type organic semiconductors. Lately oligomers, such as perfluoroalkyl substituted oligothiophenes and trifluoromethylphenyl have been reported as novel n-type organic semiconductors.

2.3.3 Gate dielectrics

Charge carriers flowing at the interface between the active and gate dielectric layers determine the performance of OTFTs. Hence an essential element in improving

OTFTs will be the development of suitable insulating materials. The thickness and permittivity of the gate dielectric determine the operating voltage of the device. The charge induced on the semiconductor's surface as a function of applied voltage in a MIS structure is given by

$$Q = CV \tag{2.6}$$

where capacitance C is the ability of a body to store an electrical charge, voltage V is gives the electrical potential between the electrodes

Several classes of dielectric materials have been studied for OTFTs so far. The classification for the materials could be as following: inorganic (conventional or high dielectric constant), organic (polymeric), ultra-thin self-assembled monolayers (SAMs), multilayer and nanocomposite dielectric materials.

2.3.3.1 Inorganic dielectrics

Over the past decade a wide range of inorganic dielectric materials have been studied and introduced as the gate dielectric layer in OTFTs. Thermally grown silicon dioxide, as the gate dielectric layer on heavily, and doped silicon, as the gate electrode is the ideal system for the initial evaluation of almost all new organic semiconductors. Silicon dioxide is well known for its thermodynamic stability and its excellent insulating properties due to its large band gap (8.9 eV) [32]. But because thermally grown silicon dioxide is not compatible with flexible substrates, the advantages of organic electronics cannot be exploited fully with this material. Hence a large number of other inorganic dielectric materials have been investigated. For example, silicon dioxide (SiO_2), barium zirconate titanate (Ba(ZrTi)O) and barium strontium titanate (Ba(SrTi)O). They have been deposited by sputtering on transparent plastic substrates at low temperature. Another approach was done by using alternative higher dielectric constant materials such as titanium dioxide (TiO_2) and tantalum oxide (Ta_2O_5). These were obtained via electrochemical anodisation of sputtered tantalum. In table 2.2 are some representative inorganic dielectric materials listed.

Table 2.1 Overview of inorganic dielectric materials [4]

Material	Preparation method	Deposition temperature	Dielectric
Al_2O_3	Sputtered	Not given	~5.1
Al_2O_3	Anodised	Room temperature	~4.2
SiO_2	Thermally grown	> 600	3.9
SiO_2	Ion Beam sputtered	80	3.9
Ta_2O_5	Sputtered	300	25
TiO_2	Anodised	Room temperature	21
Ba(ZrTi)O	RF sputtered	Room temperature	17.3
Ba(SrTi)O	RF sputtered	Room temperature	16

2.3.3.2 Polymer dielectrics

In general polymers can be deposited by dip-coating, spin-coating or inkjet-printing and present a second major class of materials for the gate dielectric. By nature most of the organic polymers are insulators. Several polymers, as reported, show excellent insulating characteristics with very low leakage currents. Representative polymers are polystyrene (PS), poly (methyl methacrylate) (PMMA), poly (vinyl alcohol) (PVA), poly (vinyl phenol) (PVP), benzocyclobutene (BCB), parylene C and cyanoethylpullulan (CYEPL). These polymers are listed in table 2.2. Their chemical structures are shown in figure 2.6. The first common polymers such as PS and PMMA were to be used as gate dielectrics. Leading to PVA and PVP being the two of the most widely used polymer dielectric materials. After dissolving with the solvents, aqueous for PVA and ethanol for PVP, they can be deposited onto organic semiconductors. Water and ethanol are orthogonal to solvent used for semiconductors. In addition the robustness of these two materials can be enhanced by cross-linking, which is done by using chemical agents such as melamine-co-formaldehyde or hexamethylene tetraamine. Materials treated in such a way show low capacitances and the corresponding OTFTs operate at relatively high voltages. Besides, OTFTs with cross-linked siloxane ultra-thin polymeric films generated by spin coating have recently shown the encouraging results of high capacitance (300 nF cm^{-2}), and low leakage currents (10^{-8} A cm^{-2}) [34]-[37].

A robust siloxane network formed by chemical agents (e.g. 1,6- 22 bis (trichlorosilyl) hexane) improves the insulating quality significantly, allowing one to produce films as thin as 10 nm.

Table 2.2 Overview of organic dielectric materials [32].

Material	Preparation	Capacitance	Dielectric
Benzocyclobutene	Spin-coated	47	2.65
Poly (methyl	Spin-coated	19.5	3.5
Polystyrene	Spin-coated	19	2.6
Poly (vinyl phenol)	Spin-coated	17.8	10
Parylene C	Vapour deposited	2.2	3.1
Cyanoethylpullulan	Spin-coated	Not given	12

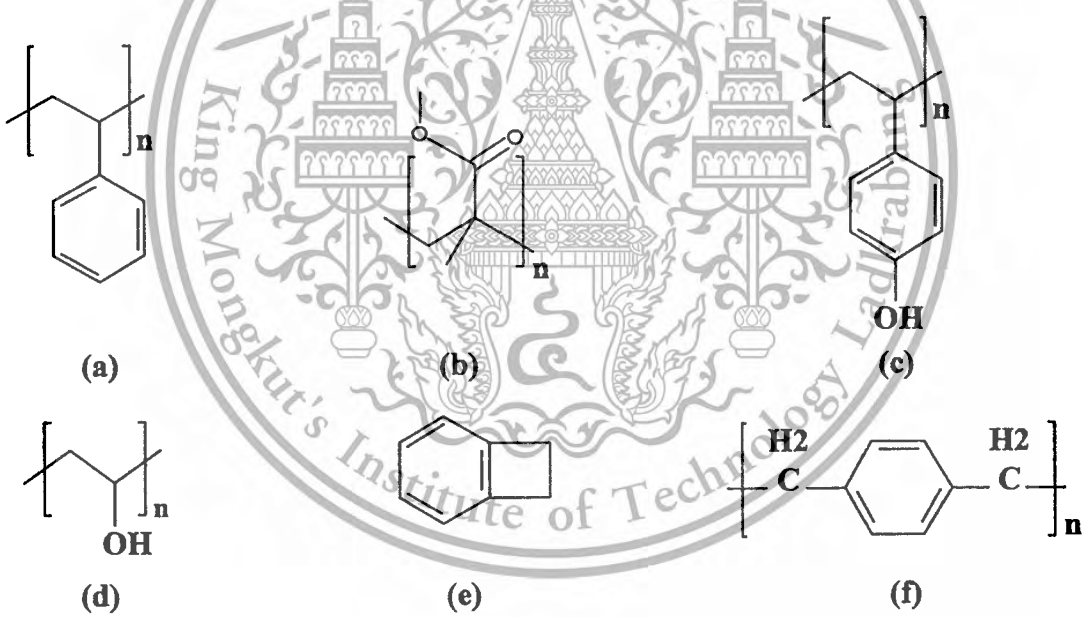

Figure 2.6 Chemical structure of (a) polystyrene (PS), (b) poly(methyl methacrylate) (PMMA), (c) poly(vinyl phenol) (PVP), (d) poly(vinyl alcohol) (PVA), (e) benzocyclobutene (BCB) and (f) parylene.

2.3.3.3 Self-assembled monolayer (SAM) dielectrics

Very promising are also ultra-thin SAM dielectrics for low-voltage OTFTs. This is because of the short chain length (in nm range) and the dense packaging of the SAMs. Under careful preparative conditions the SAMs that have been used as surface

treatments, can function as a dielectric. Generally known for generating molecular insulating layers are two approaches: bottom-up and top-down. Multiple chemical reactions are required for the former technique, where the final insulating layer is created by self-assembly from a precursor followed by one or more chemical modifications, but the result shows excellent electrical characteristics. Another new approach is the use of preliminarily modified molecules which can form dense SAMs such as alkyltrichlorosilane with an aromatic end-group, resulting in SAMs with a thickness of 2.5 nm providing a capacitance near 1 F cm^{-2}. The leakage current density is less than 10^{-9} A cm^{-2}. This is for electric fields up to 14 MV cm^{-1} [38]. But because of defects in the SAMs, arising from the imperfect surface of the target film, pathways for integration into large-volume coating processes are less obvious.

2.3.3.4 Multilayer and nanocomposite dielectrics

Multilayers are combinations of inorganic/ organic dielectrics with organic/ inorganic monolayers or thin polymer phases. Latter have been investigated to modify the surface of dielectric materials. Normally the additional layer helps to smooth the roughness of the dielectric surface. This improves the crystalline grain growth of the active materials. Some examples for additional SAMs are octadecyl-trichlorosilane (OTS) on silicon oxide dielectrics [39], alkyl phosphonic acid monolayers on alumina dielectrics [40] and octadecyl-trimethoxysilane (OTMS) on zirconium oxide dielectrics [41]. To improve the performance of OTFTs, polymers such as polystyrene [42] or poly (α-methylstyrene) [43] on oxide dielectrics have also been used. As reported, the use of an additional layer has a significant improvement on the device characteristics (e.g. field-effect mobility). However the thickness of the additional layer is much less than the thickness of the gate dielectric, the effect on the dielectric properties is less remarkable. Another method to generate nanocomposite dielectrics is to blend polymeric and ceramic materials on the nano-scale. For instance, the value of the dielectric constant can be increased from 3.5 for the traditional polymer dielectric (PVP) to 5.4 for the nanocomposite dielectric containing 7% nanoparticles (TiO_2-PVP) [44].

2.3.3.5 Methodology

The performance of OTFTs is determined by the interface between the semiconductor and the insulator. Great interest has been generated by the promises of pentacene as the semiconductor. However, recently, there have been extensive studies on different polymeric materials as the gate insulator. Among of these various

polymer gate insulators, devices using PVP possess high values of charge carrier mobility. On the other hand they exhibit a hysteresis behavior that results in a threshold voltage shift depending on the direction of the gate-source voltage sweep. A promising candidate for organic gate insulators is PMMA, which exhibits a minimal hysteresis and facilitates good ordering of the pentacene molecules as these are deposited on the surface[3]. Therefore, the purpose of this work is to create a more extensive study on pentacene-based organic electronic devices with a PMMA gate dielectric. This work aims to show low voltage OTFTs which use PMMA as the gate dielectric.

2.3.4 Contact resistance

The source and drain contacts are typically ohmic, which means that the value of the contact resistance is negligibly small compared to the channel resistance, under given bias conditions, Thus the contacts can inject and retrieve all of the charge carriers through the channel. The conventional Mott-Schottky (MS) model states that contacts are expected to be ohmic when the work function of the metal is close to the highest occupied molecular orbital (HOMO) or lowest unoccupied molecular orbital (LUMO) level of the p- and n-type semiconductors. Alternatively an energy barrier preventing charge injections can form at the metal-semiconductor's interface. But a lot of metal-organic semiconductor interfaces are not following the MS model. Figure 2.7 shows a proposed energy level diagram for the gold-pentacene interface, which exhibits an additional interface dipole barrier (Δ), which is determined by ultraviolet photoelectron spectroscopy [45]. The dipole barrier of the interface shifts up the gold vacuum level by more than 1 eV, but at this contact there is a 0.85 eV large barrier for the hole injection. There are several explanations for the origin of this interface dipole barrier. They include charge transfer between the semiconductor and the metal, reduction of the metal work function by adsorption of the semiconductor and population of metal-induced mid-gap states at the interface. Regardless of a large barrier at the metal-semiconductor's interface, it is possible to make ohmic contacts in OTFTs. This is probably because charge injection mechanisms at metal-semiconductor interfaces are not accounted to thermionic emission. There charge carriers must overcome the full potential barrier instead. Field emission (tunneling) through the barrier and/or defect-assisted transport, where charge carriers bypass the barrier by hopping becomes possible.

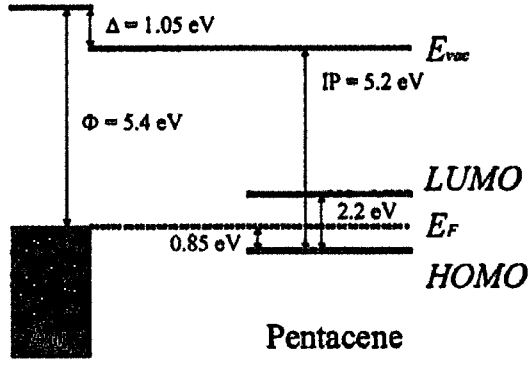

Figure 2.7 Band line-up diagram for the gold-pentacene interface [40].

The channel dimensions are critical parameter for the contact resistance. For a typical OTFT, the total resistance is given by

$$R_{total} = R_{channel} + R_{contact} = R_{channel}^{sheet}\frac{W}{L} + \frac{R_{contact}}{W} \tag{2.7}$$

where R_{sheet} is the channel sheet resistance, $R'_{contact}$ is the normalized contact resistance and L and W are the channel length and channel width of the device. The equation implies that the contact resistance could be a substantial part of the total resistance as the channel length decreases. In addition, the magnitude of the contact resistance must be considered compared to the channel resistance at high gate voltage in order to be ohmic. This is because the channel resistance decreases with increasing gate voltage.

2.3.5 Device structures of OTFTs

Various OTFT configurations are shown in figure 2.8. They result from the order in which the dielectric layer, semiconductor layer, gate electrode, source-drain (S-D) electrodes, are deposited on the substrate. To inject and retrieve charge carriers the S-D electrodes must be in direct contact with the semiconductor. The gate electrode has to be isolated from the semiconductor by the dielectric layer. Regarding the bottom-gate configuration, the gate electrodes followed by the dielectric layer are first deposited onto the substrate. This can be done in two ways. The first way is called the bottom-gate and top-contact (BG-TC) configuration, as shown in figure 2.8(a). Here the S-D electrodes are formed on top of the semiconductor layer. The bottom-gate and bottom-contact (BG-BC) configuration is shown in figure 2.8(b). Here the semiconductor is deposited on pre-deposited S-D electrodes. All of these

configurations have drawbacks and advantages. In the BC configuration, the S-D electrodes can be patterned by fine photolithographic methods. This is because the semiconductor is deposited on-top. But it has been reported, that the contact resistance is lower in the TC configuration than in the BC configuration, thus giving better device performance [4]. This is probably because of the increased metal-semiconductor contact area in the TC configuration. The top-gate and bottom-contact (TG-BC) is another configuration, as shown in figure 2.8(c). Because of the relatively "fragile" properties of the semiconductor layer, the deposition of the dielectric on the semiconductor layer is much harder than the other way around. But in this configuration, the dielectric layer serves as a passivating layer for the semiconductor and not only as the gate insulator.

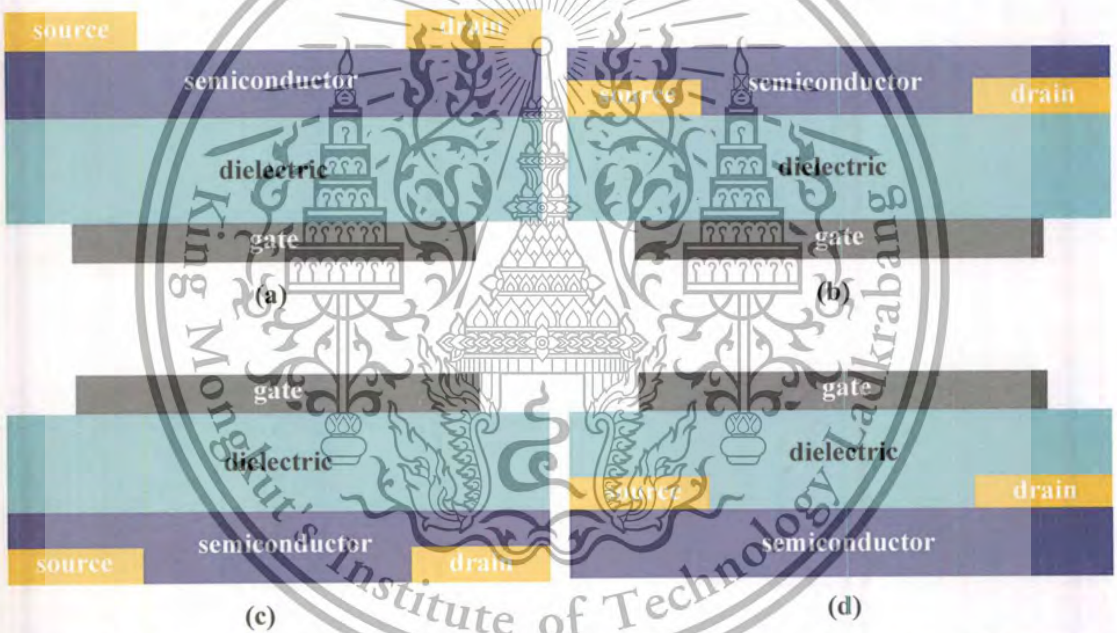

Figure 2.8 Schematic diagrams of OTFTs with (a) BG-TC configuration, (b) BG-BC configuration, (c) TG-BC configuration and (d) TG-TC configuration.

2.3.6 Electrical characteristics of OTFTs

The drain-source current is related to the drain-source voltage for low V_{DS} ($V_{DS} < V_{GS}$), by

$$I_{DSlin} = \frac{WC_i}{L}\mu\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS} \qquad (2.8)$$

where V_T is the threshold voltage, C_i is the insulator capacitance per unit area and μ is the field-effect mobility. The threshold voltage is represented by the value of the gate source voltage beyond which a conductive channel forms at the pentacene surface (i.e. the transistor is turned on). The device operation is defined by the linear region. As shown in figure 2.9 for high V_{DS}, the drain-source current saturates as the conductive channel becomes 'pinched-off'. The saturated drain-source current, $I_{DS(sat)}$, is given by

$$I_{DSsat} = \frac{WC_i}{2L}\mu(V_{GS} - V_T)^2 \tag{2.9}$$

Figure 2.9 Output characteristics for a typical OTFT, based on a p-type semiconductor. The dashed line indicates where the channel of the OTFT becomes pinched-off.

The OTFT's field-effect mobility is typically calculated either in the linear regime, where I_{DS} depends linearly on V_{DS} or in the saturation regime where I_{DS} is not dependent on V_{DS}. In this linear regime, the field-effect mobility, μ_{lin}, can be calculated through the transconductance, g_m, which follows from the derivative of equation (2.8).

$$g_m = \left[\frac{\delta I_{DSlin}}{\delta V_{GS}}\right]_{V_{DS}=\text{constant}} = \frac{WC_i}{L}\mu_{lin}V_{DS} \tag{2.10}$$

The saturation field-effect mobility, μ_{sat}, in the saturation regime can be given by rewriting equation (2.9) as

$$I_{DSsat}^{1/2} = \left(\frac{WC_i}{2L}\mu_{sat}\right)^{1/2}(V_{GS} - V_T) \tag{2.11}$$

$$\frac{\delta I_{DSsat}^{1/2}}{\delta V_{GS}} = \left(\frac{WC_i\mu_{sat}}{2L}\right)^{1/2} \tag{2.12}$$

As shown in figure 2.10(a) the value of μ_{sat} may therefore be evaluated from a plot of $I_{DSsat}^{1/2}$ compared to V_{GS}. The intercept of this plot can be used to determine the device threshold voltage. To determine the values of μ_{sat} and V_T, the straightest part of the plot is used and an average value is used for the hysteresis plot in this thesis. As shown in figure 2.10(b) the on/off current ratio and the subthreshold slope S is defined in equation (2.12) as the change in the gate-source voltage required for increasing the drain current by a factor of 10. S_{THD} is calculated by the inverse of the slope of I_{DSsat}–V_{GS} graphs.

$$S_{THD} = \frac{dV_{GS}}{d(\log I_{DSsat})} \tag{2.13}$$

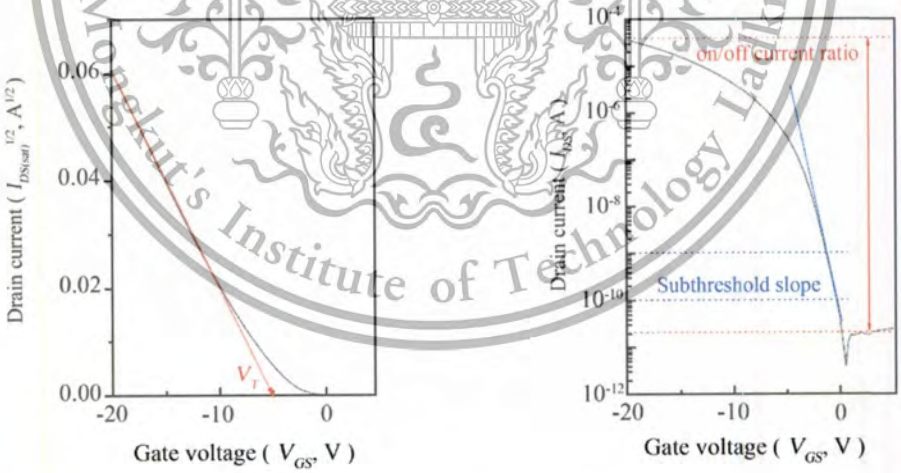

Figure 2.10 Typical OTFT transfer characteristics based on a p-type semiconductor in the form of (a) $I_{DSsat}^{1/2}$ compared to V_{GS} and (b) I_{DSsat} on a logarithmic scale compared to V_{GS}.

Equations (2.10) and (2.11) are still widely used to extract the field-effect mobility of OTFTs. However has been now clearly established that the field-effect mobility in using OTFTs, based on small molecules, is dependent on the gate bias voltage [46]-[50]. Following the model of Necliudov el. at. [46] for pentacene-based OTFTs operating above threshold region, most of the charge carriers induced by the gate-source voltage are trapped in numerous traps. Only a fraction of charge carriers participate in the current conduction. The effect of charge trapping is accounted for the gate-voltage dependent field-effect mobility [46] given by

$$\mu = \mu_0 \left(\frac{V_{GS} - V_T}{V_{AA}} \right)^{\gamma} \tag{2.14}$$

where γ and V_{AA} are empirical parameters that can be extracted from the transfer characteristics and μ_0 is a constant. As soon as V_{GS} increases, the Fermi level at the insulator-semiconductor interface moves toward the transport level and more traps are filled. Finally the energy separation between the filled traps and the transport level is reduced, so trapping becomes less efficient and the field-effect mobility increases [51]. This explanation is according to the model of polycrystalline sexithiophene (6 T) TFTs described by Horowitz and coworkers [47]. In this case, a MTR model is used to estimate the density of trap states and an empirical law of the form

$$\mu = \alpha (V_{GS} - V_T)^{\beta} \tag{2.15}$$

The variation of the mobility with gate voltage is practically linear, lowering the temperature leads to an increase of both the threshold voltage and exponent parameter β. However, it is assumed to represent the field-effect mobility. This leads to a gate voltage and temperature dependent field-effect mobility, which is given by

$$\mu = \mu_0 \frac{N_C}{N_{t0}} \left(\frac{C_i V_{GS}}{q N_{t0}} \right)^{(T_c - T)/T} \tag{2.16}$$

N_{t0} is the total surface density of traps, N_c is the effective density of states, C_i is the insulator capacitance per unit area, V_{GS} is the gate bias and T_c is the characteristic temperature of the exponential variation of the distribution [47]. However, the field-

effect mobility of single crystals of organic semiconductors is seldom dependent on the gate bias voltage. This fact supports the view that the gate bias dependence originates from the localized levels attributed to the grain boundaries and other structural defects. In addition V_{GS} modulates the contact resistance and it is observed that the contact resistance decreases with increasing V_{GS} [51].

That is why the abovementioned equations, although they are commonly used, should only be used for estimating an approximate value of the field-effect mobility in OTFTs. Usually the mobility values of pentacene OTFTs referred to in the literature are calculated in the saturation regime, the works this thesis uses the saturation field-effect mobility for comparison [9].

Chapter 3

Experimental Techniques

3.1 Device fabrication and characterization technique

3.1.1 Thermal evaporation

Solid materials begin to vaporize when heated to sufficient high temperatures. Thin film deposition occurs, when molecules are removed from a solid or liquid, depending on the depositing species, and travel over some distance in a vacuum chamber which is called transport from source to substrate. They impinge on the substrate, resulting in a film growth on the substrate. According to the Langmuir expression, the rate of evaporation Γ (in kg m^{-2} s^{-1}) from a surface is given by

$$\Gamma = P_M \left(\frac{M}{2\pi RT} \right)^{\frac{1}{2}} \tag{3.1}$$

where P_M is the vapour pressure (N m^{-2}) of material at d_m is the diameter of the molecules and k_B is the Boltzmann's constant, M is the molecular weight and R is the gas constant [52]. Even in a vacuum chamber, the molecules travel at high velocities making frequent collisions with residual gas molecules such as CO_2, H_2O, O_2 and N_2. According to the kinetic theory, the mean free path of gas atoms (λ) is given by

$$\lambda = \frac{k_B T}{P \pi d_m^2 \sqrt{2}} \tag{3.2}$$

where P is the chember pressure (N m^{-2}). Hence it is necessary to use low pressures, which result in straight line paths between the source and the substrate. The mean free path, in the pressure range of 10^{-5}~10^{-8} mbar, is compared to the source-to-substrate distance very is large (5×10^2 to 10^5 cm). Important parameters of thin film growth are the chemical and physical natures of the substrate's surface, the evaporation rate and the substrate's temperature. Residual gas molecules in the chamber also have an effect, because of their probability to be trapped in the film, or the occurrence of chemical reactions between themselves and the evaporated molecules.

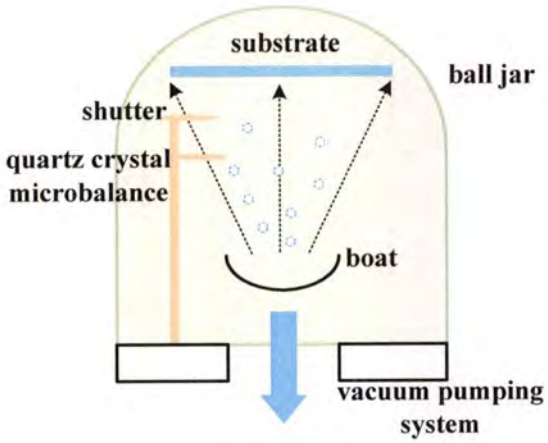

Figure 3.1 Thermal evaporation system for thin film deposition.

A schematic diagram of a thermal evaporation system is shown in figure 3.1. Typically, such a system consists of a bell jar, a vacuum pumping system, a "boat" where the source material is thermally heated up to the sublimation temperature by Joule effects or sometimes with an electron gun. A closed shutter is covering the sample, until the deposition rate is stable then the shutter is opened. While the evaporating substrate condenses on the film, a quartz crystal microbalance is generally used to measure its thickness by monitoring the change of its oscillating frequency.

3.1.2 Spin-coating

The so-called spin-coating technique is widely used in microfabrication for depositing general uniform thin films polymers, onto flat substrates such as glass slides or silicon wafers. Figure 3.2 shows the different stages involved in the process. The solution, in an excess amount, is first dispensed on the substrate which is then rotated at a fixed speed of several thousand rpm. The solution can also be applied while the substrate is slowly rotating. Due to the centrifugal force the solution spreads outwards and thus reduces the thickness of the fluid layer. The evaporation of the used solvent results in a film of uniform thickness [52]. The theoretical model for this process is given by

$$d = \left(\frac{\eta}{4\pi\rho\varpi^2}\right)^{\frac{1}{2}}\left(\frac{1}{t}\right)^{\frac{1}{2}} \tag{3.3}$$

where d is the thickness of the spun film, η is the viscosity coefficient of the solution, ρ is its density, ω is the angular velocity of the spinning and t is the spinning time [53].

According to equation (3.3), the film's thickness is independent of the quantity of the solution initially dispensed on the substrate.

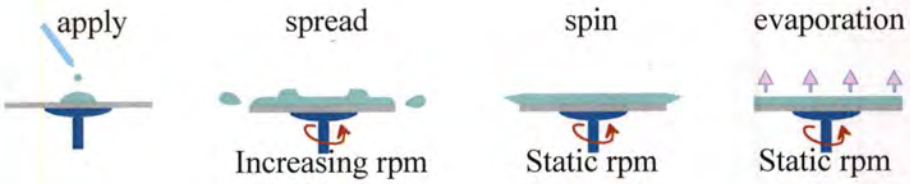

Figure 3.2 Schematic diagram of spin-coating.

3.1.3 Photolithography

Exposing a photoresist coat to a radiation of a certain wavelength will result in changes, such as the solubility of the developer in the exposed areas relative to the unexposed areas. If the resist prints in the negative resist (–ve) tone, the exposed areas are hardened. Whereas the positive resist (+ve) tone becomes more soluble in the developer solvent due to the light exposure. The changes in the exposed areas are deriving from the absorbed radiation and the chemical reactions initiated by them. The fabrication of a light mask involves the transformation of computer-aided designs of an IC into a physical layout to create a geometrical pattern of the mask.

The resolution (r) is the smallest feature that can be printed with adequate control. But there are two basic limits: the smallest image that can be projected onto the target and the dissolving capability of the photoresist in order to use that image. From the projection imaging side, the resolution is determined by the wavelength of the imaging light (λ) and the numerical aperture (NA) of the projection lens according to the Rayleigh criterion:

$$r \propto \frac{\lambda}{NA} \tag{3.4}$$

Lithography systems have changed during the time. They have progressed from the blue wavelength (436nm) to UV (365nm) to deep-UV (248nm) to the high resolution wavelength of 193nm. However, this research and the experiments conducted aim to study commercial film photoresists by decreasing its thickness and

thus improving their resolution by exposing them to a UV light at a wavelength of 365 nm.

3.1.4 Electroplating

Electroplating is a process in which electrical currents are used to reduce, positively charged, dissolved metal ions. Thus the cations are able to form a coherent metal coating on an electrode. This process is called electro-deposition. It is similar to a galvanic cell, but acting in reverse. In the electroplating process the cathode of the circuit is the part to be plated. Therefore the anode is made of the metal which has to be deposited on the cathode. As in a galvanic cell both components are immersed in an electrolyte solution, which contains one or more dissolved metal salts and ions which are necessary to ensure the flow of electricity. A direct current is supplied to the anode by a power supply. The direct current is oxidizing the metal atoms which comprise the anode, and allows them to dissolve in the solution. The dissolved metal ions in the electrolyte are reduced at the cathode. Thus they 'plate out' onto the cathode. The rate of dissolvement at the anode is equal to the rate of deposition at the cathode, and it is controlled by the current flowing through the circuit. As in a galvanic cell, the anode continuously replenishes the ions in the electrolyte bath [54]. For this thesis a nickel coating cell was used as shown in figure 3.3.

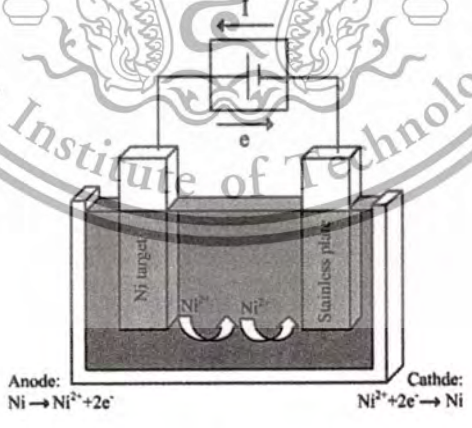

Figure 3.3 Illustration of typical setup for nickel electroplating

3.1.5 Profilometer

In order to measure and quantify the roughness of a surface's profile, a special measuring instrument, So-called profilometer is used. It is also used for measuring high resolution thickness in a step profile. In the beginning, a profilometer was a device similar to a phonograph which is measuring a surface while the surface is moved relative to the contact profilometer's stylus. This concept is changing with the development of numerous profilometery techniques measuring without having contact with the surface.

Contact profilometers were operating with a vertically moved stylus which had contact with the sample. The stylus moved laterally, keeping a specified distance and specified contact force across the sample. Small surface variations leading to a vertical stylus displacement as a function of position are measured by the profilometer. Very small vertical features in the range from 0.1 nanometers to 1 mm can be measured by a typical profilometer. The digital signal which can be stored, analyzed and displayed is converted from the analog signal which is generated by the height position of the diamond stylus. An important technical characteristic of a diamond stylus is its radius, which ranges from 10 nm to 50 µm. Other technical characteristics such as the scan speed and the data signal sampling rate are controlling the horizontal resolution. The stylus tracking force has a wide range from less than 1 up to 15 mg depending on the material of the surface[55].

3.1.6 Atomic force microscopy

In the nano-meter scale science and technology, atomic force microscopy (AFM) is used for high-resolution probe scanning. The two fundamental components of AFM are the probe and the scanner [56]. In an AFM the probe used is a sharp tip being located at the end of a cantilever. The different forces between the tip and the sample surface cause the cantilever to bend or deflect according to Hooke's law. The force, F, will be given by:

$$F = -fd \tag{3.4}$$

where d is the cantilever's displacement and f is the force constant. A laser diode sends a light beam to the cantilever where it is reflected to a position-sensitive photo-detector (PSPD), which measures the incident light. As a result, the cantilever

movements deriving from the scanning over the sample surface by the tip are measured by the PSPD. This generates a map of surface topography. A schematic diagram of a typical optical detection scheme for an AFM is shown in figure 3.4.

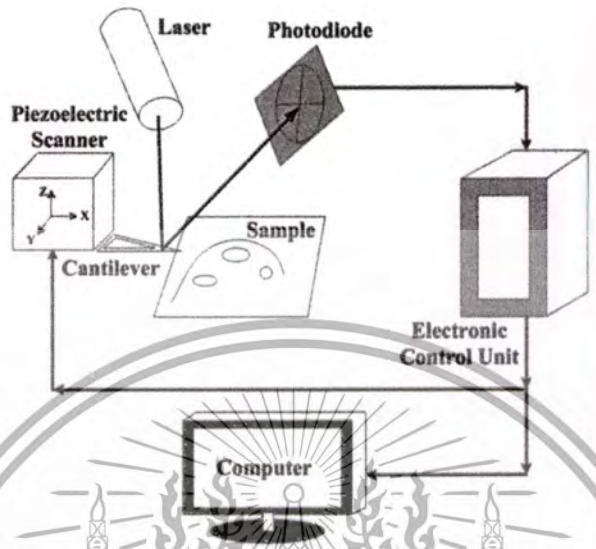

Figure 3.4 Typical optical detection scheme in atomic force microscopy.

There are three primary modes of use for an AFM: contact, tapping and non-contact mode [57]. In the contact mode AFM, the tip contacts the sample surface during scanning. A feedback loop maintains a constant deflection between the cantilever and the sample by vertically moving the scanner. The force between the tip and the sample remains constant. In the tapping mode AFM, the cantilever is oscillated at or slightly below its resonant frequency. This is realized by using an amplitude ranging typically from 20 nm to 100 nm. The tip slightly taps on the sample's surface during scanning only contacting the surface at the bottom of its swing. A feedback loop supplies constant oscillation amplitude ensuring a constant RMS of the oscillation signal and thus a constant tip-sample interaction is maintained during scanning. On the other hand, for the non-contact mode AFM, the cantilever is oscillated at a frequency which is slightly above the cantilevers own resonant frequency. Typically this is an amplitude of a few nanometers (< 10 nm). The tip does not contact the sample's surface, but oscillates above the sample's surface during scanning.

3.1.7 Scanning electron microscope

In order to generate a variety of signals at the surface of solid specimens the scanning electron microscope (SEM) uses a focused beam of high-energy electrons. These signals which derive from the electron-sample interactions reveal information about the sample including its external morphology (texture), chemical composition, crystalline structure and orientation of the materials making up the sample. In most applications, the collection of data is carried out over a selected area of the sample's surface. A 2-dimensional image which displays spatial variations in the aforementioned properties is then generated.

In an SEM accelerated electrons carry significant amounts of kinetic energy. The energy is dissipated when the incident electrons are decelerated in the solid sample and a variety of signals are produced by electron-sample interactions[58]. These signals include secondary electrons of which the SEM images are produced, and backscattered electrons (BSE). In addition diffracted backscattered electrons (EBSD) emerge, which are used for the determination of crystal structures and orientation of minerals. Commonly used for sample imaging are secondary and backscattered electrons: secondary electrons are most valuable for showing the morphology of and the topography on samples. Backscattered electrons are most valuable for illustrating contrasts in the composition of multiphase samples (i.e. for rapid phase discrimination).

3.1.8 Photoemission spectroscopy

The term Photoemission spectroscopy (PES, which is also known as photoelectron spectroscopy) is used to measure the energy of electrons being emitted by the photoelectric effect from gases, liquids or solids. This technique is used to determine the electron binding energies in a material. The term refers to different techniques, although they differ because of the source of the ionization energy. It can be provided by a X-ray photon, an EUV photon or an ultraviolet photon. Independent of the photon beam source, all photoelectron spectroscopy varieties are measuring the ejected electrons in order to perform a surface analysis.

Photoelectric ionization is induced by a beam of UV or XUV light which the sample is exposed to. The energies of the emitted photoelectrons are characteristic for their original electronic states, and depend also on vibrational state and rotational

level. Photoelectrons deriving from solid materials, can only escape from a depth in the order of nanometers, therefore only the surface layer is analyzed.

Due to the light's high frequency and the substantial charge and energy of the emitted electrons, Photoemission is one of the most accurate and sensitive techniques for measuring the energies and shapes of electronic states, as well as molecular and atomic orbitals. Photoemission is also used for detecting substances in trace concentrations assuming the sample can be distinguished from background and is compatible with the ultra-high vacuum.

In standard PES (UPS) instruments the UV light derives from helium gas sources, it has a photon energy up to 52 eV, which corresponds to a wavelength of 23.7 nm. The photoelectrons that actually into the vacuum escaping are collected, their energy is resolved, slightly delayed and counted. The outcome is a spectrum of electron intensity, which is a function of the measured kinetic energy. The source dependent kinetic energy values E_k are converted into source independent binding energy values E_b, which are more readily applied and understood. This is achieved by applying Einstein's relation.

$$E_k = h\nu - E_B \tag{3.5}$$

The term $h\nu$ of this equation is due to the energy (frequency) of the UV light that bombards the sample. The photoemission spectra are also measured using synchrotron radiation sources.

The measured electrons binding energies are characteristic for the sample's chemical structure and its molecular bonding. By adding a source monochromator, and increasing the energy resolution of the electron analyzer will result in peaks that appear with full width at half maximum (FWHM) of less than 5–8 meV.

3.1.9 Capacitance-frequency characteristics

An important aspect that determines the needed performance of integrated circuits is played by dielectric properties of the different materials used in the semiconductor's fabrication and packaging. Therefore a basic understanding of dielectric properties is needed by most engineers working in the semiconductor industry. One of the important properties of the dielectric material is its permittivity. Permittivity is a unit for the ability of a material to be polarized by an electric field.

It is easier to understand the concept of permittivity by first introducing the capacitance, a closely related property. The capacitance is for the ability of a material to hold a charge when a voltage is applied across it. It is best modeled by a dielectric layer which is sandwiched between two parallel conductive plates. As soon as a voltage is applied across a capacitor, the charge that can be held is directly proportional to the applied voltage. The capacitance as a constant proportion is explained before in equation (2.6).

The farad (coulomb per volt) is the unit of measurement for the capacitance. The capacitance of a capacitor depends on the dielectric layer and permittivity. Permittivity and capacitance are mathematically related as follows:

$$C = \frac{K\varepsilon_0 A}{d} \tag{3.6}$$

where A is the area, d is the distance between the electrode and the semiconductor, ε_0 and K are the permittivity in the free space and the dielectric constant of the dielectric, respectively. When the dielectric is measured in a vacuum, then the capacitance $C_0=\varepsilon_0(A/d)$, where ε_0 is the permittivity in the vacuum is 8.85×10^{-12} F/m. The dielectric constant of a material is the ratio of its permittivity compared to the permittivity in a vacuum is described as follows:

$$K = \frac{\varepsilon}{\varepsilon_0} \tag{3.7}$$

The dielectric constant of a material is also known as its relative permittivity. The dielectric constant is dimensionless because it is a ratio of two similar quantities. According to its definition, the dielectric constant of a vacuum is 1. All known materials are able to be polarized more than the vacuum, therefore the K of a material will always be bigger than 1 ($K > 1$). In addition in some materials the dielectric constant is also a function of the frequency. This occurs for example in polymers, primarily because polarization is affected by frequency.

A dielectric with a low permittivity or low ability to polarize and hold charges is called a low-K dielectric. Low-K dielectrics are excellent insulators for isolating signal-carrying conductors from each other. Thus, low-K dielectrics are a necessity in

very dense multi-layered IC's, wherein the coupling between very close metal lines needs to be suppressed in order to prevent a reduction in the device's performance.

A high-*K* dielectric, on the other hand, has a high permittivity. High-*K* dielectrics are good at holding charges. Therefore they are the preferred dielectrics chosen for capacitors. High-*K* dielectrics are also used in memory cells storing digital data in the form of a charge.

3.1.10 I-V Characteristics

The resistance of a material is determined by the Ohm's law, when a known current is sourced and flows through the unknown resistance.

$$R = \frac{V}{I} \tag{3.8}$$

We measure the voltage that develops across the resistance R by dividing the measured voltage V by the sourced current I. Normally 2-point electrical measurements are used for general purpose resistance measurements and I-V curve generation. But when the measured resistance is relatively low or the resistance of the probes or the contacts is relatively high more accurate results are yielded by a 4-point probe.

An insulator can be characterized by the parallel plate capacitors, the leakage measurement, which is carried out prior to the transfer or the *I-V* measurement where the dielectric quality and quantify leakage current should be the lowest through the dielectric layer.

OTFTs are characterized by two primary sets of measurement, the transfer (I_{DS}-V_{GS}) curves that allow a preliminary determination of the field-effect mobility μ and the threshold voltage V_T, and the transfer (I_{DS}-V_{DS}) curves that provide information about the saturation and the electrical performance in general.

3.2 Experimental details

3.2.1 OTFTs devices design

The bottom-gate, bottom-contact OTFTs are fabricated using the structure shown schematically in figure 3.5. We prefer and used bottom-gate, bottom-contact OTFT geometries, because with these geometries, connections between the gate

electrode layer and the S-D electrode layer only occur via holes through the gate insulator. In addition the delicate organic semiconductor can be applied as the last step in the transistor fabrication.

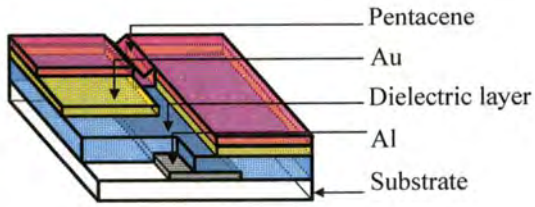

Figure 3.5 OTFT structure.

The device fabrication was carried out under ambient environmental conditions. An aluminium gate electrode was defined by thermal evaporation through a shadow mask. Spin-coating was used preparing the dielectric layer by a solution process. The gold S-D electrodes were defined by thermal evaporation through a shadow mask. As a last step pentacenes were thermally evaporated at a controlled temperature in the environment of the deposition system.

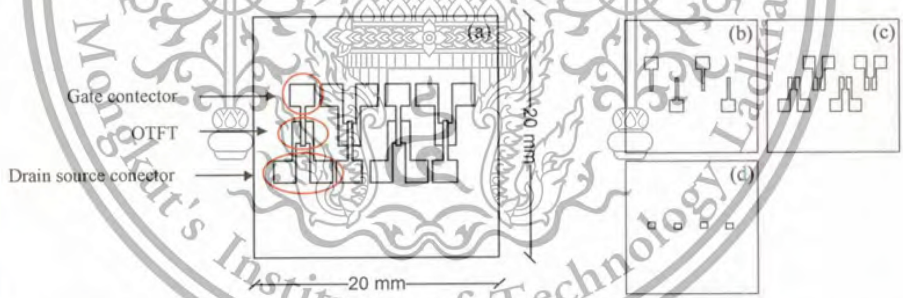

Figure 3.6 (a) Our four OTFTs, designed with a pattern of 20 mm×20 mm on the substrate. The three layers of the OTFTs were fabricated by thermal evaporation through three different shadow masks, (b) gate layer, (c) S-D layer and (d) semiconductor layer.

The four OTFT samples, fabricated by patterning of 20 mm × 20 mm on the substrate, are shown in figure 3.6. An OTFT has four layers. Thermal evaporation through shadow masks is used for the fabrication of the gate electrode, the source-drain electrodes, and the semiconductor layer. Spin-coating is used for the fabrication of the dielectric layer. The OTFT can be fabricated with a channel width in a range of 100-5000 μm and with a minimum channel length of 18 μm. The OTFT structures were

designed by using the computer program IC design (Ledit program version 8.03). The final layouts were generated to pdf files and delivered to an industrial shop for the photographic printing of the light mask.

3.2.2 Fabrication of the shadow mask

The shadow masks and the patterns on the shadow mask were fabricated by electroplating and photolithography techniques. The electroplating process uses a conducting electrolyte cell to coat a metal (donor) on the metal surface of the substrate (acceptor). The pattern on the coated metal can be generated by assuring a non-conducting area on the metal surface, for this experiment a commercial photoresist film was used.

3.2.2.1 Stainless steel substrate preparation

Stainless steel was used as an acceptor in the electroplating cell. A layer with 1 mm thickness and a low surface roughness of the substrate was patterned with 6 cm x 7 cm size, and then cleaned with acetone by a polishing wiper to remove organic residuals. Then it was cleaned again with a detergent, and finally dried with nitrogen to remove remaining substrates of the surface.

3.2.2.2 Preparation of the photoresist film on the substrate and thinning process of the photoresist film

The photoresist film was applied on a cleaned stainless steel substrate, and then inserted to roller pressing and heating to increase adhesion and ensure the application without any scratches or bubbles. On the substrate the photoresist film was soaked in a bath of Na_2CO_3 solution with a concentration of 2.5 mg/ml. Then the surface of the photoresist film was wiped at 5 sec intervals with a screen printing brush (figure 3.7) to decrease the thickness of the photoresist film.

Figure 3.8 Screen printing brush was used for thinning the photoresist film

3.2.2.3 Photolithography exposing process

In this process, the light mask was put on top of the photoresist film. Then the photoresist film is exposed through the light mask (see figure 3.9) by UV light (365 nm) with controlled exposing times. After that, the exposed photoresist film was developed by using Na_2CO_3 at a concentration of 2.5 mg/ml to generate the patterned photoresist film. The quality of the patterned photoresist film was observed with an optical microscope.

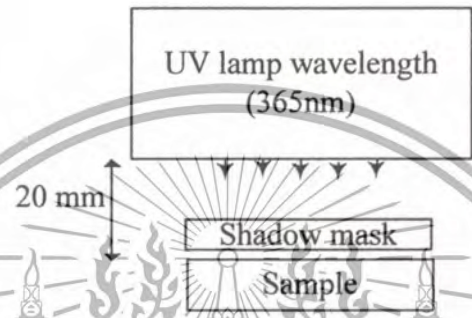

Figure 3.10 Exposing process

3.2.2.4 Electroplating process

The photoresist films patterned on the stainless steel substrate were further treated in the electroplating process in order to apply nickel to the conducting area of the fabricated shadow mask. A 1.5 liter industrial nickel coating electrolyte was introduced in to a glass tank with a length of 20 cm, a width of 15 cm and a height of 10 cm. The electrolyte was stirred with a magnetic stirrer at 200 rpm at a temperature of 70°C. Before the application, the nickel bar was cleaned with a detergent and dried with nitrogen. The nickel bar was then introduced into the glass tank (see figure 3.3) and connected to the DC power supply using the anode. The photoresist film pattern on the stainless steel substrate was also introduced into the glass tank and connected to the DC power supply using the cathode. The thickness of the metallic coating is controlled by the process's running times with a constant current of 0.5 A.

3.1.2.5 Two-step fabrication of the shadow mask

In the first step, the photoresist film coated on the stainless steel substrate was decreased to a thickness of 10 μm by the thinning process. The pattern on the photoresist film on the stainless steel plate was generated by exposing it to UV light through the light mask. Then the photoresist film, which was not exposed to the UV light was removed with a developer in the photolithography process. The patterned

photoresist film on the stainless steel substrate was then coated with nickel in the electroplating cell for 15 min, in order to fabricate the about 10 μm thick shadow mask.

In the second step, the shadow mask from the first step was coated again with the photoresist film and it was exposed to UV light in order to cover the working area of the shadow mask. To generate the frame of the shadow mask, after removing the unexposed photoresist film with a developer, then coated with nickel electroplating cell for 25 minutes was used to fabricate the frame of the shadow mask (see figure 3.9) with a thickness of 30 μm, which is needed to give it more stability.

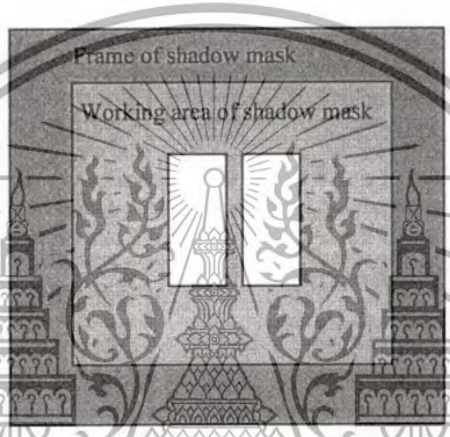

Figure 3.11 The shadow mask is fabricated in two-steps

3.2.3 Fabrication of the gate dielectric by spin-coating technique

There are several parameters affecting the thickness of a spun film. It depends on the concentration of the used solution and its viscosity coefficient. Also the angular velocity of the spinning, and the spinning time have to be considered. While producing, the solution was dropped on the substrate before starting the spinning process and then spin-coated by using a Laurell Technologies WS-400A-6NPP-LITE spin-coater. To spread the solution evenly a variable spin speed (500 - 5000 rpm) was used and after 3 minutes the speed was reduced in order to ensure the desired thickness on the substrate.

3.2.3.1 Preparation of film dielectric layer using different materials

Polystyrenes have an average molecular weight of ~400,000 measured by GPC, PMMAs have an average molecular weight of ~996,000 measured by GPC, poly-4-(vinylphenol) (PVP) poly (melamine-coformadehyde) methylated M_n ~423, 84 wt.% in 1-butanol, have a molecular weight of ~25,000. Propylene glycol monomethyl

ether acetate (PGMA) with a grade of ≥99.5% was used as reagent. Also a high grade Xylene was used as reagent. Both were purchased from Sigma-Aldrich. The analytical reagent (A.R.) n-butyl acetate (nBA) was purchased from LAB-scan Analytical sciences. The PMMA solution with nBa and the PS solution with xylene were prepared with concentrations of 1, 2, 3, 4, 5 and 6 wt.%.

For the PVP solutions, PVP was first mixed with the PGMA solvent in concentrations of 2-14 wt.%. In a second step the poly (melamine-coformadehyde) methylated solution was mixed with the PGMA solvent at a concentration of 4 wt.%. Then both solutions were mixed again in a ratio of 1:1 V/V.

3.2.3.2 Preparation of the PMMA dielectric layer using different solvents

PMMA having an average molecular weight of ~996,000 measured by GPC was purchased from Sigma-Aldrich. The Analytical reagent (A.R.) was n-butyl acetate (nBA) with a high grade, purchased from LAB-scan Analytical sciences. Dimethylformamide (DMF) and toluene were used as Analytical reagents (A.R.), both were used at lab grade and purchased from LAB-scan Analytical sciences.

DMF, nBa, and Toluene solvents were used with the PMMA solutions. The solutions of PMMA were prepared in concentrations of 1, 2, 3, 4, 5 and 6 wt.%. The samples were spun in a nitrogen glove-box for 180 s at spin speeds varying from 500 to 4000 rpm. The Films were allowed to dry for 1 hour in an argon environment at 60°C. Then the temperature was increased to 120°C for another hour, in order to remove residual solvents and to anneal the polymer films.

3.2.3.3 Preparation of PMMA dielectric layer on different substrates

PMMA (Average molecular weight of ~996,000 measured by GPC from Sigma-Alrich) was dissolved in DMF used as the Analytical reagent (A.R.) at various concentrations of 1-3 wt.%. The PMMA solution was spin coated on glass, PEN and Si wafer substrates at 2000 rpm. Then the substrates were allowed to dry at 60°C for 1 hour in an argon atmosphere in order to remove residual solvents. This process was followed by annealing at 120 °C for 1 hour in the same atmosphere in order to harden the polymer films.

3.2.4 Metal and Semiconductor fabrication by thermal evaporation

3.2.4.1 Fabrication of the Metal electrode layer

Thermal evaporation was used to deposit Gold and Aluminum at room temperature through a shadow mask. An Edwards Auto 306 evaporator with a diffusion pump was working for 1 hour at a pressure of less than 5×10^{-6} mbar. The deposition rate and film thickness were monitored by a quartz crystal microbalance. The electrode was defined with a thickness 30-50 nm through a shadow mask. The rate of evaporation was around 0.5~1.0 nm s^{-1}.

3.2.4.2 Pentacene semiconductor layer

1) First generation with commercial coater

Thermal evaporation was used to deposit pentacenes at room temperature through a shadow mask using an Edwards Auto 306 evaporator with diffusion pump at a pressure of less than 5×10^{-6} mbar with pump times of 1 hour. The film thickness and deposition rate were monitored by a quartz crystal microbalance. Pentacenes were deposited from a ceramic, resistively-heated crucible at a temperature of around 150°C. The pentacenes were defined with a thickness of 30-50 nm through a shadow mask and evaporated at a rate of around 0.5~1.0 nm s^{-1}.

2) Second generation with modified coater

Pentacenes were deposited by thermal evaporation through a shadow mask at room temperature using an in house modified thermal evaporator with a turbo pump at a pressure of less than 5×10^{-6} mbar and application times of 1 hour. The film thickness and deposition rate were monitored by a quartz crystal microbalance. Pentacenes were deposited from a ceramic, resistively-heated crucible at a temperature of around 150°C. The pentacenes were defined with a thickness of 30-50 nm through the shadow mask and evaporated at a rate of around 0.001~1.0 nm s^{-1}.

3) Third generation with modified coater for organic material

Figure 3.10 shows how pentacenes were deposited by thermal evaporation at room temperature through a shadow mask using an in house modified thermal evaporator with a diffusion pump at a pressure of less than 5×10^{-6} mbar and with pumping times of 5 hours. The film thickness and the deposition rate were monitored by a quartz crystal microbalance. Substrate and environments can be controlled by the electrical power applied through a Tungsten wire. Pentacenes were deposited from a ceramic, resistively-heated crucible at a temperature of around 150 °C. The

pentacenes were defined with a thickness of 30-50 nm through a shadow mask and evaporated at a rate of around 0.001~1.0 nm s^{-1}.

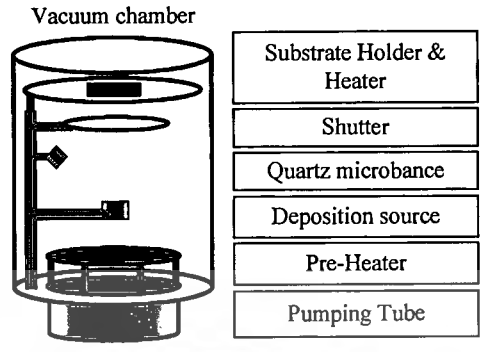

Figure 3.12 Organic thermal evaporation system

4) Fourth generation with commercial organic coater

Pentacenes were deposited by thermal evaporation at room temperature through a shadow mask using a outsource modified thermal evaporator with a turbo pump at a pressure of less than 5×10^{-6} mbar with pumping times of 1 hour. The film thickness and the deposition rate were monitored by a quartz crystal microbalance (under the shutter). Pentacene was deposited from a ceramic, resistively-heated crucible with a capacity of 2ml, at a temperature of around 150 °C. The pentacenes were defined with a thickness of 30-50 nm through a shadow mask and evaporated at a rate of around 0.001~1.0 nm s^{-1}.

3.3 Device characterization

3.3.1 Physical characterization

3.3.1.1 PMMA thin-film thickness

The thickness of the PMMA layer was measured by a profilometer. Scanning parameters used: a scan length of 2 mm, a 12.5 μm tip radius, with a 30 mg stylus force and a vertical range of 65 kA.

3.3.1.2 PMMA thin-film surface morphology

Surface morphology was scanned in the dynamic force mode, also referred to as tapping mode to study the various layers. A SPA400 atomic force microscope made by Seiko Instruments was used. Etched silicon tips were used with a resonant frequency of 140 kHz and a constant force of 3.5 N/m. The Roughness measurements

were calculated using the SPIWin version 4.08F. The area scanned had a size of 3 μm × 3 μm.

3.3.2 Electrical characterization

3.3.2.1 Capacitance-frequency characteristics

The dielectric constant in relation to the frequency and the loss factor were measured by using an impedance analyzer (Agilent 4294a) with a fixed 10-mV AC voltage.

3.3.2.2 Current-voltage characteristics

In order to measure the leakage current against the electric field for the 100 nm-thick PMMA layers of the MIM, a parallel plate capacitor structure was measured using a high-accuracy current-voltage measurement device (Keithley 2612). During the measurement process a DC voltage, sweeping from 0 V to 40 V, is applied across the electrodes and the corresponding currents are measured. The data were analyzed according to ASTM D3755.

The electrical characteristics of the fabricated OTFTs were measured using the Keithley 2612. The mobility, the on/off current ratio, and the threshold voltage of the OTFTs were calculated from the experimental electrical data.

3.4 Materials

3.4.1 Pentacene

Pentacenes ($C_{22}H_{14}$) are among the most widely studied organic semiconductors, with investigations beginning in the 1970s. A Pentacene is a planar molecule composed of five benzene rings which are linearly fused. The molecules are arranged in a herringbone pattern because of the large asymmetry in the molecule structure it forms the bulk triclinic crystal. In evaporated films, pentacene deposits with its long axis roughly perpendicular to the substrate, resulting in strong two-dimensional interactions which are parallel to the substrate [59]. The parameters of the crystal structure of pentacenes are listed in table 3.1.

Table 3.1 Crystallographic data for pentacene [60],[61]

Parameter	Unit	Value
Crystal system	-	Triclinic
a	Å	7.90
b	Å	6.06
c	Å	16.01
α		101.90
β		112.60
γ		85.80
U (volume of unit cell)	$Å^3$	692
D (density)	$g\ cm^{-3}$	1.32
Space group	-	P1
Molecular weight	-	278.30

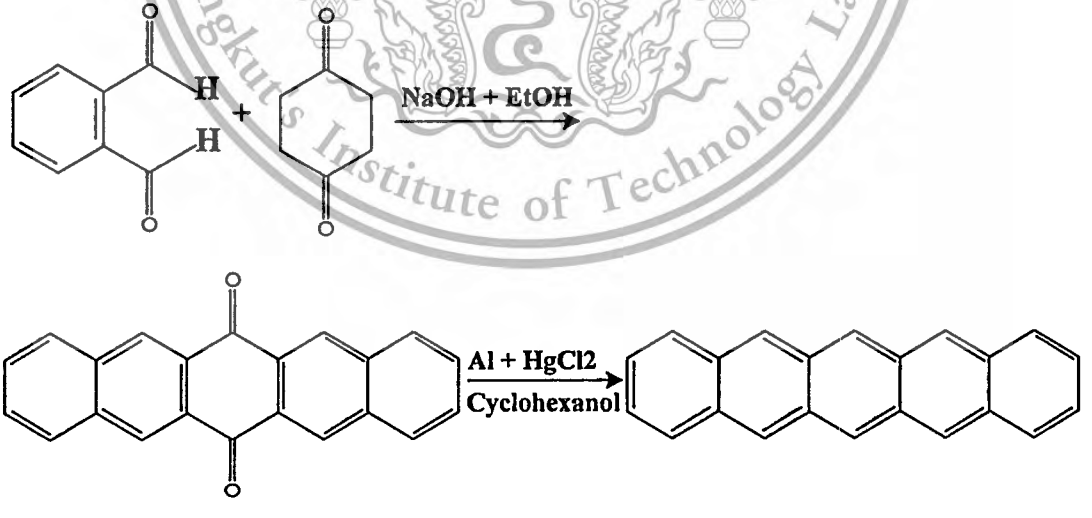

Figure 3.13 The principal synthesis of pentacene from 6,13-pentacenequinone.

Pentacenes are most conveniently synthesized from 6,13-pentacenequinone, which itself is easily prepared by a fourfold aldol condensation between phthalaldehyde and 1,4-cyclohexanedione [61]. Pentacenes are then formed from 6,13-pentacenequinone

by a simple reduction reaction as shown in figure 3.11. In this study, pentacenes (obtained from Sigma-Aldrich) were used, without further purification, as the semiconductor for the OTFTs.

3.4.2 Poly(methyl methacrylate)

PMMA is a transparent thermoplastic and one of the most common plastic materials used in electronics. PMMA was one of the first materials developed for e-beam lithography. It is the standard positive e-beam resist and still remains one of the highest resolution resists available today.

PMMA is the synthetic polymer of MMA. MMA, in bulk liquid form or suspended as fine droplets in water, is polymerized whereby its molecules are linked together in large numbers under the influence of free-radical initiators to form solid PMMA. The molecular structure of PMMA is shown in figure 2.6(b). In this study, PMMA is used for the gate dielectric layer in the OTFTs.

3.4.3 Poly-4-vinylphenol

Linear, high molecular weight poly-4-vinylphenol was first prepared by saponification of poly-4-acetoxystyrene which was obtained by radical polymerization of 4-acetoxystyrene. The polymerization of 4-vinylphenol itself, can be done easily either by the saponification of 4-acetoxystyrene or by the decarboxylation of 4-hydroxycinnamic acid. Recently, however, it has been reported that poly-4-vinylphenol can give, treated with some cationic initiators, polymers of higher molecular weight. But poly-4-vinylphenol is a rather unstable compound and not very easy to handle. In addition, the direct polymerization of vinylphenols often results in polymers whose structure is not fully polyvinylic. This may probably arise because of a reaction between the phenol nucleus and the vinyl group.

A plastic structurally similar to polystyrene is Poly-4-vinylphenol, also called polyvinylphenol or PVP. In electronics, especially in OTFT LCD displays, PVP is used as the dielectric layer in organic transistors. Thin films of cross-linked PVP, often in combination with pentacenes, are used for this application. They are used as substitutes for Novolac resins in photoresists, as adhesion promoter, they improve the heat resistance in hot melt adhesives and the surface treatment in metal finishing. Their derivatives are used as antioxidants and flame retardants in plastics and also as components of polymer blends in order to modify the surface characteristics and improve the impact resistance.

3.4.4 Polystyrene

Polystyrenes are the result of interconnecting styrene monomers. During the polymerization, the carbon-carbon pi bond in the vinyl group is broken. A new carbon-carbon single (sigma) bond is formed by attaching an additional styrene monomer to the chain. The newly formed sigma bond is much stronger than the before broken pi bond, therefore their depolymerization. A chain of polystyrene is usually comprised of a few thousand monomers, resulting in a molecular weight of 100,000–400,000.

The chiral backbone carbons with its 4-bonds-pointing toward the vertices lie at the center of a tetrahedron, this could be shown in a 3-D model. Considering that the -C-C- bonds rotate, the backbone chains lie completely in the plane of the diagram. It is not apparent which of the phenyl (benzene) groups are angled outward and which ones are angled inward from this flat schematic. Isotactic polystyrenes, where all of the phenyl groups are on the same side, are not produced commercially.

Chapter 4

Results And Discussion

4.1 Preparation of gate dielectric for OTFTs

For the application of the dielectric's layer, increasing the capacitance C, through the dielectric constant K, or reducing the film thickness d, reduces the voltage requirement necessary to induce the same amount of charge in the semiconductor as shown in equation (3.6). There are important factors to be considered for the selection and the design of gate dielectric materials. There are not only chemical/mechanical properties of the dielectric semiconductor interface and the ease of processing and reliability. Also the dielectric constant and the film thickness of the gate dielectric layer have to be taken into account. In addition the dielectric roughness which is believed to reduce the mobility in organic semiconductors due to the induced disorder at the accumulation layer.

Figure 4.1 shows optical microscope images of the surfaces of PS, PMMA, and PVP films, being spin coated on a glass substrate at a film thickness of 500 nm. Different surface properties were obtained due to the differences in viscosity, surface tension and chemical contact between the solutions and the substrate, resulting in different adhesion to the glass substrate. Figure 4.1(a) and 4.2(a) shows that the prepared PS film has higher roughness surface than the PMMA and PVP film in figure 4.2(b). According to the OM images, the PVP and the PMMA films will be good candidates for the preparation of thin film dielectrics.

(a) (b) (c)

Figure 4.1 Optical microscope images show uniform films at a thickness of 500 nm of various materials on glass substrate: (a) PS, (b) PMMA, and (c) PVP.

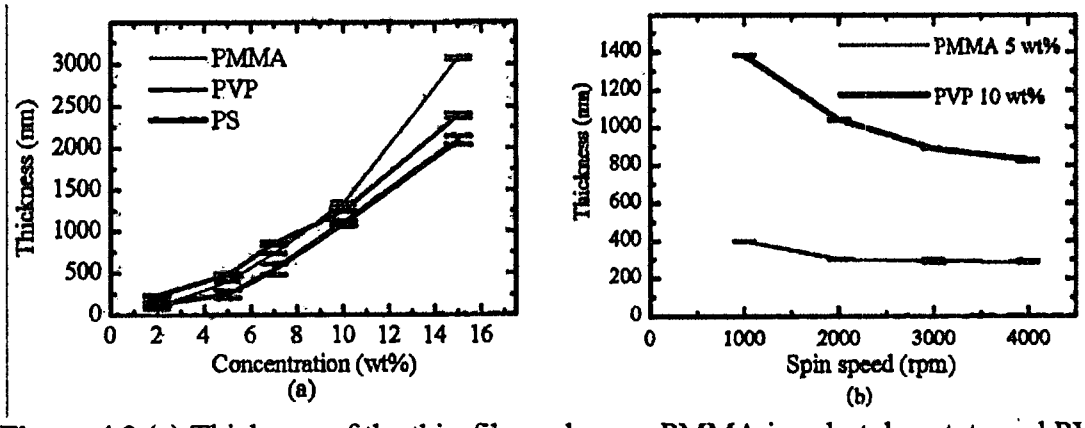

Figure 4.2 (a) Thickness of the thin-film polymers PMMA in n-butyl acetate and PVP mixed, as cross-link agent, with PGMA compared to the coating concentration at a fixed spin speed at 2000 rpm. (b) Thickness of thin-film polymer PMMA in n-butyl acetate and PVP mixed, as cross-link agent, with PGMA compared to the spin speed.

The film properties are controlled by the polymer concentration of the solution used for spinning and the spinning speed. The obtained film thickness is a result of these two parameters. In this investigation, the thin film thickness was not influenced significantly by the spinning time. The concentration and the spinning speed were used to obtain thin films of varying thickness. As expected, by increasing the concentration, the thickness of the layer increases as well. The changes in the observed thickness at a spin-speed of 2000 rpm are shown in figure 4.7(a). To investigate the effect of the spin-speed on the thickness of PVP and PMMA, the solutions were formulated with 10 wt.% and 5 wt.% and finally coated at different spin-speeds, as shown in figure 4.7(b). Then the thickness of each sample was measured. It is obvious, that the used polymer material influences the uniform thin film. This is because the viscosity of the polymer solution changes in relation to the concentration. Thus the concentration is the most suitable parameter to control the thickness of the film. The surface uniformity has been studied in ambient conditions at a thickness of 500 nm, where defects in the layer are clearly visible. The nature of the polymer used affects many factors involved, such as nucleation and changes in its properties. In addition the nature of the solvent affects its evaporation, its evaporation rate and the adhesion to the substrate. All this is related to the used polymer and the polymer's concentration. These factors involved refer to the surface morphology in figure 4.6.

In order to analyze uniform thin films, they can be monitored by a fabricated capacitor to scan on the substrate. It is interesting to see that the behavior of the

capacitance values, when compared to the thickness, can be used for explaining the surface roughness. Their values change with a changing surface roughness. Figure 4.8 shows the different changes in capacitance values according to the thickness of the polymer film for a plane capacitor. These results demonstrate the impact of determined fabrication conditions, by affecting the surface roughness and thus its effect on the capacitance values in a quantitative way. The optimal thickness of the films deriving from PMMA and PVP are at 391 and 700 nm respectively. Because of the lowest thickness achieved and the low surface roughness, the research further concentrated on PMMA as the material for the dielectric layer.

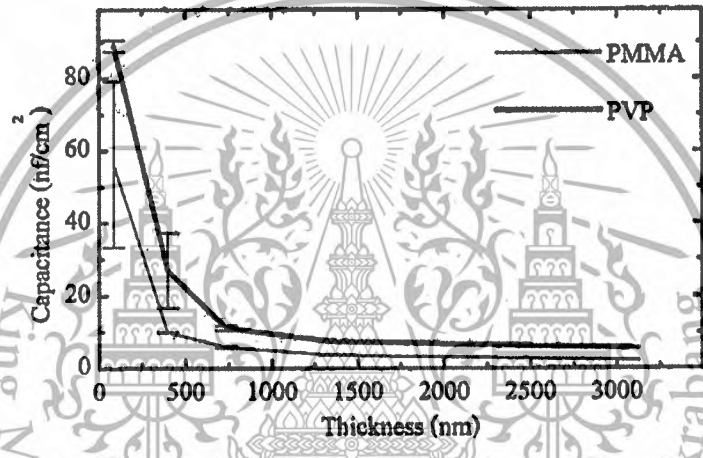

Figure 4.3 Capacitance values in relation to the dielectric's thickness.

4.1.1 Solvent effects on PMMA dielectric material for OTFTs

To study the effect of the spin speed on the thickness of PMMA, the solutions having 3 wt.% PMMA in DMF, nBA, and toluene were coated at different spin speeds. The thickness of each sample was then measured and compared to the spin speed as shown in figure 4.6(a). Among the three solvents used, DMF resulted in the lowest thickness at all spin speeds. This suggests that DMF enables the uniform extended and interconnected PMMA chain network [62]. Moreover, the hydrogen bondings in the PMMA chains formed by the replacement of the methoxy groups in the PMMA by the amide groups of DMF. This is proposed to be responsible for the superior performance of DMF over other solvents used to prepare PMMA [64]. Among all spin speeds experimented, 2000 rpm was found to give the least thickness fluctuation. When using spin speeds higher than 4000 rpm in order to decrease the thickness, fluctuations will occur among different positions on the samples. This can

be seen from the data deviation in figure 4.4(a). Figure 4.4(b) shows the PMMA thickness plotted against the concentration of PMMA in DMF, nBA and toluene, when the spin speed is kept at 2000 rpm. The thickness of 100 nm was obtained using DMF, nBA and toluene at the projected PMMA concentrations of 2.7, 1.7, and 1.2 wt.%, respectively.

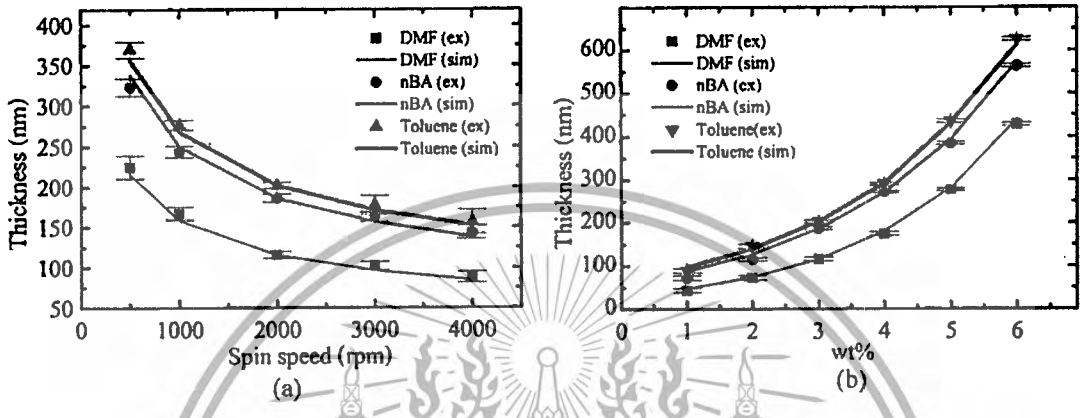

Figure 4.4 (a) Thickness of PMMA films as a function of spin speed and a concentration of 3 wt.% and (b) Thickness of spin-coated PMMA films as function of the PMMA concentrations in DMF, nBA, and toluene at a spin speed of 2000 rpm (where "ex" and "sim" represent experimental and simulation results, respectively).

In order to find the optimal conditions to achieve the desired thickness of around 100 nm to minimize leakage current, maximize breakdown field, and avoid pin-holes and cracks, a simulation of the film thickness with a variation in concentration and spin speed was conducted and found to fit well with experimental results which are shown in figure 4.4(a) and 4.4(b). Apart from the concentration and the spin speed, for example, the rate of evaporation, the substrate's surface energy, the viscosity, and the polymer molecular weight are known to affect the thickness of the spin-coated PMMA films. Lima and Andrade [65] proposed that the thickness h depends on the concentration of the PMMA solution, c, and the spin speed, ω, as indicated in equation (4.1):

$$h = Bc\omega^{-\alpha} \tag{4.1}$$

where the other parameters, which affect the thickness, result in different constants B and α. Walsh et al. [64] proposed a different equation relating the thickness of the PMMA film to c and ω, as shown in equation (4.2):

$$h = Bc^{n}\omega^{-\alpha} \tag{4.2}$$

where the exponent n is the concentration dependent system specific parameter, which is generally larger than 1. Fitting the results obtained using equations (4.1) and (4.2) did not match the experimental results in figure 4.4. However, if the concentration is explained by e^{nc} as in equation (4.3), the experimental data can be well fitted, shown as curves in figure 4.4.

$$h = Be^{nc}\omega^{-\alpha} \tag{4.3}$$

Equations (4.4) – (4.6) show the fitted details for DMF, nBA and toluene, respectively.

$$h = 951.79e^{0.445c}\omega^{-0.453} \tag{4.4}$$

$$h = 1586.26e^{0.375c}\omega^{-0.430} \tag{4.5}$$

$$h = 1502.12e^{0.370c}\omega^{-0.410} \tag{4.6}$$

The surface morphology was investigated and shown in figure 4.5. Uniform and pinhole-free PMMA films were obtained using DMF and nBA as shown in figures 4.5(a) and 4.5(b). However, as shown in figure 4.5(c), a pin-hole was observed in a random scanned area of the PMMA film prepared by using toluene. The surface rms roughnesses of the three samples, prepared by using DMF, nBA and toluene, were 0.34, 0.36 and 0.43 nm, respectively.

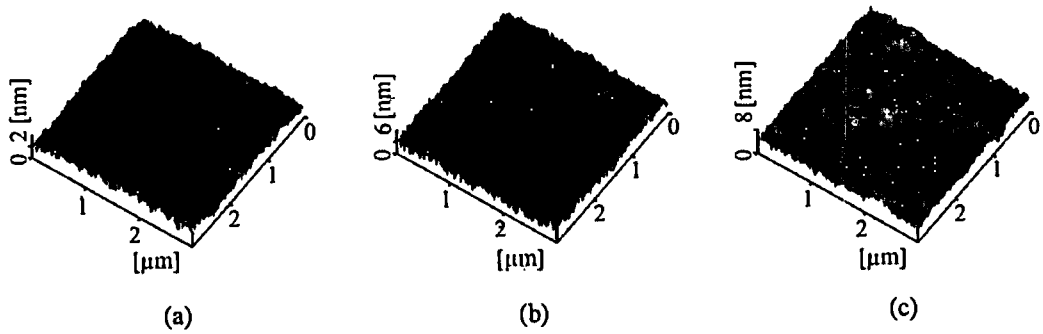

Figure 4.5 AFM images of 100 nm-thick spin-coated PMMA films prepared using (a) DMF, (b) nBA and (c) toluene with the concentrations of 2.7, 1.7 and 1.2 wt.% on glass substrate, respectively.

Figure 4.6 shows the results for the metal insulator metal (MIM), here (Aluminum/PMMA/Aluminum), parallel plate capacitor structure having an area of the 3×3 mm^2. It is obvious, that for the DMF-prepared PMMA, the leakage current density is less than 5×10^{-8} A cm^{-2} for the electric field below ~4 MV cm^{-1}. The leakage currents were found to be higher for the toluene-prepared PMMA than for the DMF-prepared PMMA, but with breakdowns at a similar electric field. The nBA-prepared PMMA showed the highest leakage current densities with a breakdown at a very low electric field.

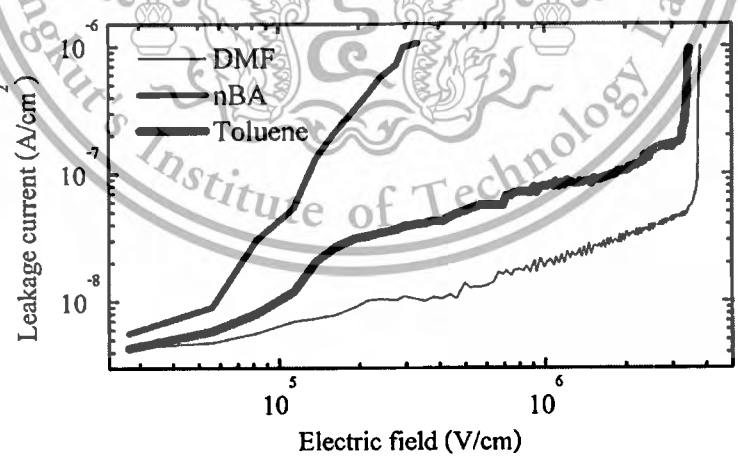

Figure 4.6 Leakage current density compared to the electric field applied to an MIM parallel plate capacitor structure with 100 nm thick PMMA films prepared using DMF, nBA, and toluene at the concentrations of 2.7, 1.7 and 1.2 wt.%, respectively.

Figures 4.7(a) and 4.7(b) show the respective dependence of the dielectric constant, K, and the dissipation factor on the frequency of the applied field, for the different solvents used to prepare the PMMA thin films. The relative dielectric constants were calculated from the measured insulator capacitances of the MIM parallel plate capacitors, using equation (3.6). The relative dielectric constant, as a function of the applied frequency (100 Hz to 1 MHz), for the DMF-prepared PMMA, was found to be the highest among all the solvents. It was followed by the relative dielectric constants of toluene-prepared PMMA and nBA-prepared PMMA.

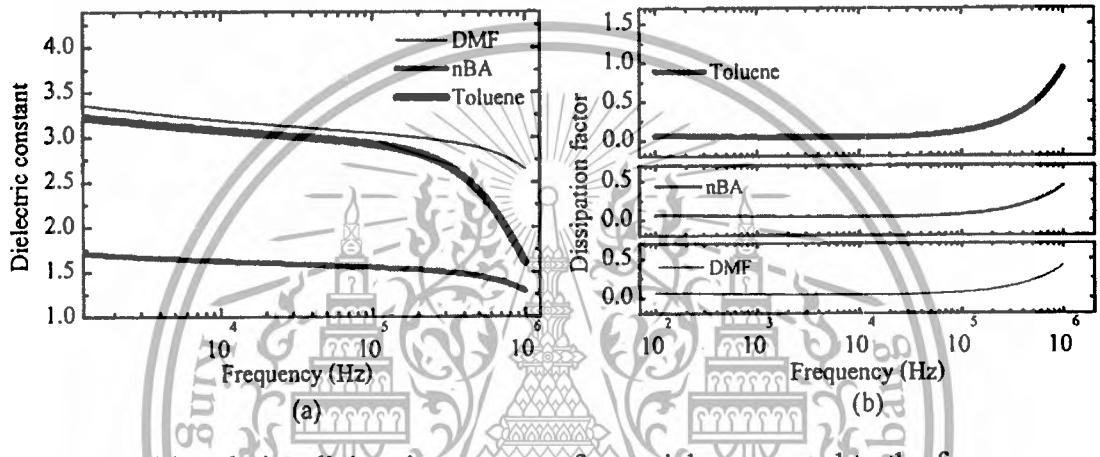

Figure 4.7 (a) Relative dielectric constant of materials compared to the frequency and (b) dissipation factor compared to the frequency of 100 nm-thick PMMA dielectric films prepared using DMF, nBA, and toluene.

An ideal capacitor should only store and release electrical energy without any dissipation. In reality, all capacitors have imperfections, which create resistance, within the capacitor's materials. The dissipation factor (loss tangent), D, is the ratio of the loss index to its relative dielectric constant, which can be calculated from equation (4.7), where K'' is the magnitude of the imaginary part of the relative complex dielectric constant, and K' is the real part of the relative complex dielectric constant. The dissipation factor, however, can be measured directly using the impedance analyzer.

$$D = \frac{K''}{K'} \tag{4.7}$$

Ions in a low-frequency electric field can hop readily out of sites having low free-energy barriers, but they tend to 'pile up' at sites, having high free-energy barriers. This leads to a net polarization of the dipoles and a large value for the relative dielectric constant. At higher frequencies, the polarization due to the charge 'pile-up' disappears and so the relative dielectric constant decreases [66].

4.1.2 DMF dissolved PMMA dielectric materials and their effect on substrates

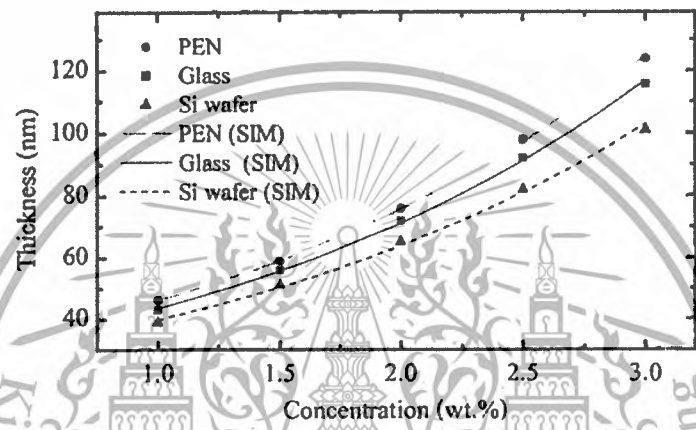

Figure 4.8 Thickness of the PMMA films on PEN, glass and Si wafer at PMMA concentrations of 1.0-3.0 wt.% in DMF at a spin speed of 2000 rpm.

The thickness of the spin-coated PMMA films on glass, PEN and Si wafer substrates at various concentrations, at a spin speed of 2000 rpm were plotted in figure 4.8. The thickness of the film on each substrate, h, was found to increase with increasing PMMA concentration, c. In order to calculate the thickness of the films prepared with different PMMA concentrations, ranging from 1.0-3.0 wt.%, the measured data were curved-fitted with a general exponential equation ($h = Be^{nc}$). The results for the used substrate are shown in the following equations, where equation (4.8) is for glass, (4.9) for PEN, and (4.10) for Si wafer substrates.

$$h = 26.50e^{0.49c} \tag{4.8}$$

$$h = 28.00e^{0.50c} \tag{4.9}$$

$$h = 24.71e^{0.48c} \tag{4.10}$$

The thickness of the PMMA films can be adjusted by controlling the PMMA concentration while the spin speed is kept constant at 2000 rpm. The viscosity characteristics, at various PMMA concentrations, are an important parameter that determines the adhesion ability of the PMMA films. Moreover, the effect of chemical contact and surface morphology of different substrates on the film thickness must also be considered [64],[65]. Figure 4.8 shows that the experimental data fit well with the characteristics shown in equations (4.8) - (4.10).

An AFM was used to investigate the surface morphologies of the PMMA films, as shown in figure 4.9. The surface roughness, rms, of the PMMA films on glass, PEN and Si wafer substrates were 0.26, 0.60, and 1.40 nm, respectively. The PMMA film on glass substrate showed the lowest roughness. This may be a result of the local molecular packing near the surface and a small periodic density fluctuation. These were tentatively attributed to a layering formation due to both, a fast solvent evaporation and a polymer autophobicity during the spin-coating process [63],[66]-[68].

According to the surface roughness profiles shown in figure 4.9, the required concentrations to obtain 95-nm film thickness were 2.60, 2.45, 2.85 wt.% PMMA in DMF for glass, PEN and Si wafer substrate, respectively. The spin speed was 2000 rpm.

Figure 4.9 Surface morphologies of spin-coated PMMA thin film on (a) glass, (b) PEN, and (c) Si wafer.

Minimizing the dielectric's thickness is an alternative way to increase the capacitance of the film, see equation (3.6). The films should have an acceptable leakage current, an effective insulation and sufficient breakdown strength. In figure 4.10 the leakage current densities of the PMMA thin films in the parallel plate capacitor's structure are compared to the applied electric field. The contact area for the measurement was 0.09 mm^2. Comparing the PMMA thin films on Si wafer and on

glass substrates, the difference in the leakage current density is about two orders of magnitude at a strong electric field.

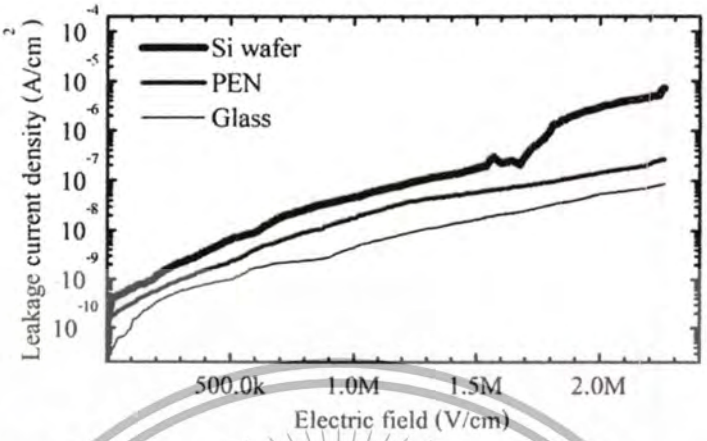

Figure 4.10 The leakage current density compared to the electric field, applied to an MIM parallel plate capacitor structure with 95 nm thick PMMA films prepared on glass, PEN, and Si wafer with the concentrations of 2.60, 2.45 and 2.85 wt.%, respectively.

For the PMMA thin film prepared on the Si wafer substrate, the current density was raised up to 10^{-5} A/cm^2 at an electrical field of 2 MV cm^{-1}. For the PMMA thin films prepared on Glass and PEN substrate, the lower leakage currents of ~10^{-7} and ~10^{-8} A/cm^2 at an electrical field of 2 MV cm^{-1} were obtained. The low leakage current density is the result of a good dielectric film with a low defect density.

In order to analyze the dielectric properties of the PMMA films in parallel plate capacitors deriving from the three substrates, the capacitance-frequency characteristics were investigated by using the relationship in equation (3.6). The relationship between capacitance densities of the PMMA films on different substrates in relation to the frequency is shown in figure 4.11. It can be seen that, at frequencies below 300 kHz, the PMMA film on Si wafer exhibits the highest capacitance density. The distribution of the electric field is inhomogeneous, because the capacitance increases with the surface roughness as a result of the rough and disordered surface [67]. At frequencies above 300 kHz, the PMMA films on glass and PEN have a higher capacitance density than the PMMA film on Si wafer. At high frequencies, the rougher surface results in capacitance density fluctuations, leading to

quantum tunneling, which introduces undesired inductance and resistance in the film [68],[69].

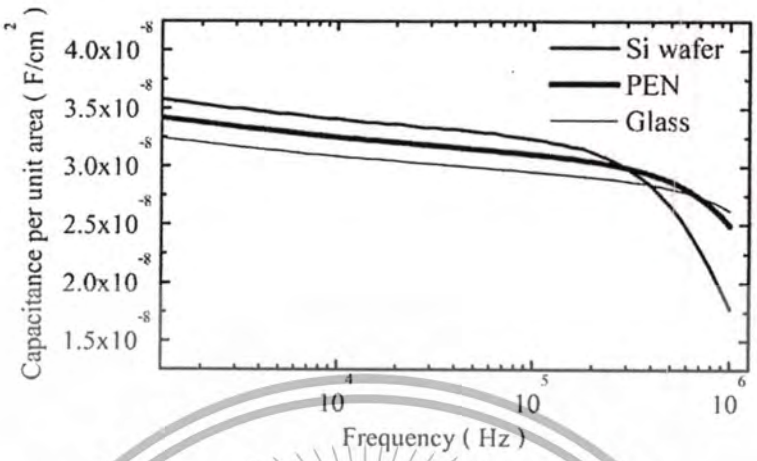

Figure 4.11 Capacitance-frequency plots (0.1kHz - 1MHz) for the PMMA thin films at a thickness of 95 nm on Si wafer, PEN and glass substrates.

Table 4.1 compares PMMA film thicknesses, leakage currents, insulator capacitances, rms roughness, and the substrates from the good values obtained in this study and previously reported values by others. It is clearly shown that the lowest leakage current could be obtained using DMF as the solvent to prepare PMMA dielectric film.

Table 4.1 Comparisons the electrical properties of dielectric layer with materials.

Materials	Solvent	Thickness (nm)	Leakage current (Acm^{-2}) at 2 $MVcm^{-1}$	C_i ($nFcm^{-2}$) at 1 kz	Roughness rms (nm)	Substrate	Ref.
PMMA	DMF	95	3×10^{-8}	33	0.26	Glass	This work
PMMA	nBA	100	$\sim10^{-2}$	-	-	Glass	[35]
PMMA	Toluene	560	-	5.6	0.32	Glass	[37]
PMMA	Anisole	150	5×10^{-8}	21	0.30	Glass	[70]
C-PMMA	nBA	100	$\sim10^{-6}$	-	-	Glass	[71]
PS	Toluene	133	$\sim10^{-6}$	19	2	Si	[73]
PVP	THF	122	$\sim10^{-5}$	42	6	Si	[73]
PVP	PGMEA	200	$\sim10^{-8}$	-	-	Glass	[74]

4.2 An investigation of pentacene as organic semiconductors

Thin-film pentacenes as the organic semiconductor layers were fabricated using the thermal evaporation technique. In order to apply pentacenes as thin films several properties, such as varying thickness, deposition rate and substrate temperature have to be investigated first.

4.2.1 Controlling pentacene thickness in the evaporation system by the mass of the pentacene

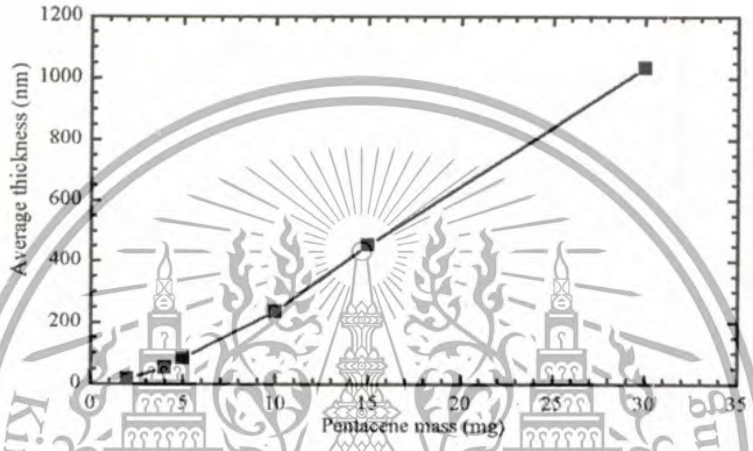

Figure 4.12 Control of thin film thickness of evaporated pentacene by its mass.

The amount of pentacene in the evaporation source was used to control the thickness of thin-film pentacenes. This technique is important for controlling the pentacene thickness in the evaporation system where in-situ thickness monitoring is not possible. The control of the thickness for thin-film pentacenes by monitoring their amount in mg of pentacene is shown in figure 4.12. It shows a plot of the pentacene film thickness in relation to the pentacene mass.

4.2.2 Controlling properties of pentacene thin-films by substrate temperatures

Figure 4.13 shows the surface morphologies having pentacene thin films, with different grain sizes, grown on a thin layer of SiO_2, which is applied to Si substrates having different temperatures.

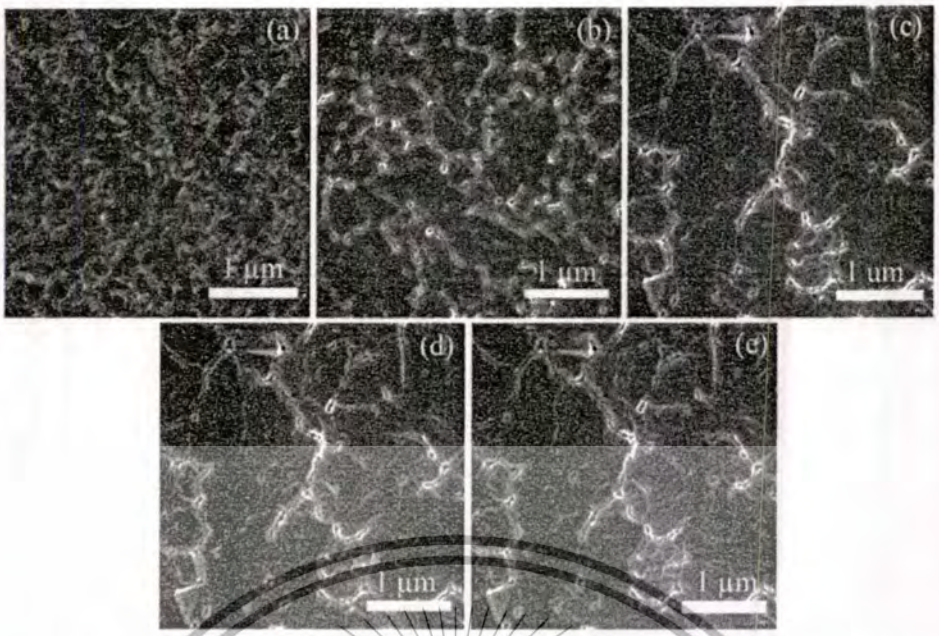

Figure 4.13 SEM images showing the surface morphology of pentacene thin-films prepared on SiO_2 substrate with temperatures of (a) 25 °C, (b) 30 °C, (c) 40 °C, (d) 50 °C, and (e) 60 °C at a deposition rate of 0.1 nm/minute.

4.2.3 Two-step deposition of thin-film pentacene

Pratontep et al.[73] grew submonolayers of pentacenes on SiO_2. Firstly, their data showed that the deposition rate affected the subsequent growth of the pentacene islands, which could be satisfactorily described by a capture zone model, under given conditions of deposition. The nucleation density of pentacene islands on SiO_2 was found to rise as the deposition rate was increased. Controlling the deposition parameters was reported to enable the tuning of the mean size of the pentacene islands, as well as the grain boundary density in the first pentacene layer. Variation in the apparent coverage was significantly affected by the evaporation of the deposited pentacene during nucleation and growth. Secondly, the number of pentacene islands per unit area was found to vary strongly with the changes in growth parameters. For example, as the deposition rate was increased by two orders of magnitude, the number of the islands and thus the density increased by a similar factor. Figure 4.19 displays AFM micrographs of the pentacene films. For the 1 nm thick samples, the bigger nuclei were obtained when the lower deposition rate of 0.01 nm/s was used. At a monolayer thickness of 1.5 nm, a better coverage was observed for the film deposited at a higher rate of 0.05 nm/s. This layer was because of its good coverage then used to deposit the next layer of pentacene. As shown in figure 4.14(c), in the two-step

deposition, the first monolayer was deposited at 0.05 nm/s. The deposition was stopped for 1 hour and the next layer of pentacene was deposited at 0.01 nm/s until the layer thickness reached 10 and 50 nm, respectively.

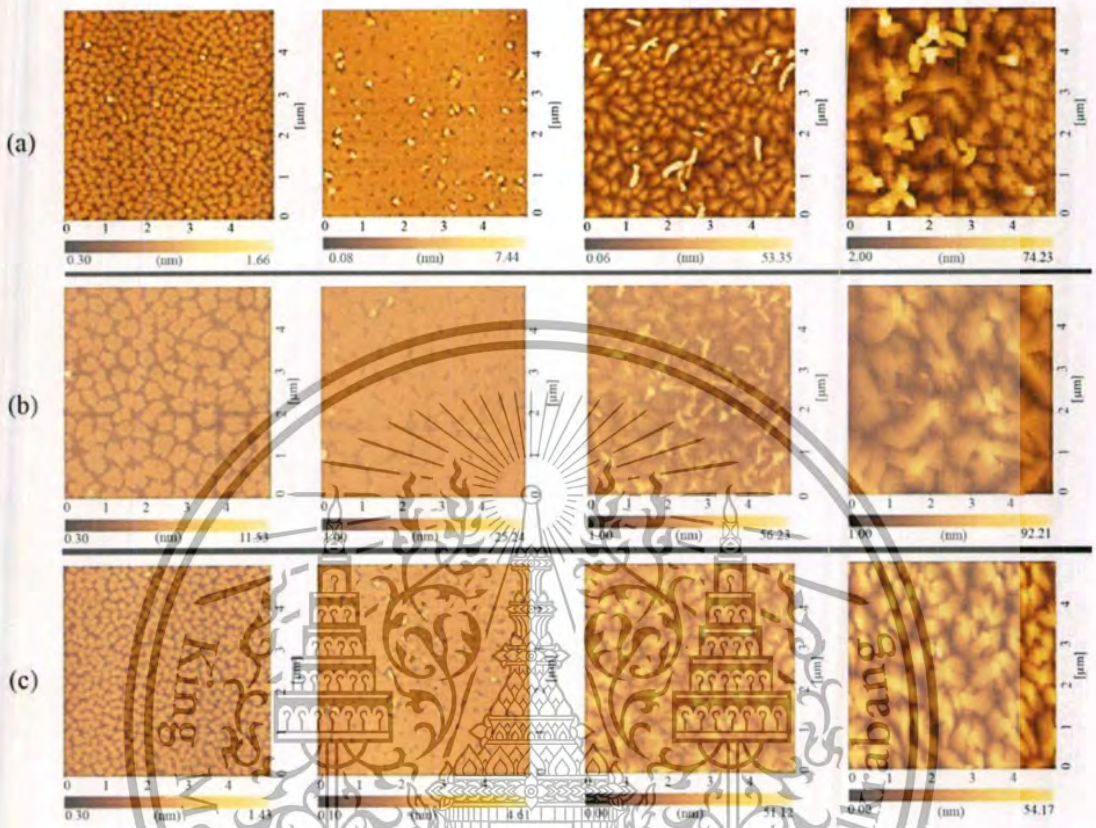

Figure 4.14 AFM of pentacene films deposited on the SiO_2 layer on Si substrates at different deposition rates of: (a) 0.05 nm/s, (b) 0.01 nm/s and (c) two-step deposition rate, the first monolayers were deposited at a rate 0.05 nm/s and the deposition of the second layers at a rate of 0.01 nm/s. The film thicknesses from left to right are 1.0, 1.5, 10, and 50 nm.

Pentacene films were deposited on silicon substrates by using the thermal evaporation technique The depositions were conducted at deposition rates of 0.01 nm/s and 0.05 nm/s, respectively. For both deposition rates, the temperature range of 160-180 ^{0}C was found to be the best for a good morphology of the pentacene thin films. At each deposition rate, the pentacene films were deposited to thicknesses of 1, 1.5, 10 and 50 nm, respectively. Moreover, a two-step growth using 0.05 nm/s for the first monolayer and 0.01 nm/s for the next layer was further investigated.

Figure 4.14 displays AFM micrographs of the pentacene films for the 1 nm thick samples, the bigger nuclei were obtained when the lower deposition rate of 0.01 nm/s was used. At a monolayer thickness of 1.5 nm, a better coverage for the film deposited was observed at the higher rate of 0.05 nm/s. This layer with good coverage was then used to deposit the next layer of pentacene by a two-step deposition. As shown in figure 4.14(c), the first monolayer was deposited at 0.05 nm/s. The deposition was stopped for 1 hour and the next layer of pentacene was deposited with 0.01 nm/s until the layer thickness reaches 10 and 50 nm, respectively. The lower roughness was shown in using two-step depositions.

4.2.4 Modified thin-film pentacene properties

Figure 4.15 shows SEM micrographs of pentacene films on PMMA gate-dielectrics (Pentacene-PMMA). Preheating at 80°C for 10 hours was found to increase the average grain sizes for all deposition rates where 100% grain coalescence with maximizing grain size could be achieved at deposition rates of 1.0 nm/min as shown in figure 4.16. A mixture of terrace- and lamellar-like structures in the pentacene films is observed. The lamellar-like structure has been identified as the bulk phase, where the faceted terrace-like structure has been identified as the thin film phase [74]-[76].

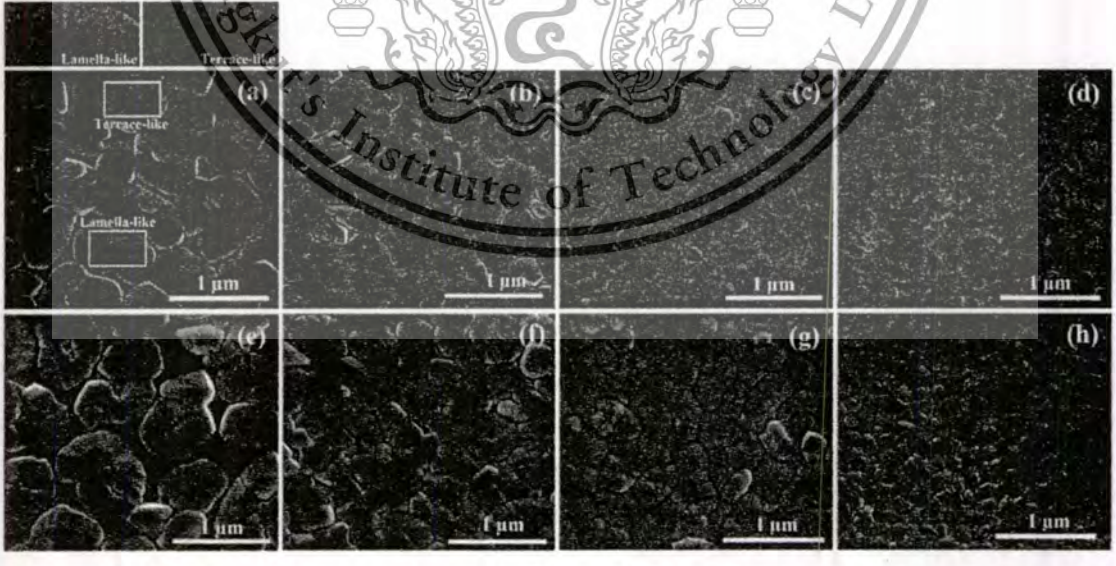

Figure 4.15 Top-view scanning electron micrographs showing pentacene films deposited on PMMA/glass substrates at a substrate temperature of 60°C with deposition rates of 0.1, 0.5, 1.0, 1.5 nm/min (pictures (a), (b), (c) and (d)) without preheating and (pictures (e), (f), (g) and (h)) with preheating, respectively.

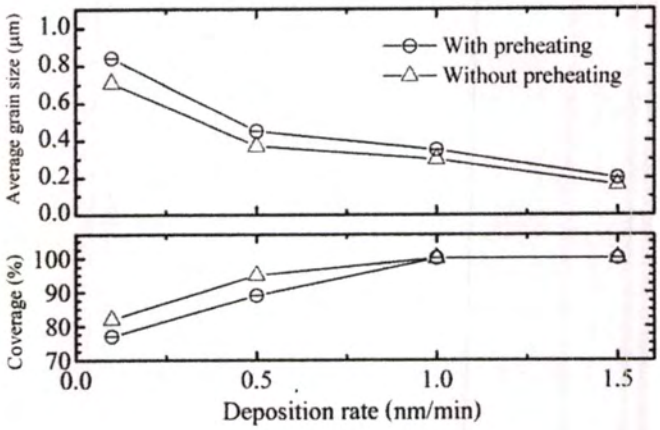

Figure 4.16 Plots of average grain size and coverage percentage according to the deposition rate.

A mixture of bulk and thin film phases in the pentacene films was confirmed by GI-XRD results as shown in figure 4.17. The results show that the pentacene molecules are slightly tilted to the plane of the PMMA dielectrics surface and form a herringbone pattern within the layers [3]. The d(001)-spacings of the thin film phase and the bulk phase are 1.51 and 1.42 nm, respectively. Figure.4.17(c) shows that preheating increases the thin film phase formation at all deposition rates.

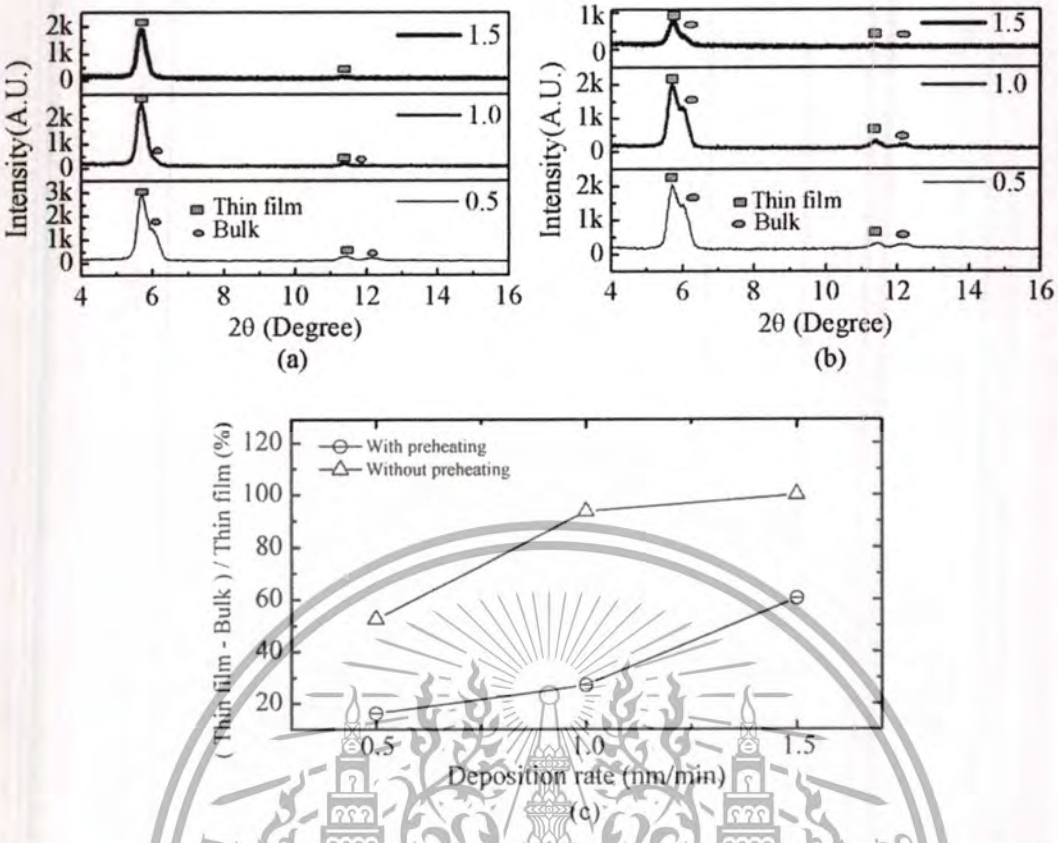

Figure 4.17 (a) GRI-XRD patterns of pentacene films prepared with deposition rates of 0.5, 1.0 and 1.5 nm/min, with and (b) without preheating. (c) Intensity ratio of thin film phase/bulk phase compared to the deposition rate.

Although preheating may give similar effects to post-fabrication thermal annealing on the electrical performance of pentacene organic thin-film transistors [3], it is well-known that charge transport along the interface, between the gate dielectric and the first few pentacene monolayers, is the most important process in the device operation. Preheating is facilitating the early stage deposition of the pentacenes, hence it is proposed to be an effective thermal treatment technique to improve the crystal and electronic structure of the pentacene.

Due to the different surface energies [78],[79] and morphologies of Au source-drain electrodes and PMMA gate-dielectrics, the pentacene layer deposited on them in the actual TFT structure (see figure 3.3), shows different morphologies, which is shown in figure 4.18. Although the effect of gate-dielectric surface energy on morphology of the pentacene has been reported [79],[80], it is interesting to observe a remarkable change in the morphology of the Pentacene-Au compared to the Pentacene-PMMA. The charging effect observed in the Pentacene-Au indicates less

electron mobility than in the Pentacene-PMMA. Higher electron mobility of Pentacene-PMMA is desirable for good carrier transport there. Moreover, electron charging is observed at grain boundaries of Pentacene-PMMA (figure 4.18(a)) and, hence, can be used as a qualitative technique to indirectly observe electron transport in the pentacene layer.

Figure 4.18 SEM micrographs showing pentacene films deposited with preheating to a substrate temperature of 60 °C and a deposition rate of 1.0 nm/min on (a) the PMMA gate-dielectric, (b) the PMMA gate-dielectric and Au source-drain electrode interface and (c) the Au source-drain electrodes.

PES using synchrotron light with a photon energy of 39.70 eV was used to determine work function and position of the highest occupied molecular orbital or valence band states of the pentacene layers on the different layers. The PES spectra of Pentacene-Au and Pentacene-PMMA are shown in figure 4.19. The peak assignment (dashed lines) of the valence band structure of the 51.2 nm thick pentacene layers deposited on Au(111), are taken from Reference [81] and are also shown in figure 4.19. The PES spectra taken from our 50 nm pentacene layers are in fair accordance with the data published and indicated by the dashed lines in figure 4.19. It was found that the σ features in the Pentacene-PMMA sample evolute in comparison with those in the Pentacene-Au. In comparison with the previous data, the predominant π feature that normally appears at 4.4 eV is weak on both spectra. These features indicate that the pentacene molecules on the PMMA gate-dielectric are rather oriented nearly perpendicular to the surface, compared to those on the Au source-drain electrode region. This might result from the rather flat pentacence film being available on the preheated PMMA gate-dielectric, than the one on the Au source-drain electrodes as shown in figure 4.18(a-c).

The inset of figure 4.19 shows the secondary electron cut-off of PES spectra taken from the Pentacene-Au and Pentacene-PMMA samples. The cut-off energy was

used for the determination of the work function. The work function of Pentacene-PMMA (4.19 eV) is found to be about 0.31 eV smaller than that in Pentacene-Au (4.50 eV). The work function of Pentacene-Au is according to the previously reported data on Pentacene-Au(111) (4.52 eV) [80]. Although, the pentacene grain orientation, on the Au source-drain electrodes is not the same as the pentacene grains on the PMMA gate-dielectric (see figure 4.18), the PES results show that the higher pentacene work function over Au ensures a good charge injection between the Au source-drain electrodes and the pentacene [82].

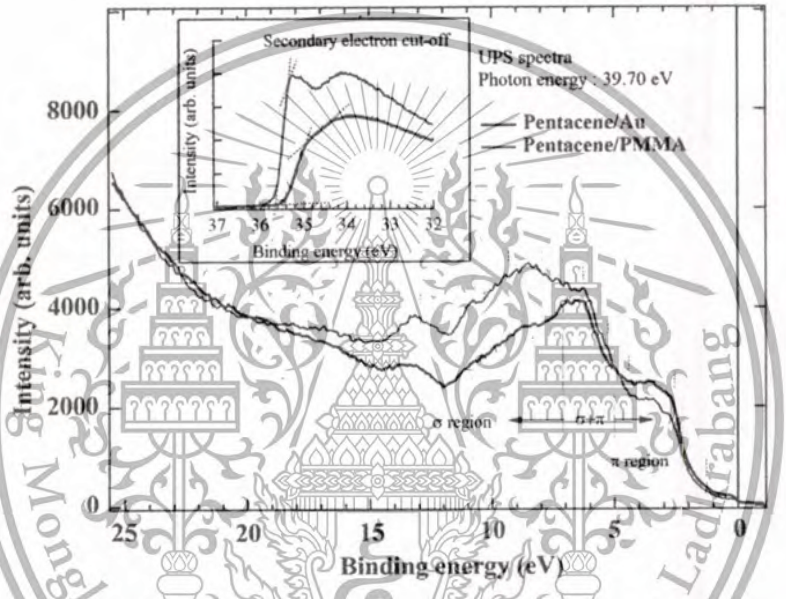

Figure 4.19 PES spectra taken from pentacene films deposited with preheating to a substrate temperature of 60 °C and a deposition rate of 1.0 nm/min.

4.3 Shadow mask preparation

Of the many parameters in the photolithography process, which can be controlled, such as light and exposure time, this research was focusing on the photoresist film, because the availability of materials which are suitable as the photoresist film are limited. That's why a commercially used photoresist was chosen for this research, although it had to be modified in order to use it. Therefore the thinning technique was used to decrease the photoresist films thickness and to increase the resolution of the pattern on the photoresist film. This was created by exposing it to light, which was limited by geometry. Only UV light at a wavelength of 365 nm was used. That a higher resolution of the pattern on the photoresist film can result in a higher resolution pattern of the shadow mask was explained in section

3.2.3. Figure 4.20 shows the thickness according to the etching time of the photoresist film, prepared as shown in section 3.2.2.2. The specification of the photoresist film's thickness is related to the thickness needed for the application. In this study the photoresist film thickness of 10 μm was used to the minimum resolution of shadow mask that can be fabricated OTFTs with 18 μm technology. However, it can be further controlled by the structure of the shadow mask in the electroplating process with a thickness in the range 8-10 μm.

Figure 4.21(b) shows an uniform photoresist film on a stainless plate comparing it before thinning at a thickness of 30 μm and after thinning for 120 sec to a thickness of 10 μm at a developer concentration of 0.25 wt.%.

Under optimized conditions the pattern of the etched resist in figure 4.22 shows a minimum line width of 18 μm.

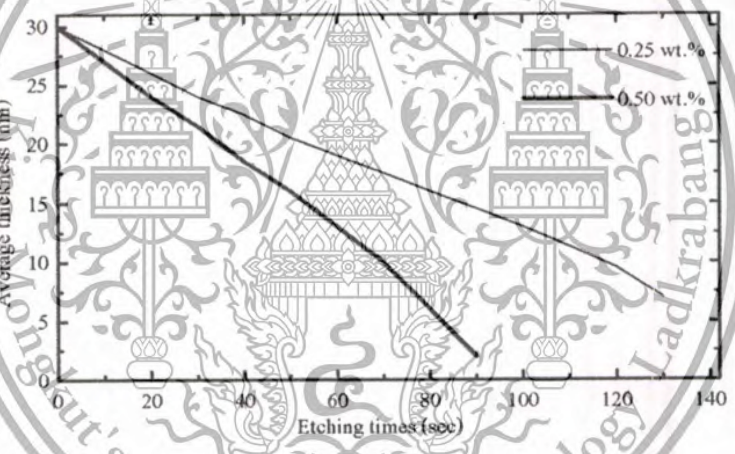

Figure 4.20 Photoresist film thickness controlled by etching times at developed concentrations of 0.25 wt.% and 0.50 wt.% of deionize water.

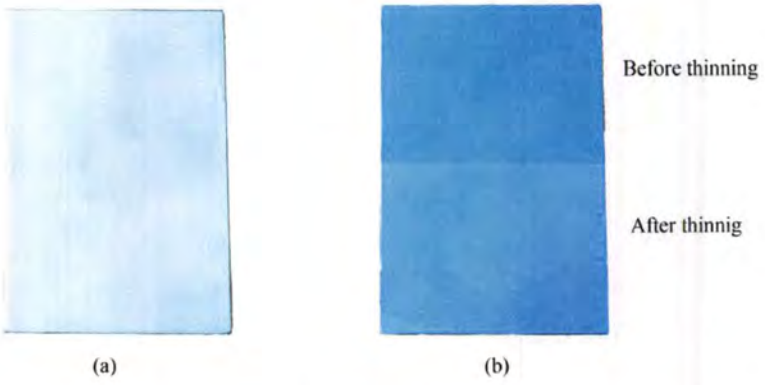

Figure 4.21 (a) Stainless substrate for the fabrication of the shadow mask. (b) Photoresist film prepared on a stainless plate was compared before and after the thinning process.

Figure 4.22 (a) Photoresist film patterned, (b) Photoresist film patterned on shadow mask. The circled area was used for the second step in the two-step fabrication of the shadow mask (c) Minimum line width of approximately 18 µm patterned on the photoresist film.

In the electroplating process, the thickness of the metallic mask was controlled by the deposition times as shown in figure 4.23. The treated area was 4 cm × 4 cm, the distance between the nickel bar and the stainless plate was 5 cm and a current of 0.5 A was applied. The time was used to limit the thickness of the shadow mask and ensure the thickness of the coated nickel is according to the patterned photoresist. In case of the shadow mask's thickness being thicker than the photoresist film patterned, distortions are raised in the shadow mask structures. These will reduce the performance of the device. Therefore a difference in the thicknesses must be avoided.

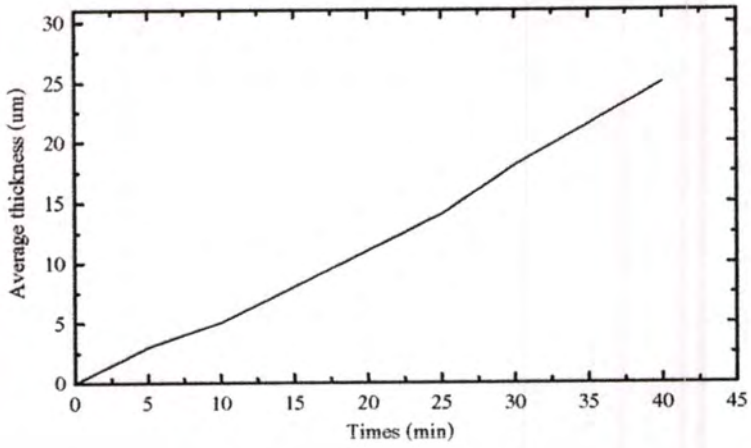

Figure 4.23 Growth of the shadow mask's film thickness on a stainless plate according to the time of application.

4.2 A two-step shadow mask fabrication

In practical, the shadow mask is used in the thermal evaporation process to pattern a device structure. The shadow mask should be stable enough for alignment, therefore the nickel coated on the stainless plate should be thick enough as shown in figure 4.24(b). At least the nickel layer should be thicker than 30 μm. However, the fabrication of high resolution pattern of the shadow mask depends on the pattern of the photoresist film, which should have the lowest thickness (10 μm), as explained before. According to the two-step shadow mask fabrication the photoresist film is minimized in the first step to the thickness 10 μm, in order to fabricate a high resolution photoresist film pattern. But at this thickness the shadow mask is not stable enough as shown in figure 4.24(a). In the second step, for the fabrication of the frame, the photoresist film is applied on top of the shadow mask's working area as shown in figure 4.22(b). A resolution pattern of 18 μm can be routinely obtained from for this process as shown in figure 4.24(c).

(a) (b) (c)

Figure 4.24 (a) single-step shadow mask, (c) two-step shadow mask, and (d) shadow mask pattern.

4.5 Fabrication of pentacene organic thin film transistors

4.5.1 First generation OTFTs

A 260 Poly-4-(vinylphenol) PVP (40 mg/ml in Propylene glycol monomethyl ether Acetate (PGMA)) was mixed with the poly (melamine-co-formadehyde) methylated (40% V/V in PGMA) in a 1:1 volume ratio in order to improve the smoothness of the film. A smooth gate dielectric promotes a better molecular ordering in the active layer, leading to improved charge transport and carrier mobility. The polymer blend was spin coated at 2000 rpm on glass substrate and cured for 1 minute at 100 °C. Cross-linking was allowed for 5 minutes at 500 °C to make the film more robust. The dielectric layer's thickness was 260 nm. The dielectric characteristics of the dielectric films were evaluated by quantitative leakage current and capacitance measurements. Typical current density-electric field (J-E) plots for parallel-plate capacitors, fabricated with a 260-nm PVP dielectric layer, usually demonstrate a leakage current density of $1\text{-}5\times10^{-7}$ A/cm^2. The electric field across the film is up to $8\text{x}10^6$ V/cm (i.e. 20 V of the applied voltage). PVP films of good electrical uniformity can be deposited on glass, using the current experimental procedure. The permittivity value of the thin-film capacitor is measured to be 3.5 at 100 Hz. Thermal evaporation was used to deposit a 100nm thick gold source-drain electrode through shadow masks. The thickness of the pentacene film applied with a deposition rate of 3 nm/s is obtained at 20 nm. The pressure was held below 5×10^{-6} mbar during the active layer deposition. A high degree molecular ordering in the active organic material is necessary for high-mobility devices, but requires careful control of the film deposition conditions [83],[84]. The geometrical resolution of 35µm

can be achieved. The transistors were fabricated with channel-length (L) of 35 μm and channel-width (W) of 500 μm. The gate-source and gate-drain overlap distance were measured to be 10 μm.

The gate and drain voltages were independently varied from 0 to -20 V to obtain the I-V characteristics of the OTFT. Mobility values of 0.02 $cm^2/V.s$, an on/off current ratio of 416. Figure 4.25 shows the measured I_D-V_{DS} (b) and I_D-V_{GS} (a) of the OTFTs.

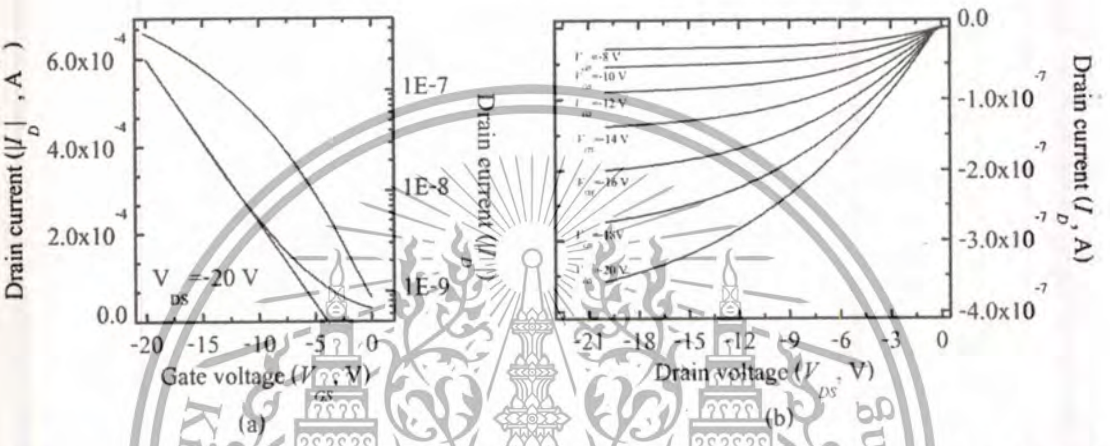

Figure 4.25 (a) I_D-V_{GS} and $I_D^{1/2}$-V_{GS} characteristics and (b) I_D-V_{DS} characteristics of the OTFTs.

The problems arising in this experiment were the short life-time and a variation of field effect mobility found in the dielectric layer when operating the OTFTs. In contrast the capacitance values varied highly for the dielectric layers at a thickness of 260 nm as shown in figure 4.8. This derived from preparing the PVP solution used in the process with a cross-link reagent. The properties of the cross-link reagent, like sol-gel, make it difficult to dilute it completely. This leads to unwanted effects of the cross-link polymer chain in the thin-film dielectric layer.

4.5.2 Second generation OTFTs

In this investigation, the two step deposition technique was used in the fabrication process of the semiconductor layer. The effect of the deposition rate and time on the morphology of thin film pentacene was investigated.

The fabrication of OTFTs, starts with thermal evaporation to deposit a 50nm thick Al gate electrode through shadow masks, at the base pressure of 5×10^{-6} mbar on to the substrate. Then the PMMA from a 5 wt.% solution in n-buthyl acetate was

spin-coated to a thickness of 390 nm. This was performed at 1000 rpm for 180 seconds and cured at 100 °C in a nitrogen glove box for one hour. The stable annealed PMMA showed a capacitance density of 9.94 nF/cm^2 and a leakage current density of 10^{-8} A/cm^2 at an electric field of 5 MV/cm. Next the 50 nm thick the Au source-drain electrodes were deposited through shadow masks at the base pressure 5×10^{-6} mbar. And final the 50 nm semiconductor layer was deposited by applying the two step deposition technique at the base pressure 5×10^{-6} mbar

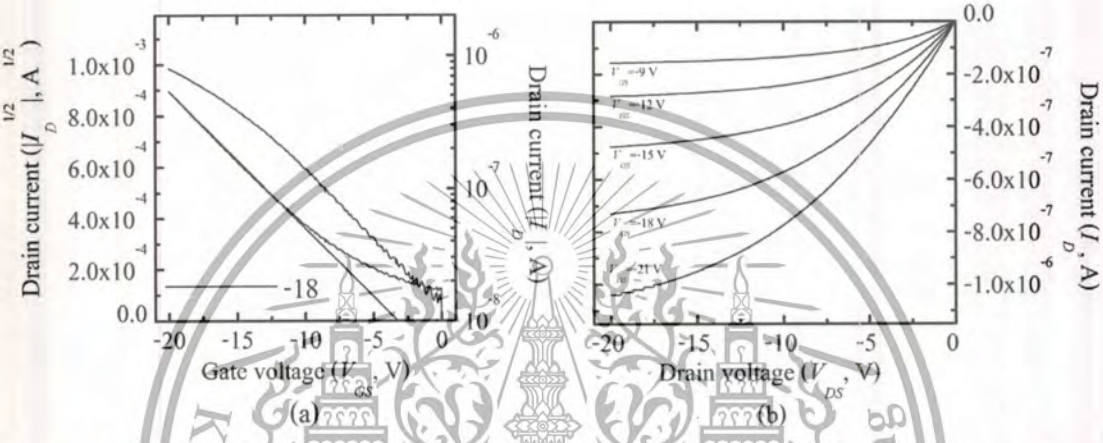

Figure 4.26 (a) I_D-V_{GS} and $I_D^{1/2}$-V_{GS} characteristics and (b) I_D-V_{DS} characteristics of the OTFTs.

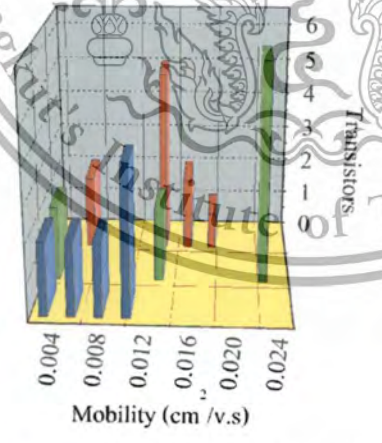

Figure 4.27 Mobility of the OTFTs fabricated at different deposition rates of 0.05 nm/s, 0.01 nm/s and 0.05 nm/s followed by 0.01 nm/s (two-step).

Figure 4.26 shows the measured drain current characteristics of the OTFTs fabricated with the two-step deposition technique as described in section 4.4.3. The gate and drain voltages of the transistors were independently varied from 0 to -20 V to

obtain I-V characteristics. Mobility values of 0.02 $cm^2/V.s$ and the minimum OFF current of about 100 pA were measured at V_{DS} = -20 V. It can be seen that the mobility is low and slightly fluctuated at the high deposition rate as shown in figure 4.27. According to this, the two step deposition process can produce thin films with low roughness

The problem of this experiment was that the on-off ratio became low with the improved morphology of the semiconductor layer. This is the result of the pentacene molecular orientation was forming a lattice structure. The random in the lattice structure resulted in the band energy of the pentacene semiconductor layer operating near conductor range.

4.5.3 Third generation OTFTs

In this investigation, the preheating technique was used in the fabrication process of the semiconductor layer. In the preheating process, the thin film pentacene with a thickness of 50 nm were deposited by thermal evaporation at the optimized evaporation rates and a substrate temperature of 60 °C. The above deposition conditions were applied with preheating at 80 °C for 10 hours.

For fabrication OTFT, start with thermal evaporation was used to deposit a 50 nm thick Al gate electrode through shadow masks at the base pressure 5×10^{-6} mbar on to substrate. Next The 390 nm thick spin-coating of PMMA from a 5 wt.% solution in n-buthyl acetate was performed at 1000 rpm for 180 seconds and cured at 100 °C in a nitrogen glove box for one hour. The stable annealed PMMA showed a capacitance density of 9.94 nF/cm^2 and a leakage current density of 10^{-8} A/cm^2 at an electric field of 5 MV/cm. Next the 50 nm thick deposited of the Au source-drain electrodes through shadow masks at the base pressure 5×10^{-6} mbar. And final the 50 nm semiconductor layer was deposited by applying preheating technique at the base pressure 5×10^{-6} mbar

Figure 4.28(a) shows I_D-V_{GS} and $I_D^{1/2}$-V_{GS} characteristics and 4.28(b) shows the I_D-V_{DS} characteristics of the pentacene OTFT fabricated in preheated technique, among all deposition rates experimented, the best field-effect mobility was obtained (0.01 $cm^2/V.s$) from the deposition rate of 1 nm/min as shown in figure 4.29. An on-off ratio of 3×10^3 and a threshold voltage of - 4.2 V were obtained from the best pentacene OTFT. The values of mobility, on-off ratio and threshold voltage obtained are typical values for both the bottom-contact and top-contact pentacene OTFT with

PMMA as the gate dielectric [85]-[87]. They are two orders of magnitude lower than the conventional top-contact OTFT with SiO_2 gate dielectrics, which is caused by the poorer morphology of the pentacene films around the source-drain electrodes in the PMMA based devices system [88].

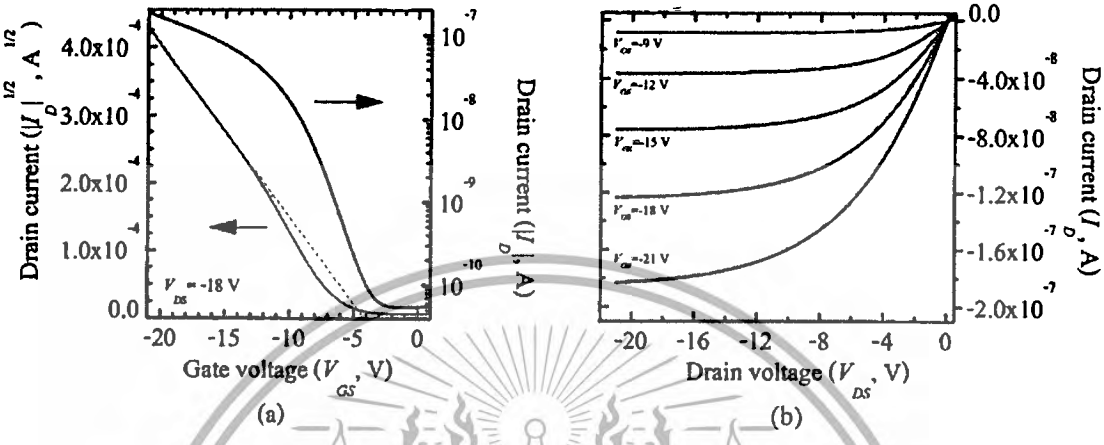

Figure 4.28 (a) I_D-V_{GS} and $I_D^{1/2}$-V_{GS} characteristics and (b) I_D-V_{DS} characteristics of the OTFTs fabricated using preheating at 80 °C for 10 h, at a substrate temperature of 60 °C and a deposition rate of 1 nm/min.

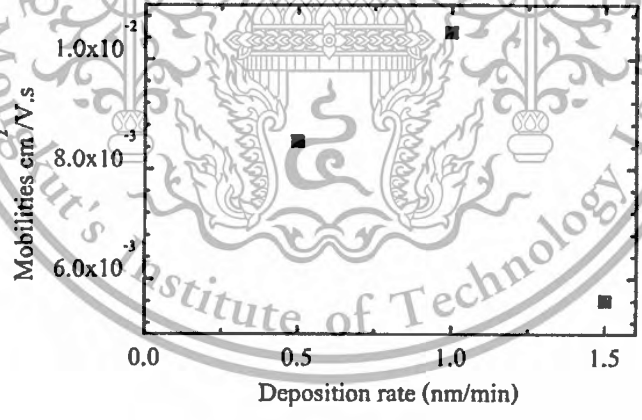

Figure 4.29 Field-effect mobility compared to deposition rate for the OTFTs

The problem of this experiment was the low field effect mobility. However, the orientation of the pentacene molecules in lattice structure was improved to the thin-film phase of the thin-film pentacene layer and thus the semiconductor properties were improved and show a high on-off ratio. In postulation, if increasing the field effect, by decreasing the thickness of dielectric layer, then the amount of charge carrier would increase in the OTFTs' operation. The decreasing dielectrics' thickness

can improve the field effect mobility as mentioned in equation (3.6) and proposed by Yun el at.[70]

4.5.4 Fourth generation OTFTs

In this investigation, the optimized process fabrication of the dielectric layer to 95 nm thickness by spin-coating, PMMA solution in DMF was compared on several substrates.

For fabrication OTFT, start with thermal evaporation was used to deposit a 50 nm thick Al gate electrode through shadow masks at the base pressure 5×10^{-6} mbar on to substrate. Next the 95 nm thick spin-coating of PMMA from a 4 wt.% solution in DMF was performed at 2000 rpm for 180 seconds and cured at 120 °C in a nitrogen glove box for one hour to uniform dielectric layer. The stable annealed PMMA showed a capacitance density of 33 nF/cm^2 and a leakage current density of 10^{-8} A/cm^2 at an electric field of 2 MV/cm. Next thermal evaporation was used to deposit a 50 nm thick Au source-drain electrodes at the base pressure 5×10^{-6} mbar. And final the 50 nm semiconductor layer was deposited through a shadow mask at a rate of 0.1 nm/min and a base pressure of 5×10^{-6} mbar

Figure 4.30(a) and (b) show I_D-V_{GS} and $I_D^{1/2}$-V_{GS} characteristics of the OTFTs prepared on glass. Figure 4.31(a) and (b) show I_D-V_{DS} characteristics of the OTFTs prepared on PEN. As described by equation (2.9), the mobilities and threshold voltages of the OTFTs can be calculated from the slopes and x-axis intercepts of their corresponding $I_D^{1/2}$-V_{GS} graphs. The calculated mobilities of the OTFTs on glass and PEN substrates are 0.16 cm^2/V.s and 0.09 cm^2/V.s, respectively. The threshold voltages of the OTFTs on glass and PEN substrates are 3.60 V and 4.50 V, respectively.

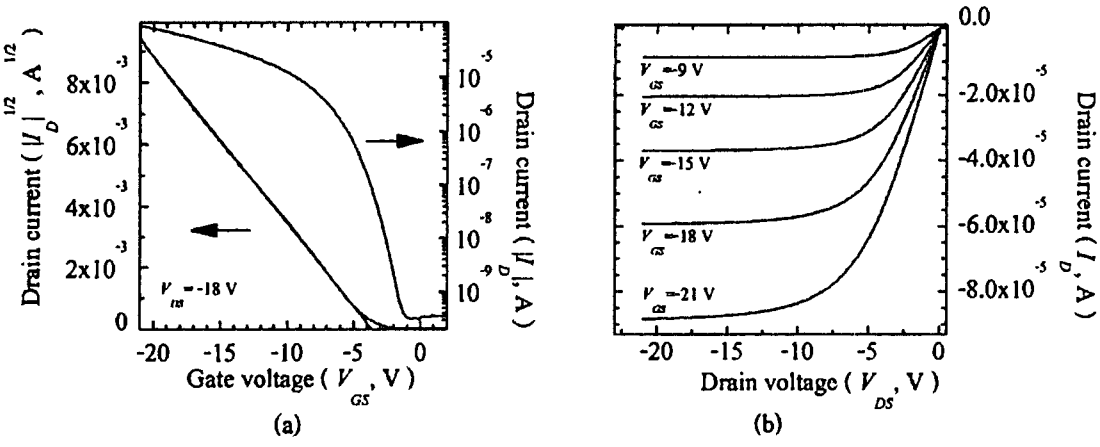

Figure 4.30 (a) I_D-V_{GS}, $I_D^{1/2}$-V_{GS}, characteristics and (b) I_D-V_{DS} characteristics of the OTFTs fabricated on glass substrate.

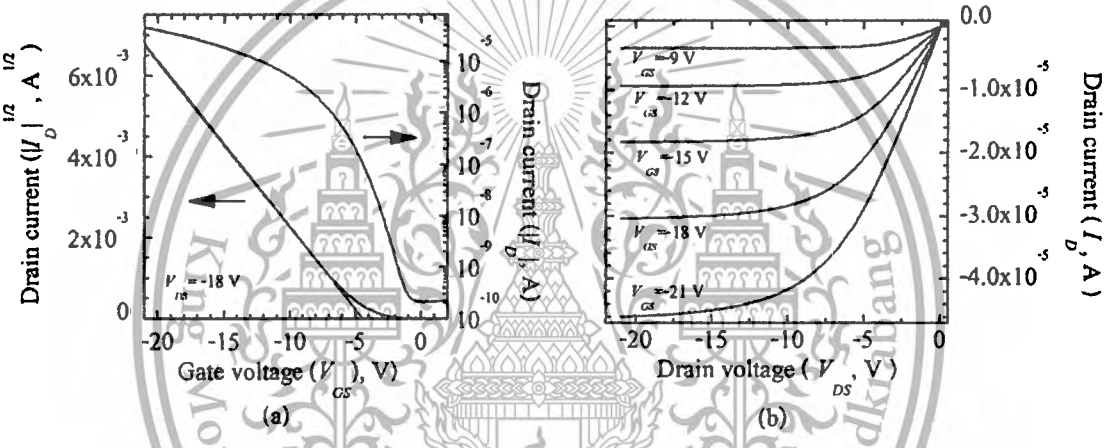

Figure 4.31 (a) I_D-V_{GS}, $I_D^{1/2}$-V_{GS}, characteristics and (b) I_D-V_{DS} characteristics of the OTFTs fabricated on PEN substrate.

The subthreshold factor S is defined in equation (2.11). A change in the gate-source voltage is required to increase the drain current by a factor of 10. S is calculated by the inverse of the slope of the I_D-V_{GS} graphs in figure 4.30(a) and 4.31(a). The calculated S values for the OTFTs on glass and PEN substrates are 0.98 and 1.23 V/decade, respectively. The calculated mobilities, threshold voltages and subthreshold factors show that PMMA films, prepared on different substrates influence the OTFTs performance significantly.

The difference in capacitance characteristics of the PMMA films on different substrates supports previous explanations [89]-[91], that the PMMA dielectric layers affect the disorder induced in the accumulation zone of the organic semiconductor

layer in the OTFT structure and thus disturb π-π stacking, resulting in different OTFT's performances.

The fabrication process of OTFTs is very complex and complicated, meaning every step of the fabrication has to be investigated and optimized. Optimizing the fabrication process for all layers, is the key to improve the electrical performance of the OTFTs. However, the highest significant improvement regarding the electrical performance of our fabricated OTFTs was achieved for the dielectric layer.

Chapter 5

Circuit Design and Simulation

5.1 Device modeling

Models for simulating DC characteristics of bottom-contact OTFTs are proposed for device characterization as mentioned in the section 4.5.3. The OTFTs electrical behavior was simulated by a for hydrogenated amorphous silicon (a-Si:H) thin film transistors adopted SPICE model . Using the output and transfer characteristics in figure 4.31, the model parameters were extracted using a commercial simulation software AIM Extract for the AIM-SPICE a-Si TFT Model ASIA2 on level 15. Estrada et al. applied the unified model and parameter extraction method (UHEM) to a-Si:H [92], to nano-crystalline silicon transistors [93] and recently to OTFTs [94]. This method is used to extract the parameters of two transfer characteristics, the linear and the saturation region above the threshold region. In order to reduce experimental noise for the output characteristic of the device an integral method has to be used. Device parameters are extracted directly from the experimental results. The modeling and parameter extraction method is crucial to determine device parameters required for an accurate simulation of semiconductor devices, circuits and systems.

It is known for the measured output characteristics of OTFTs, that mobility usually increases when V_{GS} is applied, and the mobility further increases when V_{DS} is applied in addition to V_{GS}. This increase of mobility is related to carrier hopping [95], a Frenkel-Pool type effect related to traps in material [96], according to which the emission barriers are lower in trap located areas at the boundaries between crystals of the polycrystalline semiconducting layer. The mobility dependence on V_{GS} is described as [97]:

$$\mu_{FET} = \mu_p \left[\frac{(V_{GS} - V_T)}{V_{AA}} \right]^{\gamma_A} \tag{5.1}$$

where V_T is the threshold voltage and γ_A and V_{AA} are curve-fitting parameters. μ_p is the mobility of the polycrystalline semiconducting layer's operation in the OTFT. Drain current in the linear and saturation regions is modeled as:

$$I_{DS} = C_i \frac{\mu_{FET}(V_{GS} - V_T)}{1 + R.\frac{W}{L}.C_i.\mu_{FET}.(V_{GS} - V_T)} \times \frac{V_{DS}(1 + \lambda V_{DS})}{\left[1 + \left[\frac{V_{DS}}{V_{DSsat}}\right]^M\right]^{\frac{1}{M}}} + I_0 \quad (5.2)$$

where $Z=(W/L)C_i\mu_p$, W is the channel width, L is the channel length, C_i is the gate capacitance, R is the source plus drain resistance, I_0 is the leakage current and m and λ are fitting parameters related to the knee region and to the channel length modulation respectively. In order to extract the parameter for the drain current, in the linear and saturation regions, and neglecting the leakage current, it is modeled as:

$$I_{DS} = \frac{Z/V_{AA}^{\gamma}}{1 + R(Z/V_{AA}^{\gamma})(V_{GS} - V_T)^{1+\gamma}} \times \frac{(V_{GS} - V_T)^{1+\gamma} V_{DS}(1 + \lambda V_{DS})}{\left[1 + \left[\frac{V_{DS}}{V_{DSsat}}\right]^M\right]^{\frac{1}{M}}} \quad (5.3)$$

The drain current in the linear region of polycrystalline semiconducting layer's operation in OTFTs for a small V_{DS} as in equation (5.1), and for $V_{GS}>V_T$ written as:

$$I_{DSlin} = \frac{Z}{V_{AA}^{\gamma}}(V_{GS} - V_T)^{1+\gamma} V_{DS} \quad (5.4)$$

The intrinsic channel conductance in linear region g_{ch} for low drain voltage is express as:

$$g_{ch} = \frac{Z}{V_{AA}^{\gamma}}(V_{GS} - V_T)^{1+\gamma} \quad (5.5)$$

The expression of the channel conductance and effect of total resistance at drain and source $R=R_D+R_S$ is take into account series resistance

$$g_l = \frac{g_{ch}}{1 + Rg_{ch}} \quad (5.6)$$

Where the saturation voltage, V_{DSsat} is defined by the saturation modulation parameter α_S:

$$V_{DSsat} = \alpha_s (V_{GS} - V_T) \tag{5.7}$$

For $V_{DS}=V_{GS}>V_{DSsat}$, from equation (5.2) the saturation current can be approximated by:

$$I_{DSsat} = \frac{Z}{V_{AA}^{\gamma}} \alpha_s (V_{GS} - V_T)^{(2+\gamma)} \tag{5.8}$$

For the OTFTs fabricated, the parameters γ_A and V_{AA} are extracted from the exponential behavior in the linear region by equation (5.4). The integral procedure proposed by [6] is used to extract V_T and γ_A in the linear region. The function $H(V_{GS})$ is defined as following:

$$H(V_{GS}) = \frac{\int_0^{V_{GS}} I_{DSlin}(x)dx}{I_{DSlin}(V_{GS})} \tag{5.9}$$

The result of the integration in equation (5.7) is then divided by I_{DS} as explained in equation (5.8):

$$H(V_{GS}) = \frac{1}{2+\gamma}(V_{GS} - V_T) \tag{5.10}$$

The plot between $H(V_{GS})$ and V_{GS} is used to obtain V_T from the interception with the V_{GS} axis and γ_A from the slope for $V_{GS}>V_T$. From equation (5.4), the plot between $I_{DS}^{1/(1+\gamma)}$ and V_{GS} is used to extract the value of V_{AA} by the slope S_I from

$$V_{AA} = \left[\frac{ZV_{DS}}{S_I^{1+\gamma}}\right]^{1/\gamma} \tag{5.11}$$

From equation (5.6), the plot between $I_{DS}^{1/(2+\gamma)}$ and V_{GS} is used to extract the value α_S by the slope S_s from

$$\alpha_S = \frac{S_S^{2+\gamma} V_{AA}^{\gamma}}{Z} \tag{5.12}$$

For the saturation region in equation (5.5), the value of M is extracted from equation (5.1) as:

$$M = \log 2 / \log\left[\frac{Z}{V_{AA}^{\gamma}} \frac{\alpha_s (V_{GS} - V_T)^{2+\gamma}}{I_{DSsat}(V_{DSsat})}\right] \tag{5.13}$$

The effect introduced by R can be significant even at relatively low currents from equations (5.4)-(5.6) is written as:

$$R = \left(\frac{Z}{V_{AA}^{\gamma}}(V_{GS} - V_T)^{1+\gamma} \bullet \frac{V_{DS}}{I_{DSI}} - 1\right) \Big/ \frac{Z}{V_{AA}^{\gamma}}(V_{GS} - V_T)^{1+\gamma} \tag{5.14}$$

From equation (5.1) and in saturation current can be approximated the channel length modulation λ as:

$$I_{DSsat} = \frac{Z}{V_{AA}^{\gamma}}(V_{GS} - V_T)^{2+\gamma}(1 + \lambda V_{DS}) \tag{5.15}$$

The result of the differential saturation current I_{DSsat} in equation (5.15) as explained the channel length by slope S_{SS} in saturation region in equation (5.16)

$$\lambda = S_{SS} \Big/ \frac{Z}{V_{AA}^{\gamma}}(V_{GS} - V_T)^{2+\gamma} \tag{5.16}$$

Table 5.1 shows summary result of valuated parameters using (UHEM) and modeled of the fabricated OTFTs. Figure 5.1 shows modeled output characteristics of the fabricated OTFTs. As can be seen, the device modeling for the fabricated OTFTs has very good characteristics.

Table 5.1 Modeled parameters

Parameter	Modeled
V_T [V]	-4.5
γ_a	2.42
V_{aa}	165
μ_0[cm^2/V.s]	0.09
R[kΩ]	50
α_s	0.28
M	3
λ [1/V]	1.16×10^{-5}

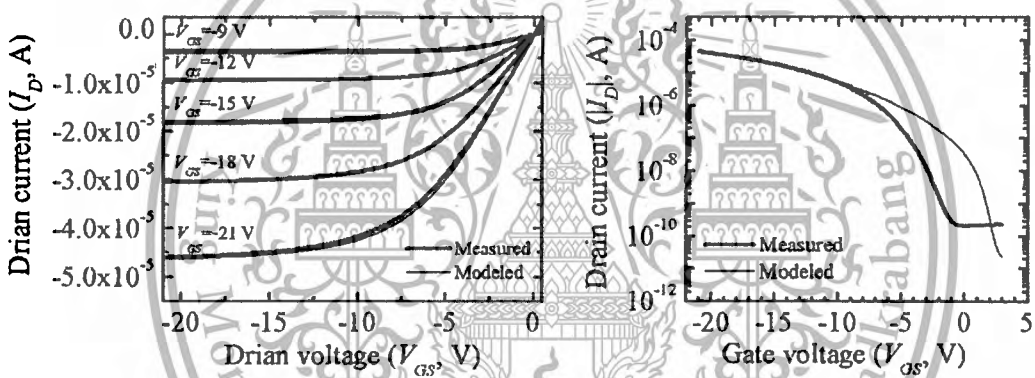

Figure 5.1 Comparison between measured and modeled OTFT (a) output and (b) transfer characteristics. Channel length 18 μm, channel width 2000 μm.

5.2 Inverters

The application of OTFTs in to electronic circuits, such as chemical sensors and E-skin are promising candidates. However, the performances of OTFTs can be used for the application in circuits, as a basic design and simulation for inverters, but they should show good characteristics. In the following experiments, the fabricated OTFTs were proposed as a Diode-connector load, a bootstrapped inverter and a ring oscillator. Normally, inverters have two configurations which can be equipped with OTFTs. A complimentary design can be used [36] if both, n-channel and p-channel are available. But, n-channel OTFTs degrade quickly by interaction with oxygen and moisture in ambient operation. Because of these problems, most organic inverters are developed by p-channel devices [40].

5.2.1 Diode-connected load inverter

The schematic of a diode-connected load inverter circuit is shown in figure 5.2. When the input signal V_{IN} is low ($V_{IN} = V_{DD}$, the lower power rail voltage), Q1 will be turned on and the output V_{OUT} will be high ($V_{OUT} = V_{CC}$), the upper power rail voltage). Q2 will also be turned on when V_{IN} is low (V_{DD}), because Q2 is used as a diode-connected load. For the circuit design, transistor Q1 should therefore have a larger channel *W/L* ratio than Q2 to pull-up V_{OUT} towards the V_{CC} value. On the other hand, when V_{IN} is high (V_{CC}), Q1 will be turned off ($V_{GS} = 0$) and Q2 will be turned on ($V_{GS} = V_{DD}$). Consequently V_{OUT} will be low (V_{DD}).

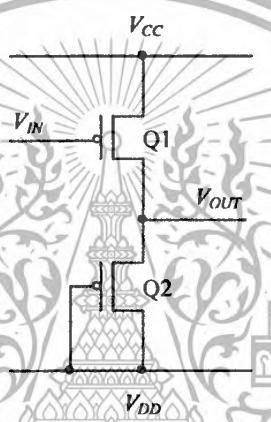

Figure 5.2 Schematic of a diode-connected load inverter circuit.

Figure 5.3 shows the dynamic switching characteristics of the diode-connected load inverter operating at a frequency of 2 kHz; the *W/L* channel ratios of the two transistors were 2000/18 μm for Q1, and 500/18 μm for Q2. The input voltage is shown in the top figure while the graph below reveals the output simulated data. It is evident that the output switching voltage range (15.5V) is significantly less than that of the input (20 V), as predicted by the SPICE simulation. This is because the output swings are determined by the dimensions and the threshold voltage of the OTFTs; in particular, the low output level is determined by the threshold voltage of P2 (-4.5 V).

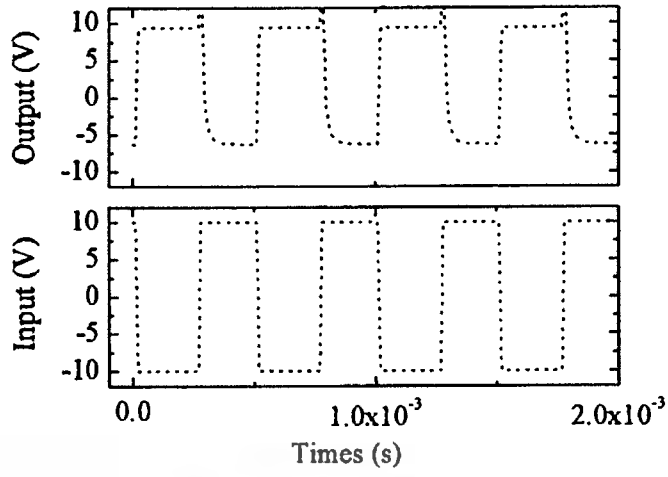

Figure 5.3 Simulated output signals of a diode-connected load inverter. Operating frequency 2 kHz, drive voltage 20 V.

5.2.1.1 A ring oscillator of diode-connected load inverter

This step of validation was the simulation of a ring oscillator at V_{DD}=-10 V and V_{CC}=10 V. Figure 5.4 shows the topology of the circuit made of 9 inverters, a resistor and a capacitor acting as loads. The inverters have the same topology as that simulated previously in figure 5.2, with the same transistor sizes and applied polarizations. The simulation results are shown in figure 5.4. The characteristics of the ring oscillator obtained are the following: V_{oh}=8.5 V, V_{ol}=-1.5 V, rise time 0.3 ms and fall time 0.28 ms. The ring oscillator frequency is 1.7 kHz.

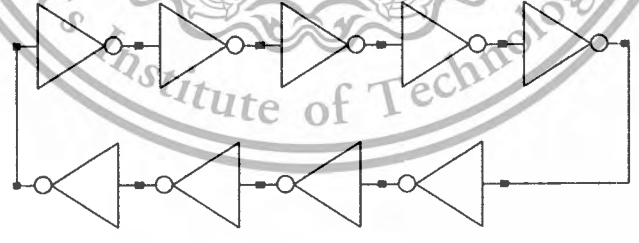

Figure 5.4 A schematic of 9-stage pentacene ring oscillator with diode-connection load invertor.

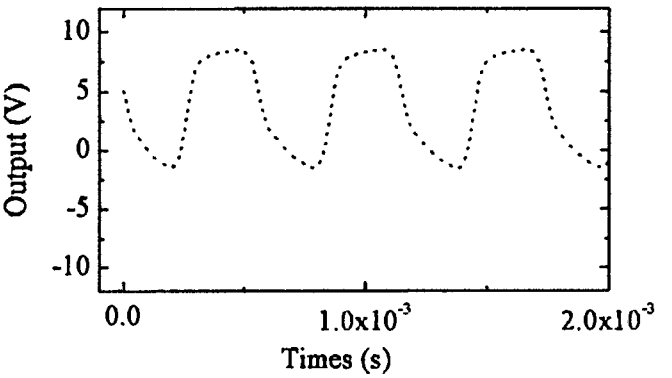

Figure 5.5 Simulated output signals of a 9-stage pentacene ring oscillator with diode-connection load invertor.

5.2.2 Bootstrapped inverter

The schematic of an alternative inverter using capacitive coupling and bootstrapping effects is shown in figure 5.5.

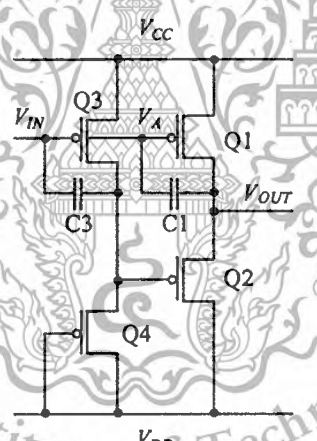

Figure 5.6 The bootstrapped inverter circuit.

The input voltage is applied simultaneously to the gates of Q1 and Q3. The capacitors C1 and C3, indicated by dotted lines in figure 5.5, are gate-drain overlap capacitors of Q1 and Q3, respectively. When V_{IN} is as low as V_{DD}), both Q1 ($V_{GS} = V_{DD}$) and Q3 ($V_{GS} = V_{DD}$) will be turned on. As a result, V_A will become high and Q4 ($V_{GS} = V_{DD}$) will be turned on. In the design, Q4 has a smaller W/L channel ratio than Q3 in order to maintain a high V_A (V_{CC}), Q2 ($V_{GS} = 0$) will be turned off and V_{OUT} will go up and remain high (V_{CC}). When V_{IN} becomes high (V_{CC}), bootstrapping effects will lead to V_{OUT} becoming higher than V_A if Q1 has a wider channel than Q3. In this case, the

capacitance of C1 is higher than C3 because the gate-drain overlap capacitance is proportional to the channel width. Q2 will be turned on and V_{OUT} will go low (V_{DD}) if the difference between V_{OUT} and V_A is greater than the threshold voltage of Q2. This means that the output voltage swings are determined by the V_{CC} and V_{DD} levels. Furthermore, to overcome the high threshold voltage of Q2, Q4 can be used to pull-down V_A. The capacitances C1 and C3 are given by equation (2.6).

Figure 5.6 shows the dynamic switching characteristics of the bootstrapped inverter operating at 2 kHz. As the input voltage is shown in the top figure while the graph below reveals the output simulated data. The *W/L* channel ratios of the OTFTs used in the bootstrapped inverter were: 1000/18 μm for Q1, 100/50 μm for Q2, 100/50 μm for Q3, and 500/100 μm for Q4. The results demonstrate that, as a result of bootstrapping, the difference between V_{OUT} and V_A is greater than the threshold voltage of Q2. This leads to operation that is not restricted by the threshold voltage of the OTFTs. Figure 5.7 compares the simulated difference voltage between nodes V_A and V_{OUT} (V_{GS} of Q2), and the input signal. This demonstrates clearly that, when V_{IN} becomes high, V_{GS} is high enough to switch on the OTFT.

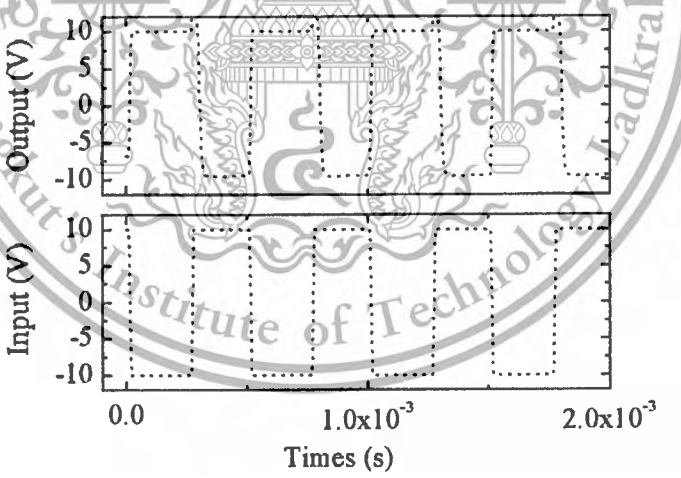

Figure 5.7 Simulated output signals of a bootstrapped inverter.

Operating frequency 2 kHz; drive voltage 20 V higher than the threshold voltage of Q2, as a result of the coupling capacitor.

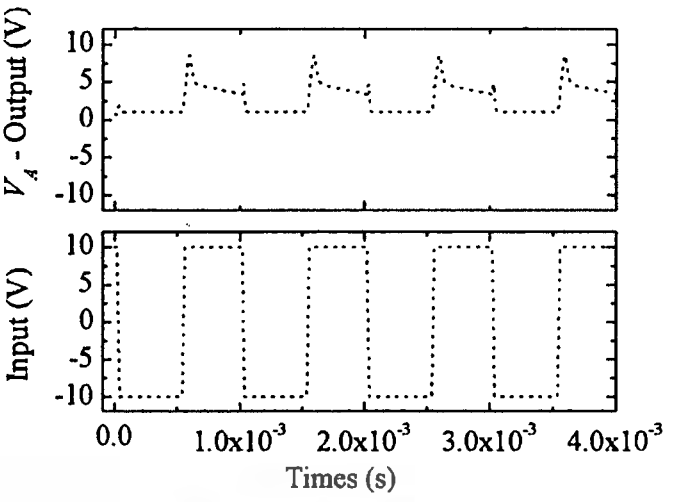

Figure 5.8 The simulated difference voltage between nodes V_A and V_{OUT} compared to the input voltage of a bootstrapped inverter.

Figure 5.8 compares the simulation of the dynamic switching characteristics for both, the diode-connected load inverter (dots) and the bootstrapped inverter (solid line) operating at 2 kHz.

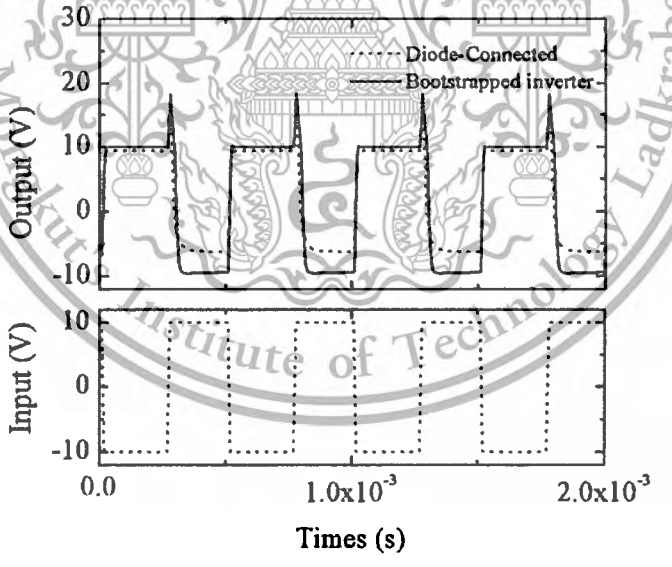

Figure 5.9 Comparison of the simulated dynamic switching characteristics of a diode-connected load inverter (dots) and a bootstrapped inverter (full line). Operating frequency 2 kHz; drive voltage 20 V.

If the rise and fall times are defined as the time required for the output voltage to rise from the -90 % to 90 % level or drop from the 90 % to -90 % level, respectively, then the bootstrapped inverter has a 30 µs rise time and a 450 µs fall time at 2 kHz with

a 20 V driving voltage. The diode-connected load inverter does not reach 90 % of the input voltage range due to the high threshold voltage of the load transistor.

5.2.2.1 A ring oscillator of bootstrapped inverter

This step of validation was the simulation of a ring oscillator at V_{DD} = 10 V and V_{CC} = -10 V. Figure 5.9 shows the topology of the circuit made of 9 inverters, a resistor and a capacitor acting as loads. The inverters have the same topology as the ones simulated previously in figure 5.5, with the same transistor sizes and applied polarizations. The simulation results are shown in figure 5.9. The characteristics of the ring oscillator obtained are the following: V_{oh} 10 V, V_{ol} -9 V, rise time 0.13 ms, and fall time 0.40 ms. The ring oscillator frequency is 1.1 kHz.

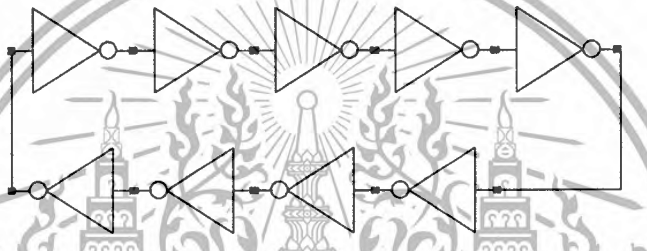

Figure 5.10 A Schematic of 9-stage pentacene ring oscillator with bootstrapped inverters.

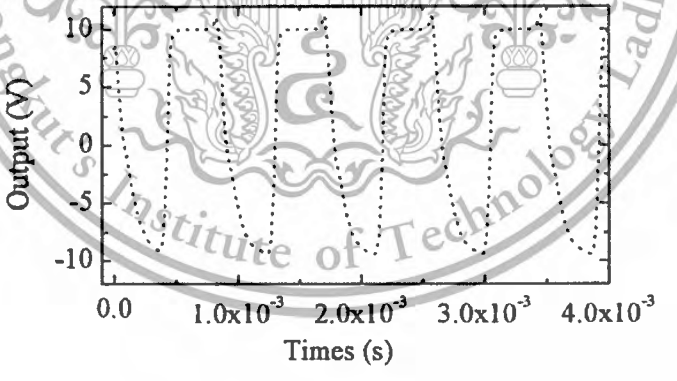

Figure 5.11 Simulated output signals of a 9-stage pentacene ring oscillator with bootstrapped inverters.

Chapter 6
Conclusions

It was found in this study that for the low cost fabrication of OTFTs, based on pentacenes the most important starting point in the fabrication is the shadow mask, which is usually produced in a 3-layer thermal evaporation process and one layer by a spin-coating process.

The process for the dielectric layer has been developed. Several materials, such as PVP, PS and PMMA were tested. Out of the tested materials for the main layer, PMMA was chosen because of its superior performance and behavior in all experiments. Then after finding the optimal material for the dielectric layer, PMMA was tested with different solvents and its effects on the electrical properties of the dielectric layer. Therefore the effect of dimethylformamide (DMF), n-butyl acetate (nBA) and toluene as solvents mixed with PMMA, in order to prepare the ultrathin PMMA dielectric films by spin-coating, was investigated. Several spin speeds were tested. Among all spin speeds experimented, 2000 rpm was found to give minimum thickness fluctuations. Thickness variations according to the applied spin speed and the prepared PMMA solutions, using the three solvents DMF, nBA and toluene with the PMMA concentrations of 2.7, 1.7 and 1.2 wt.%, respectively, were conducted, the received data was then curve fitted. PMMA has to be coated with a distinct thickness in order to minimize leakage currents, maximize the breakdown field, and avoid pin-holes and cracks. In order to achieve this, the needed film thickness is about 100 nm for PMMA. The rms roughness of the PMMA films, prepared by using DMF, nBA and toluene as solvents, were 0.34, 0.36 and 0.43 nm, respectively. A pin hole was observed on the toluene-PMMA film. In the parallel plate capacitor structure, the lowest leakage current density of less than 5×10^{-8} A cm^{-2} for the electric field of up to ~4 MV cm^{-1} was achieved with a 100-nm thick PMMA film prepared by using DMF. Moreover, the PMMA film prepared by using DMF showed the highest relative dielectric constant for the frequency range of 100 Hz to 1 MHz, among all investigated solvents. The dissipation factor dependence on the frequency applied to the PMMA films prepared using DMF and nBA showed similar characteristics. Despite the similar measured values for DMF and nBA, DMF was selected to dissolve PMMA for the fabrication of the PMMA thin-film because of its highly suiting

mechanical and physical properties. After finding the right solvent, a spin-coating method was successfully used to coat the PMMA dielectric thin films with a thickness of 95 nm on glass, PEN and Si substrates. The fluctuation in the capacitance density was found to be resulting from the rough and disordered surfaces. For the PMMA dielectric film on Si wafer substrate, the inhomogeneous distribution of the electric field, the low leakage current and the highly unstable capacitance at high frequencies were caused by the increased surface roughness. PEN and glass substrates gave similar results, except for the surface roughness, which has to be very low to establish a uniform thin film. The lowest roughness was achieved using the glass substrate. The aim of this thesis was to characterize pentacene-based organic electronic devices with a solution processed polymer dielectric. Pentacenes are one of the most promising organic semiconductors because of their high field-effect mobility. For this reason, pentacene was used as the active layer in organic thin-film transistors (OTFTs). PMMA was chosen as the gate dielectric because of its high resistivity and the low dielectric constant, which in fact is similar to that of silicon dioxide, being used normally. Furthermore, it contains hydrophobic methyl radical groups, which are responsible for and encouraging a good ordering of the active organic layer as it is deposited on its surface. Uniform, pinhole-free and crack-free films of PMMA could be obtained by spin coating to the lowest thickness of about 95 nm. The leakage current density was found to be less than 10^{-7} A cm^{-2} for fields up to 2 MV cm^{-1}. These values are small enough to allow the use of a 95 nm PMMA film as the gate dielectric in an OTFT. The dielectric constant of the PMMA was measured to be 3.45 at 1 kHz and 2.89 at 1 MHz.

The semiconductor layer needs a defect-free dielectric layer with a low surface roughness in order to achieve a pentacene active layer with a high-mobility. Pentacenes are deposited in the evaporation process. The conditions during the deposition were found to affect the grain size and the coverage of the silicon substrates by the pentacene films. A low deposition rate of 0.01 nm/s resulted in larger grains but less islands developed, thus in rougher surfaces and a worse coverage. A high deposition rate of 0.05 nm/s, results in a smaller grain size, but a higher number of grains developed on the films surface. In order to achieve the needed grain size combined with a good coverage of the film, a two-step process for the growth was introduced. It uses a deposition rate of 0.05 nm/s for the first monolayer and 0.01 nm/s for the next layer. This was carried out in order to combine

the complimentary effects of the two deposition rates. A smooth first monolayer can be prepared for a better grain growth of the next layers, resulting in an improved overall morphology and electrical performances of the semiconductor in the OTFTs. In an another evaporation process, with a deposition rate of 0.01 nm/s, the pentacene films were deposited on the Au electrodes and the PMMA channel regions, on the pentacene thin film semiconductor, which was preheated to 60 °C. This evaporation process was also carried out in a preheated environment. The OTFTs were investigated using SEM, XRD and PES measurements for their morphology, crystal structure and electronic structure, respectively. Preheating the deposition environment to 80 °C for 10 hours was found to improve the grain coalescence of the pentacene film in the region and thus improve the overall performance of the semiconductor and the OTFTs. The Carrier transport in the pentacene layer was observed to be higher in the channel region than on the Au electrodes. But the pentacene work function on the Au electrodes was found to be higher than on the channel region.

The production of the shadow mask is in general very expensive. The low-cost fabrication of the shadow mask is needed to enable a low cost OTFT fabrication process. The next issue for producing low cost OTFTs is the availability and the price of the photoresist films, which are military material and therefore not easy to purchase. Commercial photoresist films are widely used, but so far only for OTFTs, which are not demanding high-resolution, because only a resolution of 100 μm can be achieved. It was proven in this thesis that commercial photoresist films can be used by decreasing its thinness to 10 μm and using a resist pattern with a high resolution up to 18 μm. The two-step fabrication of the shadow mask is a special technique to support the fabrication of the OTFT with the 18 μm technology.

The produced and optimized OTFTs incorporating a 95 nm layer of PMMA gave the following results: The leakage currents could be reduced significantly by the thickness of the used PMMA layer. The scaling effects of the produced OTFT characteristics with respect to the channel length and width were found to correspond with the simple thin film transistor theory. The on/off current ratio, field-effect mobility, threshold voltage, and subthreshold slope for an optimized device were measured to be 0.16 $cm^2 V^{-1} s^{-1}$, -3.5 V and 1.5 V per decade, respectively.

However, on glass substrate a better electrical performance, and on PEN substrate a better flexibility of the OTFT itself, was achieved. Because of its ability to

work under deformation, it can be used in applications needing a higher flexibility, such as display.

The produced OTFTs were, according to the results from the modeling by the UHEM method then applied to circuits. The OTFTs were applied to inverters, Diod-load connectors and Bootstrapped inverters. The developed Diod-load connectors and Bootstrapped inverters were further introduced to ring oscillators. The inverters showed voltage amplification at moderate biases. For the simple 9-stage ring oscillator switching frequencies of a few kHz have been achieved.

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Appendices

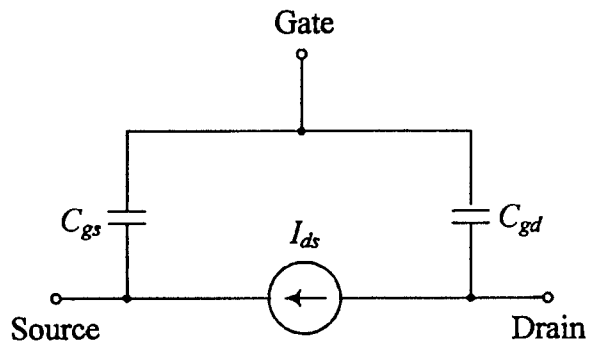
A. SPICE simulation

A. 1 Amorphous silicon (a-Si) thin-film transistor (TFT) model (an AIM-SPICE MOS15) is level 61 in the Hspice models

Name	Unit	Default	Description
ALPHASAT	-	0.6	Saturation modulation parameter
CGDO	F/m	0	Gate-drain overlap capacitance per meter channel width
CGSO	F/m	0	Gate-source overlap capacitance per meter channel width
DEF0	eV	0.6	Dark Fermi level position
DELTA	-	5	Transition width parameter
EL	eV	0.35	Activation energy of the hole leakage current
EMU	eV	0.06	Field effect mobility activation energy
EPS	-	11	Relative dielectric constant of substrate
EPSI	-	7.4	Relative dielectric constant of gate insulator
GAMMA	-	0.4	Power law mobility parameter
GMIN	$m^{-3}eV^{-1}$	1E23	Minimum density of deep states
IOL	A	3.00E-14	Zero bias leakage current parameter
KASAT	1/ȯC	0.006	Temperature coefficient of ALPHASAT

KVT	V/ȯC	-0.036	Threshold voltage temperature coefficient
LAMBDA	1/V	0.0008	Output conductance parameter
M	-	2.5	Knee shape parameter
MUBAND	m^2/Vs	0.001	Conduction band mobility
RD	m	0	Drain resistance
RS	m	0	Source resistance
SIGMA0	A	1.00E-14	Minimum leakage current parameter
TNOM	ȯC	25	Parameter measurement temperature
TOX	m	1.00E-07	Thin-oxide thickness
V0	V	0.12	Characteristic voltage for deep states
VAA	V	7.50E+03	Characteristic voltage for field effect mobility
VDSL	V	7	Hole leakage current drain voltage parameter
VFB	V	-3	Flat band voltage
VGSL	V	7	Hole leakage current gate voltage parameter
VMIN	V	0.3	Convergence parameter

Equivalent Circuit



Model Equations

Drain current

$$I_{DS} = I_{leakage} + I_{ab}$$

$$I_{ab} = g_{ch} V_{dse} (1 + LAMDA \bullet V_{ds})$$

$$V_{dse} = \frac{V_{ds}}{\left[1 + (V_{ds}/V_{sate})^{M}\right]^{1/M}}$$

$$V_{sate} = \alpha_{sat} V_{gte}$$

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}(RS + RD)}$$

$$g_{chi} = q n_s W \bullet MUBAND / L$$

$$n_s = \frac{n_{sa} n_{sb}}{n_{sa} + n_{sb}}$$

$$n_{sa} = \frac{EPSI \bullet V_{gte}}{q \bullet TOX} \left(\frac{V_{gte}}{V_{aat}}\right)^{GAMMA}$$

$$n_{sb} = n_{so} \left(\frac{t_m}{TOX} \frac{V_{gfbe}}{V0} \frac{EPSI}{EPS}\right)^{\frac{2 \bullet V0}{V_e}}$$

$$n_{so} = N_c t_m \frac{V_e}{V0} \exp\left(-\frac{DEF0}{V_{th}}\right)$$

$$N_c = 3.0 \bullet 10^{25} m^{-3}$$

$$V_e = \frac{2 \bullet V0 \bullet V_{tho}}{2 \bullet V0 - V_{th}}$$

$$t_m = \sqrt{\frac{EFS}{2q \bullet GMIN}}$$

$$V_{gte} = \frac{VMIN}{2}\left[1 + \frac{V_{gt}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gt}}{VMIN} - 1\right)^2}\right]$$

$$V_{gt} = V_{gs} - V_T$$

$$V_{gte} = \frac{VMIN}{2}\left[1 + \frac{V_{gfb}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gfb}}{VMIN} - 1\right)^2}\right]$$

$$V_{gfb} = V_{gs} - VFB$$

$$I_{leakage} = I_{hl} + I_{\min}$$

$$I_{hl} = IOL\left[\exp\left(\frac{V_{ds}}{VDSL}\right) - 1\right]\exp\left(-\frac{V_{gs}}{VGSL}\right)\exp\left[\frac{EL}{q}\left(\frac{1}{V_{tho}} - \frac{1}{V_{th}}\right)\right]$$

$$I_{\min} = SIGMA0 \bullet V_{ds}$$

Temperature Dependence

$$V_{tho} = k_B \bullet TNOM / q$$

$$V_{th} = k_B \bullet (TEMP) / q$$

$$V_{aat} = VAA\exp\left[\frac{EMU}{q \bullet GAMMA}\left(\frac{1}{V_{th}} - \frac{1}{V_{tho}}\right)\right]$$

$$V_T = VTO + KVT(TEMP - TNOM)$$

$$\alpha_{sat} = ALPHASAT + KASAT(TEMP - TNOM)$$

Capacitance

$$C_{gs} = C_f + \frac{2}{3}C_{gs}\left[1 - \left(\frac{V_{sate} - V_{dse}}{2V_{sate} - V_{dse}}\right)^2\right]$$

$$C_{gd} = C_f + \frac{2}{3}C_{gc}\left[1 - \left(\frac{V_{sate}}{2V_{sate} - V_{dse}}\right)^2\right]$$

$$C_f = 0.5 \bullet EPS \bullet W$$

$$C_{gs} = q\frac{dn_{sc}}{dV_{gs}}$$

$$n_{sc} = \frac{n_{sac}n_{sbc}}{n_{sac} + n_{sbc}}$$

$$n_{sbc} = n_{sb}$$

A. 2 SPICE code

A. 2.1 Device modeling

Modeling : Operation regions of a PMOS OTFT

```
.MODEL otft pmos Level=61
+ alphasat = 0.26    cgdo = 0.0      cgso = 0.0      def0 = 0.6
+ delta = 5.0        el = 0.35       emu = 0.06      eps = 11
+ epsi = 3.5         gamma = 1.62    gmin = 1e23     iol = 3e-14
+ kasat = 0.006      kvt = -0.036    lambda = 5e-6   m = 2.8
+ muband = 0.001     rd = 10e-3      rs = 10e-3      sima0 = 1e-14
+ tnom = 27          tox = 95e-9     v0 = 0.12       vaa = 520
+ vdsl = 7           vfb = -3 vgs    l = 7           vmin = 0.3
+ vto = -4.5
```

A 2.2 Diode-connected load inverter

```
OTFTs : Inverter test
.protect
.inc 'd:\ model61_OTFT.md'
.unprotect

m1    4    1    2    4    otft    w=2000u    l=18u
m2    2    3    3    2    otft    w=200u     l=18u
vcc   4    0    dc   10
Vss   3    0    dc   -10

vin   1    0    dc   0    ac    PULSE (10 -10 20uS 20uS 20uS 1mS
2mS)
.dc   vin  10   -10  -100m
*.tran  0.005m    2m
*.probe      par('V(2)')
.print  v(2) V(1)
.end
```

A.2.3 ring oscillator of diode-connected load inverter

```
OTFTs A ring oscillator of diode-connected load inverter test
.protect
.inc 'd:\ model61_OTFT.md '
.unprotect

m1    4    1    2    4    otft    w=2000u    l=18u
m2    2    3    3    2    otft    w=200u     l=18u
m12   4    2    22   4    otft    w=2000u    l=18u
m22   22   3    3    22   otft    w=200u     l=18u
m13   4    22   23   4    otft    w=2000u    l=18u
m23   23   3    3    23   otft    w=200u     l=18u
m14   4    23   24   4    otft    w=2000u    l=18u
m24   24   3    3    24   otft    w=200u     l=18u
m15   4    24   25   4    otft    w=2000u    l=18u
m25   25   3    3    25   otft    w=200u     l=18u
m16   4    25   26   4    otft    w=2000u    l=18u
m26   26   3    3    26   otft    w=200u     l=18u
m17   4    26   27   4    otft    w=2000u    l=18u
m27   27   3    3    27   otft    w=200u     l=18u
m18   4    27   28   4    otft    w=2000u    l=18u
m28   28   3    3    28   otft    w=200u     l=18u
m19   4    28   1    4    otft    w=2000u    l=18u
m29   1    3    3    1    otft    w=200u     l=18u

vcc   4    0    dc   10
Vss   3    0    dc   -10

.IC V(1)=4
.tran   0.01m  4m
.probe  par('V(2)')
.print  v(2) V(1)
.end
```

2.4 Bootstrapped inverter

```
OTFTs : Bootstrapped inverter test
.protect
.inc 'd:\mek\work\Supstrate_effect\model61.md'
.unprotect

m3    4    1    5    4    otft    w=500u    l=18u
m4    5    3    3    5    otft    w=100u    l=18u
m1    4    1    2    4    otft    w=1000u   l=18u
m2    2    5    3    2    otft    w=500u    l=18u

vcc   4    0    dc   10
Vss   3    0    dc   -10
vin   1    0    dc   0    ac   PULSE (10 -10 20uS 20uS 20uS 1mS
2mS)
.tran 0.005m     2m
.probe par('V(2)')
.print v(2) V(1) v(5)
.end
```

A. 2.5 A ring oscillator of bootstrapped inverter

OTFTs : Ring oscillator of bootstrapped inverter test

.protect

.inc 'd:\model61_OTFT.md'

.unprotect

m3	4	1	5	4	otft	w=500u	l=18u
m4	5	3	3	5	otft	w=100u	l=18u
m1	4	1	2	4	otft	w=1000u	l=18u
m2	2	5	3	2	otft	w=500u	l=18u
m31	4	2	51	4	otft	w=500u	l=18u
m41	51	3	3	51	otft	w=100u	l=18u
m11	4	2	21	4	otft	w=1000u	l=18u
m21	21	51	3	21	otft	w=500u	l=18u
m32	4	21	52	4	otft	w=500u	l=18u
m42	52	3	3	52	otft	w=100u	l=18u
m12	4	21	22	4	otft	w=1000u	l=18u
m22	22	52	3	22	otft	w=500u	l=18u
m33	4	22	53	4	otft	w=500u	l=18u
m43	53	3	3	53	otft	w=100u	l=18u
m13	4	22	23	4	otft	w=1000u	l=18u
m23	23	53	3	23	otft	w=500u	l=18u
m34	4	23	54	4	otft	w=500u	l=18u
m44	54	3	3	54	otft	w=100u	l=18u
m14	4	23	24	4	otft	w=1000u	l=18u
m24	24	54	3	24	otft	w=500u	l=18u

```
m35   4    24   55   4    otft   w=500u    l=18u
m45   55   3    3    55   otft   w=100u    l=18u
m15   4    24   25   4    otft   w=1000u   l=18u
m25   25   55   3    25   otft   w=500u    l=18u

m36   4    25   56   4    otft   w=500u    l=18u
m46   56   3    3    56   otft   w=100u    l=18u
m16   4    25   26   4    otft   w=1000u   l=18u
m26   26   56   3    56   otft   w=500u    l=18u

m37   4    26   57   4    otft   w=500u    l=18u
m47   57   3    3    57   otft   w=100u    l=18u
m17   4    26   27   4    otft   w=1000u   l=18u
m27   27   57   3    27   otft   w=500u    l=18u

m38   4    27   58   4    otft   w=500u    l=18u
m48   58   3    3    58   otft   w=100u    l=18u
m18   4    27   1    4    otft   w=1000u   l=18u
m28   1    58   3    1    otft   w=500u    l=18u

vcc   4    0    dc   10
Vss   3    0    dc   -10

.IC V(1)=4
.tran   0.01m  4m
.probe  par('V(2)')
```

B Publications

1. T. Tippo, C. Thanachayanont, P. Muthitamongkol, C. Junin, M. Hietschold, A. Thanachayanont "The effects of solvents on the properties of ultra-thin poly (methyl methacrylate) films prepared by spin coating" Thin Solid Films, In press (2013)
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B. 1 The effects of solvents on the properties of ultra-thin poly (methyl methacrylate) films prepared by spin coating

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The effects of solvents on the properties of ultra-thin poly (methyl methacrylate) films prepared by spin coating

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ARTICLE INFO

Available online xxxx

Keywords:
Ultrathin film
PMMA
DMF
Leakage current
Breakdown electric field
Dielectric constant
Dissipation factor

ABSTRACT

Poly (methyl methacrylate) (PMMA) is extensively used as an insulating layer in organic electronic devices. In this study, spin coating method was used to cast thin layers of PMMA for dielectric application from solutions in three different solvents, namely dimethylformamide (DMF), n-butyl acetate and toluene. The solvent's vapor pressure causes the solvent to vaporize at different rates leading to layer's distortion and different surface roughnesses. Preparation of suitable surface morphologies, for example, pinhole-free and crack-free was studied. A step profilometer was used to measure the film thicknesses. Alternatively an equation correlating final film thickness to spin speed and solution concentration was proposed. A metal/insulator/metal parallel plate capacitor structure was fabricated and the current density dependence on the applied electric field was measured. The resulting low surface roughness, low leakage currents, high breakdown voltage, and high dielectric constant were obtained for the 100 nm-thick PMMA film prepared with DMF.

1. Introduction

Poly (methyl methacrylate) (PMMA) is a thermoplastic polymer containing hydrophobic methyl radical groups, which can play a role as a moisture inhibitor, as well as encourage good ordering of the active organic over layer as it is deposited on the surface with high resistivity of 2×10^{15} Ω/cm, similar to that of silicon dioxide [1]. In electronic device applications, PMMA was used as an insulating layer in photolithography and organic thin film transistors (OTFTs). For example, PMMA acted as a positive resist for electron and ultraviolet photolithography, as an imprintable material for hot-embossing soft lithography and as a matrix for nonlinear optical composite materials because of its excellent transparency in the visible spectrum and as a good dielectric layer in OTFTs.

Effect of solvent dissolution on mechanical and physical properties of PMMA casted film has been extensively studied by many researchers while solvent effect on electrical properties of PMMA is rarely reported. Influence of solvent on mechanical and physical properties of PMMA was also shown in the literature reviews. For examples, Briscoe et al. [2] investigated the stiffness and hardness of PMMA films cast from chloroform, toluene, and carbon tetrachloride, finding lower values for the latter solvent. Patra et al. [3] investigated the thermal, mechanical, and structural properties of PMMA samples cast from solutions of chloroform, toluene, and dimethylformamide (DMF). Hydrogen bonding was found to be responsible for an increased glass transition temperature when prepared using DMF and toluene. Zhou et al. [4] found that the strong interaction between PMMA and acetone resulted in the formation of porous particles while the weak interaction between tetrahydrofuran and PMMA produced honeycomb structure particles. Semaltianos [5] spin coated PMMA films using chlorobenzene and found formation of surface pinholes and large-sized circular pits. Noh et al. [6] demonstrated that the 100 nm-thick PMMA films could be prepared using n-butyl acetate (nBA) for top-gate polymer field-effect transistors. The best root-mean-square roughness values of nBA and toluene are 0.52 and 0.32 nm, respectively [7]. From the previous reports mentioned above, the type of solvent selected plays an important role on uniformity and thickness of the PMMA films. A solvent with a lower vaporizability results in a better uniformity and a lower thickness. Therefore, the solvent should be selected on the basis of the desirable thickness and uniformity [8–10]. DMF, nBA, and toluene are promising candidates as suitable solvents that this study chooses to prepare PMMA ultrathin film. Furthermore, effect of PMMA dissolution by selected solvent is still also investigated along with PMMA thin film fabrication by spin coating. For thin film fabrication by spin coating, many parameters occur during the spin process such as spin speed, spin time including dissolution of PMMA in various selected solvents which are related to concentration, viscosity, and solvent evaporation which are optimized to give good film quality such as good thickness and surface roughness. For electrical property, in order to increase

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http://dx.doi.org/10.1016/j.tsf.2013.05.022

Please cite this article as: T. Tippo, et al., Thin Solid Films (2013), http://dx.doi.org/10.1016/j.tsf.2013.05.022

insulator capacitance to achieve the lowest leakage current corresponding to the highest breakdown strength, the film thickness must be minimized without the presence of pinholes, pits, or any other types of defects. In electronic applications, when a semiconductor thin film is deposited on the dielectric layer, a low surface roughness is also crucial in order to achieve reliability and stability of threshold voltages and other related electrical properties [11].

The aim of the present study is to investigate the influence of spin speed and concentration of PMMA dissolved in selected solvent, DMF, nBA, and toluene, on the film thickness, surface roughness, surface morphology, and the electrical property on of PMMA thin films spin-cast.

2. Experimental details

2.1. Material and device preparation

PMMA having an average molecular weight of ~996,000 as measured by gel permeation chromatography was purchased from Sigma-Aldrich. Analytical reagent grade DMF, nBA, and toluene were purchased from LAB-Scan Analytical Sciences.

Glass substrates were cleaned with a soft brush in detergent and dried with a nitrogen gas, then cleaned again with piranha solution at 60 °C for 1 h, then rinsed with deionized water and finally dried with the nitrogen jet.

A metal/insulator/metal (MIM) parallel plate capacitor structure was fabricated step by step on 2 cm × 2 cm cleaned glass substrates following below procedure. Firstly, bottom-metal aluminum electrodes were fabricated by a thermal evaporator through a metallic mask on glass substrate. For an insulating layer, PMMA was dissolved in each solvent, DMF, nBA, and toluene. The samples were spun in nitrogen glove-box on the patterned aluminum on glass substrate for 180 s at a spin speed of 2000 rpm. Films were allowed to dry in an argon atmosphere for 1 h at 60 °C, then for another 1 h at 120 °C in order to remove residual solvents and to anneal the polymer films. The last step for MIM parallel capacitor is thermal evaporation of aluminum metal again on an insulating layer to obtain parallel plate capacitor structure for further characterization.

2.2. Characterization

For accuracy and reliable result, each characterization of the sample was conducted on 3 positions on the sample with 3 samples to analyze and average data values. The thickness measurement was measured using a step profilometer (Dektak 8000). Surface roughness of the polymer layer was scanned using tapping mode (Dynamic force mode) using a SPA400 atomic force microscope made by Seiko Instruments. Etched silicon tips were used with resonant frequency of 140 kHz and force constant of 3.5 N/m. Roughness measurements were calculated using SPIWin version 4.08F from scan sizes of 3 μm × 3 μm. The leakage current versus the electric field for the 100 nm-thick PMMA layers of the MIM parallel plate capacitor structure was measured by using a high-accuracy current–voltage measurement (Keithley 2612). A DC voltage, sweeping from 0 V to 40 V, is applied across the electrodes and the corresponding currents are measured. The data were analyzed according to ASTM D3755. Dielectric constant versus frequency and loss factor were measured by using an impedance analyzer (Agilent 4294a) with a fixed 10-mV AC voltage.

3. Results and discussions

To investigate the effect of spin speed on the thickness of PMMA, the solutions having 3 wt.% PMMA in DMF, nBA, and toluene were coated at different spin speeds. The thickness of each sample was then measured and plotted versus spin speed as shown in Fig. 1a. At all spin speeds, DMF resulted in the lowest thicknesses among the three solvents

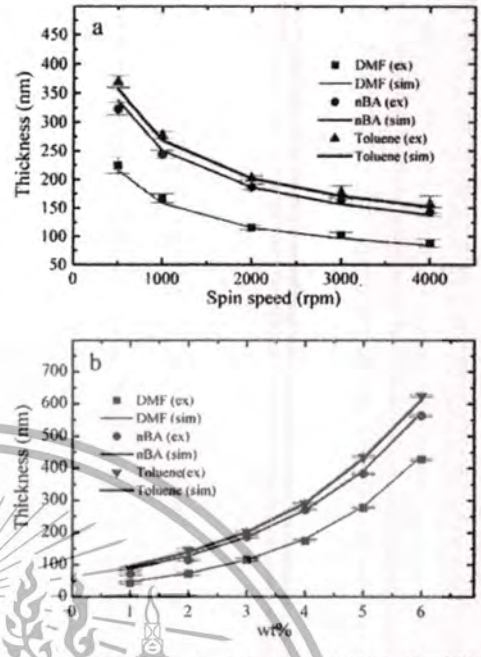

Fig. 1. (a) Thickness of PMMA films as a function of spin speed at 3 wt.% and (b) thickness of spin-coated PMMA films as a function of PMMA concentration in DMF, nBA, and toluene at a spin speed of 2000 rpm (where "ex" and "sim" represent experimental and simulation results, respectively).

used. This suggests that DMF enables uniform extended and interconnected PMMA chain network [2]. Moreover, hydrogen bonding in the PMMA chains formed by replacement of the methoxy groups of PMMA by amide groups of DMF is proposed to be responsible for the superior performance of the DMF over other solvents used to prepare PMMA [3]. Among all spin speeds experimented, 2000 rpm was found to give the least thickness fluctuation. Increasing the spin speed over 4000 rpm decreases the thickness further, however significant thickness fluctuation occurs at different locations of the samples as shown by the deviation in Fig. 1a. Although sub-100 nm-thick PMMA films are desirable in nanoelectronics, as published elsewhere [1,5], data obtained beyond 4000 rpm were not reliably recorded to draw a conclusion on their behavior. Keeping the spin speed at 2000 rpm, the PMMA thicknesses were plotted against concentration of PMMA in DMF, nBA and toluene as shown in Fig. 1b. The thicknesses of 100 nm were obtained using DMF, nBA and toluene at the projected PMMA concentrations of 2.7, 1.7 and 1.2 wt.%, respectively.

To find an optimal condition to achieve the desirable thickness (of around 100 nm to minimize leakage current, maximize breakdown field, and avoid pin-holes and cracks), simulation of the film thickness variation with concentration and spin speed was conducted and found to fit well with experimental results (shown as lines in Fig. 1a and b). Apart from concentration and spin speed, for example, rate of evaporation, substrate surface energy, viscosity, and polymer molecular weight are known to affect the thickness of the spin-coated PMMA films. Lima and de Andrade [12] proposed that thickness h depended on the concentration of the PMMA solution, c, and spin speed, ω, as indicated in Eq. (1):

$$h = Ac\omega^{-\alpha} \quad (1)$$

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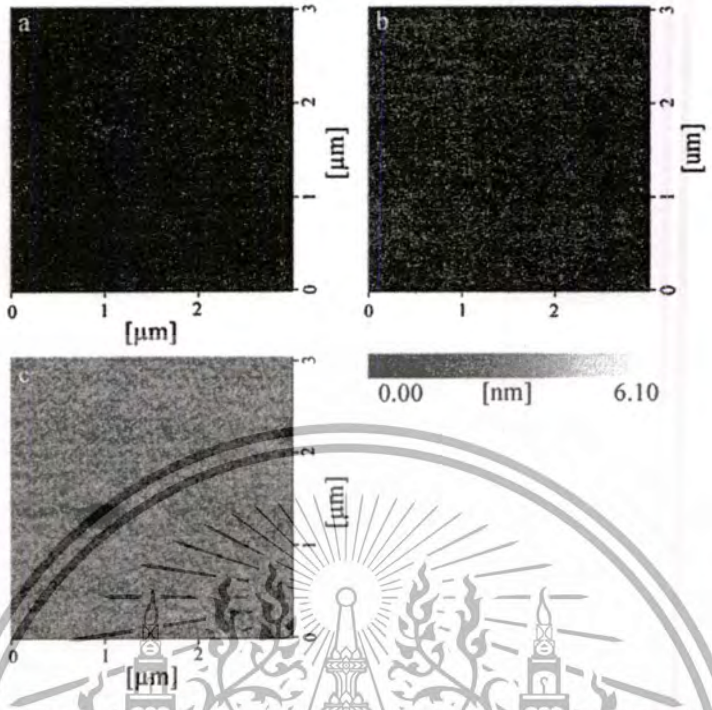

Fig. 2. AFM images of the 100 nm-thick spin-coated PMMA films prepared using (a) DMF, (b) nBA and (c) Toluene with the concentrations of 2.7, 1.7 and 1.2 wt.% respectively.

where the other parameters affecting thickness result in different constants A and α. Walsh et al. [9] proposed a different equation relating the thickness of the PMMA film to c and ω, as shown in Eq. (2).

$$h = Ac^{n}\omega^{-\alpha} \quad (2)$$

where the exponent n is the concentration dependent system specific parameter, which is generally larger than 1. Fitting the results obtained using Eqs. (1) and (2) did not match the experimental results in Fig. 1. However, if the concentration is explained by e^{nc} in Eq. (3), the experimental curves can be well fitted, shown as lines in Fig. 1, see Eq. (3).

$$h = Ae^{nc}\omega^{-\alpha} \quad (3)$$

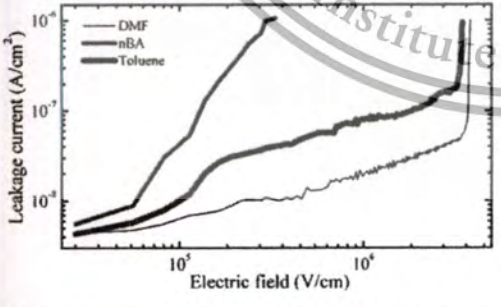

Fig. 3. Leakage current density vs. electric field applied to a MIM parallel plate capacitor structure with the 100 nm thick PMMA films prepared using DMF, nBA, and toluene with the concentrations of 2.7, 1.7, and 1.2 wt.%, respectively.

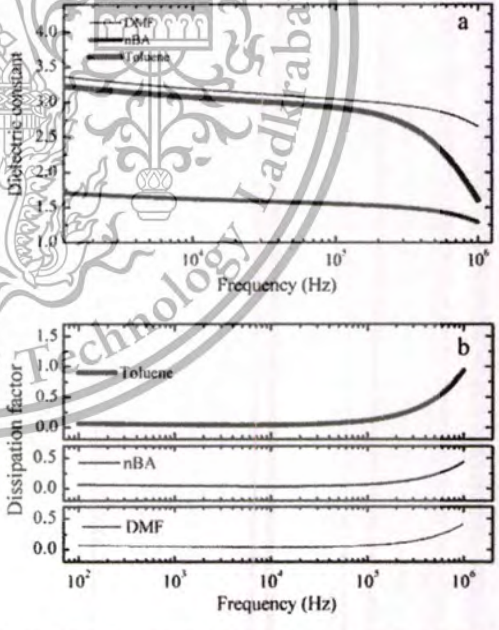

Fig. 4. (a) Relative dielectric constant of material vs. frequency and (b) dissipation factor vs. frequency of the 100 nm-thick PMMA dielectric films prepared using DMF, nBA, and toluene.

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Table 1
Comparisons of the electrical properties of insulating layer material.

Materials	Solvent	Thickness (nm)	Leakage current (A cm^{-2}) at 1 MV cm^{-1}	C_i (nF cm^{-2}) at 1 kHz	Roughness rms (nm)	Substrate	Ref.
PMMA	DMF	100	2×10^{-8}	30	0.34	Glass	This work
PMMA	Anisole	150	5×10^{-8}	21	0.30	Glass	[1]
PMMA	nBA	100	$\sim 10^{-2}$	-	-	Glass	[6]
C-PMMA	nBA	100	10^{-6}	-	-	Glass	[6]
PMMA	Toluene	560	-	5.6	0.32	Glass	[7]
PS	Toluene	133	$\sim 10^{-6}$	19	2	Si	[13]
PVP	THF	122	$\sim 10^{-5}$	42	6	Si	[13]
PVP	PGMEA	200	10^{-8}	-	-	Glass	[14]

Eqs. (4)–(6) show the fitted details for DMF, nBA and toluene, respectively.

$$h = 951.79e^{0.445c}\omega^{-0.453} \quad (4)$$

$$h = 1586.26e^{0.375c}\omega^{-0.430} \quad (5)$$

$$h = 1502.12e^{0.370c}\omega^{-0.410} \quad (6)$$

The surface morphology was investigated and shown in Fig. 2. Uniform and pinhole-free PMMA films were obtained using DMF and nBA as shown in Fig. 2a and b. However, a pin-hole was observed in a random scanned area of the PMMA film prepared using toluene as shown in Fig. 2c. Surface root-mean-square roughnesses of the three samples, prepared using DMF, nBA and toluene, were 0.34, 0.36 and 0.43 nm, respectively.

In the MIM parallel plate capacitor structure having an area of 9 mm^2, Fig. 3 shows that for the DMF-prepared PMMA, the leakage current density is less than 5×10^{-8} A cm^{-2} for the electric field of up to ~4 MV cm^{-1}. The leakage currents were found to be higher for the toluene-prepared PMMA than the DMF-prepared PMMA with similar breakdown electric field. nBA-prepared PMMA showed the highest leakage current densities with a breakdown at a very low electric field.

Fig. 4a and b shows the respective dependence of relative dielectric constant (ε_r) and dissipation factor on the frequency of the applied field, for the different solvents used to prepare the PMMA thin films. The relative dielectric constants were calculated from the measured insulator capacitances of the MIM parallel plate capacitors, using Eq. (7):

$$\varepsilon_r = C_i/C_0 = \varepsilon_r\varepsilon_0 A/dC_0 \quad (7)$$

where C_0 is the capacitance measured with vacuum between its plates, C_i is the insulator capacitance, ε_r is the relative dielectric constant, A is the area of the capacitor and d is the distance between plates. The relative dielectric constant of the DMF-prepared PMMA as a function of frequency (100 Hz to 1 MHz) was found to be the highest among all the solvents used for the whole range of frequency applied, followed by the relative dielectric constants of toluene-prepared PMMA and nBA-prepared PMMA, respectively.

An ideal capacitor should only store and release electrical energy without dissipation. In reality, all capacitors have imperfections within the capacitor's materials that create resistance. Dissipation factor (loss tangent or tan δ), D, is the ratio of the loss index to its relative dielectric constant, which can be calculated from Eq. (8), where k" is the magnitude of the imaginary part of the relative complex dielectric constant and k' is the real part of the relative complex dielectric constant. The dissipation factor, however, can be measured directly using the impedance analyzer.

$$D = k''/k' \quad (8)$$

Ions under low-frequency electric field can hop readily out of sites with low free-energy barriers but tend to 'pile up' at sites with high free-energy barriers. This leads to a net polarization of the dipoles and a large value of relative dielectric constant. At higher frequencies, the polarization due to charge 'pile-up' disappears and so relative dielectric constant decreases [10].

Table 1 compares PMMA film thicknesses, leakage currents, insulator capacitances, rms roughness, and the substrates from the good values obtained in this study and previously reported values by others. It is clearly shown that the lowest leakage current could be obtained using DMF as the solvent to prepare PMMA dielectric film.

4. Conclusion

In this study, the effect of using DMF, nBA, and toluene as solvents to prepare spin-coated ultrathin PMMA dielectric films was investigated. Among all spin speeds experimented, 2000 rpm was found to give the least thickness fluctuation. Curve-fitting of thickness variation with spin speed and concentration of the PMMA prepared using the three solvents was conducted. In order to achieve PMMA film thicknesses of 100 nm (in order to minimize leakage current, maximize breakdown field, and avoid pin-holes and cracks), DMF, nBA, and toluene with the PMMA concentrations of 2.7, 1.7 and 1.2 wt.% were prepared, respectively. The root-mean-square roughnesses of the PMMA films, prepared using DMF, nBA and toluene, were 0.34, 0.36 and 0.43 nm, respectively. A pinhole was only observed in the toluene-prepared PMMA film.

In the MIM parallel plate capacitor structure, the lowest leakage current density of less than 5×10^{-8} A cm^{-2} for the electric field of up to ~4 MV cm^{-1} was achieved with the 100-nm thick PMMA film prepared using DMF. Moreover, the PMMA film prepared using DMF showed the highest relative dielectric constant among all solvents investigated in the frequency range of 100 Hz to 1 MHz. Dissipation factor dependence on the frequency of the PMMA films prepared using DMF and nBA showed similar characteristics.

Acknowledgment

The authors would like to acknowledge the Thailand Research Fund through the Royal Golden Jubilee with its Ph.D. Program (grant No. PHD/0190/2547) for the scholarship throughout the thesis, the DeutscherAkademischerAustauschDienst (German Academic Exchange service) (DAAD) (grant No. D/08/04908) for scholarship to conduct the experiments in Germany and the National Metal and Materials Technology Center (MTEC), the National Science and Technology Development Agency (NSTDA), for the research financial support (Project MT-B-52-CER-07-240-I).

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Please cite this article as: T. Tippo, et al., Thin Solid Films (2013), http://dx.doi.org/10.1016/j.tsf.2013.05.022

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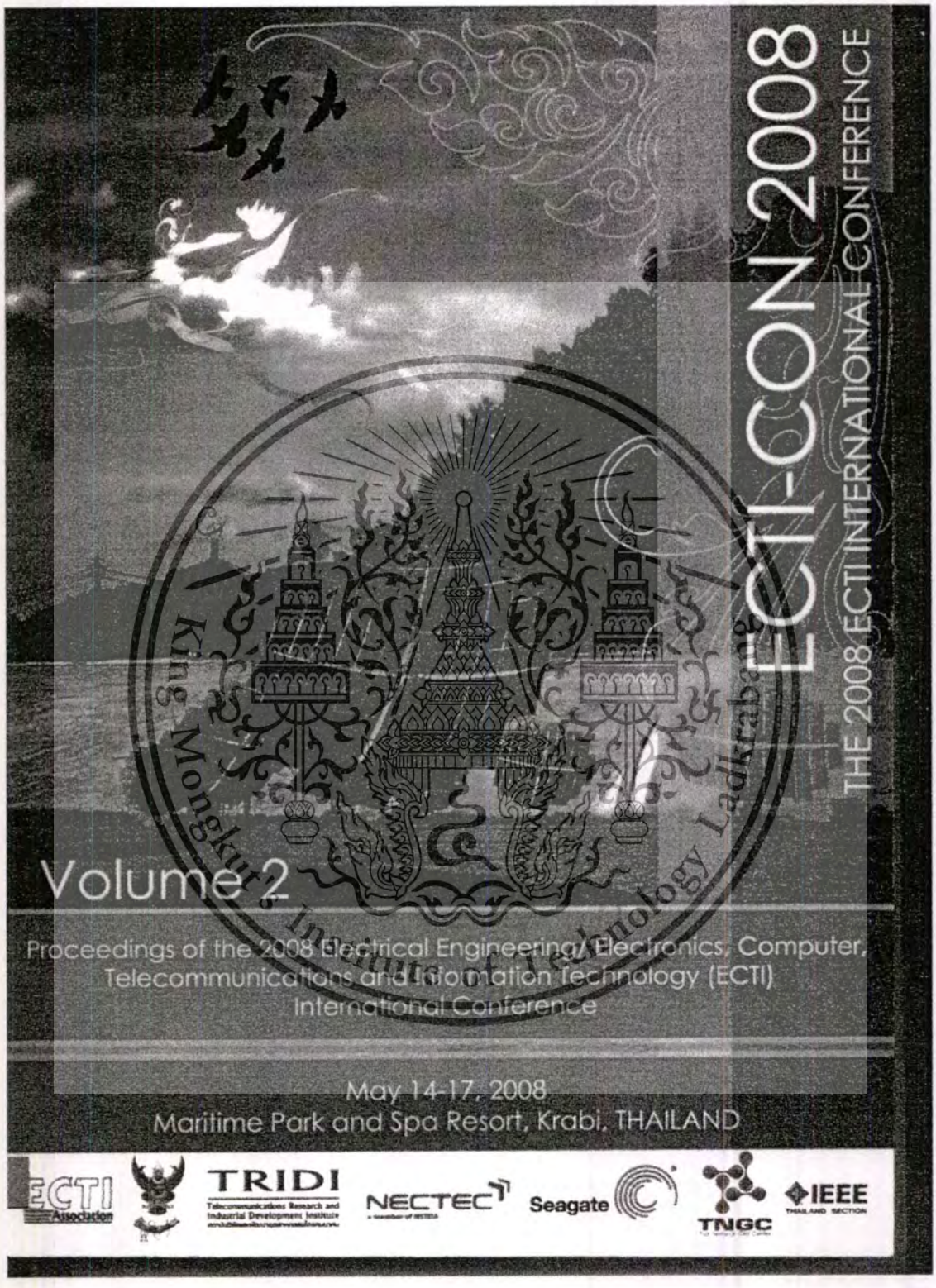
B. 2 Fabrication and Modeling of Organic Thin-Film Transistor on Glass



Proceedings of ECTI-CON 2008

Fabrication and Modeling of Organic Thin-Film Transistor on Glass Substrate

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***Abstract*-Organic thin film transistors have been fabricated using pentacene as an active material. Aluminium gate electrodes, pentacene active layers and gold source-drain contacts were fabricated on glass substrate using thermal evaporation though metallic mask. Gate dielectric layers were processed by solution-process spin-coating. The fabricated transistor exhibited the maximum carrier mobility of 0.01 cm^2/V-s and the on/off current current ratio over 400.**

I. Introduction

For the past two decades, organic thin-film transistors (OTFTs) based on conjugated polymers have been investigated for low cost, large-area and flexible application [1-4]. Among all conjugated polymers used for active layers in OTFTs, pentacene has been reported for mobility as high as 1.5 cm^2/V-s [5]. Pentacene is air-stable, commercially available and inexpensive [2] and it has been the most popular material for p-channel OTFTs [6]. For fabrication of OTFTs, simple and cost effective, solution-processing gate dielectrics have been used where achievable performance is close to those of inorganic gate dielectric materials [7].

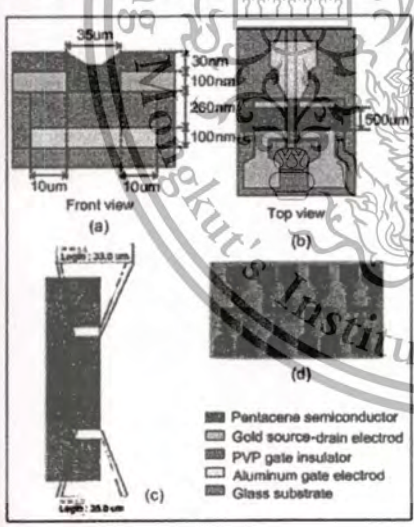

Figure1. Schematic front view (a) top view (b) and real top view (c), of the OTFT. (d) Four OTFTs on glass substrate.

This paper reports investigation and experimental results on fabrication and modeling of pentacene OTFTs on glass substrate. Pentacene, used as p-channel active layer, was deposited using thermal evaporation in vacuum and patterned by manually aligned matalic mask. Poly-4-Vinylphenol (PVP) was used as dielectric material and deposited by spin-coating.

II. Organic Thin-Film Trasistors

An OTFT is essentially similar to a typical Field-Effect Transistor, in which a voltage, V_G, applied to a gate electrode controls current between source and drain electrodes under imposed bias voltages. In a conventional inorganic FET, the active semiconductor layer is typically lightly-doped Si, where the applied voltage causes accumulation of minority charge carrier at the dielectric interface, e.g. electrons in p-type material, termed an 'inversion layer'. In this channel, carrier injection from source to drain electrodes may occur under imposed bias voltages, resulting in a current flow. In an organic transistor, the active layer is a thin film conjugated small molecule pentacene. In contrast to inorganic materials, organic materials pass current by majority carriers, and inversion regime does not exist. This fundamental difference results in much lower surface mobility values of OTFTs compared with those of single-crystalline inorganic semiconductor FETs. Therefore OTFTs are not suitable for applications, which demand high speed operation. However, due to the processing characteristics, OTFTs are competitive for large area, physical flexibility, low speed and low cost applications, such as large area, bendable displays.

Performance of OTFTs are usually reported in terms of mobility values and on/off current ratio, which determine the speed and leakage current of devices. Typical surface mobility values of OTFTs can range from 0.1-2 cm^2/V-s, which are comparable with those of amorphous-Si (a-Si) devices. Typical on/off current ratio ranges from 10^3-10^8

III. Fabrication of Devices

Figure 1 shows a cross-section bottom-contact OTFT structure used in this work. Glass substrate was cleaned by 70% hydrochloric and 30% hydrogen per oxide. A 100-nm thick gate aluminum film was deposited though a metallic mask by thermal evaporation. A 260 Poly-4-(vinylphenol) PVP (40 mg/mL in Propylene Glycol Aonomethyl ether Acetate (PGMA)) was mixed with the poly (melamine-co-formadehyde) methylated (40% V/V in PGMA) in a 1:1 volume ratio and spin coated onto substrates at 2000, 2500,

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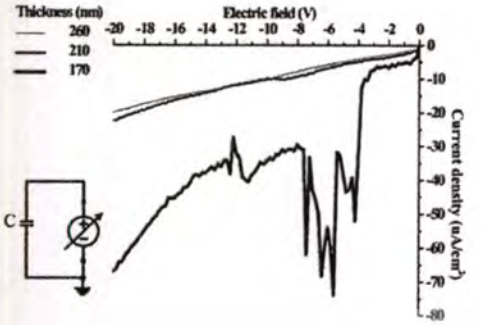

Figure2. Electrical capacitor leakage current of PVP dielectric layers having thicknesses of 170, 210 and 260 nm respectively. The inset shows parallel plate capacitor circuit diagram used to measure leakage current

3000 rpm revolutions per minute (rpm). Cross-linking was allowed for 5 minutes at 500 °C to make the film robust. Dektak surface profiler was used to measure the dielectric layer thicknesses which were found to be 260, 210 and 170 nm thick for spin speeds of 2000, 2500, 3000 rpm used to prepare the dielectric film, respectively.

A smooth gate dielectric promotes molecular ordering in active layer, leading to improved charge transport and carrier mobility. The polymer blend was spin coated at 2000 rpm on glass substrate and cured for 1 minute at 100 °C appeared the smoothest among the three dielectric films investigated. For OTFTs presented in the current investigation, the gate dielectric layer was fabricated using a spin speed of 2000 rpm.

The dielectric characteristics of the dielectric films were evaluated via quantitative leakage current and capacitance measurements. Typical current density-electric field (J-E) plots for parallel-plate capacitor fabricated with 260 nm thick PVP dielectric layer, demonstrates a leakage current density of 1-5×10^{-7} A/cm^2. Electric field across the film is up to 8x10^6 V/cm (i.e. 20 V of applied voltage). A permittivity value of the thin-film capacitor is measured to be 3.5 at 100 kHz. PVP films of good electrical uniformity over 4 cm^2 can be deposited on glass using the current experimental procedure.

Thermal evaporation was then used to deposit 100-nm thick gold source and drain electrodes via metallic masks. The thickness of the pentacene film is controlled at 20 nm with a deposition rate of 3 nm/s. The pressure was held below 5×10^{-6} Mbar during the active layer deposition. A high degree of molecular ordering in active organic material necessary for high-mobility devices requires careful control of film deposition condition [8]-[9]. Figure 1 (c) shows that the minimum geometrical resolution of 35-μm can be achieved. The patterned metallic masks were fabricated using photolithography technique and electroplating process. The transistors were fabricated with channel-length (L) 35 μm and channel-width (W) 500 μm. Gate-source and gate-drain overlap distance were measured to be 10 μm.

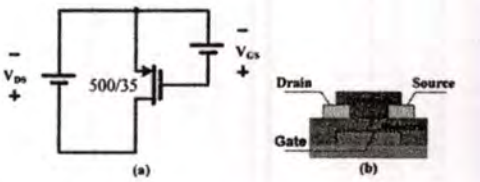

Figure 3 (a) Circuit diagram used to measure I_{DS}-V_{DS} and I_{DS}-V_{GS} (b) OTFT test configuration.

TABLE I

EXPERIMENT MEASUREMENT SETTING OTFT DEVICE

Measurement Type	V_{DS} Start	V_{DS} stop	V_{DS} Step	V_{DS} Bias	V_{GS} start	V_{GS} stop	V_{GS} Step
I_{DS} VS. V_{DS}	-2	-20	-0.2	-	-2	-20	-2
I_{DS} VS. V_{GS} #1	-	-	-	-4	-2	-20	-0.2
I_{DS} VS. V_{GS} #2	-	-	-	-20	-2	-20	-0.2

IV. MODELING AND PARAMETER EXTRACTION

A good modeling and parameter extraction method is critical to determine accurate devices parameters required for accurate simulation of semiconductor devices, circuits and systems. According to the measured input and output characteristics of OTFTs, it has been observed that mobility usually increases with gate voltage.

It has also been reported that mobility increase with V_{DS} in a more pronounced way than that of a-Si:H devices with similar geometry [13], [14]. This increase of mobility with V_{DS} is related to carrier hopping [15], a Frenkel-Pool type effect associated to traps in material [16], and the lowering of the emission barrier in traps located at the boundaries between grains in polycrystalline materials used to fabricate OTFTs [17], [18]. OTFTs can present deformation at origin of the output characteristics, due to non-ohmic contacts at drain and source [19]-[21]. They can also have leakage current across the gate dielectric [22] and/or polarization effect [23], which can be significant and must be taken into account. Estrada et al. applied the unified model and parameter extraction method (UHEM) to a-Si:H [24], to nano-crystalline silicon transistors [25] and recently to OTFTs [26]. Advantages of this method are that all above threshold parameters are extracted from two transfer characteristics, one in the linear and other in saturation region and from output characteristic of the device under study, using a single mathematical processing involving an integral method that reduces experimental noise. Device parameters are extracted in a simple and direct way from experimental results. This method uses analytical expressions for both modeling and parameter extraction. The drain-source current can be expressed as shown in (1),

TABLE II

COMPARISONS BETWEEN EXTRACTED AND CURVE-FITTED PARAMETERS

Parameter	Extracted	Curve-fitted
V_T [V]	-0.05	-0.05
γ_a	1.00	1.00
V_{aa} [V]	8.00×10^{5}	2.00×10^{4}
μ_{FET0} [cm^2/V.s]	1.01×10^{-5}	4.05×10^{-5}
R [kΩ]	13.00×10^{3}	13.00×10^{3}
α_s	0.90	0.90
M	1.70	1.60
λ [1/V]	-8.04×10^{-4}	-8.04×10^{-4}

where W is channel width, L is channel length, C_{diel} is gate capacitance, R is source plus drain resistance, I_0 is leakage current and m and λ are fitting parameters related to sharpness of knee region and the channel length modulation, respectively. Channel-length modulation factor, λ, describes the variation of the drain-source conductance with V_{DS} in the saturation regime.

$$I_{DS} = C_{diel}\frac{\mu_{FET}(V_{GS}-V_T)}{1+R.\frac{W}{L}.C_{diel}.\mu_{FET}.(V_{GS}-V_T)}\times\frac{V_{DS}(1+\lambda\cdot V_{DS})}{\left[1+\left[\frac{V_{DS}}{V_{DSsat}}\right]^m\right]^{1/m}}+I_0 \quad (1)$$

The mobility dependence with the gate-source voltage [21] is described as given by (2), where μ_{FET0} is the mobility for low perpendicular and longitudinal electric fields, V_T the threshold voltage and γ_a and V_{aa} are curve-fitting parameters. μ_0 is the mobility for the material of the TFT under analysis. Since this parameter is usually estimated, the fitting parameter γ_a is used to adjust μ_{FET0} to experimental values of low-field mobility. Parameter V_{aa} is related to conduction mechanism and can describe both an increase and decrease in mobility with V_{GS}. In OTFTs, both behaviors have been observed.

$$\mu_{FET} = \mu_0\left[\frac{(V_{GS}-V_T)}{V_{aa}}\right]^{\gamma_a} = \mu_{FET0}\cdot(V_{GS}-V_T)^{\gamma_a} \quad (2)$$

The saturation voltage is defined through the saturation modulation parameter α_s :

$$V_{DSsat} = \alpha_s(V_{GS}-V_T) \quad (3)$$

For extraction procedure in the above-threshold regime, the integral function $H(V)$ is defined as in (4).

$$H(V_{GS}) = \frac{\int_0^{V_{GS}} I_{DS}dx}{I_{DS}(V_{GS})} \quad (4)$$

Substituting (2) in (1) and calculating $H(V_{GS})$ from (4), the following expression is obtained for the above-threshold regime, as given by (5).

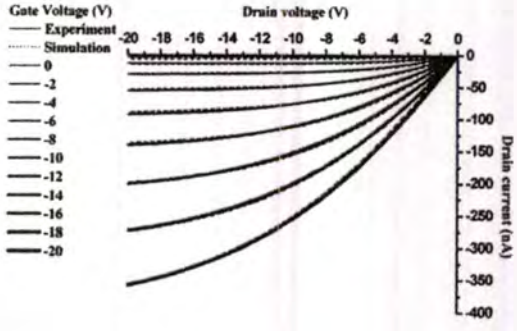

Figure4. Measured and simulated I_d-V_{ds} characteristics of OTFT.

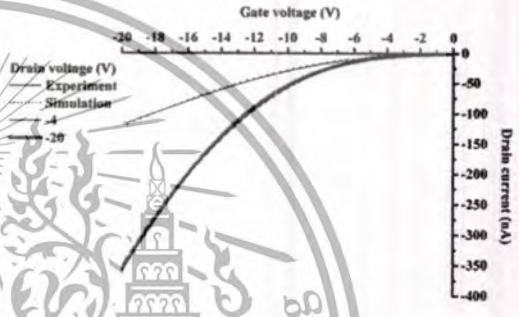

Figure 5. Measured and simulated Id-V_{GS} of OTFT.

$$H_a(V_{DS}) = \frac{1}{2+\gamma_a}(V_{GS}-V_T) \quad (5)$$

The generalized parameter extraction procedure for different devices and operation regions can be found in [24], [25]. The steps for the determination of model parameters V_T, γ_a, α_s, V_{aa}, M and λ are extracted.

V. MEASURED RESULTS

Several OTFTs in Fig. 1 were fabricated and its electrical characteristics were measured by using a source measure unit (Keithley 2616) following 1620™ IEEE standard test methods for the characterization of organic transistors and material and summarized in Table I. The gate and drain voltages were independently varied from 0 to -20 V to obtain the i-v characteristics of OTFT. The maximum drain current is about 358 nA, while the off current was measured at 0.86 nA with zero gate voltage and 20 V drain voltage. This yields an on/off current ratio of 416. Figures 4 and 5 show the measured and simulated I_d-V_{ds} and I_d-V_{gs} of the OTFTs, respectively. Simulated curves were obtained by using the model in (1) with curve-fitted parameters as summarized in Table II. Comparing with the extracted parameters, also in

Table I, V_{ss} and M had to be adjusted to best fit the measured *I-V* curves.

As mentioned earlier in section III, figure 2, leakage current though gate dielectric is highly dependent on the dielectric layer thickness and roughness. The reduction of mobility in OTFT is caused by dielectric roughness due to the disorder in accumulation layer. Roughness disturbs π-π stretching, which is critical to efficient charge transport. Roughness of the dielectric layer can be modified, e.g., by varying ratio of PVP and spin coating conditions.

It should be also noted that the experiments were conducted in ambient atmosphere and the pentacene was used as received whrere purification of the pentacene may have improved the performance of OTFT fabricated. It is known that impurities in the pentcene layer may result in charge trapping sites which lower the average mobility and degrades the OTFT on current. Moreover, the impurities can function as dopants, thereby increasing the conductivity of the film in the off or ungated state, which result in large leak currents, excessive power dissipation, and low on-to-off current ratios. Stability of the OTFTs is also known to be profoundly affected by impurities, chemical sensibility and microstructure films. As thermal vacuum deposition is used in the present investigation, controlling deposition rate and pressure is directly related to the morphologies obtained. All the parameters mentioned above are being taken in to consideration of our current work to improve the performance of the OTFTs fabricated.

VI. Conclusions

We have successfully fabricated OTFT on glass substrate using low cost processing. Transistors were patterned by manual alignment via metallic masks with the minimum geometrical resolution of 35 μm. Parameter extraction was successfully obtained with good accuracy. Design and fabrication of organic electronic circuits are under investigation and will be reported in the future.

Acknowledgment

The financial support from the Thailand Research Fund through the Royal Golden Jubilee Ph.D. Program (grant No. PHD/0190/2547) is acknowledged.

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B. 3 A comparative investigation of a pentacene layer on gold and PMMA in bottom-contact pentacene thin film transistors

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doi: 10.4028/www.scientific.net/AMR.802

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Advanced Materials Research Vol. 802 (2013) pp 27-31
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doi:10.4028/www.scientific.net/AMR.802.27

A Comparative Investigation of a Pentacene Layer on Gold and PMMA in Bottom-Contact Pentacene Thin Film Transistors

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Keywords: Semiconductor, Organic electronic

Abstract. This study demonstrates an attempt to fabricate the 25 μm channel-length bottom-contact pentacene TFTs using thermal evaporation through shadow mask technique and to investigate crystal structure, morphology and electronic structure of the pentacene layer deposited at the same time on gold (Au) source-drain electrodes and Poly(methyl methacrylate) (PMMA) gate-dielectric of the TFTs. The pentacene layers with thicknesses of 50 nm were deposited at the evaporation rates of 0.1, 0.5, 1.0 and 1.5 nm/min at substrate temperatures of 60 °C. These conditions were employed with and without preheating at 80 °C before deposition. Preheating at 80 °C was found to improve quality of the pentacene film on the PMMA gate-dielectric. Using the deposition rate of 1 nm/min and the substrate temperature of 60 °C, best performance of TFTs were obtained. At this deposition condition, pentacene film work function was found to be higher on the Au source-drain electrodes than on the PMMA gate-dielectric.

Introduction

Pentacene ($C_{22}H_{14}$) thin film transistors (TFTs) have been extensively investigated due to their promising low-cost, large-area fabrication on flexible substrates. Although the best performances of top-contact single crystal pentacene TFTs in the literature are impressive [1], the most practical and commonly used device geometry is bottom-contact with top source-drain electrodes for polycrystalline pentacene because this geometry is similar to the silicon TFTs where photolithographic fine patterning can be achieved with minimum exposure of the active semiconductor to chemicals. The largest mobility reported for sub-micrometer size polycrystalline pentacene TFTs is 0.3 $cm^2/V.s$ [2].

In the operation of the pentacene TFTs, charge injection between metal source-drain electrodes and the pentacene and charge transport along interface between gate-dielectric and the pentacene are the most important processes. Although a few studies of pentacene-metal and pentacene-dielectric interfaces have been performed [3-5], they are limited to ideal surfaces and not directly applicable to fabricated devices.

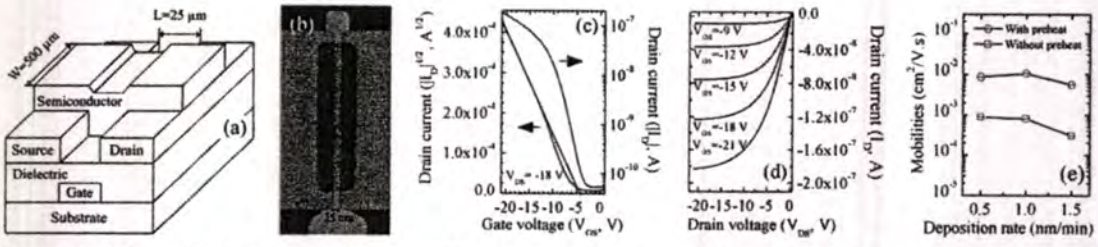

Figure 1 Schematic drawings showing (a) cross-sectional view, (b) optical micrograph showing the channel of the pentacene TFTs, (c) I_D-V_{GS} and $I_D^{1/2}$-V_{GS} characteristics, (d) I_D-V_{DS} characteristics of the TFTs fabricated using preheating at 80 °C for 10 h, at a substrate temperature of 60 °C and a deposition rate of 1 nm/min. (e) Plot of field-effect mobility versus deposition rate for the TFTs.

Gold (Au) is the most commonly used source-drain electrodes material for the pentacene TFTs because its work function of 5.1 eV matches quite well with the ionization energy of pentacene of 4.9 eV [6]. To enable future high-throughput low-cost fabrication of the pentacene TFTs, this study demonstrates our attempt to fabricate bottom-contact pentacene TFTs using evaporation technique and correlate crystal structure, morphology and electronic structure of the pentacene layer deposited at the same time on the Au source-drain electrodes and Poly(methyl methacrylate) (PMMA) gate-dielectric of the TFTs.

Experimental

Figs. 1(a-b), respectively, show a cross-sectional view and an optical micrograph of the channel of bottom-contact pentacene TFTs in this study. The TFT structure consists of channel length and width of 25 and 500 μm, respectively. A 50 nm-thick Aluminum (Al) gate electrodes and Au source-drain electrodes were deposited by thermal evaporation through shadow masks. As-received pentacene from Sigma-Aldrich (99.9% purity, average Mw ~996,000) was used without further purification. By thermal evaporation through shadow mask, the pentacene films with thicknesses of 50 nm were deposited at the evaporation rates of 0.1, 0.5, 1.0 and 1.5 nm/min and substrate temperature of 60 °C, under a base pressure of 5×10^{-6} mbar, with and without preheating at 80 °C for 10 hours before deposition. Spin coated PMMA film gate-dielectric layers were prepared from a 5 wt.% solution in n-buthyl acetate using spin speed of 2000 rpm for 3 min. The annealed PMMA films having an area of 9 mm^2 showed capacitance density of 9.94 nF/cm^2 and leakage current density of 10^{-8} A/cm^2 at an electric field of 5 MV/cm. For the TFT fabrication, a 390 nm-thick PMMA gate-dielectric layer was spin coated onto the Al gate-electrode layer on the glass substrate, followed by the Au source-drain electrodes layer and final with pentacene semiconductor layer.

Grazing-incidence X-ray diffraction (GI-XRD) (RigakuTTRAXIII(GI-XRD) (RigakuTTRAXIII, CuKα radiation with grazing incidence geometry 0.4°, 50 kV, 300 mA, step angle 0.01°, scan speed 2°/min, and 2θ = 4°-16°) and variable-pressure SEM (NovaNanoSEM™) were used to determine crystal structure and morphology of the pentacene films, respectively. The GI-XRD data was analyzed by Jade 9 software, yielding a good Pearson fitting result for the profiles of thin film and bulk phases. Image analysis software (Image-Pro® Plus 5.0) was used to analyze the SEM images to estimate coverage percentages and average grain sizes. Electronic structure of the pentacene films was performed at the photoemission spectroscopy (PES) beamline, BL3.2a, of the Synchrotron Light Research Institute of Thailand. The PES system is equipped with a Thermo VG Scientific CLAM2 electron spectrometer. All experiment data of pentacene films were analyzed on Au source-drain electrodes or gate-dielectric (in channel region) of the TFTs structure.

Finally, the bottom-gate pentacene TFTs were fabricated and the electrical characterization was performed using a source measure unit (Keithley 2616) and related 1620™ IEEE standard test methods for the organic transistors. The gate and drain voltages were independently varied from 3 to -21 V to obtain the I-V characteristics of the TFTs.

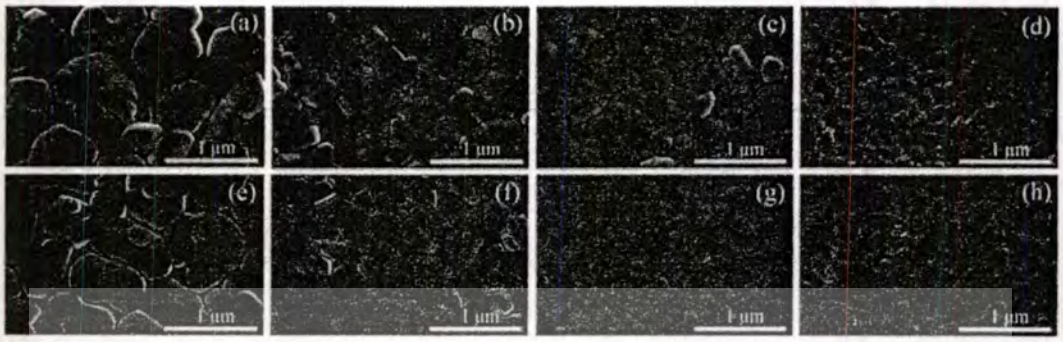

Figure 2 Top-view scanning electron micrographs showing pentacene films deposited on PMMA gate-dielectric at substrate temperature of 60 °C and deposition rates of 0.1, 0.5, 1.0, 1.5 nm/min (a, b, c, d) with preheating and (e, f, g, h) without preheating respectively.

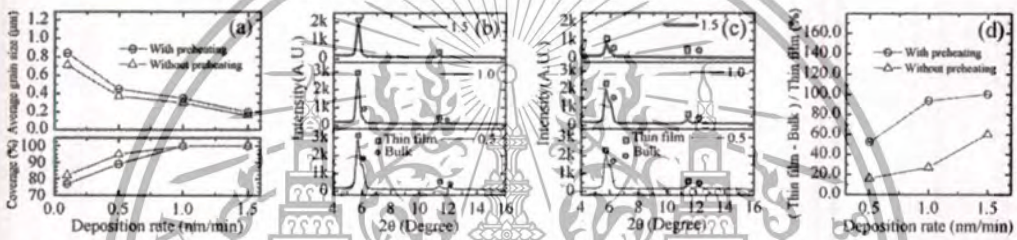

Figure 3 Plots of (a) average grain size and coverage percentage versus deposition rate. GRI-XRD patterns of pentacene films prepared with deposition rates of 0.5, 1.0, and 1.5 nm/min (b) with preheating and (c) without preheating respectively. (d) The percentage delta ratio of intensity of first order diffraction peak of bulk phase relative to thin film phase is showed as a function of deposition rate.

Results and Discussion

Fig. 2 shows SEM micrographs of the pentacene films on PMMA gate-dielectric (Pentacene-PMMA). Preheating at 80 °C for 10 hours was found to increase the average grain sizes for all deposition rates where 100% grain coalescence with maximizing grain size could be achieved at deposition rates of 1.0 nm/min, see Fig. 3(a). A mixture of bulk and thin film phases in the pentacene films was indicated by GI-XRD results as shown in Fig. 3(b and c). The d(001)-spacings of the thin film phase and the bulk phase are, respectively, 1.51 and 1.42 nm, respectively. Fig. 4(d) shows that preheating increases thin film phase formation at all deposition rates. Preheating facilitating early stage deposition of the pentacene is proposed to be a more effective thermal treatment technique to improve the crystal and electronic structure of the pentacene.

Figs. 1(c and d) show I_D-V_{GS} and $I_D^{1/2}$-V_{GS} characteristics and I_D-V_{DS} characteristics of the pentacene TFTs fabricated using preheating at 80 °C for 10 hours, at the substrate temperature of 60 °C and the deposition rate of 1 nm/min. Among all deposition rates experimented, the best field-effect mobility was obtained from the deposition rate of 1 nm/min [Fig. 1(e)]. On-off ratio of 3×10^3 and threshold voltage of -4.2 V were obtained from the best pentacene TFT.

In the actual TFT structure [see Fig. 1], due to different surface energies [7, 8] and morphologies of pentacene film on Au source-drain electrodes (Pentacene-Au) and Pentacene-PMMA, pentacene layer deposited shows different morphologies as shown in Fig. 6(a-c). Although the effect of gate-dielectric surface energy on morphology of the pentacene has been reported [8,9], it is interesting to observe a remarkable change in morphology of the Pentacene-Au compared to the Pentacene-PMMA.

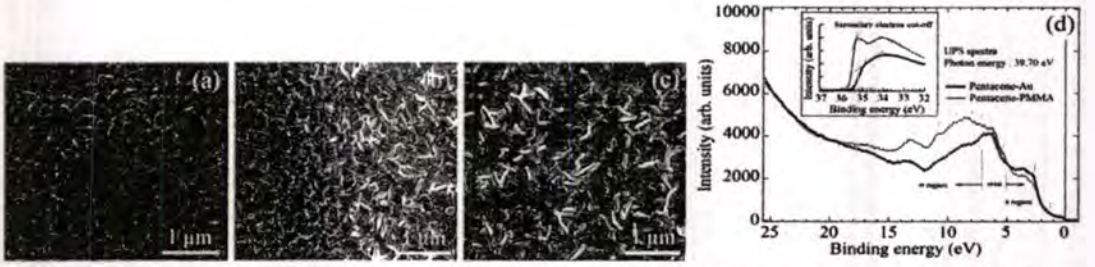

Figure 4 SEM micrographs showing pentacene film deposited at substrate temperature of 60 °C and deposition rate of 1.0 nm/min with preheating on the (a) PMMA gate-dielectric, (b) PMMA gate-dielectric and Au source-drain electrode interface, (c) Au source drain electrodes, and (d) PES spectra taken from pentacene film deposited at substrate temperature of 60 °C and deposition rate of 1.0 nm/min with preheating.

The charging effect observed on the Pentacene-Au indicates less electron mobility than in the Pentacene-PMMA. Higher electron mobility of Pentacene-PMMA is desirable for good carrier transport there. Moreover, electron charging is observed at grain boundaries of Pentacene-PMMA [Fig. 4(a)] and, hence, can be used as a qualitative technique to indirectly observe electron transport in the pentacene layer.

PES using synchrotron light with photon energy of 39.70 eV was used to determine work function and position of the highest occupied molecular orbital or valence band states of the pentacene layers on different regions. The PES spectra of Pentacene-Au and Pentacene-PMMA are shown in Fig. 4(d). The peak assignment (dashed lines) of the valence band structure of 51.2 nm pentacene on Au(111) taken from Ref. 10 is also shown in Fig. 4(d). The PES spectra taken from our 50 nm pentacene layers are in fair agreement with the data published as indicated by the dashed lines in the figure. It was found that the σ features in the Pentacene-PMMA sample evolute in comparison with those in the Pentacene-Au. In comparison with the previous data, the predominant π feature that normally appears at 4.4 eV is weak on both spectra. These indicate that the pentacene molecules on the PMMA gate-dielectric are rather oriented nearly perpendicular to the surface than those on the Au source-drain electrode region. This might result from rather flat pentacence film available on preheated PMMA gate-dielectric than that on Au source-drain electrodes as show in Fig. 4(a-c). The inset of Fig. 4(d) shows the secondary electron cut-off of PES spectra taken from the Pentacene-Au and Pentacene-PMMA samples. The cut-off energy was used for determining the work function. The work function of Pentacene-PMMA (4.19 eV) is found to be about 0.31 eV smaller than that in Pentacene-Au (4.50 eV). The work function of Pentacene-Au is in good agreement with the previously reported data on Pentacene-Au(111) (4.52 eV) [9]. Although, the pentacene grain orientation on Au source-drain electrodes are not the same as the pentacene grains on PMMA gate-dielectric [see Fig. 4], the PES results show that the higher pentacene work function over Au ensures a good charge injection between the Au source-drain electrodes and the pentacene [10].

Summary

Pentacene films deposited on Au source-drain and PMMA gate-dielectric in the pentacene TFTs were investigated using SEM, XRD and PES for their morphology, crystal structure and electronic structure, respectively. Preheating at 80 °C for 10 hours was found to improve grain coalescence with maximize grain size of the pentacene in the channel region and improve the overall performance of the pentacene TFTs. Using a deposition rate of 1 nm/min and a substrate temperature of 60 °C, on-off ratio of 3×10^3 and threshold voltage of -4.2 V were obtained. Carrier transport in the pentacene layer was observed to be higher on the PMMA gate-dielectric than on the Au source-drain electrodes. Pentacene work function was found to be higher on the Au source-drain electrodes than on the PMMA gate-dielectric.

Acknowledgment

The authors would like to acknowledge the Thailand Research Fund through the Royal Golden Jubilee with its Ph.D. Program (grant No.PHD/0190/2547) for the scholarship throughout the thesis, the DeutscherAkademischerAustauschdienst (German Academic Exchange service) (DAAD) (grant No.D/08/04908) for scholarship to conduct the experiments in Germany, the National Metal and Materials Technology Center (MTEC), the National Science and Technology Development Agency (NSTDA), for the research financial support (Project MT-B-52-CER-07-240-I). In addition, this work was also supported by the Higher Education Research Promotion and National Research University Project of Thailand, Office of the Higher Education Commission (CU56-FW12). Mr. Narin Jantaping is much appreciated for his kind assistance with the XRD investigation.

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B. 4 Effect of substrates on preparation of dissolved PMMA in DMF solution used as a dielectric layer in OTFTs

Main Theme: Advances in Material Science and Technology

Volume 802
doi: 10.4028/www.scientific.net/AMR.802

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Advanced Materials Research Vol. 802 (2013) pp 79-83
© (2013) Trans Tech Publications, Switzerland
doi:10.4028/www.scientific.net/AMR.802.79

Effect of substrates on preparation of dissolved PMMA in DMF solution used as a dielectric layer in OTFTs

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Keywords: Organic thin-film transistor, spin-coating, thin-film dielectric

Abstract. Dissolved Poly (methyl methacrylate) (PMMA) in Dimethylformamide solution was fabricated as thin films on different substrates, glass, poly (ethylene naphthalate) and Si wafer, using spin coating technique. The effect of different substrates on electrical performances of the PMMA films was investigated. For an acceptable organic thin-film transistor (OTFT) performance, uniform thickness with low defect density of the PMMA thin-films was required. A parallel plate capacitor structure was used to test electrical properties of the PMMA dielectric layers. Good dielectric properties were obtained on glass and PEN at film thicknesses of 95 nm. An optimal condition for the OTFT preparation was used to fabricate an OTFT with the PMMA dielectric layer on glass substrate. Measured results showed that the OTFT achieved a mobility of 0.16 $cm^2/V.s$, a threshold voltage of -3.6 V, and on/off current ratio of 1×10^5.

Introduction

Organic thin-film transistors (OTFTs) have received considerable attention due to their potential applications in low-cost and flexible large-area electronics such as photo-detectors, displays, and radio-frequency identification tags. In the last decade, great efforts have been paid to develop chemically and physically stable organic semiconductor materials for operating high mobility in OTFTs. Pentacene is one of widely used organic semiconductors, the mobility have been report up to 0.33 $cm^2/V.s$ on Poly (methyl methacrylate) (PMMA) gate dielectric [1]. Generally, top-contact structure OTFTs can form better contacts between metal electrodes and semiconductor layers than the bottom-contact structure type to provide more efficient charge injection. However, the bottom-contact structure is still preferred for circuit integration of OTFTs because of the process difficulty of making source-drain electrode on top of the organic semiconductor layer with high resolution patterning without exposure to chemicals [2].

A dielectric layer can be used in capacitors or OTFTs, where development of high power and high energy density dielectric materials becomes a major enabling technology [3]. Defects in the dielectric layer can influence its electrical properties. For example, defects within the dielectric layers affect leakage currents due to increased tunneling leading to high power consumption and reduced device reliability [3]. In preparation of the PMMA thin-film dielectric layers from solution by spin-coating, good interconnected polymeric chain network dispersion can be obtained by using an appropriate solvent at an optimal spin speed and post-treatment. Dissolving PMMA in dimethylformamide (DMF) solution has produced films with high-quality mechanical and physical properties [4].

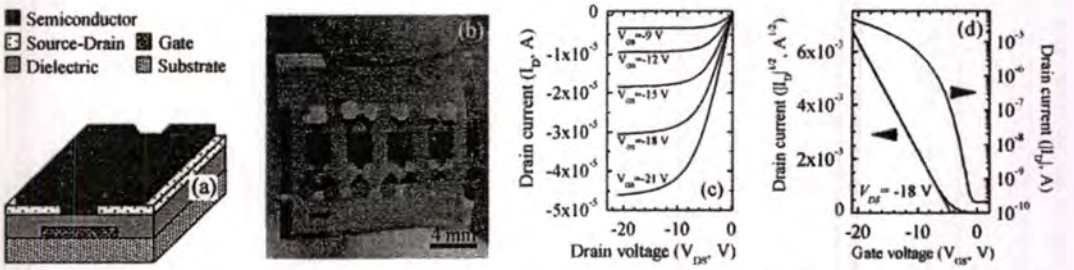

Fig. 1 (a) OTFT structure, (b) four OTFTs fabricated on PEN flexible substrate, (c) I_D-V_{DS}, (d) I_D-V_{GS}, and $I_D^{1/2}$-V_{GS} characteristics of the OTFT fabricated on PEN substrates

In this work, high quality thin-film dielectric PMMA layers were fabricated on three different substrates, i.e. glass, poly (ethylene naphthalate) (PEN), and Si wafer, via a spin-coating technique with DMF as the solvent. The electrical performances of the thin-film dielectric layers were analyzed by using parallel plate capacitors and pentacene OTFT devices.

Experiment procedure

Parallel plate capacitors and bottom-gate bottom-contact OTFTs were fabricated using PMMA films on 2 cm × 2 cm substrates. The structure of the OTFT device is shown in Fig. 1(a). Prior to fabrication, the glass substrate was successively cleaned with detergent and rinsed with deionized water and dried with nitrogen gas before being cleaned in piranha solution at 60 °C for 1 hour. Next, it was rinsed with deionized water and dried with nitrogen gas. The PEN substrate was sequentially cleaned with acetone, isopropanol and deionized water and dried with nitrogen gas. The Si wafer was cleaned in piranha solution at 60 °C for 1 hour and rinsed with deionized water and dried with nitrogen gas. For the PMMA film preparation, the PMMA (Average molecular weight of ~996,000 measured by Gel Permeation Chromatography from Sigma-Alrich) was dissolved in DMF (Analytical reagent grade from LAB-scan Analytical sciences) at various concentrations of 1-3 wt.%. The PMMA solution was spin coated onto the glass, PEN and Si wafer substrates at 2000 rpm. The substrates were then allowed to dry in argon atmosphere at 60 °C for 1 hour to remove residual solvents followed by heating at 120 °C for 1 hour in the same atmosphere to anneal the polymer films. The 30 nm-thickness aluminum films were evaporated through a metallic mask at a base pressure of 5×10^{-6} mbar to form the top and bottom electrodes of the capacitors and the gate electrode of the OTFTs. Gold electrodes 50 nm-thickness were evaporated through metallic mask at the base pressure 5×10^{-6} mbar to form the source-drain electrodes on the PMMA layer for the OTFTs. The channel length and width of the OTFTs are 18 μm and 2000 μm, respectively. The 50 nm-thickness Pentacene (Sigma-Alrich) films were evaporated through metallic mask at the base pressure of 5×10^{-6} mbar to form the semiconductor layer of the OTFTs.

The thicknesses of PMMA thin films on bare substrates were determined using a Profilometer (Dektak8000). Surface roughness of the PMMA layers on bare substrates were measured using Atomic Force Microscopy (AFM) (Seiko SPA400) with images of 3 μm × 3 μm surface area. For parallel capacitor measurement, the capacitance-frequency was measured by using an Agilent 4294a. Leakage current and breakdown measurements of the PMMA films and electrical characteristic of the OTFTs were analyzed by using a high-resolution current-voltage meter (Keithley 2612). The mobility, on/off current ratio, and threshold voltage of the OTFTs were calculated from the experimental electrical data.

Results and Discussion

The thicknesses of the spin-coated PMMA films on glass, PEN and Si wafer substrates at various concentrations with the spin speed of 2000 rpm were plotted in Fig. 2(a). The thickness of the film on each substrate, h, was found to increase with increasing concentration, c, of PMMA.

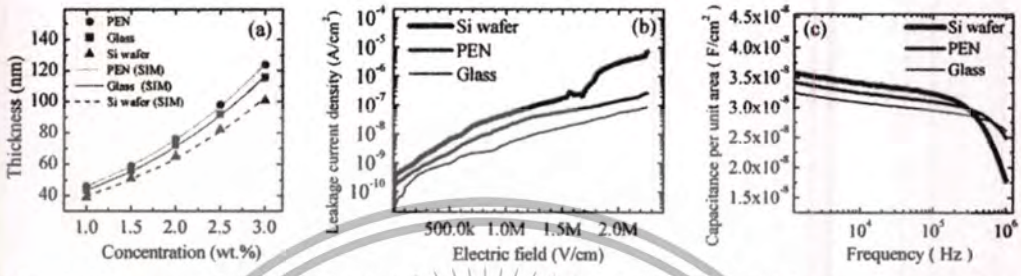

Fig. 2 (a) Thicknesses of the PMMA films on PEN, glass and Si wafer at PMMA concentrations of 1.0-3.0 wt.% in DMF at spin speed 2000 rpm., (*b*) Leakage current densities versus electric field applied to an Al/PMMA/Al structure with 95 nm thick PMMA films prepared on glass, PEN, and Si wafer with concentrations of 2.60, 2.45 and 2.85 wt.%, respectively, and (c) Capacitance-frequency plots (0.1kHz-1MHz) for the 95 nm-thick PMMA thin films on Si wafer, PEN and glass substrates.

The measured data were curved-fitted with a general exponential equation ($h=ke^{nc}$) in order to calculate the thickness of the films prepared with different PMMA concentrations, ranging from 1.0-3.0 wt.%. Equations (1), (2), and (3) are for glass, PEN, and Si wafer substrates, respectively.

$$h=26.50e^{0.49c} \quad (1)$$

$$h=28.00e^{0.50c} \quad (2)$$

$$h=24.71e0.48c \quad (3)$$

Fig. 2(a) shows that the experimental data fit well with the above equations in equations. The thicknesses of the PMMA films can be controlled by controlling the PMMA concentration when spin speed is kept constant at 2000 rpm. According to the film thickness profiles shown in Fig. 2(a), a thickness of 95 nm was found to be the highest for the PMMA film on Si wafer and it was used to fabricate all PMMA films for the parallel plate capacitors and the OTFTs on all three substrates. The required concentrations to obtain 95 nm film thickness were 2.60, 2.45, 2.85 wt.% PMMA in DMF for glass, PEN and Si wafer substrates, respectively, with the spin coating speed of 2000 rpm.

Reducing dielectric thickness is an alternative way to increase the capacitance of the films, see equation (4). The films should have acceptable leakage current, effective insulation and sufficient breakdown strength. The leakage current densities of the PMMA thin films in parallel plate capacitor structure are plotted versus applied electric field in Fig. 2(b). The contact area for measurement was 0.09 mm^2. Comparing between the PMMA thin films on Si wafer and glass substrates, the difference of leakage current density is about three orders of magnitude at strong electric fields. For the PMMA thin film prepared on Si wafer substrate, the current density was raised up to 10^{-5} A/cm^2 at an electrical field of 2 MV/cm. For the PMMA thin films prepared on PEN and glass substrates, the lower leakage currents of ~10^{-7} and ~10^{-8} A/cm^2 at electrical field of 2 MV/cm were obtained, respectively. The low leakage current density resulted from an effective dielectric film with a low defect density.

$$C = \frac{K\varepsilon_0 A}{t} \quad (4)$$

K is the relative permittivity or dielectric constant of the PMMA film, C is the measured capacitance, ε_0 is the permittivity of free space, A is an area of the capacitance, and t is the dielectric film thickness. The relationships between capacitance densities of the PMMA films on different substrates versus frequency are shown in fig. 2(c). It can be seen that, at frequencies below 300 kHz, the PMMA film on Si wafer exhibits the highest capacitance density. The distribution of the electric field is inhomogeneous because the capacitance is increased with surface roughness as a result of the rough and disordered surface [5].

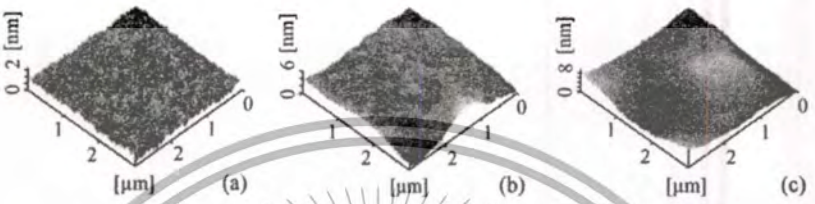

Fig. 3 Surface morphologies of spin-coated PMMA thin film on (a) glass, (b) PEN, and (c) Si wafer

At frequencies above 300 kHz, the PMMA films on glass and PEN have higher capacitance density than the PMMA on Si wafer. At high frequencies, the rougher surface suffers capacitance density fluctuation leading to quantum tunneling that can introduce undesired inductance and resistance of the film [6, 7].

AFM was used to investigate the surface morphologies of the PMMA films, Fig. 3. Surface roughness, rms, of the PMMA films on glass, PEN and Si wafer substrates were 0.26, 0.60, and 1.40 nm, respectively. In the spin coating process, mechanical spin toque, surface tension of solution, solvent evaporation and substrate free energy of substrate must be balance [8, 9], according it have been that good uniform thin film line of poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS) on substrate can be prepared by modification free surface energy of the substrate [10]. Our AFM results further show that the overall roughness of the PMMA film is influenced by the surface nature of the substrates. The small surface roughness values of the PMMA thin films deposited on glass and PEN substrates are promising for future low-cost fabrication of the OTFTs.

In this work, OTFTs with PMMA dielectric layers were successfully fabricated on glass and PEN with efficient output electrical characteristics. The MOSFET's square law characteristic equation in equation (5) was used to fit the experimental data (see Fig. 6(d)) and calculate the mobility μ and the threshold voltage Vt of the OTFTs.

$$I_D^{1/2} = \left(\mu C_i \frac{W}{2L}\right)^{1/2} (V_{GS} - V_t) \tag{5}$$

where I_D, C_i, V_{GS}, W, and L denote the drain current in the saturation regime, gate dielectric capacitance per unit area, gate-source voltage, channel width, and channel length, respectively. Fig. 6(c) show I_D-V_{DS} characteristics of the OTFTs prepared on PEN, respectively. Fig. 6(d) show I_D-V_{GS} and $I_D^{1/2}$-V_{GS} characteristics of the OTFTs prepared on PEN. As described by equation (5), the mobilities and threshold voltages of the OTFTs can be calculated from the slopes and x-axis intercepts of their corresponding $I_D^{1/2}$-V_{GS} graphs. The calculated mobilities of the OTFTs on glass and PEN substrates are 0.16 cm^2/V.s and 0.09 cm^2/V.s, respectively. The threshold voltages of the OTFTs on glass and PEN substrates are 3.60 V and 4.50 V, respectively.

$$S = \frac{dV_{GS}}{d(\log|I_D|)} \tag{6}$$

The subthreshold factor *S* is defined in equation (6) as the change in the gate-source voltage required to increase the drain current by a factor of 10. S is calculated by the inverse of the slope of I_D-V_{GS} graphs in Fig. 6(d). The calculated values of S for the OTFTs on glass and PEN substrates are 0.98 and 1.23 V/decade, respectively. The calculated mobilities, threshold voltages and subthreshold factors show that PMMA films prepared on different substrates influence the OTFTs performance significantly. The difference in capacitance, i.e. dielectric, characteristics of the PMMA films on different substrates supports previous explanations [11, 12] that the PMMA dielectric layers affect the disorder induced in the accumulation zone of the organic semiconductor layer in the OTFT structure and disturb π-π stacking resulting in different OTFTs performances.

Summary

A spin-coating method was successfully used to prepare PMMA dielectric thin films on glass and PEN substrates with thicknesses of 95 nm. DMF was selected to dissolve PMMA for fabrication of PMMA thin films due to its high-quality electrical and physical properties. The PMMA dielectric thin films on glass and PEN substrates in this study have good dielectric properties enabling successful OTFT fabrication. The calculated mobilities of the OTFTs on glass and PEN substrates are 0.16 cm^2/V.s and 0.09 cm^2/V.s, respectively. The threshold voltages of the OTFTs on glass and PEN substrates are 3.60 V and 4.50 V, respectively. The defect-free and low surface roughness dielectric layer can achieve high-mobility pentacene active layer in the OTFT structure.

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