DDCC-BASED ANALOG SIGNAL PROCESSING APPLICATIONS

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หัวข้อวิทยานิพนธ์	การประยุกต์ใช้งานดีดีซีซีในการประมวลผลสัญญาณแอนะล็อก
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บทคัดย่อ

วิทยานิพนธ์นี้นำเสนอวงจรประมวลสัญญาณแอนะล็อกโดยใช้ ดีดีซีซี(Differential difference current conveyors: DDCC) เป็นวงจรพื้นฐาน โดยได้นำเสนอการประยุกต์ใช้วงจรประมวลผลสัญญาณแอนะล็อกจำนวน สามวงจร วงจรแรกคือ วงจรตัวความต้านทานแบบลอยตัว วงจรประกอบด้วย ดีดีซีซี หนึ่งวงจร มอสทรานซิสเตอร์สี่ตัวและแหล่งจ่ายกระแสหนึ่งแหล่งจ่าย วงจรตัวต้านทานที่นำเสนอสามารถปรับค่าความต้านทานได้ด้วยแรงดันและกระแส วงจรที่สองเป็นวงจรคูณและหารกระแสแบบลอการิทึมและแอนติลอการิทึม (Logarithm-Antilogarithm) โดยใช้ ดีดีซีซี หนึ่งวงจรและไดโอดสี่ตัว โดยวงจรคูณและหารกระแสที่นำเสนอมีเสถียรภาพทางอุณหภูมิที่ดี วงจรที่สามคือ วงจรบวกและลบแรงดันที่สามารถโปรแกรมได้ด้วยวิธีทางดิจิทัลเมื่อใช้คุณสมบัติของวงจร ดีดีซีซี การบวกและลบแรงดันจึงสามารถทำได้โดยง่าย วงจรประมวลผลสัญญาณที่นำเสนอทั้งหมดมีคุณสมบัติที่โดดเด่นที่สำคัญคือ โครงสร้างของวงจรสามารถสร้างได้ด้วยเทคโนโลยีซีมอสและมีโครงสร้างที่ไม่ซับซ้อนใช้จำนวนอุปกรณ์น้อยกว่าเมื่อเทียบกับหลักการเดิมที่เคยมีการนำเสนอมาก่อน ซึ่งเหมาะกับการนำไปสร้างเป็นวงจรรวม วงจรที่ได้นำเสนอทั้งหมดจะถูกจำลองการทำงานด้วยโปรแกรม PSpice เพื่อยืนยันความถูกต้องในการทำงานของวงจรว่ามีความสอดคล้องและเป็นไปตามหลักการที่ได้นำเสนอ

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ABSTRACT

This thesis presents the applications of analog signal processing based on differential difference current conveyors (DDCCs). There are three proposed circuits of analog signal processing in this thesis. Firstly, a new voltage-controlled floating resistor based on DDCC is proposed. The proposed resistor employs one DDCC, four MOS transistors and one current source; its resistance can be controlled through adjusting of the biasing voltage and current. Secondly, a new current-mode log-antilog multiplier/divider using DDCC with one DDCC and four-diodes is presented. It is noted that the proposed circuit offers the excellent temperature stability. Finally, the development of a programmable voltage adder/subtractor using DDCC, which its function can be directly programmable by a digital signal code, is proposed. It is shown that DDCC is employed for the applications of analog signal processing. All proposed circuit configurations can be fully integrated in CMOS technology and low circuit complexity are very suitable for integrated circuit implementation, which differs from recently proposed. To confirm the theoretical analysis and implementation of an analog signal processing applications are studied through PSpice simulations.

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Usa Torteanchai

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LIST OF ABBREVIATIONS

Abbreviation	Definition
BiCMOS	Bipolar complementary metal oxide semiconductor
CC	Current conveyor
CCI	First generation current conveyor
CCII	Seconed generation current conveyor
CCIII	Third generation current conveyor
CCCII	Current controlled current conveyor
CDBA	Current differencing buffered amplifier
CMOS	Complementary metal oxide semiconductor
CMRR	Common mode rejection ratio
DDA	Differential difference amplifier
DDCC	Differential difference current conveyor
DOCCII	Dual-output seconed generation current conveyor
DVCC	Differential voltage current conveyor
ECCII	Electronically tunable second generation current conveyor
FOX	Field oxide
GaAs	Gallium arsenide
ICs	Integrated circuits
ICCII	Inverting seconed seconed generation current conveyor
IEEE	Institute of Electrical and Electronics Engineerings
JFET	Junction field effect transistor
MOSFET	Metal oxide semiconductor field effect transistor
NMOS	*n*-channel metal oxide semiconductor semiconductor
OTA	Operational transconductance amplifier
PMOS	*p*-channel metal oxide semiconductor semiconductor
SPICE	Simulation Program with Integrated Circuit Emphasis
THD	Total harmonic distortion
VCR	Voltage-controlled resistor
VLSI	Very large scale integration

LIST OF SYMBOLS

Symbol	Definition
A_d	Differential gain of amplifier
A_o	Open loop gain of amplifier
C_{db}	Drain-to-bulk capacitance
C_{db_b}	Drain-to-bulk capacitance of *pn* junction
C_{db_sw}	Drain-to-bulk sidewall capacitance
C_{gd}	Gate-to-drain capacitance
C_{gs}	Gate-to-source capacitance
C_{gs_ch}	Gate-to-source capacitance due to channel of MOS transistor
C_{gs_ov}	Gate-to-source capacitance due to overlap of MOS transistor
C_{js}	Depletion capacitance per unit area of the source junction
C_{js_sw}	Sidewall depletion capacitance per unit area of the source junction
C_{ox}	Gate capacitance per unit area
C_{sb}	Source-to-bulk capacitance
C_X, C_Y, C_Z	Low-value capacitance at terminals X, Y, and Z of the DDCC
g_m	Transconductance
i	Terminal current of an active element
i_X, i_Y, i_Z	Input or output current terminals of the current conveyor
I	Terminal current of a function block
I_B	Input bias current
I_D	Drain current of MOS transistor
I_{DS}	Drain-to-source current
I_G	Gate current of MOS transistor
I_S	Source current of MOS transistor
I_o	Control current
K_i, K_n, K_p	Transconductance parameter of an active element
L_D	Diffusion length of MOS transistor
L_x	Channel length of n^+ region of MOS transistor
NL	Nonlinearity of an active element

r_{ds}	Drain-to-source resistance
R_X	Parasitic resistance of the current conveyor
R_X, R_Y, R_Z	High-value parasitic resistance at terminals X, Y, and Z of the DDCC
V_B	Bias voltage
V_C	Control voltage
V_{cm}	Common-mode voltage
V_d	Differential voltage
V_{DD}, V_{SS}	Supply voltages of MOS structures
V_{DS}	Drain-to-source voltage
V_{eff}	Effective voltage
V_{fs}	Full scale voltage
V_{GS}	Gate-to-source voltage
V_{nn}, V_{np}	Inverting input terminals of DDA
V_{pp}, V_{pn}	Non-inverting input terminals of DDA
V_{SB}	Source-to-bulk voltage
V_T	Threshold voltage
V_{Tn}	Threshold voltage of NMOS
V_{Tp}	Threshold voltage of PMOS
V_o	Output voltage
V_{ov}	Overdrive voltage
v_X, v_Y, v_Z	Input or output voltage terminals of the current conveyor
W/L	MOS transistor dimensions
X, Y_1, Y_2, Z_1, Z_2	Input or output, current or voltage terminals of the DDCC
Z	Impedance
α	Frequency transfer function of the internal voltage followers
β	Frequency transfer function of the internal current followers
γ	Body-effect constant
δ	Matching error parameter
ε_i, ε_v	Current and voltage tracking error parameter
λ	Channel length modulation factor
μ_n	Mobility of electron
ϕ_F	Fermi potential of the substrate

CHAPTER 1

INTRODUCTION

1.1 Analog Signal Processing: a Historical Overview

1.1.1 Analog Circuit Design

Analog circuit design is the successful implementation of analog circuits and systems using integrated circuit (IC) technology. Analog circuits and systems have an important role in the implementation and application of very large scale integration (VLSI) technology. The development of VLSI technology, coupled with the demand for more signal processing integrated on a single chip, has resulted in an increased need for the design of effective analog ICs [1]. Analog circuit design is becoming increasingly important with growing opportunities. The emergence of ICs incorporating mixed analog and digital functions on a single chip has led to an advanced level of analog design [2].

Since the early 1970's, the field of analog circuits and systems has developed and matured. During this period, much has been made of the competition between analog and digital system design strategies. Advances in digital VLSI have enabled memories, microprocessors, and digital signal processors [3]. As the level of integration increased in IC technology, digital circuit implementation became more desirable than analog circuit implementation. This is because of its robustness, reliability, accuracy, ease of design, programmability, flexibility, and cost [2]. With the advances of VLSI technology, digital signal processing is proliferating and penetrating into more and more applications. Many applications which have been traditionally implemented in analog domain have been moved to digital, such as digital audio and wireless cellular phones [1].

Even if digital circuits could always outperform analog circuits with smaller or equivalent area, analog circuits would still be required. There are some facts that make analog ICs and systems increasingly important. First of all, the natural world is analog. Thus, analog systems are needed in information acquisition systems in order to prepare analog information for conversion to digital format [3]. In other words, interface functions are required between the real world and the silicon system due to the fact that most of the signals in the physical world are analog. The primary information acquired from the real world is usually in the form of time continuous analog signals and must be interfaced to digital circuitry. The result of the digital processing must likewise be converted to back to analog form. In a digital signal processing

system, amplification, filtering, and signal conditioning are required before converting to the digital format. After output signal digital to analog conversion, again filtering is needed. Finally, the smoothed output signal must be amplified to the appropriate power level to achieve the desired effect. That is, analog pre-processing before the analog to digital conversion and post-processing after the digital to analog conversion are needed for a digital signal processing system. Therefore, analog circuits will continue to be a part of large VLSI digital systems.

In recent years, the quest for ever smaller and cheaper electronic system has led manufacturers to integrate entire system onto a single chip. It is now becoming common to find that a single mixed analog and digital (mixed mode) IC contains both a digital signal processor and all the analog interface circuits required to interact with its external analog transducers and sensors [4]. That is, analog and digital VLSI circuits coexist on the same chip. On the other hand, there remain many signal processing tasks that are best performed by analog circuits. Complete analog systems will still continue to be required in some applications, mainly those in which the frequency of operation is too high for digital implementation or in very low power applications.

1.1.2 Integrated Circuit Technology

The element of principal importance concerning analog signal processing is the trend of technology. There are mainly four viable integrated technologies for analog circuits. These technologies are bipolar, complementary metal oxide semiconductor (CMOS), BiCMOS, and gallium arsenide (GaAs) [2]. Much of the analog design during the 1960's and 1970's was done in bipolar technology. The 1980's was an era of rapid evolution of MOS analog ICs, in particular CMOS.

CMOS technology has become a dominant analog technology primarily because of good quality capacitors, good switches and low power dissipation. It provides very large scale integration of both high density digital circuits and analog circuits for low cost. On the other hand, comparison between the bipolar and CMOS technologies in terms of bandwidth and noise favors the bipolar from an analog viewpoint. However, a similar comparison made from a digital viewpoint would come up on the side of CMOS. Therefore, since large volume technology will be driven by digital demands, CMOS is an obvious result as the technology of availability. Furthermore, the potential for technology improvement for CMOS is greater than for bipolar and the performance in CMOS generally increases with decreasing channel length.

During the 1990's, we have seen the BiCMOS technology emerge as a serious contender to the original technologies. BiCMOS technology combines both bipolar and CMOS technologies and obviously has the advantages of both. BiCMOS offers the ability of low power dissipation using CMOS and high speed performance using bipolar. On the other hand, it is somewhat more expensive to fabricate. GaAs technology is quickly maturing and offers many possibilities as a niche technology. From an analog viewpoint, GaAs is well developed for microwave analog but less developed for analog signal processing.

It is clear that CMOS technology is preferred for digital design. Since analog and digital functions are placed onto a single chip in modern VLSI systems, the use of CMOS technology for analog circuits is also preferred. CMOS process implementation is preferable because CMOS process makes it possible to implement mixed signal circuit chips with lower cost [5]. During the past years, we have seen a proliferation of mixed analog/digital VLSI ICs realized in state of the art CMOS technologies to optimize cost and power dissipation in consumer products, many of which are pocket size and battery powered. It has also the advantages of low power consumption and high integration density. Therefore, dominant VLSI technology for analog circuits is CMOS up to GHz range.

1.1.3 Current Mode Approach

Analog processing systems traditionally use input and output voltages which are in charge of carrying the information. The voltage-current duality, which results from the Kirchoff's laws, as well as from the Thevenin's and Norton's theorems, allows analog circuits working from current signals to be obtained, too. Because the measurement of a voltage across impedance was easier than the measurement of the current flowing through this impedance, engineers used to work with voltages rather than with currents [6]. Thus, it has become customary in electrical engineering to think of signal processing in terms of voltage variables rather than current variables. This tendency has resulted in voltage signal processing circuits such as voltage amplifiers, voltage integrators, filters which realize a voltage transfer function, etc [7].

Most analog signal processing is accomplished through the use of feedback around a high gain voltage amplifier to achieve a well defined voltage transfer function which is independent of the active devices. The high gain voltage amplifier may consist of discrete components or may be an IC such as a voltage operational amplifier (op-amp). This approach has worked well as evidenced by a large number of analog circuits which use the voltage op-amp.

Since the introduction of ICs, the op-amp has served as the basic building block in analog circuit design and has been widely used in a variety of applications such as addition/subtraction circuits, amplifiers, multipliers/dividers, interface circuitry, digital to analog converters, analog to digital converters, variable gain amplifiers, filters, oscillators, etc [8]. Most of the systems based on voltage op-amps represent the signal of interest in the voltage domain [9].

High frequency operation is an ever present demand on analog circuits. Analog circuits are always requested to work at high frequencies where digital signal processing faces difficulties with implementation. In addition to this demand, a recent advanced fabrication process forces analog circuits to operate under supply voltages as low as possible. This is because of reduction in tolerant voltages of transistors, reduction in power consumption, the same chip implementation together with digital circuits, etc [5]. In these respects, realization of low voltage and high frequency analog circuits are one of the most attractive and important issues in many signal processing fields.

However, the classical op-amp suffers from limited gain-bandwidth product problems and from low slew rate at its output. Many circuits employing op-amps have been designed and described. The limited gain-bandwidth product of the op-amp affects the parameters of the circuits designed. They remain, therefore, unsatisfactory at higher frequencies [10].

In order to correspond to the severe demands for high frequency and low power supply voltage operation on analog circuits, designers made plenty of attempts. Among these is the current mode approach. There has been a great shift in analog circuit design towards representing signals with current instead of voltage to achieve high performance analog circuits in CMOS technology. So, in the past years current mode circuits began to receive a great attention as a new alternative to voltage mode circuits. This is because one of the most promising solutions to high frequency and low voltage operation is thought to be current signal processing. A current mode circuit may be taken to mean any circuit in which current is used as the active variable in preference to voltage, either throughout the whole circuit or only in certain critical areas [11].

Current mode circuits have been receiving considerable attention due to their potential advantages such as inherently wide bandwidth, higher slew rate, wider dynamic range, simpler circuitry, low voltage operation and low power consumption. Furthermore, current mode circuits are suitable for integration with CMOS technology and thus have become more and more attractive in electronic circuit design in recent years.

Transistors are more suitable for processing currents rather than voltages because they are inherently current mode i.e., both bipolar and MOS transistors are current output devices. An important number of elementary mathematical functions can be obtained easier from current signals rather than from voltage. In this order, to generate the sum of various currents flowing to ground does not necessitate to use any passive components. This can easily be obtained onto any virtually grounded node. On the contrary, summing several voltages is not as easy. The later needs several resistances to achieve respectively both voltage-current conversion on input and current-voltage conversion on output. The operation of summation being also obtained as before, from current signals. Therefore, mathematical operations of adding, subtracting or multiplying signals represented by currents are simpler to perform than when they are represented by voltages. For this reason, integrated current mode system realizations are closer to the transistor level than the conventional voltage mode realizations and therefore simpler circuits and systems should result.

In voltage mode circuits the high valued resistors with parasitic capacitances create a dominant pole at a relative low frequency, which limits the bandwidth. In general, the node impedances in current mode circuits are low and the voltage swings are small. Thus the time constant is reduced and also the time required for charging and discharging a parasitic capacitor is kept small. Hence the slew rate for current mode circuits will be sufficiently high. They are well suited to work at higher frequencies and thus are often used in communication circuits. The low supply voltage operation is achieved because small voltages appear on the nodes.

From these major merits many analog circuit designers believe that current mode circuit techniques meet the severe demands for low power supply voltage and high frequency operation on analog circuits. Although a current mode approach is promising, voltage mode circuits have a lot of merits against current mode circuits. First of all, a fact that there exist plenty of practically used circuits is very important in terms of reliability. Because of this, most of the systems use not current signals but voltage signals. Therefore, a voltage mode approach is still attractive even though a current mode one becomes popular.

1.1.4 Current Mode Building Block

Recent researches on integrated circuits and systems in last decade have presented a new trend in integrated circuit design which is regarded as "Current-Mode Signal Processing". Unlike in Voltage-Mode signal processing, current-mode signal processing techniques mostly focus on

current that is to be used as input and output signals. As circuit designers show a dense interest to current-mode signal processing, new building blocks appear in academic papers. As an obvious result of these efforts, Current Conveyor was introduced in academic papers to be one of the most powerful building blocks for the future of current-mode signal processing [12].

The first current conveyor was introduced by A. Sedra & K. C. Smith in 1968 [12]. However, at the time of the introduction, designers and researchers mostly dedicated their attention to op-amp based integrated circuits and systems. Recent development of current-mode signal processing makes this early invention an important item for today's analog integrated circuit design theory and practice. In 1970, A. Sedra and K. C. Smith introduced a more versatile building block named as CCII [13] having many different features over CCI which no doubt made it a shining star for active network synthesis. By the year 1995, a new version of current conveyor named as CCIII was introduced [14] which as well relies on the common current conveying approach behind the invention of CCI. All the mentioned conveyors and the derived conveyor types have been used in construction of many complex circuits and systems so far. For today, current conveyor can be regarded as one of the most famous building blocks for analog integrated circuit and system design.

1.2 Thesis Motivation and Aim of the Thesis

The goal of the present thesis is to develop applications of analog signal processing using current conveyors, which is suitable for implementation of analog circuits. This would enable designers to show advantages of current conveyor over voltage-mode circuits. The current conveyor offers several advantages over the conventional op-amp; specifically a current conveyor circuit can provide a higher voltage gain over a larger signal bandwidth under small or large signal conditions than a corresponding op-amp circuit in effect a higher gain-bandwidth product.

In addition, current conveyors have been extremely successful in the development of analog circuits which does not depend critically on the matching of external components, instead depends only on the absolute value of a single component. In applications such as analog signal processing, automatic control, and instrumentation systems, processing differential voltage signals is very common, thus a single voltage input terminal is hardly competent.

The conventional current conveyor (CCI and CCII) have apparent disadvantage of having only one input terminal, while in the differential difference current conveyor (DDCC) [15]-[16], it has multi-input voltage terminal and also has differential voltage signal at X input current

terminal. The DDCC has the advantages of both the CCII and the differential difference amplifier (DDA) (such as high input impedance and arithmetic operation capability) [17]. As a result, a number of DDCC-based circuits have been presented in technical literatures [15]-[23].

The DDCC circuit is quite useful as a powerful active building block of current-mode circuits because it has high performances and is suitable for analog signal processing applications.

As the result, taking all the mentioned point into realization of analog signal processing circuits by using a new CMOS DDCC can be regarded as an important research area in analog signal processing, analog integrated circuits and systems.

1.3 Thesis Organization

The main objective of this thesis is to introduce new analog signal processing applications using the differential difference current conveyor (DDCC). The literature reviews, of which previous work done in this field are discussed and background theory will be explained in Chapter 2. The detailed description of differential difference current conveyor (DDCC) and CMOS realization of DDCC representation will be shown in Chapter 3. In Chapter 4 the applications of analog signal processing based on DDCC will be proposed with the schematic, symbol and simulation results. Finally, thesis ends in Chapter 5 with the conclusions and the scope for the future work.

CHAPTER 2

LITERATURE REVIEW AND BACKGROUND THEORY

2.1 IEEE Papers Review with Critique

The current conveyor introduced in 1968 by A. S. Sedra and K. C. Smith [12]. At the time of the introduction of the current conveyor it was not clear what advantages the current conveyor offered over the conventional op-amp. The electronics industry was focusing its efforts on the creation and application of the first generation of monolithic op-amps. The second generation current conveyor CCI introduced by Sedra and Smith is widely used in realization of an analog signal processing applications [13]. It is available with both polarity as CCII+ and CCII–. By connecting CCII+ and CCII– together a dual output CCII (DOCCII) is formed which has got its importance in the realizations of current-mode analog signal processing.

The circuit design principles and techniques for current-mode processing, such as the Trans linear circuit principal introduced by Barrie Gilbert in 1975 [24] are becoming powerful tools for the development of high performance analogue circuits and systems. A further consequence of the development of current mode analogue signal processing has been the emergence of new analogue building-blocks ranging from the current conveyor and current-feedback op-amp through to sampled-data current circuits such as dynamic current-mirrors and analogue neural networks. It has proved to be functionally flexible and versatile, rapidly gaining acceptance as a practical device with a wide range of high performance circuit and system applications. The recent introduction of a commercially integrated circuit current conveyor is reported and is indeed very timely and welcome.

The accurate CMOS based current conveyor technique for implementing both positive and negative second generation current conveyor (CCII) is described by Wanlop Surakampontorn, Reiewruja, Kiattisak Kumwachara and Kobchai Dejhan [25]. It can be employed as an element in a digital-to-analog converter that can provide current source output, or as a current measuring device in a digital measuring of current, or as a plug-in unit or probe for a digital volt-meter.

High CMRR and low THD current-mode instrumentation amplifier using current inversion technique is introduced by Behnam Babaei and Sattar Mirzakuchaki [26]. The current-mode instrumentation amplifier based on second generation current conveyor (CCII) offers many benefits over conventional instrumentation amplifier architectures. In addition, current conveyors

have been extremely successful in the development of an instrumentation amplifier which does not depends critically on the matching of external components, instead depends only on the absolute value of a single component. In applications such as analog signal processing, automatic control, and instrumentation systems, processing differential voltage signals is very common, thus a single voltage input terminal is hardly competent.

Current conveyors and related current-mode circuits have begun to emerge as an important class of circuits with properties that enable them to rival their voltage-mode counterparts in a wide range of applications. The use of current rather than voltage as the active parameter can result in higher usable gain, accuracy and bandwidth due to reduced voltage excursion at sensitive nodes.

The differential difference current conveyor (DDCC) was proposed in 1996 by Chiu et al. [15] and a new CMOS realization of DDCC is presented by Jianping Hu, Yinshui Xia and Tiefeng Xu, Huiying Dong [16]. The negative feedback action is introduced by using a current mirror to reduce channel length modulation effect of MOS transistors. Furthermore, the circuit is insensitive to the threshold voltage variation caused by the body effect of MOS transistors. Comparing with conventional design, the DDCC circuit has less harmonic distortion and larger linear range. DDCC based analog signal processing application circuits are described [15]-[16].

The conventional current conveyor such as CCI and CCII have apparent disadvantage of having only one input terminal but in the differential difference current conveyor, it have multi input voltage terminal and also have differential voltage signal at X input current terminal.

The DDCC circuit is quite useful as a powerful building block of current-mode circuits because of its high performances. The DDCC is useful for processing differential voltages signals and suitable for implementation of analog signal processing circuits [18]-[23].

2.2 CMOS Technology

Today's field of microelectronics is dominated by a type of device call the metal-oxide-semiconuctor field-effect transistor (MOSFET). Conceived in the 1930s but first realized in the 1960s, MOSFETs (also called MOS devices) offer unique properties that have led to the revolution of the semiconductor industry. This revolution has culminated in microprocessors having 100 million transistors, memory chip containing billions of transistors, and sophisticate communication circuits providing tremendous signal processing capability.

CMOS transistor is discussed in this section. This section provides an overview of device structure, their modes of operation, small-signal model of active devices and analytical expressions of the small-signal model parameters.

2.2.1 CMOS Transistors

Complementary Metal-Oxide Semiconductor (CMOS) transistors are the most commonly used components in the digital circuit implementations. In CMOS technology, *n*-channel and *p*-channel MOSFETs (Metal-Oxide Semiconductor Field-Effect Transistors) are fabricated on single silicon-wafer. CMOS technology is the most common choice for digital logic due to low cost, having complementary devices with similar characteristics, small feature size which enables the designer to integrate large number of devices in small chip area, infinite input resistance at the gate and zero static power dissipation in the digital logic cells.

2.2.2 Device Structure

A simplified cross section of an *n*-channel MOS (NMOS) transistor is shown in Fig.2.1. It is built on a lightly doped *p*-type substrate (p^-) that separates two heavily doped *n*-type regions (n^+) called source and drain. A dielectric of silicon oxide and a polysilicon gate are grown over the separation region. The region below the oxide is the transistor channel and its length is the length that separates the source and the drain, is the channel length, denoted by L. In a *p*-channel MOS (PMOS) all the regions are complementary doped.

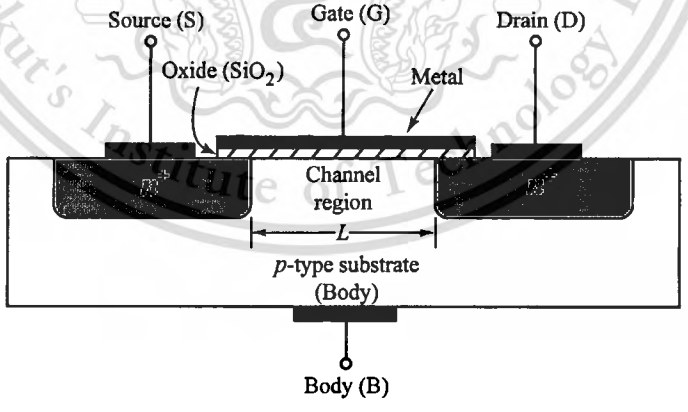


Figure 2.1. NMOS device structure

There is no physical difference between the source and the drain as the device is symmetric, the notations source and drain only depend on the voltage applied. In an NMOS, the source is the terminal at the lower potential while, in a PMOS the source is the terminal at the higher potential.

2.2.3 Device Operation

To understand the basic operation of an NMOS, its behavior is analyzed based on the voltages applied to its terminals. If the source and drain are grounded then the device behaves as a capacitor formed by the polysilicon gate and substrate, separated by silicon oxide. When a negative voltage (with respect to source) is applied to the gate terminal, negative charges are accumulated at the gate surface near oxide layer, which push negative charges deep in the substrate creating a positive charge space in the substrate near the oxide between drain and source regions. It is called charge accumulation and transistor works as a capacitor. If small voltage difference is applied between the source and drain terminals, then a very small leakage current will flow through the accumulated channel.

Now a positive voltage (with respect to source) is applied to the gate. Positive charges repel holes near the oxide surface in substrate and attract free electrons towards the channel between drain and source. As the positive gate-to-source voltage (V_{GS}) is increased, the more electrons are attracted to the channel. At sufficient positive gate voltage, the region between source and drain under the oxide layer becomes n-type and channel is said to be inverted as shown in Fig.2.2. The minimum gate voltage required to create an inverted channel is called Threshold voltage (V_T). If a very small drain-to-source (V_{DS}) voltage is applied to the device, a small amount of current will flow through the channel. As V_{GS} exceeds V_T, more electrons are attracted into the channel and the channel will grow deep in the substrate. The excess gate voltage ($V_{GS} - V_{Tn}$) is known as the effective voltage (V_{eff}) or the overdrive voltage (V_{OV}). The conductance of the channel is proportional to the effective voltage.

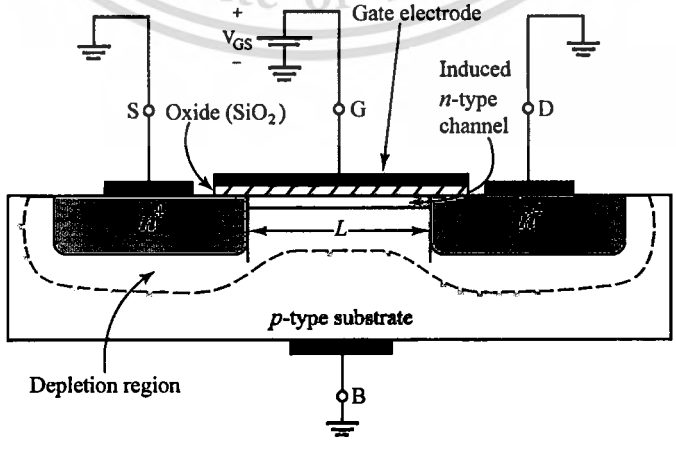


Figure 2.2. NMOS channel

2.2.3.1 Triode or Linear Region

Small values of V_{DS} do not affect the charge density of the channel and the channel behaves as a linear resistor due to unformed channel charge density. For small V_{DS}, the channel current or drain-to-source current (I_{DS}) can be expressed as [27].

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{Tn})V_{DS} \tag{2.1}$$

where

μ_n : represents mobility of electrons

C_{ox} : represent gate capacitance per unit area

W : represent width of the channel of NMOS

L : represent length of the channel of NMOS

V_{GS} : represent gate-to-source input voltage to NMOS load

V_{Tn} : represent threshold voltage of NMOS

Fig.2.3 shows a sketch of I_{DS} versus V_{DS} for various values of V_{GS}. As stated before that the NMOS is operating as a linear resistance whose value is controlled by V_{GS}. The resistance is infinite for $V_{GS} \leq V_T$ (cutoff region) and its value decreases as V_{GS} exceeds V_T.

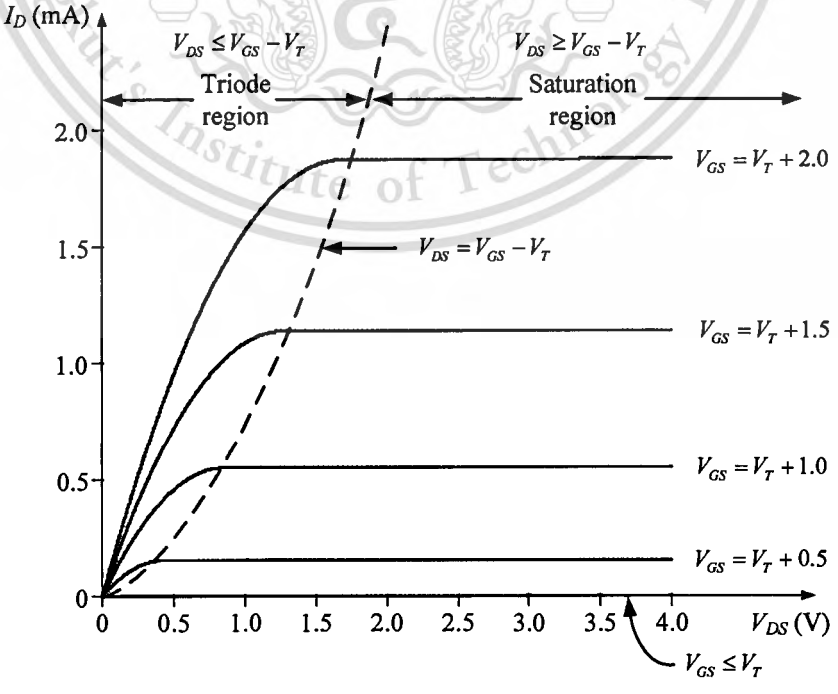


Figure 2.3. NMOS operational region

As the drain voltage is increased, the voltage drop at every point in the channel does not remain same, creating a non-uniform channel charge density. Due to increase in drain voltage, the voltage drop between gate and drain is decreased causing a reduction in the channel depth at the drain as shown in Fig.2.4. Due to non-uniform channel, channel resistance increases and the drain current (I_{DS}) will no longer remain linear function of V_{DS}. Large values of V_{DS} introduce a quadratic dependence in the current-voltage relationship [28] and $I_{DS} - V_{DS}$ curve does not continue as a straight line but bends as shown in Fig.2.3.

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{Tn} - \frac{V_{DS}}{2})V_{DS} \tag{2.2}$$

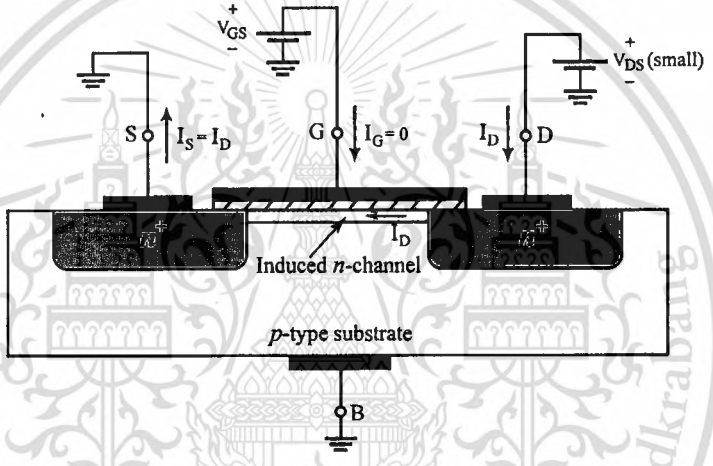


Figure 2.4. NMOS triode region

The current I_{DS} is linearly related to V_{GS} and has a quadratic dependence on V_{DS}. Under this condition the device is said to operate in *Triode* or *Linear region*. The operating condition to bias the transistor in triode region is [27].

$$V_{DS} < V_{GS} - V_{Tn} \tag{2.3}$$

2.2.3.2 Saturation or Active Region

A further increase of V_{DS} leads to the situation where voltage drop between gate and drain becomes equal to threshold voltage (V_T) i.e., $V_{GD} = V_T$, or $V_{GS} - V_{DS} = V_T$, or $V_{DS} = V_{DSsat} = V_{GS} - V_T = V_{eff}$. The channel depth at the drain end decrease to almost zero, and the channel is said be *pinched off*. Increasing V_{DS} beyond this value has a small effect on the channel

shape. Theoretically, the drain current through the channel remains constant under this condition and the transistor is said to operate in *Saturation* or *Active region*. The drain current, for the values of V_{DS} greater than V_{DSsat}, becomes independent of drain voltage and can be expressed as

$$I_{DS} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{Tn})^2 \tag{2.4}$$

The operating condition to bias the transistor in triode region is

$$V_{DS} \geq V_{GS} - V_{Tn} \tag{2.5}$$

Eq.(2.4) is first order approximation. In fact, increasing V_{DS} yields an increase in the pinch-off region as well as decrease in channel length as shown in Fig.2.5. This effect is commonly known as *channel-length modulation*. A decrease in channel length results in increase in drain current. To take channel-length modulation effect into account, a corrective term is introduced in Eq.(2.4).

$$I_{DS} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{Tn})^2[1 + \lambda(V_{DS} - V_{DSsat})] \tag{2.6}$$

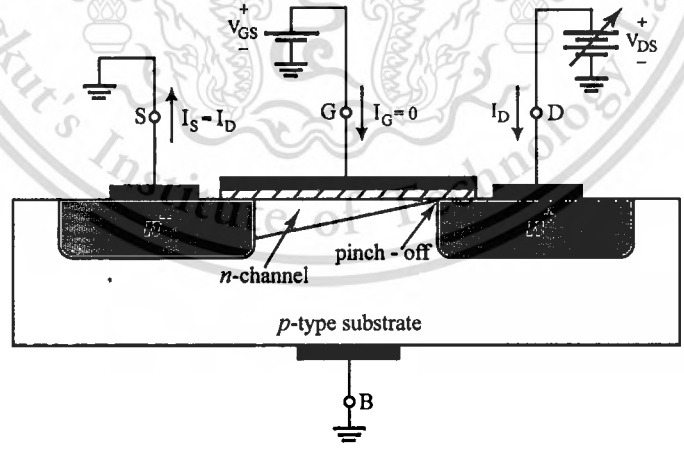


Figure 2.5. NMOS pinch off channel

The parameter λ is referred to as channel length modulation factor and it is inversely proportional to the channel length.

2.2.3.3 Body Effect

While deriving current-voltage relationship for different operating region of MOS, its is assumed that source and substrate (bulk) are at same potential. This common condition is not applicable in some conditions, e.g. diode-connected NMOS active load with output taken from source terminal. Voltage difference between source and bulk gives rise to a second order effect, known as *body-effect*. Body-effect increases the threshold voltage of MOS device resulting in following expression for threshold voltage.

$$V_{Tn} = V_{Tn0} + \gamma(\sqrt{V_{SB} + 2|\phi_F|} - \sqrt{2|\phi_F|}) \tag{2.7}$$

where

V_{SB} : represent source-to-bulk voltage

V_{Tn0} : represent threshold voltage for zero V_{SB}

γ : represent body-effect constant

ϕ_F : represent Fermi potential of the substrate

2.2.4 Device Modeling

In this section, small-signal model for NMOS transistor is presented to model the dc behavior and the charge effect in different regions of operation.

2.2.4.1 Small-Signal Modeling in the Saturation Region

Low-Frequency Small-Signal Model:

The most commonly used small-signal model for NMOS is shown in Fig.2.6.

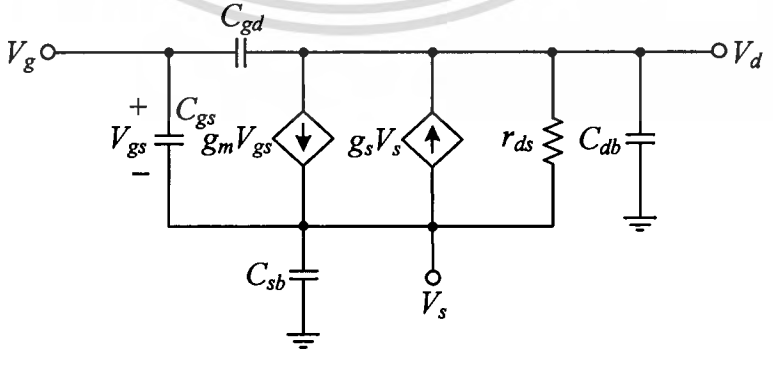


Figure 2.6. NMOS small signal model

The most important model component is the voltage-controlled current generator, $g_m v_{ds}$ with the transistor transconductance g_m defined as [29].

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{Tn}) \tag{2.8}$$

Transconductance (g_m) can be expressed in terms of drain current I_{DS} as

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{DS}} \tag{2.9}$$

The model includes body effect in form of second voltage-dependent current source $g_s v_{sb}$ and its transconductance is defined as

$$g_{sb} = -\frac{\partial I_{DS}}{\partial V_{SB}} = \frac{\partial I_{DS}}{\partial V_{Tn}} \frac{\partial V_{Tn}}{\partial V_{SB}} \tag{2.10}$$

From Eq.(2.4), we have

$$\frac{\partial I_{DS}}{\partial V_{Tn}} = -\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{Tn}) = -g_m \tag{2.11}$$

And using Eq.(2.7), we can deduce

$$\frac{\partial V_{Tn}}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{V_{SB} + 2|\phi_F|}} \tag{2.12}$$

Therefore, substituting Eq.(2.11) and Eq.(2.13) into Eq.(2.10), we get

$$g_s = \frac{\gamma g_m}{2\sqrt{V_{SB} + 2|\phi_F|}} \tag{2.13}$$

Note that g_s is not zero for zero source-to-bulk voltage (V_{SB}). If source is connected to bulk then body-effect need not be included in the analysis but if source and bulk has same

potential but not connected, body-effect should be taken into account as V_{SB} is not necessarily zero.

The last model parameter is the drain-to-source resistance (r_{ds}) which models the channel-length modulation and its effect on the drain current due to changes in $V_{DS} \cdot r_{ds}$ can be calculated using Eq.(2.6).

$$\frac{1}{r_{ds}} = g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = \lambda\left(\frac{\mu_n C_{ox}}{2}\right)\left(\frac{W}{L}(V_{GS} - V_{Tn})^2\right) = \lambda I_{DS} \tag{2.14}$$

and finally

$$r_{ds} = \frac{1}{\lambda I_{DS}} \tag{2.15}$$

High-Frequency Small-Signal Model:

Charge effect of a MOS transistor in saturation region is modeled by several capacitors shown in the cross-section of device is shown in Fig.2.7

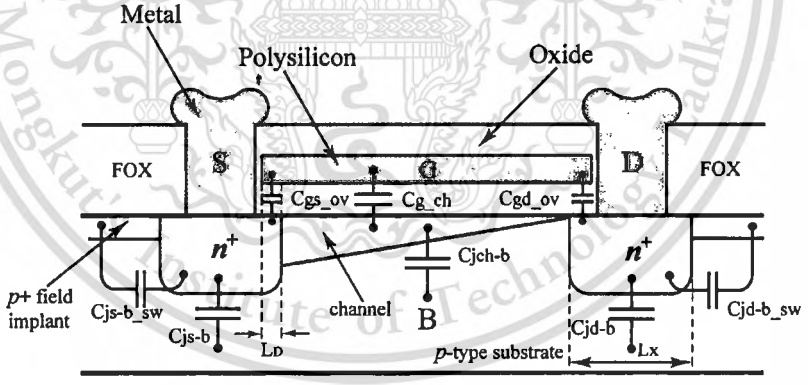


Figure 2.7. NMOS capacitive model

The largest contribution to device charge profile is from channel charges. Channel charges can be modeled by the capacitive effect between gate and channel that is electrically connected to the source. Gate-to-source capacitance due to channel C_{gs_ch} can be approximated as a linear capacitor that depends on the oxide thickness as well as on the device area and its value is given by

$$C_{gs\_ch} = \frac{2}{3} WLC_{ox} \tag{2.16}$$

During fabrication process, the doping profiles of n^+ regions spread creating an unavoidable overlap between gates and n^+ source and drain regions. Overlap between the gate and the source junction gives rise to fringing capacitance. For accurate modeling of gate-to-source capacitance, an additional term accounting for fringing effect should be added to Eq.(2.16). The additional capacitance due to overlap (C_{gs_ov}) with L_D as the overlap diffusion length and the total gate-to-source capacitance (C_{gs}) are given by

$$C_{gs\_ov} = WL_D C_{ox} \tag{2.17}$$

$$C_{gs} = C_{gs\_ch} + C_{gs\_ov} = W(\frac{2}{3}L + L_D)C_{ox} \tag{2.18}$$

The second largest capacitive contribution to the device model is introduced by the source-bulk charge density. Source-to-bulk capacitance (C_{sb}) consists of depletion capacitance contributed by three reverse biased *pn* regions formed between source and bulk, channel and bulk (as channel is connected to source), and source sidewall and bulk.

Depletion capacitance between n^+ sources with area WL_x (L_x is the length of n^+ region) and bulk is given by

$$C_{sb\_b} = WL_x C_{js} \tag{2.19}$$

Depletion capacitance between channel and bulk is given by

$$C_{sb\_ch} = WLC_{js} \tag{2.20}$$

C_{js} is the depletion capacitance per unit area of the source junction, given by

$$C_{js} = \frac{C_{j0}}{\sqrt{1 + \frac{V_{SB}}{\phi_0}}} \tag{2.21}$$

Due to presence of a highly p^+ doped region (field implant) under the thick field oxide (FOX) to prevent the leakage current from flowing between two adjacent transistors, a reverse biased *pn* junction is created between sidewalls of source region and field-implant which gives rise to source-bulk sidewall capacitance (C_{sb_sw}). Contribution from (C_{sb_sw}) can be large if the field implant is heavily doped. The expression of (C_{sb_sw}) is given by

$$C_{sb\_sw} = (W + 2L_x)C_{jsw} \tag{2.22}$$

where

$(W + 2L_x)$: represents the perimeter of source region, excluding the side adjacent to the channel

C_{js_sw} : represents the sidewall depletion capacitance per unit length of source junction and is given by

$$C_{js\_sw} = \frac{C_{js\_sw0}}{\sqrt{1 + \frac{V_{SB}}{\phi_0}}} \tag{2.23}$$

Therefore, using Eqs, (2.19), (2.20) and (2.22), total source-to-bulk capacitance can be expressed as

$$C_{sb} = C_{sb\_b} + C_{sb\_ch} + C_{sb\_sw} = W(L + L_x)C_{js} + (W + 2L_x)C_{jsw} \tag{2.24}$$

At the drain, since no channel is connected to it, so the only charge contribution to gate-to-drain capacitance is due to overlap of diffusion length (L_D) with the gate. Therefore, gate-to-drain capacitance (C_{gd}) can be modeled by expression

$$C_{gd} = C_{gd\_ov} = WL_DC_{ox} \tag{2.25}$$

The last capacitor to be modeled is the drain-to-bulk capacitance (C_{db}). Due to absence of channel, C_{db} is only contributed by depletion capacitance of drain-to-bulk *pn* junction (C_{db_b}) and drain-to-bulk sidewall capacitance (C_{db_sw}).

$$C_{db\_b} = WL_x C_{jd} \tag{2.26}$$

$$C_{db\_sw} = (W + 2L_x)C_{jd\_sw} \tag{2.27}$$

$$C_{jd} = \frac{C_{j0}}{\sqrt{1 + \frac{V_{DB}}{\phi_0}}} \tag{2.28}$$

$$C_{jd\_sw} = \frac{C_{jd\_sw0}}{\sqrt{1 + \frac{V_{DB}}{\phi_0}}} \tag{2.29}$$

$$C_{db} = C_{db\_b} + C_{db\_sw} = WL_x C_{jd} + (W + 2L_x)C_{jd\_sw} \tag{2.30}$$

2.2.4.2 Small-Signal Modeling in the Triode Region

Low-Frequency Small-Signal Model:

In triode region, MOS device's small-signal behavior is modeled as a resistor which can expressed using Eq.(2.2) as,

$$\frac{1}{r_{ds}} = \frac{\partial I_{DS}}{\partial V_{DS}} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{Tn} - V_{DS}) \tag{2.31}$$

If V_{DS} is small, Eq.(2.31) can also be approximated as

$$r_{ds} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{Tn})} \tag{2.32}$$

High-Frequency Small-Signal Model:

The high frequency model will be same as for saturation region because in the triode region the drain current is also dependent on V_{GS} Eq.(2.2), so the transistor has transconductance equal to the inverse of the triode linear resistance i.e. $g_m = 1/r_{ds}$. Therefore simplified high-frequency model for small V_{DS} values is shown in Fig.2.8.

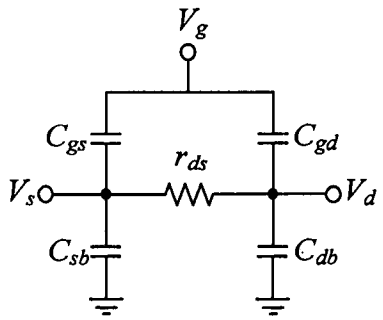


Figure 2.8. NMOS triode model

The accurate high-frequency model for MOS device operating in triode region is difficult as the channel is directly connected to both the source and the drain region. To approximate the gate-to-source and the gate-to-drain capacitance, it is assumed that the channel capacitance is divided equally between source and drain nodes. The fringing capacitance due gate-to-junction overlap will be same as defined for saturated region. Therefore, the total gate-to-source capacitance (C_{gs}) and the total gate-to-drain capacitance (C_{gd}) in the triode region are given by

$$C_{gs} = C_{gd} = W(\frac{L}{2} + L_D)C_{ox} \tag{2.33}$$

Eq.(2.33) shows that C_{gs} and C_{gd} are large compared to saturation region capacitances. The channel-to-substrate capacitance has also been divided in half and shared between the source and drain junctions. The source-to-bulk capacitance and the drain-to-bulk capacitance definitions in the triode region are same as defined for saturation region. The only difference is that now both capacitances have channel-to-bulk capacitance contribution.

$$C_{sb} = W(\frac{L}{2} + L_x)C_{js} + (W + 2L_x)C_{jsw} \tag{2.34}$$

$$C_{js} = \frac{C_{j0}}{\sqrt{1 + \frac{V_{SB}}{\phi_0}}} \tag{2.35}$$

$$C_{js\_sw} = \frac{C_{js\_sw0}}{\sqrt{1 + \frac{V_{SB}}{\phi_0}}} \tag{2.36}$$

$$C_{db} = W(\frac{L}{2} + L_x)C_{jd} + (W + 2L_x)C_{jd\_sw} \tag{2.37}$$

$$C_{jd} = \frac{C_{j0}}{\sqrt{1 + \frac{V_{DB}}{\phi_0}}} \tag{2.38}$$

$$C_{jd\_sw} = \frac{C_{jd\_sw0}}{\sqrt{1 + \frac{V_{DB}}{\phi_0}}} \tag{2.39}$$

The source-to-bulk capacitance is of same size as gate-to-source due to its large area and the sidewall capacitance.

2.2.4.3 Small-Signal Modeling in the Cutoff Region

In cutoff region ($V_{GS} \le V_{Tn}$), no channel is present to model at low frequency. At high frequencies, due to absence of channel, both C_{gs} and C_{gd} are represented by small overlap contribution.

$$C_{gs} = C_{gd} = WL_D C_{ox} \tag{2.40}$$

Source-to-bulk and drain-to-bulk capacitances are similar to those given by Eqs.(2.34, 2.37) with the difference that the channel does not make any contribution [5], therefore

$$C_{sb} = WL_x C_{js} + (W + 2L_x)C_{jsw} \tag{2.41}$$

$$C_{db} = WL_x C_{jd} + (W + 2L_x)C_{jd\_sw} \tag{2.42}$$

In cutoff region, gate-to-bulk capacitances come into play as shown in Fig.2.9. This capacitance is due to accumulation of charges near the oxide surface and highly dependent on gate voltage. For negative gate voltage, the capacitance between gate and bulk is defined as

$$C_{gb} = WLC_{ox} \tag{2.43}$$

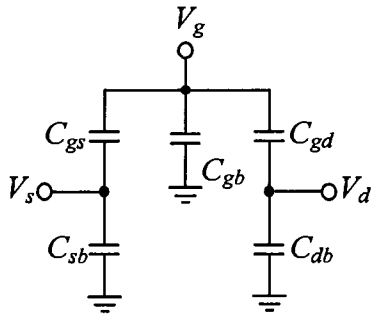


Figure 2.9. NMOS cutoff high frequency model

2.2.5 P-Channel MOS Transistor (PMOS)

In the preceding sections, all the analysis is performed for NMOS transistor. All the derived equations can also be used for PMOS transistor by placing a negative sign in front of every voltage variable. Thus V_{GS} becomes V_{SG}, V_{DS} becomes V_{SD}, V_{Tn} becomes $-V_{Tp}$ and so on. The condition required for conduction is now $V_{SG} > V_{Tp}$, where V_{Tp} is now a negative quantity for PMOS. The requirement on the source-drain voltage for a PMOS to be in active region is $V_{SD} > V_{SG} + V_{Tp}$. The equation for I_{SD}, in both regions (Eqs.(2.2, 2.4)), remain unchanged, because all voltage variables are squared, resulting in positive hole current flow from the source to the drain in PMOS.

2.3 Historical Background of Current Conveyors

To overcome the certain limitations of op-amp in analog circuits, many new building blocks that are suitable for current-mode circuits have been introduced. Among these current conveyors are very famous.

The concept of the current conveyor was first presented in 1968 [12] and further developed to a second generation current conveyor in 1970 [13]. The current conveyor is intended as a general building block as with the op-amp. On the other hand, neither of these building blocks became popular as a consequence of the introduction of the integrated op-amp at the time. Because of the op-amp concept has been current since the late 1940's, it is difficult to get any other similar concept widely accepted. Additionally, integrated current conveyors were difficult to realize due to the lack of high performance integration technologies in the 1970's. During the 1980's, research societies started to notice that the voltage op-amp is not necessarily the best solution to all analog circuit design problems. Voltage op-amps do not perform well in

applications where a current output signal is needed and consequently there is an application field for current conveyor circuits. Since current conveyors operate without any global feedback, a different high frequency behavior compared to op-amp circuits results.

In many applications, only one of the virtual grounds in the input terminals of the first generation current conveyor is used and the unused terminal must be grounded or otherwise connected to a suitable potential. This grounding must be done carefully since a poorly grounded input terminal may cause unwanted negative impedance at the other input terminal. Moreover, for many applications a high impedance input terminal is preferable. For these reasons, the second generation current conveyor was developed. It has one high and one low impedance input rather than the two low impedance inputs of the first generation current conveyor. Yet another current conveyor was proposed in 1995 [14]. The operation of the third generation current conveyor is similar to that of the first generation current conveyor, with the exception that the currents in the input terminals flow in opposite directions. This current conveyor can be used as an active current probe.

Furthermore, a commercial product, the current feedback operational amplifier, became available. The high slew rate and wide bandwidth of this amplifier resulted in its popularity in video amplifier applications. It provides the advantage of having constant bandwidth irrespective of the gain as oppose to classical op-amp. It is also used in voltage mode operation as well as in current mode. The current feedback operational amplifier is in effect a positive second generation current conveyor with an additional voltage buffer at the conveyor current output. The current at the inverting input of the current feedback operational amplifier is transferred to the high impedance current conveyor output, causing a large change in output voltage.

There are some other additional types of building blocks as the variations of the current conveyors such as; differential voltage current conveyor (DVCC) [30], differential difference current conveyor (DDCC) [15], inverting current conveyor, operational floating conveyor, current differencing buffered amplifier (CDBA) [31], etc. Most of these elements are unity gain amplifiers. There are many applications of these building blocks both in voltage mode and current mode operation.

A new CMOS realization of differential difference current conveyor (DDCC) is presented in [16]. The negative feedback action is introduced by using a current mirror to reduce channel length modulation effect of MOS transistors. Furthermore, the circuit is insensitive to the threshold voltage variation caused by the body effect of MOS transistors. Comparing with

conventional design, the DDCC has the advantages of both the CCII and the differential difference amplifier (DDA) such as high input impedance, less harmonic distortion and larger linear range. Therefore, apart from above advantages following are the driving force behind development of the analog signal processing applications

2.3.1 Classification of Current Conveyors

A CC is a three or more terminals (X, Y and Z) network. The commonly used block representation of a CC is shown in Fig. 2.10 [14], whose input-output relationship is given by

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & A & 0 \\ B & R_X & 0 \\ 0 & C & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \tag{2.44}$$

where A, B, C assume a value either 1, 0 or –1 and R_X is the intrinsic resistance offered by the terminal X to the input currents. For an ideal CC $(v_X = v_Y)$ and the input resistance (R_X) at terminal X is zero Eq.(2.44). But in practical CCs, R_X is a nonzero positive value. So the equivalent symbol of a CC should include R_X in its representation and the popular CC symbol is shown in Fig. 2.10. The equivalent circuits are used to analyze the complex circuits. One can understand the circuit operation better when the complex structures are simplified using equivalent circuits. For an analog circuit designer precise equivalent models of devices are essential for getting the near exact circuit performance and the one such model is given in reference [2].

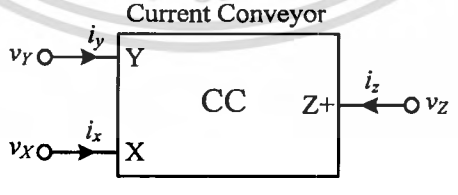


Figure 2.10. Current conveyor symbol

There are several schemes for classification of CCs. Most common techniques among them are based on the characteristics of its terminals X, Y and Z. CCs have also been classified similar to power amplifiers based on the quiescent current flow.

2.3.1.1 Terminal -Y Based Classification

Terminal Y is used as input for voltage signals and it should not load the input voltage source by drawing current. But in some applications, it is desirable to draw currents from the input voltage source.

When terminal Y draws a current equal to the current injected at terminal X, $A = 1$ according to Eq.(2.44), this configuration is termed as first generation current conveyor. When terminal Y draws zero current ($A = 0$), it is second generation current conveyor.

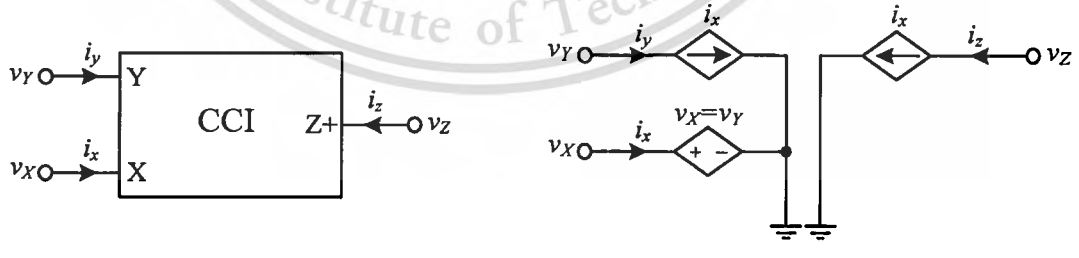
Similarly, when this current equals to the current injected at terminal X but of opposite polarity, the configuration is known as third generation current conveyor for which $A = -1$ [32]-[34].

- **First Generation Current Conveyors - CCI**

The first generation current conveyors are three terminal networks with terminals X, Y and Z as represented in Fig.2.11. The network of the first generation current conveyor CCI has been formulated in a matrix form as follows [12]:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \tag{2.45}$$

The first generation current conveyor CCI forces both the currents and the voltages in terminals X and Y to be equal and a replica of the currents is mirrored (or conveyed) to the output terminal Z.



(a) (b)

Figure 2.11. (a) The first generation current conveyor symbol (b) Equivalent circuit of CCI

- **Second Generation Current Conveyors - CCII**

For many applications a high impedance input terminal is preferable and to increase the versatility of the current conveyor, which no current flows in terminal Y. For these reasons,

the second generation current conveyor was developed. It has one high and one low impedance input rather than the two low impedance inputs of the CCI [13]. This building block has since proven be more useful than CCI. CCII can be described by following matrix:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \tag{2.46}$$

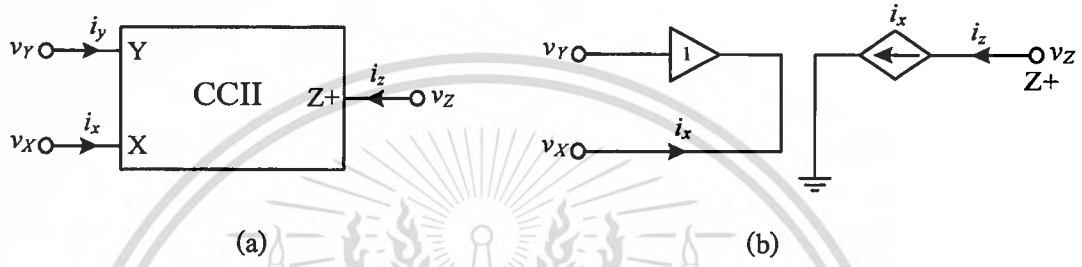


Figure 2.12. (a) The second generation current conveyor symbol (b) Equivalent circuit of CCII

The current flowing into (CCII+) or out of (CCII–) the Z node is proportional to the current flowing into the X node. The second generation current conveyor is a principle of voltage-follower with a voltage input Y node and a voltage output X node, and a current-follower (or current-inverter) with a current input X and a current output Z connected together Fig.2.12. CCII has proven to be by far the more useful of the current conveyor family types. Wide range of applications was published. It's very suitable building block for design of the analog signal processing applications. In the last decade the numbers of high-speed and wide-range op-amps are based on current conveyor structure. And also for low voltage applications CCII is starting to be very powerful building block.

- **Third Generation Current Conveyors - CCIII**

Yet another current conveyor was proposed in 1995 [14]. The network of this third generation current conveyor CCIII is formulated in a matrix form as follows. This type is similar to CCI, there is opposite current transfer between terminals X and Y. Matrix described this CC type is following:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \tag{2.47}$$

The input current flows into the terminal Y and out from the terminal X, one might think that a differential current input could be realized with this amplifier. However, the CCIII has high input impedance with common-mode current signals, i.e. identical currents are fed both to terminals Y and X. Therefore common-mode currents can push the input terminals out from the proper operation range. This current conveyor can be used as an active current probe. Fig.2.13 depicts the symbol and equivalent circuit of CCIII.

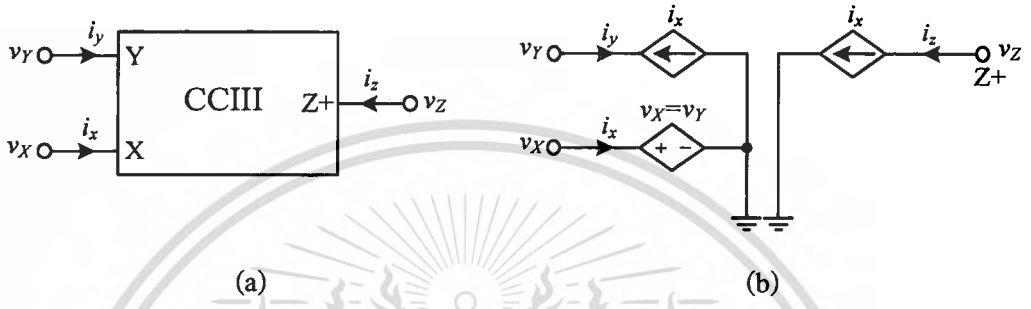


Figure 2.13. (a) The third generation current conveyor symbol (b) Equivalent circuit of CCIII

2.3.1.2 Terminal - X Based Classification

For voltage signals, terminal Y serves as input terminal and now the terminal X serves as output terminal. The output voltage at terminal X can either have same polarity as that of the input voltage (v_Y), in this case current conveyor is called as non-inverting CC. or that of opposite polarity, are termed as inverting CCs [35].

The inverting second generation current conveyor "positive" (ICCII+), has the following terminal relation between terminal voltages and currents:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \tag{2.48}$$

2.3.1.3 Terminal - Z Based Classification

Terminal Z is the current output terminal and usually, the magnitude of the output current at terminal Z equals to the magnitude of the current injected into terminal X. In some cases, however, this amplitude may be scaled version (generally up scaled) of the input current and also the direction of the current may be same or opposite to that of the current in terminal X. CC with positive current output is termed as CC+ and with negative output currents as CC– [36].

A CC can have two or more output terminals, which can independently sink or source currents. Such a CC is known as multi-terminal CC. A multi-terminal CC with both types of output terminals (positive as well as negative), is known as composite terminal CCII.

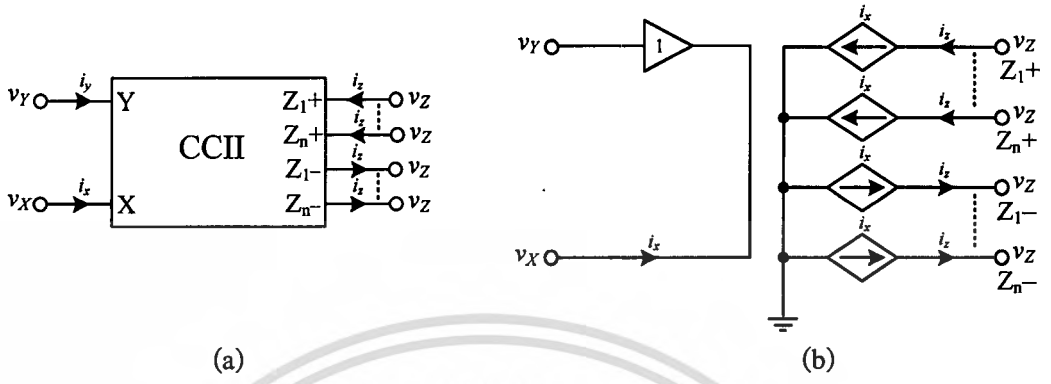


Figure 2.14. Multi-terminal CCII basic block (a) Symbol (b) Equivalent circuit

2.3.1.4 Quiescent Current Based Classification

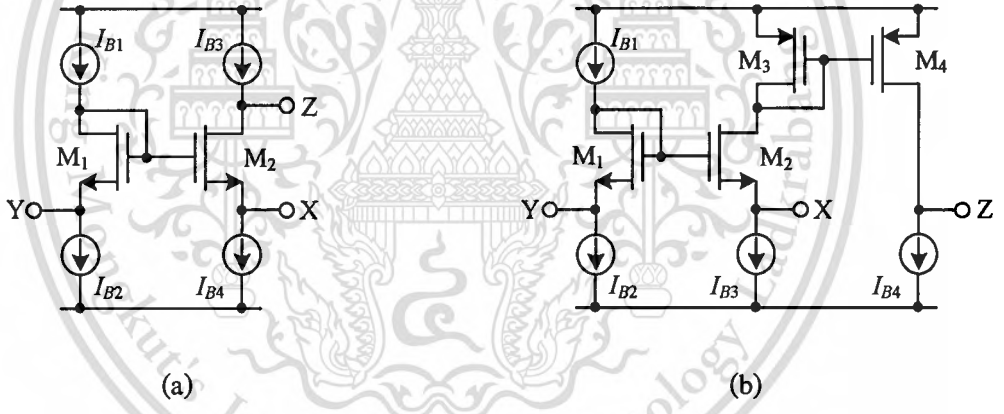


Figure 2.15. Class A CCIIs (a) CCII– (b) CCII+

Similar to the classification of power amplifiers, CCs have been classified as Class A shown in Fig.2.15, Class B which rarely uses due to strongly nonlinear characteristic and Class AB mode CCs shown in Fig.2.16. In a class A CC, a quiescent current flows throughout the circuit operation. The bandwidth of this CC is high. Contrary to this, in class B CC, current flows through the circuit only when the input signal is present. Such a circuit consumes negligible power in standby mode, but its bandwidth is much smaller compared to class A CCs. Class AB CCs have emerged as the best alternative, where a small amount of quiescent current flows throughout the circuit operations. Class AB CCs have higher bandwidth than that of a class B CCs and the power consumption is much less than a class A CC [37]-[39].

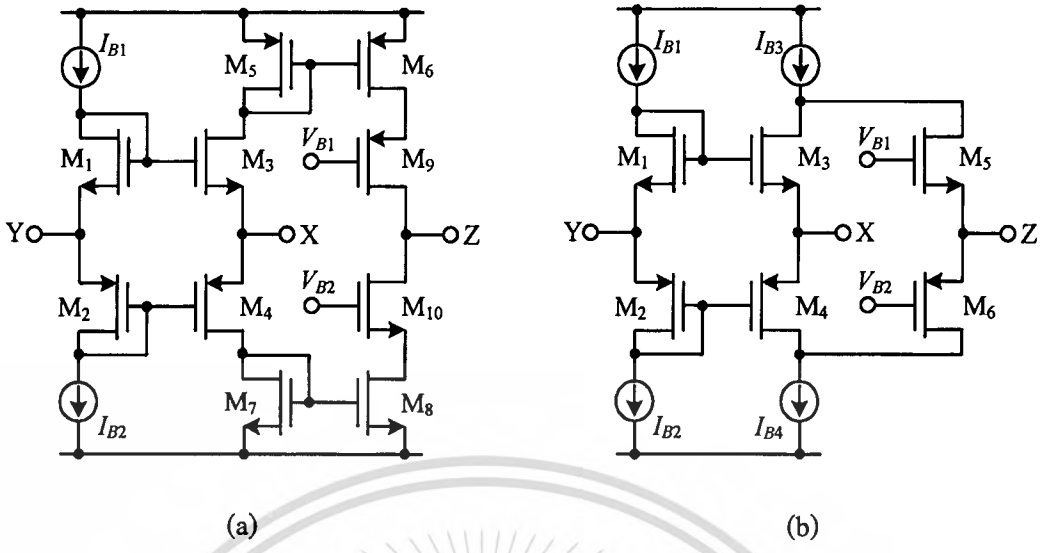


Figure 2.16. Class AB CCIIs (a) CCII+ (b) CCII–

2.3.1.5 Other Current Conveyor Configurations

Other CC configurations are electronically controlled current conveyors (ECCII),

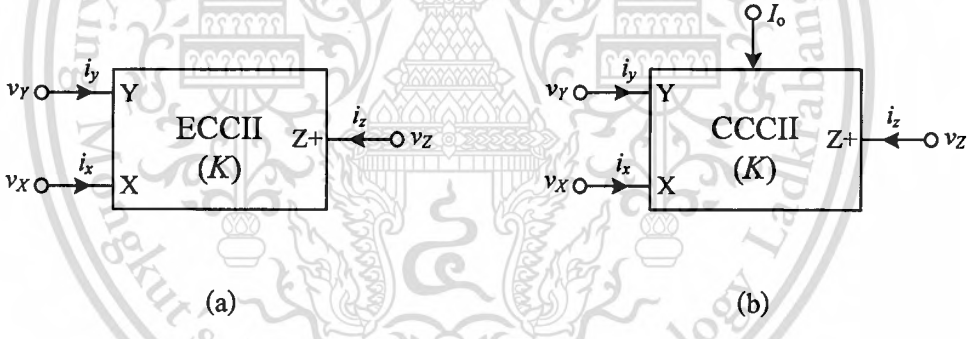


Figure 2.17. (a) ECCII basic block (b) CCCII basic block

If i_Z is designed K times higher with respect to i_X, the new block so implemented is named Electronically Controlled Current Conveyor (ECCII) [40] as shown in Fig.2.17 (a). The designer can adjust the value of the X node parasitic impedance, the current I_o may control the biasing of the output stage, so modifying the parasitic resistance R_X, in Current Controlled Current Conveyor, or (CCCII) [41]-[42] as shown in Fig.2.17 (b). Deferential approach, leads to several circuit solutions such as differential difference current conveyor (DDCC), the DDCC is a powerful current mode building block with properties that make it ideal for designing all MOS analog circuits which can be integrated on a single chip. The detail of DDCC-based analog signal processing applications will be discussed in the next chapter.

2.3.2 Advantages of Current Conveyor

• **Higher voltage gain**: The current conveyor circuit can provide a higher voltage gain over a larger signal bandwidth under small or large signal conditions. Successful in the current conveyors have been extremely successful in the development of an instrumentation amplifier which does not depends critically on the matching of external components, instead depends only on the absolute value of a single component.

• **More accuracy**: Current Conveyor-based implementations offer improved performance to the voltage op amp based implementations in terms of accuracy, and bandwidth.

• **Larger bandwidths wider dynamic ranges**: The current conveyor attributed to the bandwidths and wider dynamic ranges obtain able compared to the classical operational amplifier based circuits.

• **Larger linearity**: The current conveyor-based implementations have larger linearity as compare to voltage mode circuit.

• **Higher slew rate**: Slew rate of current conveyor is more as compare to voltage mode circuit this advantage is very useful in analog signal processing applications.

2.3.3 Applications of Current Conveyor

Because of the separate voltage and current inputs both voltage and current amplifiers can easily be realized with the current conveyors and the gain can be set by resistor ratios as in operational amplifier circuits. Signal processing in current conveyor circuits is based on voltage-to-current and current-to-voltage conversions and on signal buffering by voltage and current buffers. Because there is typically no feedback in current conveyor circuits, wide bandwidth operation without any slewing at large signal amplitudes is achieved. The conventional applications of current conveyors include amplifiers, oscillators, filters, wave shaping circuits, analog computers etc. [37]. Low-voltage and low-power architectures of current conveyors are particularly suitable in the design of analog signal processing systems, which examples of analog computation elements based on current conveyor circuits as shown in [13].

2.4 Conclusion

Literature review and background theory contained in this chapter focuses on an analog signals processing. For the purpose of this review, a literature survey has been carried out on

current conveyors background of the first, second and third generation current conveyors as well as the classification of them. Then a new active building block called a "Differential Difference Current Conveyor (DDCC)" has been focused. It should be noted that the DDCC is a circuit similar to a Differential difference amplifier (DDA) at the input side and a CCII at the output side. Consequently, one is able to design DDCC-based circuits which combine the properties of DDAs, such as high input impedance, low output impedance, with the higher usable gain, accuracy and bandwidth of the CCII. Moreover, this chapter provided an overview of CMOS technology and it was seen that the current conveyor can be realized as a CMOS analog integrated circuits, it is very suitable to use in a current-mode for analog signal processing.

CHAPTER 3

CMOS REALIZATION OF DDCC

3.1 Introduction of Differential Difference Current Conveyor (DDCC)

3.1.1 Historical Background of DDCC

Differential Difference Current Conveyor (DDCC) was proposed by W. Chiu, S. I. Liu, H. W. Tsao and J. J. Chen in 1996 [15]. Since CCII was proposed in 1970 [13], it has proven to be a versatile building block and the invention of the powerful CCII resulted in many applications of analog signal processing circuits to be constructed based on CCII. In 1987, a new building block called differential-difference amplifier (DDA) was proposed by E. Sackinger and W. Guggenbuhl, 1987 [17]. Taking advantage of the high input impedance and the arithmetic operation capability, designers have been able to construct new applications with a reduced number of components by using DDA. The advantages of CCII and DDA are combined to build the new versatile block called DDCC.

The DDA, widely used in op-amp circuits, is a fundamental amplifier circuit applied to integrated circuits, which formed by at least two BJT or MOS differential pairs, has several advantages, such as a reduction of the number of passive devices requiring matching, and a simplified design process. In view of current technology, the conventional DDA still has many drawbacks and requires further improvement. First, like the conventional op-amp circuit, performance of the DDA is limited by its finite gain-bandwidth product, so that it is unsuitable for application in high frequency circuits. However, a device call a current conveyor is quite appropriate for use in high frequency circuit. The principle and performance of the current conveyor has been disclosed in U.S. Pat. No.5,124,666 [43].

In view of the disadvantages of the conventional technology described above, W. Chiu et. al. [15] provides a novel device, a differential difference current conveyor, to solve these problems. The objective of the present is to provide a device, which has a superior finite gain-bandwidth product, and as a result, is appropriate for application in high frequency circuits.

Recently, Jianping Hu et al. [16] proposed a new CMOS realization of DDCC. The negative feedback action is introduced by using a current mirror to reduce channel length modulation effect of MOS transistors. Furthermore, the circuit is insensitive to the threshold

voltage variation caused by the body effect of MOS transistors. Comparing with conventional design, the proposed DDCC circuit has less harmonic distortion and larger linear range.

The differential difference current conveyor (DDCC) is an extremely powerful analog building block, combining voltage and current-mode capability. It has proved to be functionally flexible and versatile, rapidly gaining acceptance as a practical device with a wide range of high performance circuit and system applications [18]-[23].

3.1.2 Black Box Representation of DDCC

DDCC is a five terminal device as given in Fig.3.1. DDCC was designed to have three distinct infinite impedance input terminals (Y_1, Y_2 and Y_3) which allows no current flowing through Y terminals. X terminal has the equal potential to the potential difference between terminals Y_1 and Y_2 plus the potential of Y_3 [15].

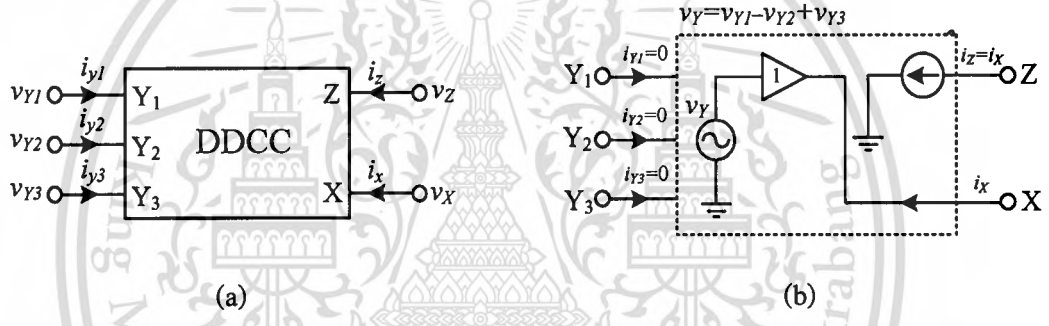


Figure 3.1. Black box representation of DDCC (a) Electrical symbol (b) Equivalent circuit

Relying on the common current conveying characteristic, current flowing through terminal X is conveyed to the Z terminal. DDCC is named as either DDCC+ or DDCC– depending on the polarity of the current flowing through Z terminal. In DDCC+, the current flowing through terminal Z has the same polarity with the current flowing through X terminal, whereas in DDCC-current is conveyed from X terminal to Z terminal with an inverse polarity. The hybrid matrix equation of DDCC is given in Eq.(3.1) [15].

$$\begin{bmatrix} v_X \\ i_{Y1} \\ i_{Y2} \\ i_{Y3} \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \pm 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_X \\ v_{Y1} \\ v_{Y2} \\ v_{Y3} \\ v_Z \end{bmatrix} \tag{3.1}$$

In 2004, a novel CMOS implementation of DDDC was proposed. (Jianping,Yinshui & Tiefeng, 2004) [16]. The implementation covers the current conveying functionality of both DDCC– and DDCC+ devices as the proposed CMOS implementation has two high impedance output terminals.

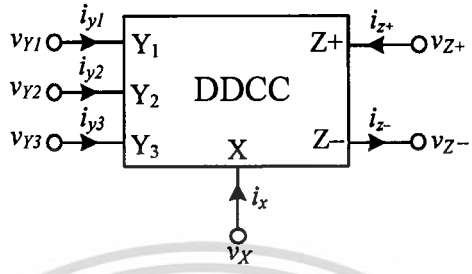


Figure 3.2. Symbol of new DDCC [16]

The new DDCC is a six-terminal building block as shown in Fig.3.2. It has three voltage input terminals: Y_1, Y_2 and Y_3, which have high input impedance. Terminal X is a low impedance current input terminal. There are two high impedance current output terminals: Z_1 and Z_2. The input-output characteristic of the DDCC is defined as [16].

The output currents (i_{Z+} and i_{Z-}) follow the input current through terminal X. i_{Z+} has the same polarity as i_X, and i_{Z-} is in the opposite polarity as i_X. The voltage of X terminal is related by the three input voltage: $v_X = v_{Y1} - v_{Y2} + v_{Y3}$. Table 3.1 summarizes the impedances at each terminal.

Table 3.1 Summary of DDCC characteristics

DDCC Node	Ideal Impedance	Realizable Impedance
X	0	LOW
Y	∞	HIGH
Z	∞	HIGH

3.1.3 CMOS Realization of DDCC

Conventional CMOS realization of DDCC is given in Fig.3.3 (Chiu, Liu, Tsao & Chen, 1996) [15]. The circuit structure of this CMOS DDCC is similar to that of the CCII+ in [25] and to the DDA realization in [17]. All MOS transistors operate in the saturation, and their bulk is connected to the appropriate positive or negative supply rail. The input transconductance

elements are realized with two differential stages (M_1 and M_2, M_3 and M_4). The high-gain stage is composed of a current mirror (M_5 and M_6) which converts the differential current to a single-ended output current (M_7). The output voltage of this amplifier can be expressed as

$$v_X = A_o\left[(v_{Y1} - v_{Y2}) - (v_{G3} - v_{Y3})\right] \tag{3.2}$$

where A_o is the open-loop gain of the amplifier and v_{G3} is the gate of M_3

Negative feedback was then applied from the output node of the gain stage (node X) to the input node (gate of M_3). If the open-loop gain of the amplifier is much larger than one, the relationship between the four input terminal voltages can be obtained as

$$v_X = \frac{A_o}{A_o + 1}(v_{Y1} - v_{Y2} + v_{Y3}) \cong v_{Y1} - v_{Y2} + v_{Y3} \tag{3.3}$$

The output terminal Z is constituted with MOS transistor M_{12} and the MOS transistor M_8 which duplicates the current of the M_7. It can be clearly seen that both i_X and i_Z flow simultaneously towards or away from the DDCC.

In order to extract the detail of DDCC, we will be discussed the operation of differential difference amplifier (DDA) be clarify to explain before, because the DDCC has the advantages of both the CCII and the DDA (such as high input impedance and arithmetic operation capability) [17].

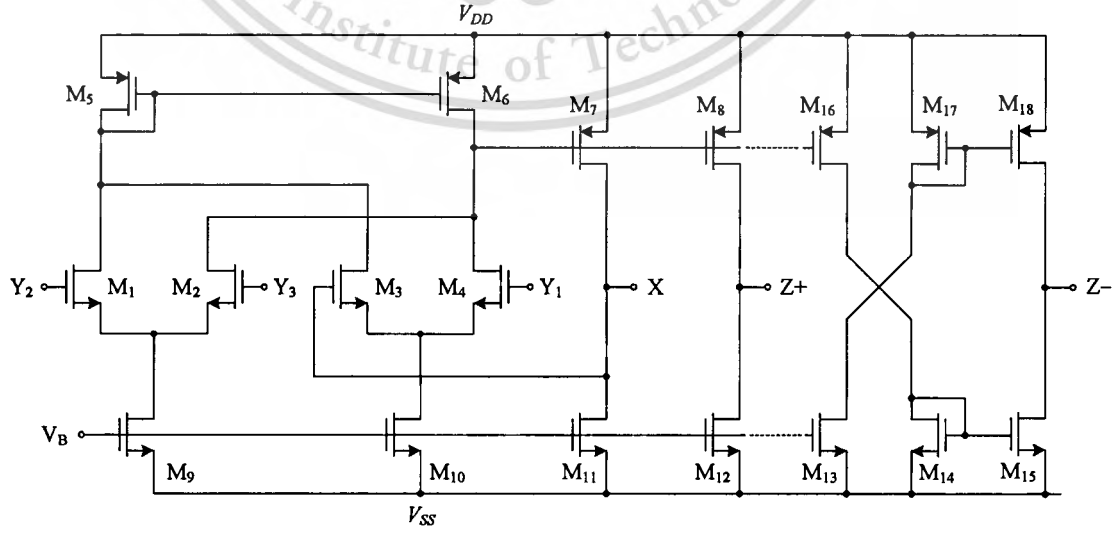


Figure 3.3. The CMOS realization of DDCC [16]

3.1.3.1 The CMOS Differential Difference Amplifier

The differential difference amplifier (DDA), whose symbol and basic block diagram is shown in Fig.3.4. The DDA is an extension to the concept of the op-amp. The main difference is that instead of two single-ended inputs as is the case in op-amps, it has two differential input terminals $(V_{pp} - V_{pn})$ and $(V_{np} - V_{nn})$. Therefore, the output of the DDA can be written as [17].

$$V_o = A_o\left[(V_{pp} - V_{pn}) - (V_{np} - V_{nn})\right] \tag{3.4}$$

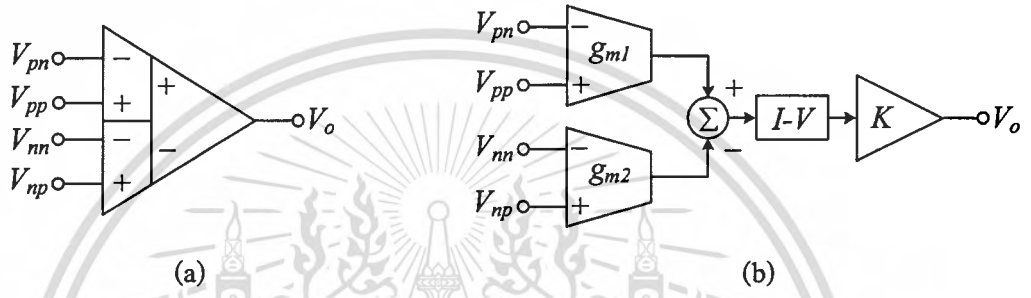


Figure 3.4. Building box representation of DDA (a) Electrical symbol (b) Equivalent circuit

where A_o is the open-loop gain of the DDA. When a negative feedback is introduced, i.e., to V_{pn} and/or V_{np}, which appear in Eq.(3.5) with a negative sign, the following expression is obtained [44]:

$$V_{pp} - V_{pn} = V_{np} - V_{nn} \quad \text{with} \quad A_o \to \infty \tag{3.5}$$

For a finite open-loop gain A_o, the difference between the two differential voltages increase as A_o decreases. Therefore, the open-loop gain should be as large as possible in order to achieve high-performance operation. According to Eq.(3.5), some interesting circuits can be realized with the DDA and without using components or matched components external to the DDA.

The definition can be described by specifying the respective transformation matrix [17]:

$$\begin{bmatrix} V_d \\ V_{cp} \\ V_{cn} \\ V_{cd} \end{bmatrix} = \begin{bmatrix} 1 & -1 & -1 & 1 \\ 1/2 & 1/2 & 0 & 0 \\ 0 & 0 & 1/2 & 1/2 \\ 1/2 & -1/2 & 1/2 & -1/2 \end{bmatrix} \begin{bmatrix} V_{pp} \\ V_{pn} \\ V_{np} \\ V_{nn} \end{bmatrix} \tag{3.6}$$

While the first row describes the differential voltage V_d, the second, third, and fourth rows assigned to the common-mode voltages V_{cp}, V_{cn}, and V_{cd}, respectively, can be chosen arbitrarily to yield any regular transformation matrix. In Eq.(3.6) the definition of the common-mode voltages is given in order to be compatible with the definition used for the normal op-amp[45].

The nonideal op-amp is usually characterized by the parameters of its linear model [45]. This means that the nonlinear relation between the input voltage (differential-V_d and common-mode V_{cm} voltage) and the output voltage V_o.

$$V_o = F(V_d, V_{cm}) \tag{3.7}$$

is linearized at the bias point $V_o = 0$ and $V_{cm} = V_{cm0}$:

$$V_o = A_d\left[(V_d - V_{off}) + \frac{1}{CMRR}(V_{cm} - V_{cm0})\right] \tag{3.8}$$

Eq.(3.8) contains three well-known parameters: differential gain A_d, offset voltage V_{off}, and common-mode rejection CMRR. All three parameters depend on the bias point, i.e., V_{cm0}. (Note: the CMRR definition given here has a sign, in contrast to the standard definition which uses only the absolute value [45].)

This procedure is now extended to four inputs in a straightforward manner. The nonlinear function

$$V_o = F(V_d, V_{cp}, V_{cn}, V_{cd}) \tag{3.9}$$

is linearized around the point $V_o = 0, V_{cp} = V_{cp0}, V_{cn} = V_{cn0}, V_{cd} = V_{cd0}$. This yields

$$\begin{aligned} V_o = A_d\Bigg[&(V_d - V_{off}) + \frac{1}{CMRR_p}(V_{cp} - V_{cp0}) \\ &+ \frac{1}{CMRR_n}(V_{cn} - V_{cn0}) \\ &+ \frac{1}{CMRR_d}(V_{cd} - V_{cd0})\Bigg] \end{aligned} \tag{3.10}$$

The meaning of A_d and V_{off} is analog to the corresponding quantities of the op-amp, but here are three CMRR's and all parameter (A_d, V_{off}, $CMRR_p$, $CMRR_n$, and $CMRR_d$) depend on all common-mode voltages (V_{cp0}, V_{cn0}, and V_{cd0}). The *p*-and *n*-common-mode rejection rations ($CMRR_p$, $CMRR_n$) describe the effect of the common-mode voltages at the two input terminals, whereas the *d*-common-mode rejection ratio ($CMRR_d$), not known from the ordinary op-amp, measures the effect of equal floating voltages at the two input terminals.

A further operating parameter which must be introduced for the understanding of the later sections is the nonlinearity NL. Its definition is given in Eq.(3.11):

$$NL = \frac{\max\left|(V_{pp} - V_{pn}) - (V_{np} - V_{nn})\right|}{V_{fs}}\Bigg|_{V_o=0},$$

$$\text{for } (V_{pp} - V_{pn}) = -V_{fs} \cdots V_{fs} \tag{3.11}$$

In words, the nonlinearity is the maximum deviation of the two terminal voltages over a given terminal voltage range [$-V_{fs}$ to V_{fs}] normalized to this range (always assuming an output voltage of zero). Using Eq.(3.10) and $V_d \ll V_{cd}$ the nonlinearity can be rewritten in terms of the offset voltage function:

$$NL = \frac{\max\left|V_{off}(V_{cp0}, V_{cn0}, V_{cd0})\right|}{V_{fs}},$$

$$\text{for } V_{cd0} = -V_{fs} \cdots V_{fs} \tag{3.12}$$

A simple circuit suitable for the analog processing has been discussion. Its simple implementation makes it suitable as a single universal building block or as part of a larger integrated circuit. Some nonidealities which limit its performance have been identified and treated mathematically. The DDA described in this section has a near relation to the operating of differential difference current conveyor (DDCC). This will be subject of DDCC future work [15]-[16].

3.1.3.2 DDCC Circuit Performance Analysis

The CMOS realization of DDCC is shown in Fig.3.3. The input stage is similar to the DDCC in [15]. Assuming that M_5 and M_6 are matched, the current mirror formed by transistor M_5

and M_6 forces the sum of drain currents of M_1 and M_4 to be equal to the sum of the drain currents of M_2 and M_3, hence

$$i_5 = i_6 = i_2 + i_4 = i_1 + i_3 \tag{3.13}$$

therefore,

$$i_1 - i_2 = i_4 - i_3 \tag{3.14}$$

Because the differential output current of the differential pair is a monotonous function of differential input current and input voltage, the following expression can be obtained

$$i_{Y1} = i_{Y2} = i_{Y3} = 0 \tag{3.15}$$

$$v_X = v_{Y1} - v_{Y2} + v_{Y3} \tag{3.16}$$

$$i_Z = \pm i_X \tag{3.17}$$

Except M_1-M_4, all the MOS transistors have sources that are connected to the positive or negative supply rail, thus there isn't threshold voltage variation caused by the body effect. Because the transistors (M_1 and M_2) have equal variation in the threshold voltage caused by the body effect, the threshold voltage variation can be canceled out. The same is true for the differential pair M_3 and M_4. Therefore, the circuit is insensitive to the threshold voltage variation caused by the body effect.

In the preceding analysis, we assumed that i_5 equals to i_6. If V_{D6} doesn't equals to V_{D5}, the channel length modulation effect of the MOS transistors will cause a current error. In the DDCC circuit, the transistors M_7 and M_{11} provide the necessary buffering action with a rail to rail swing capability. The X terminal current is then mirrored to the Z terminal by the action of transistors M_8, and M_{12}. The current mirror formed by M_{14} and M_{15} changes the direction of the output current at terminal Z– and hence, both the DDCC+ and DDCC– are realized simultaneously.

In the discussion so far, we have assumed that the current mirrors have unity gain, and MOS transistors are perfectly matched. However, in practical realizations, several nonidealities must be present. The major factors we will consider here are finite transconductance g_m of the MOS transistors, and transistor mismatch.

The relationship between v_{Y1}, v_{Y2}, v_{Y3} and v_X can be obtained using small-signal analysis. The CMOS realization of DDCC circuit in Fig.3.3 is replaced by appropriate equivalent circuits and node equations can be derived. To simplify discussion, the body effect has been neglected and the two differential pairs are assumed to be identical. Then, by solving the equations, can be expressed as

$$v_X \approx \frac{g_{m7}g_{meq}}{g_{m7}g_{meq} + (g_{d12} + g_{d34} + g_{d6})(g_{d7} + g_{dI})} \times (v_{Y1} - v_{Y2} + v_{Y3}) \tag{3.18}$$

with

$$g_{meq} = \frac{2g_{m1}g_{m2}}{g_{m1} + g_{m2}} = \frac{2g_{m3}g_{m4}}{g_{m3} + g_{m4}} \quad \text{and} \quad g_{dij} = \frac{2g_{di}g_{dj}}{g_{di} + g_{dj}}$$

where g_{di} and g_{mi} denote the drain conductance and transconductance of MOS transistor M_i, respectively, and g_{dI} is the drain conductance of the current source. The current source formed by transistors M_9, M_{10}, M_{11} and M_{12}. It is clear that the voltages at terminal Y_1, Y_2, and Y_3 will be accurately transferred to terminal X only if $g_{m7}g_{meq} \gg (g_{d12} + g_{d34} + g_{d6})(g_{d7} + g_{dI})$.

Similarly, the terminal impedance looking in to X can be derived by setting v_{Y1}, v_{Y2}, and v_{Y3} to zero, applying a test voltage v_X at node X, and calculating the current i_X. The resulting is

$$R_X \approx \frac{(g_{m3}+g_{m4})(g_{d12} + g_{d34}+g_{d6})}{2g_{m3}g_{m4}g_{m7}} \tag{3.19}$$

The terminal impedance at Z can be also derived as

$$R_Z \approx \frac{1}{g_{d8} + g_{dI}} \tag{3.20}$$

The resistance can be further increased if a Wilson current mirror or a cascade mirror is employed. For high-frequency operation, the major limitation is due to the stray capacitances at terminal X. The high-frequency response can be expressed in term of v_{Y1}, v_{Y2}, v_{Y3} and v_X as

$$\frac{v_X}{v_{Y1} - v_{Y2} + v_{Y3}} \approx \frac{g_{m7} g_{meq}}{g_{m7} g_{meq} + (g_{d12} + g_{d34} + g_{d6})(g_{d7} + g_{dl})} \frac{1}{\tau_1 s + 1} \tag{3.21}$$

with

$$\tau_1 = \left[C_{gs7} + C_{gs8} + C_{gd8}\left(1 + \frac{g_{m8}}{g_{dl} + g_{d8}}\right) + 2C_{gd6} \right] \times \left(\frac{1}{g_{d12} + g_{d34} + g_{d6}} \right) \tag{3.22}$$

where C_{gdi} and C_{gsi} are the gate-to-drain capacitance and gate-to-source capacitance o device M_i, respectively. The pole frequency is quite low and will be the dominant frequency limiting factor of the circuit.

The input offset voltage (V_{OS}) is defined as the differential input voltage required causing the voltage across a resistor between terminal X and ground to be exactly zero. Large signal analysis is performed to solve the node equations. Then the offset voltage can be obtained as

$$V_{OS} = (V_{T2} - V_{T1} = V_{T3} - V_{T4}) - \sqrt{\frac{I}{K_1 + K_2}}\left(\frac{K_2 - K_1}{K_2 + K_1}\right) - \sqrt{\frac{I}{K_3 + K_4}}\left(\frac{K_3 - K_4}{K_3 + K_4}\right) \tag{3.23}$$

where V_{Ti} and K_i are the threshold voltage and the transconductance parameter of the device M_i, respectively. The first term is due to the mismatch among the threshold voltages, which is bias-current independent and is a strong function of process cleanliness and uniformity. The second term is caused by geometrical mismatch and can be reduced by increasing (W/L) or reducing bias current. The input signal range is quite limited due to the use of simple differential pair as input stage; it can be improved by using the wide range linear $V - I$ converter as discussed in [44] or some other techniques.

3.1.3.3 Modeling of Non-Ideal DDCC

Taking the non-idealities of the DDCC into account, the relationship of the terminal voltages and current can be written as:

$$\begin{bmatrix} v_X \\ i_{Y1} \\ i_{Y2} \\ i_{Y3} \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & \alpha_1 & -\alpha_2 & \alpha_3 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \pm\beta & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_X \\ v_{Y1} \\ v_{Y2} \\ v_{Y3} \\ v_Z \end{bmatrix} \tag{3.24}$$

where α_1, α_2 and α_3 represent the frequency transfer functions of the internal voltage followers and β represent the frequency transfer function of the internal current follower of the DDCC. Then, $\alpha_1 = 1 - \varepsilon_{1v}$ and $\varepsilon_{1v}\left(|\varepsilon_{1v} \ll 1|\right)$ denotes the voltage tracking error from v_{Y1} terminal to v_X terminal of the DDCC, $\alpha_2 = 1 - \varepsilon_{2v}$ and $\varepsilon_{2v}\left(|\varepsilon_{2v} \ll 1|\right)$ denotes the voltage tracking error from v_{Y2} terminal to v_X terminal of the DDCC, $\alpha_3 = 1 - \varepsilon_{3v}$ and $\varepsilon_{3v}\left(|\varepsilon_{3v} \ll 1|\right)$ denotes the voltage tracking error from v_{Y3} terminal to v_X terminal of the DDCC, and $\beta = 1 - \varepsilon_i$ and $\varepsilon_i (\varepsilon_i \ll 1)$ denotes the output current tracking error of the DDCC from X to Z+ and Z– terminals respectively.

Eq.(3.1) have been realized by considering the ideal description of the DDCC. The Y_1, Y_2, Y_3 and Z terminals exhibit an infinite input resistance. Practically, when implementing the active element using transistors, these resistances assume some finite value depending on the device parameters. Similarly, the high frequency effects also need to be accounted by assuming capacitances at these terminals. The non-ideal DDCC symbol with various parasitic elements is shown in Fig.3.5. It is shown that X terminal exhibits low-value intrinsic serial resistance R_X, and Y_1, Y_2 and Y_3 terminals exhibit low-value capacitance C_{Y1}, C_{Y2} and C_{Y3} with high-value parasitic resistance R_{Y1}, R_{Y2} and R_{Y3}, respectively. The Z+ and Z– terminals exhibit high-value parasitic resistance R_Z in parallel with low-value capacitor C_Z.

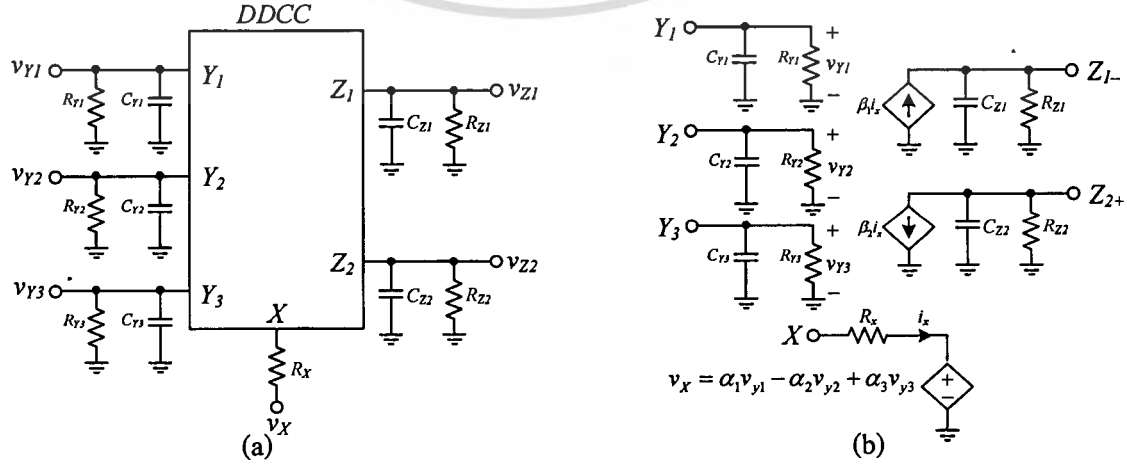


Figure 3.5. Non-ideal model of DDCC (a) Electrical symbol (b) Equivalent circuit

3.1.3.4 Relationship between Voltages of Terminals - X and Y_1, Y_2 and Y_3

The voltage at terminal X may be found by analyzing the differential difference part (comprising of MOS transistors M_1-M_7 and M_9-M_{11}) of the circuit in Fig.3.3 as follows:

$$v_X = \alpha_1 v_{Y1} - \alpha_2 v_{Y2} + \alpha_3 v_{Y3} + \varepsilon_v \tag{3.25}$$

where

$$\alpha_1 = \frac{1}{K}\left(g_{m4}g_{m5} + \frac{g_{m4}(g_{m3}g_{m6} - g_{m4}g_{m5})}{g_{m3} + g_{m4}} \right) \tag{3.26}$$

$$\alpha_2 = \frac{1}{K}\left(g_{m1}g_{m6} + \frac{g_{m1}(g_{m1}g_{m6} - g_{m2}g_{m5})}{g_{m1} + g_{m2}} \right) \tag{3.27}$$

$$\alpha_3 = \frac{1}{K}\left(g_{m2}g_{m5} + \frac{g_{m2}(g_{m1}g_{m6} - g_{m2}g_{m5})}{g_{m1} + g_{m2}} \right) \tag{3.28}$$

$$\varepsilon_v = -\frac{I_B}{K}\left(\frac{g_{m1}g_{m6} - g_{m2}g_{m5}}{g_{m1} + g_{m2}} + \frac{g_{m3}g_{m6} - g_{m4}g_{m5}}{g_{m3} + g_{m4}} \right) \tag{3.29}$$

$$K = g_{m3}g_{m6} - \frac{g_{m3}(g_{m3}g_{m4} - g_{m4}g_{m5})}{g_{m3} + g_{m4}} \tag{3.30}$$

and I_B represents current through MOS transistors M_i (i = 9, 10, 11, 12, 13) with matched transconductances $g_{m1} = g_{m2} = g_{m3} = g_{m4}$ and $g_{m5} = g_{m6}$; v_X is obtained as shown in Eq.(3.16).

3.1.3.5 Relationship between Currents of Terminals - Z+, Z– and X

The analysis of the portion of the circuit comprising of MOS transistors M_7 to M_{18} of the circuit in Fig.3.3 gives

$$i_{Z+} = \beta_1 i_X + \varepsilon_{i1} \tag{3.31}$$

$$i_{Z-} = \beta_2 i_X + \varepsilon_{i2} \tag{3.32}$$

where

$$\beta_1 = \frac{g_{m8}}{g_{m7}}, \quad \varepsilon_{i1} = \left(1 - \frac{g_{m8}}{g_{m7}}\right) I_B \tag{3.33}$$

$$\beta_2 = \frac{g_{m18}}{g_{m7}}, \quad \varepsilon_{i2} = \left(1 - \frac{g_{m18}}{g_{m7}}\right) I_B \tag{3.34}$$

For matched transconductances $g_{m7} = g_{m8} = g_{m18}$, the currents terminal are simplified to $i_{Z+} = i_{Z-} = i_X$.

3.1.3.6 Simulation Results of CMOS Realization of DDCC

The performance of the CMOS realization of DDCC in Fig. 3.3 was verified by performing PSpice simulation with supply voltage ±2.5 V using 0.5μm standard CMOS technology from MIETEC. The transistor aspect ratios of MOS transistor were chosen as in [21] and the biasing voltage V_B was taking as 1.7 V. The DC transfer characteristics of the DDCC from Y1, Y2, Y3 terminals to X terminal are shown in the Fig.3.6.

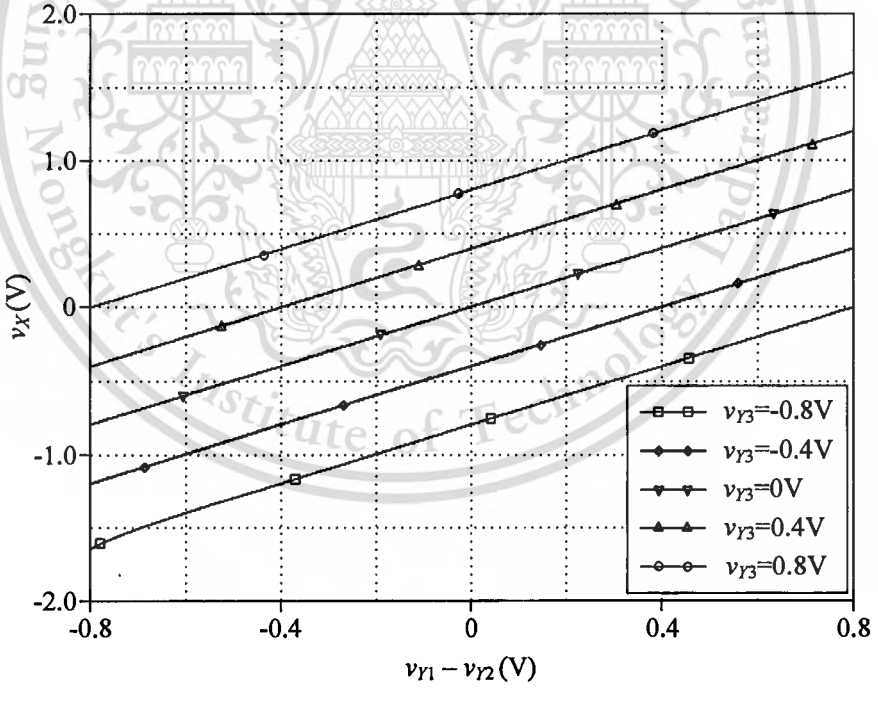


Figure 3.6. DC-voltage transfer from Y-terminal to X-terminal

It is clear that the voltage at X terminal follows the Y terminal. The variation of current at Z+ terminal with X terminal current from –150μA to +150μA is shown in Fig.3.7. In Fig.3.8 show the magnitude frequency response of the DDCC, when terminal X and terminal Z are

connected to the loads of 10kΩ respectively, and terminal is driven by voltage source of 100 mV with $v_{Y2} = v_{Y3} = 0$ V (connected to ground). The DDCC shows a flat response with 359.89MHz at –3dB bandwidth. The frequency response of the Z+ and Z– terminals output current are then displayed in Fig.3.9 respectively.

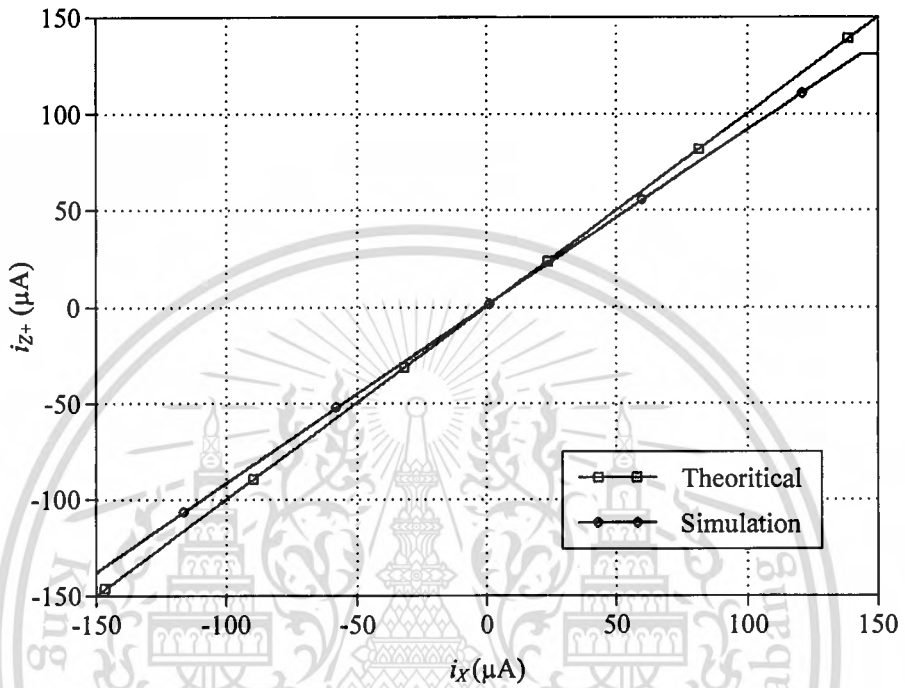


Figure 3.7. Variation of X-terminal current against the current i_{Z+}

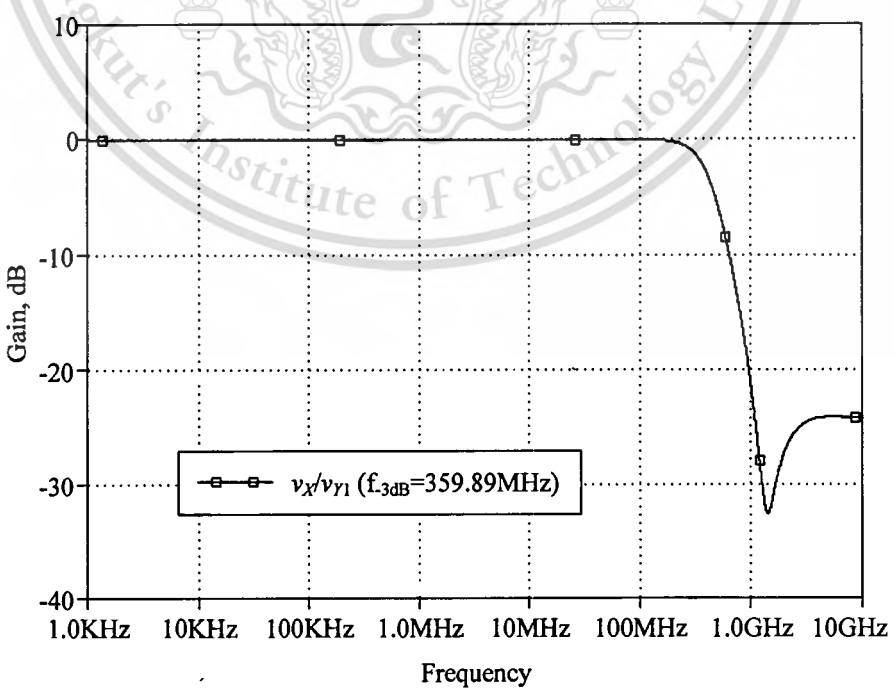


Figure 3.8. Magnitude frequency response of the voltage transfer gain

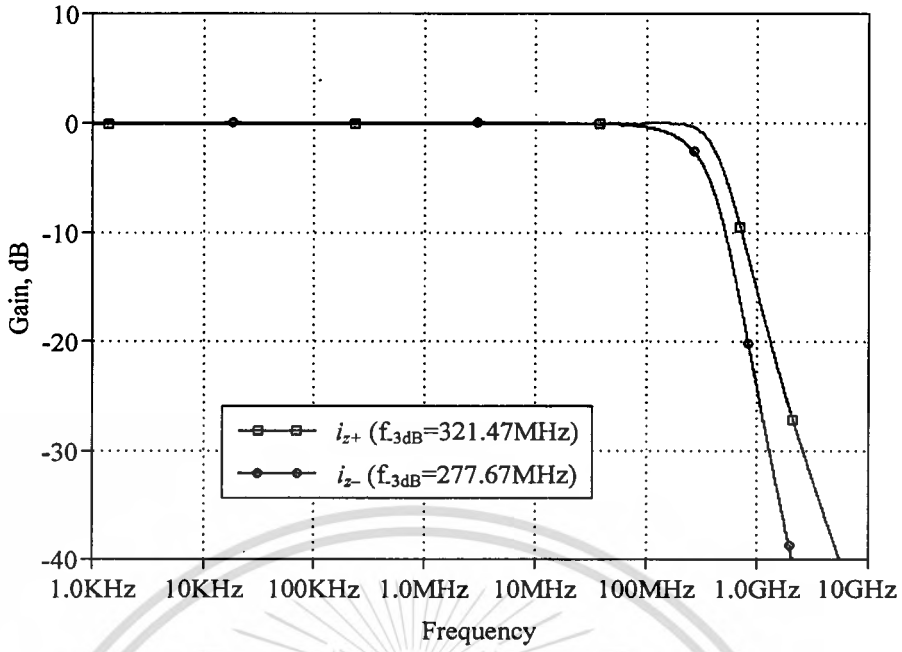


Figure 3.9. Frequency response of the Z-terminal output current

3.2 Applications to Realization of Current Conveyors Based on DDCC

The DDCC circuit as shown in Fig.3.3 is quite useful as a powerful building block of current mode circuits because of its high performances. The popular current conveyors, such as CCII, CCIII, ICCII, and DVCC, can be easily realized by using DDCC is shown in Fig.3.10. Therefore, all the design techniques based on these current conveyors can be directly used for DDCC.

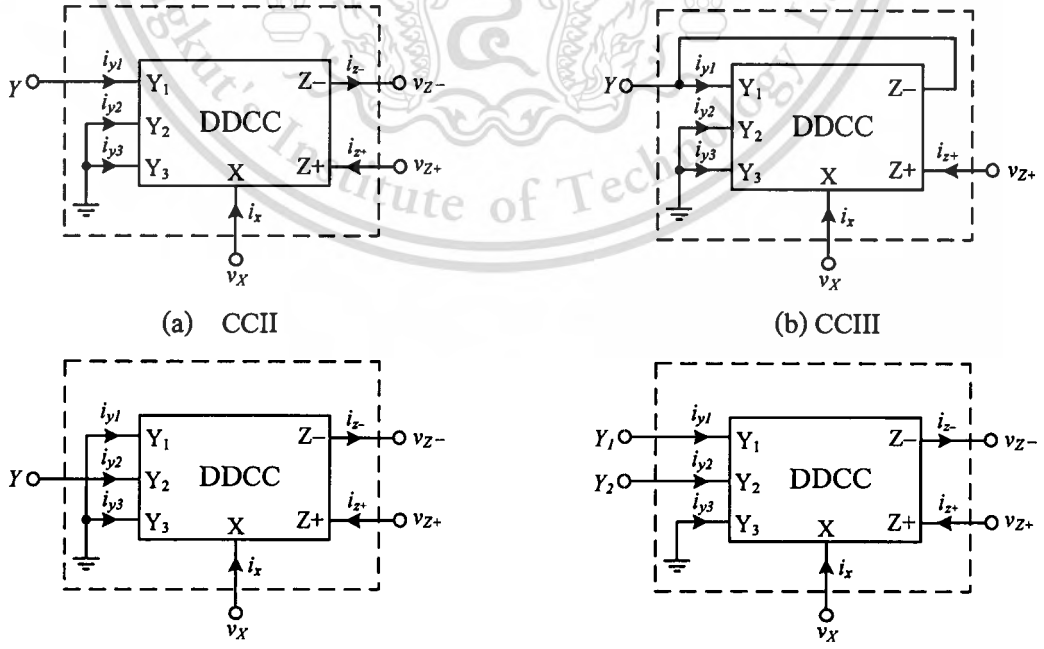


Figure 3.10. Realization of conventional current conveyors using DDCC [16]

3.3 Conclusion

The CMOS realization configuration of the analog building block namely DDCC has been presented in this chapter. The DDCC was developed based on full-differential signal processing circuits such as differential difference amplifier (DDA) or second generation current conveyors (CCII). This device composes the outstanding benefits of DDA and CCII, which are differential difference, wide-bandwidth, and arithmetic operation capability. The element is realized in a CMOS technology, which differs from the recently proposed analog building block [15]-[16]. The non-ideal model of the DDCC is also examined in this chapter. Modification of such DDCC active building block is found to be very appropriate to realize in commercially-purposed integrated circuit [16]. In the next chapter will present some applications of analog signal processing based on this DDCC.

CHAPTER 4

APPICATIONS OF ANALOG SIGNAL PROCESSING BASED ON DDCC

This chapter presents the results of some studies of analog signal processing applications based on differential difference current conveyor (DDCC). These active building blocks are further used in this thesis for voltage-controlled floating resistor, log-antilog current multiplier/divider and programmable voltage adder/substractor circuits.

The main thrust of the work presented here has been focused on the review of the prominent work in the area of DDCC analog building block. Further, the recent developed DDCC signal processing has been used to develop many processing circuit structures, using in analog signal processing, are also presented in this chapter. All circuits are novel and their advantages are compared with the literature presented solutions.

4.1 Voltage-Controlled Floating Resistor Using DDCC

4.1.1 Introduction

The voltage-controlled resistor (VCR) is widely used in analog signal processing. Its applications can be found in telecommunications, electronics and measurements such as active RC filters with variable cutoff frequencies, controlled oscillators, variable gain amplifiers, voltage or current dividers, voltage or current to frequency converters. In VLSI technology, a resistor is formed on silicon wafer. However, resistors of practical values on silicon wafer suffer from limited values and high variability due to process variations. Moreover, its resistance values are not variable. Therefore, they are generally replaced by active resistors. During the last three decades, many approaches for implementing active resistors have been found in the literature [46]-[54]. In [46], a floating resistor circuit has been proposed to use a transconductance operational amplifier (OTA) as an active element with the inputs connected to the outputs. The active resistor circuits based on the use of the intrinsic resistance of the class-AB configuration have been proposed in [47]-[48]. However, the limitation of these reported circuits is suffered from the narrow input voltage range ($\approx$26mV). The limitation of the simulated resistance based on the intrinsic resistance of the bipolar class-AB and bipolar OTA configuration is caused by its

resistance directly proportional to absolute temperature. Moreover, the high value of total harmonic distortion (THD) and the narrow dynamic range are occurred when the large value of simulated resistance is achieved. The floating resistor circuit based on MOS transistor operating in saturation region has been proposed in [49], but it still suffers from the small input voltage range. The second-generation current conveyor (CCII)-based floating resistor has been reported [50]. However, this CCII is composed of four OTAs and one floating resistor. Then, for a floating resistor, the circuit in [50] employs four OTAs and one floating resistor. New techniques to realize a floating resistor using junction field effect transistor (JFET) and operational amplifiers (op-amps) have been developed by [51]-[52]. However, they utilized too many external resistor and a number of them float which is not ideal for integrated circuit implementation. Although op-amps is still commercial availability, unlike current conveyors which is very few in integrated circuit (IC) form but this does not affect their popularity amongst researchers, as is evident from the many of published literature [15]-[23], [50]-[57]. Moreover, the circuits based on newer active elements are better targeted for IC implementation rather than for realization using commercial ICs.

Recently, a voltage-controlled resistor using MOS transistor operating in non-saturation region and voltage follower circuit, which is suitable for integrated circuit implementation, has been reported [53]. However, it suffers from the complexity. Due to the design of voltage followers for canceling the nonlinear component term of MOS transistor in non-saturation region, i.e. $(K/2)(V_{DS})^2$. Moreover, it employs two-matched floating resistor. Although, two floating resistors used in [53] do not need to have specified values. However, the floating resistor value about 30kΩ is used for simulation. The floating resistor realization in [54] requires no passive resistors but still suffers from the difficult design of adder, subtractor and voltage follower circuits for canceling the nonlinear component term. It should be noted that the VCRs in [53] and [54] employ 20 and 17 MOS transistors, respectively.

In this section, a new voltage-controlled resistor based on DDCC, which is suitable for integrated circuit implementation, is presented. The proposed circuit employs one DDCC and four MOS transistors. By using voltage addition and voltage follower properties that are already included in a DDCC, the nonlinear component term of MOS transistor in non-saturation region $\{(K/2)(V_{DS})^2\}$ can be easily cancelled. Also, the voltage divider can be achieved by using two MOS transistors in cascode form. The proposed resistor employs only 16 MOS transistors.

4.1.2 Proposed Circuit Description

Fig.4.1 shows the principle concept of the proposed VCR, which NMOS M_1 in the non-saturation region is used to configure a floating linear resistor. The voltages V_{D1} and V_{S1} are summed by the summer circuit. The output voltage of the summer circuit will be divided by resistor voltage divider R-R. In the non-saturation region, the drain current of the MOS transistor M_1 can be expressed as [58].

$$I_{D1} = K_n\left((V_{GS1} - V_{Tn})V_{DS1} - \frac{V_{DS1}^2}{2}\right) \tag{4.1}$$

where the transconductance parameter $K_n = \mu_n C_{ox} W/L$, μ_n is the mobility of the carrier, C_{ox} is the gate capacitance per unit area, W is the effective channel width, L is the effective channel length, V_{Tn} is the threshold voltage NMOS, V_{GS1} and V_{DS1} are the gate-to-source voltage and the drain-to-source voltage, respectively. The Eq.(4.1) can be simply rewritten as [54]

$$I_{D1} = K_n\left(V_{GS1} - V_{Tn} - \left(\frac{V_{D1} + V_{S1}}{2}\right)\right)V_{DS1} \tag{4.2}$$

From Eq.(4.2), the component term $K_n\{(V_{D1} + V_{S1})/2\}$ should be eliminated to obtained a linear current/voltage (I/V) relationship. Therefore, to obtain a linear I/V relationship, the gate-source voltage of MOS transistor M_1 (V_{GS1}) should be given by

$$V_{GS1} = \frac{V_{D1} + V_{S1}}{2} + \frac{V_B}{2} + V_C \tag{4.3}$$

where V_C is the control voltage and V_B is the constant voltage. The Eq.(4.3) can be achieved by using the voltage follower and resistive voltage divider R-R as shown in Fig.4.1. Substituting Eq.(4.3) into Eq.(4.2), the drain current of the MOS transistor M_1 can be given as

$$I_{D1} = K_n\left(V_C - V_{Tn} + \frac{V_B}{2}\right)V_{DS1} \tag{4.4}$$

According to Eq.(4.4), a linear relationship between drain current and drain-to-source voltage in Fig.4.1 can be obtained. If we let $V_B = 2V_{Tn}$, the resistance value of Fig.4.1 can be expressed as

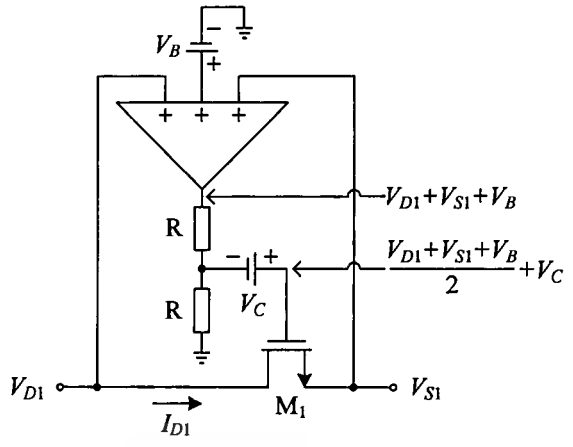


Figure 4.1. Principle concept of proposed floating resistor

$$R_{DS1} = \frac{V_{DS1}}{I_{D1}} = \frac{1}{K_n(V_C)} \tag{4.5}$$

which is controlled by V_C. Thus, we have a non-saturation floating resistor with the equivalent resistance inversely proportional to the control voltage V_C. Also, it can seen from Eq.(4.5) that the circuit can be realized the resistance without temperature effect in term of the threshold voltage. The linear operation of the proposed resistor, described by Eq.(4.5), is obtained under the assumption that the MOS transistor M_1 operates in the non-saturation region. This assumption is satisfied if

$$V_{GS1} > V_{DS1} + V_{Th} \tag{4.6}$$

From Eq.(4.3) and Eq.(4.6), it follows that the lowest value of the control voltage V_C that provides the linear operation of the proposed resistor is given by

$$V_{C(\min)} = \frac{V_{DS1}}{2} \tag{4.7}$$

Consequently, from Eq(4.5) and Eq.(4.7), the maximum equivalent resistance can be achieved for a given V_{DS1} is

$$R_{DS1(\max)} = \frac{2}{K_n V_{DS1}} \tag{4.8}$$

The proposed floating resistor is shown in Fig.4.2. The MOS transistor M_1 in the non-saturation region is used to configure a floating linear resistor. The DDCC operates as voltage summer and voltage follower. Using Eq.(3.1), namely $v_{Y1} - v_{Y2} + v_{Y3} = v_X$, hence the voltage at X-terminal of Fig.4.2 is $V_X = V_{D1} + V_{S1} + V_B$. Also, using MOS diode voltage divider M_2-M_3, it is obvious that the relation of Eq.(4.3) is valid. Note that the MOS transistors in the voltage divider M_2-M_3 do not need to have specified conditions but only the same characteristics. In addition, it should be noted that the voltage divider in this paper is the cascode of two MOS transistors M_1-M_2 with grounded form whereas the divider voltage in [53] is two resistors with ungrounded form which is achieve by diffused or polysilicon resistor. Therefore, compared to [53], the voltage divider in this paper has easy implementation. From the proposed floating resistor in Fig.4.2, the MOS transistor M_4 and current source I_C are operated as a floating control voltage V_C. The MOS transistor M_4 is the source follower operation. The control voltage can be realized as a variable source-to-gate voltage (V_{SG4}) of MOS transistor M_4 in the saturation region. The control voltage V_C can be given by

$$V_C = V_{GS4} = \sqrt{\frac{2I_C}{K_p}} + V_{Tp} \tag{4.9}$$

where the transconductance parameter $K_p = \mu_p C_{ox} W/L$ for PMOS transistor, μ_p is the mobility of the carrier of PMOS transistor, C_{ox} is the gate capacitance per unit area, W is the effective channel width, L is the effective channel length, V_{Tp} is the threshold voltage of PMOS transistor. Substituting Eq.(4.9) into Eq.(4.5), yields

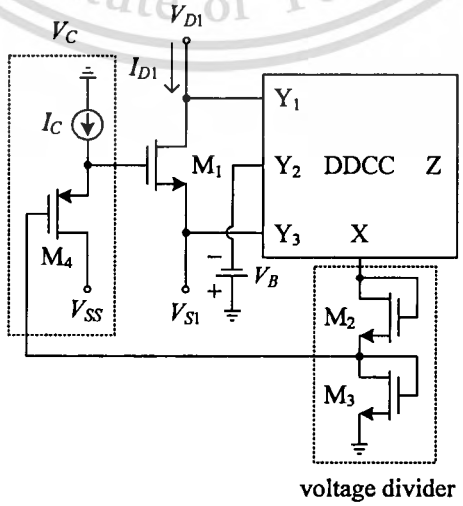


Figure 4.2. Proposed DDCC-based floating resistor

$$R_{DS1} = \frac{V_{DS1}}{I_{D1}} = \frac{1}{K_n\left(\sqrt{\frac{2I_C}{K_p}} + V_{Tp}\right)} \tag{4.10}$$

Letting $K_n = K_p = K$, Eq.(4.10) can be rewritten as

$$R_{DS1} = \frac{1}{\sqrt{2KI_C} + KV_{Tp}} \tag{4.11}$$

Thus, this proposed resistor can be additionally considered as a current-controlled resistor. From Eq.(4.11), the temperature effect that included in term of threshold voltage (V_{Tp}) is slightly changes the resistance value. According to Eqs.(4.8) and (4.11), the lowest value of the current control I_C can be given as

$$I_{C(\min)} = \frac{KV_{DS1}^2}{8} - \frac{K^2V_{Tp}^2}{2} \tag{4.12}$$

Note from the proposed VCR in Fig.4.2 that DDCC-based VCR can be provided the simple configuration. With respect to the proposed VCR, the circuit complexity of voltage follower in [53] is reduced. With respect to the VCR circuit in [54], the proposed circuit enjoys easier realization than the previous VCR circuit where the summer and follower circuits can overcome by using DDCC. Therefore, the resistors can be simply achieved by using one DDCC, one MOS transistor operated in non-saturation region and three MOS transistors operated in saturation region. From Fig.4.2, it can see that the proposed circuit consists of 16 transistors and can be fully integrated in CMOS technology.

To consider the non-ideal effect of DDCC, taking the non-idealities of the DDCC into account, the relationship of the terminal voltages and currents, described by Eq.(3.24). The Eq.(4.3) can be expressed as

$$V_{GS1} = \frac{\alpha_1 V_{D1} + \alpha_3 V_{S1}}{2\delta} + \frac{\alpha_2 V_B}{2} + V_C \tag{4.13}$$

where δ is the matching error of the resistor voltage divider R-R(M_2-M_3). Substituting Eq.(4.13) into Eq.(4.2), Eq.(4.2) becomes

$$I_{D1} = K_n\left(\frac{\alpha_1 V_{D1} + \alpha_3 V_{S1}}{2\delta} + \frac{\alpha_2 V_B}{2} + V_C - V_{Tn} - \left(\frac{V_{D1} + V_{S1}}{2}\right)\right)V_{DS1} \qquad (4.14)$$

From Eq.(4.14), the tracking error and the matching error slightly increase the non-linearity of the resistor circuit, namely the nonlinear component $(K/2)(V_{DS})^2$ maybe not eliminated to zero. The matching error of two MOS transistors M_2-M_3 (δ) can be improved by adjusting the aspect ratios (W/L) of MOS transistor M_2 or M_3. Note that the resistance value in Fig.4.2 is tuned by adjusting the bias current. If the floating resistor in Fig.4.2 is required for tuning by the bias voltage, the bias voltage may be replaced directly instead of the current source or an additional voltage-to-current converter may be used.

4.1.3 Simulation Results

The proposed VCR has been simulated by PSPICE. The PSPICE model 1.2μm CMOS parameter through MOSIS for NMOS and PMOS is listed in [20]. The supply voltages used are ±5V. The aspect ratios for DDCC circuit are given in Table 4.1 [20]. The bias voltage V_{BB} used for DDCC is –4.5V and the constant voltage V_B used is 1.38V. The aspect ratios (W/L) MOS transistors in Fig.4.2 for M_1, M_2, M_3, and M_4 are 20μm /10μm, 4.8μm /4.8μm, 4.8μm /4.8μm, and 33.2μm /4.8μm, respectively.

Table 4.1 Transistor aspect ratio of DDCC [20]

MOS transistor	W/L (μm/μm)
M_1-M_4	7.2/4.8
M_5, M_6	39.6/4.8
M_7, M_8	111.6/3.6
M_9-M_{12}	144/4.8

To avoid the channel length modulation effect, the effective channel length should be larger than 5μm [51]. Fig.4.3 shows the simulation results of $I_{D1} - V_{DS1}$ characteristics with I_C as a parameter. The drain-to-source voltage V_{DS1} of MOS transistor M_1 is swept from 0V to 4V. The minimal control voltages $V_{C(\min)}$ = 2V is calculated according to Eq.(4.7) and it corresponds to the control current $I_{C(\min)}$ = 300μA (K =153.8μA/V^2) calculated according to Eq.(4.12).

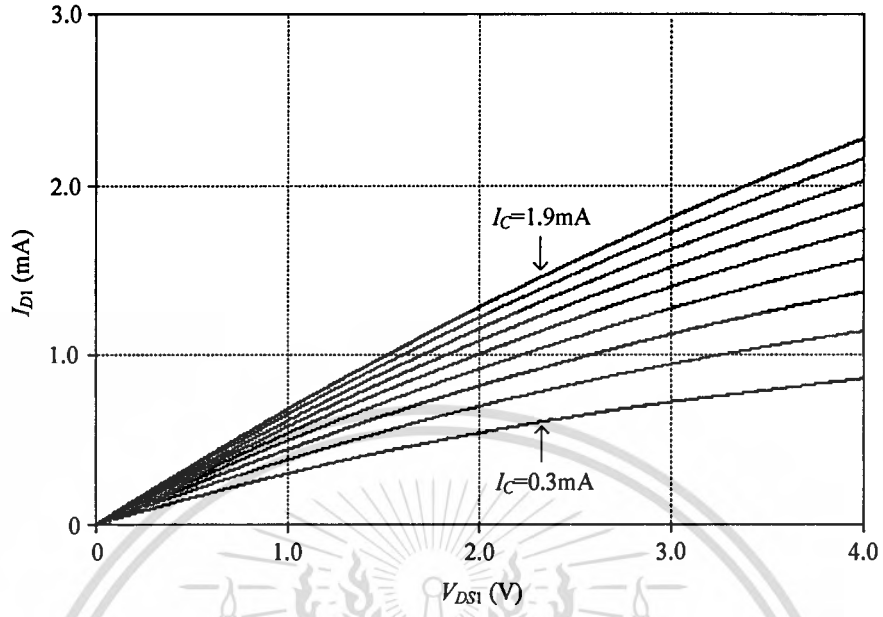


Figure 4.3. Simulated resistor current against resistor voltage

To analyze the frequency characteristics of the proposed floating resistor, a voltage divider circuit was designed as shown in Fig.4.4. Simulation results at the output V_o showed that, for a 4Vp-p signal and 100kHz sine wave across the proposed floating resistor, where the current I_C is fixed as 500μA, the total harmonic distortion (THD) was about 3.8%.

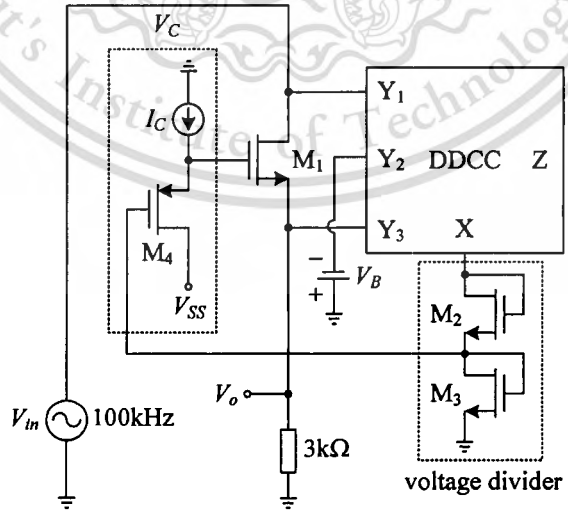


Figure 4.4. Voltage divider using the proposed floating resistor

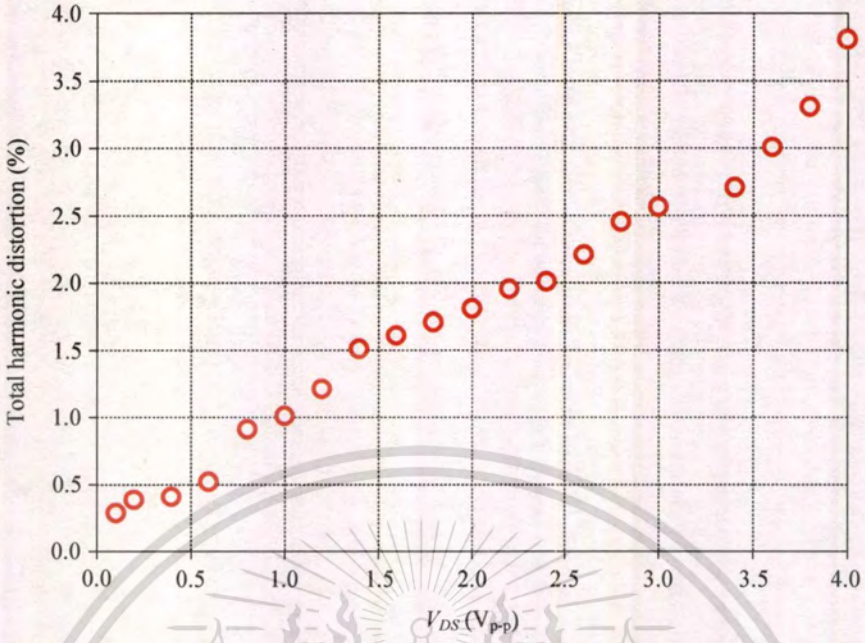


Figure 4.5. Distortion against signal amplitude

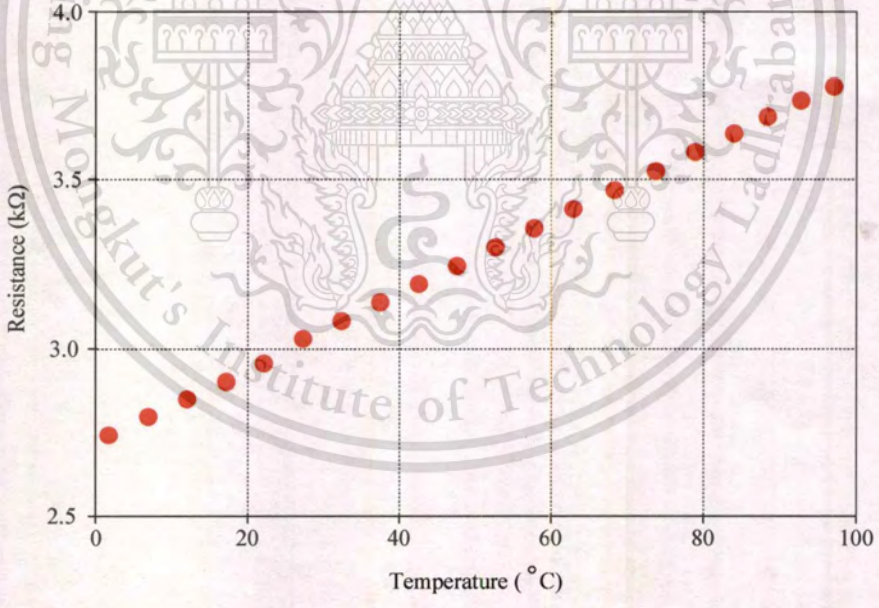


Figure 4.6. Resistance values at different temperatures

The variation of THD with input signal amplitude for a nominal resistance of 3kΩ (I_C =0.5mA and W/L =20μm/10μm) is illustrated in Fig.4.5. Fig.4.6 shows the resistance values at temperature of 0°C to 100°C where I_C =500μA and V_{DS} =1.5V. From Fig.4.6, the resistance is 2.9kΩ and 3.64kΩ at the temperature 0 °C and 100 °C, respectively. This evaluates that the

resistance error is about 20% when the temperature change from 0°C to 100°C. It is the effect of the transconductance parameter $(K = \mu_n C_{ox} W/L)$ that dominates parameters of the proposed circuit which appears in Eq.(4.10). This effect may be cancelled by interconnected with the voltage-to-current converter. The parameter μ associated with the temperature effect can be described as [54].

$$\mu(t) = \mu(T_r)\left(\frac{T}{T_r}\right)^{-k_3} \tag{4.15}$$

where T is absolute temperature and T_r is room temperature (Kelvin), and k_3 is the constant (1.5 to 2). Finally, sine wave signals (2Vp) were supplied to V_{in} of Fig.4.4. When the frequencies were increased, it was found that the proposed VCR could operate with the –3dB bandwidth of about 140MHz.

Table 4.2 Comparison of the proposed VCR with those of previous works

Parameter	Proposed VCR	Senani [52]	Tadic et al. [53]	Prommee et al. [54]
Components	1 DDCC (12 MOS's), 4 MOS's, 1 current source	1 or 3 op-amps, 1 MOS of JFET, 4 floating resistors, 1 grounded resistors	20 MOS's, 2 floating resistors, 1 current source	17 MOS's
Supply voltage	±5V	±15V	±6V	±5V
Input range (V_{DS})	4V (V_S=0)	±1V	3V (V_S=2V)	±1V
Suitable for IC	Yes	No	No	Yes
Ease for realization	Yes	Yes	No	No

4.1.4 Conclusion

A new simple voltage-controlled floating resistor is presented. The proposed circuit consists of one DDCC and three MOS transistors, and can be fully integrated in CMOS technology. The DDCC is employed to provide a simple circuitry of the circuit. The divider voltage in this section is implemented by cascode of two MOS transistors M_1-M_2 and the nonlinear component term $\{(K/2)(V_{DS})^2\}$ which can be easily eliminated by using DDCC. The proposed voltage-controlled resistor is very suitable for implementation in CMOS VLSI circuits which interface the continuous analog signal carrying the measuring information to the digital

signal processing circuits. A comparison of this proposed VCR and previous works is summarized in Table 4.2.

4.2 A CMOS Log-Antilog Current Multiplier/Divider Circuit Using DDCC

4.2.1 Introduction

An analog multiplier and divider is a useful circuit building block used in communication, electronic and control systems such as amplitude modulation, frequency multiplier, frequency divider, automatic gain control, phase lock loop, adaptive filtering. Generally, the well-known multiplier can realize multiplier function by using Gilbert cell [24], [59] and MOS transistors operating in either a saturation region or a triode region [60]-[63]. However, these reported circuits suffer from the circuit complexity.

Log-antilog multipliers use the exponential property of a forward bias *pn* junction, using either a diode or bipolar transistor, to provide the necessary log and antilog function [1]. Typically, conventional log-antilog multipliers could be realized using operational amplifiers, bipolar transistors and resistors for it multiplication function [64]. However, using operational amplifiers as building blocks to synthesize the multiplication function will limit the high frequency operation of the multiplier. Moreover, it will also increase the cost, power consumption, and chip areas. For these reasons, it is useful to apply the translinear log-antilog multipliers/dividers avoiding operational amplifiers, and introducing current-mode signal processing [2], [65]. The current-mode techniques provide large benefits in practical circuits and systems, and give elegant solutions for many circuit and system problems [66]. However, log-antilog multiplier/divider configurations in [2], [65] are only suitable for bipolar technology.

In this section, a new current-mode one-quadrant log-antilog multiplier/divider based on DDCC is proposed. The circuit employs one DDCC and four diodes. Since the addition and subtraction operation of voltage signals have been offered by DDCC, hence the proposed circuit is simple circuitry. Also, the circuit enjoys excellent temperature stability and very suitable for implementation in CMOS technology.

4.2.2 Proposed Circuit Description

The proposed log-antilog multiplier/divider is shown in Fig.4.7. It is composed of one DDCC and four diodes.

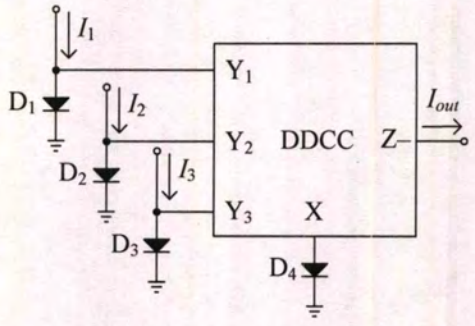


Figure 4.7. Proposed current-mode log-antilog multiplier/divider

The operation of the circuit can be explained as follows. If input currents (I_1, I_2, I_3) are supplied, using the logarithm property of a forward bias *pn* junction of diode [59], the voltages, v_{Y1}, v_{Y2} and v_{Y3}, of DDCC can be obtained, respectively, as

$$v_{Y1} = V_T \ln\left(\frac{I_1}{I_S}\right) \tag{4.16}$$

$$v_{Y2} = V_T \ln\left(\frac{I_2}{I_S}\right) \tag{4.17}$$

$$v_{Y3} = V_T \ln\left(\frac{I_3}{I_S}\right) \tag{4.18}$$

where I_S is the reverse saturation current and V_T is the thermal voltage.

Using Eq.(3.1), the voltage v_X can be obtained as

$$v_X = V_T \ln\left(\frac{I_1}{I_S}\right) - V_T \ln\left(\frac{I_2}{I_S}\right) + V_T \ln\left(\frac{I_3}{I_S}\right) \tag{4.19}$$

Assume that diodes (D_1, D_2, D_3, D_4) are closely matched, the current output I_{out} can be given by

$$I_{out} = \frac{I_1 I_3}{I_2} \tag{4.20}$$

which means that the output current I_{out} is a multiplier/divider of the input signal currents I_1, I_2 and I_3. It should be noted that the output current is also temperature independent.

To consider the non-ideal effect of DDCC, taking the non-idealities of the DDCC into account, the relationship of the terminal voltage and currents, described by Eq.(3.24). The characteristic equation of Fig.4.7 become

$$I_{out} = \frac{\beta I_1^{\alpha_1} I_3^{\alpha_3}}{I_2^{\alpha_2}} I_S^{(1-\alpha_1+\alpha_2-\alpha_3)} \tag{4.21}$$

From Eq.(4.21), the tracking errors slightly increase the linearity error of the multiplier/divider circuit. Fig.4.8 shows the across-section of PMOS transistor in a *p*-substrate CMOS process. In this figure, the PMOS transistor is implemented in *n*-well and the diodes, D_1 and D_2, are the junction diode which is established between p-substrate and n^+ diffusion of the drain region. This junction diode is used in this paper. The diodes, D_1 to D_4, of Fig.4.7 will be replaced by the junction diodes in Fig.4.8. Therefore, the proposed log-antilog multiplier/divider in this paper can easily be implemented by CMOS technology.

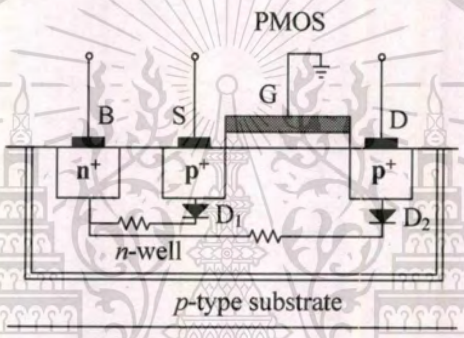


Figure 4.8. Cross-section of PMOS transistor in a *p*-substrate CMOS process

4.2.3 Simulation Results

To verify the theoretical prediction of the proposed circuit, Fig.4.7 has been simulated using PSPICE simulations. The DDCC and diodes were simulated using the 0.5μm MIETEC [21]. The transistor aspect ratios of DDCC are listed in Table 4.3 [21]. The supply voltages were used $V_{DD} = -V_{SS} = 2.5\text{V}$ and the biasing voltage V_B was taken as –1.7V.

Table 4.3 Transistor aspect ratio of DDCC and diodes

MOS transistor	W/L (μm/μm)
M_1-M_4	1.6/1
M_5, M_6	8/1
M_7, M_8	20/1
M_9, M_{10}	29/1
M_{11}, M_{12}	90/1
D_1-D_4	1/1

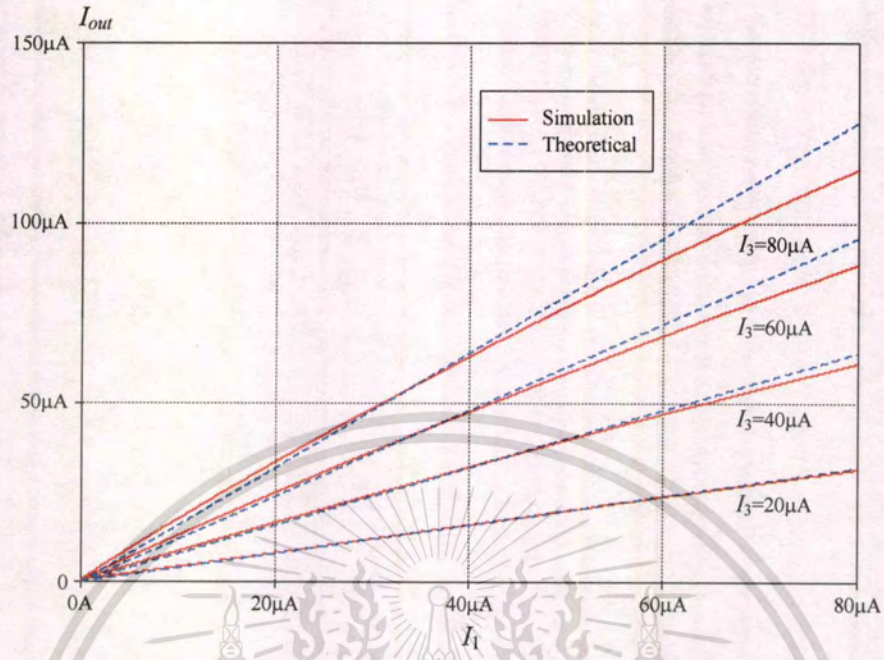


Figure 4.9. Simulated DC transfer characteristic of the multiplier circuit

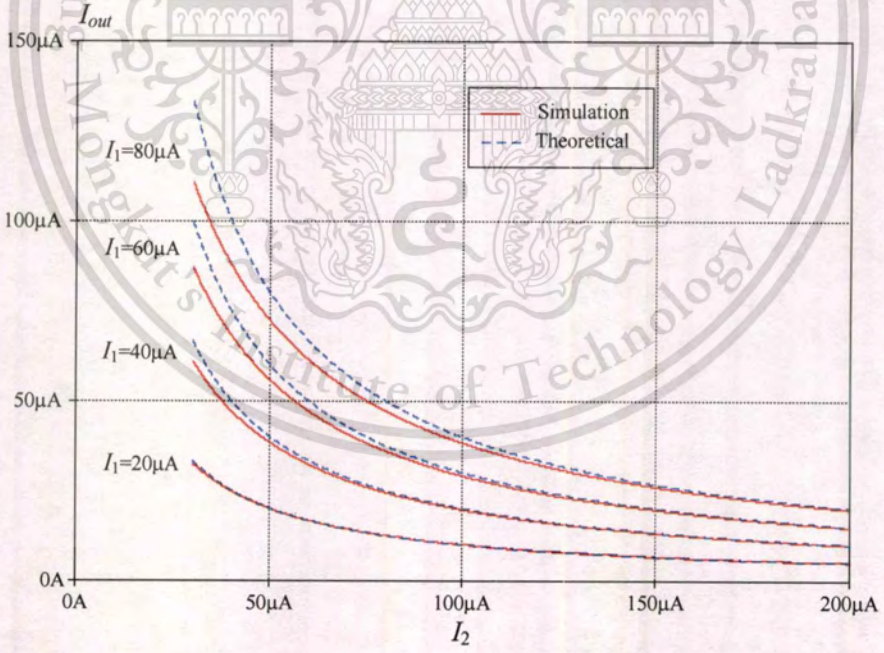


Figure 4.10. Simulated DC transfer characteristic of the divider circuit

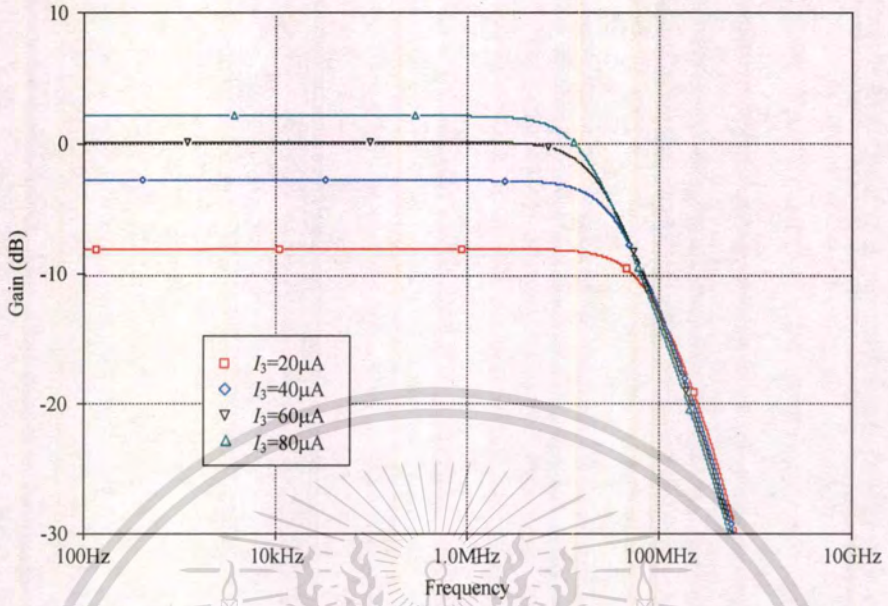


Figure 4.11. Simulated frequency response of proposed circuit

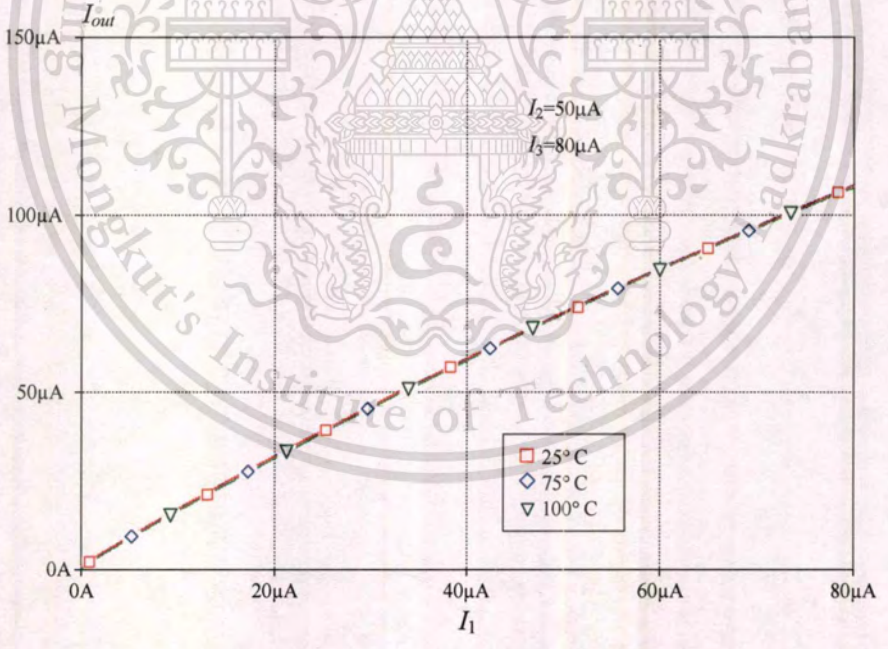


Figure 4.12. Output current at different temperatures

Fig.4.9 shows the simulated DC transfer characteristics of the multiplier. Here, the current I_2=50μA, the current I_1 is swept from 0 to 80μA and I_3 is changed in step from 0 to 80μA. In this figure, the maximum error between simulated curve and theoretical curve is about 15.3% at

$I_1 = I_3$=80μA. The transfer characteristics of the divider are shown in Fig.4.10. In this figure, the current I_3=80μA, the current I_2 is swept from 0 to 200μA and I_1 is changed in step from 0 to 80μA. The maximum error between simulated curve and theoretical curve of Fig.4.10 is about 16.8%. The frequency response of the proposed multiplier/divider is shown in Fig.4.11 when I_2 is fixed as a 50μA, I_3 are 20, 40, 60 and 80μA and I_1 is the sinusoidal current with peak amplitude of 50μA. In this figure, the –3dB frequency for I_3=80μA is about 17MHz. To demonstrate the temperature performance of the proposed circuit, we again simulate the proposed circuit at the currents I_2=50μA, I_3=80μA and I_2 is varied from 0 to 80μA by changing the temperature from 0°C to 100°C. Fig.4.12 shows the output currents of the proposed multiplier at temperature of 25°C, 75°C and 100°C. It shows that the proposed circuit provides excellent temperature stability. Fig.4.13 shows the multiplier being used for amplitude modulation with inputs of a 1MHz and a 10MHz sine wave.

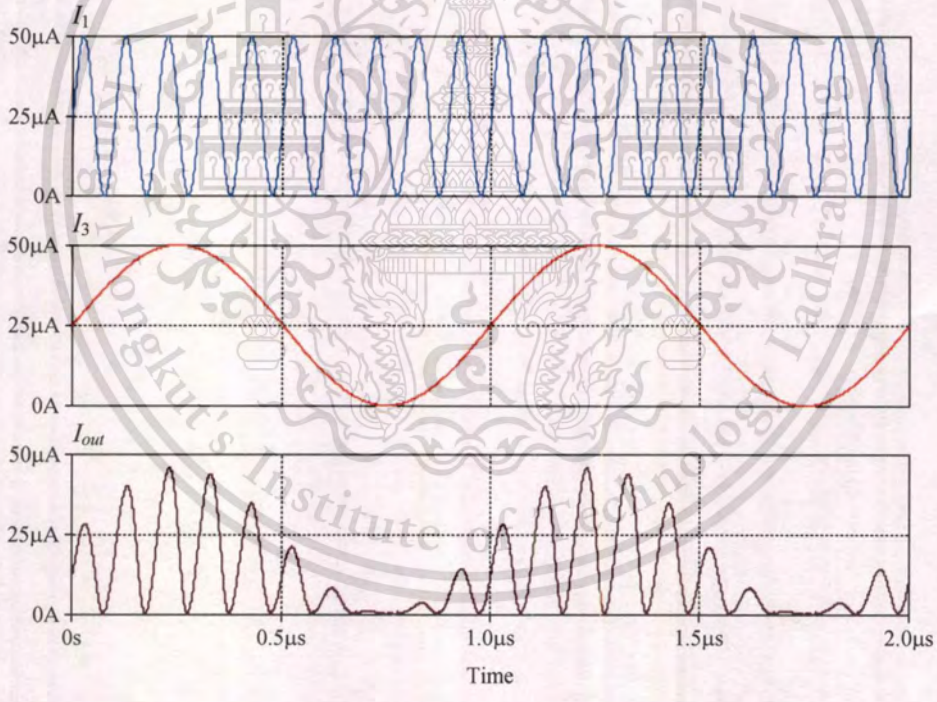


Figure 4.13. Product between a 1MHz and a 10MHz sinusoidal wave

4.2.4 Conclusion

A new one-quadrant log-antilog current multiplier/divider has been presented. The proposed circuit employs one DDCC and four diodes which is very suitable for implementation in CMOS technology. This circuit will be a useful sub-circuit for analogue signal processing system

such as four-quadrant multiplier, function generator and log-antilog amplifier. The proposed log-antilog multiplier/divider has not been found in the previous literature.

4.3 Programmable Voltage Adder/Substractor Using DDCC

4.3.1 Introduction

Adder and subtractor circuits can be applied widely in communication and electronic systems, such as digital encoder, automatic gain amplifier, AM and FM modulations and neural networks. Therefore, several adders and subtractors have been reported in the technical literature [67]–[71]. In [67]–[68], voltage adder/subtractor circuits have been proposed. However, they provide only a positive voltage output operation range, although both positive and negative supply voltages are applied. In [69], Fried and Enz proposed a simple and accurate voltage adder with MOSs biased in weak-inversion, which is suitable for low power circuit application. However, its frequency performance and voltage operation range are limited. The operational amplifier (op-amp) based adder/subtractor circuit in [70] offers the simplest way to obtain both positive and negative voltage output operation range, but the op-amp based adder/subtractor uses passive resistors, although these resistors can be substituted by MOS-resistors, the drawback of using many devices and consuming high power of the op-amp still exists. Moreover, the drawback of these circuits is the well-known limitations of the op-amps.

Recently, a new technique for realizing programmable adder/subtractor using a current conveyor analogue switch is proposed [71]. The circuit uses the bias current of the current conveyor which makes program possible through the bias current. When it applies to encoder, the advantages of this circuit identified by the author are the following:

I. The encoder uses fewer devices.

II. The encoding formats of the encoder circuit can be changed by the voltage levels fed to the encoder whereas the encoding formats of a conventional encoder using digital gates can be changed by changing the circuit configuration. This shows that this encoder provides more flexibility.

III. The encoder yields the voltage level output but a conventional encoder using digital gates yields the digital output. Thus the proposed encoder is more suitable for wireless analogue communication than a conventional one: frequency modulation (FM) by using an additional voltage-controlled oscillator and amplitude modulation (AM) by using an additional voltage controlled gain amplifier. For a conventional

encoder, to obtain an FM or AM signal by using the same method, it needs a digital-to-analogue converter to change the digital output to the voltage, which is unnecessary for the proposed encoder.

With respect to (I)-(III) above, the circuit of [71] is a good adder/subtractor circuit for IC fabrication. However, it suffers from three disadvantages. First, the circuit uses an excessive active component, such as for a three-input adder/subtractor, it employs three CCIIs and four MOS resistors. Second, the amplification and attenuation of the circuit is controlled by current which applies through the bias current of the current conveyor. Therefore, if the voltage signal (i.e. digital signal) is supplied, the voltage-to-current converter is may be required. Third, the circuit is suitable for a high impedance load. If the low impedance load is applied, the circuit needs a voltage buffer at an output.

In this section, we pursue the objective of developing adder/subtractor that is suitable for IC fabrication. We propose a new circuit that improves on the advantages of the circuit of [71] while overcoming the disadvantages. For a three-input adder/subtractor, the proposed circuit employs only one DDCC, six MOS switches and three inverter circuit (6 MOS transistors). In particular, the circuit has the following features:

I. The proposed a three-input adder/subtractor uses 24 MOS transistors whereas the proposed circuit in [71] uses 51 MOS transistors; hence when the proposed circuit is fabricated, the proposed circuit will be used small area of chip than the previous adder/subtractor.

II. For application to digitally programmable, the digital signal can be directly controlled the MOS switch without additional voltage-to-current converter circuit.

III. It possesses low output impedance voltage signals.

4.3.2 Proposed Circuit Description

The proposed a three-input adder/subtractor is shown in Fig.4.14. The proposed circuit consists one DDCC, six-MOS transistor switches (M_{S1} to M_{S6}) and three MOS inverters. Assuming that voltages V_{C1}, V_{C2}, and V_{C3} are applied, using Eq.(3.1), the output voltage of proposed circuit is

$$V_o = V_1 - V_2 + V_3 \tag{4.22}$$

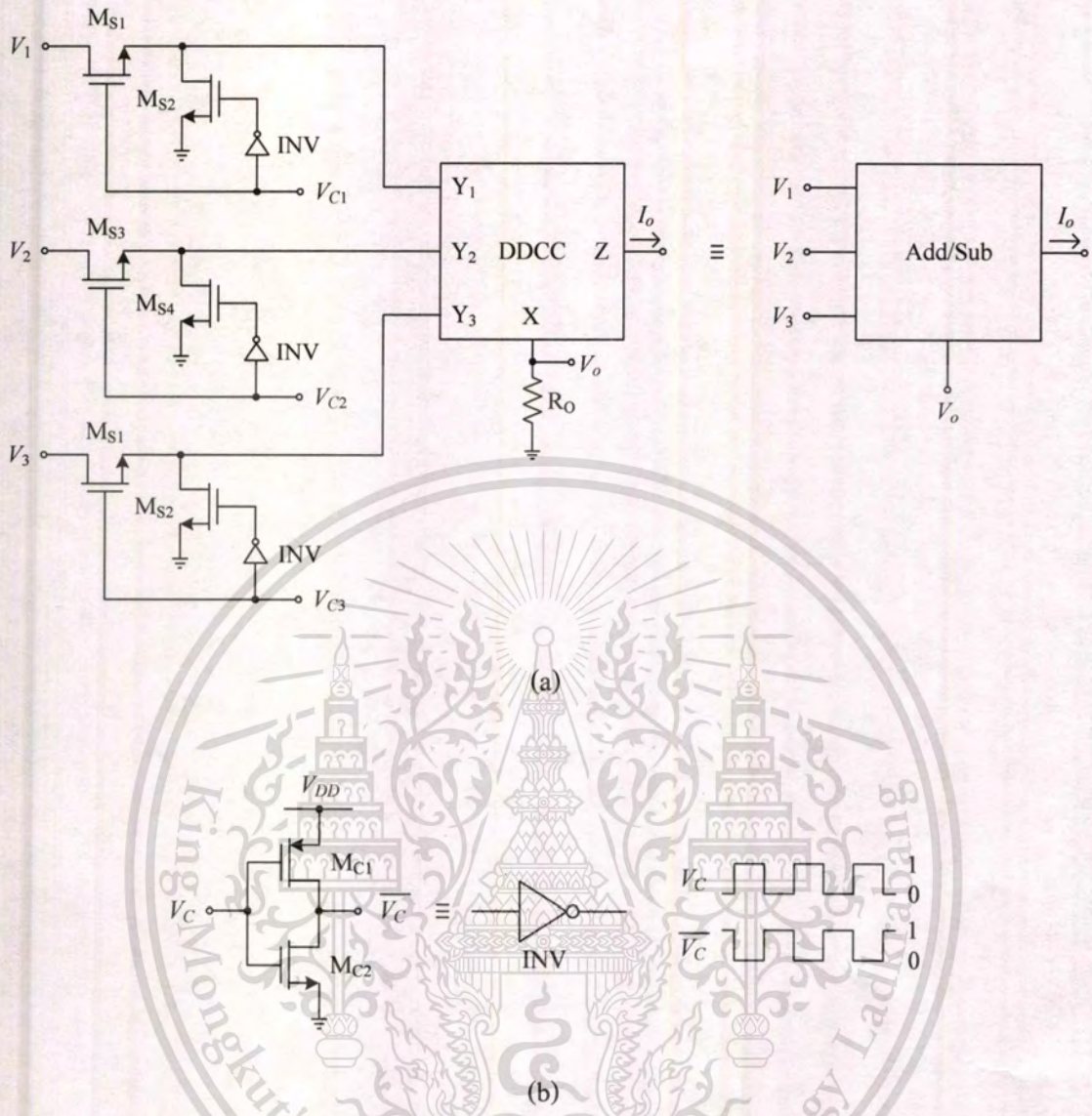


Figure 4.14. (a) Proposed programmable three-input adder/substractor circuit (b) MOS inverter

The operation of proposed adder/subtractor can be explained. If the voltages V_{C1}, V_{C2}, and V_{C3} are not supplied, the function of adder and subtractor $(V_1 - V_2 + V_3)$ will be ignored $(V_o = 0)$. On the other hand, If the voltages V_{C1}, V_{C2}, and V_{C3} are supplied, the function of adder and subtractor will be achieved $(V_o = V_1 - V_2 + V_3)$. Each function of adder and subtractor can be obtained in Table 4.4. It can see that the output voltage can be programmed by V_{C1}, V_{C2}, and V_{C3}, where "0" in Table 4.4 is having no voltage for V_C and "1" is a constant voltage.

Table 4.4 Operation of the proposed three-input programmable adder/substractor

V_{C1}	V_{C2}	V_{C3}	V_o
0	0	0	0
0	0	1	V_3
0	1	0	$-V_2$
0	1	1	$-V_2+V_3$
1	0	0	V_1
1	0	1	V_1+V_3
1	1	0	V_1-V_2
1	1	1	$V_1-V_2+V_3$

The impedance approximation can be derived by small signal model analysis of Fig. 4.13. Input impedance of the proposed adder/subtractor is the impedance at node Y of a DDCC. Due to input port for voltage controls (V_{C1}, V_{C2}, V_{C3}) is the gate of MOS transistor, impedance at port V_C (Z_C) is extremely high. Then input port impedance Z_C is approximately expressed as

$$Z_C \approx \infty \tag{4.23}$$

Input impedance (Z_{in}) for voltage inputs (V_1, V_2, V_3) is the impedance at node Y of a DDCC serried with g_{ds} of MOS switch operating in non-saturation region. Then, input port impedance can be approximated as

$$Z_{in} \approx \infty + g_{ds(SW)} \tag{4.24}$$

where $g_{ds(SW)}$ is the conductance between drain and source of MOS switches in non-saturation region. Output impedance of the proposed adder/subtractor is the impedance at node X of a DDCC. The terminal impedance looking into X can be derived by setting V_{in} and V_C to zero, applying a test voltage V_o at node X, and calculating the current I_o. The output impedance can be obtained as

$$Z_o \approx \frac{(g_{m3}+g_{m4})(g_{d12}+g_{d34}+g_{d6})}{2g_{m3}g_{m4}g_{m7}} \tag{4.25}$$

where g_{mi} is the transconductance and g_{di} is the drain conductance of transistor M_i, respectively. From Eq.(4.25), the following parameters are given as $g_{m3} = g_{m4} = 1.19\times10^{-4}$ A/V,

$g_{m7} = 2.86\times10^{-4}$A/V, $g_{d12} = g_{d34} = 5.42\times10^{-7}$A/V and $g_{d6} = 1\times10^{-6}$A/V. Output port impedances calculation is obtained around 61.23Ω agreed with the theoretical.

4.3.3 Simulation Results

To verify the theoretical prediction of the proposed circuit, Fig.4.13 has been simulated using PSPICE simulations. The DDCC was simulated using the 0.5μm MIETEC [21]. The transistor aspect ratios of DDCC are listed in Table 4.3 [21]. The supply voltages were used $V_{DD} = -V_{SS} =$ 2V and the biasing voltage V_B was taken as –1.2V. The W/L ratios of MOS inverters (M_{C1} and M_{C2}) and MOS switches (M_{S1} to M_{S6}) are 2μm/2μm. The constant voltage V_C for turning on the MOS switch is 1.5V and for turning off is 0V.

Sine wave signals were supplied to V_1, V_2, and V_3. When the frequencies were increased, it was found that the proposed adder/subtractor could operate with the –3dB bandwidth of about 150MHz as shown in Fig.4.15.

For the tested proposed programmable, its output voltage V_o is $V_1 - V_2 + V_3$. Fig. 4.16 shows the operation of proposed programmable adder/subtractor when applies a DC 0.1V at a three-input of the proposed digitally programmable adder/subtractor. Theoretically, the digital levels, 000, 001, 010, 011, 100, 101, 110, and 111 yield the DC outputs: 0, 0.1, – 0.1, 0, 0.1, 0.2, 0, and 0.1V, respectively. It can see in Fig.4.16 that the proposed circuit can be operated as adder/subtractor corresponding with theory.

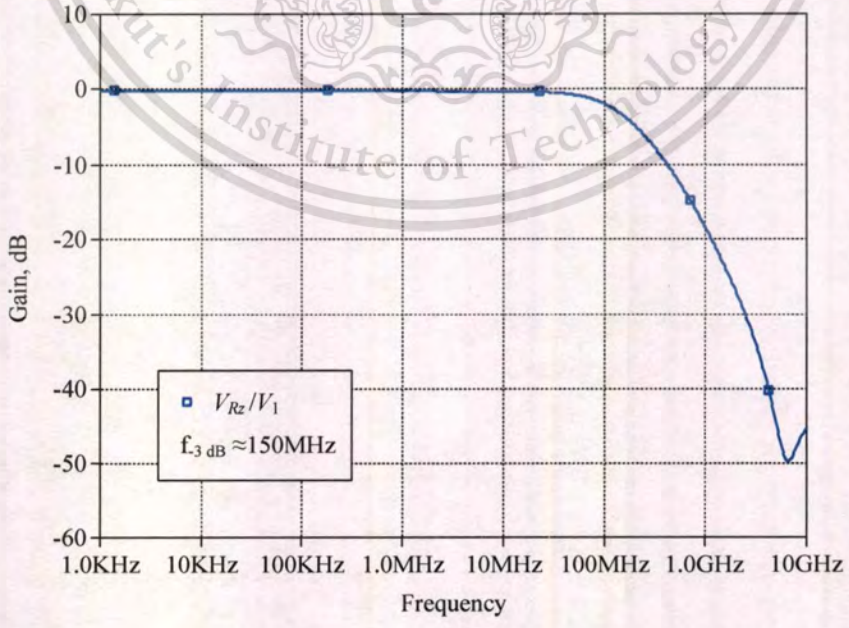


Figure 4.15. The frequency response of the proposed programmable adder/subtractor

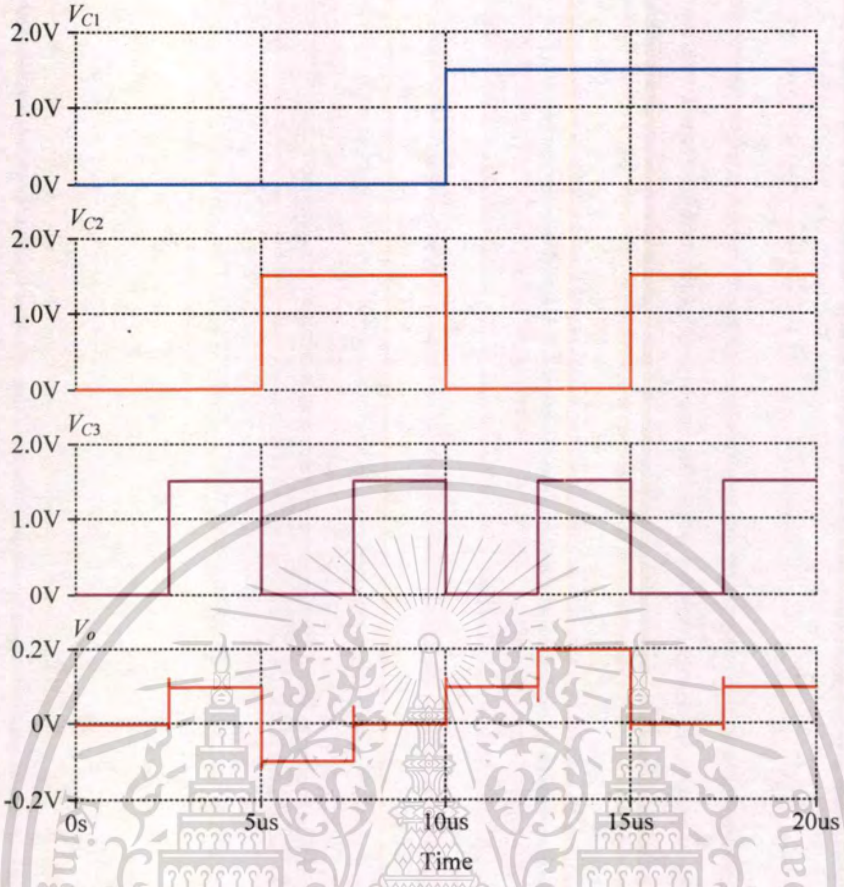


Figure 4.16. Operation of the proposed programmable adder/subtractor

4.3.4 Conclusion

In this section, a programmable voltage adder/subtractor has been presented. Compared previous adders and subtractors, the proposed adder/subtractor uses lesser transistors, yields simpler structure and offers lower output impedance. Moreover, its operation can be directly programmable by a digital signal. It is to be further noted that the proposed adder/subtractor can be realized an encoder as same as the recent work in [71]. Hence when it is applied to the encoder it also yields advantages in view of a number of devices, a changeable encoding format by the voltages, and a DC output suitable for wireless analogue communication as presented in the recent work [71].

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

The goal of this thesis was to bring the contribution on the field of the analog building blocks for the modern integrated circuits operated in current-or mixed-mode. The group of the blocks was made tighter by focusing on Differential Difference Current Conveyor (DDCC). The aim exploration of the DDCC circuits is to extend the applications in analog signal processing.

New DDCC-based design of resistance function pertaining to ideal floating resistor simulation schemes with a further extension to the design of operation of an electronically controllable were presented in this thesis. The theoretical analysis has been verified based on simulation through the application circuits such as voltage divider circuit. These designs have been very low total harmonic distortion (THD) without requiring any passive component.

Arithmetic operation capability found wide variety applications, the well-known multiplier/divider and adder/substractor circuits gives rise to some limit of high frequency operation and temperature stability; however, the problem had been avoided by the modified designs.

In addition, new DDCC-based design of multiplier/divider and adder/substractor in both current-mode and voltage-mode forms; programmable capability had been derived in some of the designs. It was shown that these designs are well-suited for monolithic integrated circuits fabrication process in which event the sensibility of the time constant may be reduced to extremely low values.

The present work represents modern applications of DDCC active building block in analog signal processing have not yet been found in previous literatures. The functionalities of the proposed circuits were proved by simulations using the PSPICE program, where the results closely match with theoretical values and validity of using it in analog functions.

With respect to the above summary, it can be declared that aims of this thesis were fulfilled.

5.2 Future Work

The aim of this thesis has been focused on the realization of analog signal processing applications using DDCC. Many research activities are currently under way in the direction of development of novel active building blocks, which are suitable for signal processing circuits. Several directions in which the present work can be extended have been given in references. Some of them are given below

I. This research is designed based on 0.5μm and 1.2μm CMOS technology. If better performances, i.e., low-power, voltage and higher operating frequency, are required, it can be redesigned by using newer technology such as 0.18μm, 0.25μm or 0.35μm. The CMOS implementations of building blocks could be developed according to functional requirement imposed by the power efficiency and compatibility with deep-submicron technology.

II. The performances of this research are confirmed only from simulations. If the proposed circuits are built as an IC, the performances will be decreased by the effect of parasitic parameters and process of production.

III. The layout of the design of signal processing circuits must be completed in order to complete the whole design cycle. After doing layout versus schematic, it can be seen that design is ready for fabrication.

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APPENDICES

APPENDIX A

SPICE MODEL PARAMETERS

Tab. A.1: Model parameters of 0.5μm CMOS technology from MIETEC

.MODEL CMOSN NMOS (LEVEL=3 UO=460.5 TOX=1.0E-8 TPG=1 VTO=0.62 JS=1.08E-6
+ XJ=0.15U RSH=2.73 LD=0.04U VMAX=130E3 NSUB=1.71E17 PB=0.761 ETA=00 THETA=0.129
+ PHI=0.905 GAMMA=0.69 KAPPA=0.10 CJ=76.4E-5 MJ=0.357 CJSW=5.68E-10 MJSW=0.302
+ CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=3.07E-28 AF=1 WD=+0.11U
+ DELTA=+0.42 NFS=1.2E11 DELL=0U LIS=2 ISTMP=10 TT=0.1E-9)
.MODEL CMOSP PMOS (LEVEL=3 UO=100 TOX=1.0E-8 TPG=1 VTO=-0.58 JS=0.38E-6
+ XJ=0.10U RSH=1.81 LD=0.03U VMAX=113E3 NSUB=2.08E17 PB=0.911 ETA=00 THETA=0.120
+ PHI=0.905 GAMMA=0.76 KAPPA=2 CJ=85E-5 MJ=0.429 CJSW=4.67E-10 MJSW=0.631
+ CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=1.08E-29 AF=1 WD=+0.14U
+ DELTA=0.81 NFS=0.52E11 DELL=0U LIS=2 ISTMP=10 TT=0.1E-9)

Tab. A.2: Model parameters of 1.2μm CMOS technology from MOSIS

.MODEL CMOSN NMOS (LEVEL=3 PHI=0.700000 TOX=3.0500E-08 XJ=0.200000U TPG=1
+ VTO=0.6315 DELTA=6.8460E-01 LD=2.8040E-08 KP=7.6909E-05 UO=679.3 THETA=8.2320E-02
+ RSH=4.4110E+01 GAMMA=0.6672 NSUB=1.7190E+16 NFS=5.9090E+11 VMAX=2.2420E+05
+ ETA=1.6160E-01 KAPPA=5.1440E-01 CGDO=5.0000E-11 CGSO=5.0000E-11 CGBO=4.2794E-10
+ CJ=2.8658E-04 MJ=5.3467E-01 CJSW=1.3469E-10 MJSW=1.0000E-01 PB=9.9000E-01)
.MODEL CMOSP PMOS (LEVEL=3 PHI=0.700000 TOX=3.0500E-08 XJ=0.200000U TPG=-1
+ VTO=-0.7989 DELTA=1.7180E+00 LD=1.1E-09 KP=2.0198E-05 UO=178.4 THETA=8.8040E-02
+ RSH=1.1510E+02 GAMMA=0.3752 NSUB=5.4370E+15 NFS=5.5960E+11 VMAX=1.4890E+05
+ ETA=1.0030E-01 KAPPA=1.0000E+01 CGDO=5.0000E-11 CGSO=5.0000E-11 CGBO=4.0045E-10
+ CJ=2.8863E-04 MJ=4.3630E-01 CJSW=1.7894E-10 MJSW=1.0000E-01 PB=7.5965E-01)

APPENDIX B

RELATED PUBLICATIONS

The related research papers have been published in international journal and conferences. The lists of publication are listed below.

B.1: Publication Paper in International Journal

1. Montree Kungern, **Usa Torteanchai**, Kobchai Dejhan, "Voltage-Controlled Floating Resistor Using DDCC," *Radioengineering Journal*, vol. 20, no. 1, pp. 1-7, April 2011.

B.2: Publication Paper in International Conferences

1. M. Kumngern, **U. Torteanchai**, K. Dejhan, "Electronically Tunable Multiple-Input Single-Output Voltage-Mode Multifunction Filter Employing Simple CMOS OTAs," *2010 IEEE Asia Pacific Conference on Circuits and Systems(APCCAS 2010)*, Kuala Lumpur, Malaysia, December 6-9, 2010.

2. M. Kumngern, **U. Torteanchai**, K. Dejhan, "Electronically Tunable Current-Mode Universal Filter with Three-Input Single-Output," *IEEE International Conference on Communication Systems (IEEE ICCS 2010)*, Singapore, November 17-19, 2010.

3. **U. Torteanchai**, M. Kumngern, S. Junnapiya, K. Dejhan, "Programmable voltage adder/subtractor using differential difference current conveyors," *2010 International Workshop on Information Communication Technology (ICT 2010)*, KMITL, Bangkok, Thailand, August 24-25, 2010.

4. M. Kumngern, J. Chanwutitum, **U. Torteanchai**, K. Dejhan,"Current-mode quadrature sinusoidal oscillator using translinear current conveyors," *2010 International Workshop on Information Communication Technology (ICT 2010)*, KMITL, Bangkok, Thailand, August 24-25, 2010.

5. M. Kumngern, **U. Torteanchai**, S. Junnapiya, K. Dejhan, "Current-mode first-order all-pass filter using differential difference current conveyors," *The 25th International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC 2010)*, Chonburi, Thailand, July 4-7, 2010.

6. M. Kumngern, **U. Torteanchai**, K. Dejhan, "High-input impedance voltage-mode multifuction filter using differential difference current conveyors," *The 25th International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC 2010)*, Chonburi, Thailand, July 4-7, 2010.

7. **Usa Torteanchai**, Montree Kumngern, Kobchai Dejhan "Current-Controlled CCDDCC with Controlled Current Gain," *2011 IEEE International Conference on Computer Science and Automation Engineering(CSAE 2011)*, Shanghai, China, June 10-12, 2011.

8. **Usa Torteanchai**, Montree Kumngern, Kobchai Dejhan "A CMOS Log-Antilog Current Multiplier/Divider Circuit Using DDCC," *IEEE Region 10 Conference TENCON 2011*, Bali, Indonesia, November 21-24, 2011.

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