A NOVEL VERSATILE MODULATOR CIRCUIT

PANWIT TUWANUT

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หัวข้อวิทยานิพนธ์	วงจรการมอดูเลตได้หลายประเภทแบบใหม่
นักศึกษา	นาย ปานวิทย์ ธุวะนุติ
รหัสประจำตัว	47060062
ปริญญา	วิศวกรรมศาสตรดุษฎีบัณฑิต
สาขาวิชา	วิศวกรรมไฟฟ้า
พ.ศ.	2552
อาจารย์ที่ปรึกษาวิทยานิพนธ์	รศ.ดร.ปราโมทย์ วาดเขียน
อาจารย์ที่ปรึกษาวิทยานิพนธ์ร่วม	รศ.ดร.วิภา แสงพิสิทธิ์

บทคัดย่อ

วิทยานิพนธ์ฉบับนี้เป็นการนำเสนอ วงจรการมอดูเลตได้หลายประเภทแบบใหม่ ซึ่งได้แก่ การมอดูเลตเชิงขนาด การมอดูเลตเชิงความถี่ การมอดูเลตแบบซิกมาเดลต้า และการมอดูเลตแบบเดลต้า ซึ่งการทำงานเป็นวงจรมอดูเลตแบบต่างๆ นั้น ไม่ต้องเพิ่มอุปกรณ์ใดๆ เข้าไปในวงจร วงจรดังกล่าว ก็สามารถมอดูเลตได้หลายประเภทดังที่กล่าวมาข้างต้น โดยโครงสร้างของวงจรการมอดูเลตได้หลายประเภทแบบใหม่นี้ ประกอบด้วย วงจรขยายความนำถ่ายโอน จำนวน 3 ชุด, ตัวเก็บประจุ 1 ตัว และตัวต้านทาน 2 ตัว ต่อร่วมกัน โดยอาศัยพื้นฐานจากวงจรกำเนิดสัญญาณคลื่นรูปสี่เหลี่ยม (วงจรสมิททริกเกอร์) โดยข้อได้เปรียบที่เด่นชัดของวงจรดังกล่าวคือ สามารถกำเนิดสัญญาณนาฬิกา / คลื่นพาห์ ได้ด้วยตนเอง (Clock Inherent) จึงไม่จำเป็นต้องใช้สัญญาณนาฬิกา/คลื่นพาห์ จากภายนอกเข้าสู่วงจร ยิ่งไปกว่านั้น ความถี่ และ ขนาดของสัญญาณเอาต์พุต สามารถปรับได้ โดยวิธีการทางอิเล็กทรอนิกส์ ได้อย่างเป็นอิสระต่อกัน จากโครงสร้างของวงจรที่มีขนาดเล็ก กระชับ จึงสามารถเหมาะสมที่จะนำไปสร้างเป็นวงจรรวมต่อไป ผลการจำลองแบบโดยโปรแกรมคอมพิวเตอร์โดยใช้เทคโนโลยีซีมอส เป็นการยืนยันการทำงานของวงจร ซึ่งสัมพันธ์กับการวิเคราะห์ที่ได้ในทางทฤษฎี

Thesis Title	A novel versatile modulator circuit
Student	Mr. Panwit Tuwanut
Student ID	47060062
Degree	Doctor of Engineering
Program	Electrical Engineering
Year	2009
Thesis Advisor	Assoc.Prof. Pramote Wadkien
Thesis Co-Advisor	Assoc.Prof. Wipa Sangpisit

ABSTRACT

This thesis presents a novel versatile modulator that can operate either as a delta modulator, a sigma-delta modulator, an amplitude modulator or a frequency modulator in a same circuit without adding any component. The proposed circuit mainly composes of a few components: which are three OTAs, one capacitor and two resistors which basically form square wave generator (Schmitt-trigger circuit). The advantage of this circuit is that the clock (carrier) signal employed for modulation is inherent in the circuit, no external clock (carrier) is needed. The modulating signal therefore is an external input requirement. In addition, its frequency and amplitude can be independently controlled by electronic tuning. With the compactness of the circuit, it is thus suitable for IC realization. The computer simulation based on CMOS technology demonstrates that the results agree well with the theoretical analysis.

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CHAPTER 1

Introduction

1.1 Literature review

It is well-known that modulator circuits have played a necessary part in communication systems. One reason is that the modulators can shift the spectrum of modulated signal to frequency range that is satisfied with frequency characteristic of transmission medium. In general, modulators can be classified into two main categories which are analog modulation and pulse modulation. For analog modulators, amplitude modulation and frequency modulation are mostly employed in radio and television broadcast system. On the other hand, delta modulation and sigma delta modulation, which are pulse modulation, are widely used in digital communication, digital signal processing and power system.

In a classical scheme of modulator circuit, most modulator networks were designed by using composite circuits. For example: an amplitude modulator is composed of a multiplier, an amplifier, a carrier's oscillator and a summing circuit. Based on the complication of the multiplier circuit, the collector modulator for AM is presented [1]. However, the requirement of carrier's oscillator is existed. In 1987, Comer, D., et al. submitted the loop-gain modulator [2] which the carrier is inherent in the circuit, no carrier's oscillator is needed resulting in a compact circuit. Likewise, Maneechukate, T., et al. proposed an amplitude modulation based on time-varying forced function of second-order oscillator circuit [3] in 2006. It is shown that the sinusoidal oscillator can operate as an amplitude modulator, thus the multiplier is not required, the AM modulator circuit is also compact.

In term of sigma delta modulator, the circuit is typically comprised of an integrator circuit, a comparator, a subtracting circuit and a clock generator. Next, most proposed circuits focused on the construction of circuits which either were based on switch capacitor or MOS structure [4],[11]-[14]. However, the main disadvantage of these circuits is that the clock signal was not included in the circuits. The external clock signal is thus required. In 2001, Tipsuwanporn, V., et al. presented an economical function generator and sigma delta modulator circuits [5], it is indicated that the external clock signal is not required. Moreover, among these proposed modulators, the circuits given in [9-10] can function either as delta modulator or sigma delta modulator.

As has been described above, any modulator circuit which is designed by using composite circuits will have a large scale, power consumption and low frequency range. For new trend of

technology, this kind of circuit is not suitable where a multi-mode modulator circuit [17] in a small area with low power dissipation is much preferable.

1.2 Significance of the research

Because of the disadvantages of the classical modulator circuit, it is a great significance to alleviate these problems in this research. Hence, a multi-mode modulator circuit or a versatile modulator circuit which can function either as an amplitude modulator, a frequency modulator, a delta modulator or a sigma delta modulator is proposed in this thesis. The proposed circuit is a single circuit that based on a Schmitt-trigger circuit. It is mainly composed of a few components: which are three OTAs, one capacitor and two resistors. Furthermore, the advantage of this circuit is that the clock (carrier) signal used for modulation is inherent in the circuit. The modulating signal is thus only a required external signal. With the compactness of the circuit, it is therefore suitable for IC realization and result in low power consumption.

1.3 Objective and organization of thesis

In the past, most modulator networks were designed by using complex circuits, consequently providing a large scale, power consumption and low frequency range of the modulators. In order to be fitted in a modern and portable electronic device, low power dissipation of the circuit is required. It is thus necessary to design a single modulator circuit which occupies in a small area and low power consumption. This thesis therefore presents the modulator circuit which can operate either as an amplitude modulator, a frequency modulator, a delta modulator or a sigma delta modulator.

In this thesis, it is organized into six chapters as the following:

Chapter 1 is the introduction providing the motivation for the research, and reviewing the published researches.

In chapter 2, the fundamental of modulation is provided. It is started with a brief introduction of analog modulation which is an amplitude modulation and a frequency modulation. Next, it is followed by the digital modulation which is a delta modulation. The last section of the chapter, a sigma delta modulation is presented. The significant parameters of each modulation technique discussed in this chapter will be employed to describe and analyze the behaviour of the modulator circuit in chapter 4.

In chapter 3, a brief description of a balanced OTA is mentioned. This includes a description of the circuit's function and shows the significant parameter such as gain bandwidth product, slew rate of the circuit. Also, the procedure to design a balanced OTA is presented.

Chapter 4 describes a novel versatile modulator circuit that can operate either as a delta modulator, a sigma delta modulator, an amplitude modulator or a frequency modulator. In this chapter, the technique to modify a Schmitt-trigger circuit as a modulator circuit is fully described. For each modulator circuit, the important parameter is considered and used to explain the behaviour of the modulator's circuit. In addition, the performance of the proposed circuit in term of slew rate and the noise of OTA is also analyzed.

In chapter 5, the simulation results are demonstrated. Various characteristics of the proposed circuit such as amplitude and frequency control, the frequency response of the circuit and the temperature stability of the output frequency are shown. Then the results of applying the circuit for amplitude and frequency modulation are illustrated in both time domain and frequency domain. In addition, the waveform and the corresponding spectrum of delta modulation and sigma delta modulation are given. Furthermore, a short brief of analog layout design for the proposed circuit is introduced.

Finally, the conclusions are provided in chapter 6.

CHAPTER 2

Fundamental of modulation

In telecommunications, modulation is the process of shifting the spectrum of the information signal to frequency range that is satisfied with frequency characteristic of transmission medium. In analog modulation, the modulation is applied in response to the analog information signal, for example an audio signal or TV signal. Common analog modulation techniques are amplitude modulation and frequency modulation which are mostly used in radio and television broadcast system. In addition, pulse modulation schemes also allow the analog signal to be transferred as a digital signal. Some cases of this technique are delta modulation and sigma delta modulation which are widely employed in digital signal processing and power system.

In this chapter, the fundamental of modulation is presented. It is started with a brief introduction of an analog modulation theory which are an amplitude modulation and a frequency modulation, respectively. It is then followed by the pulse modulation which is a delta modulation in the next section. Finally, a sigma delta modulation is presented in the last section of the chapter.

2.1 Amplitude modulation

For the amplitude modulation (AM), the carrier signal's amplitude is linearly varied to an input signal. It can also be classified into AM double sideband suppressed carrier (AM-DSBSC), AM single sideband (AM-SSB) and AM with carrier or AM large carrier. Based on the complication of the demodulation in AM-DSBSC and AM-SSB, the AM with carrier is widely used in the communication, mostly in radio and television broadcast. Thus, in this section, the brief review of AM with carrier is presented.

In general, the carrier signal is a sinusoidal signal that can be written as

$$c(t) = A_C \cos(\omega_C t), \tag{2.1}$$

where A_C is an amplitude of a carrier and ω_C is a carrier's frequency. Then amplitude modulation is created by

$$\phi_{AM}(t) = [A + m(t)] \cdot c(t) \tag{2.2}$$

$$= [A + m(t)] \cdot A_C \cos(\omega_C t), \tag{2.3}$$

where A represents a constant.

From Eq.(2.3), if A is large enough, the magnitude of the modulated waveform will be proportional to $m(t)$, so that $|A + m(t)| \geq 0$ at all time, or

$$A \geq |m(t)|_{\min}. \tag{2.4}$$

For a special case of single frequency sinusoidal modulation signal, which is $m(t) = A_m \cos(\omega_m t)$, the relative proportion of information's magnitude and carrier's magnitude are defined as a modulation index of AM waveform which is obtained by

$$\text{modulation index} = \frac{|m(t)|_{\min}}{|A|}. \tag{2.5}$$

By substituting $m(t) = A_m \cos(\omega_m t)$ into Eq.(2.3) and it is assumed that $A_C = 1$, it thus yields

$$\phi_{AM}(t) = [A + A_m \cos(\omega_m t)] \cdot \cos(\omega_C t) \tag{2.6}$$

$$\phi_{AM}(t) = A\cos(\omega_C t) + \frac{A_m}{2}\cos((\omega_C + \omega_m)t) + \frac{A_m}{2}\cos((\omega_C - \omega_m)t). \tag{2.7}$$

where $m(t)$ is an input signal, $c(t)$ is a carrier signal, A represents an amplifier's gain.

From Eq.(2.7), the modulated signal has three components which are a carrier wave and two sinusoidal waves (known as sidebands). Since both sidebands contain the carrier component, therefore, this type of AM is called AM with carrier as the system shown in Fig.2.1. Moreover, the bandwidth of AM with carrier can be determined by computing the difference between the highest frequency component and the lowest frequency component, which is

$$\text{bandwidth} = (\omega_C + \omega_m) - (\omega_C - \omega_m) = 2\omega_m. \tag{2.8}$$

In addition, it is noticed that if A in Eq.(2.7) is zero, the carrier component is eliminated. In this case, it is called AM double sideband suppressed carrier (AM-DSBSC).

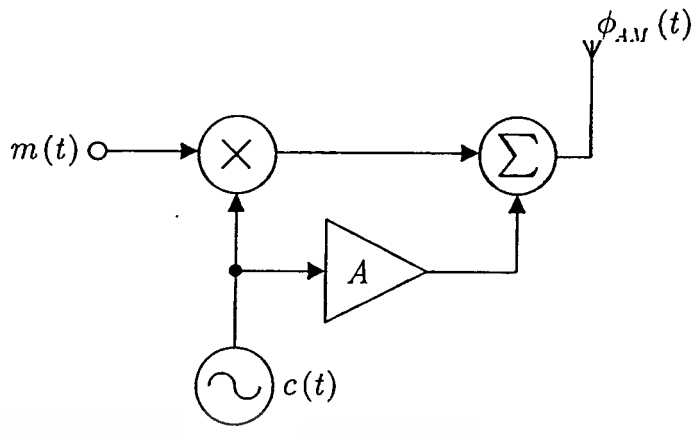


Fig.2.1. AM with carrier modulator system

Performance of AM with carrier

In AM with carrier signal, the message signal is contained in the sidebands (see Eq.(2.7)). Thus, the power is wasted in sending the carrier component. In general, the performance of AM with carrier can be defined as

$$\text{Efficiency} = \frac{P_{sideband}}{P_{total}}. \tag{2.9}$$

Under the best condition where modulation index is 100%, the efficiency at best is found to be 33% where 67% of the total power is wasted in the carrier. For other case which modulation index is lower than 100%, the efficiency of AM with carrier will of course be less than 33%.

AM with carrier demodulation

Based on the modulated waveform, it is found that the amplitude is linearly varied with the message signal. The envelope of the AM signal thus represents the message signal. The envelope detector then is the most popular that is used to directly detect the envelope of the modulated signal. The block diagram of the envelope detector is demonstrated in Fig.2.2.

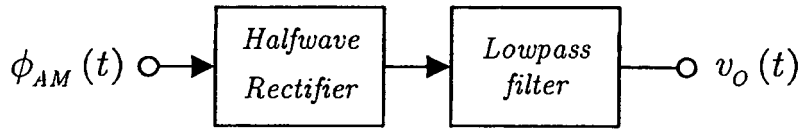


Fig.2.2. Block diagram of the envelope detector

The rectifier output is found to be

$$V_r(t) = \begin{cases} \phi_{AM}(t), & \phi_{AM}(t) > 0 \\ 0 \quad , & \phi_{AM}(t) \le 0 \end{cases}, \tag{2.10}$$

it can be rewritten as

$$V_r(t) = \phi_{AM}(t) \cdot p(t), \tag{2.11}$$

$$p(t) = \begin{cases} 1 \quad , & \phi_{AM}(t) > 0 \\ 0 \quad , & \phi_{AM}(t) \le 0 \end{cases}, \tag{2.12}$$

where $p(t)$ is a square wave whose frequency is ω_C, that is

$$p(t) = \frac{1}{2} + \frac{2}{\pi}\sum_{n=0}^{\infty} \frac{\sin(2n+1)}{2n+1}\omega_C t. \tag{2.13}$$

By Substituting Eq.(2.3) and Eq.(2.13) into Eq.(2.11), then

$$V_r(t) = \left[\left[A + m(t)\right] \cdot A_C \cos\left(\omega_C t\right)\right] \cdot \left[\frac{1}{2} + \frac{2}{\pi}\sum_{n=0}^{\infty} \frac{\sin(2n+1)}{2n+1}\omega_C t\right]. \tag{2.14}$$

The lowpass filter is used to filter out the component at ω_C and the higher harmonics, the output will be

$$v_O(t) = \frac{\left[A + m(t)\right] \cdot A_C}{\pi}. \tag{2.15}$$

It is found that the output signal is a message signal and a DC term. In addition, it is noted that the system shown in Fig.2.2 is not complicate, so it is the reason why the AM-with carrier is widely used than AM-DSBSC and AM-SSB.

2.2 Frequency modulation

For frequency modulation, the information signal $(m(t))$ is the factor that vary the carrier's frequency. Based on the modulation index (β), FM can be categorized into narrow band FM and wideband FM. If the FM modulation index is less than 0.5, it is the narrowband FM. The bandwidth of narrow band FM can be determined by

$$BW_{NBFM} = 2\omega_m, \tag{2.16}$$

where ω_m is frequency of the information signal.

For the case that β is larger than 0.5, it gives the wideband FM. To determine bandwidth of the wideband FM, the Carson's rule is used to approximate, which is

$$BW_{WBFM} \approx 2(\beta + 1)\omega_m. \tag{2.17}$$

For frequency modulation, it is well-known that the instantaneous frequency of FM is directly proportional to the input signal, as given by

$$\omega_i = \omega_C + k_f m(t), \tag{2.18}$$

where ω_C is carrier signal's frequency and k_f represents modulation sensitivity. Let the sinusoidal modulating signal be

$$m(t) = A_m \cos(\omega_m t). \tag{2.19}$$

then Eq.(2.18) can be rewritten as

$$\omega_i = \omega_C + k_f A_m \cos(\omega_m t). \tag{2.20}$$

Now let the peak frequency deviation be defined by

$$\Delta\omega = k_f A_m . \tag{2.21}$$

Hence,

$$\omega_i = \omega_C + \Delta\omega \cos(\omega_m t). \tag{2.22}$$

In addition, it is found that phase of FM signal is

$$\theta(t) = \omega_C t + \frac{\Delta\omega}{\omega_m}\sin(\omega_m t) = \omega_C t + \beta \sin(\omega_m t), \tag{2.23}$$

where

$$\beta = \frac{\Delta\omega}{\omega_m} \tag{2.24}$$

is called FM modulation index. Therefore, the FM signal is defined as

$$\phi_{FM}(t) = A_C \cos(\omega_C t + \beta \sin(\omega_m t)). \tag{2.25}$$

By applying a trigonometry's formula into Eq.(2.25), it then can be rewritten as

$$\phi_{FM}(t) = A_C \cos(\omega_C t)\cos(\beta \sin(\omega_m t)) - A_C \sin(\omega_C t)\sin(\beta \sin(\omega_m t)). \tag{2.26}$$

Using a Taylor's series for a small β $(\beta < 0.5)$, it yeilds

$$\cos(\beta \sin(\omega_m t)) \approx 1, \tag{2.27}$$

$$\sin(\beta \sin(\omega_m t)) \approx \beta \sin(\omega_m t). \tag{2.28}$$

Thus, Eq.(2.26) can be reformed as

$$\phi_{FM}(t) = A_C \cos(\omega_C t) - A_C \beta \sin(\omega_C t)\sin(\omega_m t), \tag{2.29}$$

$$\phi_{FM}(t) = A_C \cos(\omega_C t) - \frac{A_C \beta}{2}\cos\left((\omega_C - \omega_m)t\right) + \frac{A_C \beta}{2}\cos\left((\omega_C + \omega_m)t\right). \quad (2.30)$$

Similarly to AM, it is seen that the modulated signal shown in Eq.(2.30) is composed of carrier wave and two sidebands. For bandwidth of FM. it can be computed from the difference between the highest frequency component and the lowest frequency component as given by

$$\text{bandwidth} = (\omega_C + \omega_m) - (\omega_C - \omega_m) = 2\omega_m. \quad (2.31)$$

With the condition of a small $\beta\ (\beta < 0.5)$ that provide such bandwidth, this type of FM is called the narrowband FM.

For the larger $\beta\ (\beta \geq 0.5)$ which otherwise provides the wideband FM, Eq.(2.27) and Eq.(2.28) cannot be directly applied into Eq.(2.26). In this case, Fourier series is used to analyze the spectrum of the FM signal as following

$$\phi_{FM}(t) = \mathrm{Re}\left\{A_C e^{j\omega_C t} \cdot e^{j\beta\sin(\omega_m t)}\right\}. \quad (2.32)$$

By expanding term $e^{j\beta\sin(\omega_m t)}$ with Fourier's series, which is

$$e^{j\beta\sin(\omega_m t)} = \sum_{n=-\infty}^{\infty} F_n e^{jn\omega_m t}, \quad (2.33)$$

where

$$F_n = \frac{1}{T}\int_{-T/2}^{T/2} e^{j\beta\sin(\omega_m t)} e^{-jn\omega_m t} dt. \quad (2.34)$$

This integral can be evaluated numerically in term of the parameter β and n, denoted by $J_n(\beta)$ which is called a Bessel function of the first kind of order n and argument β. Using these results, Eq.(2.33) can be expressed as

$$e^{j\beta\sin(\omega_m t)} = \sum_{n=-\infty}^{\infty} J_n(\beta) e^{jn\omega_m t}, \quad (2.35)$$

and Eq.(2.32) becomes

$$\phi_{FM}(t) = \mathrm{Re}\left\{A_C e^{j\omega_C t} \cdot \sum_{n=-\infty}^{\infty} J_n(\beta) e^{jn\omega_m t}\right\}, \tag{2.36}$$

$$\phi_{FM}(t) = A_C \sum_{n=-\infty}^{\infty} J_n(\beta)\cos(\omega_C + n\omega_m)t. \tag{2.37}$$

From Eq.(2.37), it is noticed that the FM signal has an infinite sideband. However, the magnitude of the spectrum components of high order sidebands are insignificant as demonstrated in Fig.2.3.

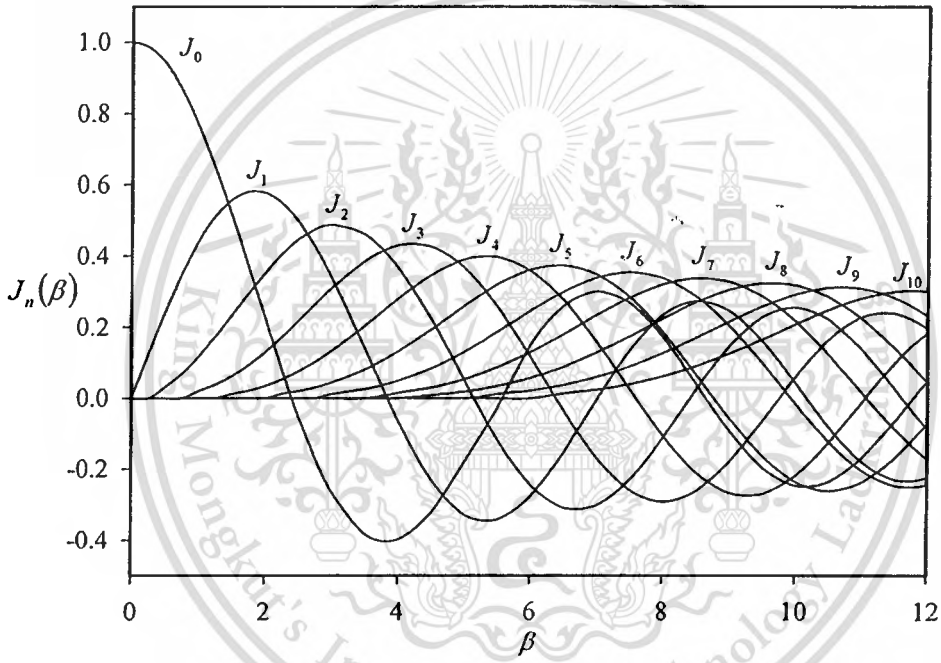


Fig.2.3. Plot of Bessel function of the first kind

Therefore, bandwidth of the FM signal with large β depends on number of significant sidebands which are based on the value of β. However, J.R.Carson proposed the approximation of a FM's bandwidth which is defined by

$$BW_{WBFM} \approx 2(\beta + 1)\omega_m. \tag{2.38}$$

and it is called Carson's rule.

FM demodulation

There are many techniques to recover the modulating signal from the FM waveform. In this section, only a direct method is discussed. A block diagram of the direct method is shown in Fig.2.4.

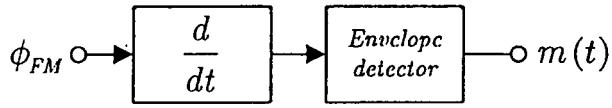


Fig.2.4. A direct method

The general FM waveform is

$$\phi_{FM}(t) = A_C \cos\left[\omega_C t + k_f \int m(t)\,dt\right]. \tag{2.39}$$

Then, the differentiated output is

$$\phi'_{FM}(t) = -\left(\omega_C + k_f m(t)\right) A_C \cos\left[\omega_C t + k_f \int m(t)\,dt\right]. \tag{2.40}$$

It is noticed that Eq.(2.40) is in the form of AM with carrier's signal. Thus, the envelope detector circuit is used to detect an envelope of the modulated signal directly.

2. 3 Delta modulation

Pulse code modulation (PCM) is a technique that is known as an analog to digital signal conversion and used for voice transmission. The magnitude of the signal is sampled regularly at uniform intervals, and then quantized to a series of symbols in a binary code. But the major disadvantage of PCM is that there exists data redundancy in encoding digital signal. To alleviate this problem, the difference between a current sample and its predicted value has been instead encoded. Such technique is well-known as differential pulse code modulation (DPCM). For a special case of DPCM which provides one-bit encoding output, it is known to be delta modulation (DM), whose encoder system is shown in Fig.2.5 where $x(t)$ is an input signal , $\bar{x}(t)$ is a predicted signal and $y(t)$ is a delta modulation's signal.

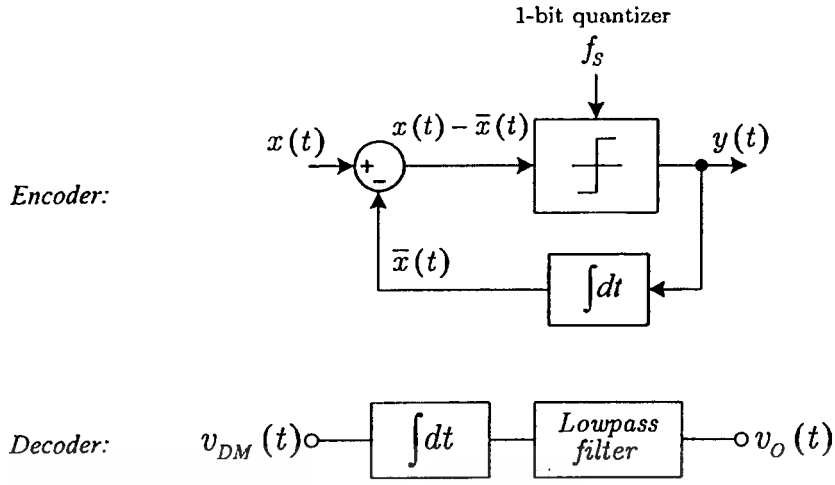


Fig.2.5. Delta modulator system

From Fig.2.5, when an input signal is present, it is compared with a predicted signal that accomplished by successive steps, either up or down, by a step size (a) which resulted from integrating a digital output signal. The difference signal $x(t) - \overline{x}(t)$ is then fed to 1-bit quantizer. If the difference signal is positive then the predicted signal will be increased with step size a, and output logic is high. If the difference signal is negative then the predicted signal is decreased with step size a, and output logic is low. The delta modulator output can be demonstrated in Fig.2.6.

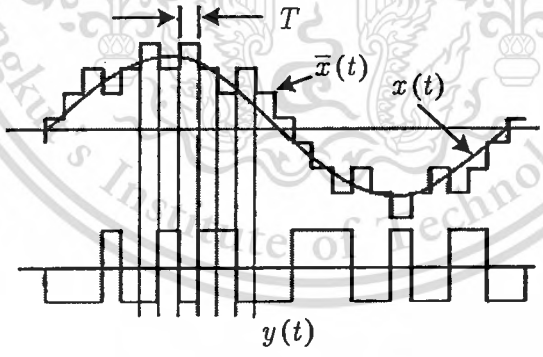


Fig.2.6. Delta modulation's signal

Since the output of the 1-bit quantizer in the encoder is a stepped approximation of the input signal. Therefore, an integrator is used to estimate the original signal where a low pass filter is employed to smooth the recovered signal.

Distortion of Delta modulation

In general, there are two types of distortion occurred in delta modulation as follow.

1. Slope overload distortion

This type of distortion is due to the use of too small step size. It then cannot follow portions of the waveform that have a steep slope as shown in Fig.2.7.

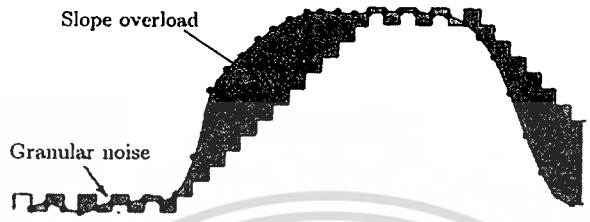


Fig.2.7. Delta modulation's distortion

The rate of rise, or slope overload in the approximation of the input signal, can be determined from the changing of an input signal related to the changing of time. In case that, the input signal $m(t)$ is assumed to be $A\cos(2\pi ft)$, then the slope overload is

$$\left|\frac{dm(t)}{dt}\right|_{max} = A2\pi f. \tag{2.41}$$

If the step size is a, then the slope of step size is

$$\text{Slope of step size} = \frac{a}{T} = af_s. \tag{2.42}$$

Hence, to avoid the slope overload distortion

$$af_s \geq A2\pi f. \tag{2.43}$$

From Eq.(2.43), the slope overload distortion can be reduced by

- Increasing the sampling frequency (f_s),however, it also increases an output's bit rate.
- Increasing the step size (a), but it similarly gains the quantization error.

2. Granular noise (also called as quantization error)

This distortion results from using too large step size. From Eq.(2.43), it indicates that if $af_s \geq A2\pi f$, then the slope overload distortion will have no effect. Therefore, the quantization error is considered. Assume that the quantization error is uniformly distributed over the interval $[-a, a]$, then the mean square quantization error is $a^2/3$. To measure quantization error, it is assumed that its power spectrum density is constant to $f_s = \frac{1}{T}$. Moreover, if the filter has a bandwidth f_m where $f_m \leq f_s$, then the mean squared quantization error is

$$N = \overline{n_{qnt}^2(t)} = \frac{a^2}{3} \cdot \frac{f_m}{f_s}. \tag{2.44}$$

The mean square of the input signal is $\overline{m^2(t)}$, thus the signal to quantization noise ratio is

$$\frac{S}{N} = \frac{3}{a^2} \cdot \frac{f_s}{f_m} \overline{m^2(t)} \tag{2.45}$$

From Eq.(2.45), the granular noise can be reduced by decreasing the step size. To consider the detail, let $m(t)$ be $A\cos(2\pi ft)$, the mean squared value be $\frac{A^2}{2}$. In addition, using Eq.(2.43) to eliminate slope overload distortion, a step size is specified to $a = \frac{A2\pi f}{f_s}$ so that

$$\frac{S}{N} = \frac{3}{8\pi^2} \cdot \frac{f_s^3}{f_m f^2} \tag{2.46}$$

In general, the amplitude of an input signal should be covered in a dynamic range which is $(A_{max}/A_{min})^2$, where A_{max} and A_{min} are the maximum amplitude of an input signal and minimum amplitude of an input signal, respectively. In addition, the signal to noise ratio is minimum when the amplitude of an input signal is A_{min}. Since, the step size is designated by A_{max}, thus $a = \frac{A_{max}2\pi f}{f_s}$ and Eq.(2.45) is rewritten to

$$\begin{aligned} \frac{S}{N} &= \frac{3}{8\pi^2} \cdot \frac{f_s^3}{f_m f^2} \cdot \frac{A_{min}^2}{A_{max}^2} \\ &= \frac{3}{8\pi^2 DR} \cdot \frac{f_s^3}{f_m f^2} \end{aligned} \tag{2.47}$$

Effect of quantization noise in a delta modulation system

To analyze the characteristics of the delta modulator, the Laplace transform is used to model it in the frequency domain as illustrated in Fig.2.8. The integrator is replaced with a transfer function 1/s and the quantizer is modeled as a noise source N(s).

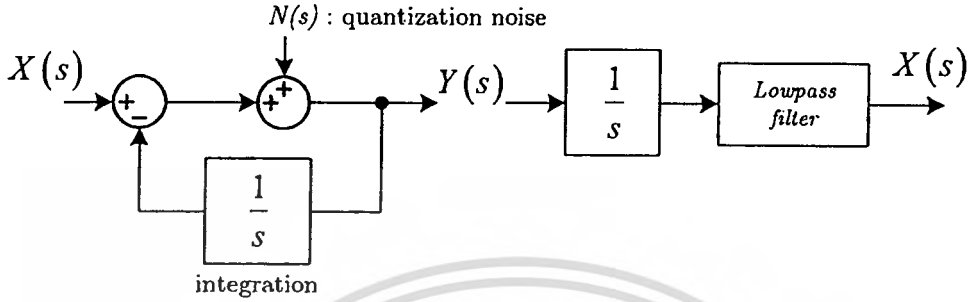


Fig.2.8. Delta modulation system

Signal transfer function

To examine a signal transfer function, the quantization noise is set to be zero, then

$$Y(s) = X(s) - \frac{Y(s)}{s} \tag{2.48}$$

$$\frac{Y(s)}{X(s)} = \frac{s}{s+1} \tag{2.49}$$

From Eq.(2.49), the magnitude response of the signal transfer function is shown in Fig.2.9, which is seen to be a high pass filter.

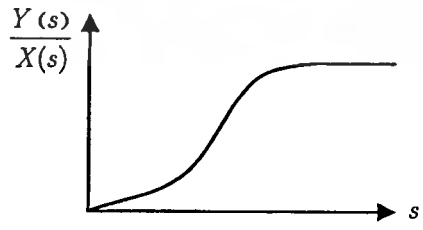


Fig.2.9. Magnitude response of signal transfer function (DM system)

Noise transfer function

To analyze a noise transfer function, the input's signal is set to be zero, then the following result is obtained

$$Y(s) = N(s) - \frac{Y(s)}{s} \tag{2.50}$$

$$\frac{Y(s)}{N(s)} = \frac{s}{s+1} \tag{2.51}$$

From Eq.(2.51), the magnitude response of noise transfer function is a high pass filter that is similar to that of the signal transfer function.

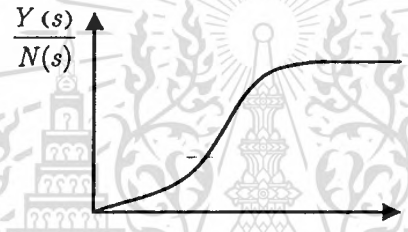


Fig.2.10. Magnitude response of noise transfer function (DM system)

Since the signal transfer function and noise transfer function occupy the same frequency response, hence, no filter can remove quantization noise from the modulated signal.

2.4 Sigma delta modulation

For the delta modulation, its output signal is found to be a differentiated version of the input signal. The integrator is therefore needed for the demodulation process. Hence, to omit the integrator in the demodulator, the input signal must be integrated before the modulation. Since an integrator operator is a linear function, i.e., $e(t) = \int v_{in}(t)\,dt - \int v_{DM}(t)\,dt = \int \left(v_{in}(t) - v_{DM}(t)\right) dt$, a single integrator is only required in the modulator. The resulted system as depicted in Fig.2.11 is well-known to be a sigma delta modulation system.

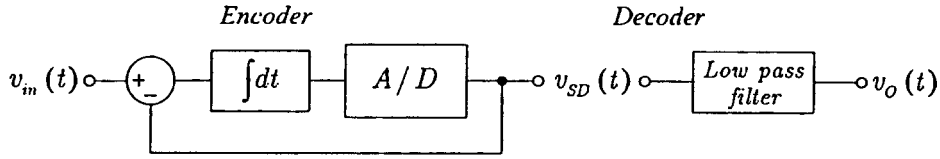


Fig.2.11. Sigma delta modulation system

Effect of quantization noise in a sigma delta modulation system

To examine the characteristics of the sigma delta modulator, the model in the frequency domain of the system is employed as shown in Fig.2.12. The integrator is replaced with a filter whose transfer function is $H(s) = 1/s$ and the quantizer is modeled as a noise source whose noise contribution is $N(s)$.

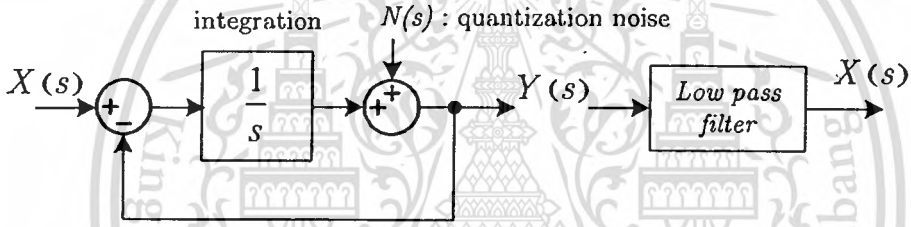


Fig.2.12. Sigma delta modulation system in frequency domain realization

Signal transfer function

By letting $N(s)$ be zero for the moment, and solving for $Y(s)/X(s)$, the following result is obtained

$$Y(s) = (X(s) - Y(s))\frac{1}{s} \tag{2.52}$$

$$\frac{Y(s)}{X(s)} = \frac{1}{s+1} \tag{2.53}$$

From Eq.(2.53), the magnitude response of signal transfer function is shown in Fig.2.13, which is a low pass filter.

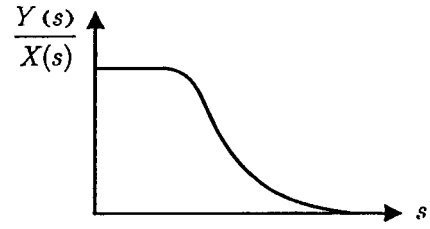


Fig.2.13. Magnitude response of signal transfer function (Sigma delta modulation)

Noise transfer function

By letting the signal $X(s) = 0$ and solving for $Y(s) / N(s)$ that is

$$Y(s) = N(s) - \frac{Y(s)}{s} \tag{2.54}$$

$$\frac{Y(s)}{N(s)} = \frac{s}{s+1} \tag{2.55}$$

From Eq.(2.55), the magnitude response of noise transfer function is depicted in Fig.2.14. It is seen to be a high pass filter.

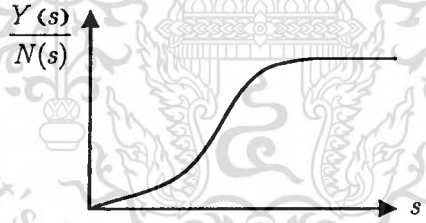


Fig.2.14. Magnitude response of noise transfer function (Sigma delta modulation)

By examining Eq.(2.53) and Eq.(2.55) above, they indicate that the modulator acts as a low pass filter for the input signal and a high pass filter for noise. As the result, in the lower frequency band, the desired input signals are passed, while the noise is suppressed to a great extent which is called a noise shaping. The sigma delta modulation thus provides higher SNR compared to the delta modulation.

CHAPTER 3

Operational transconductance amplifier

Operational tansconductance amplifier (OTA) is a device that converts an input voltage to an output current. Its property is thus identical to a voltage controlled current source (VCCS) where the ratio of output current to input voltage is called transconductance gain. The characteristics of the ideal OTA are high input impedance, high output impedance and the transconductance parameter is controlled by an external bias current.

In general, OTA is constructed by semiconductor with bipolar or CMOS technology. In addition, there are several topologies of OTA such as the single stage topology, the multi-stage cascode topology, the folded-cascode topology, the telescopic topology and the balanced topology. To select an optimal topology for the OTA, several fundamental principles and trade offs are required for consideration based on the specific requirements.

In this chapter, the discussion of the balanced OTA is briefly reviewed in the first section. Next section, the important parameters such as gain bandwidth product, slew rate are introduced. Finally, design procedure of the balanced OTA is described.

3.1 Balanced OTA

A CMOS balanced OTA is a single stage topology which is realized with a differential pair (M_1 - M_2) as input stage and three current mirrors (M_3 - M_8) as depicted in Fig. 3.1.

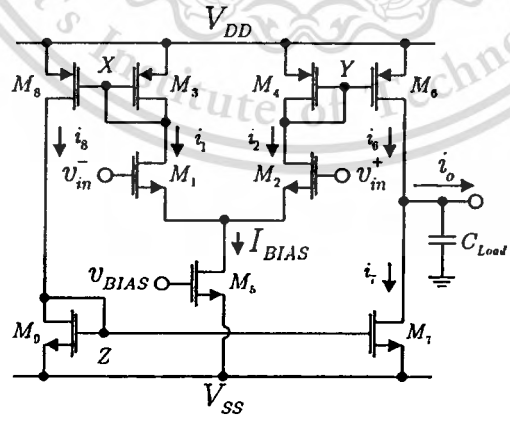


Fig. 3.1. A CMOS balanced operational transconductance amplifier

Circuit operation

Based on the circuit given in Fig.3.1, let the MOSFET M_1 and M_2 be matched, and the current mirrors have unity current gain and all MOSFETs are biased in order to operate in saturation region. In the circuit, the current i_2 is a reference current of the current mirror that is composed of the transistor M_4 and M_6, then $i_6 = i_2$. Likewise, the current i_1 is a reference current of the current mirror that is comprised of the transistor M_3 and M_8, thus $i_8 = i_1$. Also, the current i_8 is a reference current of the current mirror that is comprised of the transistor M_7 and M_9, thus $i_7 = i_8$. The output current is then found to be

$$i_o = i_6 - i_7 = i_2 - i_1 \tag{3.1}$$

and is equal to the different current in the differential pair M_1 and M_2. Thus,

$$i_o = g_m v_{in} \tag{3.2}$$

where the transconductance is

$$g_m = \sqrt{\mu_n C_{OX} \left(W/L\right)_{1,2} I_{BIAS}} \tag{3.3}$$

and μ_n is a carrier mobility, C_{OX} is a gate capacity per unit area, $\left(W/L\right)_{1,2}$ is an aspect ratio of M_1 and M_2 and I_{BIAS} is an external bias current.

3.2 Parameters of OTA

3.2.1 Gain bandwidth product

For the expression of the dc open-loop gain and the dominant pole of OTA, they are known to be $A_v = g_{m1,2}R_{out}$ and $f_{pole} = 1/\left(2\pi R_{out}C_{Load}\right)$, respectively, where $g_{m1,2}$ is the small-signal transconductance of M_1 and M_2, R_{out} and C_{Load} are the equivalent resistance and capacitance at the output node. Therefore, the gain bandwidth product (GBW) is given by

$$GBW = g_{m1,2} / \left(2\pi C_{Load}\right). \tag{3.4}$$

The first internal pole of OTA at the internal node X is determined by the total capacitance C_X at the internal node X and the transconductance g_{m3} of M_3 as follows

$$f_X \approx g_{m3} / (2\pi C_X). \tag{3.5}$$

The capacitance C_X is the sum of intrinsic, overlap, and drain-substrate capacitances of M_3, M_8, and M_1 connected to the node X which is

$$C_X = C_{GS3} + C_{GS8} + C_{GSO3} + C_{GSO8} + C_{GDO8} + C_{BD3} + C_{BD1} + C_{GDO1}, \tag{3.6}$$

where

C_{GS} : Gate-source intrinsic capacitance,

C_{GSO} : Gate-source overlap capacitance,

C_{GDO} : Gate-drain overlap capacitance,

C_{BD} : Drain-substrate capacitance.

By considering only the significant intrinsic capacitance which is the capacitance between gate and source, it yields

$$C_X \approx C_{GS3} + C_{GS8}. \tag{3.7}$$

Likewise, the internal poles of OTA at node Y and node Z respectively are

$$f_Y \approx g_{m4} / (2\pi C_Y), \tag{3.8}$$

$$f_Z \approx g_{m9} / (2\pi C_Z). \tag{3.9}$$

Similarly, the capacitance C_Y and C_Z at the node Y and Z respectively are

$$C_Y \approx C_{GS4} + C_{GS6}, \tag{3.10}$$

$$C_Z \approx C_{GS7} + C_{GS9}. \tag{3.11}$$

Practically, the condition $2GBW < \min[f_X, f_Y, f_Z]$ achieves a phase margin greater than 45°.

3.2.2 Slew rate

In this circuit, the maximum current delivered to the load is I_{BIAS}, the slew rate then will be

$$\text{Slew rate} = \frac{I_{BIAS}}{C_{Load}} \tag{3.12}$$

where C_{Load} is the capacitance at the output node. To avoid limitation of settling time by slew rate, I_{BIAS} should be large enough. However, the increasing in I_{BIAS} leads to the increasing in static power dissipation.

3.3 Design procedure

Design procedure for the conventional OTA

In modern wireless and portable electronics, low weight and small size of the battery, including low voltage operation and low power dissipation are required to extend battery lifetime. But, for high-speed operation, fast OTA settling response is required which demands both high slew rate and wide bandwidth. Hence, there exists traded-off between static power consumption and slew rate which must be well compromised.

In the following design procedure, it is assumed that the specifications of the following parameters are given: load capacitance, output voltage swing, power dissipation, unity gain-bandwidth product, slew rate, gain at dc and input common mode range. Then, the design procedure is listed as following steps:

Step 1. The maximum bias current is determined by considering the power dissipation and the slew rate specifications of the circuit, which are

$$P_{diss} = I_{BIAS} \cdot (V_{DD} - V_{SS}). \tag{3.13}$$

$$\text{Slew rate} = \frac{I_{BIAS}}{C_{Load}}. \tag{3.14}$$

Step 2. Next, by using the unity gain-bandwidth product, the transconductance of M_1, M_2 is defined which is

$$g_{m1,2} = 2\pi C_{Load} \cdot GBW. \tag{3.15}$$

Step 3. From the previous step, by using at least 2 parameters which are I_D and g_m of M_1, M_2, an aspect ratio W/L of M_1, M_2 then is

$$\left(\frac{W}{L}\right)_{1,2} = \frac{g_m^2}{2K_N I_D} \qquad \text{where } K_N = \frac{1}{2}\mu_n C_{OX}. \tag{3.16}$$

Step 4. By assuming that the MOS diode loads of M_3, M_4 run in saturation region, the aspect ratio W/L of M_3, M_4, M_6 and M_8 can be calculated by

$$\left(\frac{W}{L}\right)_{3,4,6,8} = \frac{2I_D}{K_P\left(V_{DS}(sat)\right)^2} \tag{3.17}$$

where $V_{DS}(sat) = \dfrac{V_{DD} - V_{out(max)}}{2}$ and $K_P = \dfrac{1}{2}\mu_P C_{OX}$.

To consider the worst case scenario, let $I_D = I_{BIAS}/2$. In this step, if the aspect ratio W/L is very large then the bandwidth is affected by the internal poles at the node *X, Y*.

Step 5. Similar to the previous step, the aspect ratio W/L of M_7, M_9 can be determined as follows

$$\left(\frac{W}{L}\right)_{7,9} = \frac{2I_D}{K_N\left(V_{DS}(sat)\right)^2} \tag{3.18}$$

where $V_{DS}(sat) = \dfrac{V_{out(min)} - V_{SS}}{2}$ and $I_D = I_{BIAS}/2$ is considered for the worst case.

Step 6. In this step, $V_{DS5}(sat)$ is considered from the common mode case which is

$$V_{DS5}(sat) = V_{icm(min)} - V_{GS1} \tag{3.19}$$

where V_{icm} is an input common mode voltage.

Step 7. The aspect ratio W/L of M_5 then is

$$\left(\frac{W}{L}\right)_5 = \frac{2I_D}{K_N\left(V_{DS5}(sat)\right)^2}. \tag{3.20}$$

Step 8. To verify the designed OTA, the gain specification is examined by

$$A_V = g_{m1} R_{out} = \frac{g_{m1}}{I_{BIAS}} \times \left(\frac{2}{\lambda_6 + \lambda_7} \right) \tag{3.21}$$

where λ_i is the channel length modulation of the i'th MOS.

If the gain specification is not satisfied, it can be adjusted by increasing the aspect ratio W/L of M_1 or decreasing the bias current. However, calculation of all steps must be rechecked whenever any parameter is changed to ensure that the specifications have been satisfied.

Step 9. Once all parameters are satisfied, the circuit is simulated to verify all specifications.

CHAPTER 4

A novel versatile modulator circuit

Based upon the literature reviews in chapter 1, a novel versatile modulator circuit that can operate either as a delta modulator, a sigma delta modulator, an amplitude modulator or a frequency modulator is presented in this chapter. The principle of the proposed scheme is based on a schmitt-trigger circuit which is composed of a few components such as three OTAs, one capacitor and two resistors. In addition, the advantage of this circuit is that the clock (carrier) signal employed for modulation is inherent in the circuit. Therefore, the modulating signal is just only one requirement for an external input. With the compactness of the circuit, it is then suitable to be fabricated for integrated circuit.

The organization of this chapter will be arranged as follows. In section I, the principles of a pulse generator is discussed. For section II, a delta modulator, a sigma delta modulator, an amplitude modulator and a frequency modulator are described. Finally the performance analysis such as a frequency error by slew rate of the OTA and a noise of the OTA are given in section III.

4.1 A pulse generator circuit

In this section, a pulse generator which has played an important role in this work is presented. The proposed circuit employed here is basically modified from the Schmitt trigger circuit [15]-[17] as illustrated in Fig.4.1.

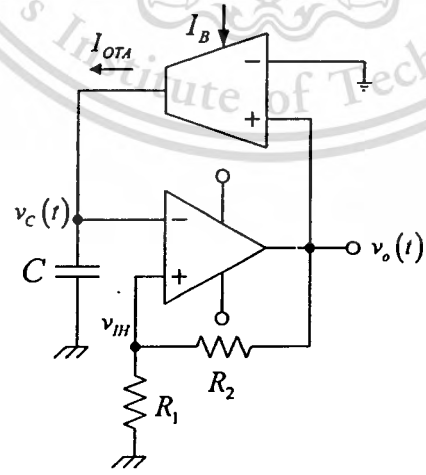


Fig.4.1. Schmitt trigger circuit

Basically, the OTA is considered as an adjustable resister, which is controlled by bias current (I_B), where the Op-Amp, the capacitor C and the resisters R_1, R_2 are cooperated to function an inverting Schmitt trigger circuit. But the disadvantage of this scheme is high sensitive to temperature. Hence, a temperature insensitive pulse generator circuit is proposed as demonstrated in Fig.4.2.(a). Moreover, to gain the ability of electrical amplitude control, the circuit given in Fig.4.2.a is further modified by replacing the Op-Amp with the OTA2 and a resister R_O which is shown in Fig.4.2.(b).

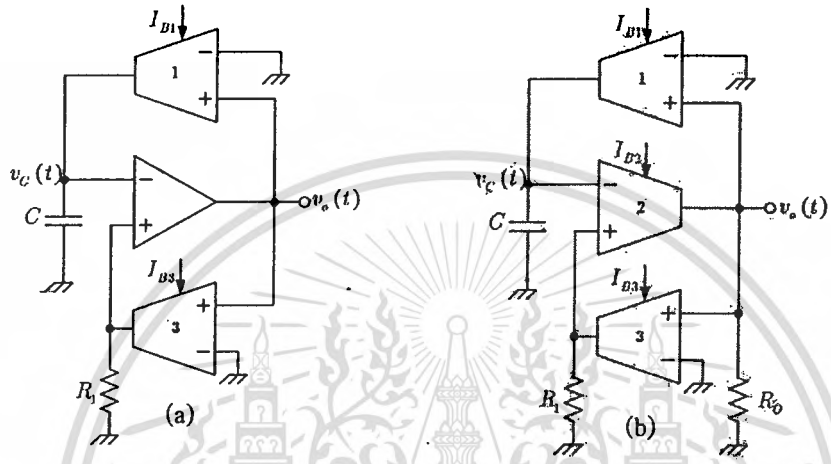


Fig.4.2. Improved pulse generator circuit

(a) for temperature-insensitive

(b) for both temperature-insensitive and electrical amplitude control

As can be seen, an OTA1 and a timing capacitor C function as an integrator whose time constant is directly proportional to the bias current I_{B1}. Next, the voltage divider circuit is achieved by a resistor R_1 and an OTA3 where the threshold level (v_{IH}, v_{IL}) is varied with the bias current I_{B3}. For the last part, an OTA2 is a comparator whose saturation voltage across a resistor R_O is directly controlled by the bias current I_{B2}.

For the operation of the proposed scheme, it can be described as follows. At the first instance, it is supposed that the voltage across the capacitor is zero ($v_C(0) = 0$) and all OTAs are operated in saturate mode. When the power supplies are turn on, the OTA2 and the OTA3 give the output current I_{OTA2} and I_{OTA3}, respectively. These currents are assumed to be in outward directions of the OTAs, then the upper threshold voltage of the OTA3 is

$$v_{IH} = I_{OTA3}R_1 . \tag{4.1}$$

Simultaneously, the output current I_{OTA1} is provided by OTA1 that causes the capacitor C to be charged. The voltage $v_C(t)$ is then linearly increased. When this voltage level is nearly close to the threshold voltage v_{IH}, the output current of the OTA2 starts to change its direction. As the result, the threshold voltage of the OTA3 is changed to its lowest level, which is

$$v_{IL} = -I_{OTA3}R_1 . \tag{4.2}$$

Suddenly, the output current of the OTA1 converts its direction and flows into the device, the capacitor C is discharged resulting in the voltage $v_C(t)$ is linearly decreased. When this voltage level is almost equal to the lower threshold voltage v_{IL}, the output current of the OTA2 starts changing its direction again. The same operation of the proposed circuit is therefore repeated, which is based on periodical charge and discharge of the capacitor. Consequently, the triangular wave and square wave are then generated which can be graphically shown in Fig.4.3.

4.1.1 Oscillation frequency

In the previous subsection, the operation of the proposed circuit and how the fundamental triangular and square wave are generated have been described. The oscillated frequency thus will be discussed in this subsection. It is noted that all of active elements employed in the circuit are assumed to be ideal.

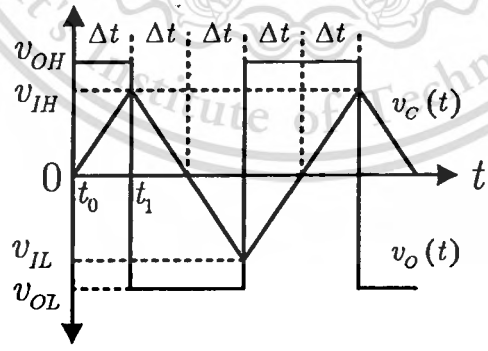


Fig.4.3. The oscillated signals of the proposed circuit

For the explanation, let us begin with the relation between voltage and current of the capacitor which is

$$i_C = C\frac{dv_C(t)}{dt}. \tag{4.3}$$

By rearranging of Eq.(4.3) that is

$$\frac{i_C}{C} = \frac{dv_C(t)}{dt} \approx \frac{v_C(t_1) - v_C(t_0)}{t_1 - t_0}. \tag{4.4}$$

As depicted in Fig.4.3, let us consider the voltage $v_C(t)$ at time t_0 and t_1, which are $v_C(t_1) = v_{IH}$ and $v_C(t_0) = 0$. Eq.(4.4) is thus rewritten to be

$$\frac{i_C}{C} = \frac{v_{IH} - 0}{t_1 - t_0} = \frac{v_{IH}}{\Delta t}. \tag{4.5}$$

It is obtained that the rising time Δt of the triangular wave then is

$$\Delta t = C\frac{v_{IH}}{i_C}. \tag{4.6}$$

Since $i_C(t) = I_{OTA1}$ and $v_{IH} = I_{OTA3}R_1$, it thus gives

$$\Delta t = CR_1\frac{I_{OTA3}}{I_{OTA1}}. \tag{4.7}$$

As can be seen in Fig.4.3, the period of oscillation is four times of the rising time Δt which is

$$T = 4\Delta t = 4CR_1\left(\frac{I_{OTA3}}{I_{OTA1}}\right). \tag{4.8}$$

Hence, the oscillation frequency readily is

$$f = \frac{1}{4CR_1}\left(\frac{I_{OTA1}}{I_{OTA3}}\right). \tag{4.9}$$

Based on the fact that all OTAs are simultaneously operated in either saturation or non-saturation mode. The operation of OTAs is therefore briefly reviewed as follows.

Case I: the OTA1 and the OTA3 are operated in saturation mode

When the OTA1 and OTA3 are operated in saturation mode, their output currents are at the maximum level which are I_{B1} and I_{B3}, respectively. The oscillated frequency of this case therefore is

$$f = \frac{1}{4CR_1}\left(\frac{I_{B1}}{I_{B3}}\right). \tag{4.10}$$

Case II: the OTA1 and the OTA3 are operated in non-saturation mode

By realizing that the OTAs are in CMOS structure, the output current of the OTAs thus are $I_{OTA1} = g_{m1}v_O(t), I_{OTA3} = g_{m3}v_O(t)$. It is noted that the transconductance of the OTA1 and the OTA3 [13] are approximately to be $g_{m1} = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_{B1}}$ and $g_{m3} = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_{B3}}$, respectively. It is also supposed that both OTAs are matched. By substituting these parameters into Eq.(4.9), it thus results in

$$f = \frac{1}{4CR_1}\sqrt{\frac{I_{B1}}{I_{B3}}}. \tag{4.11}$$

The relations in Eq.(4.10) and Eq.(4.11) show that the oscillation frequency is independent on the transconductance of the OTAs. More importantly, it implies that not only frequency is temperature-insensitive but also can be electronically adjusted by the bias currents I_{B1} and/or I_{B3}. Furthermore, when the OTA2 is in saturation mode, the peak-to-peak amplitude of the output signal is given by

$$\left|v_{o_{p-p}}(t)\right| = 2I_{B2}R_O. \tag{4.12}$$

It is noticed that, the amplitude of the output signal can be electronically adjusted by the bias current I_{B2}.

As previously described, it is obvious that the proposed circuit given in Fig.4.2.b has advantages in both temperature-insensitive and amplitude/frequency independently adjustment which are confirmed by Eq.(4.10), Eq.(4.11) and Eq.(4.12), respectively. However, the non-ideal effect of the active components will have an affect on the ideal operation which will be later discussed.

4.2 A novel versatile modulator circuit

4.2.1. Amplitude modulator circuit

Base on the characteristic of the proposed circuit that the amplitude of the pulse signal can be adjusted by electronic tuning which is confirmed by Eq.(4.12), hence if the bias current I_{B2} is an information signal, the proposed scheme then operates as an amplitude modulator as illustrate in Fig.4.4. With this concept, by assuming that the bias current I_{B2} is $I_{offset} + I_{m(t)}$, where I_{offset} is dc offset current and $I_{m(t)}$ denotes the information signal.

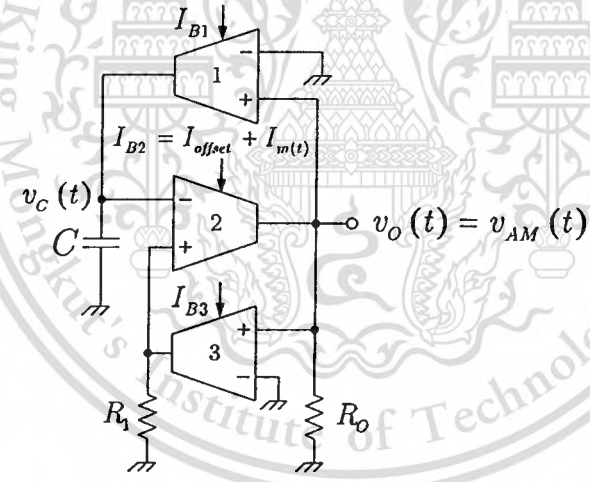


Fig.4.4. The proposed circuit for an amplitude modulator

Eq.(4.12) is then rewritten to be

$$\left|v_{o_{P-P}}(t)\right| = 2R_O\left|I_{offset} + I_{m(t)}\right|. \tag{4.13}$$

From Eq.(4.13), to eliminate the over modulation, the dc offset current I_{offset} must be large enough, the magnitude of the modulated waveform will be directly proportional to $I_{m(t)}$, so that $\left|I_{offset} + I_{m(t)}\right| \geq 0$ at all time, or

$$I_{offset} \geq \left|I_{m(t)}\right|_{\min} . \tag{4.14}$$

For a special case of a single frequency sinusoidal modulating signal, $I_m(t) = I_m \cos \omega_m t$, the relative proportion of information's magnitude and carrier's magnitude are defined as a modulation index of AM waveform, which is found to be

$$\text{modulation index} = \frac{\left|I_{m(t)}\right|_{\min}}{\left|I_{offset}\right|} . \tag{4.15}$$

Thus, the efficiency of AM can be determined.

4.2.2 Frequency modulator circuit

As described in section 4.1.1, the pulse's frequency of the proposed circuit can be electronically tuned as approved by Eq.(4.11), Eq.(4.12), then if I_{B1} performs as an information signal, the proposed scheme thus can be applied to be a frequency modulator. The frequency modulator circuit is given in Fig.4.5.

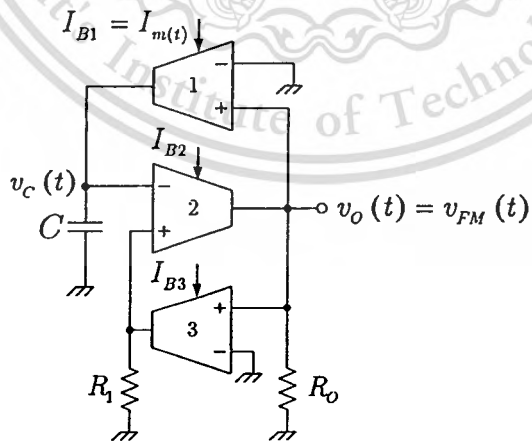


Fig.4.5. The proposed circuit for a frequency modulator

Then, by assuming that the OTA1 and the OTA3 are operated in saturation mode where the bias current I_{B1} is the information signal $I_{m(t)}$, the frequency of the FM circuit thus is

$$f = \frac{I_{m(t)}}{4CR_1 I_{B3}}. \tag{4.16}$$

The relationship in Eq.(4.16) indicates that the pulse's frequency is directly changed to the information signal. The changing ratio of the output frequency to the information signal is defined to be modulation sensitivity $\left(k_f\right)$, as given by

$$k_f = \frac{\Delta f}{\Delta I_{m(t)}} = \frac{1}{4CR_1 I_{B3}}. \tag{4.17}$$

Therefore, the peak frequency deviation (Δf), modulation index (β) and bandwidth of FM (BW) are obtained as following

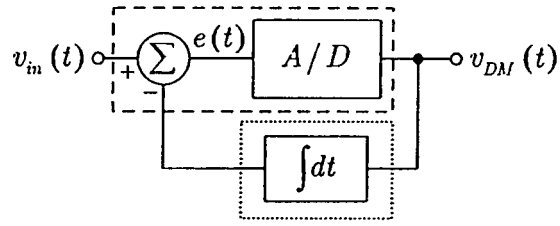
$$\beta = \frac{\Delta f}{f_m}, \tag{4.18}$$

where f_m is an information signal's frequency, and bandwidth of FM is approximate to

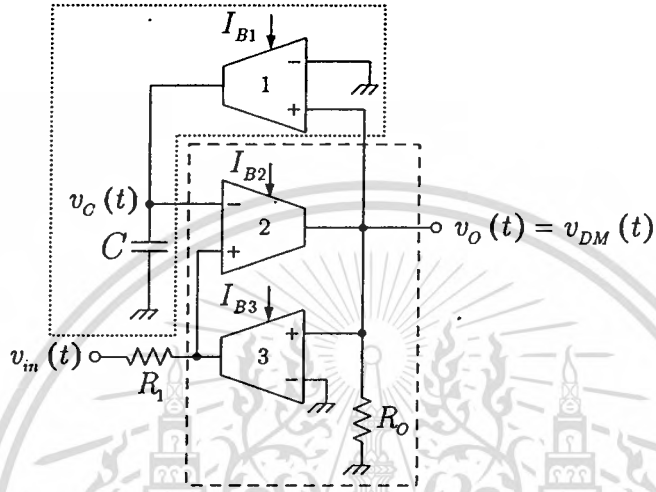
$$BW \approx 2(\beta + 1) f_m. \tag{4.19}$$

4.2.3 Delta modulator circuit

Now let us describe how the proposed circuit depicted in Fig.4.2 (b) can be applied for a delta modulator circuit. To achieve this application, the proposed circuit is slightly modified where the terminal of resistor R_1, rather than grounded, is employed to be a feeding node for the input signal. The modified circuit for a delta modulator is given in Fig.4.6 (b) which can be compared with a delta modulation system as shown in Fig.4.6 (a).



(a) Delta modulator system



(b) Delta modulator circuit

Fig.4.6. A delta modulator circuit compared with a delta modulator system

In this case, the capacitor and the OTA1 construct the integrator circuit as shown in a dot line block, where

$$v_C(t) = \frac{g_{m1}}{C}\int v_O(t)\,dt. \tag{4.20}$$

It is noticed that the integrator's gain is g_{m1}/C. When the input signal $v_{in}(t)$ is presented, it thus is compared with $v_c(t)$. The pulse output signal is therefore generated according to the different signal as shown in a dash line block in Fig.4.6 (b), that is given by

$$v_O(t) = \mathrm{sgn}\left[e(t)\right], \tag{4.21}$$

$$v_O(t) = \mathrm{sgn}\left[v_{in}(t) - \frac{g_{m1}}{C}\int v_O(t)\,dt\right]. \tag{4.22}$$

Hence, the described operation confirms that this circuit is a delta modulator circuit.

To obtain the performance of a delta modulator, step size and sampling frequency discussed in Chapter 2 are considered. In this circuit, step size can be estimated by an integrator's gain which is

$$step\ size = \frac{g_{m1}}{C}. \tag{4.23}$$

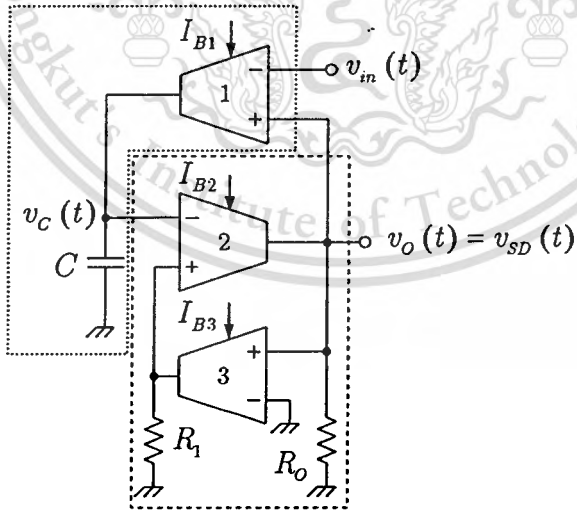
Furthermore, the sampling frequency (f_S) is inherent in the circuit as given by

$$f_S = \frac{1}{4CR_1}\left(\frac{I_{B1}}{I_{B3}}\right). \tag{4.24}$$

4.2.4 Sigma delta modulator circuit

To apply the proposed circuit to be a sigma delta modulator, it can be accomplished by feeding the input signal at the inverting node of the OTA1 as shown in Fig.4.7 (b) where a block diagram of a sigma delta modulator system is given in Fig.4.7 (a).

(a) Sigma delta modulator system



(b) Sigma delta modulator circuit

Fig.4.7. A sigma delta modulator circuit compared with a sigma delta modulator system

For the operation of the sigma delta modulator, it can be described as follows. It is seen that the capacitor and the OTA1 operate as an integrator (shown in a dot line block). Hence, when $v_{in}(t)$ is present, the difference between the input signal $v_{in}(t)$ and the output signal $v_O(t)$ is thus integrated to be $v_C(t)$ with the gain g_{m1}/C.

$$v_C(t) = \frac{g_{m1}}{C}\int[v_{in}(t) - v_O(t)]dt. \tag{4.25}$$

When $v_C(t)$ is compared with the threshold voltage either v_{OH} or v_{OL}, it results in $v_O(t)$ which obviously is the sigma delta modulator output (displayed in a dash line block).

$$v_O(t) = \mathrm{sgn}[v_C(t)]. \tag{4.26}$$

As discussed in section 2.4 of chapter 2, it is well-known that the noise transfer function is a high pass filter which results in noise shaping characteristic of the circuit. The proposed sigma delta modulator circuit gives a noise transfer function as

$$\frac{v_O(s)}{n(s)} = \frac{s}{s + \frac{g_{m1}}{C}} \tag{4.27}$$

and a granular noise in sigma delta modulator is

$$\overline{n_{qnt}^2(t)} = \left|\frac{s}{s + (g_{m1}/C)}\right|\frac{a^2}{3}\cdot\frac{f_m}{f_s}, \tag{4.28}$$

where a is a step size, f_m is a maximum frequency of information signal and f_s is a sampling's frequency or clock's frequency. By defining that a f_s / f_m is an over sampling rate (OSR), then

$$N = \overline{n_{qnt}^2(t)} = \frac{2\pi f_m}{\sqrt{4\pi^2 f_m^2 + (g_{m1}/C)^2}}\cdot\frac{a^2}{3}\cdot\frac{1}{OSR}. \tag{4.29}$$

If the input signal $f(t)$ is $A\cos(2\pi ft)$ then the mean square value is $\frac{A^2}{2}$, the signal to noise ratio of the circuit thus is

$$\frac{S}{N} = \frac{3\sqrt{4\pi^2 f_m^2 + (g_{m1}/C)^2}}{16\pi^3 f_m} \cdot (OSR)^2. \tag{4.30}$$

4.3 Performance Analysis

4.3.1 Frequency error by slew rate of the OTA

Since output voltage does not change instantaneously during the transition from the upper saturated voltage to the lower saturated voltage as shown in Fig.4.8, the slew rate thus has influence on frequency of the oscillated signals.

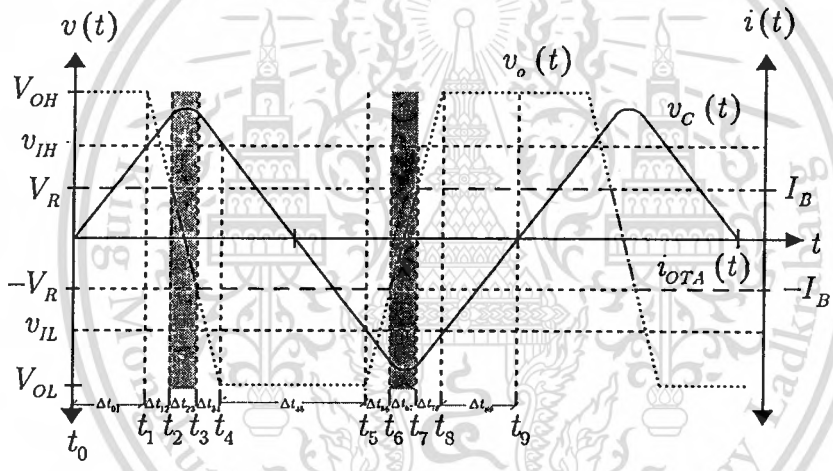


Fig.4.8. Voltage waveforms including slew rate effect

As shown in Fig.4.8, the period of oscillation is consisted of time interval of saturated operation and that of non-saturated operation. Based on the relationship between voltage and current of the capacitor as shown in Eq.(4.3), the slew rate (SR) is expressed as

$$SR = \frac{dv_o(t)}{dt}. \tag{4.31}$$

Therefore, the time interval of saturated operation can be calculated by

$$T_{SAT} = \Delta t_{01} + \Delta t_{12} + \Delta t_{34} + \Delta t_{45} + \Delta t_{56} + \Delta t_{78} + \Delta t_{89}$$
$$= \left(C\frac{v_{IH}}{I_{OTA1}} \right) + \left(\frac{V_R - v_{OH}}{-SR} \right) + \left(\frac{v_{OL} - (-V_R)}{-SR} \right) + \left(-C\frac{v_{IL} - v_{IH}}{I_{OTA1}} \right)$$
$$+ \left(\frac{-V_R - v_{OL}}{SR} \right) + \left(\frac{v_{OH} - V_R}{SR} \right) + \left(-C\frac{v_{IL}}{I_{OTA1}} \right) \quad (4.32)$$

whereas, the time interval of non-saturated operation can be expressed by

$$T_{non-SAT} = \Delta t_{23} + \Delta t_{67} = \left(\frac{-V_R - V_R}{-SR} \right) + \left(\frac{V_R - (-V_R)}{SR} \right). \quad (4.33)$$

The summation of T_{SAT} and $T_{non-SAT}$ thus results in the period of oscillation, which is

$$T = T_{SAT} + T_{non-SAT}$$
$$= \frac{2C(v_{IH} - v_{IL})}{I_{OTA1}} + \frac{2(v_{OH} - v_{OL})}{SR}. \quad (4.34)$$

By substituting v_{IL} and v_{OL} by $-v_{IH}$ and $-v_{OH}$,respectively , it thus yields

$$T = 4C\frac{v_{IH}}{I_{OTA1}} + \frac{4v_{OH}}{SR}. \quad (4.35)$$

Furthermore, it is assumed that the saturated voltage (v_{OH}) is equal to the supply voltage (V_{CC}) and $v_{IH} = I_{OTA3}R_1$, Eq.(4.35) can be rewritten to be

$$T = 4CR_1\frac{I_{OTA3}}{I_{OTA1}} + \frac{4V_{CC}}{SR}. \quad (4.36)$$

Consequently, the oscillation frequency including the slew rate effect then is

$$f = \frac{1}{4CR_1\frac{I_{OTA3}}{I_{OTA1}} + \frac{4V_{CC}}{SR}}. \quad (4.37)$$

From Eq.(4.37), it implies that if an OTA has high slew rate compared to $4v_{OH}$ then the distortion in the oscillation frequency can be neglected.

4.3.2 Noise of the OTA

Another limitation of CMOS component that should be mentioned is noise effect. In CMOS circuit, noise can be modeled by a current source that represents two sources of noise, called thermal noise and flicker noise [18]. Based upon the OTA which used in this thesis as illustrated in Fig.3.1, this noise can be illustrated as the short-circuit mean-square noise current which is a function of all the noise source (e_n) in a series with the gate as given by

$$\overline{i_{total}^2} = g_{m1}^2\overline{e_{n1}^2} + g_{m2}^2\overline{e_{n2}^2} + g_{m6}^2\left(\overline{e_{n4}^2} + \overline{e_{n6}^2}\right) + g_{m8}^2\left(\overline{e_{n3}^2} + \overline{e_{n8}^2}\right) + g_{m7}^2\left(\overline{e_{n7}^2} + \overline{e_{n9}^2}\right). \tag{4.38}$$

Eq.(4.38) can be written to be

$$\overline{i_{total}^2} = 4g_{mP}^2\overline{e_{nP}^2} + 2g_{m1}^2\overline{e_{nN}^2} + 2g_{m7}^2\overline{e_{nN}^2} \tag{4.39}$$

where the following parameters are assumed $g_{m6}^2 = g_{m8}^2 = g_{mP}^2$, $g_{m1}^2 = g_{m2}^2$, $\overline{e_{n4}^2} = \overline{e_{n6}^2} = \overline{e_{n3}^2} = \overline{e_{n8}^2} = \overline{e_{nP}^2}$ and $\overline{e_{n1}^2} = \overline{e_{n2}^2} = \overline{e_{n7}^2} = \overline{e_{n9}^2} = \overline{e_{nN}^2}$.

By dividing both sides of Eq.(4.39) by g_{m1}^2, it results in the equivalent input mean-square voltage noise as

$$\overline{e_{eq}^2} = 4\left(\frac{g_{mP}^2}{g_{m1}^2}\right)\overline{e_{nP}^2} + 2\left(1 + \left(\frac{g_{m7}^2}{g_{m1}^2}\right)\right)\overline{e_{nN}^2}. \tag{4.40}$$

For thermal noise, $\overline{e_{nP}^2} = \overline{e_{nN}^2} = \overline{e_{n1}^2}$ [13], then

$$\overline{e_{eq}^2} = \left[4\left(\frac{g_{mP}^2}{g_{m1}^2}\right) + 2\left(1 + \left(\frac{g_{m7}^2}{g_{m1}^2}\right)\right)\right]\left(\frac{8KT}{3g_{m1}}\right) \tag{4.41}$$

where K is Boltzmann's constant and T is temperature in Kelvin.

But for flicker noise, [18]

$$\overline{e_{n,N}^2} = \frac{B_N}{fWL} \text{ and } \overline{e_{nP}^2} = \frac{B_P}{fWL} \tag{4.42}$$

where $B_N = \frac{KF}{2C_{OX}K_N}$, $B_P = \frac{KF}{2C_{OX}K_P}$,KF is a flicker noise coefficient ,W is the width of MOS, L is the length of MOS and f is a frequency.

Finally, the total equivalent input mean-square voltage noise then is

$$\overline{e_{eq}^2} = \sqrt{\left\{\left[4\left(\frac{g_{mP}^2}{g_{m1}^2}\right)+2\left(1+\left(\frac{g_{m7}^2}{g_{m1}^2}\right)\right)\right]\cdot\frac{8KT}{3g_{m1}}\right\}^2 + \left\{4\left(\frac{g_{mP}^2}{g_{m1}^2}\right)\frac{B_P}{fW_PL_P}+2\frac{B_N}{fW_1L_1}+2\left(\frac{g_{m7}^2}{g_{m1}^2}\right)\frac{B_N}{fW_7L_7}\right\}^2}. \tag{4.43}$$

By considering Eq.(4.43), to minimize the thermal noise, it is obvious that the transconductance, g_{m1}, must be large which can be achieved by large dc current or large aspect ratio of $M_{1,2}$. For the flicker noise, it can be minimized through the circuit topology and aspect ratio of all MOS transistors.

CHAPTER 5

Simulation results

In this chapter, a novel versatile modulator circuit which is implemented by a balanced OTA is shown and its simulation results are also presented. The simulation results are composed of the characteristic of amplitude and frequency control, the frequency response of the circuit and the temperature stability of the output frequency. Then, amplitude and frequency modulation's results are illustrated in both time domain and frequency domain. In addition, the waveform and the spectrum of delta modulation and sigma delta modulation are given. Moreover, brief review of analog layout design is introduced, and then the layout of the proposed circuit is also demonstrated.

5.1 A novel versatile modulator circuit

The proposed circuit is now implemented by using CMOS OTAs. This circuit is composed of 12 PMOSs, 18 NMOSs, two resistors and one capacitor as shown in Fig.5.1. It is noted that the input's feeding points for amplitude modulation, frequency modulation, sigma delta modulation and delta modulation are $i_{in-AM}(t)$, $i_{in-FM}(t)$, $v_{in-SDM}(t)$ and $v_{in-DM}(t)$, respectively, whereas the modulated output signal is measured at the v_{out} node.

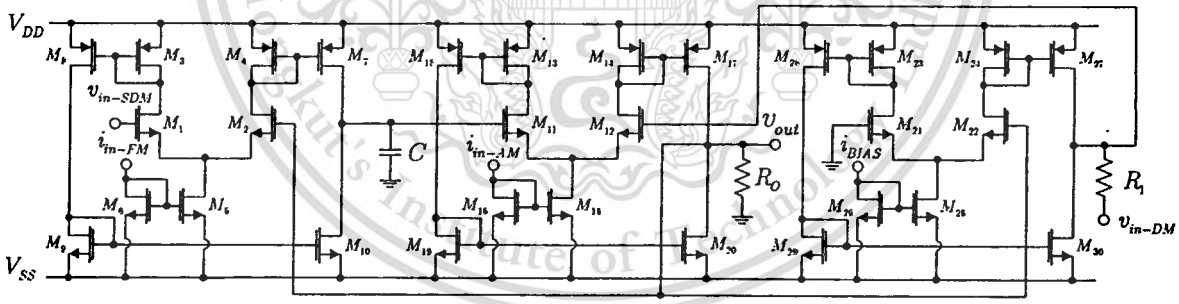


Fig.5.1. Circuit description of the proposed scheme

5.2 Design a CMOS balanced OTA

The complete CMOS OTA circuit in Fig.5.1 is designed and post-layout simulated using Cadence with level-49 process parameters of AMS 0.35 micron as shown in Table I.

Table I. Process parameters of AMS 0.35 micron

Parameter Description	Typical Parameter Value		
	N-Channel	P-Channel	Unit
Threshold voltage (V_T)	0.5	-0.65	V
Transconductance parameter (K)	170	58	$\mu A/V^2$

SPECIFICATIONS

Based on the design procedures described in Section 3.3., the OTA is designed with the following requirements:

1. Gain: 80 dB
2. Gain bandwidth product: 100 MHz
3. Slew rate: 100V/μs
4. Load Capacitance: 2 pF
5. $V_{DD} = -V_{SS} = 1.65V$
6. Power consumption < 2 mW

With the specification, the aspect ratio $(W/L)_i$ of the ith MOS obtained from the designed procedures is summarized in Table II.

Table II. Summarized the aspect ratio $(W/L)_i$ of the ith MOS

MOS	(W/L)	MOS	(W/L)	MOS	(W/L)
M_1	23μ/ 0.35μ	M_2	23μ/ 0.35μ	M_3	53.5μ/ 0.35μ
M_4	53.5μ/ 0.35μ	M_5	3.6μ/ 0.35μ	M_6	3.6μ/ 0.35μ
M_7	53.5μ/ 0.35μ	M_8	53.5μ/ 0.35μ	M_9	3.6μ/ 0.35μ
M_{10}	3.6μ/ 0.35μ				

It is found from the design that the power dissipation is 1.32 mW and the gain is 8000, then the specification of the desired OTA is satisfied. This designed OTA is employed to construct the proposed versatile modulator circuit (as depicted in Fig.5.1). The circuit is simulated with ±1.65 V and R_1,R_2 are 2 kΩ and the capacitor is 0.01 μF.

5.3 Simulation results

5.3.1 Simulation results of pulse generator circuit

Firstly, the simulated result of pulse generator (as shown in Fig.5.1) is examined to demonstrate the ability of electronically amplitude and frequency control. It can be accomplished by putting the feeding point for $v_{in-SDM}(t)$ and $v_{in-DM}(t)$ to the circuit's ground whereas $v_{in-FM}(t)$ and $v_{in-AM}(t)$ to are set to be DC voltage signal. The obtained results are given in Fig.5.2 where y-axis on left-handed side and right-handed side are respectively for frequency and amplitude. For frequency adjustment, I_{B2} = 0.1 mA, I_{B3} = 0.2 mA are employed whereas I_{B1} is varied as shown on the x-axis (bottom). For amplitude adjustment, I_{B2} is varied as shown on the x-axis (top) whereas I_{B1} = 0.2 mA, I_{B3} = 0.2 mA are set.

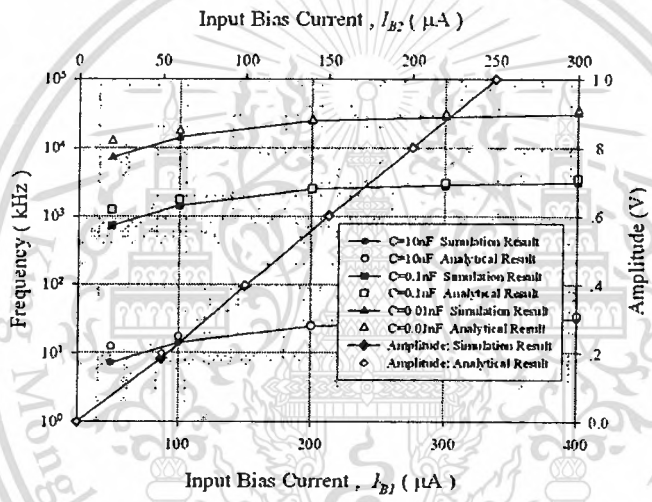


Fig.5.2. Electronically control of frequency and amplitude of the proposed circuit

To illustrate the frequency response of the proposed pulse generator, it is simulated by setting the current I_{BIAS} of all MOS transistors to be 500μA and the capacitor C is varied from 0.1 nF to 0.1 pF. The magnitude of frequency response is depicted in Fig.5.3. It is seen that the obtained cut-off frequency is approximately 200 MHz.

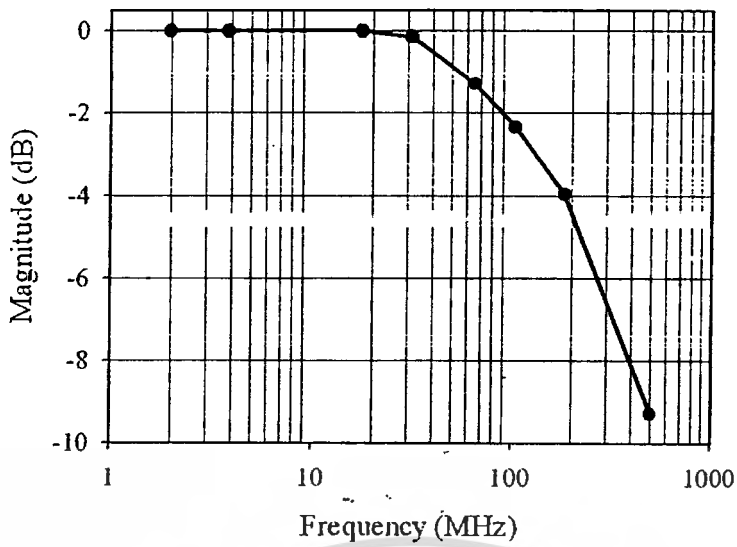


Fig.5.3. Frequency response of the proposed pulse generator

In general, the frequency stability of the pulse generator is primarily determined by the temperature coefficient of oscillation frequency which is defined as $\frac{1}{f_0}\frac{\Delta f_0}{\Delta T}\times 10^6$ (ppm/° C). Fig.5.4 shows the temperature stability of the output frequency for low frequency at 100Hz and high frequency at 100 MHz versus the temperature range from -45 to 85 ° C. It is found that their temperature coefficients of -1025 ppm/ ° C and -692 ppm/ ° C are obtained at frequency 150 Hz and at frequency 100 MHz, respectively.

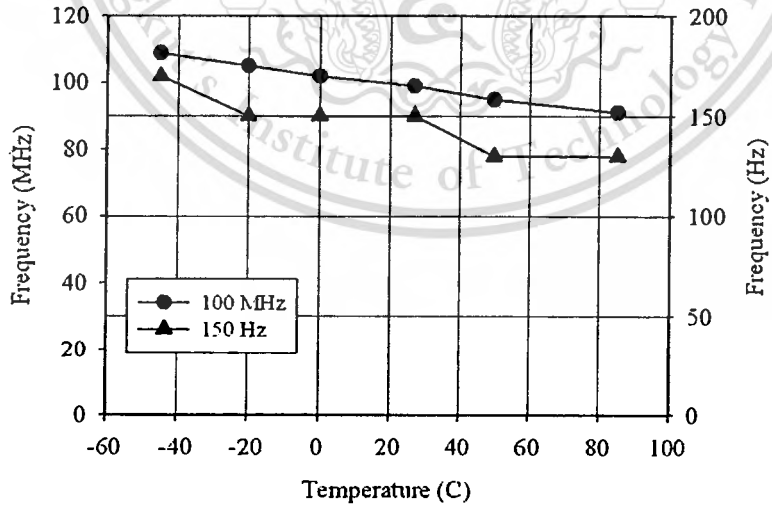


Fig.5.4. Deviation of frequency versus temperature

5.3.2 Simulation results of amplitude modulator circuit

In order to demonstrate the application from the ability of electrically amplitude control, the circuit is therefore applied for amplitude modulator. When input signal is fed to the bias input node of the OTA2, namely, $I_{B2}(t)=I_{m(t)}$. The magnitude of output signal is directly proportion to bias current of the OTA2. Let I_{B1} and I_{B3} be fixed at 0.5 mA which provide inherent 25 kHz carrier signal. Firstly, the simulated result of electronically amplitude control is shown in Fig.5.5.

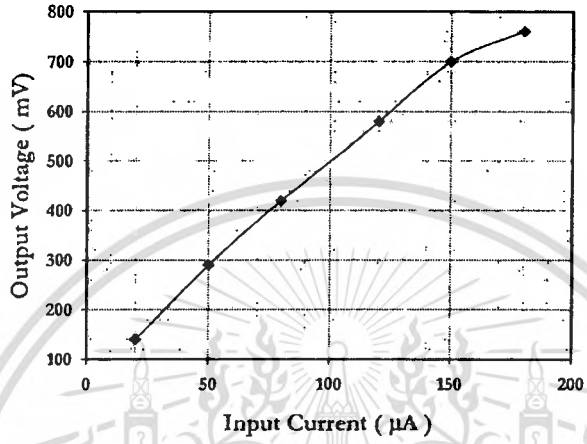


Fig.5.5. The simulated result of electronically amplitude control

Later, the amplitude modulation outputs are given in Fig 5.6 – Fig 5.14.

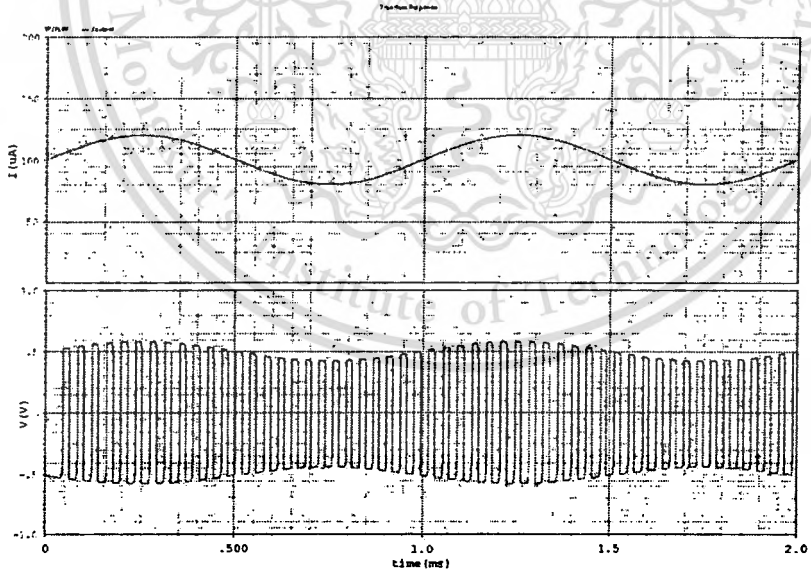


Fig.5.6. Amplitude modulation result where the sinusoidal modulating signal with 1 kHz frequency, 20μA amplitude and 100μA offset is shown in the upper trace and the lower trace is the square wave AM signal whose modulation index is 16%.

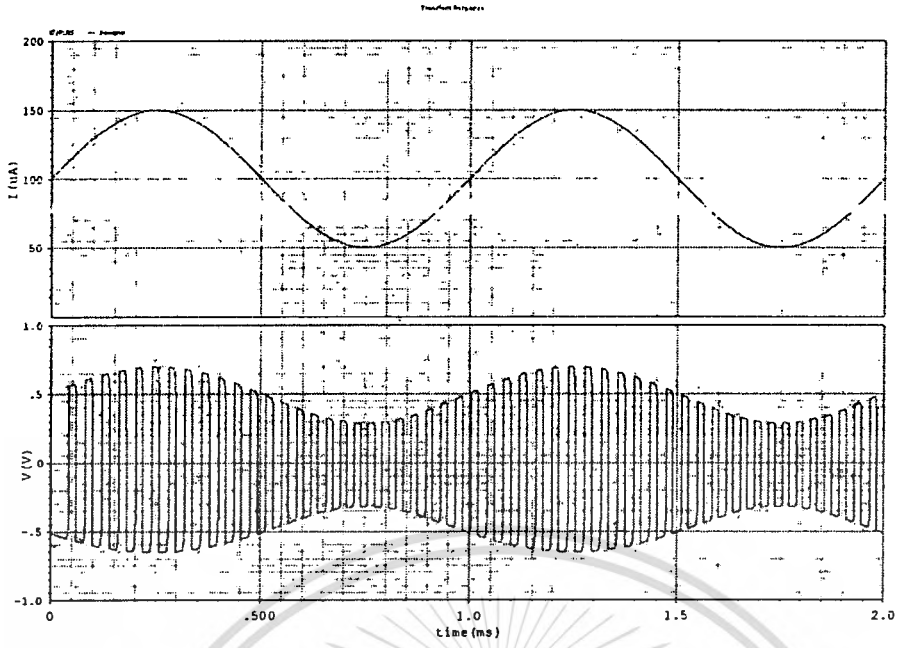


Fig.5.7. Amplitude modulation result where the sinusoidal modulating signal with 1 kHz frequency, 50μA amplitude and 100μA offset is shown in the upper trace and the lower trace is the square wave AM signal whose modulation index is 40%.

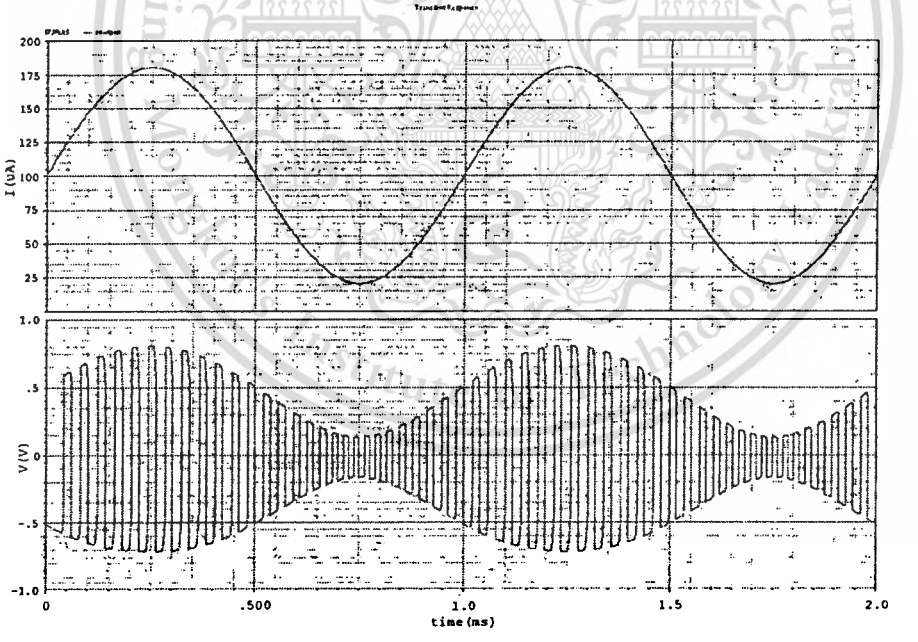


Fig.5.8. Amplitude modulation result where the sinusoidal modulating signal with 1 kHz frequency, 80μA amplitude and 100μA offset is shown in the upper trace and the lower trace is the square wave AM signal whose modulation index is 70%.

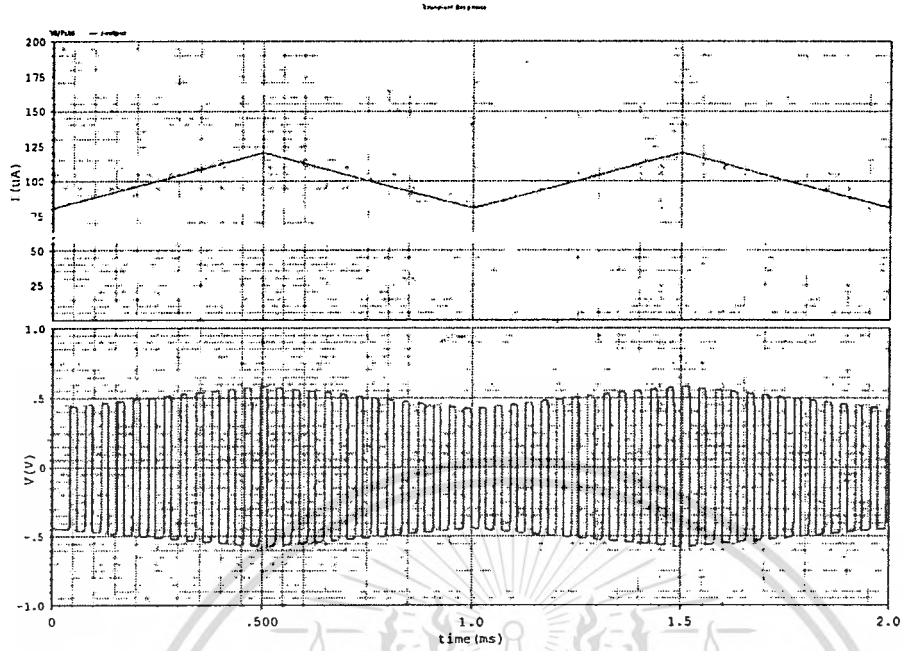


Fig.5.9. Amplitude modulation result where the triangular wave modulating signal with 1 kHz frequency, 20μA amplitude and 100μA offset is shown in the upper trace and the lower trace is the square wave AM signal whose modulation index is 16%.

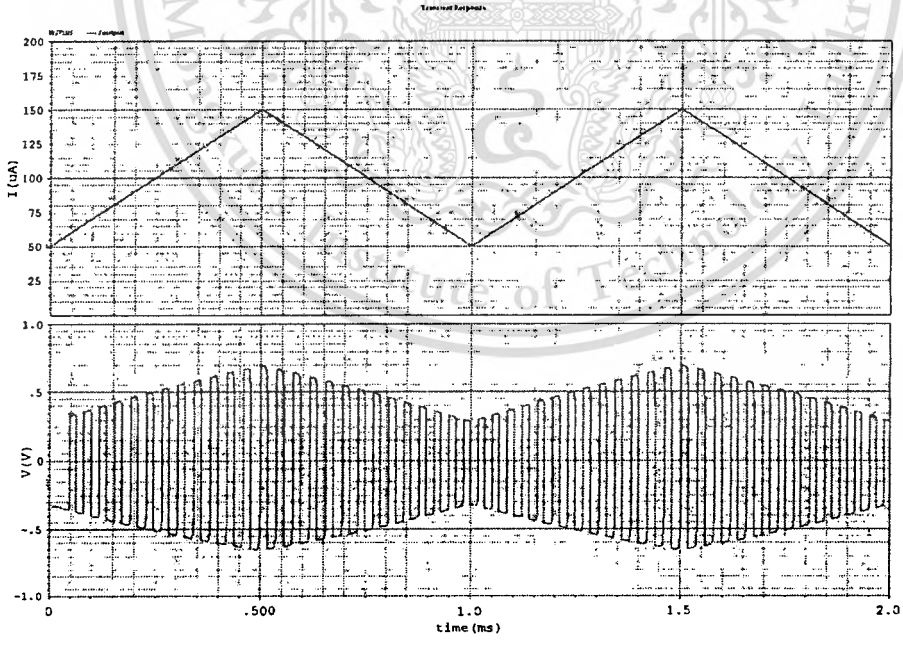


Fig.5.10. Amplitude modulation result where the triangular wave modulating signal with 1 kHz frequency, 50μA amplitude and 100μA offset is shown in the upper trace and the lower trace is the square wave AM signal whose modulation index is 40%.

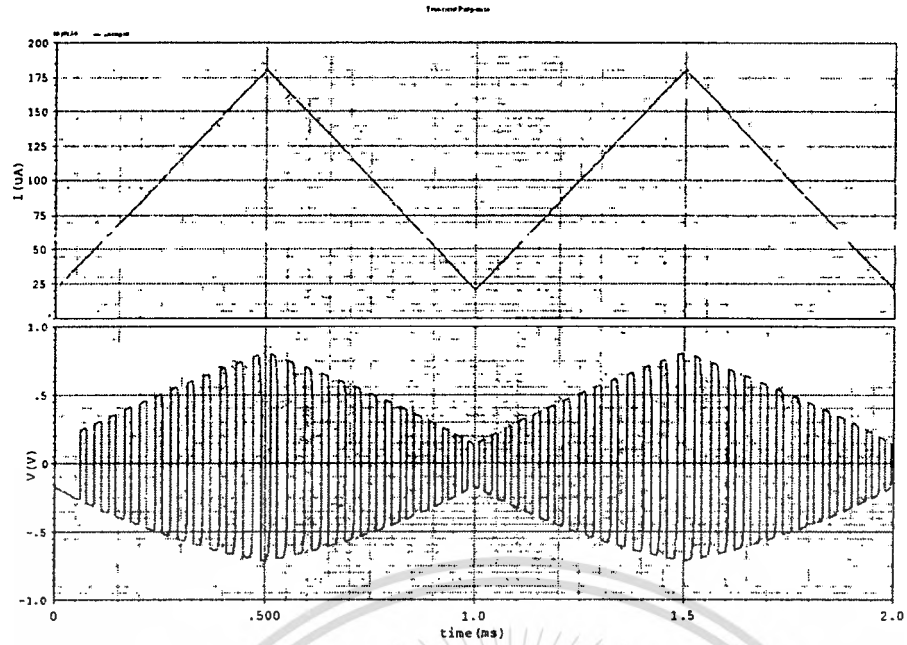


Fig.5.11. Amplitude modulation result where the triangular wave modulating signal with 1 kHz frequency, 80μA amplitude and 100μA offset is shown in the upper trace and the lower trace is the square wave AM signal whose modulation index is 70%.

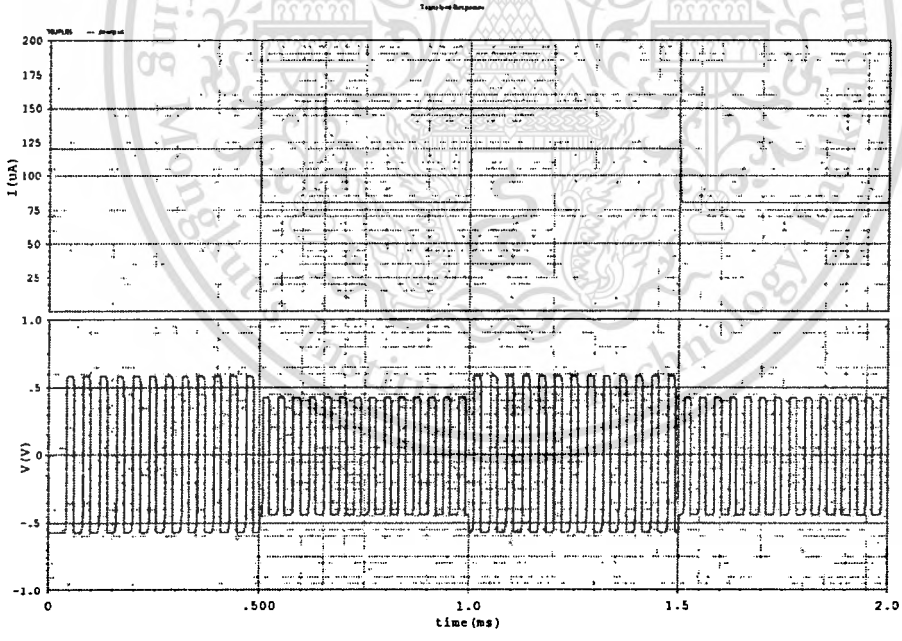


Fig.5.12. Amplitude modulation result where the square wave modulating signal with 1 kHz frequency, 20μA amplitude and 100μA offset is shown in the upper trace and the lower trace is the square wave AM signal whose modulation index is 16%.

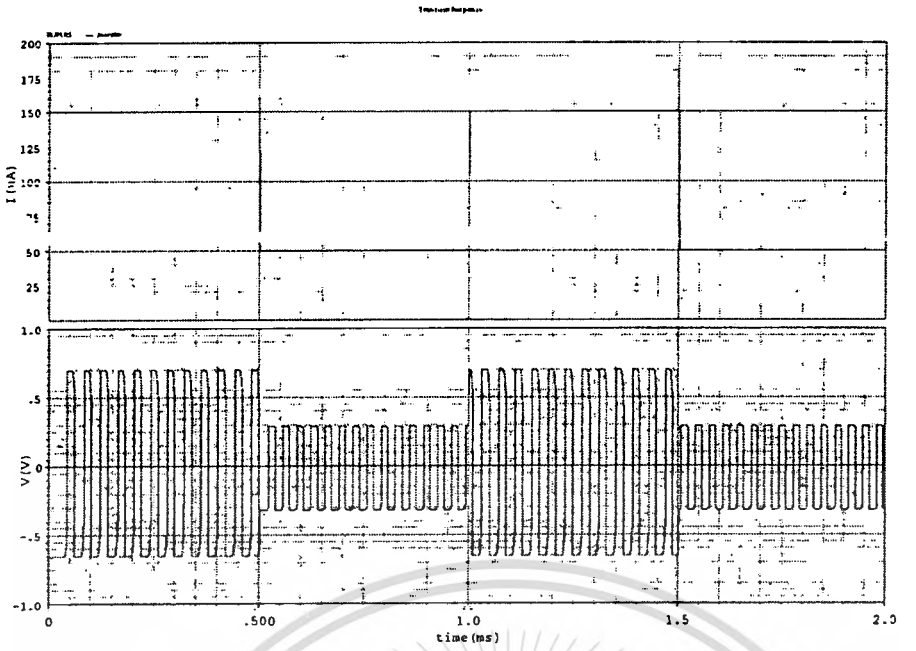


Fig.5.13. Amplitude modulation result where the square wave modulating signal with 1 kHz frequency, 50μA amplitude and 100μA offset is shown in the upper trace and the lower trace is the square wave AM signal whose modulation index is 40%.

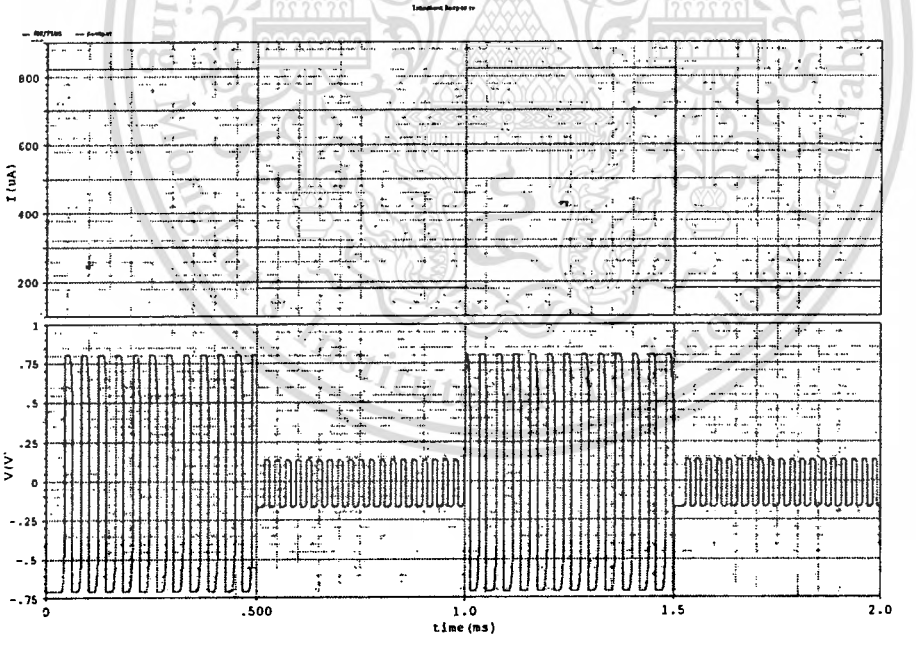


Fig.5.14. Amplitude modulation result where the square wave modulating signal with 1 kHz frequency, 80μA amplitude and 100μA offset is shown in the upper trace and the lower trace is the square wave AM signal whose modulation index is 70%.

5.3.3 Simulation results of frequency modulator circuit

Later, with electrical frequency-control ability of the circuit, the circuit can then be functioned as a frequency modulator. When input signal is fed to the bias input node of the OTA1, namely, $I_{B1}(t) = I_{m(t)}$. The frequency of output signal is thus directly proportional to bias current of the OTA1. In this case, I_{B2} = 0.1 mA, I_{B3} = 0.5 mA are fixed, for this situation, the circuit produces the inherent 25 kHz carrier signal. The simulated result of electronically frequency control is shown in Fig.5.15. The slope of graph is defined as the modulation sensitivity $\left(k_f\right)$, where in this case, the modulation sensitivity $\left(k_f\right)$ is 5.23kHz/100μA.

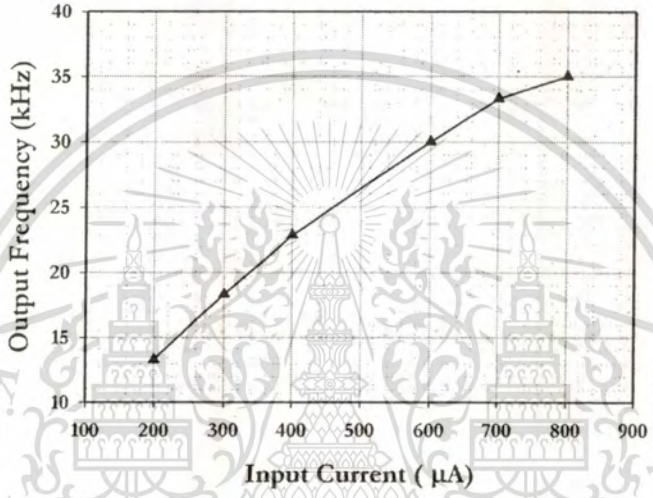


Fig.5.15. The simulated result of electronically frequency control

Later, the frequency modulation outputs are displayed in Fig 5.16 – Fig 5.27.

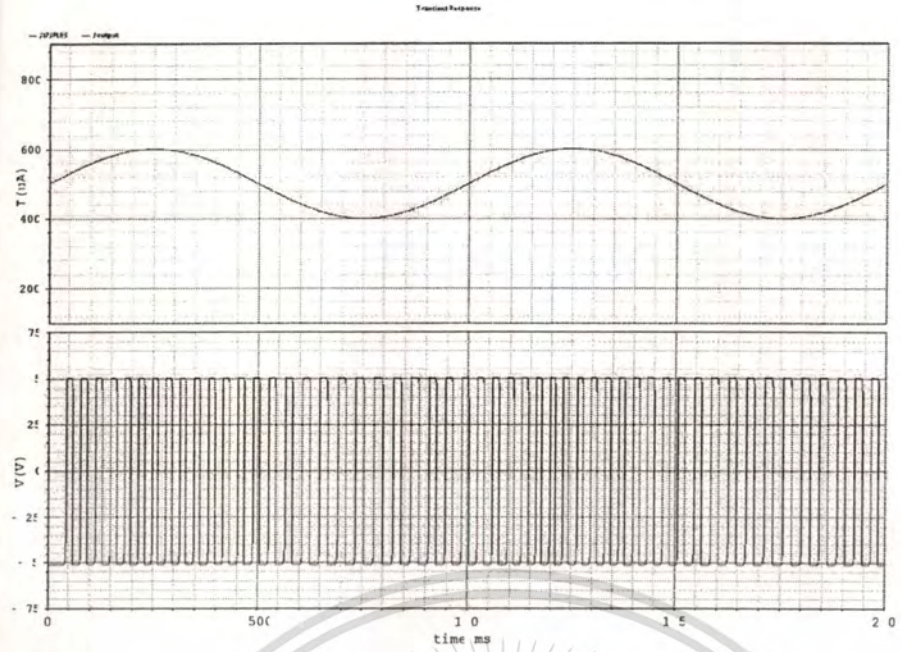


Fig.5.16. Frequency modulation result where the sinusoidal modulating signal with 1 kHz frequency, 100μA amplitude and 500μA offset is shown in the upper trace and the lower trace is the square wave FM signal whose modulation index is 5.23.

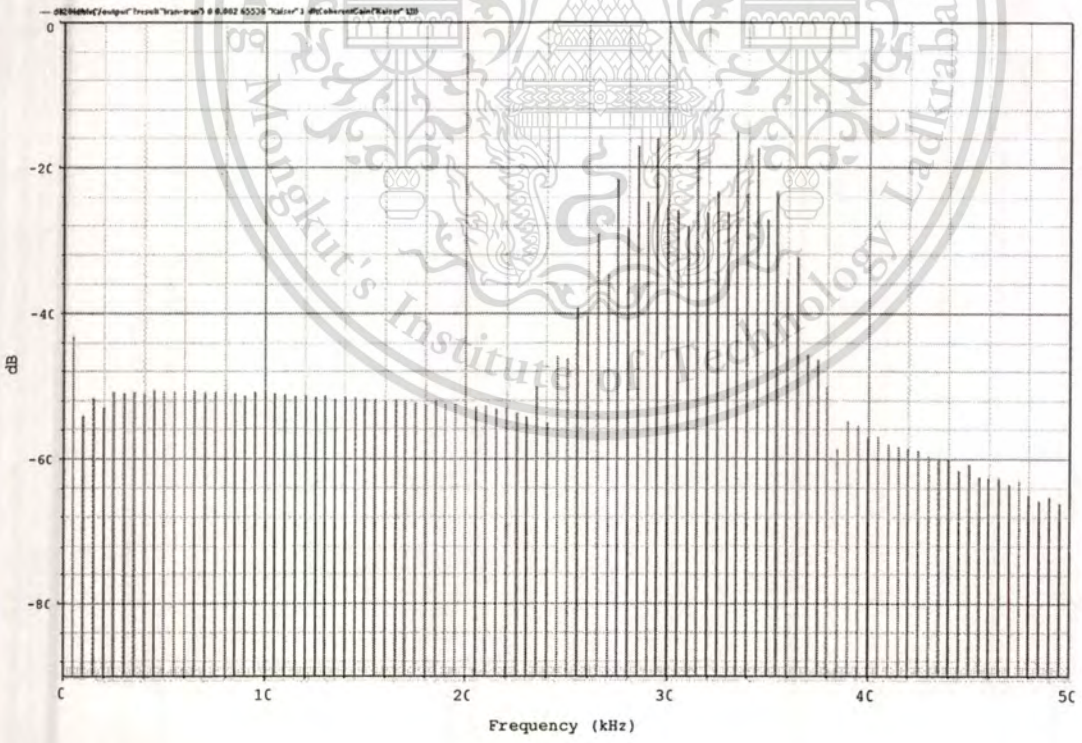


Fig.5.17. Spectrums of the FM output shown in Fig 5.16.

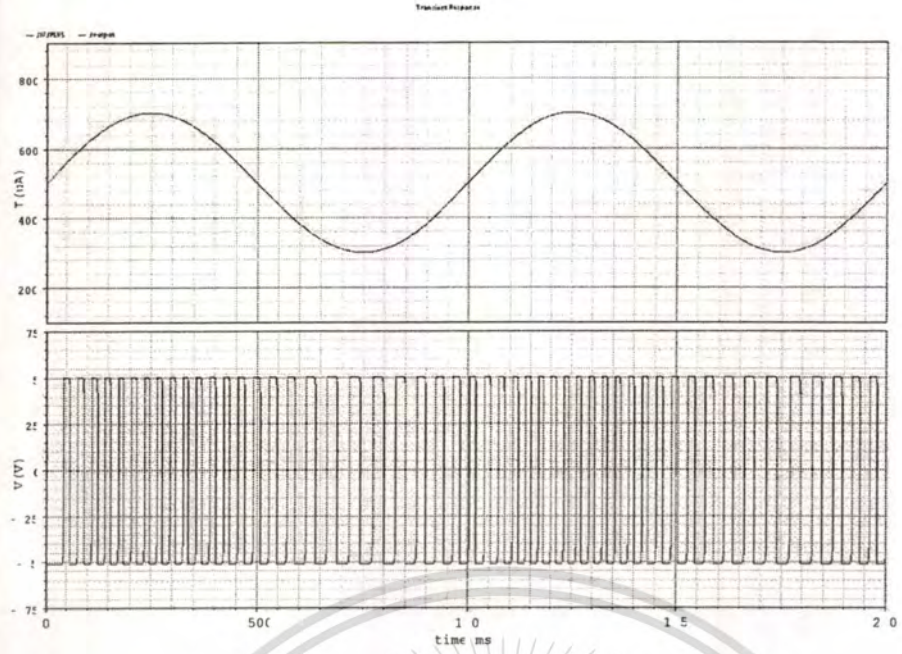


Fig.5.18. Frequency modulation result where the sinusoidal modulating signal with 1 kHz frequency, 200μA amplitude and 500μA offset is shown in the upper trace and the lower trace is the square wave FM signal whose modulation index is 10.46.

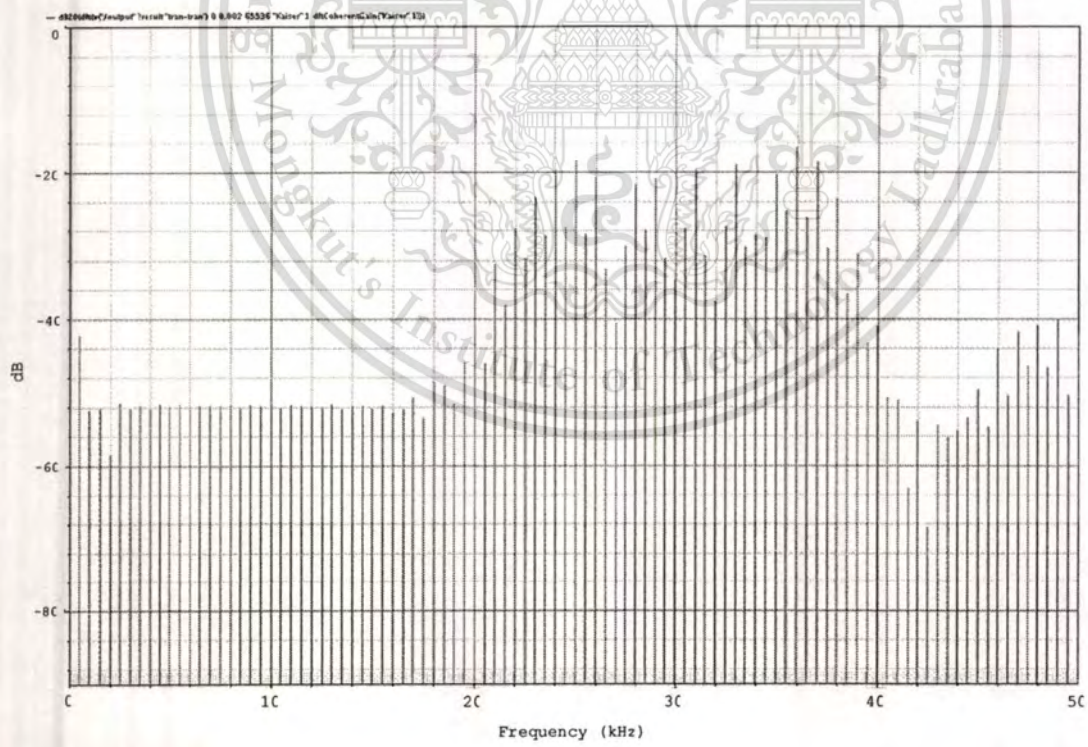


Fig.5.19. Spectrums of the FM output shown in Fig 5.18.

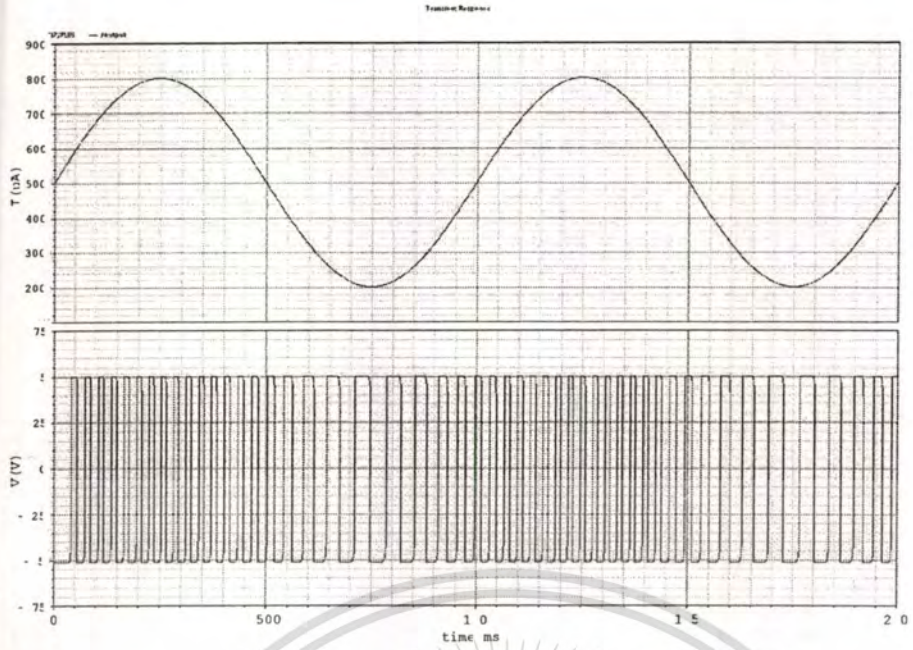


Fig.5.20. Frequency modulation result where the sinusoidal modulating signal with 1 kHz frequency, 300μA amplitude and 500μA offset is shown in the upper trace and the lower trace is the square wave FM signal whose modulation index is 15.69.

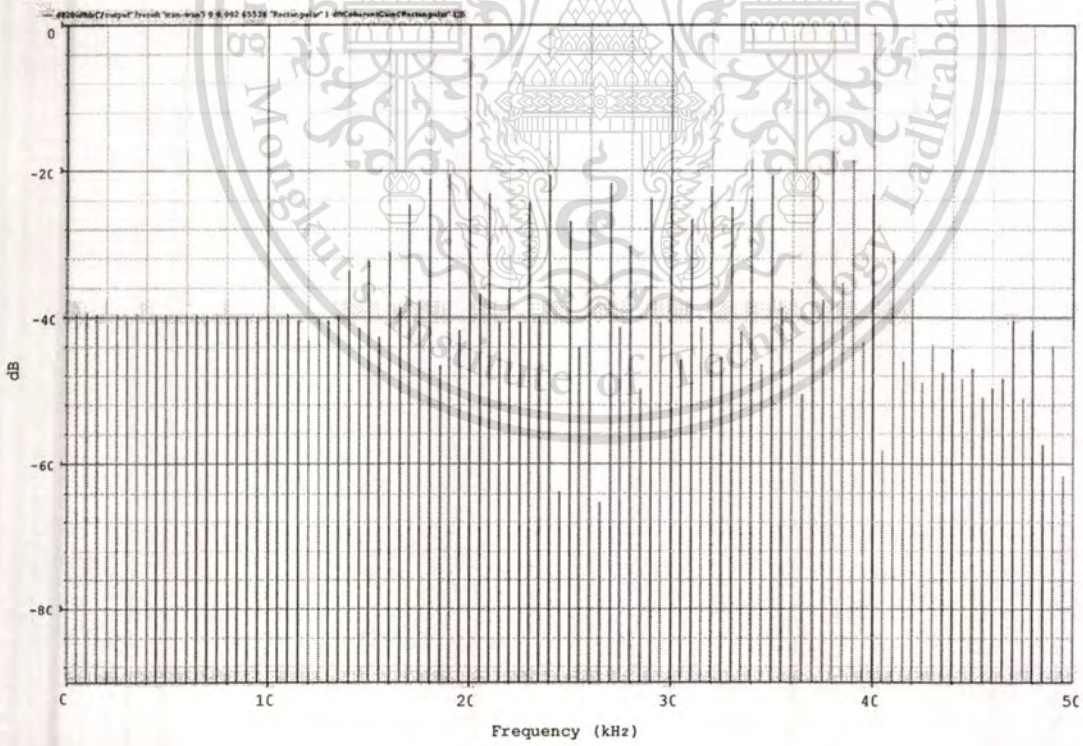


Fig.5.21. Spectrums of the FM output shown in Fig 5.20.

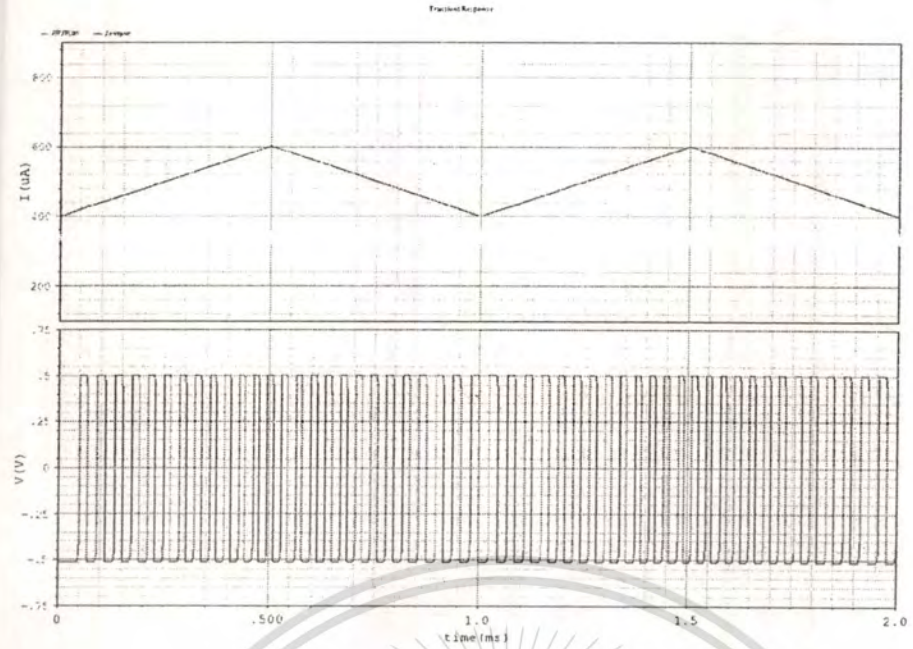


Fig.5.22. Frequency modulation result where the triangular wave modulating signal with 1 kHz frequency, 100μA amplitude and 500μA offset is shown in the upper trace and the lower trace is the square wave FM signal.

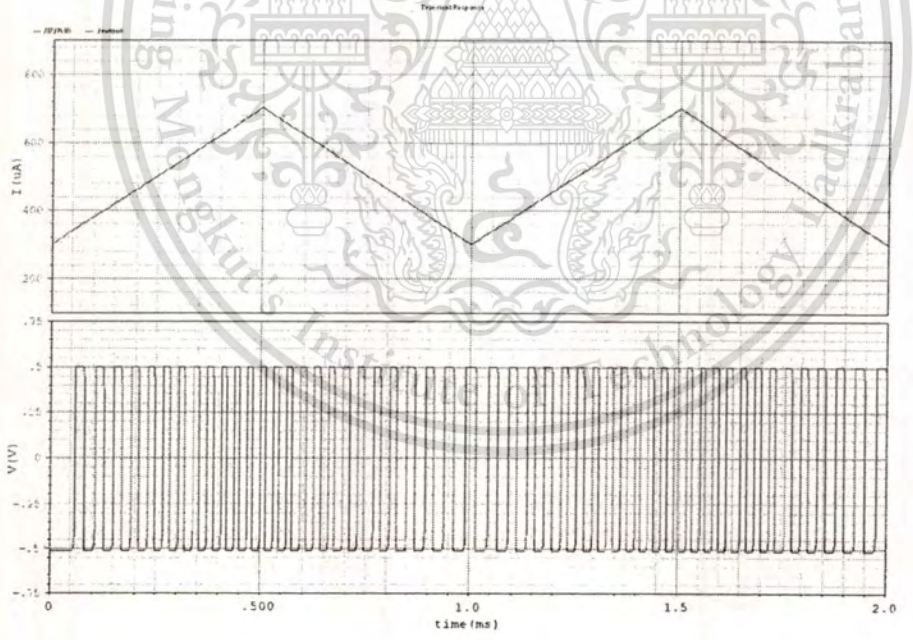


Fig.5.23. Frequency modulation result where the triangular wave modulating signal with 1 kHz frequency, 200μA amplitude and 500μA offset is shown in the upper trace and the lower trace is the square wave FM signal.

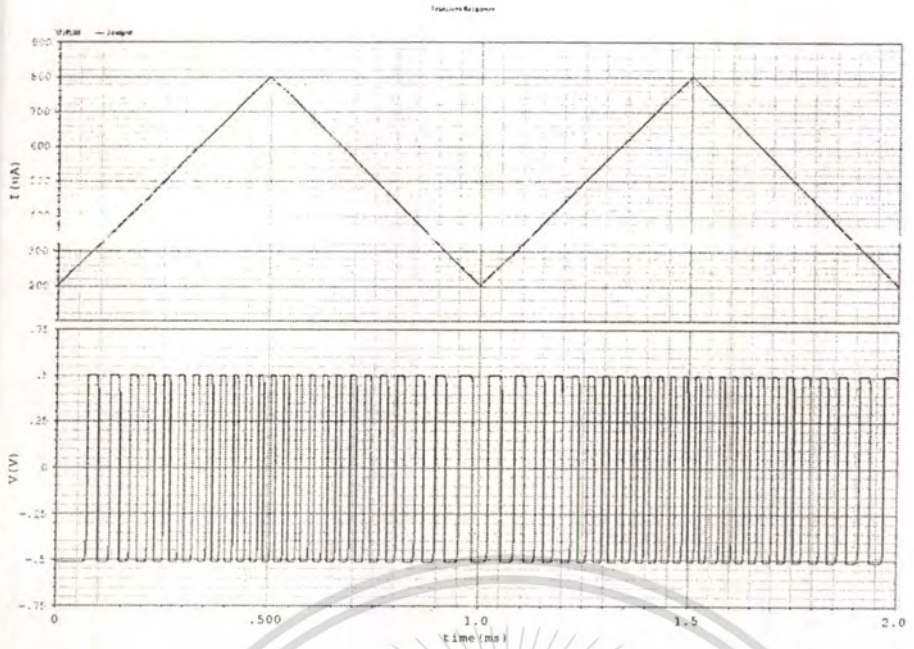


Fig.5.24. Frequency modulation result where the triangular wave modulating signal with 1 kHz frequency, 300μA amplitude and 500μA offset is shown in the upper trace and the lower trace is the square wave FM signal.

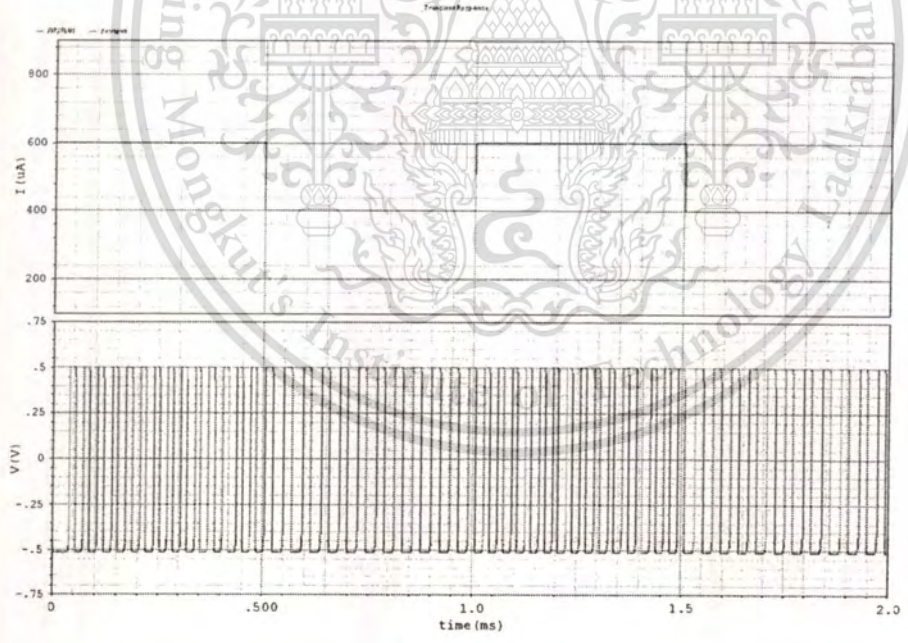


Fig.5.25. Frequency modulation result where the square wave modulating signal with 1 kHz frequency, 100μA amplitude and 500μA offset is shown in the upper trace and the lower trace is the square wave FM signal.

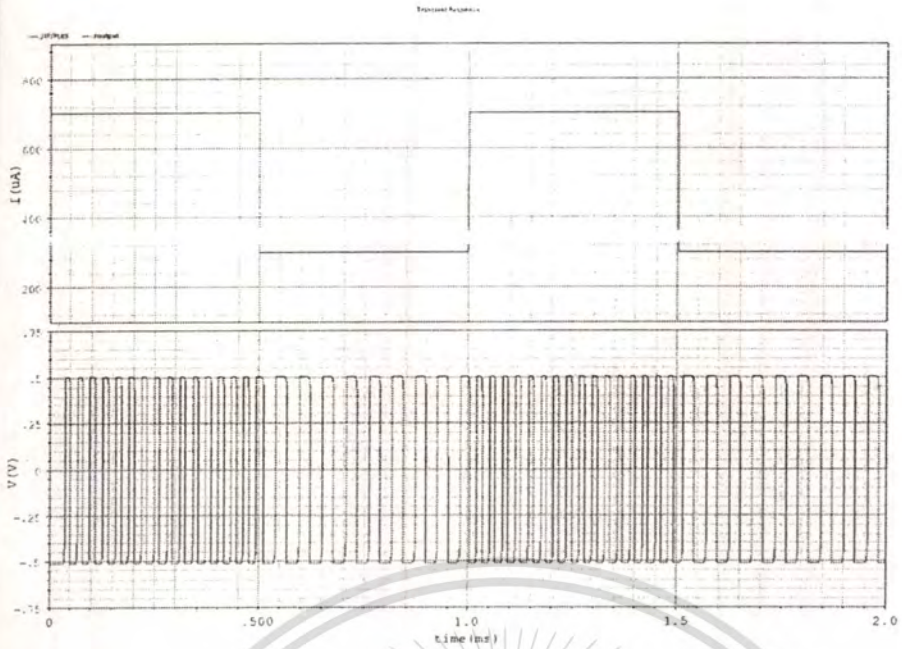


Fig.5.26. Frequency modulation result where the square wave modulating signal with 1 kHz frequency, 200μA amplitude and 500μA offset is shown in the upper trace and the lower trace is the square wave FM signal.

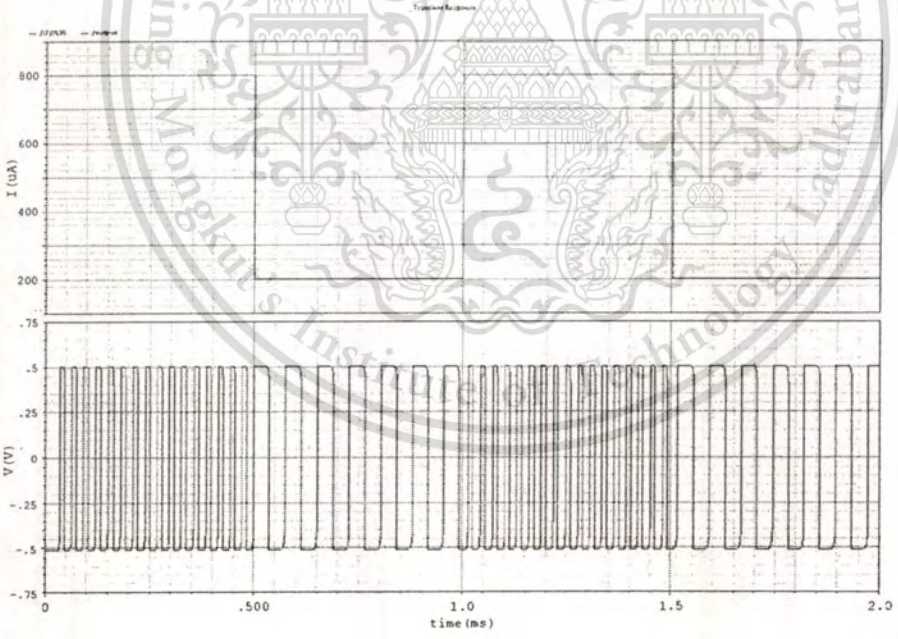


Fig.5.27. Frequency modulation result where the square wave modulating signal with 1 kHz frequency, 300μA amplitude and 500μA offset is shown in the upper trace and the lower trace is the square wave FM signal.

5.3.4 Simulation results of sigma delta modulator circuit

From the circuit depiced in Fig.9 of section 4.2.4, I_{B1} = 0.5 mA, I_{B2} = 0.1 mA and I_{B3} = 0.35 mA are set, which provides an inherent 36 kHz clock carrier signal. The following results are the sigma delta modulation signal and their magnitude spectrums. It is noticed that the information signal's spectrum is appeared at low frequency, the low pass filter then can be used to recover the information signal.

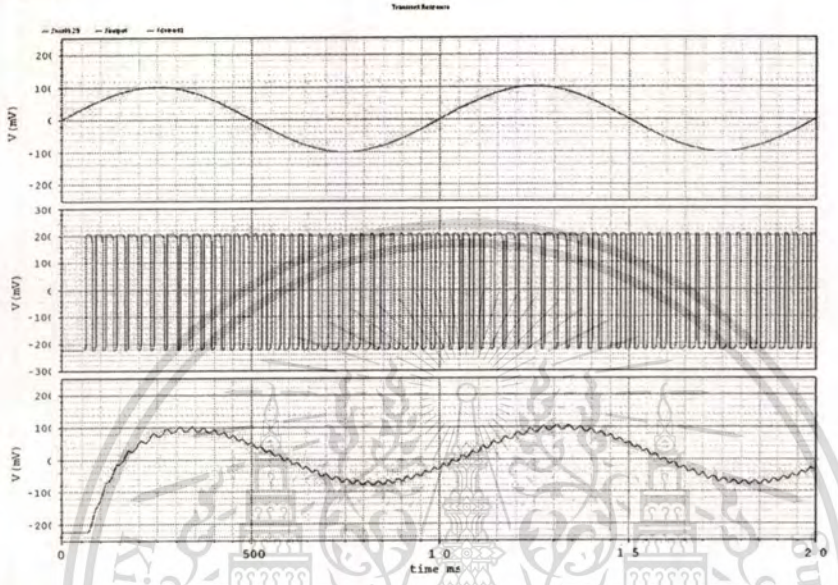


Fig.5.28. Simulation result for sigma delta modulation where the upper trace is 1 kHz, 0.2 V_{PP} sinusoidal modulating signal, the middle trace is the sigma delta modulation output and the lower trace is low pass filter output.

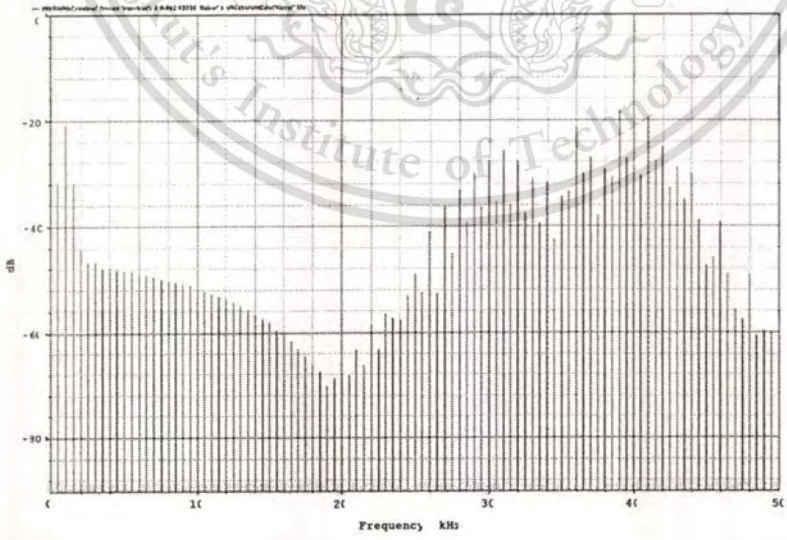


Fig.5.29. The spectrums of the sigma delta modulation output shown in Fig 5.28.

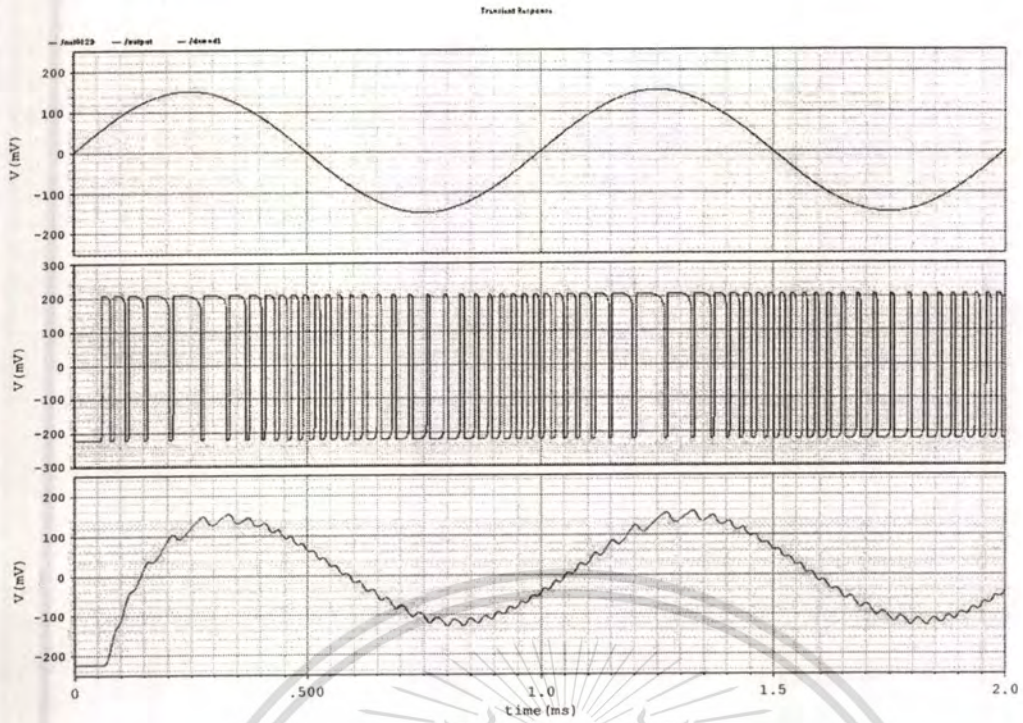


Fig.5.30. Simulation result for sigma delta modulation where the upper trace is 1 kHz, 0.3 V_{PP} sinusoidal modulating signal, the middle trace is the sigma delta modulation output and the lower trace is low pass filter output.

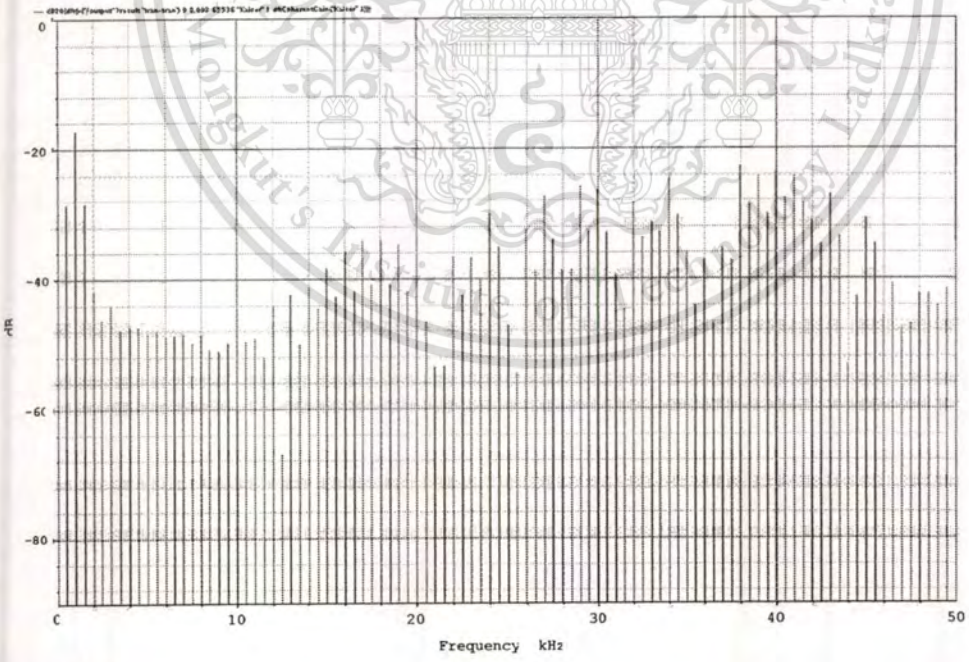


Fig.5.31. The spectrums of the sigma delta modulation output shown in Fig 5.30.

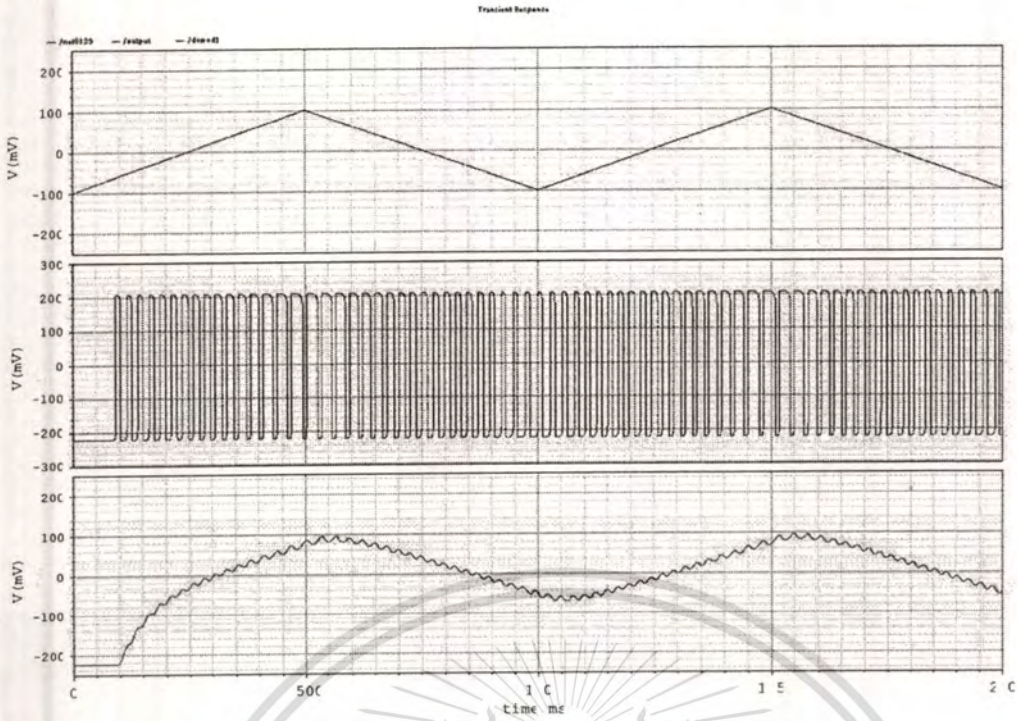


Fig.5.32. Simulation result for sigma delta modulation where the upper trace is 1 kHz, 0.2 V_{PP} triangular wave modulating signal, the middle trace is the sigma delta modulation output and the lower trace is low pass filter output.

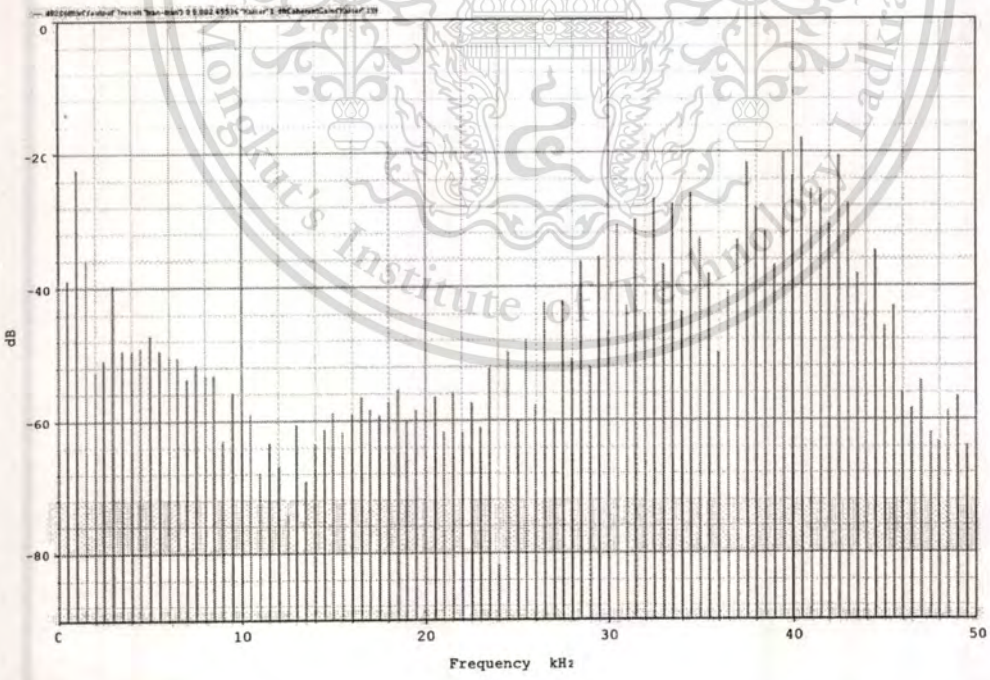


Fig.5.33. The spectrums of the sigma delta modulation output shown in Fig 5.32.

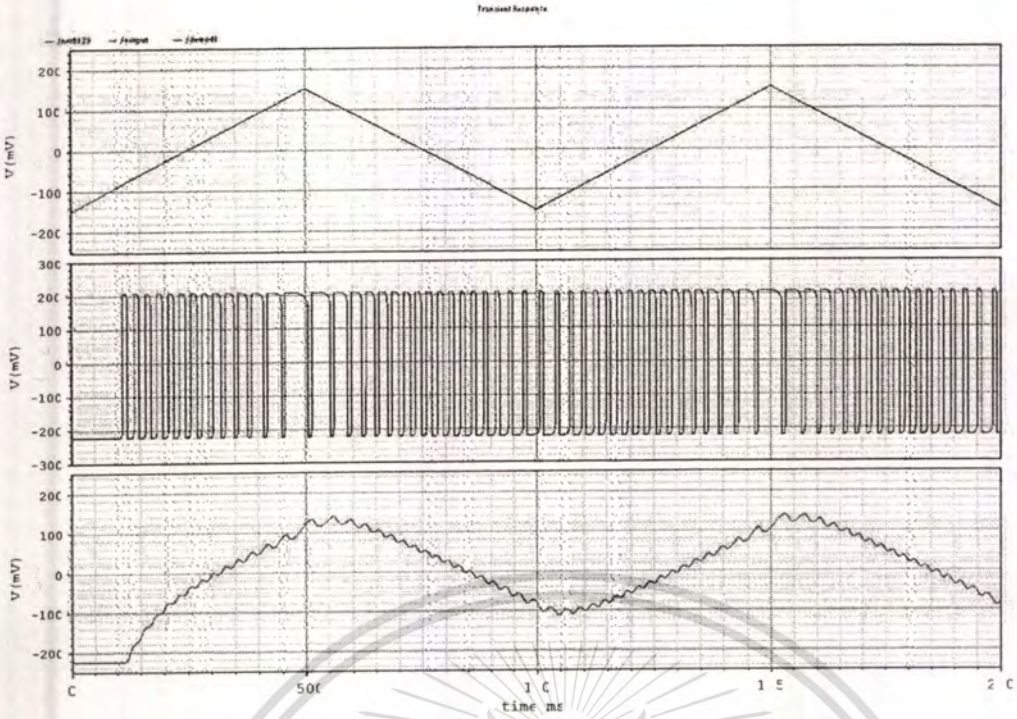


Fig.5.34. Simulation result for sigma delta modulation where the upper trace is 1 kHz, 0.3 V_{PP} triangular wave modulating signal, the middle trace is the sigma delta modulation output and the lower trace is low pass filter output.

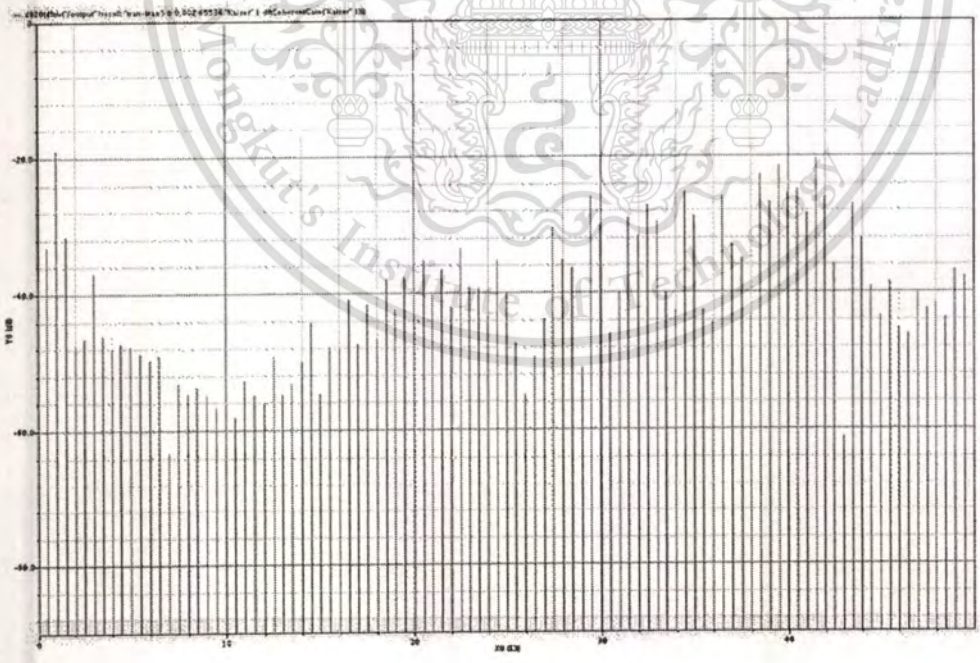


Fig.5.35. The spectrums of the sigma delta modulation output shown in Fig 5.34.

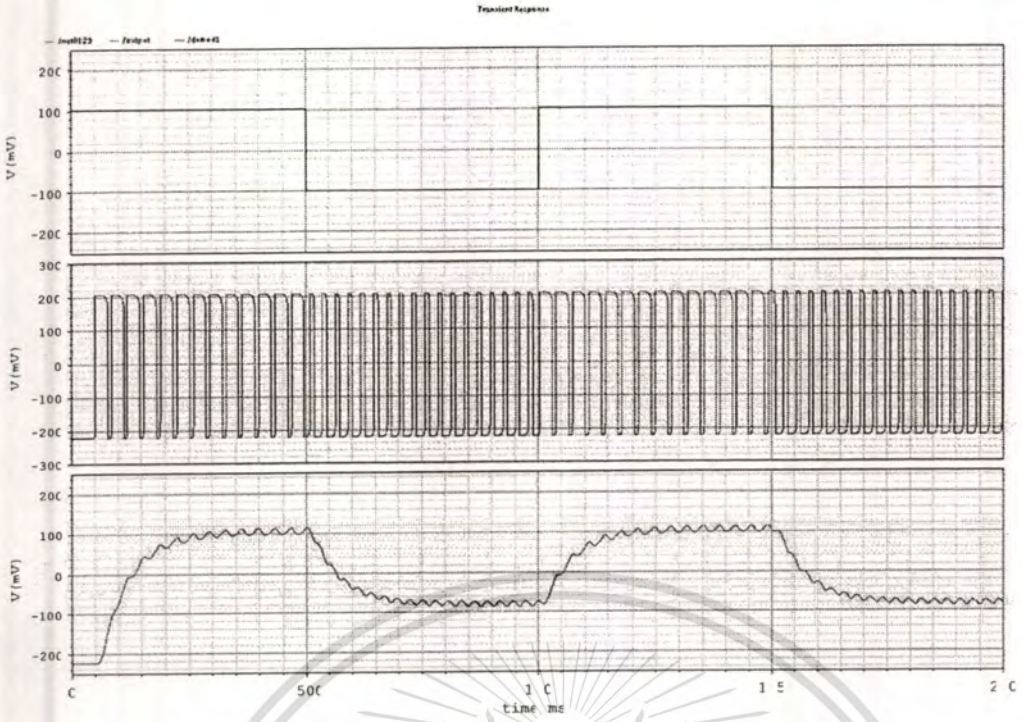


Fig.5.36. Simulation result for sigma delta modulation where the upper trace is 1 kHz, 0.2 V_{PP} square wave modulating signal, the middle trace is the sigma delta modulation output and the lower trace is low pass filter output.

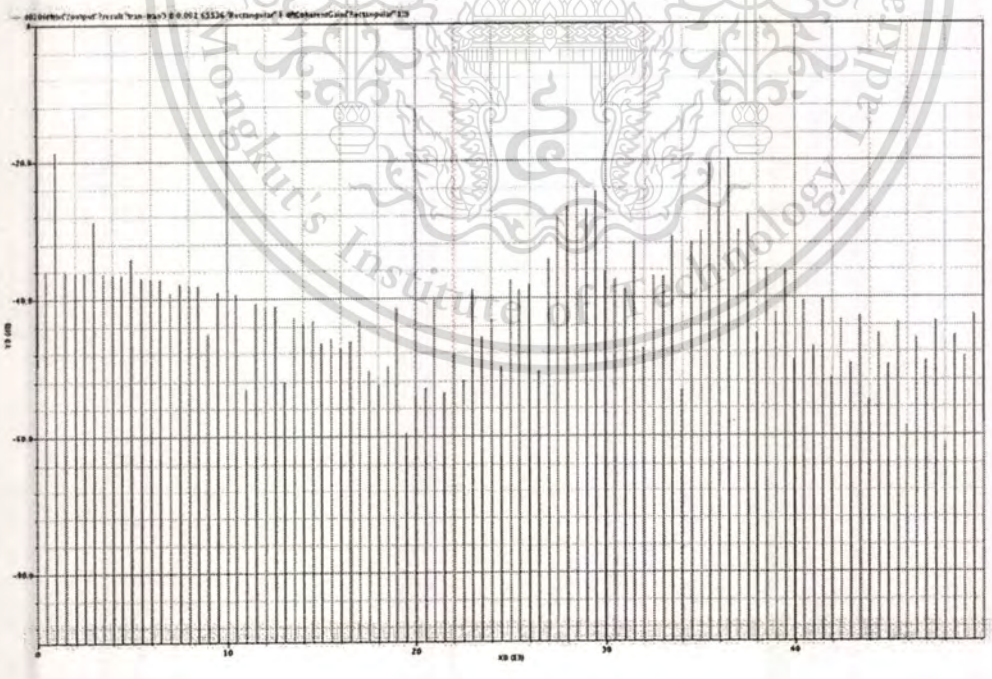


Fig.5.37. The spectrums of the sigma delta modulation output shown in Fig 5.36.

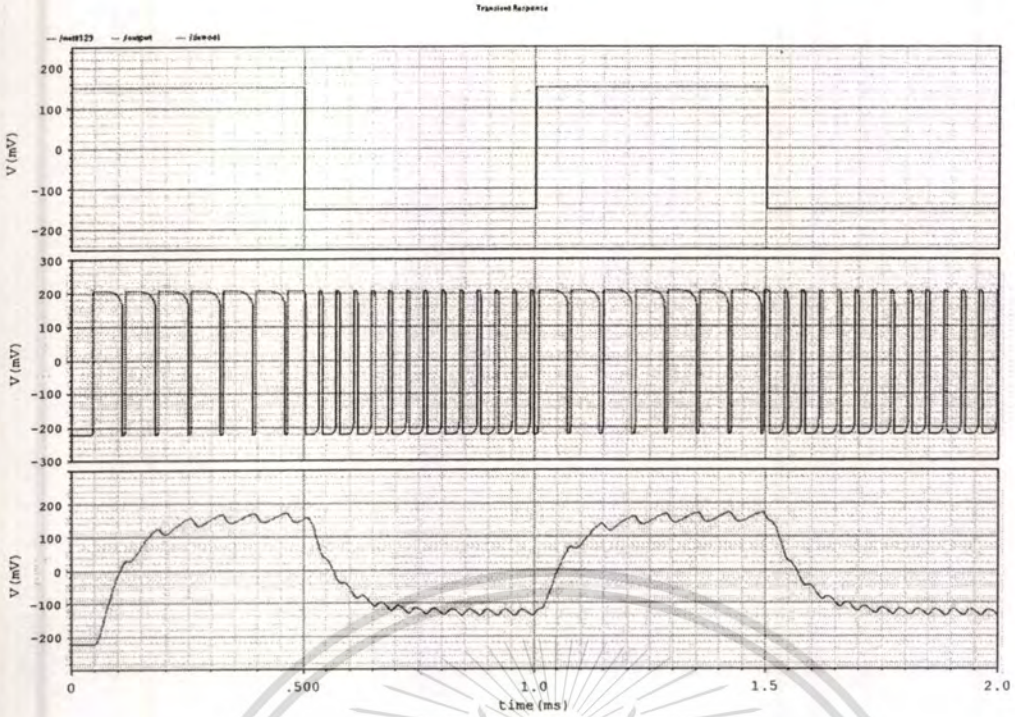


Fig.5.38. Simulation result for sigma delta modulation where the upper trace is 1 kHz, 0.3 V_{PP} square wave modulating signal, the middle trace is the sigma delta modulation output and the lower trace is low pass filter output.

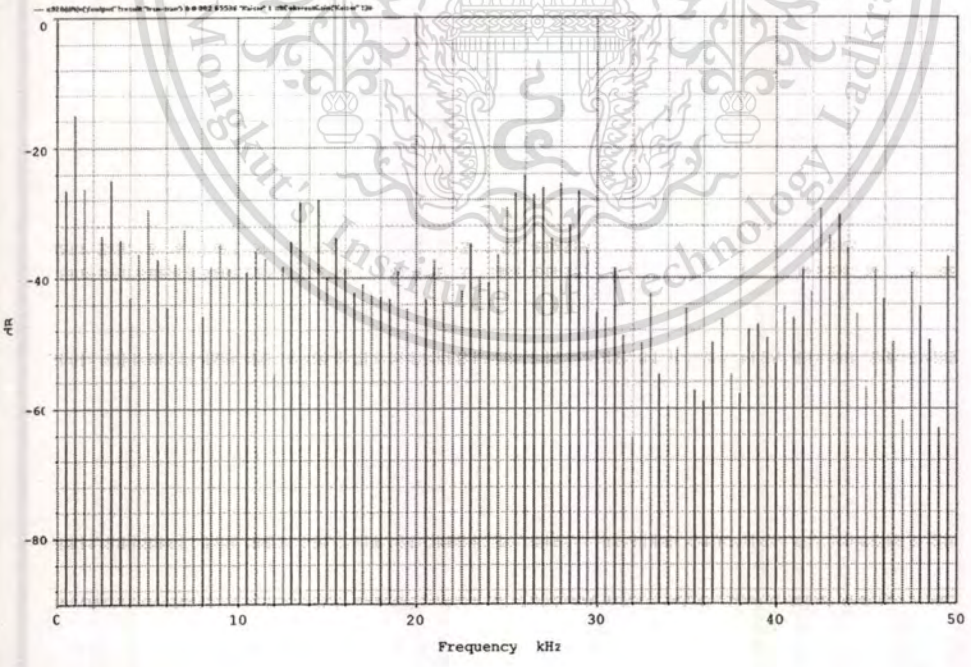


Fig.5.39. The spectrums of the sigma delta modulation output shown in Fig 5.38.

Furthermore, the circuit performance of sigma delta modulation is evaluated by SDR versus input level (dBr) as given in Fig.5.40. It is noted that SNDR is defined to SNR plus THD in baseband and 0 dBr is defined as full swing of input signal [24].

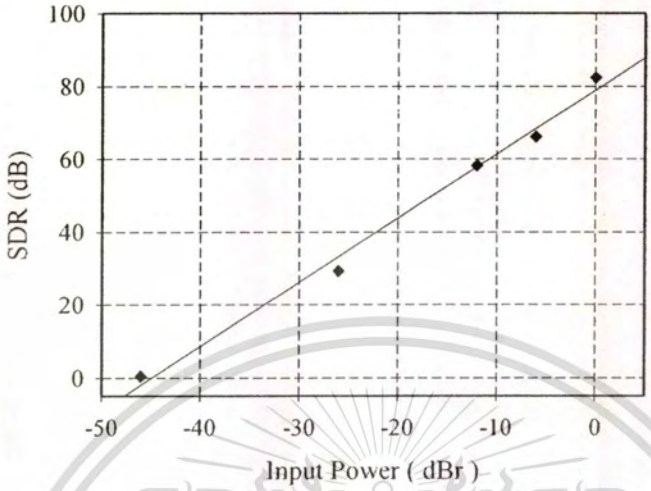


Fig.5.40. SDR(dB) versus input level (dBr) for 1 kHz sinusoidal wave

5.3.5 Simulation results of delta modulator circuit

Without adding any component, delta modulation application can be achieved. The following results are the delta modulation signal and their magnitude spectrum as shown in Fig 5.41- Fig 5.52.

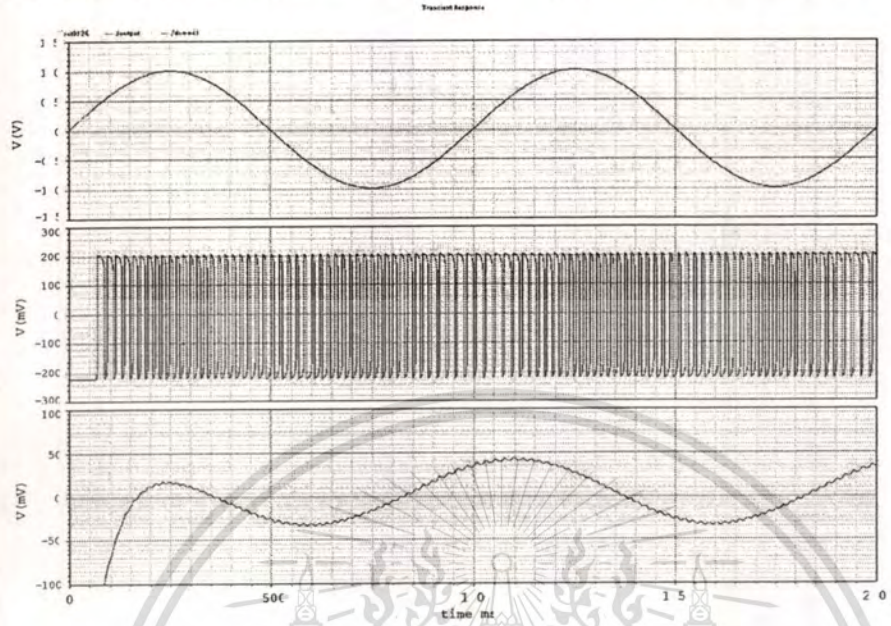


Fig.5.41. Simulation result where the upper trace is 1 kHz, 2 V_{PP} sinusoidal modulating signal, the middle trace is the delta modulation output and the lower trace is low pass filter output.

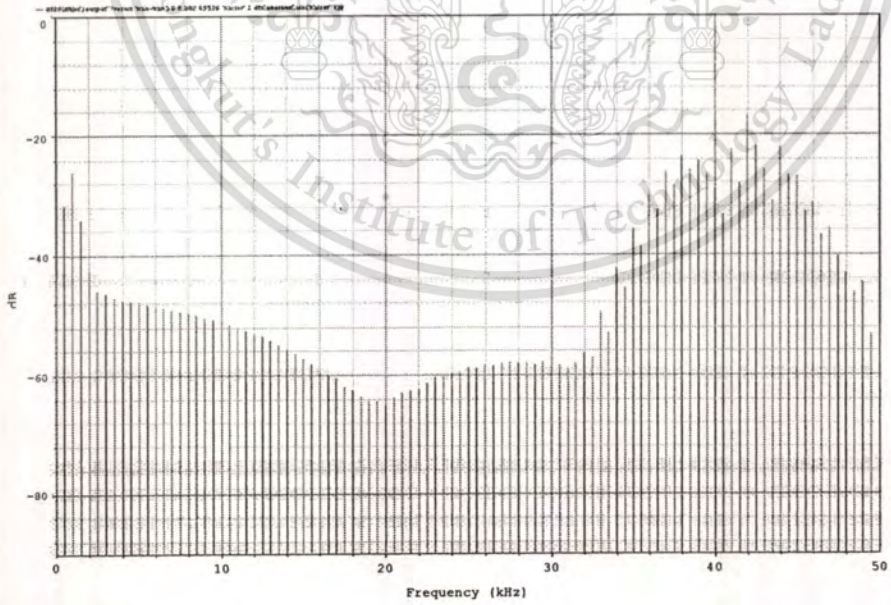


Fig.5.42. The spectrums of the delta modulation output given in Fig 5.41.

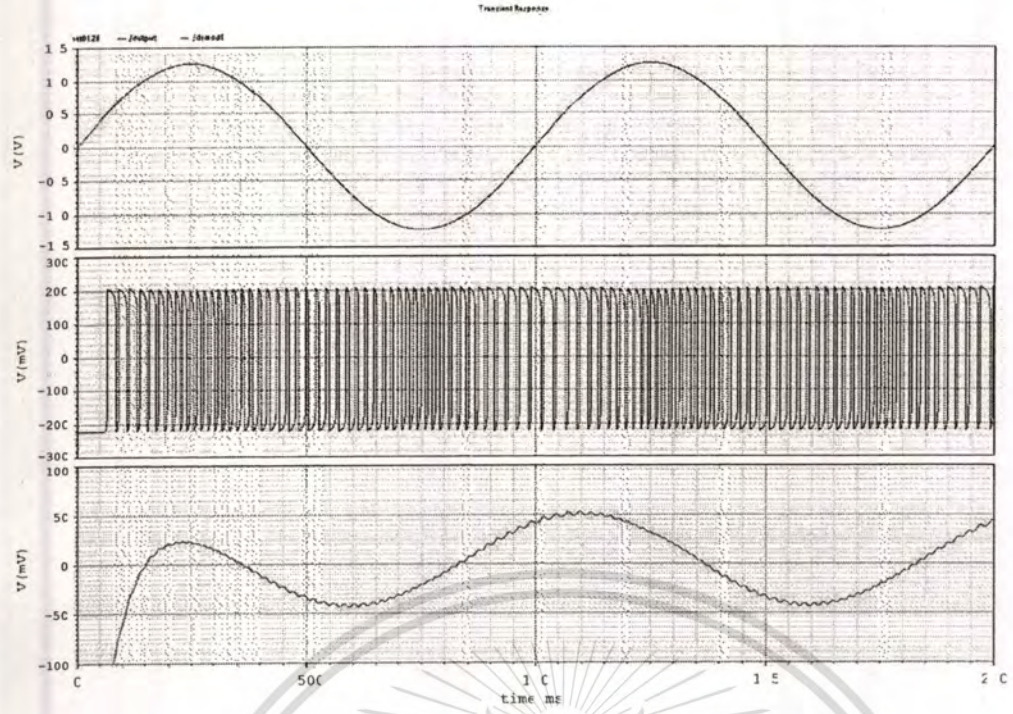


Fig.5.43. Simulation result where the upper trace is 1 kHz, 2.5 V_{PP} sinusoidal modulating signal, the middle trace is the delta modulation output and the lower trace is low pass filter output.

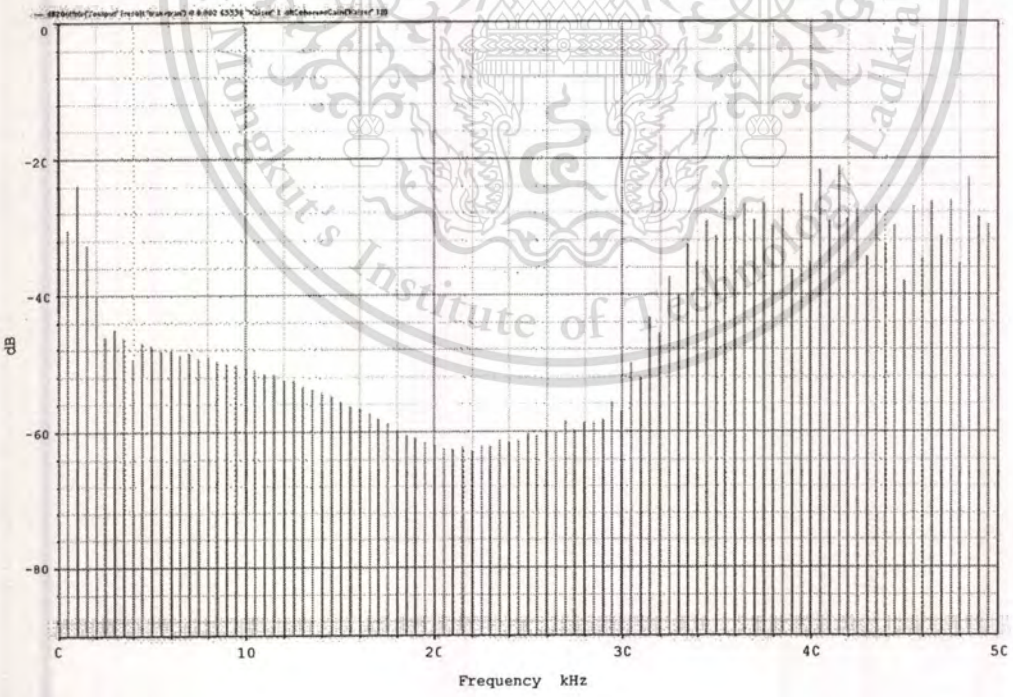


Fig.5.44. The spectrums of the delta modulation output given in Fig 5.43.

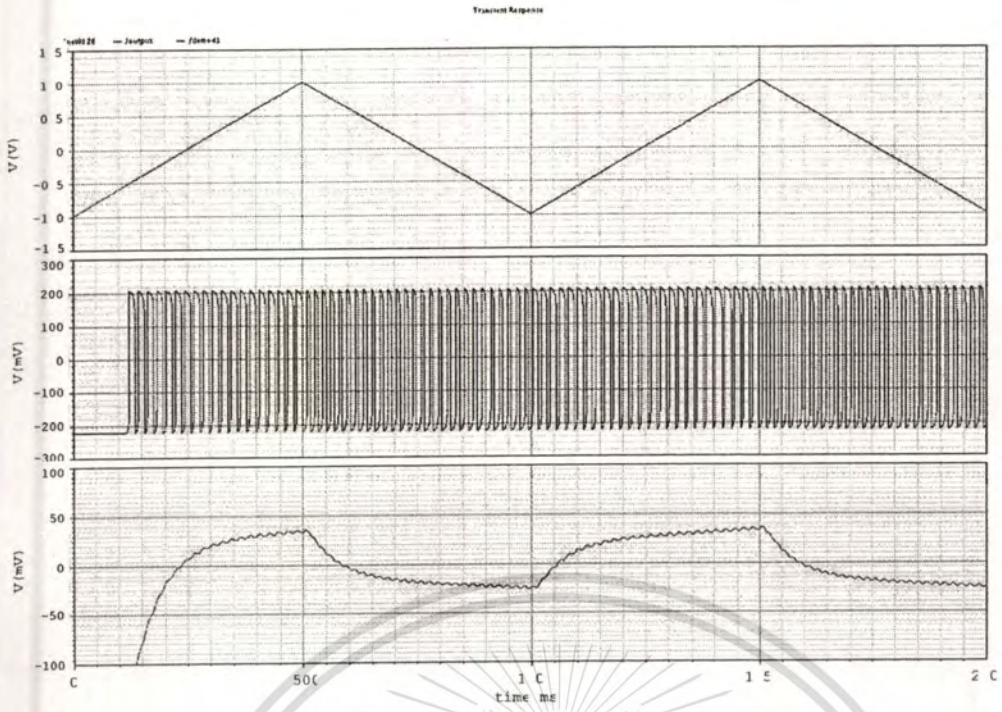


Fig.5.45. Simulation result where the upper trace is 1 kHz, 2 V_{pp} triangular wave modulating signal, the middle trace is the delta modulation output and the lower trace is low pass filter output.

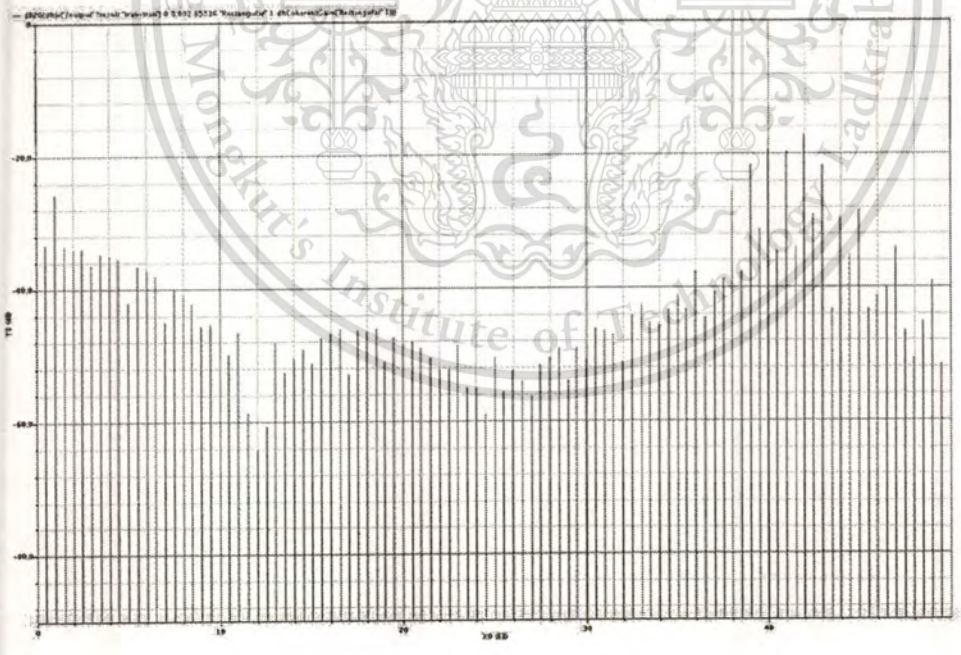


Fig.5.46. The spectrums of the delta modulation output given in Fig 5.45.

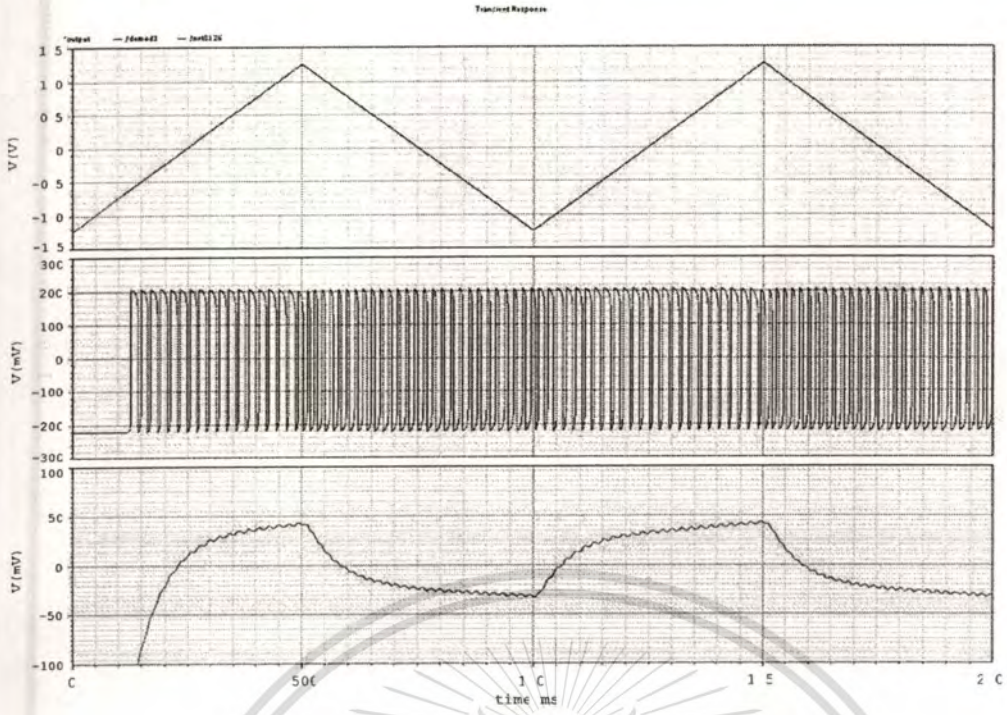


Fig.5.47. Simulation result where the upper trace is 1 kHz, 2.5 V_{PP} triangular wave modulating signal, the middle trace is the delta modulation output and the lower trace is low pass filter output.

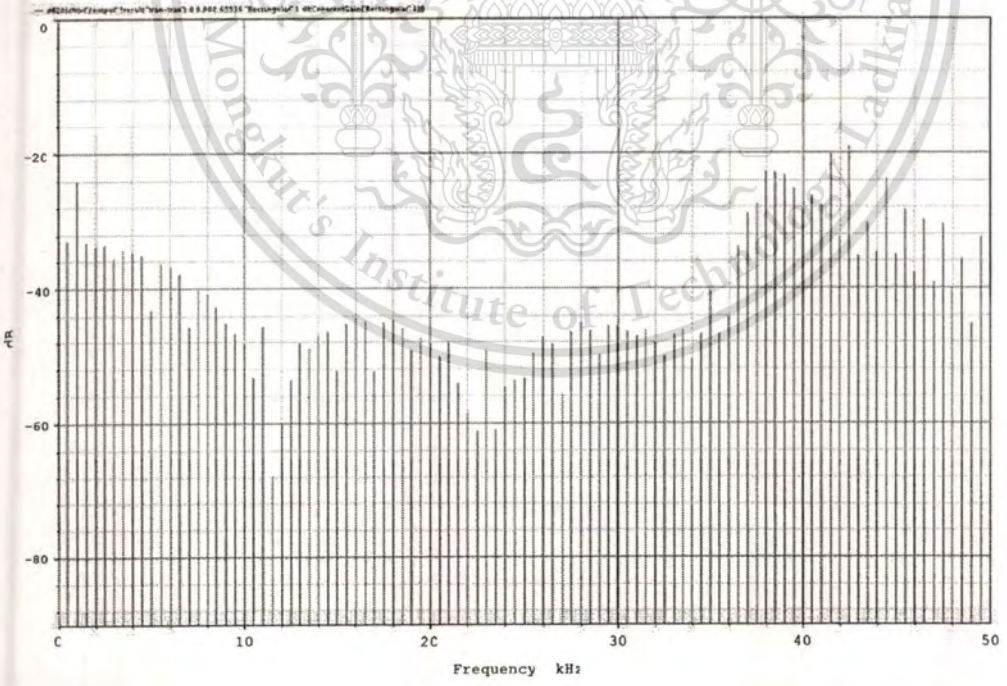


Fig.5.48. The spectrums of the delta modulation output given in Fig 5.47.

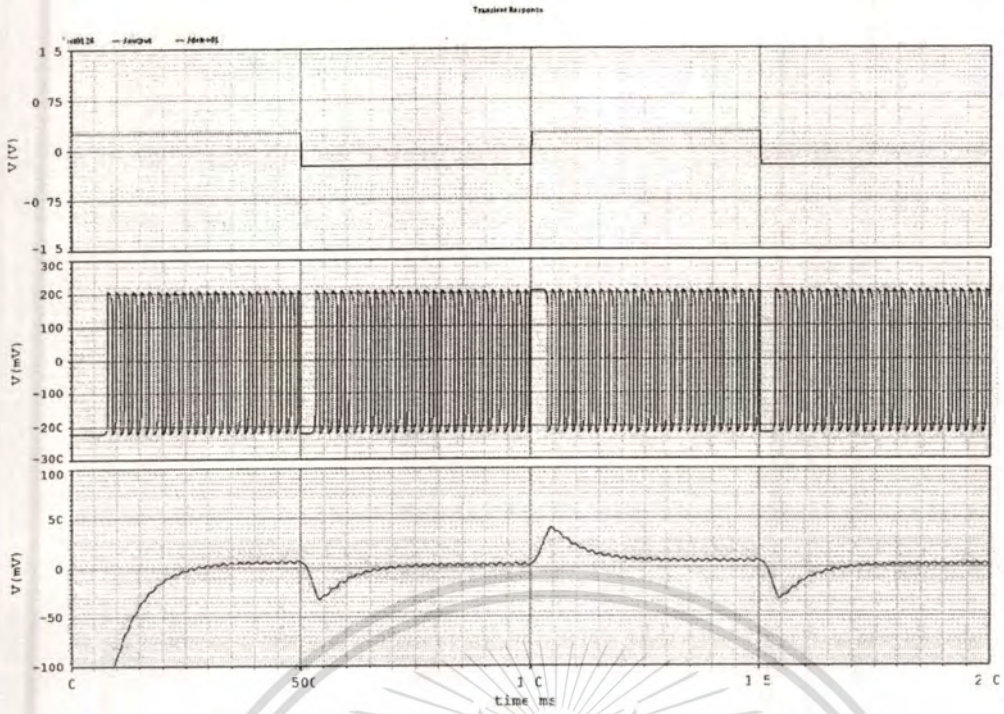


Fig.5.49. Simulation result where the upper trace is 1 kHz, 0.5 V_{PP} square wave modulating signal, the middle trace is the delta modulation output and the lower trace is low pass filter output.

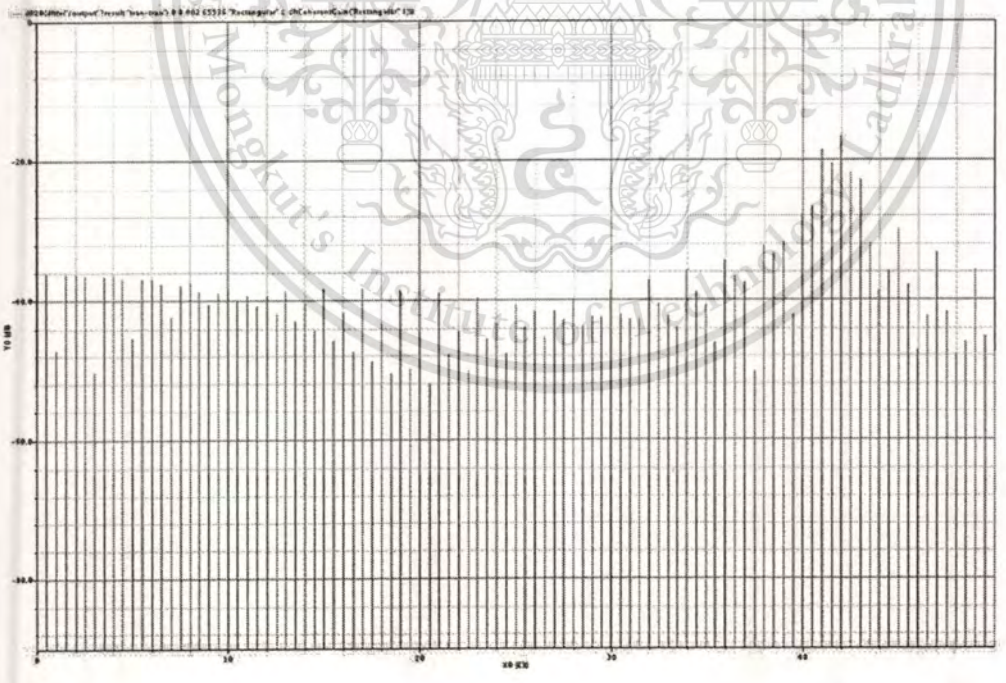


Fig.5.50. The spectrums of the delta modulation output given in Fig 5.49.

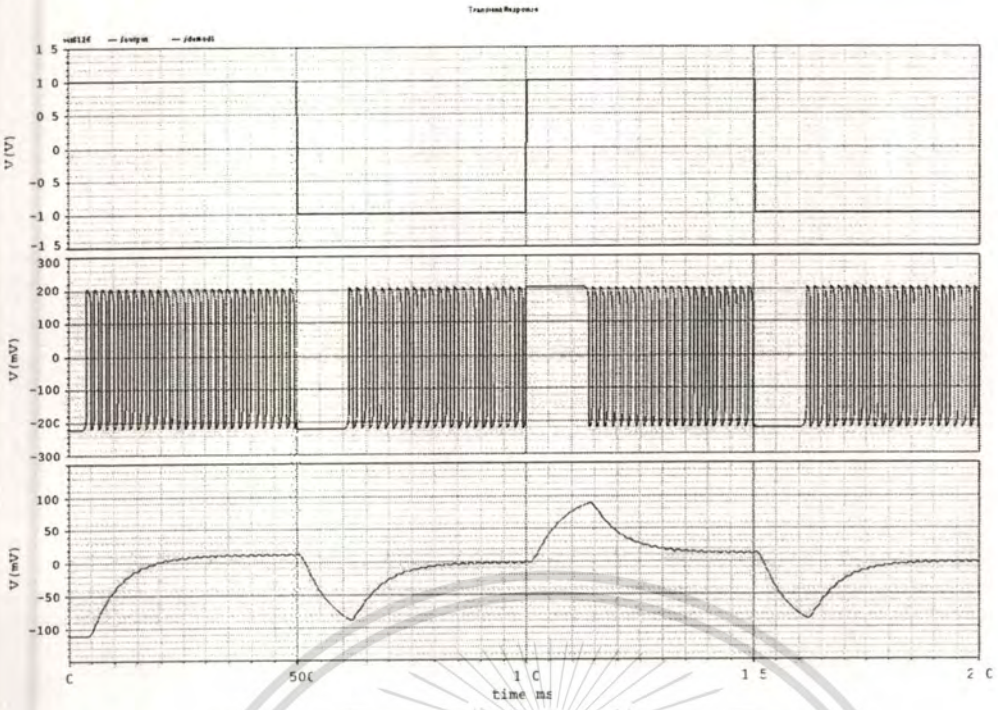


Fig.5.51. Simulation result where the upper trace is 1 kHz, 2 V_{PP} square wave modulating signal, the middle trace is the delta modulation output and the lower trace is low pass filter output.

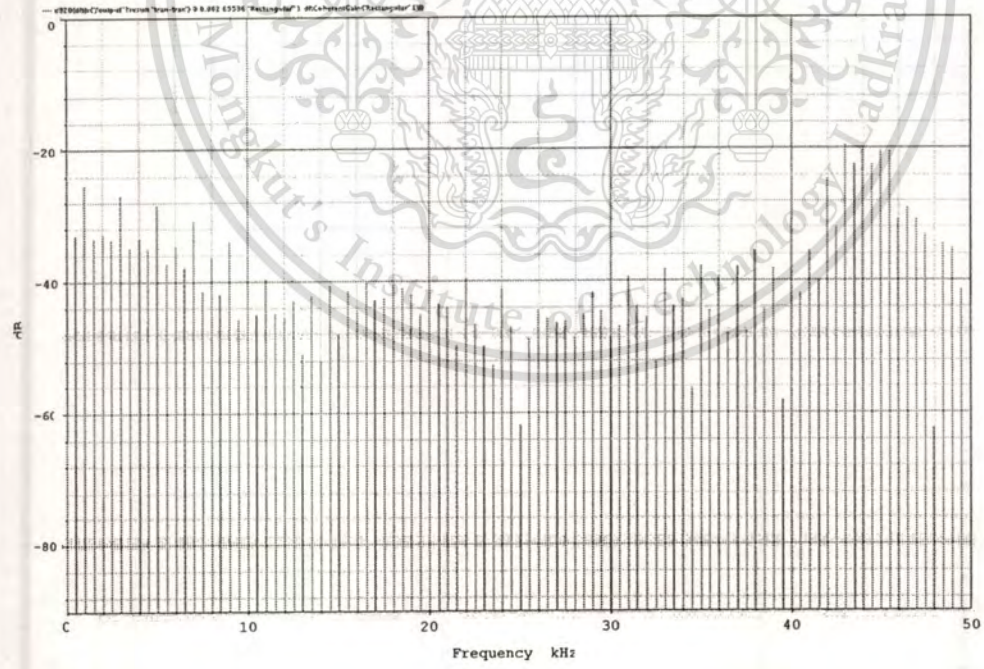


Fig.5.52. The spectrums of the delta modulation output given in Fig 5.51.

5.4 Analog layout design

5.4.1 Layout design rule

The physical layout of the circuit which is manufactured by using a fabrication process must be confirmed to a set of geometric constraints, which are generally called layout design rules. These rules usually specify the minimum allowable line widths for physical objects on chip such as a metal, a polysilicon interconnects, a diffusion areas, a minimum feature dimensions and a minimum allowable separations between two objects. If a metal line width is too small, for example, it is possible for the line to break during the fabrication process, resulting in an open circuit. If the two lines are placed too close to each other in the layout, they may form an unwanted short circuit by merging during or after the fabrication process. The main objective of design rules is to achieve a high overall yield and reliability while using the smallest possible silicon area. The design rules are usually described in two ways:

1. Micron rules, in which the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers.

2. Lambda rules, which specify the layout constraints in terms of a single parameter and thus allow linear, proportional scaling off all geometrical constraints.

5.4.2 Layout of MOS transistor

The final step in integrated design is physical description which consists of defining the masks to be used for processing. A MOS transistor is achieved by the simple overlap of two rectangles: one defining the active area and the other defining the polysilicon gate. A typical layout of a NMOS transistor is shown in Fig.5.53. It represents a pattern typical of analog circuits: the aspect ratio (W/L) of the transistor is not at a minimum, as is usually the case for analog designs.

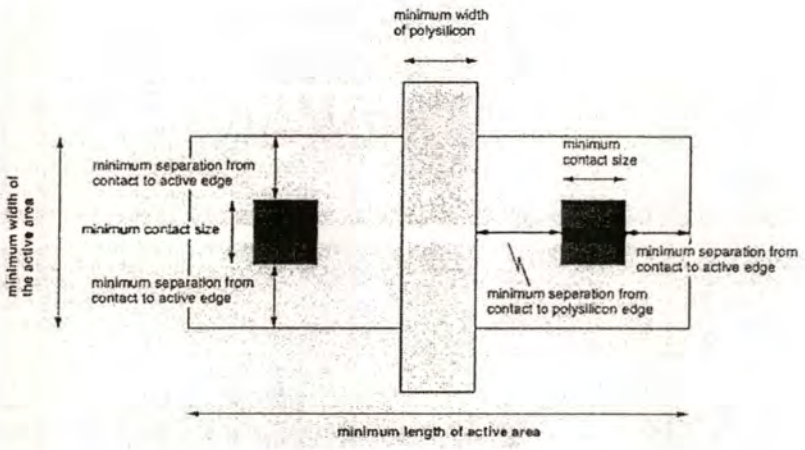


Fig.5.53. Layout of NMOS transistor

The key points to consider when draw transistor layouts are the following:

- Parasitic resistances at source and drain must be kept as low as possible.
- Parasitic capacitances should be minimized.
- Matching between paired elements is very important.

Concerning the first condition, it should remember that drain and source diffusions have a given sheet resistance. With only a few squares, it thus can achieve the hundreds of ohms of resistance. Even with a current as low as few tens of μA, it can drop voltage of millivolt. Therefore, the following choices are good in practical in layout to minimize parasitic resistance:

- Use as many metal connections as possible
- Use multiple contacts as possible if space allows. Moreover, many contacts placed close to each other also make the surface of metal connections smoother than when using only one contact.

Parasitic capacitances derive from the reverse source-substrate or drain substrate diodes. It was seen that this is useful in establishing good contacts. Hence, source and drain area must be large enough to accommodate contacts and to fulfill the design rules. However, it is possible to reduce the source and drain area and reduce the parasitic capacitances. This is achieved by using the layout that split into a given number parts that are connected in parallel that is called multifinger techniques.

Matching is very important when design current mirrors and differential pairs. In general, bad matching produces high offset. Therefore, we have to use layouts that optimize matching. This is achieved by providing the best symmetrical conditions.

5.5 Layout of a novel versatile modulator circuit

Using the techniques of analog layout as described above, the CMOS OTA layout is designed. An inter digitized transistor method and a symmetry technique have been applied to improve matching performance. In addition, the guard ring is employed to shield each transistor from leakage current. Each PMOS is surrounded by N-Well guard ring which is tied to V_{DD} but each NMOS is not required to be guarded. The layout without the pads is illustrated in Fig.5.54. where the total area is 0.004 mm^2.

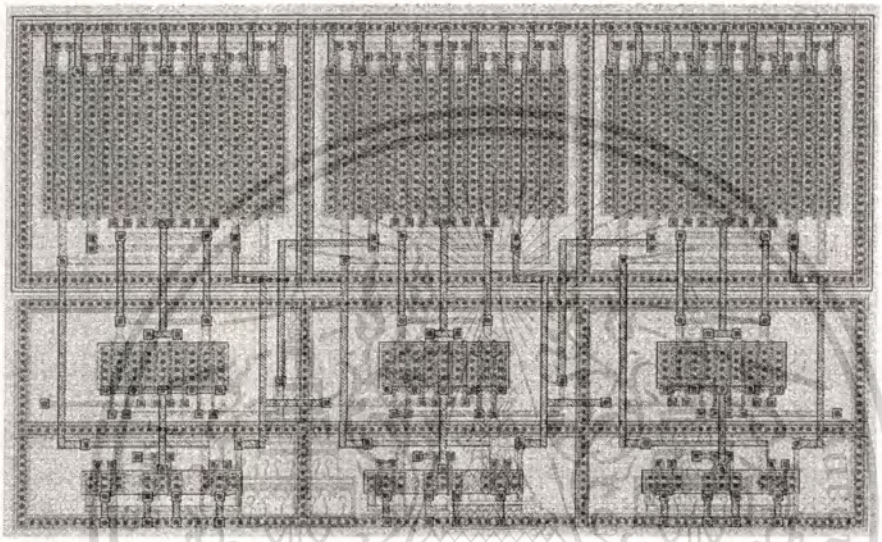


Fig.5.54. Physical Layout of the OTA

CHAPTER 6

Conclusions

Based upon the most classical modulator networks were designed by using complex circuits, they consequently provide a large scale, power consumption and low frequency range of the modulators. In order to be fitted in a modern and portable electronic device, low power dissipation of the circuit is required. It is thus necessary to design a single modulator circuit which occupies small area and low power consumption.

A simple versatile modulator which can be either delta modulator, sigma delta modulator, amplitude modulator or frequency modulator has been presented in this thesis. The advantage of the proposed scheme is that the clock signal which is the carrier used for modulation is inherent in the circuit, the modulating signal is thus only a required external signal. The proposed circuit is a single circuit that based on a Schmitt-trigger circuit. It is mainly composed of a few components: which are three OTAs, one capacitor and two resistors. With the compactness of the circuit, it is therefore suitable for IC realization.

Hence, the balanced OTA circuit was designed for simulation. The results show that this proposed circuit, which was fed the input signal at the different nodes in the circuit, can be functioned as various modulators. The power dissipation of this circuit is 1.32 mW, with total chip area is 0.18 mm^2. In addition, the performance of the proposed circuit in term of slew rate and the noise of OTA are also analyzed. Based on the low power consumption and small area, it can be applied for using in modern wireless and portable electronics. In addition, with a simple construction of the proposed circuit, it can be properly realized in integrated circuit technology as well. Moreover, in comparison the classic scheme with the proposed circuit in this thesis, it is summarized in Table III.

Table III. Comparison with the other research

Research		[1]	[2]	[3]	[4]	[5]	[9,10]	Thesis
Mode of modulator	Single mode	✓	✓	✓	✓	✓		
	Multi mode						✓	✓
Circuit structure	Complex circuit	✓			✓			
	Single circuit		✓	✓		✓	✓	✓
Carrier/Clock	Inherent		✓	✓		✓	✓	✓
	External	✓			✓			
Frequency range		middle	middle	middle	middle	low	middle	high

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APPENDIX

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A novel versatile modulator circuit

Panwit Tuwanut, Jeerasuda Koseeyaporn*, Paramote Wardkein

Telecommunication Department, Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL), Ladkrabang, Bangkok 10520, Thailand

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Abstract

A novel versatile modulator that can operate either as a delta modulator, a sigma-delta modulator, an amplitude modulator or a frequency modulator is presented. The proposed circuit mainly composes of a few components: which are three OTAs, one capacitor and two resistors. Among these components, two OTAs and two resistor construct a Schmitt trigger network whereas the other OTA and a capacitor compose an integrator. The advantage of this circuit is that the clock (carrier) signal employed for modulation is inherent in the circuit. No external clock is needed, only the modulating signal is required for an input. With the compactness of the circuit, it is thus suitable for IC realization. The computer simulation based on CMOS technology demonstrates that the results agree well with the theoretical analysis.

Keywords: CMOS OTA; AM; FM; Delta modulation; Sigma delta modulation

1. Introduction

It is well known that modulator circuits have played an essential role in communication systems. One reason is that modulators can shift the spectrum of modulated signal to frequency range that is satisfied with frequency characteristic of transmission medium. Generally, modulators can be classified into two main categories which are analog modulation and digital modulation. For analog modulators, amplitude modulation and frequency modulation are mostly employed in radio and television broadcast system. On the other hand, delta modulation and sigma delta modulation, which are digital modulation, are widely employed in digital communication, digital signal processing and power system.

In the past, most modulator networks were designed by using composite circuits, causing a large scale, power consumption and low-frequency range of the obtained modulator. Many researches thus had been intensively studied to alleviate these problems. It is noted that most of these modulators were based on relaxation oscillator [1–5]. Among these proposed modulators, the circuits given in [4,5] can function either as delta modulator or sigma delta modulator.

In term of sigma delta modulator, most proposed circuits [6–9] focused on the construction of circuits which either were based on switch capacitor or MOS structures. However, the main disadvantage of these circuits is that the carrier (clock) signal is not included in the circuits. The external carrier signal is thus required.

As has been described above, a novel versatile modulator circuit which has an inherent clock signal and can provide either sigma-delta modulator, delta modulator, amplitude modulator, or frequency modulator is proposed. The fundamental principle of the proposed circuit is based on a pulse generator (a Schmitt-trigger circuit) which is composed of a few components: three OTAs, one capacitor and two resistors. Based on this simple pulse generator, it is found that amplitude and frequency of the oscillated pulse signal can

* Corresponding author. Tel.: +66 232 64242.
E-mail address: kkjeeras@kmitl.ac.th (J. Koseeyaporn).

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be electronically adjusted. With the ability of amplitude control and frequency control in electrical, the circuit then can be applied for amplitude modulation and frequency modulation, respectively. In addition, without an additional device requirement, the proposed circuit can also function either as a sigma-delta modulator or a delta modulator when an input signal is provided at the proper node. The performance analysis of the proposed scheme has been investigated. In addition, the proposed circuit can be perfectly realized in IC structure where the results of computer simulation with CMOS technology confirm well with the obtained analysis.

In this paper, the organization of the contents is given as follows. The circuit description and operation will be addressed in Section 2. For Section 3, the circuit realization with CMOS technology is described. In addition, the performance analysis which is demonstrated in terms of frequency error due to the effect of slew rate is discussed in Section 4. To verify the analysis, simulation results of the proposed circuit based on CMOS technology are illustrated in Section 5. Finally, Section 6 is devoted to the conclusions of this paper.

2. Circuit description and operation

2.1. A pulse generator

In this section, let us begin with a pulse generator which has played an important role in this work. The circuit employed in here is basically modified from Schmitt trigger [10–12] as illustrated in Fig. 1. As can be seen, an OTA1 and a timing capacitor C function as an integrator whose time constant is directly proportional to the bias current I_{B1}.

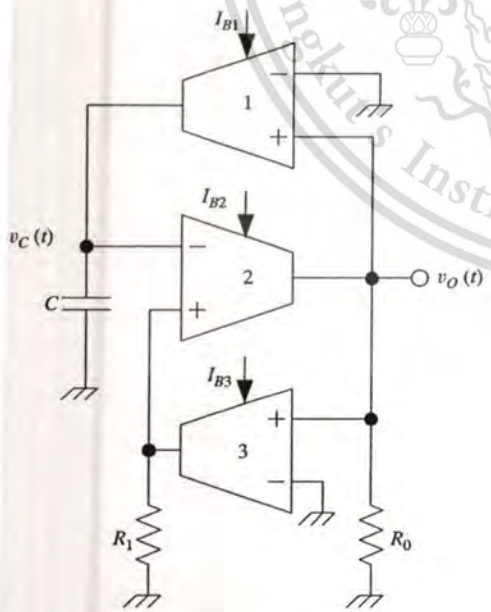

Fig. 1. The proposed circuit.

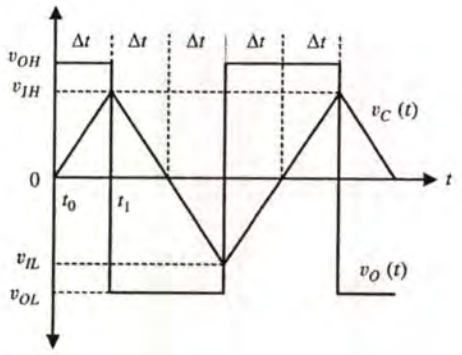

Fig. 2. The oscillated signals of the proposed circuit.

Next, the voltage divider circuit is achieved by a resistor R_1 and an OTA3 where the threshold level (v_{IH}, v_{IL}) is varied with the bias current I_{B3}. For the last part, an OTA2 is a comparator whose saturation voltage across a resistor R_O is directly controlled by the bias current I_{B2}.

For the operation of the pulse generator, it can be described as follows. At the first instance, it is supposed that the voltage across the capacitor is zero ($v_C(0) = 0$) and all OTAs are operated in saturate mode. When the power supplies are turned on, the OTA2 and the OTA3 give the output current I_{OTA2} and I_{OTA3}, respectively. These currents are assumed to be outward of the OTAs, then the upper threshold voltage of the OTA3 is

$$v_{IH} = I_{OTA3} R_1. \tag{1}$$

Simultaneously, the OTA1 provides the output current I_{OTA1} causing the capacitor C to be charged. The voltage $v_C(t)$ is then linearly increased. When this voltage level is nearly close to the threshold voltage v_{IH}, the output current of the OTA2 starts to change its direction. As a result, the threshold voltage of the OTA3 is changed to its lowest value, which is

$$v_{IL} = -I_{OTA3} R_1. \tag{2}$$

Suddenly, the output current of the OTA1 converts its direction and flows into the device, the capacitor C is discharged resulting in linearly decreasing of the voltage $v_C(t)$. When this voltage level is almost equal to the lower threshold voltage v_{IL}, the output current of the OTA2 starts changing its direction again. The same operation of the proposed circuit is therefore repeated, which is based on periodical charge and discharge of the capacitor. Consequently, the triangular wave and square wave are then generated which can be graphically shown in Fig. 2.

2.2. Oscillation frequency

In the previous subsection, the operation of the proposed circuit and how the fundamental triangular and square wave are generated have been described. The oscillated frequency

thus will be discussed in this subsection. It is noted that all of active elements employed in the circuit are assumed to be ideal.

For the explanation, let us begin with the relation between voltage and current of the capacitor which is

$$i_C = C\frac{dv_C(t)}{dt}. \tag{3}$$

By rearranging of Eq. (3) that is

$$\frac{i_C}{C} = \frac{dv_C(t)}{dt} \approx \frac{v_C(t_1) - v_C(t_0)}{t_1 - t_0}. \tag{4}$$

As shown in Fig. 2, let us consider the voltage $v_C(t)$ at time t_0 and t_1, which are $v_C(t_1) = v_{IH}$ and $v_C(t_0) = 0$. Eq. (4) is thus rewritten to be

$$\frac{i_C}{C} = \frac{v_{IH} - 0}{t_1 - t_0} = \frac{v_{IH}}{\Delta t}. \tag{5}$$

It is found that the rising time Δt of the triangular wave then is

$$\Delta t = C\frac{v_{IH}}{i_C}. \tag{6}$$

Since $i_C(t) = I_{OTA1}$ and $v_{IH} = I_{OTA3}R_1$, it thus gives

$$\Delta t = CR_1\frac{I_{OTA3}}{I_{OTA1}}. \tag{7}$$

As can be seen in Fig. 2, the period of oscillation is four times of the rising time Δt which is

$$T = 4\Delta t = 4CR_1\left(\frac{I_{OTA3}}{I_{OTA1}}\right). \tag{8}$$

Thus, the oscillation frequency readily is

$$f = \frac{1}{4CR_1}\left(\frac{I_{OTA1}}{I_{OTA3}}\right). \tag{9}$$

Due to the fact that all OTAs are simultaneously operated in either saturation or non-saturation mode. The operation of OTAs is therefore briefly reviewed as follows.

Case I: The OTA1 and the OTA3 are operated in saturation mode.

When the OTA1 and OTA3 are operated in saturation mode, their output currents are at the maximum level which are I_{B1} and I_{B3}, respectively. The oscillated frequency of this case therefore is

$$f = \frac{1}{4CR_1}\left(\frac{I_{B1}}{I_{B3}}\right). \tag{10}$$

Case II: The OTA1 and the OTA3 are operated in non-saturation mode.

By realizing that the OTAs are in CMOS structure, the output current of the OTAs thus are $I_{OTA1} = g_{m1}v_O(t)$, $I_{OTA3} = g_{m3}v_O(t)$. It is noted that the transconductance of the OTA1 and the OTA3 [13] are approximately to be

$$g_{m1} = \sqrt{2\mu_n C_{OX}(W/L)I_{B1}} \quad \text{and}$$
$$g_{m3} = \sqrt{2\mu_n C_{OX}(W/L)I_{B3}},$$

respectively. It is also supposed that both OTAs are matched. By substituting these parameters into Eq. (9), it thus results in

$$f = \frac{1}{4CR_1}\sqrt{\frac{I_{B1}}{I_{B3}}}. \tag{11}$$

The relations in Eqs. (10) and (11) show that the oscillation frequency is independent on the transconductance of the OTAs. More importantly, it implies that not only frequency is temperature-insensitive but also can be electronically adjusted by the bias currents I_{B1} and/or I_{B3}. Furthermore, when the OTA2 is in saturation mode, the peak-to-peak amplitude of the output signal is given by

$$|v_{op-p}(t)| = 2I_{B2}R_O. \tag{12}$$

It is seen that the amplitude of the output signal can be electronically adjusted by the bias current I_{B2}. As previously described, it is obvious that the proposed circuit given in Fig. 1 has advantages in both temperature-insensitive and amplitude/frequency independently adjustment which are confirmed by Eqs. (10)–(12), respectively. However, the non-ideal effect of the active components can affect on the ideal operation which will be later discussed in Section 3.

2.3. Amplitude modulator circuit

Based on the fact that the amplitude of the pulse signal can be adjusted by electronic tuning which is confirmed by Eq. (12), hence, if the bias current I_{B2} is an information signal, the proposed circuit then operates as an amplitude modulator. With this concept, by assuming that the bias current I_{B2} is $I_{offset} + I_{m(t)}$, where I_{offset} is dc offset current and $I_{m(t)}$ denotes the information signal, Eq. (12) is then rewritten to be

$$|v_{op-p}(t)| = 2R_O|I_{offset} + I_{m(t)}|. \tag{13}$$

From Eq. (13), if I_{offset} is large enough, the magnitude of the modulated waveform will be proportional to $I_{m(t)}$, so that $|I_{offset} + I_{m(t)}| \geq 0$ at all time, or

$$I_{offset} \geq |I_{m(t)}|_{min}. \tag{14}$$

For a special case of single-frequency sinusoidal modulating signal, $I_m(t) = I_m \cos \omega_m t$, the relative proportion of information's magnitude and carrier's magnitude are defined as a modulation index of AM waveform, which is found to be

$$\text{modulation index} = \frac{|I_{m(t)}|_{min}}{|I_{offset}|}. \tag{15}$$

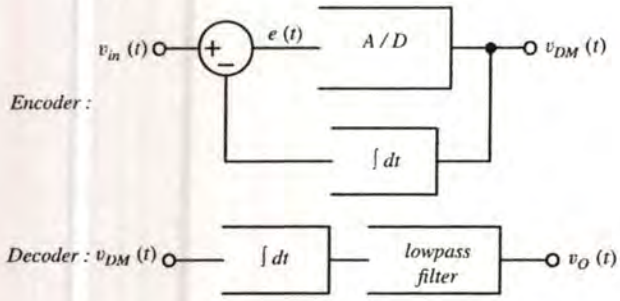

Fig. 3. Delta modulator system.

2.4. Frequency modulator circuit

As described in Section 2.2, the pulse's frequency can be electronically tuned as shown by Eqs. (11) and (12), then if I_{B1} performs as an information signal, the proposed circuit thus can be applied to be a frequency modulator. By assuming that the OTA1 and the OTA3 are operated in saturation mode where the bias current I_{B1} is the information signal $I_{m(t)}$, the frequency of the FM circuit thus is

$$f = \frac{I_{m(t)}}{4CR_1I_{B3}}. \tag{16}$$

The relationship in Eq. (16) indicates that the pulse's frequency is changed directly to the information signal. The changing ratio of the output frequency to the information signal is defined to be modulation sensitivity (k_f), as given by

$$k_f = \frac{\Delta f}{\Delta I_{m(t)}} = \frac{1}{4CR_1I_{B3}}. \tag{17}$$

2.5. Delta modulator circuit

For digital modulation, the basic technique is pulse code modulation (PCM). But major disadvantage of PCM is that there exists data redundancy in encoding digital signal. To alleviate this problem, the difference between a current sample and its predicted value has been instead encoded. Such technique is well known as differential pulse code modulation (DPCM). For a special case of DPCM which provides one-bit encoding output, it is known to be delta modulation (DM), whose system is shown in Fig. 3.

Now let us describe how the proposed circuit depicted in Fig. 1 can be applied for a delta modulator circuit. To achieve this application, the proposed circuit is slightly modified where the terminal of resistor R_1, rather than grounded, is employed to be a feeding node for the input signal. The modified circuit for a delta modulator is given in Fig. 4.

In this case, the capacitor and the OTA1 construct the integrator circuit, where $v_C(t) = \int v_O(t)\,dt$. When the input signal $v_{in}(t)$ is presented, it thus is compared with $v_C(t)$. The pulse output signal is therefore generated according to

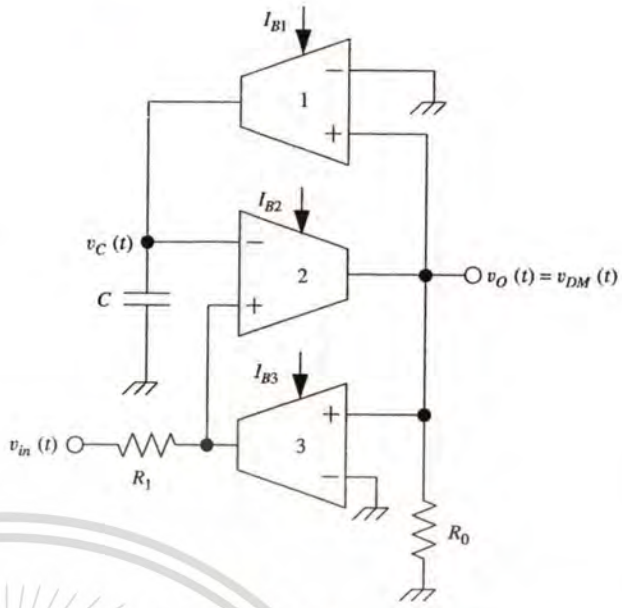

Fig. 4. The proposed circuit for a delta modulator.

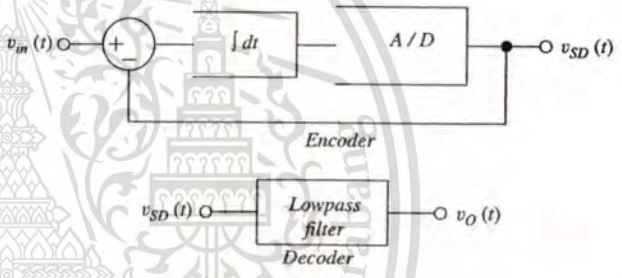

Fig. 5. Sigma-delta modulation system.

the different signal. Hence, the described operation confirms that this circuit is a delta modulator circuit.

2.6. Sigma-delta modulator circuit

For the delta modulator, its output signal is well known to be a differentiated version of the input signal. The integrator is therefore needed for the demodulation process. Hence, to omit the integrator in the demodulator, the input signal must be integrated before the modulation. Since an integrator operator is a linear function, i.e., $e(t) = \int v_{in}(t)\,dt - \int v_{DM}(t)\,dt = \int (v_{in}(t) - v_{DM}(t))\,dt$, a single integrator is only required in the modulator. The resulted system as depicted in Fig. 5 is well known to be a sigma-delta modulation system.

To apply the proposed circuit to be a sigma-delta modulator, it can be accomplished by feeding the input signal at the inverting node of the OTA1 as shown in Fig. 6. To describe the output signal of the sigma-delta modulator, let us consider the basic generated signals $v_C(t)$ and $v_O(t)$ as

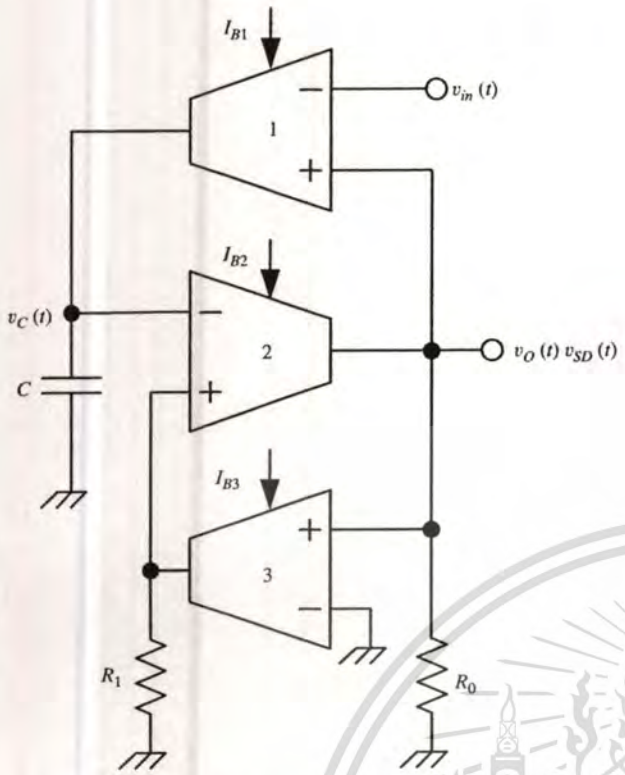

Fig. 6. The proposed circuit for a sigma-delta modulator.

illustrated in Fig. 2. It is seen that the capacitor and the OTA1 operate as an integrator. Hence, when $v_{in}(t)$ is present, the difference between the input signal $v_{in}(t)$ and the output signal $v_O(t)$ is thus integrated to be $v_C(t)$. When $v_C(t)$ is compared with the threshold voltage either v_{OH} or v_{OL}, it results in $v_O(t)$ which obviously is the sigma-delta modulator output.

3. Circuit realization

3.1. CMOS operational transconductance amplifier

A typical simple CMOS operational transconductance amplifier is shown in Fig. 7.

3.2. Circuit operation

Based on the circuit given in Fig. 7, let the MOSFET M_1 and M_2 be matched, and the current mirrors have unity current gain and all MOSFETs be operated in saturation region. In the circuit, the current i_2 is a reference current for the current source that is composed of the transistor M_4 and M_6, then $i_6 = i_2$. Likewise, the current i_1 is a reference current for the current source that comprises of the transistor M_3 and M_8, thus $i_8 = i_1$. Also, the current i_8 is a reference current for the current source that comprises of the transistor

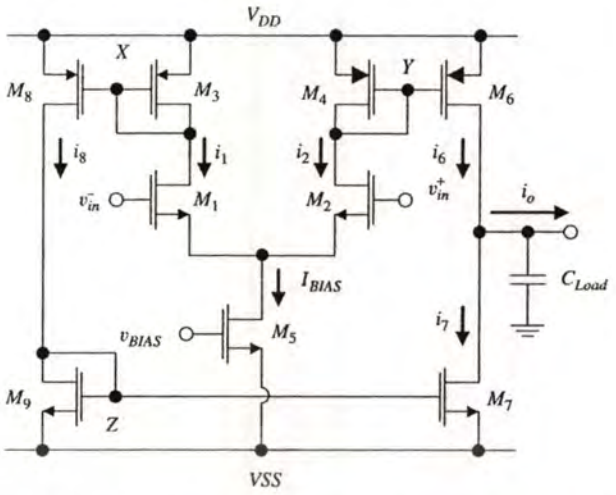

Fig. 7. A conventional CMOS operational transconductance amplifier.

M_7 and M_9, thus $i_7 = i_8$. The output current is then found to be

$$i_o = i_6 - i_7 = i_2 - i_1 \tag{18}$$

and is equal to the different current in the differential pair M_1 and M_2. Thus,

$$i_o = g_m v_{in}, \tag{19}$$

where the transconductance is

$$g_m = \sqrt{\mu_n C_{OX}(W/L)_{1,2} I_{BIAS}} \tag{20}$$

and μ_n is a carrier mobility, C_{OX} is a gate capacity per unit area and $(W/L)_{1,2}$ is an aspect ratio of M_1 and M_2.

3.3. Slew rate

In this circuit, the maximum current delivered to the load is I_{BIAS}. The slew rate (SR) then will be

$$SR = \frac{I_{BIAS}}{C_{LOAD}}, \tag{21}$$

where C_{LOAD} is the capacitance at the output node. To avoid limitation of settling time by slew rate, I_{BIAS} should be large enough. However, the increasing in I_{BIAS} leads to the increasing in static power dissipation.

4. Performance analysis

4.1. Frequency error by slew rate of the OTA

Due to the fact that the output voltage does not change instantaneously during the transition from the upper saturated voltage to the lower saturated voltage as shown in

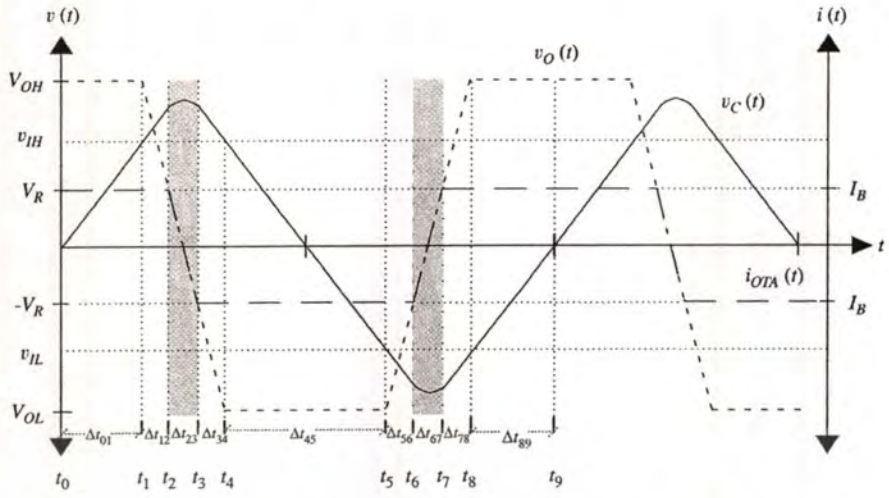

Fig. 8. Voltage waveforms including slew rate effect.

Fig. 8. The SR thus has influence on frequency of the oscillated signals.

As shown in Fig. 8, the period of oscillation is consisted of time interval of saturated operation and that of non-saturated operation. Based on the relationship between voltage and current of the capacitor as shown in Eq. (3), the SR is expressed as

$$\mathrm{SR} = \frac{\mathrm{d}v_o(t)}{\mathrm{d}t}. \tag{22}$$

Therefore, the time interval of saturated operation can be calculated by

$$\begin{aligned} T_{\mathrm{SAT}} &= \Delta t_{01} + \Delta t_{12} + \Delta t_{34} + \Delta t_{45} \\ &\quad + \Delta t_{56} + \Delta t_{78} + \Delta t_{89} \\ &= \left(C\frac{v_{\mathrm{IH}}}{I_{\mathrm{OTA1}}}\right) + \left(\frac{V_{\mathrm{R}} - v_{\mathrm{OH}}}{-\mathrm{SR}}\right) + \left(\frac{v_{\mathrm{OL}} - (-V_{\mathrm{R}})}{-\mathrm{SR}}\right) \\ &\quad + \left(-C\frac{v_{\mathrm{IL}} - v_{\mathrm{IH}}}{I_{\mathrm{OTA1}}}\right) + \left(\frac{-V_{\mathrm{R}} - v_{\mathrm{OL}}}{\mathrm{SR}}\right) \\ &\quad + \left(\frac{v_{\mathrm{OH}} - V_{\mathrm{R}}}{\mathrm{SR}}\right) + \left(-C\frac{v_{\mathrm{IL}}}{I_{\mathrm{OTA1}}}\right), \end{aligned} \tag{23}$$

whereas, the time interval of non-saturated operation can be expressed by

$$\begin{aligned} T_{\text{non-SAT}} &= \Delta t_{23} + \Delta t_{67} \\ &= \left(\frac{-V_{\mathrm{R}} - V_{\mathrm{R}}}{-\mathrm{SR}}\right) + \left(\frac{V_{\mathrm{R}} - (-V_{\mathrm{R}})}{\mathrm{SR}}\right). \end{aligned} \tag{24}$$

The summation of T_{SAT} and $T_{\text{non-SAT}}$ thus results in the period of oscillation, which is

$$\begin{aligned} T &= T_{\mathrm{SAT}} + T_{\text{non-SAT}} \\ &= \frac{2C(v_{\mathrm{IH}} - v_{\mathrm{IL}})}{I_{\mathrm{OTA1}}} + \frac{2(v_{\mathrm{OH}} - v_{\mathrm{OL}})}{\mathrm{SR}}. \end{aligned} \tag{25}$$

By substituting v_{IL} and v_{OL} by $-v_{\mathrm{IH}}$ and $-v_{\mathrm{OH}}$, respectively, it thus yields

$$T = 4C\frac{v_{\mathrm{IH}}}{I_{\mathrm{OTA1}}} + \frac{4v_{\mathrm{OH}}}{\mathrm{SR}}. \tag{26}$$

Furthermore, it is assumed that the saturated voltage (v_{OH}) is equal to the supply voltage (V_{DD}) and $v_{\mathrm{IH}} = I_{\mathrm{OTA3}}R_1$, Eq. (26) can be rewritten to be

$$T = 4CR_1\frac{I_{\mathrm{OTA3}}}{I_{\mathrm{OTA1}}} + \frac{4V_{\mathrm{DD}}}{\mathrm{SR}}. \tag{27}$$

Consequently, the oscillation frequency including the slew rate effect then is

$$f = \frac{1}{4CR_1(I_{\mathrm{OTA3}}/I_{\mathrm{OTA1}}) + 4V_{\mathrm{DD}}/\mathrm{SR}}. \tag{28}$$

From Eq. (28), it implies that if an OTA has high slew rate compared to $4v_{\mathrm{OH}}$ then the distortion in the oscillation frequency can be neglected.

5. Simulation results

The complete CMOS OTA circuit in Fig. 7 is designed and simulated using Cadence with level-3 process parameter of AMS 0.35 μm as shown in Table 1.

Table 1. Process parameters of AMS 0.35 μm

Parameter description	Typical parameter value		
	NMOS	PMOS	Unit
Threshold voltage (V_T)	0.5	−0.65	V
Transconductance parameter (K)	170	58	$\mu A/V^2$

For the specification of the designed OTA, the parameters are defined as follows: $V_{DD} = -V_{SS} = 1.65\,V$, slew rate = $100\,V/ms$ with 2 pF load, GBW = 100 MHz, power consumption $\leqslant 2\,mW$. Based on the specification, the aspect ratio $(W/L)_i$ of the ith MOS obtained from the designed procedures is summarized in Table 2.

It is found from the design that the power dissipation is 1.32 mW and the gain is 8000, then the specification of the desired OTA is satisfied. Next, the CMOS OTA layout is designed by using layout technique which can improve performance. A inter digitized transistor method and a symmetry technique have been applied to improve matching. In addition, the guard ring is employed to shield each transistor from leakage current.

Each PMOS is surrounded by N-Well guard ring which is tied to V_{DD} but each NMOS is not required to be guarded. The layout without the pads is illustrated in Fig. 9 where the total area is $0.18\,mm^2$. This designed OTA is employed to construct the proposed versatile modulator circuit. The circuit is simulated with $\pm 1.65\,V$ and R_1, R_2 are $2\,k\Omega$ and the capacitor is $0.01\,\mu F$.

Firstly, the simulated result of pulse generator (as shown in Fig. 1) is examined to demonstrate the ability of electronically amplitude and frequency control. The obtained results are given in Fig. 10 where y-axis on left-handed side and right-handed side are respectively for frequency and amplitude. For frequency adjustment, $I_{B2} = 0.1\,mA$, $I_{B3} = 0.2\,mA$ are employed whereas I_{B1} is varied as shown on the x-axis (bottom). For amplitude adjustment, I_{B2} is instead varied as shown on the x-axis (top) whereas $I_{B1} = 0.2\,mA$, $I_{B3} = 0.2\,mA$ are set.

In order to demonstrate the application from the ability of electrically amplitude control, the circuit is therefore applied for amplitude modulator. When input signal is fed to the bias input node of the OTA2, namely, $I_{B2}(t) = I_{m(t)}$.

Table 2. Summarized the aspect ratio $(W/L)_i$ of the ith MOS

MOS	(W/L) (μm)	MOS	(W/L) (μm)
M_1	16/0.35	M_2	16/0.35
M_3	107/0.35	M_4	107/0.35
M_5	3.6/0.35	M_6	107/0.35
M_7	3.6/0.35	M_8	107/0.35
M_9	3.6/0.35		

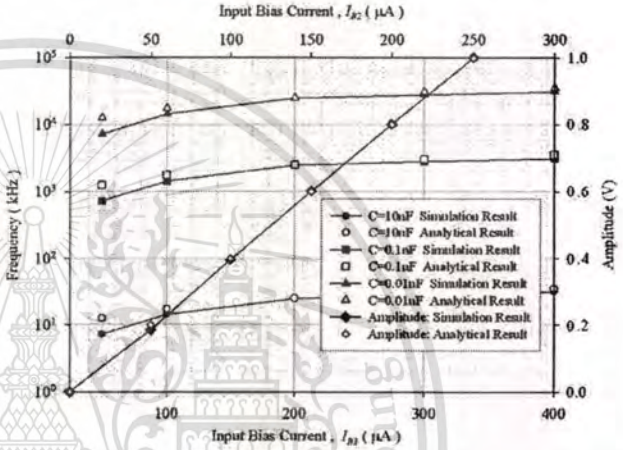

Fig. 10. Electronically control of frequency and amplitude of the proposed circuit.

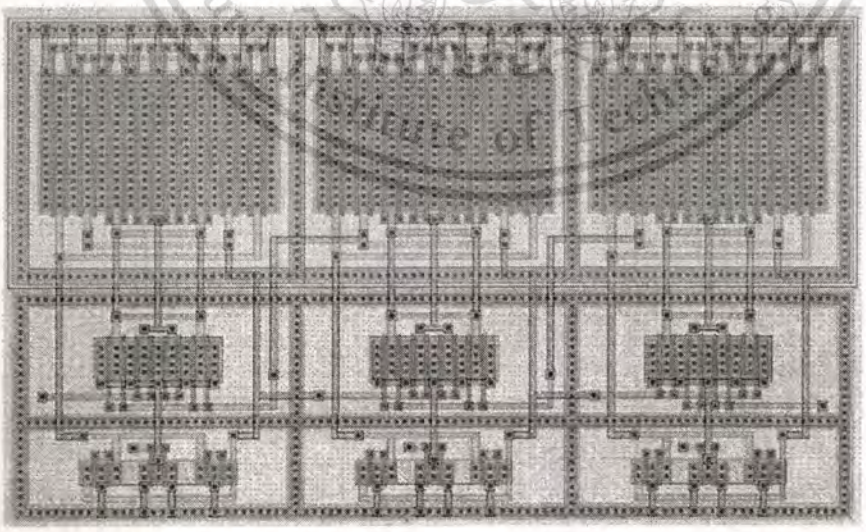

Fig. 9. Physical layout of the OTA.

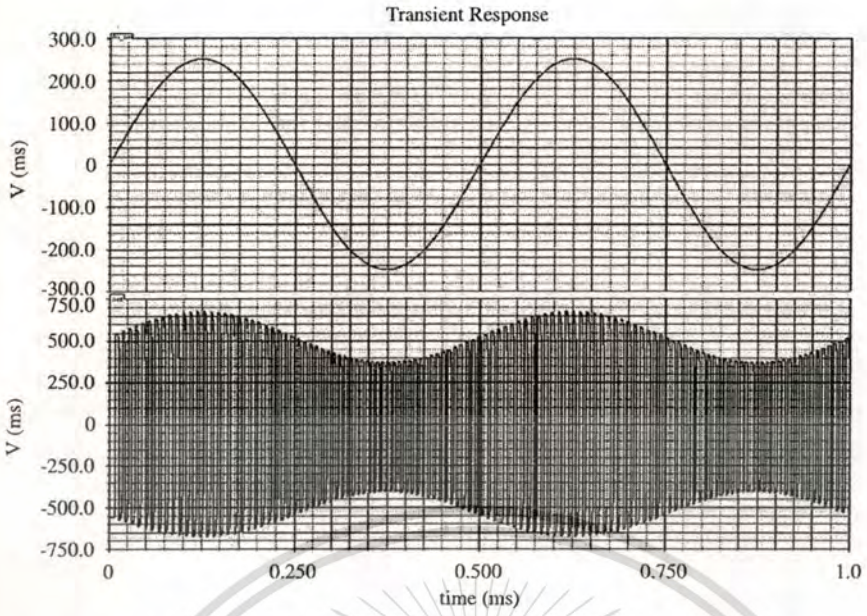

Fig. 11. Amplitude modulation result where upper trace is sinusoidal modulating signal (2 kHz frequency, 250 mV (333 A) amplitude) and the lower trace is square wave AM signal modulation output.

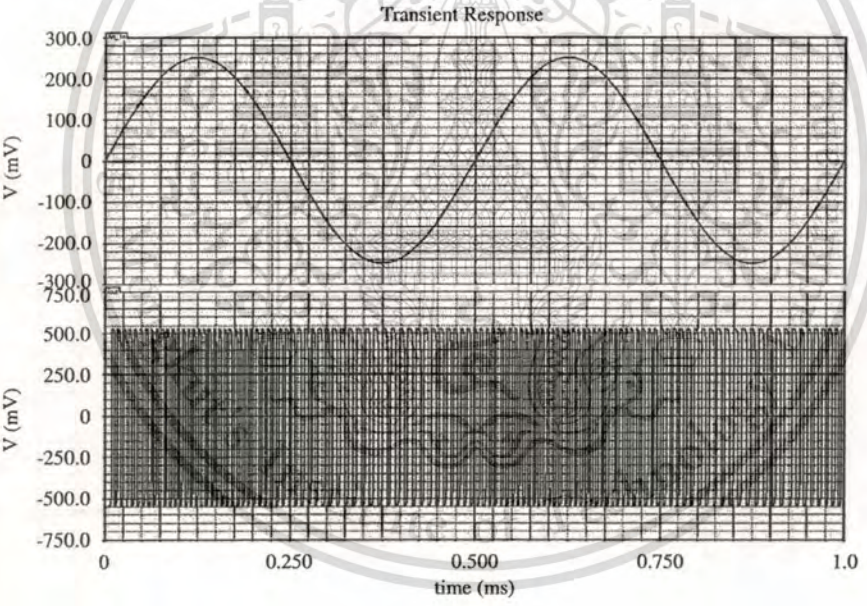

Fig. 12. Frequency modulation result where upper trace is sinusoidal modulating signal (2 kHz frequency, 250 mV (333 A) amplitude) and the lower trace is a square wave FM signal modulation output.

The magnitude of output signal is directly proportion to bias current of the OTA2. Let I_{B1} and I_{B3} be fixed at 0.2 mA which provide inherent 115 kHz carrier signal whereas 2 kHz frequency, 333 μA amplitude and 0 μA offset sinusoidal modulating input is employed. The modulation index which is given by the ratio of the magnitude of modulated signal to the offset current can be adjusted by changing either I_{offset} or $I_{m(t)}$. In this case, the modulation index of the circuit is 30%. Then generated amplitude modulation output is given in Fig. 11.

Later, with electrical frequency-control ability of the circuit, the circuit can then be functioned as a frequency modulator. When input signal is fed to the bias input node of the OTA1, namely, $I_{B1}(t) = I_{m(t)}$. The frequency of output signal is thus directly proportional to bias current of the OTA1. In this case, $I_{B2} = 0.1$ mA, $I_{B3} = 0.2$ mA are fixed resulting in

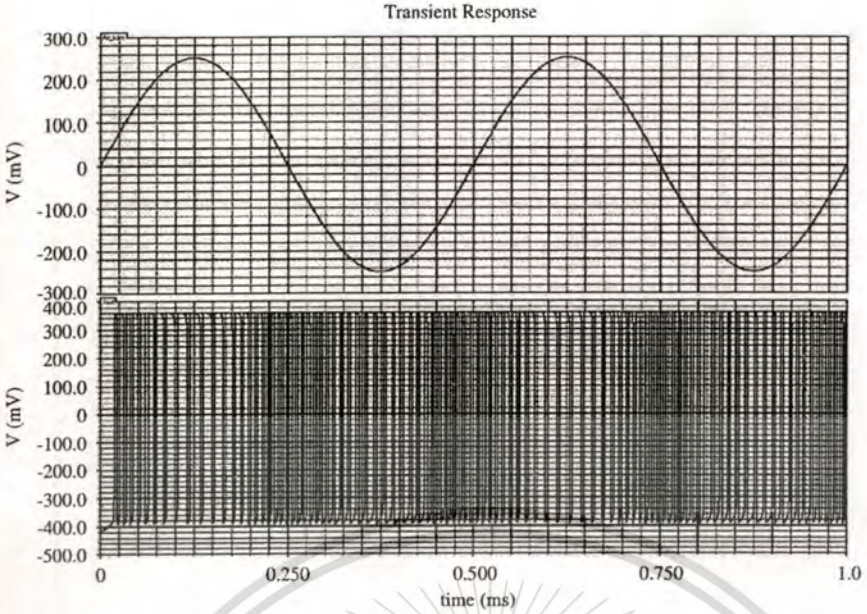

Fig. 13. Simulation results where upper trace is 2 kHz, $0.5V_{PP}$ sinusoidal modulating signal, the lower trace is a sigma-delta modulation output.

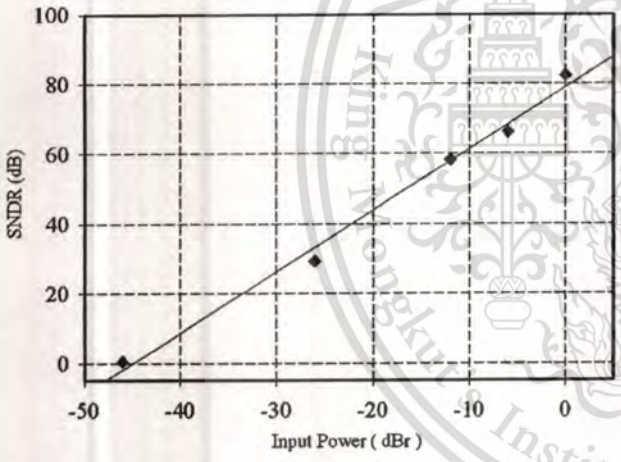

Fig. 14. SNDR(dB) versus input level (dBr) for 1 kHz sinusoidal.

inherent 115 kHz carrier signal. The 2 kHz frequency, 333 μA amplitude and 0 μA offset sinusoidal signal is employed for the modulating input. The obtained frequency modulation result is shown in Fig. 12. In this case, the modulation sensitivity (k_f) is 180 kHz/V and the modulation index is 22.5.

From the circuit depicted in Fig. 6, $I_{B1} = 0.2$ mA, $I_{B2} = 0.1$ mA and $I_{B3} = 0.2$ mA are fixed providing an inherent 100 kHz clock carrier signal. By setting $v_i(t) = 0.25\sin(4000\pi t)$ as shown in the upper trace of Fig. 13, the sigma delta output is then generated as depicted in the lower trace.

Furthermore, the circuit performance of sigma delta modulation is evaluated by SNDR (dB) versus input level (dBr) as given in Fig. 14. It is noted that SNDR is referred to as SNR plus THD in baseband and 0 dBr is defined as full swing of input signal [14].

Without adding any component, delta modulation application can be achieved. In the simulation, 4 kHz, $0.8V_{PP}$ triangular wave input signal is employed (see the upper trace of Fig. 15) where the delta modulation output is given in the lower trace of Fig. 15.

6. Conclusions

A simple versatile modulator which can be either delta modulator, sigma delta modulator, amplitude modulator or frequency modulator has been presented in this work. The advantage of the proposed scheme is that the clock signal which is the carrier used for modulation is inherent in the circuit, the modulating signal is thus only a required external signal. The simulation results illustrate that, without adding any additional device, the proposed circuit can function as various modulators by feeding input signal at different nodes in the circuit. The power dissipation of this circuit is 1.32 mW, with total chip area is 0.18 mm^2. Based on the low power consumption and small area, it can be applied for using in modern wireless and portable electronics. In addition, with a simple construction of the proposed circuit, it can be properly realized in integrated circuit technology as well.

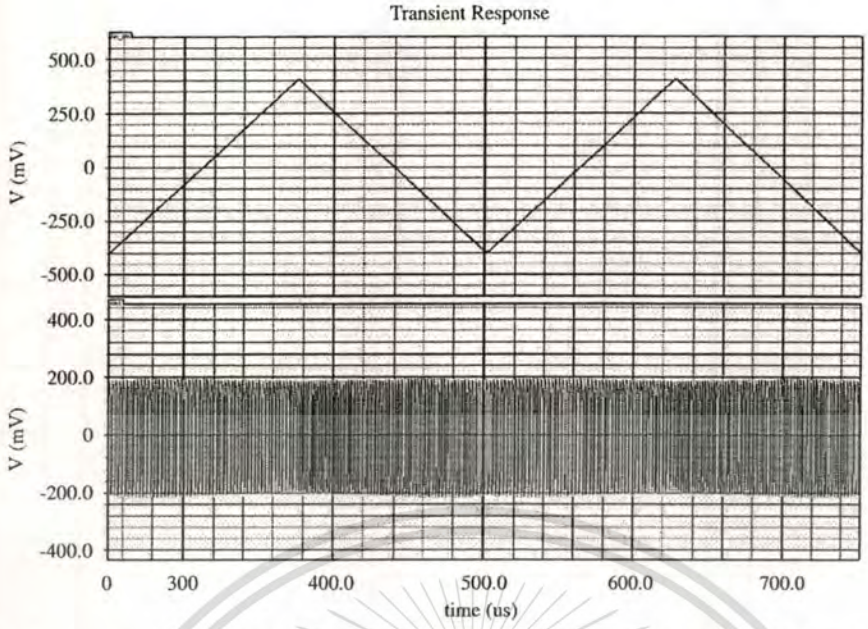

Fig. 15. Simulation results where upper trace is 1 kHz, $0.8V_{PP}$ triangular modulating signal, the lower trace is delta modulation output.

Acknowledgement

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Panwit Tuwanut received his B.Eng. in Telecommunication Engineering and M.Eng. degree in Electrical Engineering from King Mongkut Institute of Technology Ladkrabang (KMITL) in 1999 and 2003, respectively. Now he is currently working toward his D. Eng. degree in Electrical Engineering at KMITL.

Jeerasuda Koseeyaporn graduated M.S. and Ph.D. degrees in Electrical Engineering from Vanderbilt University, Nashville, TN, USA, in 1999 and 2003, respectively. She is currently an assistant professor of Telecommunication Engineering Department, Faculty of Engineering, KMITL, Thailand.

Paramote Wardkein received his M.E. and D.Eng. degree in electrical engineering from King Mongkut's Institute of Technology Ladkrabang (KMITL), Bangkok, Thailand, in 1990 and 1997, respectively. He is now an associate professor of the Department of Telecommunication Engineering, Faculty of Engineering, KMITL.

A Simple and Economic PWM and ΣΔ Modulator Circuit Based on Modified Source-Couple Oscillator

Panwit Tuwanut, Jeerasuda Koseeyaporn, Paramote Wardkein
Telecommunication Engineering Department, Faculty of Engineering
King Mongkut's Institute of Technology Ladkrabang
Ladkrabang, Bangkok, 10520 Thailand
panwit@telecom.kmitl.ac.th, jeerasuda@telecom.kmitl.ac.th, pramote@telecom.kmitl.ac.th

Abstract

In this article, a simple and economic Pulse Width Modulator (PWM) and Sigma Delta Modulator (ΣΔ) circuit which is based on the modified CMOS source couple voltage-control oscillator is presented. The circuit can work either as PWM or ΣΔ modulator, depending on the condition of the two bias currents which are forced of the source couples. Namely, the circuit is a PWM when these two bias currents are out of phase. Otherwise, it is a ΣΔ modulator when both bias currents are identical. In addition, another feature of the proposed circuit is that the modulated signal can be either in voltage or current format. Moreover, the proposed circuit provides wide range of frequency operation because of few numbers of CMOS in the circuit. Furthermore, the circuit is very suitable for realization in integrated circuits (ICs) form and can be employed for optical communication application. The simulation results of the circuit are demonstrated and agreed well with theoretical anticipation.

1. Introduction

It is well known that modulator circuits have played an essential role in the first order of element of communication systems. One reason is that the spectrum of modulated signal is shifted by modulator to frequency range that is satisfied with frequency characteristic of medium. For pulse modulator (PWM, PPM, PAM and ΣΔ etc.), the PWM and ΣΔ modulators are circuits that have gained much attention and been continuously researched. In the past, these modulator networks were designed by composite circuits which were composed of current source or voltage source, flip-flop, comparator and analog switch [1]. Consequently, the obtained circuits were in large scale, power consumption and work well only in low frequency range.

To alleviate those problems, many researchers had proposed their modulators in a single circuit which they were mostly based on relaxation oscillator. One example of such circuit [2, 3] was composed of Op-Amp, OTA and RC component. Although, this modulator can function either as differentiate PWM or ΣΔ modulator in the same circuit; however, it cannot be operated in high frequency range and is composed of many components.

The goal of this paper is to present a new PWM and ΣΔ modulator based on source-coupled oscillator [4 - 11]. The PWM and ΣΔ operations are determined by the condition of the two bias currents of the source couples. When they are out of phase, the PWM is achieved. Otherwise, the circuit is ΣΔ modulator if both bias currents are identical. The modulated signal can also be either current or voltage signals. The proposed circuit is incorporated with few numbers of CMOS; it thus is suitable for IC realization which results in high frequency range of operation.

In this paper, the principle of the modified source-couple oscillator will be given in section II. For section III, the proposed PWM/ΣΔ modulators are described. In addition, error analysis is demonstrated in section IV. To verify the performance of the proposed circuit, simulation and experimental results are illustrated in section V. Finally, section VI is devoted for conclusions.

2. Principle

The proposed PWM and ΣΔ modulator circuit is based on a modified relaxation oscillator which is constructed by using PMOS and NMOS transistors. The principle of source-coupled oscillator depicted in Fig. 1 is first given in this section.

As shown in Fig. 1, M_3 and M_4 determine threshold voltage V_{TH} for charge and discharge operation of the

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capacitor C, whereas M_1 and M_2 are on-off switches for the current sources M_5 and M_6. Initially, it is assumed that the charged voltage of C is zero. In addition, M_2 and M_3 are on whereas M_1 and M_4 are off. The capacitor C is thus charged by the current I_D. When the voltage across M_2 and M_3 are added up to $2V_{TH}$, M_1 and M_4 are simultaneously on whereas M_2 and M_3 are concurrently off. Consequently, the capacitor C is discharged by the current I_D. When the voltages across M_2 and M_3 reach to $2V_{TH}$, M_1 and M_4 are off and M_2 and M_3 are on once again. These operations are repeated resulting in periodic waveforms as shown in Fig.2.

Based on charge/discharge operation of the capacitor, $\Delta t_1, \Delta t_2$ which are time of charge and discharge are defined by

$$\Delta t_1 = \Delta t_2 = \frac{2CV_{TH}}{I_D}. \quad (1)$$

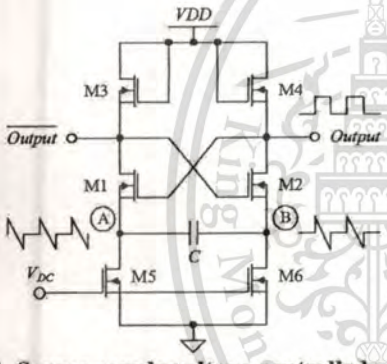

Figure 1. Source couple voltage-controlled oscillator

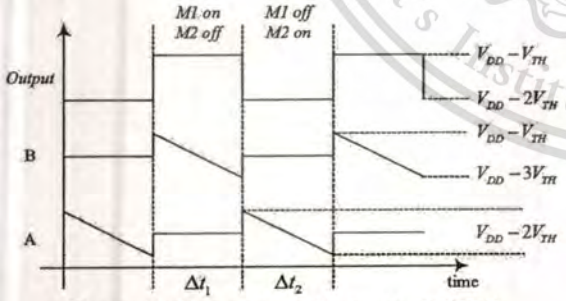

Figure 2. Voltage waveforms for NMOS source- coupled VCO

Due to the symmetrical property of charge/discharge time, the period and frequency of output waveform can thus be determined by

$$T = \frac{4CV_{TH}}{I_D} \quad (2)$$

$$f = \frac{I_D}{4CV_{TH}}. \quad (3)$$

3. PWM and ΣΔ modulator

The PWM and ΣΔ circuit operation is based on the modified source-coupled oscillator which is described in previous section. As earlier mentioned the operation of the circuit to work either as PWM or ΣΔ is determined by the condition of the bias currents to the source-coupled oscillator. For PWM operation, the two bias currents must be out of phase, the PWM circuit is demonstrated in Fig. 3(a) for the modulating signal in voltage mode. Contrarily, when the two bias currents are identical, the circuit thus is ΣΔ modulator where the circuit for is illustrated in Fig, 3(b).

For simplification of analysis, it is assumed that the carrier frequency is much higher than the frequency of modulating signal. The modulating signal is thus approximated to be stable during one period of carrier signal. The resulted charged/discharged time, period and frequency of the modulated PWM/ΣΔ output can thus be respectively determined by the following relationships:

$$\Delta t_1 = \frac{2CV_{TH}}{I_D + I_{in}} \quad (4)$$

$$\Delta t_2 = \frac{2CV_{TH}}{I_D - I_{in}} \quad (5)$$

$$T = \frac{4I_D CV_{TH}}{I_D^2 - I_{in}^2} \quad (6)$$

$$f = \frac{I_D^2 - I_{in}^2}{4I_D CV_{TH}} \quad (7)$$

where I_{in} is an information current's signal. In addition, the duty cycle (D) is given by

$$D\% = \frac{I_D + I_{in}}{2I_D} \times 100\%. \quad (8)$$

4. Error analysis

The error analysis can be archived by considering a slew rate of the circuit. This is because the output voltage does not change instantaneously during the transition from maximum saturated voltage to minimum saturate voltage as shown in Fig. 4. With the slew rate effect, the modulated frequency and duty cycle are respectively found to be

$$f = \frac{1}{\frac{4I_D CV_{TH}}{I_D^2 - I_{in}^2} + \frac{2V_{TH}}{SR}} \quad (9)$$

$$D\% = \left(\frac{I_D + I_{in}}{2I_D} + \frac{I_D^2 - I_{in}^2}{2CI_D SR}\right)\left(1 + \frac{I_D^2 - I_{in}^2}{2CI_D SR}\right)^{-1} \times 100\% \quad (10)$$

where S is defined as a slew rate of the circuit.

5. Simulation and experimental results

To verify that the proposed circuit can work either as PWM or ΣΔ modulator, it thus is simulated by PSPICE program where the level-3 model parameter of the standard 0.5μ MIETEC CMOS technology is employed. The MOS model MbreakN with aspect ratio W/L=50μm/1 μm and MbreakP with aspect ratio W/L =10μm/1μm are employed where the circuit is operated with +5V and C =5pF. Firstly, the circuit is examined to demonstrate the duty cycle and frequency of the PWM output signal versus the DC modulating current variation. The obtained result is shown in Fig. 5 which is found that the duty cycle of the PWM signal is directly proportional to the magnitude of the modulating signal whereas the frequency is reduced relative to magnitude of the modulating signal.

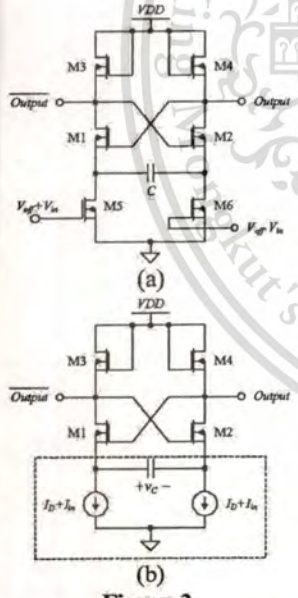

Figure 3.
(a) PWM circuit (voltage mode modulating signal)
(b) ΣΔ circuit (current mode modulating signal)

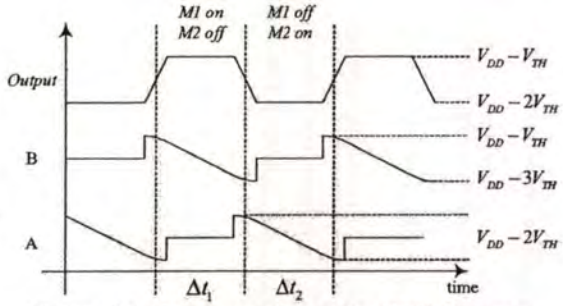

Figure 4. Voltage waveforms for NMOS source-coupled VCO with slew rate effect

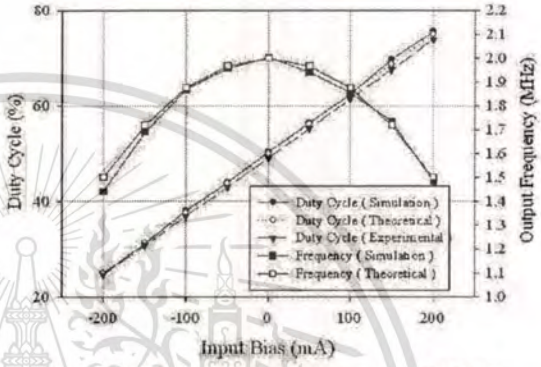

Figure 5. Characteristic of proposed PWM signal generator

In addition, frequency response of the circuit (shown in Fig. 1) is simulated by setting the current I_D at 500μA and varying the capacitor C from 0.1nF to 0.1pF. The magnitude frequency response is depicted in Fig. 6. It is seen that the obtained cut-off frequency is approximately 200MHz.

The proposed circuit is also experimented by using ALD1106 and ALD1107 as NMOS and PMOS, respectively, and the capacitor C is 1nF. The circuit is operated with +5V power supply. The experimental results are depicted in Fig. 7 and Fig. 8, respectively for PWM and ΣΔ outputs.

6. Conclusions

In this paper, a simple and economic PWM and ΣΔ modulator circuit based on the modified source-coupled oscillator is proposed. The main concept is that the two bias currents of source-coupled oscillator are proportional to the modulating input signal. When both bias currents are in phase or out of phase, ΣΔ or PWM modulator are respectively achieved. Due to few

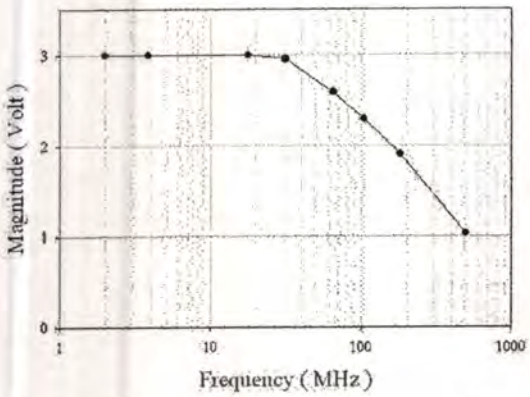

Figure 6. Magnitude frequency response of the proposed circuit

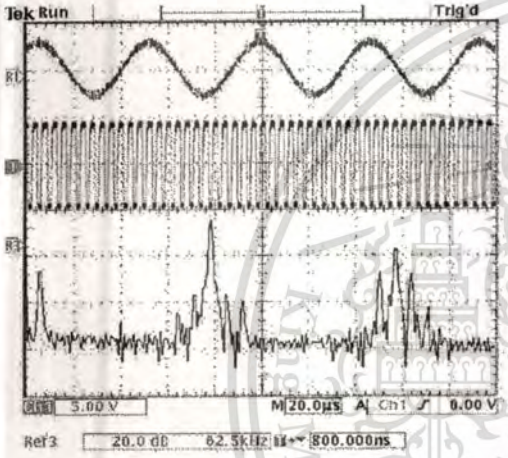

Figure 7. Experimental result of PWM : modulating signal (upper trace), PWM signal (middle trace), and frequency spectrum (lower trace)

transistors employed in the proposed circuit, it is thus economic and suitable for IC realization. The simulation and experimental results demonstrate that the proposed circuit can work as theoretical anticipation.

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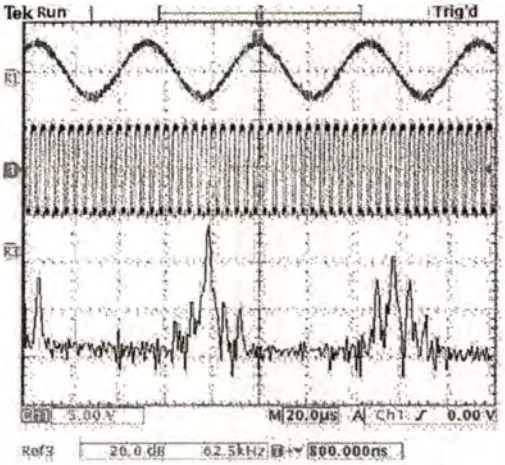

Figure 8. Experimental result of ΣΔ : modulating signal (upper trace), PWM signal (middle trace), and frequency spectrum (lower trace)

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A Novel Monostable Multivibrator Circuit

Panwit Tuwanut, Jeerasuda Koseeyaporn, and Paramote Wardkein
Telecommunication Department, Faculty of Engineering,
King Mongkut's Institute of Technology Ladkrabang, Ladkrabang, Bangkok THAILAND 10520
E-mail: panwit@telecom.kmitl.ac.th

***Abstract*—This article represents a novel monostable multivibrator circuit in which width and height of the pulse output can be independent electronically adjusted. In addition, the pulse width of output is not restricted to be wider or narrower than that of input pulse as conventionally employed. Namely, there is no restriction on the width of input and output pulse, the circuit's implementation is thus more convenient. The proposed circuit is composed of three OTAs, two resistors and one capacitor, basically constructed a simple pulse generator (Schmitt-trigger circuit). Therewith the compactness of the circuit, it is thus suitable to be fabricated for integrated circuit. The results of circuit simulation is accordance well with theoretical analysis.**

***Index Terms*—analog circuit, monostable multivibrator, PPM, PWM.**

I. Introduction

MONOSTABLE multivibrator or one-shot timer is widely used in communication system, such as pulse position modulation, FM demodulation, clock recovery circuit. One of many conventional monostable multivibrator circuits that is typically employed for this purpose is the IC 555. It is composed of voltage comparator, timing resistor, timing capacitor and flip-flop. The basic operation of this circuit is RC series network. With the provided voltage source, the capacitor is charged and discharged where the voltage across capacitor rises and falls exponentially. When the charged voltage reaches an upper threshold level, it results in the changing of the flip-flop's state. The positive output pulse is then generated. The height of output pulse depends on the supply's voltage whereas the pulse width is directly proportional to the RC time constant. However, it is interesting to mention about some disadvantages of the conventional monostable circuits. Firstly, the input pulse width has an effect on the operation of the circuits. Namely, most circuits require the input pulse width to be either wider or narrower than the output pulse width. Secondly, the output pulse height of most circuits cannot be electronically adjusted which is important in some application. Recently, W.-S. Chung et al. proposed a monostable multivibrator in which its output pulse weight and height can be tuned by current [1]. However, this circuit remains the restriction of pulse width between input and output as previously mentioned.

In this paper, a novel monostable multivibrator circuit is presented where its output pulse width and height can be electronically tuned. In addition, the circuit operation does not depend heavily on the input pulse width. In other words, there is no restriction between pulse width of input and output. The proposed circuit scheme is composed of three OTAs, two resistors, and one capacitor. It is seen that the components of this circuit are fewer than that of proposed by [1].

The outline of this paper will be arranged as follows. In section II, the circuit description and operation are discussed where the experimental and simulation results are given in section III. Finally the conclusion is presented in section IV.

II. Circuit Principle

A. Pulse Generator

The proposed circuit has been modified from astable multivibrator circuit [2]-[4] which is shown in Fig.1(a). The operation of this circuit is thus first given. It is assumed that the realization of the circuit is based on CMOS transistors. Basically, the OTA serves as an adjustable resister, which is controlled by bias current (I_B), where the Op-Amp, the capacitor C and the resisters R_1, R_2 construct an inverting Schmitt trigger circuit. Based on periodic charge/discharge operation of the capacitor, the triangular wave $v_C(t)$ and the square wave $v_o(t)$ are then generated as illustrated in Fig. 1 (b) where the oscillated frequency is given by

$$f = \frac{g_m}{4kC} \quad \text{where } k = \frac{R_1}{R_1 + R_2} \,. \tag{1}$$

As shown in Fig. 1.(b), v_{OH} and v_{OL} represent positive and negative saturate voltages of $v_o(t)$, respectively, whereas v_{IH} and v_{IL} are respectively positive and negative threshold voltage of the Op-Amp non-inverting node. The circuit shown in Fig. 1(a) is improved, for temperature-insensitive purpose, the by replacing R_2 with the OTA3 (see Fig. 2.(a)). The oscillated frequency of pulse signal $v_o(t)$ is obtained by

$$f = \frac{1}{4CR_1}\left(\frac{I_{o1}}{I_{o3}}\right). \tag{2}$$

By substituting $I_{o1} = g_{m1} v_o(t)$ and $I_{o3} = g_{m3} v_o(t)$ and $g_{m1} = \sqrt{K\left(W/L\right) I_{B1}}$ and $g_{m3} = \sqrt{K\left(W/L\right) I_{B3}}$, $K = \mu_n C_{ox}$ into (2), it thus results in

$$f = \frac{1}{4CR_1}\sqrt{\frac{I_{B1}}{I_{B3}}}. \quad (3)$$

Equation (3) indicates that the oscillated frequency can be electronically adjusted with the bias currents I_{B1} and/or I_{B3}.

To gain the ability of electrical amplitude control, the circuit given in Fig. 2.(a) is further modified by replacing the Op-Amp with the OTA2 and a resister R_O as shown in Fig. 2.(b). When the OTA2 is in saturation mode, the peak-to-peak amplitude of output signal is given by

$$v_o(t)_{pp} = 2I_{B2}R_O \quad (4)$$

implying that the amplitude can be electronically adjusted by the bias current I_{B2}.

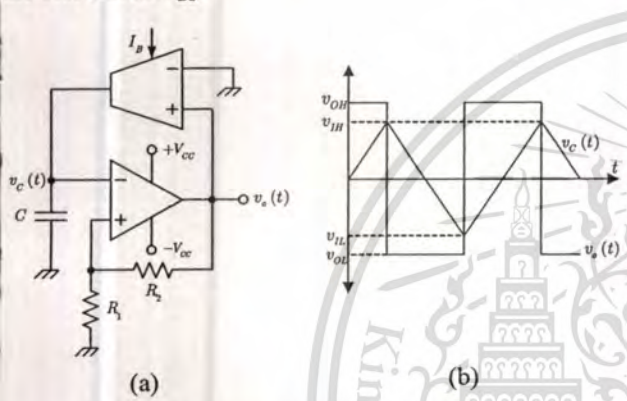


Fig. 1(a). Basic pulse generator circuit (b). Circuit's signal.

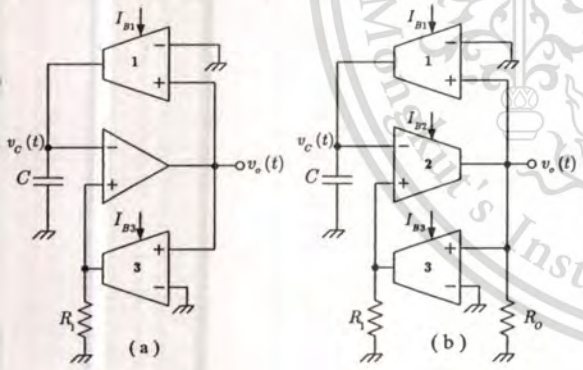


Fig. 2. An improvement pulse generator circuit.
(a). Improved for temperature-insensitive
(b). Improved for both temperature-insensitive and amplitude controllable.

B. *Monostable Multivibrator*

Based on the circuit illustrated in Fig. 2.(b), it is applied for a proposed monostable multivibrator. The input signal $v_{in}(t)$ is fed into the negative node of the OTA3 where a switch is put parallel with a capacitor at the negative node of the OTA2 to control voltage as depicted in Fig. 3.

At the initial state, $v_{in}(t)$ is firstly grounded. It causes the output voltage $v_o(t)$ to be $+I_{B2}R_0$ and closes the switch to ground. Let us consider the OTA3, $v_X(t)$ is equal to $+I_{B3}R_1$. When the positive rising edge of the input signal is presented and its maximum voltage level is greater than $v_O(t)$, $v_X(t)$ then changes to negative saturate voltage $-I_{B3}R_1$ causing $v_O(t)$ converts to negative saturate voltage $-I_{B2}R_0$. With the negative voltage level of $v_O(t)$, the switch is in open state, resulting in discharging process of C by I_{B1}. The voltage across C, $v_C(t)$ is thus linearly decreased. When $v_C(t)$ reaches to a voltage level that is less than $-I_{B3}R_1$, $v_O(t)$ and $v_X(t)$ are again converted to positive voltage $+I_{B2}R_0$ and $+I_{B3}R_1$, respectively, whereas the switch is closed. The described circuit operation is illustrated by the timing diagram given in Fig. 4. The output pulse width of the proposed circuit is

$$T = CR_1\sqrt{\frac{I_{B3}}{I_{B1}}} \quad (5)$$

where its height is defined by

$$v_o(t)_{pp} = 2I_{B2}R_O. \quad (6)$$

Both (5) and (6) expresses that the pulse's width and height of this circuit are electronically tunable which are adjusted by the bias current I_{B1} and/or I_{B3} and I_{B2}, respectively.

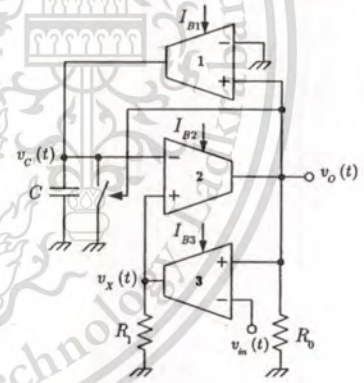


Fig 3. A monostable multivibrator.

As can be seen, the advantage of the proposed scheme is focused on the ability of electronically control. However, the circuit shown in Fig. 3. has the limitation in input pulse width. Namely, the pulse width of input signal must be shorter than the output signal. To eliminate this restriction, the circuit in Fig. 3. is further modified by adding AND gate and an inverter as shown in Fig. 5. The timing diagram of the modified circuit's operation is demonstrated in Fig. 6.

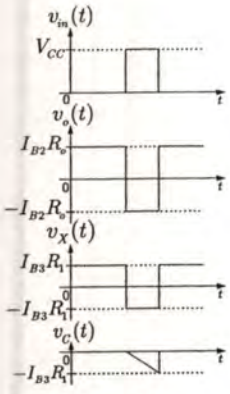


Fig. 4. Timing Diagram.

Let us consider the case that the pulse width of $v_{in}(t)$ is wider than the $v_o(t)$. It is assumed that $v_{in}(t)$ is grounded at the initial state, $v_o(t)$ is thus a positive saturate at $+I_{B2}R_0$, causing the switch is closed. When the positive edge of the input is present the AND output $\hat{v}_{in}(t)$, which is the AND operation between $v_{in}(t)$ and the inverse of output signal $v_o(t)$, behaves as an input signal.

Whereas $\hat{v}_{in}(t)$ is greater than $v_O(t)$, the output signal of the OTA3 $v_X(t)$ changes to its negative saturate voltage $-I_{B3}R_1$. At the same tine, $v_O(t)$ also converts to its negative saturate voltage $-I_{B2}R_0$. Therefore, the switch is open. The capacitor C is thus linearly charged by I_{B1}. Until $v_C(t)$ reaches to a threshold level $-I_{B3}R_1$, $v_O(t)$ is again converted to its positive voltage $+I_{B2}R_0$. In despite of a high status of $v_{in}(t)$, it has no effect on the circuit's operation. This is because $\hat{v}_{in}(t)$ is in ground level, causing a positive saturate level of $v_X(t)$ and the switch in close operation. It is thus seen that the pulse width of input signal has no effect on the output's pulse width.

III. Simulation Results

The CMOS level [5] of the proposed circuit (shown in Fig. 5.) is depicted in Fig. 7. It is designed by using a level-3 model parameter of the standard 0.5μ MIETEC CMOS technology. The circuit is simulated using PSPICE where the aspect ratio of transistors is demonstrated in Table I. In addition, the following circuit's parameters are employed $R_1 = R_2 = 2k\Omega$, $C = 0.05\mu F$, $V_{CC} = 3V$, $I_{B2} = 1mA$ $I_{B3} = 0.5mA$, and $I_{B3} = 1mA$.

Firstly, the case of the input pulse width is greater than that of the output signal is examined. The simulation result is depicted in Fig. 8(a). where the upper trace is $v_{in}(t)$, the middle trace is $v_C(t)$, and the lower trace is $v_o(t)$. Similarly, Fig. 8(b) shows the simulation result when pulse width of the input signal is greater than pulse width's the output signal.

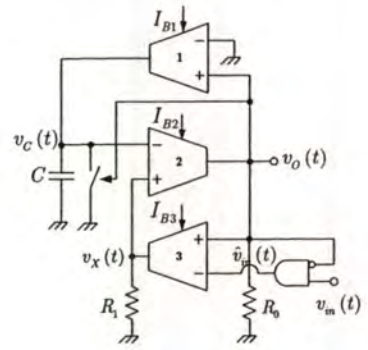


Fig 5. A modified monostable multivibrator.

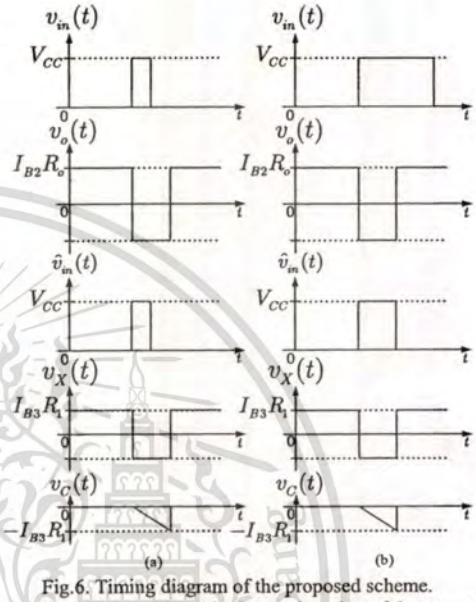


Fig.6. Timing diagram of the proposed scheme.
(a) pulse width's the input signal is shorter than that of the output signal.
(b) pulse width's the input signal is longer than that of the output signal.

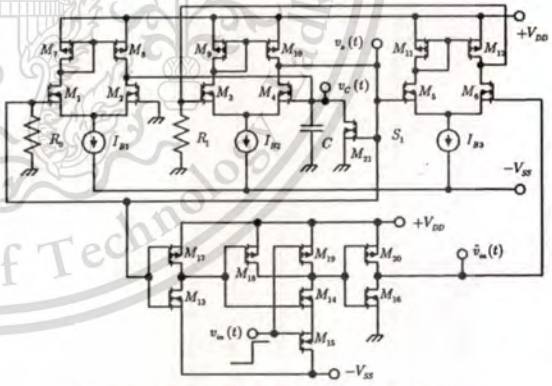
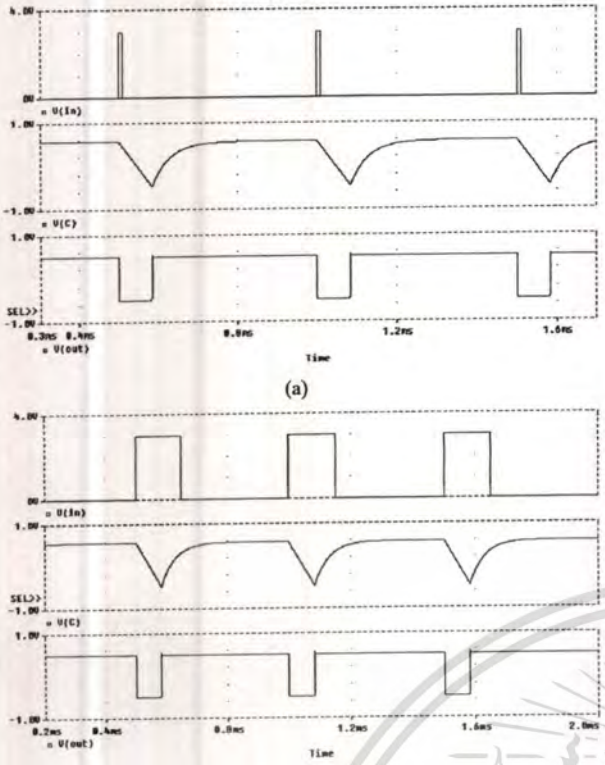


Fig 7. The CMOS level of the proposed scheme.

Table I. Dimension of transistors employed in the proposed circuit.

MOS	W (μM)	L (μM)	MOS	W (μM)	L (μM)
$M_1 - M_6$	126	1	$M_{14} - M_{16}$	20	1
$M_7 - M_{12}$	116	1	$M_{17} - M_{20}$	100	1
M_{13}	10	1	M_{21}	400	1



(a)

(b)

Fig. 8. Simulation result of the proposed scheme
(a) pulse width's input signal is shorter than output signal.
(b) pulse width's input signal is longer than output signal.

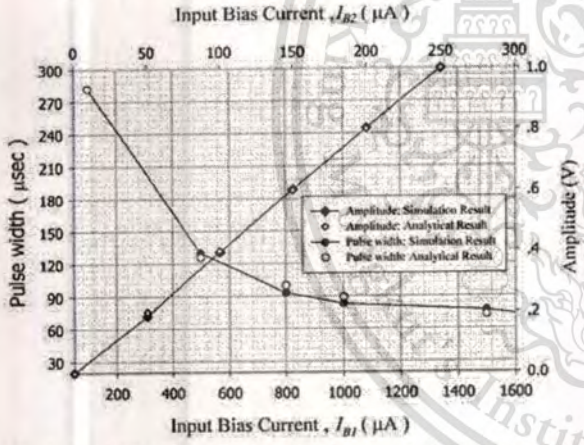


Fig. 9. Pulse width and amplitude tuning by current of the proposed circuit.

Next, the ability of electronically amplitude control and pulse width control is demonstrated in Fig. 9. For pulse width adjustment, $I_{B2} = 0.1mA, I_{B3} = 0.2mA$ are employed whereas I_{B1} is varied as shown on the x-axis. For amplitude adjustment, I_{B2} is instead varied as shown on the x-axis whereas $I_{B1} = 0.2mA, I_{B3} = 0.2mA$ are set.

IV. Conclusion

The novel monostable multivibrator is presented in this paper. The main advantage of this proposed scheme is that there is no restriction on the input's pulse width. Namely, it can be either greater or less than that of the output's pulse width. The operation of this scheme only depends on the positive edge of the input signal. Furthermore, the pulse width and height can be independently adjusted by currents. In addition, the proposed circuit can be applied for PWM, PPM, DM circuits. With the compactness of the circuit structure, the proposed scheme is suitable to be fabricated in the integrated circuit technology.

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A Novel Versatile Modulator Circuit

Panwit Tuwanut, Jeerasuda Koseeyaporn, Paramote Wardkein †
Telecommunication Department, Faculty of Engineering
King Mongkut's Institues of Technology Ladkrabang
Bangkok, Thailand 10520
E-mail: panwit@telecom.kmitl.ac.th, jeerasuda@telecom.kmitl.ac.th, pramote@telecom.kmitl.ac.th

Abstract— **In this paper, a novel versatile modulator that can function either as delta modulator, sigma-delta modulator, amplitude modulator and frequency modulator is proposed. The principle of the proposed scheme is based on schmitt-trigger circuit and composed of a few components : three OTAs, one capacitor and two resistors. The advantage of this circuit is that the clock (carrier) signal employed for modulation is inherent in the circuit. The modulating signal is therefore an external input requirement. Based on the compactness of the circuit, it is suitable for IC realization. The computer simulation demonstrates the results which agree well with the theoretical analysis.**

Keywords: **Modulator, sigma delta, delta, AM, FM**

I. INTRODUCTION

In communication system, there are various techniques for modulation such as AM, FM, PM (analog modulation), PCM, PWM, DM (digital modulation). Digital signal is well known to be superior to analog signal in noise immunity. For construct digital signal, a basic technique in digital modulation is pulse code modulation (PCM). However, it has one major disadantage in data redundancy. To reduce this problem, the difference signal between a current sample and a predictive of next sample has been instead encoded. Such technique is well known as differential pulse code modulation (DPCM).

For a special case of DPCM which provides one-bit encoding output, it is known as delta modulation (DM). To improve the performance of this technique, it is further developed to be sigma-delta modulator. Sigma-delta modulation is nowadays widely used in telecommunication system, digital signal processing and power system. Many researches [1]-[4] are mostly focused on the construction of sigma-delta modulation circuit such as using switch capacitor or MOS structure. However, the requirement of clock signal is the main limitation of these researches.

In this paper, a novel versatile modulator circuit is proposed. Based on this circuit, it can operate either as sigma-delta modulator, delta modulator, amplitude modulator, or frequency modulator, depending on node of feeding information signal. The proposed circuit is composed of a few components which are three OTAs, two resistors and one capacitor. These components basically forms a Schmitt trigger circuit. Based on this simple pulse generator, its amplitude and frequency characteristics can be electronically adjusted. With the ability of amplitude control and frequency control in electrical, the circuit thus can applied for amplitude modulation and frequency modulation, respectively. In addition, without an additional device requirement, the proposed circuit can also function as a sigma-delta modulator or a delta modulator depending on node of feeding information in the circuit.

The outline of this paper will be arranged as follows. In section II, the circuit's principles are discussed where the simulation results are provided in section III. Finally the conclusion is given in section IV.

II. PRINCIPLES

A. Pulse Generator

The proposed circuit has been modified from astable multivibrator circuit [1],[5]-[7] which is shown in Fig.1(a). The operation of this circuit is thus first given. It is assumed that the realization of the circuit is based on CMOS transistors. Basically, the OTA serves as an adjustable resister, which is controlled by bias current (I_B), where the Op-Amp, the capacitor C and the resisters R_1, R_2 construct an inverting Schmitt trigger circuit. Based on periodically charged/discharged operation of the capacitor, the triangular wave $v_C(t)$ and the square wave $v_o(t)$ are then generated as illustrated in Fig. 1(b) where the oscillated frequency is given by

$$f = \frac{g_m}{4kC} \quad \text{where } k = \frac{R_1}{R_1 + R_2} . \qquad (1)$$

As shown in Fig. 1.(b), v_{OH} and v_{OL} represent positive and negative saturate voltages of $v_o(t)$, respectively, whereas v_{IH} and v_{IL} are respectively positive and negative threshold voltage of the Op-Amp non-inverting node. Later, the circuit shown in Fig. 1(a) is improved, for temperature-insensitive purpose, by replacing R_2 with the OTA3 (see Fig. 2.(a)). The oscillated frequency of pulse signal $v_o(t)$ is obtained by

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$$f = \frac{1}{4CR_1}\sqrt{\frac{I_{o1}}{I_{o3}}} \qquad (2)$$

By substituting $I_{o1} = g_{m1}v_o(t)$, $I_{o3} = g_{m3}v_o(t)$, $g_{m1} = \sqrt{K\left(W/L\right)I_{B1}}$, and $g_{m3} = \sqrt{K\left(W/L\right)I_{B3}}$, and $K = m_n C_{ox}$ into (2), it thus results in

$$f = \frac{1}{4CR_1}\sqrt{\frac{I_{B1}}{I_{B3}}}. \qquad (3)$$

Equation (3) indicates that the oscillated frequency can be electronically adjusted by the bias currents I_{B1} and/or I_{B3}. To gain the ability of electrical amplitude control, the circuit given in Fig. 2.(a) is further modified by replacing the Op-Amp with the OTA2 and a resister R_O as shown in Fig. 2.(b). When the OTA2 is in saturation mode, the peak-to-peak amplitude of output signal is given by

$$v_{o_{p-p}}(t) = 2I_{B2}R_O \qquad (4)$$

implying that the amplitude can be electronically adjusted by the bias current I_{B2}.

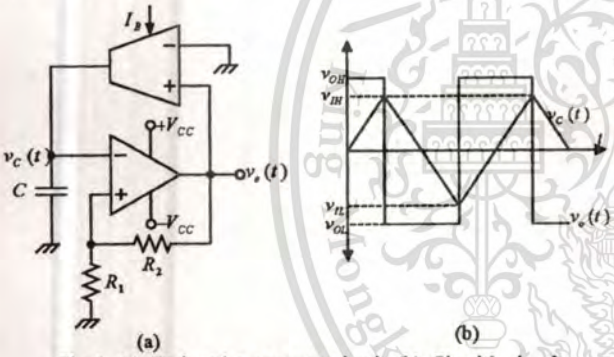


Fig. 1. (a). Basic pulse generator circuit (b). Circuit's signal.

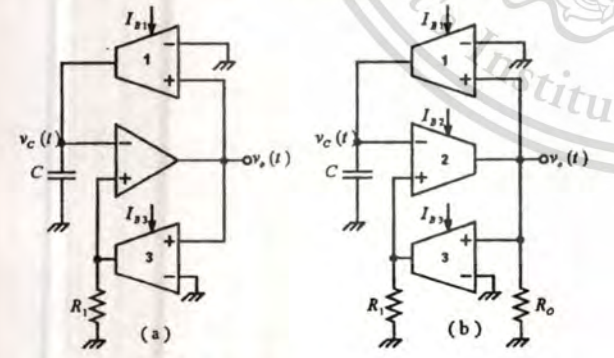


Fig. 2. An improvement pulse generator circuit.
(a). Improved for temperature-insensitive
(b). Improved for both temperature-insensitive and amplitude controllable.

B. Frequency Modulator and Amplitude Modulator

As previously described, it is seen that the developed circuit given in Fig. 2(b) has advantages in frequency/amplitude adjustment which are confirmed by (3) and (4), respectively. Based on the characteristic of electrical frequency-control, when either I_{B1} or I_{B3} functions as an information signal the circuit thus can be applied for frequency modulator. Similarly, as can be seen from (4), when I_{B2} functions as an information signal it can then be operated as amplitude modulator.

C. Sigma-delta Modulator

With the circuit depicted in Fig. 2(b), it can be applied for a sigma-delta modulator as illustrated in Fig. 3. The non-inverting of the OTA1 is connected with the input signal rather than connected to ground.

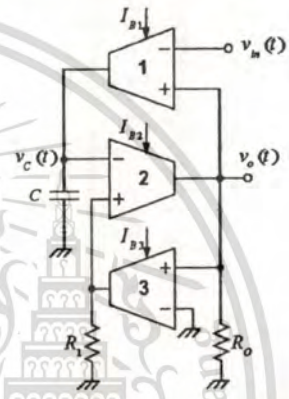


Fig. 3. The proposed circuit for sigma-delta modulator circuit.

From the generated signals $v_C(t)$ and $v_o(t)$ illustrated in Fig. 1.(b), it is seen that the capacitor and the OTA1 functions as an integrator. Hence, when $v_{in}(t)$ is present, the difference between the input signal $v_{in}(t)$ and the output signal $v_o(t)$ is thus integrated to be $v_C(t)$. When $v_C(t)$ is compared with the threshold voltages v_{OH} or v_{OL}, it results in $v_o(t)$ which obviously is a sigma-delta modulator output.

D. Delta modulator circuit

For this application, the feeding point of the input signal is changed as depicted in Fig. 4. When the input signal $v_{in}(t)$ is present, it is compared with $v_C(t)$. The difference signal $v_{in}(t)$- $v_C(t)$ is then compared with the threshold voltages v_{OH} or v_{OL} resulting in a delta modulator output.

III. Simulation Results

In this section, the proposed circuit is simulated by PSPICE where the level-3 model parameter of the standard 0.5μ MIETEC CMOS technology [8] is employed as depicted in Fig. 5. The MOS Model MbreakN with W/L=126μm/1μm and MbreakP with W/L = 116μm/1μm are employed where the circuit is operated with ±3V and circuit's element are $R_1, R_2 = 2kW, C = 0.01mF$. Firstly, this circuit is experimented to demonstrate the ability of electronically amplitude and frequency control. It can be accomplished by putting the feeding point for $v_{in}(t)$ shown in Fig. 5. to circuit's ground. The result is given in Fig. 6 where y-axis on left- handed side and right-handed side are respectively for frequency and amplitude. For frequency adjustment, $I_{B2} = 0.1mA, I_{B3} = 0.2mA$ are employed whereas I_{B1} is varied as shown on the x-axis (bottom). For amplitude adjustment, I_{B2} is instead varied as shown on the x-axis (top) whereas $I_{B1} = 0.2mA, I_{B3} = 0.2mA$ are set.

Later, $I_{B2} = 0.1mA, I_{B3} = 0.2mA$ are fixed and with electrical frequency-control ability of the circuit, it can then be operated as frequency modulator. When input signal is fed to the bias input node of the OTA1, namely, $I_{B1}(t) = I_{in}(t)$. The frequency of output signal is thus directly proportional to bias current of the OTA1. For this case, 1kHz frequency, 100μAp-p amplitude and 200μA offset sinusoidal modulating input signal is fed to the circuit, the frequency modulation result is shown in Fig. 7.

Based on the characteristic of electrical amplitude-control, the circuit can thus be applied for amplitude modulator. Let $I_{B1} = I_{B3} = 0.2mA$ be fixed when input signal is fed to the bias input node of the OTA2, namely, $I_{B2}(t) = I_{in}(t)$. The magnitude of output signal is therefore directly proportion to bias current of the OTA2. When 1kHz frequency, 40μAp-p amplitude and 100μA offset sinusoidal modulating input is employed, it results in the amplitude modulation output as given in Fig. 8.

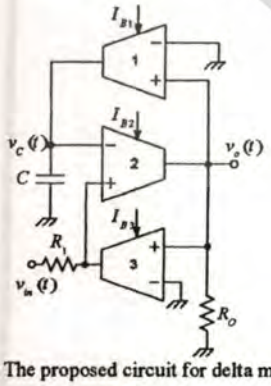


Fig. 4. The proposed circuit for delta modulator.

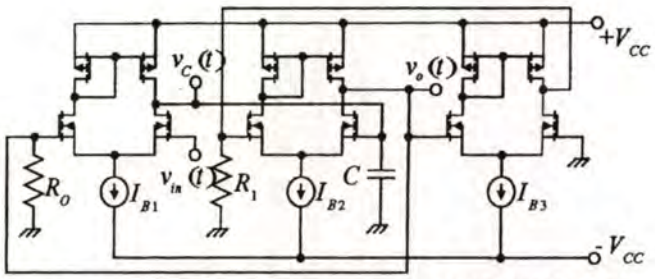


Fig. 5. The proposed circuit based on the standard 0.5μ MIETEC CMOS technology.

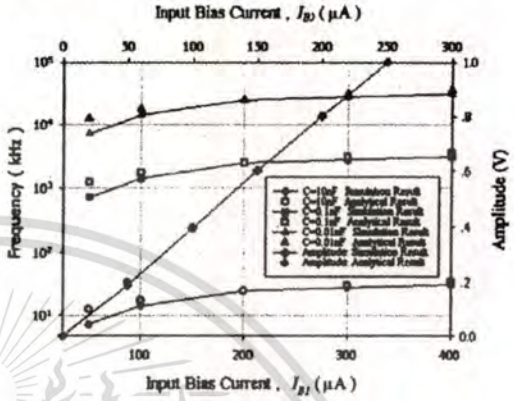


Fig. 6. Electronically control of frequency and amplitude of the proposed circuit.

From the circuit shown in Fig. 5., by setting $v_{in}(t) = 0.2V_{p-p}\sin(2000pt)$ shown in the upper trace of Fig. 9., the output pulse is depicted in the middle trace of Fig. 9. When this output signal is passed to a lowpass filter, the recovered input signal is given in the bottom trace of Fig. 9. It is confirmed that the resulted output is sigma-delta modulation signal.

Similarly for delta modulation, without adding any component, the feeding point of input signal is now changed to at resistor R_1. In this case, a triangular modulating signal with 1Vp-p amplitude and 1kHz frequency is employed where the output signal is given in the middle trace of Fig. 10. When this output signal is passed to a lowpass filter, the filter output signal is shown in the bottom trace of Fig. 10. It is seen that the filter output is the derivative version of the input signal. It thus confirms that the circuit cans functions as a delta modulator.

IV. Conclusions

A simple versatile modulator for delta modulator, sigma-delta modulator, amplitude modulator and frequency modulator has been presented in this work. The advantage of the proposed scheme is that the clock or carrier used for modulation is inherent in the circuit, the modulating signal is thus only an external input needed. The simulation

results illustrate that without an additional device requirement, the proposed circuit can be function either as various modulators by feeding input signal at different nodes in the circuit. In addition, with a simple construction of the proposed circuit, it is suitable for realize in integrated circuit technology.

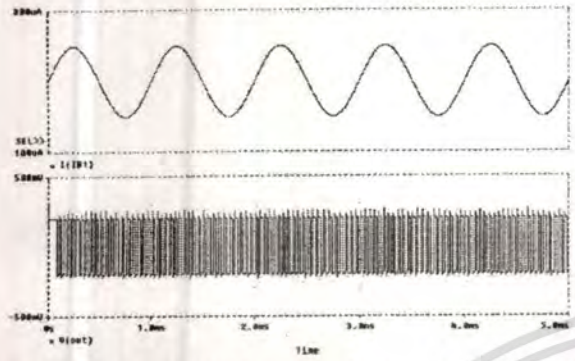


Fig. 7. Frequency modulation result where upper trace is sinusoidal modulating signal (1 kHz frequency, 50μA amplitude, 200μA offset) and the lower trace is a square wave FM signal modulation output.

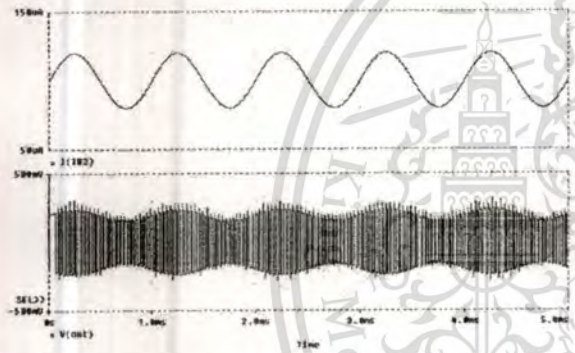


Fig. 8. Amplitude modulation result where upper trace is sinusoidal modulating signal (1 kHz frequency, 20μA amplitude, 100μA offset) and the lower trace is a square wave AM signal modulation output.

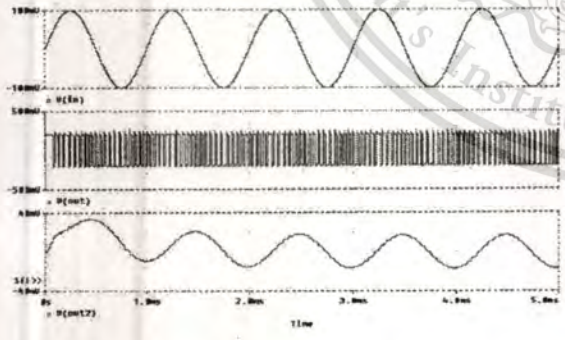
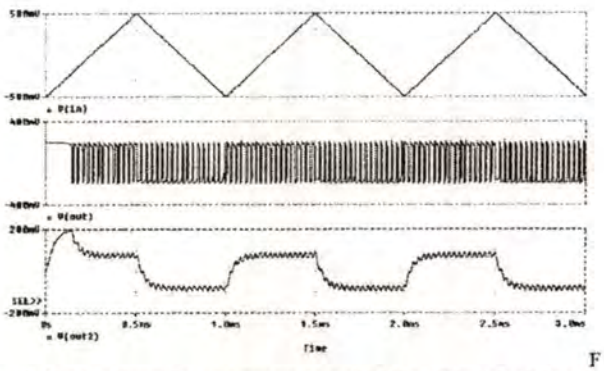


Fig. 9. Simulation results where upper trace is 1kHz, 0.2Vp-p sinusoidal modulating signal, the middle trace is a sigma-delta modulation output and the lower trace is a lowpass filter output signal.



ig. 10. Simulation results where upper trace is 1kHz, 1Vp-p triangular modulating signal, the middle trace is a delta modulation output and the lower trace is a lowpass filter output signal.

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A Simple Circuit for Sigma-Delta /Delta Modulation

Panwit Tuwanut, Thongchai Maneechukate, Jeerasuda Koseeyaporn , Paramote Wardkein
Telecommunication Department, Faculty of Engineering
King Mongkut's Institute of Technology Ladkrabang
Bangkok, Thailand 10520
panwit@telecom.kmitl.ac.th, thongchaidum@yahoo.com, jeerasuda@telecom.kmitl.ac.th, pramote@telecom.kmitl.ac.th

Abstract— **This article represents a simple circuit which can function either as sigma-delta or delta modulation. The circuit is composed of three OTAs, a capacitor and two resistors which basically form Schmitt-trigger circuit. When input signal is present and fed to the inverting input node of OTA1, the circuit acts as a sigma-delta modulation. Contrarily, without adding any component, the same circuit functions as delta modulation when input signal is instead fed to a resister R_1 node. In addition, frequency and amplitude of the modulated signal not only are independently adjusted but also these characteristics are electrical tuned. Based on the compactness of the proposed circuit, it is therefore suitable for IC realization. The computer simulation results are illustrated to confirm with the given circuit analysis.**

I. Introduction

In communication system, digital signal is well-known to be useful for noise immunity. Pulse code modulation (PCM) is a technique used to construct digital signal where analog input samples are quantized and encoded to *n*-bit digital output. Due to data redundancy problem of PCM signal, the difference between current sample and predicted version is instead encoded, which is well-known as differential pulse code modulation (DPCM). The simplest system of DPCM which provides one-bit output is called delta modulation, DM. The DM system is shown in Fig. 1.

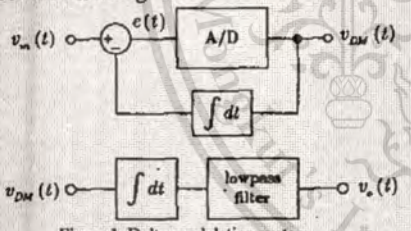

Figure 1. Delta modulation system.

As can be seen in Fig. 1, the delta modulation output is found to be a differentiated version of the input signal. The integrator is therefore needed for demodulation [1]. Hence to omit the integrator in the demodulator, the input signal must be integrated in the modulator. An addition integrator is thus needed. However, since integration is a linear function i.e., $e(t) = \int v_m(t)dt - \int v_{DM}(t)dt = \int (v_m(t) - v_{DM}(t))dt$, a single integrator is only required in the modulator which results in a well-known sigma-delta modulation system as depicted in Fig. 2.

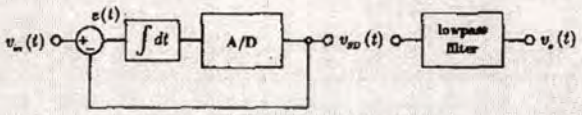

Figure 2. Sigma-delta modulation system.

Sigma-delta modulation is nowadays widely used in telecommunication system, digital signal processing and power system. Many researches are mostly focused on the construction of sigma-delta modulation circuit such as using switch capacitor [2,3] or MOS structure [4]. The main limitation of these works is that the clock signal is an additional input which is required for generating the sigma-delta modulation signal.

In this paper, a simple sigma-delta/delta modulator circuit is presented. The circuit scheme is composed of three OTAs, one capacitor and two resistors which fundamentally generates a clock signal. Without an additional device requirement, the proposed scheme acts as a sigma-delta modulator when an information signal is given at an inverting input of the OTA1. In addition, the circuit functions as a delta modulator when the input is provided at a resister node. Moreover, it is not only that the clock signal is inherent in the proposed circuit but also its frequency and amplitude can be independently controlled by electronic tuning.

The outline of this paper will be arranged as follow. In section II, the circuit description and operation are discussed where the experimental and simulation results are treated in section III. Finally the conclusion is presented in section IV.

II. Principle

A. *Pulse generator*

The proposed scheme has developed from a basic circuit shown in Fig.3(a). Let us consider when the input signal $v_m(t)$ of this circuit is grounded. Basically, the OTA1 serves as an adjustable resister, which is controlled by bias current (I_{B1}), where the Op-Amp, the capacitor C and the resisters R_0, R_1 construct an inverting Schmitt trigger circuit. Based on periodic charge/discharge operation of the capacitor, the triangular wave $v_C(t)$ and the square wave $v_o(t)$ are then generated as illustrated in Fig. 3(b) where the oscillated frequency is given by

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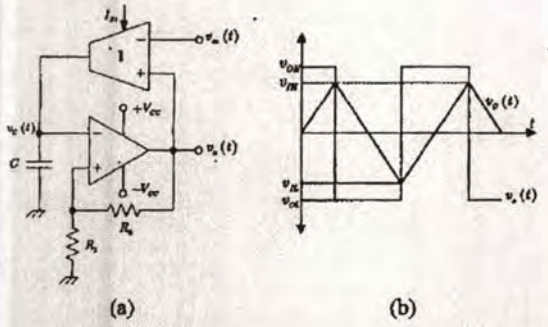


(a) (b)

Figure 3 (a). Basic sigma-delta modulator circuit.
(b). Circuit's signal when $v_{in}(t)$ is grounded.

$$f = \frac{I_B}{8kCV_T} \quad \text{where } k = \frac{R_1}{R_1 + R_0} . \tag{1}$$

As shown in Fig. 3(b), v_{OH} and v_{OL} represent positive and negative saturate voltages of $v_o(t)$, respectively, whereas v_{TH} and v_{TL} are respectively positive and negative threshold voltage of the Op-Amp non-inverting node.

B. Sigma-delta modulator circuit

From the generated signals $v_C(t)$ and $v_o(t)$, it is seen that the capacitor and the OTA shown in Fig. 3(a) functions as an integrator. Hence, when $v_{in}(t)$ is present, the difference between the input signal $v_{in}(t)$ and the output signal $v_o(t)$ is integrated and compared with the threshold voltages v_{OH} and v_{OL}. The $v_o(t)$ signal is therefore a sigma-delta modulator output.

In this case, it is noted that when $v_{in}(t)$ is present, the oscillated frequency is deviated from (1) which is approximately given by

$$f' = \frac{I_B}{8kCV_T}(1 - \mu) \tag{2}$$

where $\mu = \left(v_{in}/V_{CC}\right)^2$ is defined to be a sigma-delta modulation index of the circuit and confined in the range $0 \le \mu < 1$. It should be mentioned that the deviation of the fundamental frequency, however, has no affect on the proposed circuit for the application of modulation. Certainly, it causes synchronization problem in the demodulator if this circuit is applied for A/D converter.

The circuit shown in Fig. 3(a) is improved, for temperature-insensitive purpose, the by replacing R_0 with the OTA3 (see Fig. 4(a)). For $v_{in}(t) = 0$, the oscillated frequency of pulse signal $v_o(t)$ is obtained by

$$f = \frac{1}{4CR_1}\left(\frac{I_{o1}}{I_{o3}}\right). \tag{3}$$

Since $I_{o1} = g_{m1}v_o(t)$ and $I_{o3} = g_{m3}v_o(t)$ and $g_{m1} = I_{B1}/2V_T$ and $g_{m3} = I_{B3}/2V_T$, it then yields

$$f = \frac{1}{4CR_1}\left(\frac{I_{B1}}{I_{B3}}\right). \tag{4}$$

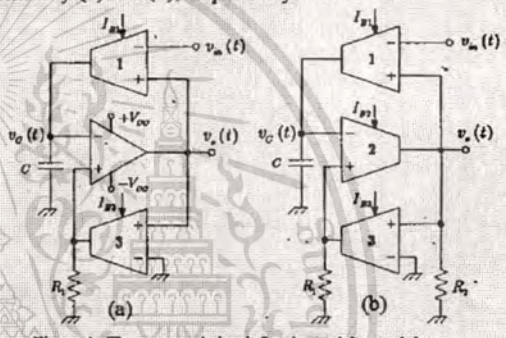
Equation (4) shows that the oscillated frequency is independent on OTA transconductance gain, implying not only that frequency is temperature-insensitive but also can be electronically adjusted with the bias currents I_{B1} and/or I_{B3}.

To gain the ability of electrical amplitude control, the circuit given in Fig. 4(a) is further modified by replacing the Op-Amp with the OTA2 and a resister R_2 as shown in Fig. 4(b). When the OTA2 is in saturation mode, the peak-to-peak amplitude of output signal is

$$v_o(t)_{pp} = 2I_{B2}R_2 \tag{5}$$

which implies that the amplitude can be electronically adjusted by the bias current I_{B2}.

As previously described, it is seen that the developed circuit given in Fig. 4(b) has advantages in both temperature-insensitive and amplitude/frequency adjustment which are confirmed by (4) and (5), respectively.



(a) (b)

Figure 4. The proposed circuit for sigma-delta modulator.
(a). Improved for temperature-insensitive
(b). Improved for both temperature-insensitive and controllable amplitude.

C. Delta modulator circuit

Additionally, the improved circuit depicted in Fig. 4(b) can be applied for a delta modulator. For this application, the feeding point of the input signal is changed (see Fig. 5). In this case, the capacitor and the OTA1 (serves as an adjustable resister) function as the integrator, thus $v_C(t) = \int v_o(t)dt$. When the input signal $v_{in}(t)$ is present, it is compared with $v_O(t)$ and the pulse output signal is therefore generated. Hence, this operation confirms that this circuit is a delta modulator. Due to limited space, only the result of this application will be given in the following section where the circuit analysis is not mentioned in details.

III. Simulation Results

As described in section II, it has been shown that the proposed circuit can be either sigma-delta or delta modulator. In this section, the proposed circuit depicted in Fig. 4(b) and Fig. 5 are thus simulated by computer program to examine the

proposed circuit's operation for sigma-delta modulator and delta modulator, respectively.

A. PSPICE simulation

The proposed circuit is simulated by PSPICE. Fig. 6 demonstrates the sigma-delta modulator which is designed by using a level-3 model parameter of the standard 0.5μ MIETEC CMOS technology. The MOS model MbreakN and MbreakP with W/L = 126μm/1μm and 116μm/1μm, respectively are employed where the circuit's elements are $R_1, R_2 = 2k\Omega, C = 0.01\mu F, V_{CC} = 3V$. Firstly, this circuit is experimented to demonstrate the ability of electronically amplitude and frequency control. It can be accomplished by putting the feeding point for $v_{in}(t)$ shown in Fig. 6 to circuit's ground. The result is given in Fig. 7 where y-axis on left-handed side and right-handed side are respectively for frequency and amplitude. For frequency adjustment, $I_{B2} = 0.1mA, I_{B3} = 0.2mA$ are employed whereas I_{B1} is varied as shown on the x-axis (bottom). For amplitude adjustment, I_{B2} is instead varied as shown on the x-axis (top) whereas $I_{B1} = 0.2mA, I_{B3} = 0.2mA$ are set.

Later, $I_{B1} = 0.2mA, I_{B2} = 0.1mA, I_{B3} = 0.2mA$ are fixed providing an inherent 25kHz clock signal. When 1kHz, 0.2Vpp sinusoidal signal $v_{in}(t)$ is employed, yielding $\mu = 0.0044$, the sigma-delta modulator output is then generated as shown in the middle trace of Fig. 8. To retrieve the input signal, the sigma-delta modulator output is passed through lowpass filter where the result is given in lower trace of Fig. 8. Additionally, the frequency spectrum of the sigma-delta modulation output is computed by using MATLAB 65,536-point FFT which is shown in Fig. 9.

Furthermore, to measure the proposed circuit's performance, SNRD(dB) versus input level(dBr) [6] is the value of the interest. It is noted that SNRD is defined to be SNR plus THD in baseband (0-10kHz) and 0dBr is defined as full swing of 0.2mVpp input signal. As shown in Fig. 10, it is SNRD(dB) versus input level(dBr) for the output bit stream of 0dBr, 1kHz sinusoidal input where the slope implies sensitivity of the circuit which is approximately 1.76.

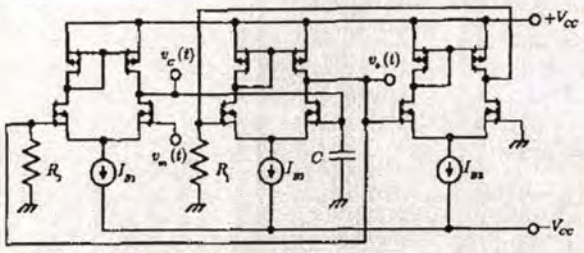


Figure 6. The proposed circuit based on the standard 0.5 micron MIETEC CMOS technology.

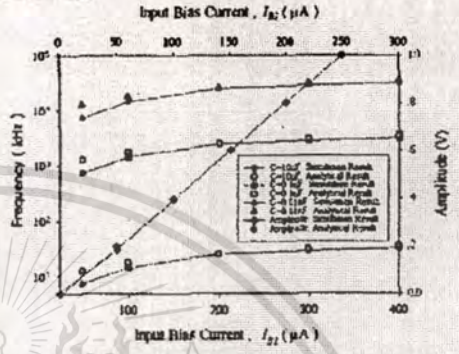


Figure7. Frequency and amplitude tuning of the circuit.

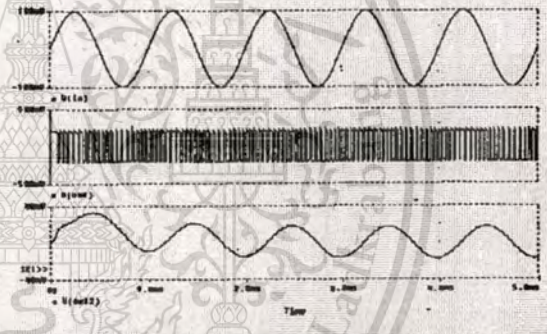


Figure 8. The simulation results where the upper trace is 1kHz, 1Vpp sinusoidal modulating signal, the middle trace is sigma-delta modulation output and the lower trace is lowpass filter output

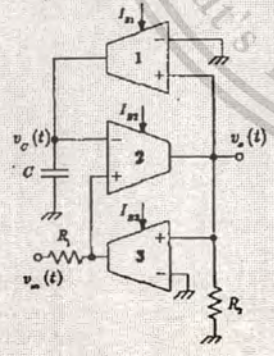


Figure 5. The proposed circuit for delta modulator.

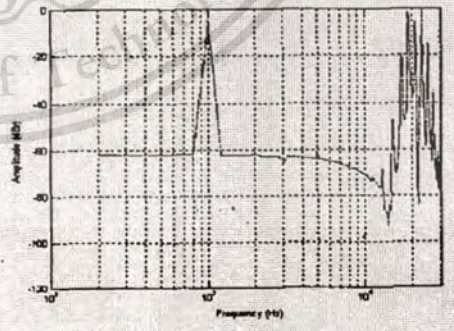


Figure 9. The frequency spectrum of the sigma-delta modulation output.

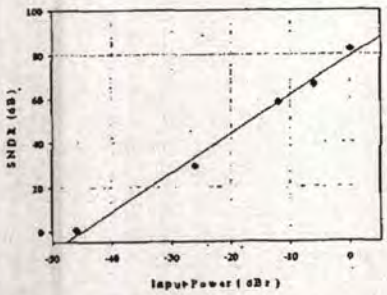


Figure 10. SNDR(dB) versus input level(dBr) for 1kHz sine wave.

For delta modulator application, the feeding point of the input signal is changed (referred to as Fig. 5). In this case, the 1kHz, 1Vpp triangular wave input signal $v_{in}(t)$ is employed where the simulation result is depicted in Fig. 11. It is seen that the lowpass filter output is the differentiated version of the input $v_{in}(t)$ and must be integrated to recover the input signal. It thus confirms that the proposed circuit can be applied for a delta modulator.

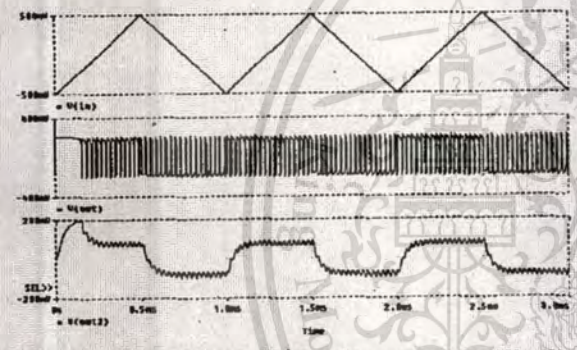


Figure 11. The simulation result where the upper trace is 1kHz, 1Vpp triangular wave signal, the middle trace is the delta modulation output and the lower trace is lowpass filter output.

B. *TSPICE simulation*

The L-edit layout of the proposed circuit is shown in Fig. 12 where the occupied active area is 0.45mm^2. The simulation result for sigma-delta modulator by using TSPICE where $C = 0.05\mu F$, $I_{B1} = I_{B2} = I_{B3} = 0.1mA$ is demonstrated in Fig. 13.

IV. CONCLUSIONS

A simple circuit for sigma-delta/delta modulation has been presented. One advantage of the proposed circuit is that the clock signal used for modulation is inherent in the circuit; the modulating signal is thus only an external input needed. Furthermore, frequency and amplitude of the digital pulse output can be independently adjusted by electronic tuning. The PSIPCE simulation results have demonstrated that without an additional device requirement, the proposed scheme can function either as sigma-delta or delta modulation by feeding the modulating signal at different node of the circuit. For the TSPICE simulation of the layer circuit with L-edit, it is only given for sigma-delta modulation due to limited space. With simple structure of the circuit, the proposed scheme is therefore suitable to be fabricated in the integrated circuit.

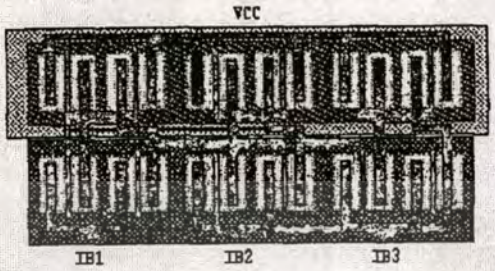


Figure 12. L-edit layout of the proposed circuit.

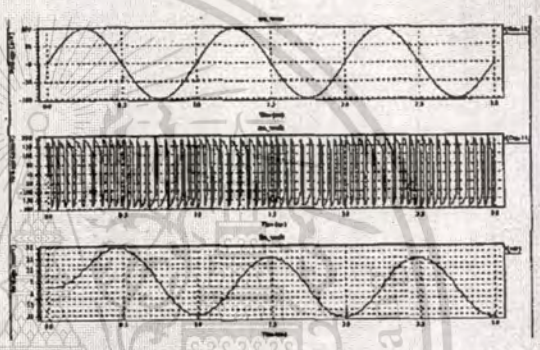


Figure 13. The TSPICE simulation result where the upper trace is 1kHz, 0.2Vpp sinusoidal input, the middle trace is sigma-delta modulation output, and the lower trace is lowpass filter output.

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AUTHOR BIOGRAPHY

Author : Mr. Panwit Tuwanut

Date of Birth : Septermber 21, 1977

Bechelor Degree : Bachelor of Telecommunications Engineering

Institute : Department of Telecommunications Engineering

Faculty of Engineering

King Mongkut's Institute of Technology Ladkrabang (KMITL)

Year of Graduation : 2001

Master Degree : Master of Electrical Engineering

Institute : Department of Telecommunications Engineering

Faculty of Engineering

King Mongkut's Institute of Technology Ladkrabang (KMITL)

Year of Graduation : 2004

Interested Researches : Analog and digital signal processing.

Related Publication

[1] Panwit Tuwanut, Jeerasuda Koseeyaporn, Paramote Wardkein. "A novel versatile modulator circuit" **AEU - International Journal of Electronics and Communications**, Vol. 63, Issue 5, May 2009, pp. 387-397

[2] Tuwanut, P.; Koseeyaporn, J.; Wardkein, P., "A Simple and Economic PWM and EA Modulator Circuit Based on Modified Source-Couple Oscillator" **TENCON 2006. 2006 IEEE Region 10 Conference**, 14-17 Nov. 2006, pp.1 – 4

[3] Tuwanut, P.; Koseeyaporn, J.; Wardkein, P., "A Novel Monostable Multivibrator Circuit" **TENCON 2005 2005 IEEE Region 10**, 21-24 Nov. 2005, pp.1 - 4

[4] Tuwanut, P.; Koseeyaporn, J.; Wardkein, P., "A novel versatile modulator circuit" **Communications and Information Technology, 2005. ISCIT 2005. IEEE International Symposium on,** vol. 2, 12-14 Oct. 2005, pp.1035 – 1038

[5] Tuwanut, P.; Maneechukate, T.; Koseeyaporn, J.; Wardkein, P., "A simple circuit for sigma delta/delta modulation Signals", **Circuits and Systems, 2005. ISSCS 2005. International Symposium on,** vol. 1, 14-15 July 2005, pp.143 - 146 Vol. 1