RESISTORLESS REALIZATION OF CURRENT-MODE FIRST-ORDER ALLPASS SECTION AND TWO-INTEGRATOR LOOP FILTER STRUCTURES USING CDTAs

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หัวข้อวิทยานิพนธ์	**การสังเคราะห์วงจรกรองผ่านทุกความถี่อันดับหนึ่งและวงจรกรองสัญญาณโครงสร้างลูปสองอินทิเกรเตอร์ที่ปราศจากตัวต้านทานพาสซีฟโดยใช้ CDTA**
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บทคัดย่อ

วิทยานิพนธ์ฉบับนี้นำเสนอการสังเคราะห์วงจรกรองผ่านทุกความถี่อันดับหนึ่งและวงจรกรองสัญญาณโครงสร้างลูปสองอินทิเกรเตอร์โดยใช้วงจร CDTA เป็นอุปกรณ์แอคทีฟและตัวเก็บประจุเทียบกราวด์เป็นอุปกรณ์พาสซีฟเท่านั้นโดยปราศจากตัวต้านทานพาสซีฟจากภายนอก วงจรแรกที่นำเสนอคือวงจรกรองผ่านทุกความถี่อันดับหนึ่งโดยใช้วงจร CDTA จำนวนสองตัวต่อร่วมกับตัวเก็บประจุเทียบกราวด์เพียงหนึ่งตัว ซึ่งสามารถสังเคราะห์ฟังก์ชันกรองผ่านทุกความถี่ได้ทั้งแบบกลับเฟสและแบบไม่กลับเฟสได้โดยไม่ต้องเปลี่ยนแปลงรูปแบบของวงจร รวมทั้งมีค่าอิมพีแดนซ์เอาต์พุตที่สูงจึงเหมาะสมกับการต่อใช้งานแบบคาสเคดในโหมดกระแส นอกจากนี้ยังได้นำเสนอแนวทางการประยุกต์ใช้วงจรกรองผ่านทุกความถี่ที่ได้ออกแบบ ในการสังเคราะห์วงจรออสซิลเลเตอร์แบบควอดราเจอร์โหมดกระแส สำหรับวงจรที่สองที่ได้นำเสนอ คือ วงจรกรองสัญญาณโครงสร้างลูปสองอินทิเกรเตอร์โหมดกระแสโดยใช้วงจร CDTA และตัวเก็บประจุเทียบกราวด์ ซึ่งสามารถสังเคราะห์ฟังก์ชันถ่ายโอนกระแสอันดับสองได้ครบทุกฟังก์ชัน

โครงสร้างของวงจรที่นำเสนอขึ้นทั้งหมดในวิทยานิพนธ์ฉบับนี้ มีรูปแบบเหมาะสมกับแนวทางการออกแบบวงจรรวม การต่อแบบคาสเคด และการปรับแต่งค่าทางอิเล็กทรอนิกส์ คุณสมบัติในการทำงานของวงจรทั้งหมดได้ถูกตรวจสอบและยืนยันความถูกต้องด้วยผลการจำลองการทำงานโดยใช้คอมพิวเตอร์ ซึ่งปรากฏผลสอดคล้องเป็นไปตามหลักการทางทฤษฎีที่ได้นำเสนอ

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ABSTRACT

This thesis presents a methodology for resistorless realizing current-mode first-order allpass (AP) filter section and two-integrator loop filter structures based on current differencing transconductance amplifiers (CDTAs) as active components and grounded capacitor as the only passive component. For the first presented configuration, the current-mode first-order AP filter section using only two CDTAs and one virtually grounded capacitor is introduced. The proposed circuit realizes both inverting and non-inverting types of AP filters, and also exhibits high-output impedances, which are easily cascading in the current-mode operation. It requires no external resistor and is electronically adjustable via an external bias current of the CDTA. No component-matching constraints are required. As an application of the proposed CDTA-based AP section, a current-mode quadrature oscillator is given. For the second presented configuration, the current-mode two integrator loop CDTA filter structures are described. The basic filter building blocks consist of current proportional block, current lossless and current lossy integrators. It is demonstrated that the derived filters can realize a general class of second-order current transfer functions.

Since the resulting structures contain only CDTAs and grounded capacitors, they are general and very appropriate for integration, cascading and electronic tuning. The influences of the CDTA non-idealities are also investigated. To confirm the theoretical analysis, all the proposed configurations and their applications are verified by computer simulation results.

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Tattaya Pukkalanun

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CHAPTER 1

Introduction

1.1 Statement and Signification of The Problems

An electric filter is a frequency selective network that shapes the spectrum of the input signal in such a manner that desired frequency content is achieved in the output signal [1]. It is employed to separate, pass or suppress a group of signals from the mixture of signals. Applications of filters are to eliminate contamination such as noise in communication systems and to separate relevant frequency components from irrelevant frequency components. Another important application is to band-limit signal before sampling and to convert discrete time signals into continuous time signals. Filters are also used to detect and demodulate signals in radio and television. In addition, they can be employed for improving quality of audio equipment, conversion of time domain multiplexed (TDM) signals into frequency domain multiplexed signals (FDM), speech synthesis, equalization of transmission lines ans cables, and numerous other applications involving signal processing. Continuous time filters can be broadly classified as passive and active filters. Passive filters are realized with passive components, i.e., resistor, capacitor and inductor. Other passive components like distributed RC elements and quartz crystal are also used. Such filters are used to work in MHz range. Active filters also use resistors and capacitors,

but the inductors are replaced by active devices capable of producing power gain. For the active devices, they can range from single transistor to integrated circuit controlled sources such as operational amplifier (OA) and more exotic devices, such as operational transconductance amplifier (OTA), current feedback operational amplifier (CFOA) and second generation current conveyor (CCII), etc. [2]-[8].

1.2 Area of Works

During the last decade, current-mode continuous time circuits are providing their important in the filed of analog signal processing and integrated circuit design in modern electronic community [9]. This is due to the well known fact that current-mode circuit design techniques have now been advocated as a candidate for low voltage, wide bandwidth, high speed signal processing and for several reasons. One reason is that in real current-mode signal processing, the circuit nodes are kept at a low impedance level which minimizes the influence of parasitic capacitances, leading to good high frequency performance. Another reason is the dynamic current range achievable even with low supply voltage. A low-voltage technique is one of the most important issues because of the advance of the large-scale integration with complicated circuit systems and the increasing demands for battery-operated portable equipments. In these respects, the realization of current-mode circuits with low-voltage and high-frequency operations seems to be attractive and importantly emerges

in several analog signal-processing fields. Hence, this thesis presents the research that only concentrated on the design of current-mode continuous-time filter.

In 1999, a versatile active building block circuit, namely current differencing buffered amplifier (CDBA), was introduced for the first time to provide new possibilities in the circuit synthesis and to simplify the circuit implementation [10]. Since the CDBA can be considered as a collection of current and voltage-mode unity gain cells, it has large dynamic range and quite wide bandwidth similar to its current-mode counterparts such as, current feedback operational amplifiers (CFAs) and CCIIs. In addtion, the current differncing feature also provides design flexibility. A lot of works about the CDBA applications have been published, particularly from the area of frequency selective systems [11]-[17]. However, the major drawbacks of the CDBA are also well known ; its transfer parameters cannot be controlled electronically and the CDBA applications from the area of frequency filters require some external passive resistors.

The above factors became important motivations for the design of a recently reported current-mode active building block, the so-called current differencing transconductance amplifier (CDTA) [18]. The internal structure of the CDTA device is quite similar to the CDBA, in which the voltage buffer is replaced by the single-input multiple-output type OTA. Due to the fully current-mode operation and the compactness of the circuit, the CDTA is capable of high-frequency operation and suitable for current-mode analog filtering applications [19]-[31]. Especially, when

more than two output terminals are used, it is possible to obtain very compact circuit topologies requiring less passive elements [22]-[23]. In this regard, the CDTA device seems to be promising and therefore attractive solution that deals with the issue of new active choice in designing low-component-count, high-frequency and resistor-less current-mode analog signal processing circuits. Recently, a trend in analog circuit design has emerged in which external passive resistors are not required. With no external passive resistor, the chip area occupied is saved and integration density is therefore increased. Moreover, the power consumption is also reduced thereby improving efficiency. This issue is also considered as the desired target of this work.

1.3 Goals and Objectives

The main objective of this study is to design and realize novel current-mode filter configurations based on the use of only CDTAs and grounded capacitors, which is considered to be an effective approach in filter design. Electronic tuning property is one of the major features of the design. The employment of only grounded capacitors in circuit implementation makes the designs suitable for integrated circuit development in both bipolar and CMOS technologies [32]-[33]. Besides, the purpose of this research may be divided into two main topics. The first topic deals with a realization of the resistorless current-mode first-order allpass (AP) filter, which can realize both inverting and non-inverting types of AP filtering functions all at high-output impedance terminals. The second objective is the structural generation of

current-mode two integrator loop filters, which can generate all the five standard biquadratic filtering functions from the same circuit configuration.

1.4 Novel Concepts of The Study

Novel concepts and techniques proposed in this thesis are summarized and given below.

1) Firstly, a circuit design of the current-mode first-order AP filter using only two CDTAs and one virtually grounded capacitor is presented [30]. The proposed circuit requires no external passive resistors and component-matching conditions for its realization. It also realizes both inverting and non-inverting types of first-order AP filters simultaneously without changing circuit configuration. The phase response of the proposed circuit is electronically tunable through the external DC bias current of the CDTA.

2) The second aim of this thesis is to propose a simple design for the implementation of current-mode quadrature oscillator, widely used in analog signal processing systems, by using the proposed CDTA-based first-order AP sections. The proposed oscillator configuration is realized through the cascade connection of the proposed CDTA-based AP filter and the CDTA-based current lossless integrator. The presented method shows that the resulting circuit contains only three CDTAs and two grounded capacitors without needing any external resistors, which is simpler and

employs less active and passive components than compared with the previously reported implementations.

3) The third deals with a versatile family of current-mode two integrator loop filter structures using CDTAs and grounded capacitors. The basic filter building blocks for the filter realization are composed of current proportional block, current lossless integrator and current lossy integrator based on the use of CDTAs as the major active components. The derived filter structures can realize a general class of second-order current transfer functions, and also exhibit both low-input and high-output impedances that is easily cascading in current-mode operation.

1.5 Organization of The Thesis

This thesis is organized into five chapters, and three appendices. Each chapter contains references at its end. Each chapter carries brief introduction of the study undertaken and followed by the detailed circuit descriptions, analysis, circuit parameters and the computer simulation results of the circuits belonging to the scope of that particular chapter. The contents of the thesis are as follows.

Chapter 1 describes the statement and significance of the research topic, and the objectives of this work. The outline of this thesis will also be described in this chapter.

Chapter 2 is mainly concerned with the main characteristic of the CDTA device, which is the active circuit building block mainly used in this thesis. There is an

elaboration on how this device is useful in realizing various filter circuits, and why this should be selected for the design of circuits. This chapter starts with the description of the distinguishing features of the CDTA, and subsequently gives details of some of circuit design techniques for realizing the CDTA. The CDTA-based fundamental active circuit building blocks, i.e., current-controlled resistance, current proportional block, and current integrators are also briefly introduced.

In chapter 3, a circuit technique for designing the current-tunable current-mode first-order AP filter, constructed from only two CDTAs and one virtually grounded capacitor with the absence of the passive resistors, is presented and analyzed. This chapter also describes the attactive features of the proposed circuit compared with the previously realization ones. The non-ideal analysis and the sensitivity study of the proposed circuit are investigated in detail. As an application of the proposed CDTA-based allpass section, the design of current-mode quadrature oscillator has been included in this chapter. To demonstrate the performances of all the proposed circuits and verify the theory, PSPICE simulations are accomplished.

Chapter 4 outlines the generation of the current-mode two-integrator loop filter structure. It describes the novel filter topologies using only CDTAs and grounded capacitors. The influences of the CDTA non-idealities on the filter performance are discussed in detail. Finally, the functionality of the resulting filters has been verified by simulation results.

In chapter 5, conclusions with respect to all the set objectives and goals are given. It gives a comprehensive summary of how the goals were achieved, and also offers recommendations for future investigation that may be undertaken in the same direction.

Finally, appendices are given, which contains the detailed analysis of the proposed circuits developed in this thesis.

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CHAPTER 2

Basic Concept of CDTA and Related Works

2.1 Introduction

Since the introduction of the current differencing buffered amplifier (CDBA) in 1999, it has been acknowledged to be a versatile active building block in designing analog circuits [1]. The CDBA can be considered as a collection of current-mode and voltage-mode unity gain amplifiers, it thus offers large dynamic range and wide bandwidth similar to its current-mode counterparts such as a second-generation current conveyor (CCII) and a current feedback amplifier (CFA) [2]. A variety of CDBA applications has also been considered by various researchers [1]-[23]. On the other hand, due to its voltage-mode operation nature, this element is thus appropriate for the implementation of particularly voltage-mode filters. In order to enjoy the inherent advantages of current-mode signal processing, an innovative design which does not involve a voltage-mode unity gain amplifier is highly desirable. Moreover, the major drawback of this device is that it cannot be controlled electronically.

To overcome these problems, a new active element with two current inputs and two kinds of current output, namely the current differencing transconductance amplifier (CDTA), has been recently introduced [24]. This device is a synthesis of the well-known advantages of the CDBA and a multi-output transconductance

amplifier to facilitate the implementation of electronically tunable continuous-time current-mode filter circuits. During the past few years, many implementations of CDTA device have been developed in the technical literature [25]-[33]. More recent works introduce transistor-level CDTA structures in CMOS technology [25]-[31]. The first CMOS-based circuit for the realization of the CDTA [25]-[26] as well as another topology proposed in [27]-[28] utilized 0.5 μm CMOS MIETEC process with ±2.5 V supply voltages. The work introduced in [29] presents the so-called multiple-output CDTA as an extension of the original circuit scheme from [25]-[26] by additional current outputs. The circuit from [28] is faster than those in [25]-[26], enabling easy g_m control, but with much higher parasitic input resistances of p and n terminals. The CMOS structure reported in [30] can operate in supply rails down to ±0.75 V, utilizing the 0.35 μm AMIS technology. The circuit performance is excellent up to tens of MHz, in particular the p and n input resistances are only 25 Ω thanks to the flipped voltage followers. However, this structure has not been optimized for high-frequency applications. In [31], the CMOS-based circuit realization of high-performance CDTA was demonstrated with TSMC 0.35-μm n-well CMOS process. This realization provides very low-input impedances (i.e., $r_p = r_n \cong$ 1.92 Ω), and very high frequency operation (≅ 1 GHz). However, one drawback of all mentioned CMOS structures are that the realized transconductance (g_m) is proportional to a square-root function of the bias current, which is non-linearly controlled.

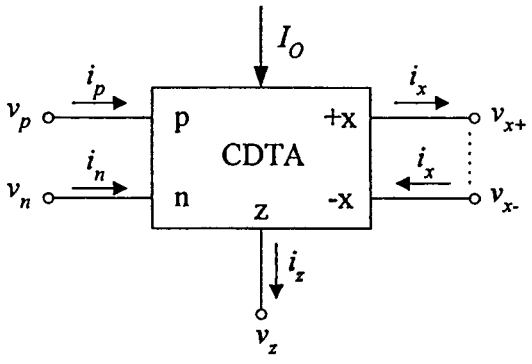
In addition, the bipolar realization of the CDTA described in [32]-[33] was proposed with transistor model of PR100N (PNP) and NP100N (NPN) of bipolar arrays ALA400 from AT&T. In comparison with the above-mentioned CMOS realizations, the bipolar CDTA provides very low p and n input resistances (below 5 Ω) and higher values of transconductance gain (approximately 2 mA/V). However, the current offset is too high (about 8 μA) and the maximum bandwidth is limited to tens of MHz.

In this chapter, the description of the CDTA is discussed. It also describes the historical developments of the CDTA element in both CMOS and bipolar technologies, and some CDTA-based basic active building blocks leading up to the development of current-mode filter systems.

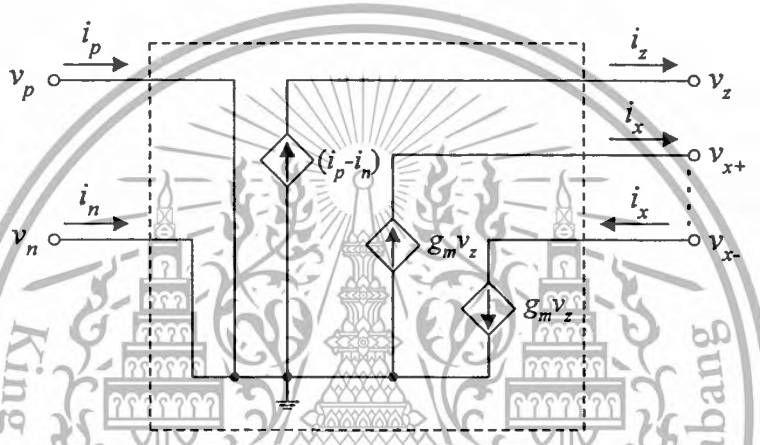
2.2 Description of CDTA

2.2.1 Ideal Behavior

The CDTA device with its electrical symbol in figure 2.1 has a pair of low-resistance current inputs p and n and an auxiliary current terminal z, whose outgoing current is the difference of input currents. At the x-terminals, output currents are equal in magnitude, and the product of the transconductance gain (g_m) and the voltage at the z-terminal gives their magnitudes.



(a)



(b)

Figure 2.1 : Ideal CDTA.

(a) electrical symbol (b) equivalent circuit

The port relations characterizing this device can be described by the following expressions [24]-[33] :

$$v_p = v_n = 0 \quad , \quad i_z = i_p - i_n \quad \text{and} \quad i_x = g_m v_z = g_m Z_z i_z \qquad (2.1)$$

where $v_z = i_z.Z_z$ and Z_z is an external impedance connected at the terminal z. Thus, according to the equivalent circuit of figure 2.1(b), the CDTA can be considered as a combination of a current substractor unit followed by a multiple-output operational

transconductance amplifier (MO-OTA). Theoretically, an OTA is assumed as an ideal voltage-controlled current source that can be described by $i_x = g_m(v^+ - v^-)$, where i_x is the output current, and v^+ and v^- are the non-inverting and inverting input voltages of the OTA, respectively. Note that g_m is a function of an external bias current. When this element is used in CDTA, one of its input terminals is connected to ground (e.g., $v^- = 0$ V). With multiple-output availability, $i_x = g_m v^+ = g_m v_z = g_m Z_z i_z$ is assumed.

2.2.2 Non-ideal Behavior

In practice, the deviation from the ideal CDTA performance can be divided into two categories, i.e., parasitic gain effects and parasitic impedance effects. Considering the parasitics and transfer errors, the simplified equivalent circuit represented the behavior of the non-ideal CDTA can be illustrated in figure 2.2 [34]-[35]. These result from the series input resistances R_p and R_n at terminals p and n, and the shunt output impedances ($R_z//C_z$ and $R_x//C_x$) at terminals z and x, respectively. More specifically, α_p, α_n, γ and β are the parasitic current gains between the p to z, n to z, and +x to –x terminals, and transconductance inaccuracy factor between the z to +x terminals of the CDTA, respectively. These parasitic values slightly differ from their ideal unit values by the effect of the CDTA tracking errors, those absolute values being much less than unity. Therefore, for the non-ideal case, the terminal relations of the CDTA describing in equation (2.1) can be rewritten by :

$$v_p = v_n = 0 \quad , \quad i_z = \alpha_p i_p - \alpha_n i_n \quad ,$$

$$i_{x+} = \beta g_m v_z = \beta g_m Z_z i_z \qquad \text{and} \qquad i_{x-} = \gamma\beta g_m v_z = \gamma\beta g_m Z_z i_z \,. \tag{2.2}$$

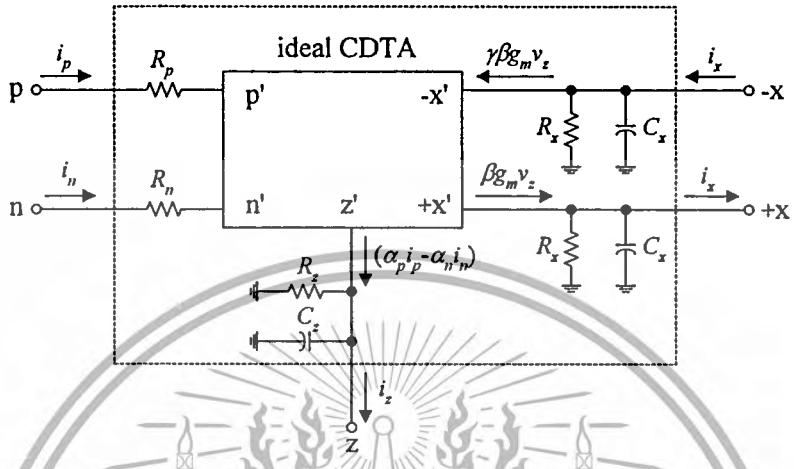


Figure 2.2 : Simplified equivalent circuit of the non-ideal CDTA.

2.3 CDTA Realizations

This section considers the design approaches for CMOS and bipolar CDTAs. Various structures that can be used to implement this element will be discussed in detail.

2.3.1 CMOS CDTA Realizations

2.3.1.1 Early Keskin and Biolek CDTA

An early simple realization of the CDTA by Keskin and Biolek is shown in figure 2.3 [25]-[26]. In this circuit, transistors M_1 to M_{12} perform the current differencing operation while transistors M_{13} to M_{24} convert the voltage at the z-terminal to output currents at the two outputs of the dual-output OTA (DO-OTA) section. DO-OTA's transconductance (g_m) is controllable electronically via its bias

current I_{B3}. Also, a resistor R_z connected at the z-terminal can be used to adjust the gain of CDTA, while the voltage at the output of DO-OTA is equal to $v_z = i_z Z_z$.

The gate terminals of the output transistors M_{11} and M_{12} in current differencing section are connected to bias voltages to provide drain output and high impedance at z terminal (ideal current controlled current source, CCCS). Since an external resistor with relatively low resistance value (at the order of few kΩ) is connected to the z-terminal, the use of diode-connected transistors M_{11} and M_{12} becomes advantageous from integrated circuit (IC) manufacturing point of view. This is due to the fact that the need for two additional bias-voltages is eliminated by using diode-connected transistors.

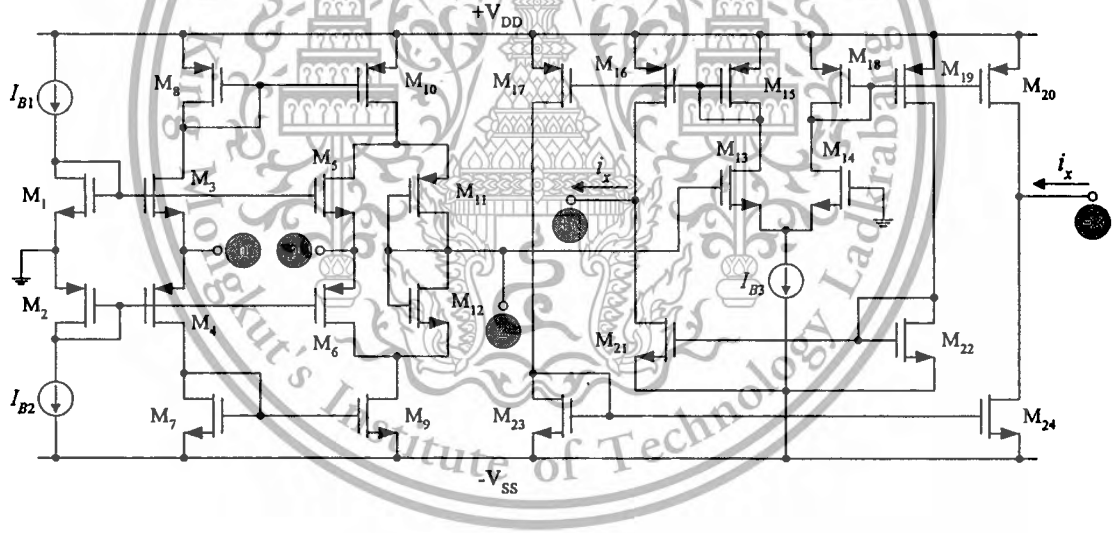


Figure 2.3 : Early CMOS-based CDTA realization by Keskin and Biolek.

2.3.1.2 Uygur and Kuntman CDTA

Uygur and Kuntman have suggested a possible CMOS-based CDTA circuit realization, which is used in a current-mode anti-aliasing video filter and suitable for video signal-processing applications [27]-[28]. This technique is based on the use of

a differential current controlled current source (DCCCS) [12] as an input stage, followed by a floating current source (FCS) [36] which realizes the dual-output transconductance. A complete implementation of this CDTA is presented in figure 2.4. The transistors M_1 to M_{16} function the input DCCCS stage, which is used for transforming the differential input current to the intermediate voltage that is the voltage at the z-terminal, while M_{17} to M_{22} form the dual-output transconductor stage. Due to the output transconductor stage is built by FCS, it is also reported for high-frequency operation [36]. Note that, in this approach, aspects of the transistors M_8 and M_9 should be chosen two times of the M_3, M_4 and M_{12}, M_{13} transistors in order to operate the input stage correctly. In this circuit, the g_m-parameter is determined by the transconductance of output transistors that can be approximated as [28] :

$$g_m = \frac{g_{m18} + g_{m20}}{2} \tag{2.3}$$

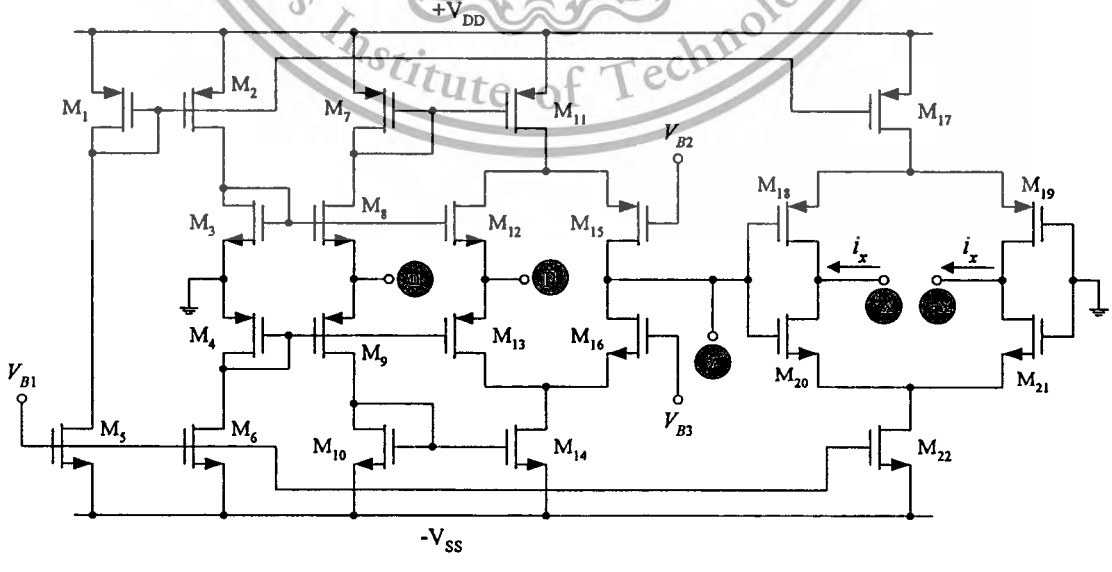


Figure 2.4 : Complete configuration of CMOS CDTA by Uygur and Kuntman.

Summary of the performance of this CDTA element with CMOS process parameters of 0.5 μm MIETEC technology is given in table 2.1.

Table 2.1 : Performance data of the CMOS CDTA given in figure 2.4.

Parameter	Value
Technology	0.5 μm MIETEC
The supply voltages	$+V_{DD} = -V_{SS} = 2.5V$
Transconductance gain (g_m)	400 μA/V
i_z/i_p (-3 dB) bandwidth	497 MHz
i_z/i_n (-3 dB) bandwidth	301 MHz
r_p (p-terminal input reistance)	1.24 kΩ at 100 MHz
r_n (n-terminal input reistance)	834 Ω at 100 MHz
Power consumption	4 mW

2.3.1.3 Low-voltage CMOS CDTA

After the introduction of the CMOS CDTA realization, Uygur and Kuntman have also described the low-voltage CMOS CDTA structure that can operate in supply rails down to ±0.75V [30]. In this configuration shown in figure 2.5, the transistors M_1 to M_{10} form an input stage that is realized by using flipped voltage followers (FVFs) M_3-M_4 and M_8-M_9 [37]. To construct the current mirrors, the outputs of FVFs are used as inputs p and n of the CDTA. The feedback action of FVF circuits results in very low-input resistances at the p and n terminals (r_p and r_n), which can be calculated approximately using the following equations [30].

$$r_p \cong \frac{1}{g_{m2}g_{m3}r_{o3}} \tag{2.4}$$

and

$$r_n \cong \frac{1}{g_{m8}g_{m9}r_{o8}} \tag{2.5}$$

where g_{mi} and r_{oi} represent the transconductance and the output resistance of the transistors M_i, respectively.

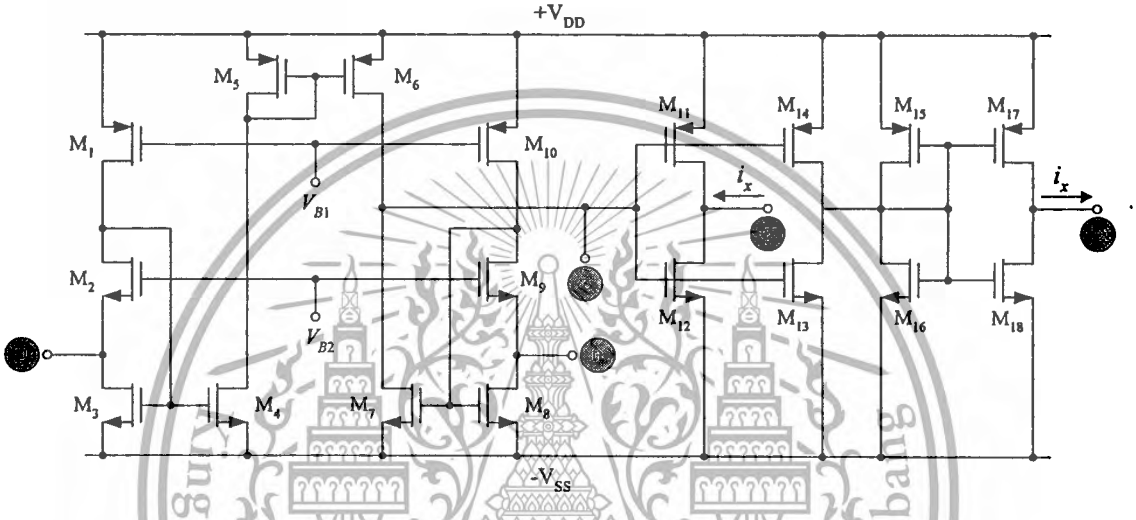


Figure 2.5: Low-voltage CMOS CDTA realization by Uygur and Kuntman.

For the output stage, it consists of inverters. Negative output (-x) is taken at the output of the first inverter, signal is mirrored at the input of the second inverter that is connected in a unity gain topology. The last one inverts the negative signal and also produces positive output current (+x) [38]. Therefore, the transconductance parameter of this CDTA is directly dependent on the transconductance of these inverters, which is equal to the sum of the inverter transistor transconductances as follows.

$$g_m = g_{m11} + g_{m12} \tag{2.6}$$

In table 2.2, the performance of this CDTA is summarized in a tabular format.

Table 2.2 : Performance data of the low-voltage CMOS CDTA shown in figure 2.5.

Parameter	Value
Technology	0.35 μm AMIS
The supply voltages	$+V_{DD} = -V_{SS} = 0.75V$
Transconductance gain (g_m)	210 μA/V
i_z/i_p (-3 dB) bandwidth	87 MHz
i_z/i_n (-3 dB) bandwidth	20 MHz
r_p (p-terminal input reistance)	25 Ω at 1 MHz
r_n (n-terminal input reistance)	25 Ω at 1 MHz
Power consumption	3.7 mW
Bias voltages	$V_{B1} = -0.2V$, $V_{B2} = 0.3V$
Bias current	54 μA
Input offset current	0.4 μA

2.3.1.4 High-performance CMOS CDTA

Recently, in 2008, Biolek and Keskin developed an improved CDTA, combining the features of low parasitic input impedances and high-speed operation [31]. Figure 2.6 illustrates the CMOS transistor-level structure of the high-performance CDTA. The current differencer is implemented by transistors M_1 to M_{17}. The voltage buffers provide low-input impedances and also keep the input terminals at virtual ground ($v_p = v_n \cong 0$). The current mirrors convey the difference of input signals to the z-terminal. The transistors M_{21} to M_{28} form a DO-OTA, which is composed of two inverting amplifiers. It should be noted that the two inverting

amplifiers are the same configuration as that in figure 2.4. Performance data of the improved CMOS CDTA with 0.35 μm n-well CMOS real process from TSMC are given in table 2.3. Detail of model parameters is listed in Appendix A.1.

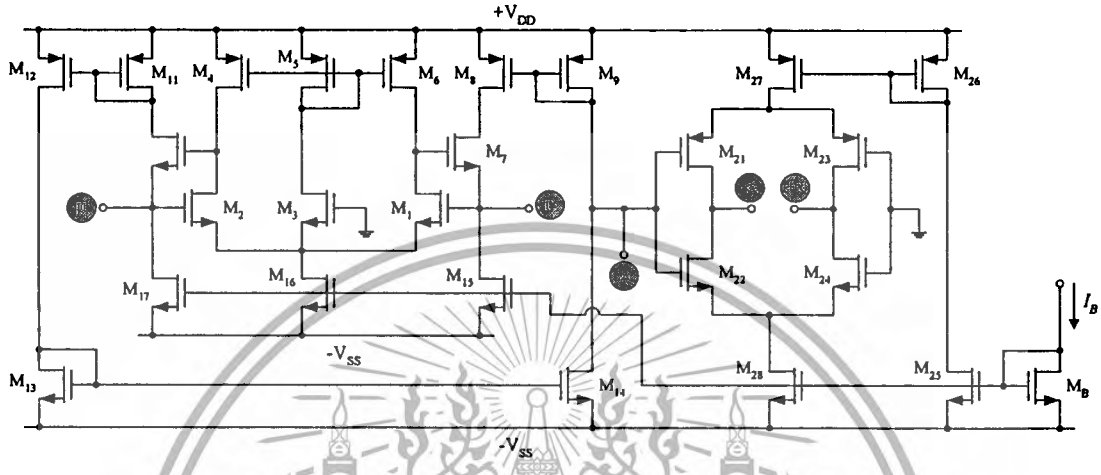


Figure 2.6 : High-performance CMOS CDTA realization by Biolek and Keskin.

Table 2.3 : Performance data of the high-performance CDTA shown in figure 2.6.

Parameter	Value
Technology	0.35 μm TSMC
The supply voltages	$+V_{DD} = -V_{SS} = 1.8V$
Bias current (I_B)	40 μA
Transconductance gain (g_m)	873 μA/V
i_z/i_p , i_z/i_n	1.36 GHz, 1.14 GHz
i_{x+}/i_p , i_{x+}/i_n	1.01 GHz, 0.93 GHz
i_{x-}/i_p , i_{x-}/i_n	1.23 GHz, 0.96 GHz
r_p , r_n	1.92 Ω , 1.92 Ω
r_z (z-terminal reistance)	388 kΩ
r_{x+} , r_{x-}	16.30 MΩ , 16.21 MΩ
Power consumption	6.31 mW
Input current range	±210 μA

2.3.2 Bipolar CDTA Realization

Interestingly, because of intrinsically higher transconductance values, bipolar transistors can offer power dissipation advantages over CMOS technology realization. Only bipolar CDTA described in the literature will be considered in this sub-section. Tangsrirat and co-workers considered the design of the bipolar technology CDTA, whose the complete schematic is depicted in figure 2.7 [32]-[35]. Note that in this circuit, the transistors Q_1 to Q_{11} function as an input stage (i.e. the current differencing circuit) followed by a DO-OTA implemented by using transistors Q_{12}-Q_{30}. Thus, in this case, the transconductance parameter g_m of the CDTA is directly proportional to the external bias current I_O, which can be written by [33]:

$$g_m = \frac{I_O}{2V_T} \tag{2.7}$$

where $V_T \cong 26$ mV at 27°C is the usual thermal voltage given by kT/q, k = Boltzmann's constant = 1.38×10^{-23} J/K, T = the absolute temperature (in kelvins), and $q = 1.6\times10^{-19}$ Couloumb.

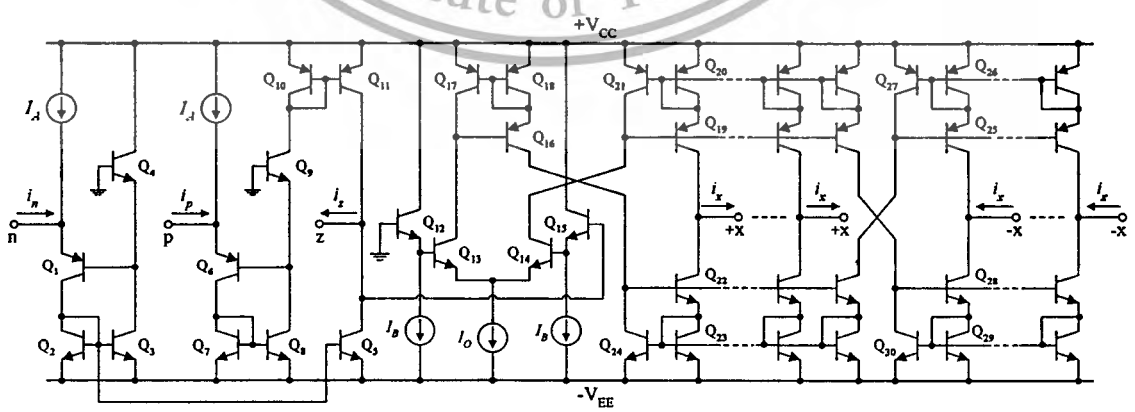


Figure 2.7 : Bipolar realization of the CDTA by Tangsrirat et. al..

Since the internal negative feedback transistors Q_1 and Q_6 are respectively incorporated to achieve low input resistance at the input terminal p and n, the input resistances r_p and r_n of this circuit will be approximately equal to [5], [33] :

$$r_p = \frac{r_{e9}}{\beta_6} \tag{2.8}$$

and

$$r_n = \frac{r_{e4}}{\beta_1} \tag{2.9}$$

where $r_{ei} = V_T/I_A$ and β_i denote the small-signal emitter resistance and the common-emitter current gain of Q_i, respectively. Equations (2.8) and (2.9) show that, with negative feedback factors (β_1 and β_6), the values of r_p and r_n are relatively low as desired. Table 2.4 summarizes the simulated performance of the bipolar CDTA realization using the transistor model of PR100N (PNP) and NP100N (NPN) of bipolar arrays ALA400 from AT&T, which are tabulated in Appendix A.2.

Table 2.4 : Performance data of the bipolar CDTA shown in figure 2.7.

Parameter	Value
Technology	PR100N and NP100N of ALA400
The supply voltages	$+V_{CC} = -V_{EE} = 3V$
Bias currents ($I_A = I_B$)	100 μA
Transconductance gain (g_m)	2 mA/V
i_z/i_p (-3 dB) bandwidth	30 MHz
i_z/i_n (-3 dB) bandwidth	32 MHz
r_p , r_n	4.5 Ω , 4.5 Ω
r_z , r_x	360 kΩ, 713 kΩ
Power consumption	3.23 mW
Input offset current	4 μA

2.4 CDTA-based Fundamental Active Building Blocks

The following section introduces the basic CDTA-based building blocks used for realizing the proposed current-mode filter structures. Several active building blocks based on CDTAs and grounded capacitors are discussed in detail.

2.4.1 Current-Controlled Resistance

An electronically tunable resistance can easily be obtained using the CDTA as shown in figure 2.8 [34]. Since $i_x = g_m v_z = g_m v_{in}$ and $i_{in} = -i_z = -(-i_n) = -(-i_x)$, the input admittance ($Y_{in}$) seen at input port will be

$$Y_{in} = \frac{i_{in}}{v_{in}} = \frac{i_x}{v_{in}} = g_m \tag{2.10}$$

Clearly, the circuit in figure 2.8 acts as a grounded current-variable resistor.

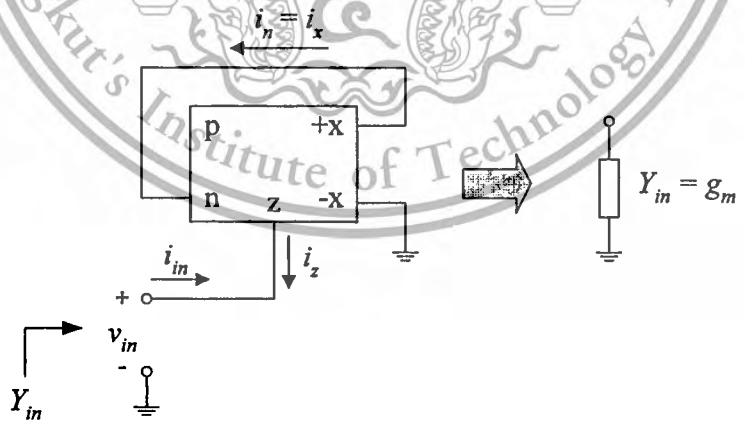


Figure 2.8 : CDTA-based controlled resistance.

2.4.2 Current Proportional Block

Figure 2.9 illustrates the current proportional block based on the realization with a single CDTA [39]-[40]. Its current transfer relationship can be found to be :

$$I_o = \left(\frac{g_{m1}}{Y}\right)(I_{i1} - I_{i2}) \tag{2.11}$$

Consequently, the current proportional block corresponds to the condition : $Y = g_1$ (conductance). Furthermore, if the conductance g_1 is realized by the controlled resistance of figure 2.8, then the resulting circuit, as shown in figure 2.10, functions as an electronically controllable current amplifier without needing any external passive resistors. In this case, the current gain (K) of this circuit can be expressed as :

$$K = \frac{I_o}{I_{i1} - I_{i2}} = \frac{g_{m1}}{g_{m2}} \tag{2.12}$$

From equation (2.12), it is worth mentioning here that the amplifier gain K can be tuned linearly and electronically through adjusting the transconductance ratio (g_{m1}/g_{m2}).

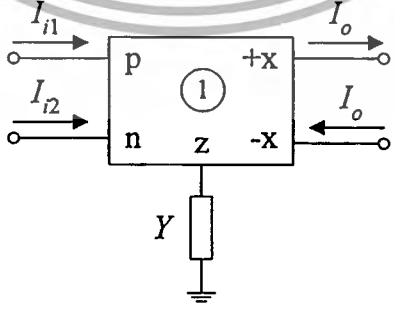


Figure 2.9 : Simple current proportional block using CDTA.

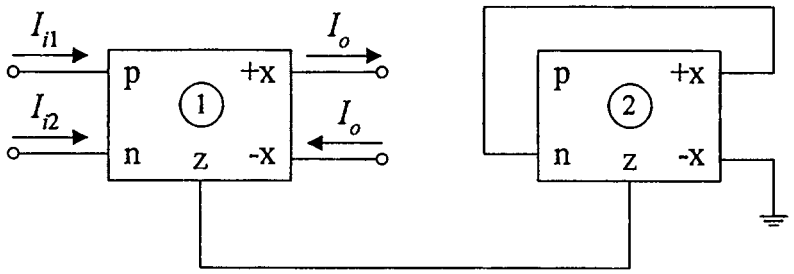


Figure 2.10 : CDTA-based current-controlled current amplifier.

2.4.3 Current Lossless Integrator

Similarly, if Y represents an admittance of a capacitor C_1, or $Y = sC_1$, the current-mode lossless integrator is then obtained. The corresponding relation of the ideal integrator becomes :

$$I_o = \left(\frac{g_{m1}}{sC_1}\right)(I_{i1} - I_{i2}) \tag{2.13}$$

2.4.4 Current Lossy Integrator

Another interesting structure is obtained when $Y = g_2 + sC_2$. As shown in figure 2.11, the current lossy integrator can be realized with the following current realtion :

$$I_o = \left(\frac{g_{m1}}{g_2 + sC_2}\right)(I_{i1} - I_{i2}) \tag{2.14}$$

In a practical viewpoint, the conductance g_2 may be realized by replacing with the controlled resistance of figure 2.8. Therefore, the usage of any external passive resistors is not necessary for this structure, which is especially important for achieving higher integration.

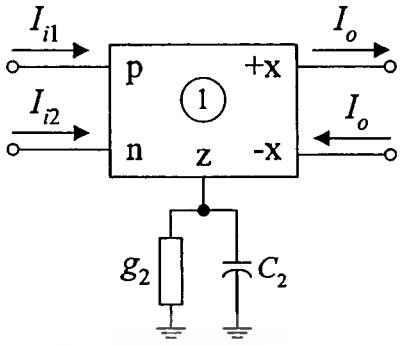


Figure 2.11 : CDTA-based current lossy integrator.

2.5 Conclusions

In this chapter, the essential characteristics of the CDTA including the detailed circuit descriptions, circuit parameters and simulation results are discussed in detail. It also briefly describes the historical developments and some basic entities leading up to the implementation of CDTA elements. The great merit of the CDTA-based circuit realization is that the transconductance gain (g_m) is available as a design parameter. Thus, the need for external passive resistors is of course eliminated. This type of circuit contains only CDTAs and grounded capacitors which can be very conveniently implemented in monolithic form. In addition, this chapter also explains the basic CDTA-based active building blocks, which will be used in the design of current-mode filter structures in all subsequent chapters.

2.6 References

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CHAPTER 3

Resistorless Realization of Current-Mode First-Order Allpass Filter Using CDTAs

3.1 Introduction

It is well known that the first-order allpass filter is widely used in several analog signal-processing applications. In general, it is used for phase shifting from 0° to 180° or from 180° to 0°, while keeping the amplitude of the signal constant over the frequency range of interest. It can also be used to realize universal biquadratic filters, to synthesize quadrature and multiphase oscillators, and to implement high quality-factor frequency selective filters. Current-mode circuits are receiving much attention because of their potential advantages such as wider bandwidth, wider dynamic range, simpler circuitry, and lower power consumption. As a result, a number of current-mode first-order allpass filter realizations using different active building blocks were reported in the technical literature [1]-[12]. However, some of these networks suffer from the use of floating resistors or capacitors [1]-[6]. The networks reported in [6]-[8] use a number of passive elements with matching conditions, but provide high impedance outputs suited for current-mode cascading. Furthermore, most of the existed realizations do not include electronically tunability property [1]-[3], [6]-[11]. Although first-order allpass sections with electronic tuning

properties were reported in [4]-[5], [13]-[15], the current-mode configurations of [4]-[5] do not exhibit high output impedance while the works in [13]-[15] operated in voltage-mode. In [12], an electronically tunable current-mode first-order allpass filter realization was presented, which requires only current differencing transconductance amplifier (CDTA) and three passive components. Moreover, most of them usually realize either non-inverting or inverting types of allpass function [1]-[5], [7]-[14]. For the realization of the complementary type, the circuit configuration need to be changed. In view of above explanation, none of the earlier circuits is able to achieve all the desirable features simultaneously.

This chapter presents the resistorless and cascadable current-mode first-order allpass filter employing only two CDTAs and a single-virtually grounded capacitor, which contains a minimum number of components. Due to electronically tunability property of the CDTA, the phase response of the proposed circuit can be adjusted by an external bias current. No component-matching conditions for realizing the allpass functions are required. The circuit can realize both inverting and non-inverting types of current-mode first-order allpass filters without changing circuit topology. The proposed circuit also exhibits high-output impedance, which is easily cascading in the current-mode operation. In view of the literature surveys, a comparison of the previously reported realizations from [1]-[12] and the proposed circuit introduced in this work is summarized in table 3.1. It reveals that the proposed circuit is capable of achieving all the above-mentioned important parameters simultaneously. In order to

illustrate the design utility of the proposed CDTA-based allpass section, an application in realizing a current-mode quadrature sinusoidal oscillator is also given.

3.2 Circuit Description

Figure 3.1 shows the proposed resistorless current-mode first-order allpass filter with electronic tuning properties employing only two CDTAs and one virtually grounded capacitor. Due to internally grounded input terminals of the CDTA, one end of the capacitor C connected in the structure is effectively grounded and the problem associated with this capacitor is not expected. Therefore, the proposed configuration is a canonical structure and is compatible with monolithic implementation.

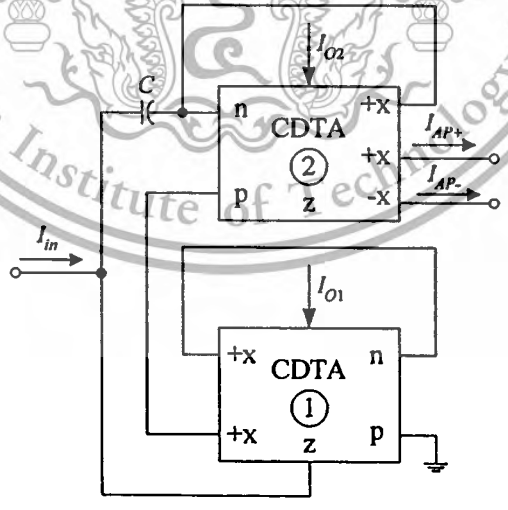

Figure 3.1 : CDTA-based current-mode first-order allpass filter.

Table 3.1 : Comparison of proposed allpass filter with previously reported ones.

AP filters	No. of active elements	No. of passive elements	Without component matching conditions	High output impedance	Grounded/virtually grounded capacitor	Resistorless circuit	Electronically tunable	Realizability of both the allpass types
[1]	1	4	×	✓	×	×	×	×
[2]	1	3	×	×	✓	×	×	×
[3]	1	2	✓	×	✓	×	×	×
[4]	1/2	1	×/✓	×	×	✓	✓	×
[5]	1	2	×	×	×	✓	✓	×
[6]	1	5	×	✓	×	×	×	✓
[7]	2	4	×	✓	✓	×	×	×
[8]	2	3	×	✓	✓	×	×	×
[9]	1	2	✓	✓	✓	×	×	×
[10]	1	2	✓	✓	✓	×	×	×
[11]	1	2	✓	✓	✓	×	×	×
[12]	1	3	✓	✓	✓	×	✓	×
Proposed	2	1	✓	✓	✓	✓	✓	✓

A routine analysis of the circuit using the characterisc of the CDTA describing in equation (2.1) yields the following current transfer function [Appendix B.1] :

$$\frac{I_{AP+}}{I_{in}} = -\frac{I_{AP-}}{I_{in}} = \frac{1-s\left(\frac{C}{g_{m1}}\right)}{1+s\left(\frac{C}{g_{m1}}\right)} \tag{3.1}$$

From equation (3.1), it can be seen that the circuit can realize both non-inverting and inverting type first-order allpass functions. As it is demonstrated in figure 3.1, the proposed CDTA-based allpass section does not require any external passive resistor, and any matching conditions for realizing first-order allpass function. Here, the pole frequency of the circuit is expressed as :

$$\omega_o = \frac{g_{m1}}{C} = \frac{I_{O1}}{2V_T C} \tag{3.2}$$

and the phase responses are respectively given by :

$$\phi_{AP+} = -2\tan^{-1}\left(\frac{\omega C}{g_{m1}}\right) \tag{3.3}$$

and

$$\phi_{AP-} = 180^\circ - 2\tan^{-1}\left(\frac{\omega C}{g_{m1}}\right) \tag{3.4}$$

Equations (3.3) and (3.4) show that the proposed allpass filter can provide phase shifting both between 0° to -180° and 180° to 0°. Moreover, the shifted phase value can be controlled electronically by adjusting the value of g_{m1}.

3.3 Effects of non-ideal CDTA

In this section, the proposed allpass circuit is studied taking into account the non-idealities of the CDTA. Taking into account the parasitics and transfer errors of the non-ideal CDTA described in section 2.2.2, the non-ideal current transfer functions for the circuit of figure 3.1 can be expressed as [Appendix B.2] :

$$\frac{I_{AP+}}{I_{in}} = \left[\frac{\left(\frac{\alpha_{p2}}{\alpha_{n2}}\right)}{1+\left(\frac{1}{\alpha_{n2}\beta_2 g_{m2} R_{z2}}\right)+s\left(\frac{C_{z2}}{\alpha_{n2}\beta_2 g_{m2}}\right)} \right] \left[\frac{1-sC\left(\frac{\alpha_{n2}}{\alpha_{p2}\alpha_{n1}\beta_1 g_{m1}}+\frac{\alpha_{n2}R_{p2}}{\alpha_{p2}}-R_{n2}\right)}{1+sC\left(\frac{1}{\alpha_{n1}\beta_1 g_{m1}}+R_{p2}+R_{n2}\right)} \right] \tag{3.5}$$

and

$$\frac{I_{AP-}}{I_{in}} = \left[\frac{-\left(\frac{\alpha_{p2}\gamma_2}{\alpha_{n2}}\right)}{1+\left(\frac{1}{\alpha_{n2}\beta_2 g_{m2} R_{z2}}\right)+s\left(\frac{C_{z2}}{\alpha_{n2}\beta_2 g_{m2}}\right)} \right] \left[\frac{1-sC\left(\frac{\alpha_{n2}}{\alpha_{p2}\alpha_{n1}\beta_1 g_{m1}}+\frac{\alpha_{n2}R_{p2}}{\alpha_{p2}}-R_{n2}\right)}{1+sC\left(\frac{1}{\alpha_{n1}\beta_1 g_{m1}}+R_{p2}+R_{n2}\right)} \right] \tag{3.6}$$

where R_{pi}, R_{ni}, R_{zi}, α_{pi}, α_{ni}, γ_i, β_i and C_{zi} denote the parameters R_p, R_n, R_z, α_p, α_n, γ, β and C_z of the i-th CDTA (i = 1, 2), respectively. Since usually $R_{z2} >> 1$ and $(1/\alpha_{n1}\beta_1 g_{m1}) >> R_{p2}, R_{n2}$, equations (3.5) and (3.6) are approximately

$$\frac{I_{AP+}}{I_{in}} \cong \left[\frac{\left(\frac{\alpha_{p2}}{\alpha_{n2}}\right)}{1+s\left(\frac{C_{z2}}{\alpha_{n2}\beta_2 g_{m2}}\right)} \right] \left[\frac{1-s\left(\frac{C}{\alpha_{n1}\beta_1 g_{m1}}\right)\left(\frac{\alpha_{n2}}{\alpha_{p2}}\right)}{1+s\left(\frac{C}{\alpha_{n1}\beta_1 g_{m1}}\right)} \right] \tag{3.7}$$

and

$$\frac{I_{AP-}}{I_{in}} \cong \left[\frac{-\left(\frac{\alpha_{p2}\gamma_2}{\alpha_{n2}}\right)}{1+s\left(\frac{C_{z2}}{\alpha_{n2}\beta_2 g_{m2}}\right)}\right]\left[\frac{1-s\left(\frac{C}{\alpha_{n1}\beta_1 g_{m1}}\right)\left(\frac{\alpha_{n2}}{\alpha_{p2}}\right)}{1+s\left(\frac{C}{\alpha_{n1}\beta_1 g_{m1}}\right)}\right] \quad (3.8)$$

It is apparent from equations (3.7) and (3.8) that the filter gain (H) is now dependent on the parasitic current gains α_{p2}, α_{n2} and γ_2 of the CDTA2. To eliminate this effect, a careful circuit realization of CDTA, which provides $\alpha_p \cong \alpha_n \cong \gamma \cong 1$, should be strictly considered. Similarly, the pole frequency ω_o of the proposed circuit is slightly deviated from the ideal case by the factor $\alpha_{n1}\beta_1$. However, we can also alleviate the effect of this factor by trimming the g_{m1}-value. It is further noted that one extra pole ($\omega_p = \alpha_{n2}\beta_2 g_{m2}/C_{z2}$) due to the parasitic elements appears in the filter characteristic. For a practical CDTA, $C_{z2} << C$, the frequency of ω_p is sufficiently higher than ω_o of the proposed allpass circuit ($\omega_p >> \omega_o$), thus the influence of ω_p on the frequency response can be ignored.

3.4 Sensitivity Analysis

In general, the relative sensitivity of a circuit parameter G to the component of variation x can be defined as:

$$S_x^G = \frac{\%\text{change in G}}{\%\text{change in } x} = \frac{(\Delta G/G)\times 100\%}{(\Delta x/x)\times 100\%} \quad (3.9)$$

which can also be written as follows :

$$S_x^G = \frac{\partial G/G}{\partial x/x} = \frac{x}{G}\frac{\partial G}{\partial x} \quad (3.10)$$

Using the above definition, the incremental sensitivities of H and ω_o to active and passive components for the introduced allpass filter described by equations (3.7) and (3.8) are analyzed and also found as [Appendix B.3]:

$$S_{\alpha_{p2}}^{H} = -S_{\alpha_{n2}}^{H} = S_{\gamma_2}^{H} = 1 \tag{3.11}$$

$$S_{\alpha_{p1},\alpha_{n1},\beta_1,\beta_2,g_{m1}}^{H} = S_C^{H} = 0 \tag{3.12}$$

$$S_{\alpha_{n1},\beta_1,g_{m1}}^{\omega_o} = -S_C^{\omega_o} = 1 \tag{3.13}$$

and

$$S_{\alpha_{p1},\alpha_{p2},\alpha_{n2},\beta_2}^{\omega_o} = 0 \tag{3.14}$$

It is evident that the H and ω_o sensitivities are within unity in magnitude. Also, note from the sensitivity results that H is only sensitive to variations of tracking errors of the CDTA2. On the other hand, these errors have no influence on ω_o. To further illustrate this point, for instance, let us assume that $\alpha_{p2} = \alpha_{n2} = \gamma_2 \cong 0.99$ (a -1% change from their theoretical values, i.e., the unity value). From the defining relation for H sensitivity in (3.11), we can find

$$\frac{\Delta H}{H} = \left(\frac{\Delta\alpha_{p2}}{\alpha_{p2}}\right)S_{\alpha_{p2}}^{H} + \left(\frac{\Delta\alpha_{n2}}{\alpha_{n2}}\right)S_{\alpha_{n2}}^{H} + \left(\frac{\Delta\gamma_2}{\gamma_2}\right)S_{\gamma_2}^{H}$$

$$= (-0.01)(1) + (-0.01)(-1) + (-0.01)(1) = -0.01$$

We may conclude, therefore, that the total effect of a -1% change in the values of α_{p2}, α_{n2} and γ_2 will produce a -1% change in the gain H. Clearly, in this case, H is reduced by 1%, a -1% error.

3.5 Simulation results

PSPICE program was carried out to check the workability of the proposed circuit of figure 3.1. For the simulation purpose, the CDTA given in figure 2.7 was constructed with the transistor model parameters of PR100N (PNP) and NP100N (NPN) [20] and DC supply voltages of ±2 V. The designed capacitor value and the bias currents of the CDTAs were chosen as : $C = 1$ nF, $I_{O1} = 100$ μA and $I_{O2} = 10$ μA, which leads to achieve $f_o = \omega_o/2\pi \cong 318$ kHz, $\phi_{AP-} \cong 90°$ and $\phi_{AP+} \cong 270°$.

Figure 3.2 shows the time domain responses of the proposed filters in which 100 μA peak sinusoidal input current at 318 kHz is applied. This causes the time shifts of 805 nS and 2.38 μS at the filter outputs corresponding to the phase shifts of about 92.3° and 271.1°, respectively, which are in good agreement with the theoretical analysis.

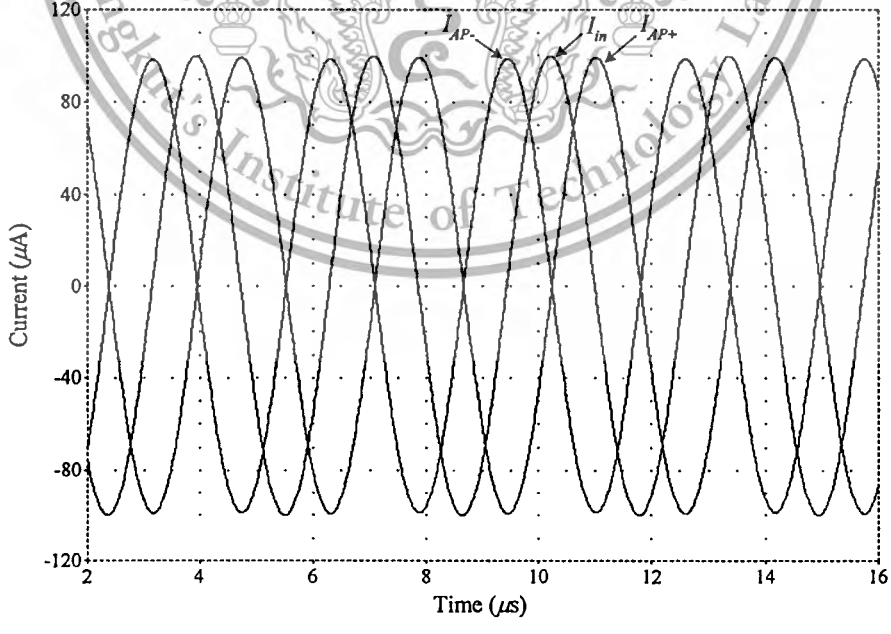

Figure 3.2 : Time domain responses of the presented allpass filter in figure 3.1.

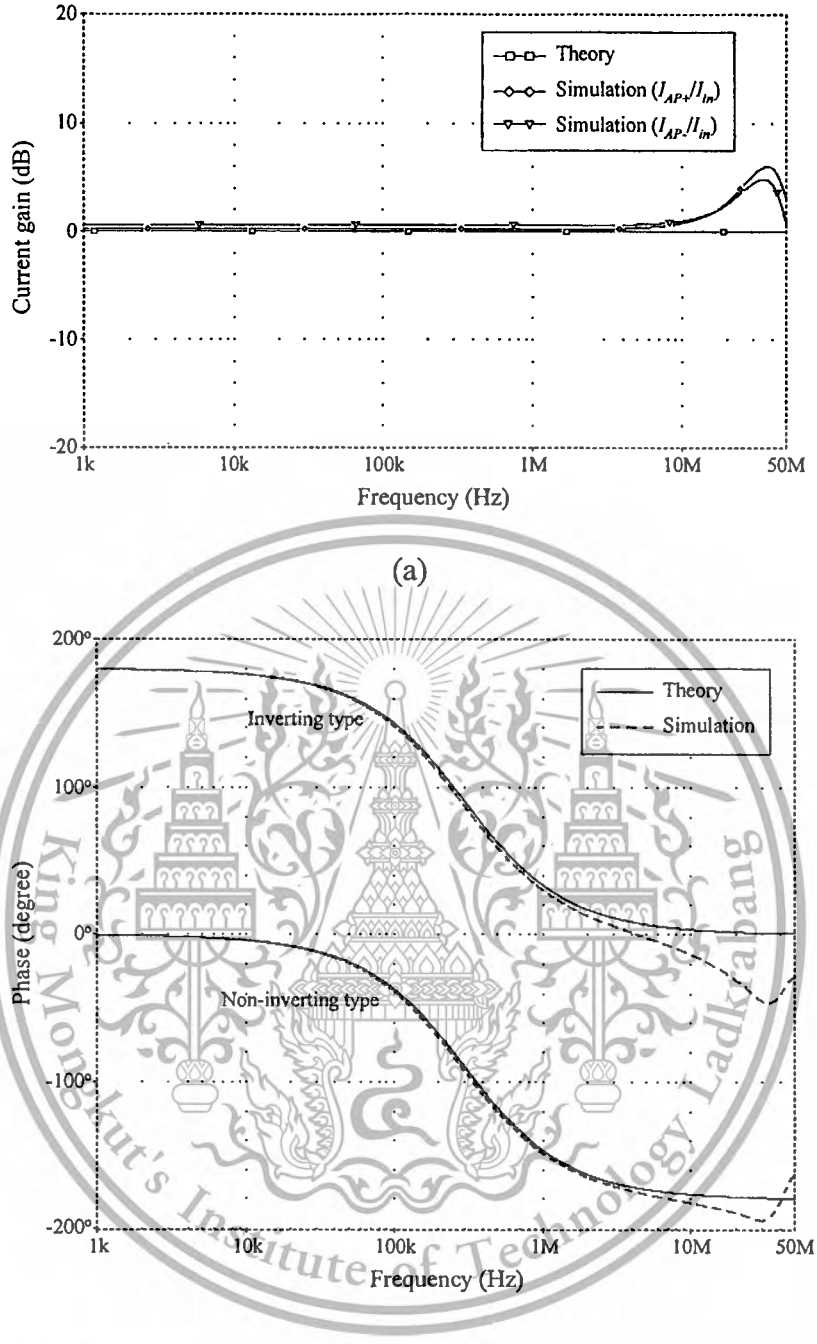

Figure 3.3 : Frequency responses of the presented allpass filter in figure 3.1.

(a) magnitude-frequency responses (b) phase-frequency responses

In figure 3.3, the simulated frequency domain responses of the proposed filters are also shown for the designed component values as previously given. The simulated phase-frequency plots of both types of the allpass filters for three different bias

current values are depicted in figure 3.4. It can be observed that the electronically controllability of the phase response can be achieved through adjusting I_{O1}.

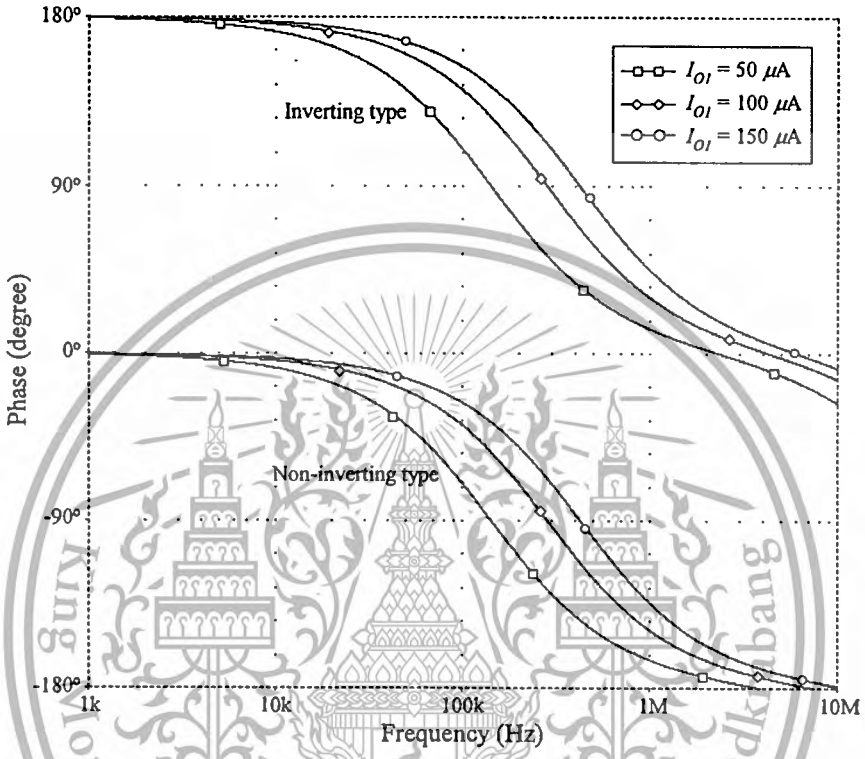

Figure 3.4 : Simulated phase responses when I_{o1} is varied.

With the above designed component values, the variation of the total power consumption with the pole frequency f_o for the proposed allpass filter of figure 3.1 is shown in figure 3.5. It is obvious from the curve that the total power consumption is found to be low and remains within 9 mW through the wide frequency range of 10 kHz-1 MHz. Thus, the results confirm the practical low-power operation of the circuit.

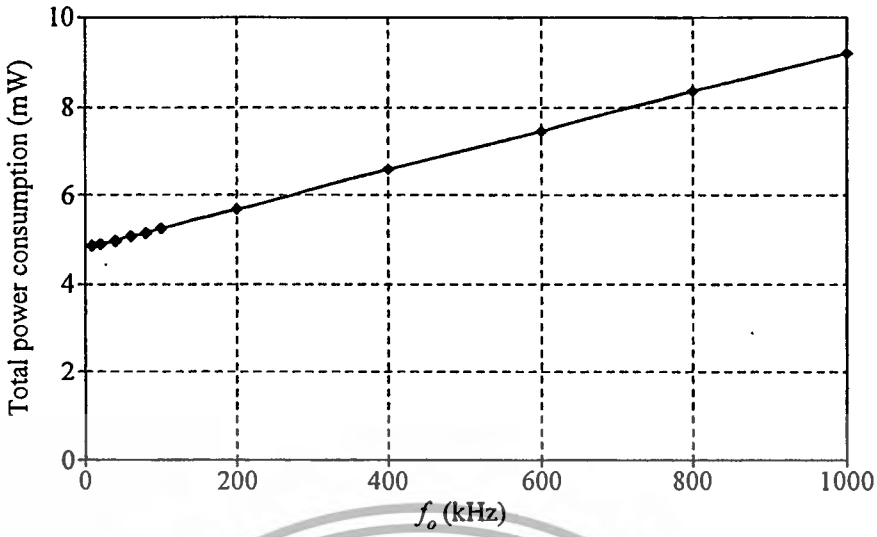

Figure 3.5 : Variation of total power consumption as a function of f_o.

3.6 Application to Current-Mode Quadrature Oscillator Realization

As an application example, a current-mode quadrature sinusoidal oscillator is realized by cascading the proposed allpass filter of figure 3.1 and the current lossless integrator (CDTA3 and C_2) of figure 2.9, and closing the circuit's loop to provide a unity loop gain at the pole frequency [21]. The resulting circuit is shown in figure 3.6. Complementary circuit analysis using equation (2.1) yields the characteristic equation of the circuit as the following relation :

$$s^2 + \left(\frac{g_{m1}}{C_1} - \frac{g_{m3}}{C_2} \right) s + \frac{g_{m1} g_{m3}}{C_1 C_2} = 0 \qquad (3.15)$$

From equation (3.15), the oscillation condition and the oscillation frequency (ω_o) obtained from the circuit can respectively be found as :

$$g_{m1} C_2 = g_{m3} C_1 \qquad (3.16)$$

and

$$\omega_o = \sqrt{\frac{g_{m1}g_{m3}}{C_1C_2}} \tag{3.17}$$

Furthermore, if setting $C_1 = C_2 = C$ and $g_{m1} = g_{m3} = g_m$, then the oscillator circuit of figure 3.6 can be controlled to oscillate at the oscillation frequency of

$$f_o = \frac{\omega_o}{2\pi} = \frac{g_m}{2\pi C} \tag{3.18}$$

Note from above equation that the frequency of oscillation can be controlled electronically by linearly adjusting the g_m -value.

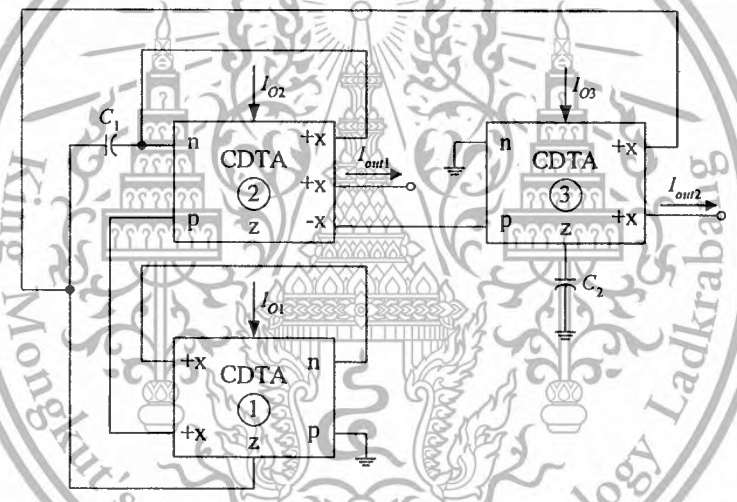

Figure 3.6 : Current-mode quadrature oscillator realized by cascading the proposed allpass filter and lossless integrator.

Also from figure 3.6, the relationship between two quadrature outputs I_{out1} and I_{out2} can be expressed as :

$$\frac{I_{out2}}{I_{out1}} = \frac{g_{m3}}{sC_2} \tag{3.19}$$

which shows that the phase difference (ϕ) between I_{o2} and I_{o1} is equal to $\phi = 90°$. This means that the current I_{out1} and I_{out2} are quadrature outputs.

Figure 3.7 shows simulated time domain responses of the quadrature output currents I_{out1} and I_{out2}, which demonstrates the 90° phase-shift waveforms. For this purpose, the designed component values are chosen as : $I_{O1} = I_{O2} = I_{O3} = I_O = 100$ μA and $C_1 = C_2 = C = 1$ nF, which results in the oscillation frequency of $f_o \cong 318$ kHz. Additionally, figure 3.8 also shows the simulated frequency spectrums of the quadrature outputs I_{out1} and I_{out2}. From the simulation results, the circuit gives the oscillation frequency as $f_o \cong 283$ kHz, and the total harmonic distortion (THD) is found as 1.69%. Also, the total power consumption is found to be less than 9.89 mW.

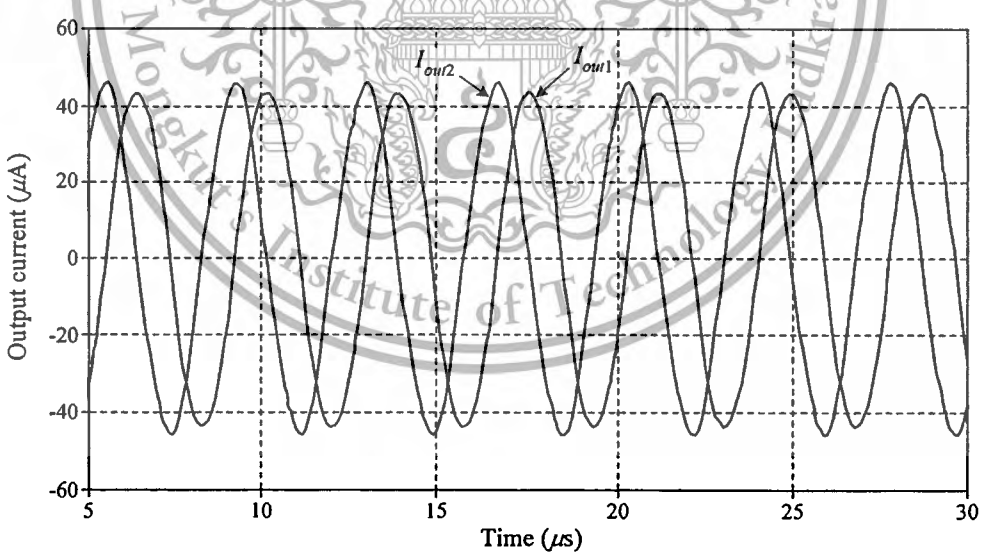

Figure 3.7 : Simulated waveforms of the quadrature outputs I_{out1} and I_{out2} of figure 3.6.

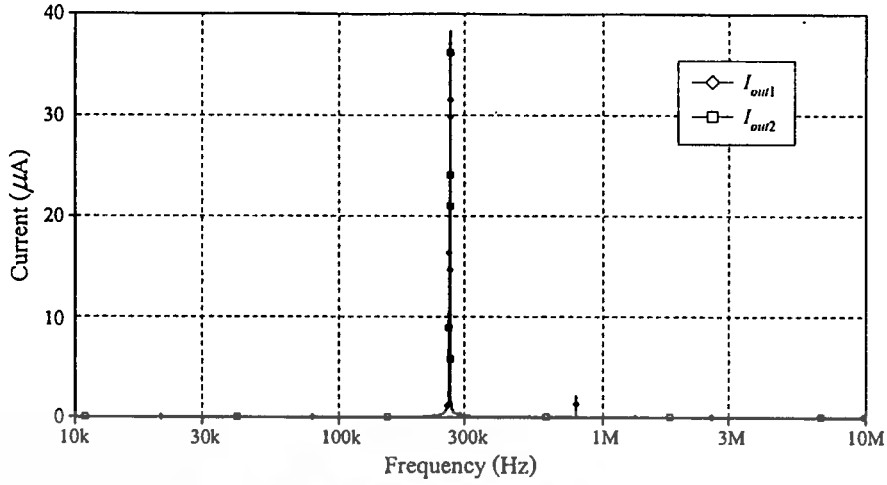

Figure 3.8 : Simulated spectrums of the quadrature outputs I_{out1} and I_{out2} of figure 3.6.

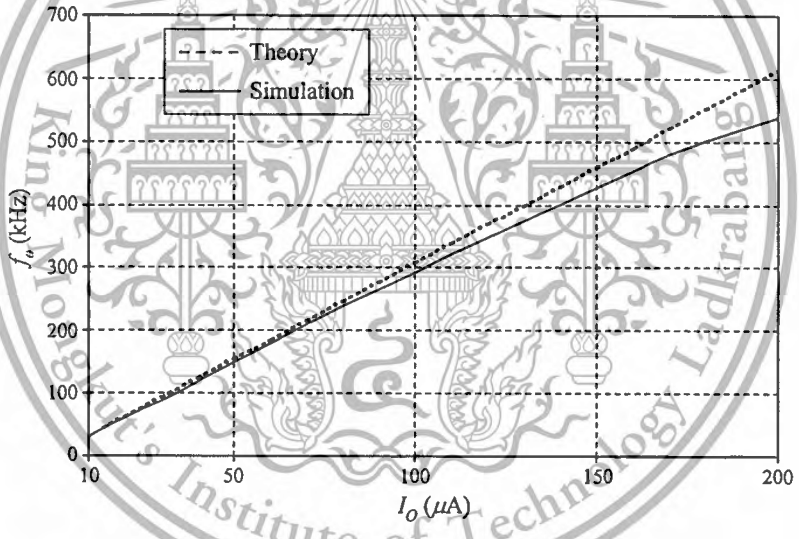

Figure 3.9 : Variation of f_o as a function of I_O.

The simulated oscillation frequency when I_O is varied is represented in figure 3.9. The deviations between the theoretical calculated from equation (3.18) and simulated values are less than 2%, 4%, 6% and 12% for I_O within the ranges 10-50 μA, 50-100 μA, 100-150 μA and 150-200 μA, respectively.

3.7 Conclusions

In this chapter, a canonical current-mode first-order allpass filter is presented. It can realize both inverting and non-inverting type allpass filtering functions by using only two CDTAs and one virtually grounded capacitor. The proposed circuit has following advantages : (i) the phase shift can be electronically tuned by an external bias current; (ii) no matching condition is imposed for realizing the allpass functions; (iii) since all the outputs are provided through high output impedance terminals, it can be directly connected to the next stage without any impedance matching requirement. The important features of the propose circuit are compared with those of previous works in table 3.1.

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CHAPTER 4

Structural Generation of Current-Mode Two Integrator Loop CDTA Filter Structures

4.1 Introduction

Two integrator loop structures are very popular and useful blocks to realize biquad filters [1]-[4]. Nawrocki and Klein proposed a two-integrator loop universal biquad with single-input and single-output using eight operational transconductance amplifiers (OTAs) and two grounded capacitors [1]. In 1988, Sanchez-Sinencio *et. al.* have systematically summarized and extended the work on the two-integrator loop OTA-C filters based on the block diagram method [2]. In [3], the author developed the Nawrocki and Klein biquad to derive many new filter structures. However, all the above mentioned methods are based on the voltage-mode approach. Moreover, some obtained filter structures in [2] need the capacitor injection of excitation signals in the circuit design, which are not suitable for cascade implementation, and the resulting floating capacitors are not suitable for integrated circuit (IC) implementation [5]-[6]. In 1996, a comprehensive set of current-mode continuous-time two integrator loop filter structures incorporating dual-output OTA (DO-OTA) and capacitors was developed in [4]. However, the structures also require capacitor injection of excitation signals, which do not exhibit the feature of low-impedance inputs.

Of the various methods of current-mode biquad filter design, those based upon second-generation current conveyors (CCIIs) have been reported in the literature [7]-[14]. However, most of them still require capacitor injection of input signal currents [7]-[9], [11], [13], [14], whereas the other also require an input current injection into the external grounded resistance or internal parasitic resistance connected at the input terminal [7]-[8], [10], [12], [13]. Thus, the low-input impedance characteristic is not recommended for these structures. Ideally, it is preferred that the current-mode filters should provide low-input and high-output impedances for easy cascadability to implement higher-order filter and generation of additional filter responses by simply connecting two or more responses.

Therefore, this chapter largely focuses on presenting a structural generation to synthesize the two integrator loop filters with CDTAs. The proposed configurations employ the current proportional blocks and current integrators based on using CDTAs as the basic building units. By suitably selecting the input and output currents, the derived filters can realize all the standard biquadratic filters, i.e., lowpass (LP), highpass (HP), bandpass (BP), bandstop (BS) and allpass (AP), from the same configuration. The resulting filter characteristics can be electronically adjusted with separate tunable transconductances. All the filter structures contain only grounded capacitors, which are helpful for easing the IC implementation. In addition, all the proposed filters exhibit both low-input and high-output impedance levels, thus permitting easy cascadability.

4.2 Generation of Two Integrator Loop CDTA Filter Structures

Basically, the two integrator loop structures consist of a lossless integrator and a lossy integrator. Figure 4.1 shows four different block diagram representations of the basic two-integrator loop operation that will be used to illustrate the proposed approach. Observe that figures 4.1(a) and 4.1(c) contain two negative-feedback loops including two lossless integrators ($1/s\tau_1$ and $1/s\tau_2$) and two proportional gain blocks (A_0, A_1 and A_0, A_2), while figures 4.1(b) and 4.1(d) contain a single negative-feedback loop consisting of one lossy integrator, one lossless integrator and one proportional gain block. In considering two-integrator loop configurations of figures 4.1(a) and 4.1(b), the characteristic equation is identical and can be given by [Appendix C.1]:

$$D_1(s) = s^2\tau_1\tau_2 + s\tau_2 A_1 + A_0 \tag{4.1}$$

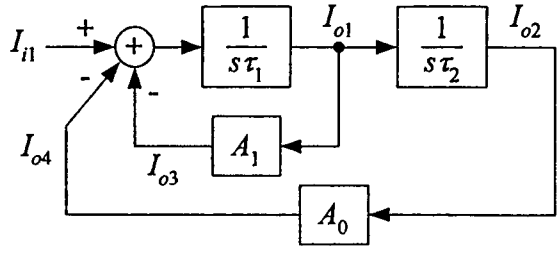
where τ_1 and τ_2 are the integrator time constants. Hence, the natural angular frequency (ω_o), bandwidth (BW) and quality factor (Q) for both configurations, respectively, become :

$$\omega_o = \sqrt{\frac{A_0}{\tau_1\tau_2}} \tag{4.2}$$

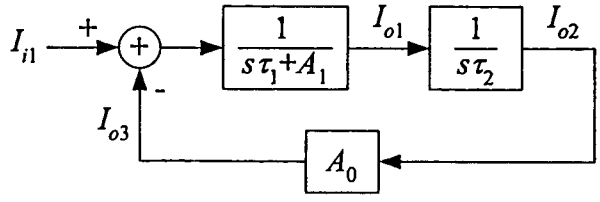
$$BW = \frac{A_1}{\tau_1} \tag{4.3}$$

and

$$Q = \frac{1}{A_1}\sqrt{\frac{A_0\tau_1}{\tau_2}} \quad . \tag{4.4}$$



(a)



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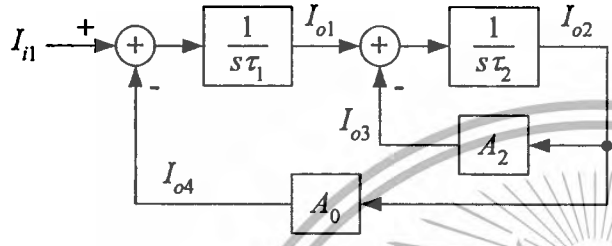
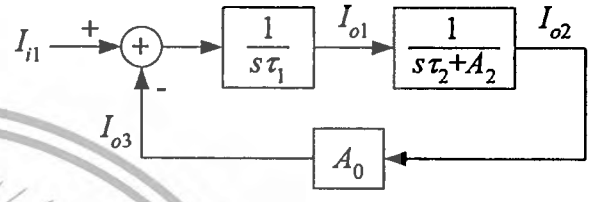


(c)



(d)

Figure 4.1 : Two integrator loop structures.

(a) Configuration A (b) Configuration B

(c) Configuration C (d) Configuration D

In a similar way, we can obtain the same characteristic equation for both two-integrator loop configurations of figures 4.1(c) and 4.1(d), written by [Appendix C.2]:

$$D_2(s) = s^2\tau_1\tau_2 + s\tau_1 A_2 + A_0 \quad . \tag{4.5}$$

The parameters ω_o, BW and Q are, respectively, obtained as :

$$\omega_o = \sqrt{\frac{A_0}{\tau_1\tau_2}} \tag{4.6}$$

$$BW = \frac{A_2}{\tau_2} \tag{4.7}$$

and

$$Q = \frac{1}{A_2}\sqrt{\frac{A_0\tau_2}{\tau_1}} \quad . \tag{4.8}$$

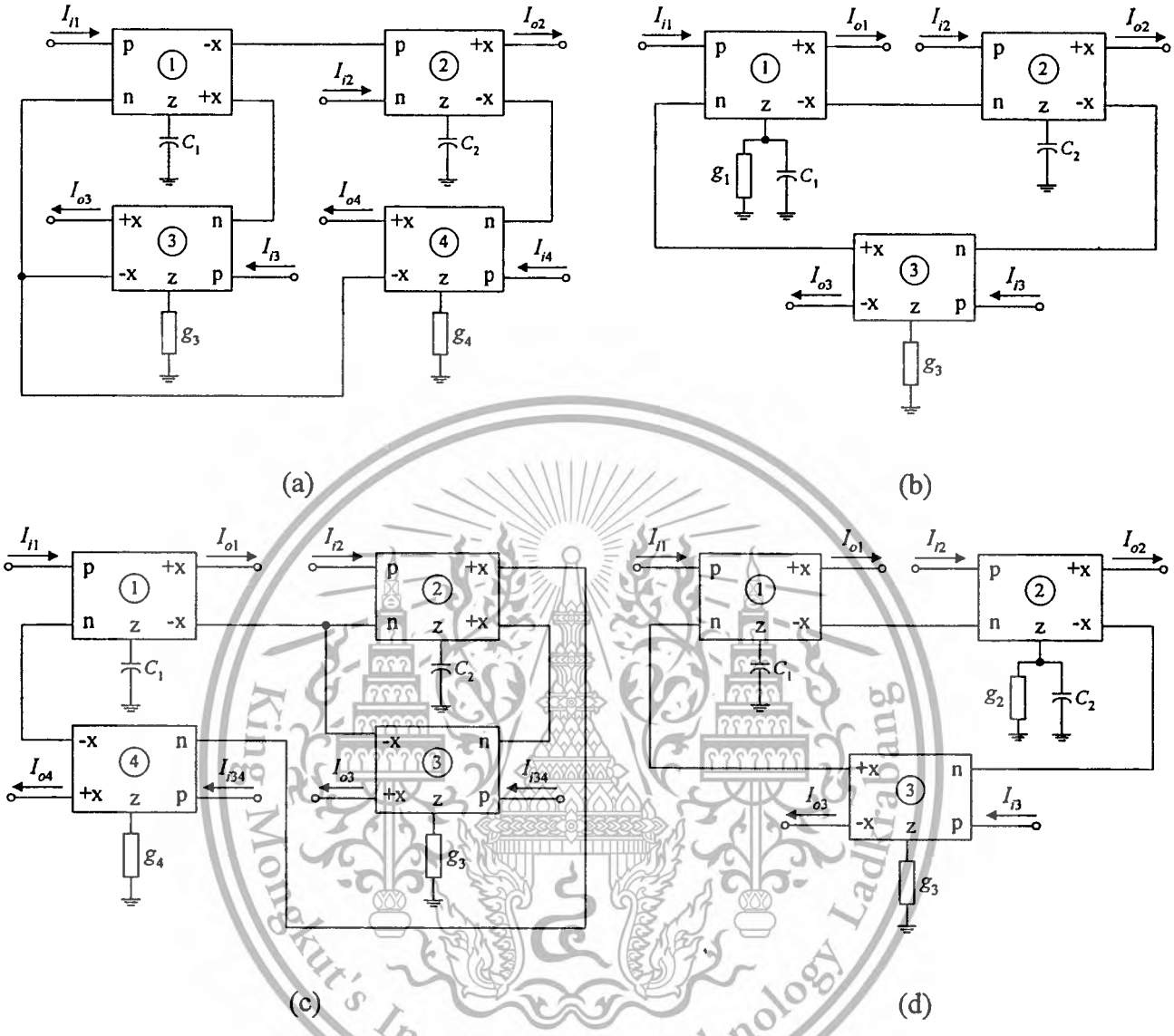


Figure 4.2 : Generation of CDTA-based biquadratic filter configurations based on two integrator loop structures of figure 4.1.

(a) Configuration A (b) Configuration B

(c) Configuration C (d) Configuration D

Let us now consider the CDTA-based circuit implementations of architectures of figure 4.1. By employing the CDTA-based basic current building blocks described in section 2.4, we can realize figure 4.1 in the current-mode domain. The corresponding circuits derived from four block diagram structures of figures 4.1(a)-4.1(d) are shown in figures 4.2(a)-4.2(d), respectively. The mathematical expressions for the corresponding parameters ω_o, BW and Q, given in equations (4.2)-(4.4) and (4.6)-(4.8), for all the derived realizations are summarized in table 4.1. All the possible current transfer functions derived from figures 4.2(a)-4.2(d) are formulated by the following expressions, where $D_1(s)$ and $D_2(s)$ are the same as in equations (4.1) and (4.5), respectively.

For figure 4.2(a), [Appendix D.1]

$$\left.\begin{aligned} I_{o2} &= \frac{-I_{i1}+(s\tau_1+A_1)I_{i2}-A_1I_{i3}-A_0I_{i4}}{D_1(s)} \\ I_{o3} &= \frac{-(s\tau_2A_1)I_{i1}+(A_0A_1)I_{i2}+A_1(s^2\tau_1\tau_2+A_0)I_{i3}-(s\tau_2A_0A_1)I_{i4}}{D_1(s)} \\ I_{o4} &= \frac{-A_0I_{i1}-A_0(s\tau_1+A_1)I_{i2}-(A_0A_1)I_{i3}-s\tau_2A_0(s\tau_1+A_1)I_{i4}}{D_1(s)} \\ I_{o3}+I_{o4} &= \frac{-(s\tau_2A_1+A_0)I_{i1}-(s\tau_1A_0)I_{i2}+(s^2\tau_1\tau_2A_1)I_{i3}+(s^2\tau_1\tau_2A_0)I_{i4}}{D_1(s)} \end{aligned}\right\} \quad (4.9)$$

For figure 4.2(b), [Appendix D.2]

$$\left.\begin{aligned} I_{o1} &= \frac{(s\tau_2)I_{i1} - A_0 I_{i2} - (s\tau_2 A_0)I_{i3}}{D_1(s)} \\ I_{o2} &= \frac{I_{i1} + (s\tau_1 + A_1)I_{i2} - A_0 I_{i3}}{D_1(s)} \\ I_{o3} &= \frac{A_0 I_{i1} + A_0(s\tau_1 + A_1)I_{i2} + s\tau_2 A_0(s\tau_1 + A_1)I_{i3}}{D_1(s)} \end{aligned}\right\} \quad (4.10)$$

For figure 4.2(c), [Appendix D.3]

$$\left.\begin{aligned} I_{o1} &= \frac{(s\tau_2 + A_2)I_{i1} - A_0 I_{i2} - (s\tau_2 A_0)I_{i34}}{D_2(s)} \\ I_{o3} &= \frac{-A_2 I_{i1} - (s\tau_1 A_2)I_{i2} + (s^2\tau_1\tau_2 A_2)I_{i34}}{D_2(s)} \\ I_{o4} &= \frac{-A_0 I_{i1} - (s\tau_1 A_0)I_{i2} + (s^2\tau_1\tau_2 A_0)I_{i34}}{D_2(s)} \end{aligned}\right\} \quad (4.11)$$

For figure 4.2(d), [Appendix D.4]

$$\left.\begin{aligned} I_{o1} &= \frac{(s\tau_2 + A_2)I_{i1} - A_0 I_{i2} - A_0(s\tau_2 + A_2)I_{i3}}{D_2(s)} \\ I_{o2} &= \frac{I_{i1} + (s\tau_1)I_{i2} - A_0 I_{i3}}{D_2(s)} \\ I_{o3} &= \frac{A_0 I_{i1} + (s\tau_1 A_0)I_{i2} + s\tau_1 A_0(s\tau_2 + A_2)I_{i3}}{D_2(s)} \end{aligned}\right\} \quad (4.12)$$

It should be noted from equations (4.9)-(4.12) that, by suitably connecting the input current terminals, all five standard biquadratic filtering signals can be realized. From equation (4.9), it can readily be seen that the proposed filter configuration of figure

Table 4.1 : Expressions for the filter parameters of figure 4.2.

Configuration	A_0	A_1	A_2	τ_1	τ_2	ω_o	BW	Q
Configuration A, figure 4.2(a)	$\frac{g_{m4}}{g_4}$	$\frac{g_{m3}}{g_3}$	--	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}g_{m4}}{g_4C_1C_2}}$	$\frac{g_{m1}g_{m3}}{g_3C_1}$	$\frac{g_3}{g_{m3}}\sqrt{\frac{g_{m2}g_{m4}C_1}{g_{m1}g_4C_2}}$
Configuration B, figure 4.2(b)	$\frac{g_{m3}}{g_3}$	$\frac{g_1}{g_{m1}}$	--	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}g_{m3}}{g_3C_1C_2}}$	$\frac{g_1}{C_1}$	$\frac{1}{g_1}\sqrt{\frac{g_{m1}g_{m2}g_{m3}C_1}{g_3C_2}}$
Configuration C, figure 4.2(c)	$\frac{g_{m4}}{g_4}$	--	$\frac{g_{m3}}{g_3}$	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}g_{m4}}{g_4C_1C_2}}$	$\frac{g_{m2}g_{m3}}{g_3C_2}$	$\frac{g_3}{g_{m3}}\sqrt{\frac{g_{m1}g_{m4}C_2}{g_{m2}g_4C_1}}$
Configuration D, figure 4.2(d)	$\frac{g_{m3}}{g_3}$	--	$\frac{g_2}{g_{m2}}$	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}g_{m3}}{g_3C_1C_2}}$	$\frac{g_2}{C_2}$	$\frac{1}{g_2}\sqrt{\frac{g_{m1}g_{m2}g_{m3}C_2}{g_3C_1}}$

4.2(a) can provide lowpass (LP), highpass (HP), bandpass (BP), bandstop (BS), and allpass (AP) current responses with different inputs and outputs. It is further noted from equation (4.9) that the output current $I_{o3} + I_{o4}$ can easily be obtained by connecting two corresponding terminals together. Equations (4.10) and (4.12) also show that the configurations in figure 4.2(b) and 4.2(d) realize LP and BP characteristics, while equation (4.11) indicates that figure 4.2(c) provides LP, HP and BP characteristics. It may be stated here that all of the above multifunction biquadratic filters can be realized without any constraints on the component values, and all the proposed configurations exhibit both low-input and high-output impedance characteristics, which will be more convenient in terms of cascading and connecting to other networks.

Furthermore, special types of CDTA-based biquadratic filters can be realized from figure 4.1 by appropriately setting the proportional gain $A_i = 1$ ($i = 0, 1$). Recall that when A_0 or A_1 becomes unity, they can simply be replaced by the short-circuit connection. The CDTA-based filter realizations derived from the configuration A of figure 4.1(a) with $A_0 = 1$, $A_1 = 1$ and $A_0 = A_1 = 1$ are respectively shown in figures 4.3(a)-4.3(c). The realizations of figures 4.3(d) and 4.3(e) are constructed with $A_0 = 1$ of figures 4.1(b) and 4.1(d), respectively. Table 4.2 summarizes the expressions for all the filter parameters for the derived structures obtained from figure 4.3. According to figures 4.3(a)-4.3(e), the explicit expressions for the current transfer functions can be derived as follows.

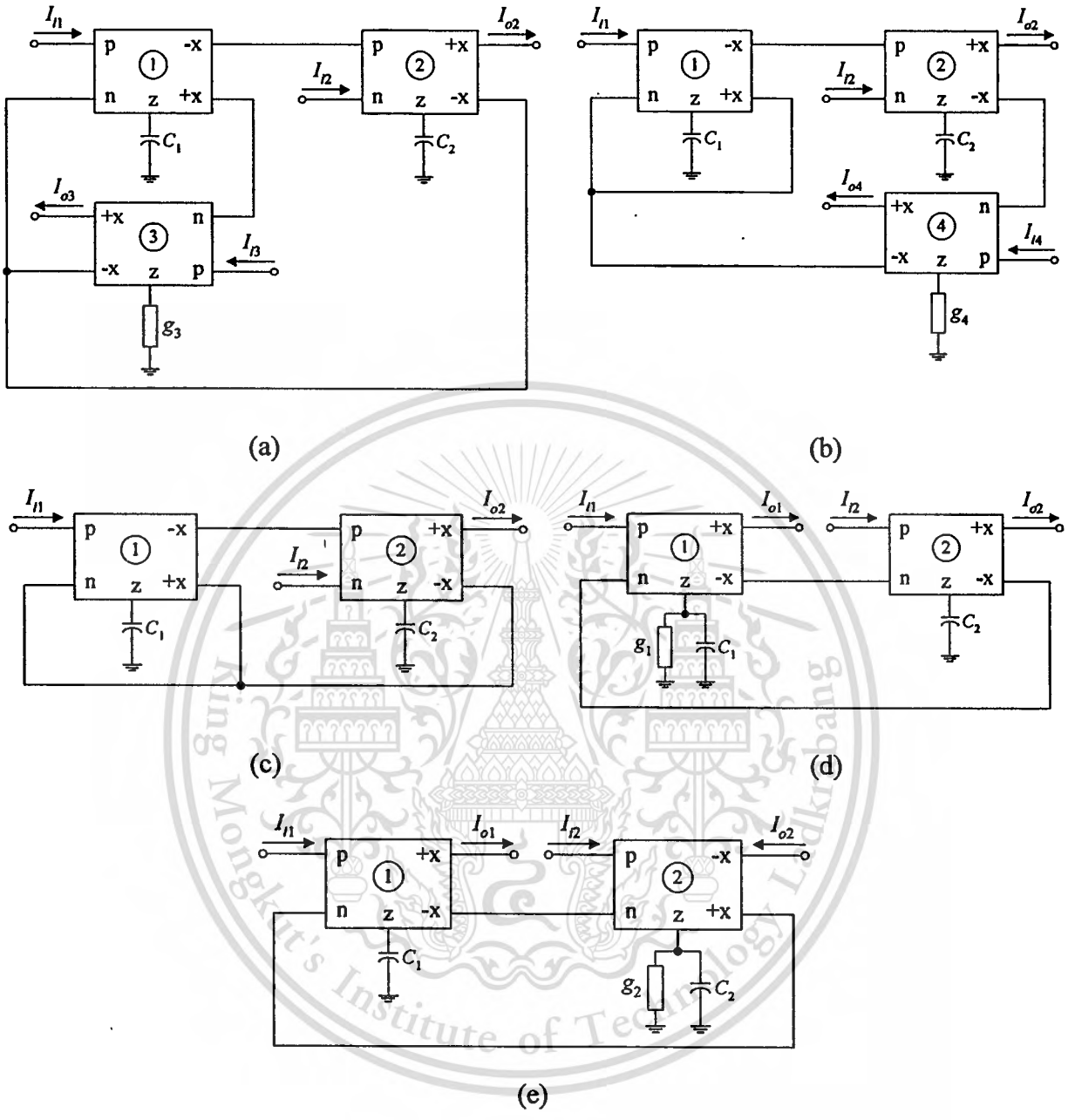


Figure 4.3 : Special types of CDTA-based biquadratic filters of figure 4.1.

(a) Configuration A (when $A_0 = 1$)

(b) Configuration A (when $A_1 = 1$)

(c) Configuration A (when $A_0 = A_1 = 1$)

(d) Configuration B (when $A_0 = 1$)

(e) Configuration D (when $A_0 = 1$)

For figure 4.3(a), [Appendix E.1]

$$\left.\begin{aligned} I_{o2} &= \frac{-I_{i1}-(s\tau_1+A_1)I_{i2}-A_1I_{i3}}{D_1(s)} \\ I_{o3} &= \frac{-(s\tau_2A_1)I_{i1}+A_1I_{i2}+A_1(s^2\tau_1\tau_2+1)I_{i3}}{D_1(s)} \\ I_{o2}+I_{o3} &= \frac{-(s\tau_2A_1+1)I_{i1}-(s\tau_1)I_{i2}+(s^2\tau_1\tau_2A_1)I_{i3}}{D_1(s)} \end{aligned}\right\} \quad (4.13)$$

For figure 4.3(b), [Appendix E.2]

$$\left.\begin{aligned} I_{o2} &= \frac{I_{i1}+(s\tau_1+1)I_{i2}-A_0I_{i4}}{D_1(s)} \\ I_{o4} &= \frac{-A_0I_{i1}-A_0(s\tau_1+1)I_{i2}-s\tau_2A_0(s\tau_1+1)I_{i4}}{D_1(s)} \end{aligned}\right\} \quad (4.14)$$

For figure 4.3(c), [Appendix E.3]

$$I_{o2} = \frac{-I_{i1}-(s\tau_1+1)I_{i2}}{D_1(s)} \quad (4.15)$$

For figure 4.3(d), [Appendix E.4]

$$\left.\begin{aligned} I_{o1} &= \frac{(s\tau_2)I_{i1}-I_{i2}}{D_1(s)} \\ I_{o2} &= \frac{I_{i1}+(s\tau_1+A_1)I_{i2}}{D_1(s)} \end{aligned}\right\} \quad (4.16)$$

For figure 4.3(e), [Appendix E.5]

$$\left.\begin{aligned} I_{o1} &= \frac{(s\tau_2+A_2)I_{i1}-I_{i2}}{D_2(s)} \\ I_{o2} &= \frac{I_{i1}+(s\tau_1)I_{i2}}{D_2(s)} \end{aligned}\right\} \quad (4.17)$$

Table 4.2 : Expressions for the filter parameters of figure 4.3.

Configuration	A_0	A_1	A_2	τ_1	τ_2	ω_0	BW	Q
Configuration A, ($A_0 = 1$) Figure 4.3(a)	1	$\frac{g_{m3}}{g_3}$	--	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$	$\frac{g_{m1}g_{m3}}{g_3C_1}$	$\frac{g_3}{g_{m3}}\sqrt{\frac{g_{m2}C_1}{g_{m1}C_2}}$
Configuration A, ($A_1 = 1$) Figure 4.3(b)	$\frac{g_{m4}}{g_4}$	1	--	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}g_{m4}}{g_4C_1C_2}}$	$\frac{g_{m1}}{C_1}$	$\sqrt{\frac{g_{m2}g_{m4}C_1}{g_{m1}g_4C_2}}$
Configuration A, ($A_0 = A_1 = 1$) Figure 4.3(c)	1	1	--	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$	$\frac{g_{m1}}{C_1}$	$\sqrt{\frac{g_{m2}C_1}{g_{m1}C_2}}$
Configuration B, ($A_0 = 1$) Figure 4.3(d)	1	$\frac{g_1}{g_{m1}}$	--	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$	$\frac{g_1}{C_1}$	$\frac{1}{g_1}\sqrt{\frac{g_{m1}g_{m2}C_1}{C_2}}$
Configuration D, ($A_0 = 1$) Figure 4.3(e)	1	--	$\frac{g_2}{g_{m2}}$	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$	$\frac{g_2}{C_2}$	$\frac{1}{g_2}\sqrt{\frac{g_{m1}g_{m2}C_2}{C_1}}$

Clearly, equation (4.13) shows that the realization of LP, BP, HP, and BS functions can be obtained from figure 4.3(a) by connecting the appropriate terminals. In a similar way, equations (4.14)-(4.17) indicate that the realizations can directly offer LP and BP functions.

From the mathematical expressions in tables 4.1 and 4.2, we can see that the filter characteristics (ω_o, BW and Q) provide electronic tunability through an adjustment of the associated transconductance g_{mi} of the CDTA. From table 4.1, it can be seen that, for all the proposed configurations in figure 4.2, the quality factor Q can be controlled without disturbing the natural angular frequency ω_o. Hence, all the configurations of table 4.1 support an independent electronic-control of Q and ω_o. Similarly, it can also be seen in table 4.2 that the proposed configurations of figures 4.3(a), 4.3(d) and 4.3(e) enjoy independent control of the parameters Q and ω_o.

4.3 Sensitivity Analysis

As mentioned previously in section 3.4, the incremental sensitivities of the filter parameters G (= ω_o, BW, Q) to the element of variation x (= g_i, g_{mi}, C_i) may be defined as :

$$S_x^G = \left(\frac{x}{G}\right)\left(\frac{\partial G}{\partial x}\right) \tag{4.18}$$

Thus, using this definition, the sensitivities for the configurations in figures 4.2 and 4.3 with respect to transconductances g_i, g_{mi}, and capacitors C_1, C_2 are calculated as

either 0, or ±0.5, or ±1. This implies that the proposed filter configurations have low active and passive sensitivities.

4.4 Analysis of Non-ideal Effects

In practical sense, the performance of the proposed circuits may deviate from the ideal by the non-ideal characteristic of the CDTA being used. For the non-ideal case, the terminal relations of the CDTA describing in equation (2.1) can be rewritten by equation (2.2) and repeated here as :

$$v_p = v_n = 0 \quad , \quad i_z = \alpha_p i_p - \alpha_n i_n \quad \text{and} \quad i_x = \beta g_m v_z = \beta g_m Z_z i_z \qquad (4.19)$$

Therefore, using the above equation, all the proposed configurations of figures 4.2 and 4.3 are reanalyzed and the mathematical expressions for the non-ideal filter parameters are respectively illustrated in tables 4.3 and 4.4, where α_{pi}, α_{ni} and β_i are the parameters α_p, α_n and β of the i-th CDTA ($i = 1, 2, 3, 4$).

From tables 4.3 and 4.4, it can be observed that the tracking errors of the CDTA may cause small deviations of the values of the filter parameters. However, these deviations should not be seen as a drawback, as we can compensate these effects as low as possible by appropriately tuning transconductance values. Also from tables 4.3 and 4.4, and according to equation (4.18), the sensitivity analysis of the filter characteristics with respect to the CDTA tracking errors can be calculated, and reveals that they are found to be not more than unity in magnitude.

Table 4.3 : Expressions for the non-ideal filter parameters of figure 4.2.

Configuration	ω_o	BW	Q
Configuration A, figure 4.2(a)	$\sqrt{\frac{g_{m1}g_{m2}g_{m4}\alpha_{n1}\alpha_{n4}\alpha_{p2}\beta_1\beta_2\beta_4}{g_4C_1C_2}}$	$\frac{g_{m1}g_{m3}\alpha_{n1}\alpha_{n3}\beta_1\beta_3}{g_3C_1}$	$\left(\frac{g_3}{g_{m3}\alpha_{n3}\beta_3}\right)\sqrt{\frac{g_{m2}g_{m4}C_1\alpha_{n4}\alpha_{p2}\beta_2\beta_4}{g_{m1}g_4C_2\alpha_{n1}\beta_1}}$
Configuration B, figure 4.2(b)	$\sqrt{\frac{g_{m1}g_{m2}g_{m3}\alpha_{n1}\alpha_{n2}\alpha_{n3}\beta_1\beta_2\beta_3}{g_3C_1C_2}}$	$\frac{g_1}{C_1}$	$\frac{1}{g_1}\sqrt{\frac{g_{m1}g_{m2}g_{m3}C_1\alpha_{n1}\alpha_{n2}\alpha_{n3}\beta_1\beta_2\beta_3}{g_3C_2}}$
Configuration C, figure 4.2(c)	$\sqrt{\frac{g_{m1}g_{m2}g_{m4}\alpha_{n1}\alpha_{n2}\beta_1\beta_2\beta_4}{g_4C_1C_2}}$	$\frac{g_{m2}g_{m3}\alpha_{n2}\alpha_{n3}\beta_2\beta_3}{g_3C_2}$	$\left(\frac{g_3}{g_{m3}\alpha_{n3}\beta_3}\right)\sqrt{\frac{g_{m1}g_{m4}C_2\alpha_{n1}\beta_1\beta_4}{g_{m2}g_4C_1\alpha_{n2}\beta_2}}$
Configuration D, figure 4.2(d)	$\sqrt{\frac{g_{m1}g_{m2}g_{m3}\alpha_{n1}\alpha_{n2}\alpha_{n3}\beta_1\beta_2\beta_3}{g_3C_1C_2}}$	$\frac{g_2}{C_2}$	$\frac{1}{g_2}\sqrt{\frac{g_{m1}g_{m2}g_{m3}C_2\alpha_{n1}\alpha_{n2}\alpha_{n3}\beta_1\beta_2\beta_3}{g_3C_1}}$

Table 4.4 : Expressions for the non-ideal filter parameters of figure 4.3.

Configuration	ω_o	BW	Q
Configuration A, ($A_0 = 1$) figure 4.3(a)	$\sqrt{\frac{g_{m1}g_{m2}\alpha_{n1}\alpha_{p2}\beta_1\beta_2}{C_1C_2}}$	$\frac{g_{m1}g_{m3}\alpha_{n1}\alpha_{n3}\beta_1\beta_3}{g_3C_1}$	$\left(\frac{g_3}{g_{m3}\alpha_{n3}\beta_3}\right)\sqrt{\frac{g_{m2}C_1\alpha_{p2}\beta_2}{g_{m1}C_2\alpha_{n1}\beta_1}}$
Configuration A, ($A_1 = 1$) figure 4.3(b)	$\sqrt{\frac{g_{m1}g_{m2}g_{m4}\alpha_{n1}\alpha_{p2}\alpha_{p4}\beta_1\beta_2\beta_4}{g_4C_1C_2}}$	$\frac{g_{m1}\alpha_{n1}\beta_1}{C_1}$	$\sqrt{\frac{g_{m2}g_{m4}C_1\alpha_{p2}\alpha_{p4}\beta_2\beta_4}{g_{m1}g_4C_2\alpha_{n1}\beta_1}}$
Configuration A, ($A_0 = A_1 = 1$) figure 4.3(c)	$\sqrt{\frac{g_{m1}g_{m2}\alpha_{n1}\alpha_{p2}\beta_1\beta_2}{C_1C_2}}$	$\frac{g_{m1}\alpha_{n1}\beta_1}{C_1}$	$\sqrt{\frac{g_{m2}C_1\alpha_{p2}\beta_2}{g_{m1}C_2\alpha_{n1}\beta_1}}$
Configuration B, ($A_0 = 1$) figure 4.3(d)	$\sqrt{\frac{g_{m1}g_{m2}\alpha_{n1}\alpha_{n2}\beta_1\beta_2}{C_1C_2}}$	$\frac{g_1}{C_1}$	$\frac{1}{g_1}\sqrt{\frac{g_{m1}g_{m2}C_1\alpha_{n1}\alpha_{n2}\beta_1\beta_2}{C_2}}$
Configuration D, ($A_0 = 1$) figure 4.3(e)	$\sqrt{\frac{g_{m1}g_{m2}\alpha_{n1}\alpha_{n2}\beta_1\beta_2}{C_1C_2}}$	$\frac{g_2}{C_2}$	$\frac{1}{g_1}\sqrt{\frac{g_{m1}g_{m2}C_2\alpha_{n1}\alpha_{n2}\beta_1\beta_2}{C_1}}$

4.5 Effects of Parasitic Impedances

This section presents a study on the effects of parasitic impedances of the CDTA used in the proposed filters. A non-ideal CDTA model including parasitic resistors and capacitors, which is explained in section 2.2.2 and shown in figure 2.2, is employed [15]-[17]. Therefore, taking into account the CDTA parasitics with $\alpha_p = \alpha_n = \beta \cong 1$, the frequency range of operation for the proposed filters can be considered as follows.

Firstly, consider each z terminal of the CDTA in the proposed configurations of figures 4.2 and 4.3 which are terminated with the external grounded impedances. It is to be noted that the frequency responses of the filters strongly depend on the external grounded impedances and the parasitic impedances at the z terminal. Therefore, the filter frequency responses associated with this influence can be summarized as three following cases.

Case 1) Consider the case of a parallel impedance $R_i//C_k$ connected at the terminal z, where $R_i = 1/g_i$ and $k = 1, 2$. In the practical CDTA, the parasitic resistance R_z is normally much greater than the value of R_i ($R_z >> R_i$), while the parasitic capacitance C_z is very much smaller than the grounded capacitance C_k ($C_z << C_k$). Hence, in this case, it can be evaluated that the parasitic impedances of the z terminal are not found to severely affect the filter performance.

Case 2) If a grounded capacitor C_k is connected at the terminal z of the CDTA, there is a low-frequency limitation due to the capacitor C_k and the z terminal parasitic resistance R_z. In this case, the frequency range at low frequencies can be defined as :

$$f \geq \left(\frac{1}{2\pi R_z C_k} \right) = f_{L1} \tag{4.20}$$

Case 3) If a grounded resistor R_i is connected at the terminal z, the high-frequency range of operation is limited by this resistor and the z terminal parasitic capacitance C_z. Thus, the high-frequency limitation of the filters can be defined as :

$$f \leq \left(\frac{1}{2\pi R_i C_z} \right) = f_{H1} \tag{4.21}$$

Secondly, consider the n and x terminals in Figs.4.2 and 4.3 which are connected together. It should be mentioned that there are double x terminals connected to the n terminal, and a single x terminal connected to the n terminal of the CDTA. Here, two cases for determining the frequency responses of the proposed filters can be considered.

Case 1) Consider the configurations A and C, where the n terminal is connected with two x terminals. In this case, the parasitic resistance R_n will connect in parallel with the parasitic impedances at two x terminals, i.e. $(R_n//R_x//R_x//2C_x)$. Since $R_n << R_x$, the pole frequency that limits the high-frequency operation of these filters can thus be approximated to

$$f \leq \left(\frac{1}{4\pi R_n C_x} \right) = f_{H2} \tag{4.22}$$

Case 2) Consider the configurations B and D, where each n terminal is directly connected with only x terminal. In this case, the maximum frequency attributed to the parasitic resistance R_n and the parasitic impedances at the x terminal ($R_x//C_x$) can be given by

$$f \le \left(\frac{1}{2\pi R_n C_x} \right) = f_{H3} \tag{4.23}$$

Finally, to achieve ideal responses, the frequency range of operation of the proposed configurations A and C should be restricted to the following conditions [18]

$$f \le f_{H(A,C)} = 0.1 \times \min\{f_{H1}, f_{H2}\} \tag{4.24}$$

and

$$f \ge f_L = 10 \times \max\{f_{L1}\} \tag{4.25}$$

or it can be conclude that the overall frequency range of the configurations A and C can be defined as $f_L \le f \le f_{H(A,C)}$.

Similarly, for a proper operation at high frequencies, the operating frequency of the proposed configurations B and D should be selected as

$$f \le f_{H(B,D)} = 0.1 \times \min\{f_{H1}, f_{H3}\} \tag{4.26}$$

Therefore, the overall frequency range of these configurations can be defined as $f_L \le f \le f_{H(B,D)}$.

4.6 Simulation Results

To confirm the theoretical analysis, the proposed circuits were simulated by PSPICE program. At present, there are several techniques to implement the CDTA

active element in IC form. Nevertheless, the simulation results reported here were obtained by using the CMOS realization of the CDTA proposed in [19], and already shown in figure 2.6. This realization, design details of which are also given in section 2.3.1.4, was adopted because it provides very low-input impedances at the p and n terminals (i.e., $r_p = r_n \cong 1.92\ \Omega$), and very high frequency operation. To perform the CDTA element in simulations, TSMC 0.35-μm n-well CMOS process was performed with dimensions of NMOS and PMOS transistors as that of [19]. The supply voltage are $\pm V = \pm 1.8V$, and the bias current is $I_B = 40\ \mu A$.

As an example, the proposed circuit of figure 4.2(a) was designed with the transconductance values of $g_{mi} = g_i = 0.88$ mA/V and the capacitance values of $C_1 = C_2 = 10$ pF. This setting was selected to obtain the LP, BP and HP filters with unity gain at $f_o = \omega_o/2\pi \cong 14$ MHz and $Q = 1$. Figure 4.4 illustrates the simulated magnitude frequency responses, which are the same as expected characteristics. From the simulation results, the power dissipation is approximately 19 mW.

To test the large signal behavior of the proposed filter, the total harmonic distortion (THD) at the output of the BP response for sinusoidal input signal of 14 MHz was obtained. The THD results are depicted in figure 4.5, which clearly shows that the percentage THD (%THD) is low and remains within acceptable limits of 4% till input current of 200 μA.

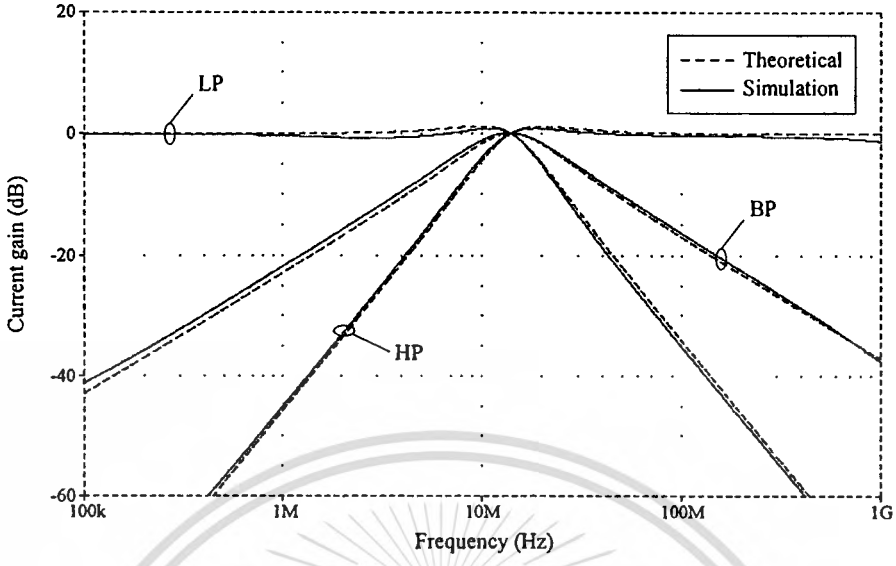


Figure 4.4 : Theoretical and simulation frequency plots for LP, BP and HP characteristics of figure 4.2 (a).

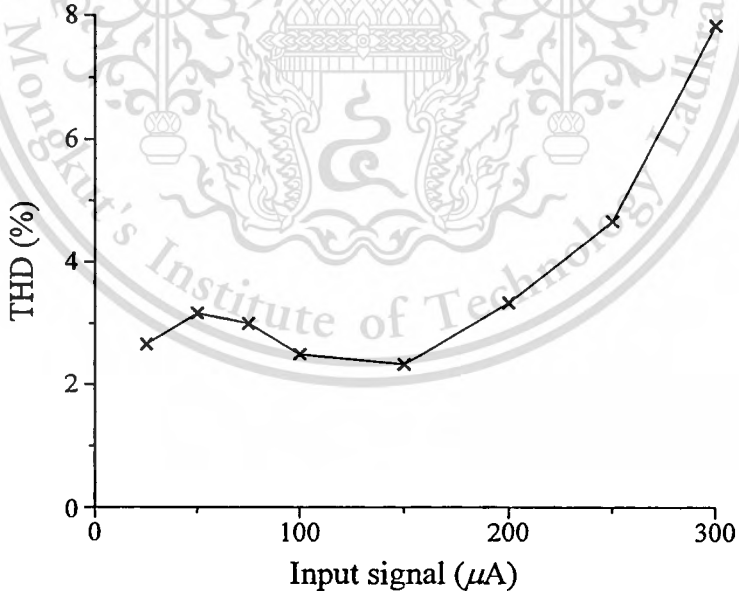


Figure 4.5 : Dependence of %THD on the input signal amplitude of BP filter.

4.7 Conclusions

In this chapter, an approach for the structural generation of two integrator loop filters using CDTAs and grounded capacitors has been presented. All of the proposed filters have the following advantages :

(i) realization of all standard biquadratic filtering functions;

(ii) making the filter characteristics electronically tunable in frequency response using external bias current;

(iii) the capacitors in the structures are all grounded, which are highly suitable for integrated implementation;

(iv) cascading can easily be achieved since they have low-input and high-output impedance characteristics;

(v) low sensitivity performance.

On the whole, this approach is convenient for monolithic integration, and suitable for cascading and electronic tuning.

4.8 References

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CHAPTER 5

Conclusions and Suggestions

5.1 Summary and Discussions

In summary, this thesis deals with the analog current-mode filter design and resistorless realization with the implementation of the current differencing transconductance amplifier (CDTA), which is newly reported active circuit building block. For the CDTA device, it is realized through the cascade connection of a current differencing circuit and a multiple-output operational transconductance amplifier (MO-OTA). Some novel applications on the continuous-time current-mode filter realized with CDTAs as active elements and grounded capacitors as passive elements were developed.

The first developed circuit is the resistorless current-mode first-order allpass filter section as shown in figure 3.1. It uses only two CDTAs and one virtually grounded capacitor, which is a very simple structure and is a canonic design. When compared with other similar circuits reported in technical literature, this design is better in that it uses fewer components and gives both inverting and non-inverting types of first-order allpass filter functions. Its phase response can be tuned electronically. Another benefit offered by the circuit is that it provides high-output impedance.

In the second developed filter structures, a versatile family of two integrator loop filter structures using CDTAs and grounded capacitors is generated. The basic filter building blocks consist of current proportional blocks, current lossless integrators and a current lossy integrator based on the use of CDTAs as the major active components. It is demonstrated that the derived filter structures can realize a general class of second-order current transfer functions. Since the resulting structures contain only CDTAs and grounded capacitors, they are general and very appropriate for integration, cascading and electronic tuning. All the filter structures provide both low-input and high-output impedances. The influences of the CDTA non-idealities on the filter performance are also studied.

In the circuits using CDTAs developed in this thesis, the important parametrs, which are the natural angular frequency (ω_o), bandwidth (BW) and quality factor (Q), are electronically tunable through the g_m-value, and the tunability extends in a linear manner over four decade. This is quite an effective range and gives most of the practical coverage in the filter circuits in which these are supposed to work.

All the proposed circuits employ the grounded capacitors, which is one of the fundamental requirements of the current-mode circuits. The use of grounded capacitors has the merit that they occupy lesser chip area and thus results in an increased component density.

Moreover, all the developed filters have been found to exhibit excellent circuit behavior with respect to active and passive sensitivities. Sensitivity is one of the main

parameters of electronic circuits, as it determines the stability of performance that in many cases is very essenstial. In all the circuits presented in the thesis, this parameter is quite satisfactory. They have all the sensitivities of ω_o, BW and Q less than or equal unity in magnitude. These figures are generally the values in which most of the works reported at international level in the literature lie. This means that the research produced meets this international criteria.

Finally, all the filter circuits developed in this thesis were tested through simulation, and produces the responses that agree with the presented theory; thereby confirming the truth of the concept leading to the development of these circuits.

5.2 Scope of Future Work

In this section, some comments and suggestions are presented, which may facilitate further work.

The transconductance (g_m) of the CDTA is temperature dependent. In some circuit designs, the g_ms of the CDTAs appear in the ratio form, and hence cancel out. However, in some circuits, this is not the case, and the g_ms appear without canceling each other. In such cases, there remains the possibility of parameter variation as the temperature changes. Therefore, a suggestion for further work may be to go for the design of these circuits with a modified architecture so that the whole structure becomes temperature independent. Another suggestion is to add temperature compensation to such the designs.

In the case of the resistorless CDTA-based current-mode first-order allpass filter shown in figure 3.1, it has been shown that the circuit operated in current-mode only. Hence, a simple suggestion one is, of course, that the improvement of the allpass section in figure 3.1 should be further developed and investigated in order to create a mixed-mode (voltage/current/trans-impedance/trans-admittance) allpass filter using CDTA. A resistorless CDTA-based mixed-mode allpass filter seems to be a more interesting circuit.

As can be observed from all the circuit configurations developed in the thesis, we found that the current differencing property at an input of the CDTA can be achieved by the negative current feedback connection via the -x terminal. This implies that the n terminal of the CDTA is unnecessary in these designs. Thus, in all the circuit configurations, the newly reported active building block so-called current follower transconductance amplifier (CFTA) can be used instead of CDTA. The CFTA can be thought of as a combination of the current follower and the multi-output operational transconductance amplifier. Its behavior is quite similar to the CDTA element, in which the current follower is used instead of the current differencing unit at the input stage. As a result, all the resulting circuits can reduce hardware and power consumption. It is also advantageous in terms of saving chip area from the point of view of integrated circuit implementation.

APPENDIX A

A.1 TSMC SPICE Model Parameters for Level 3, 0.35 μm n-well CMOS Real Process Parameters

TSMC (Taiwan Semiconductor Manufacturing Company, Ltd.)

NMOS TRANSISTOR

```
.MODEL  MN   NMOS
+ LEVEL=3  TOX=7.9E-9  NSUB=1E+17  GAMMA=0.5827871  PHI=0.7
+ VTO=0.5445549  DELTA=0  UO=436.256147  ETA=0  THETA=0.1749684
+ KP=2.055786E-4  VMAX=8.309444E+4  KAPPA=0.2574081  RSH=0.0559398
+ NFS=1E+12  TPG=1  XJ=3E-7  LD=3.162278E-11  WD=7.046724E-8
+ CGDO=2.83E-10  CGSO=2.82E-10  CGBO=1E-10  CJ=1E-03  PB=0.9758533
+ MJ=0.3448504  CJSW=3.777852E-10  MJSW=0.3508721
```

PMOS TRANSISTOR

```
.MODEL  MP   PMOS
+ LEVEL=3  TOX=7.9E-9  NSUB=1E+17  GAMMA=0.4083894  PHI=0.7
+ VTO=-0.7140674  DELTA=0  UO=212.2319801  ETA=9.999762E-4
+ THETA=0.2020774  KP=6.733755E-5  VMAX=1.181551E+5  KAPPA=1.5
+ RSH=30.0712458  NFS=1E+12  TPG=-1  XJ=2E-7  LD=5.000001E-13
+ WD=1.249872E-7  CGDO=3.09E-10  CGSO=3.09E-10  CGBO=1E-10
+ CJ=1.419508E-03  PB=0.8152753  MJ=0.5  CJSW=4.813504E-10  MJSW=0.5
```

A.2 AT&T ALA400-CBICR Models Typical Case 8/31/87 Revision 1

NPN TRANSISTOR

```
* NR100N-1X  NPN TRANSISTOR
.MODEL NX1 NPN  RB=524.6  IRB=0  RBM=25  RC=50  RE=1
+ IS=121E-18  EG=1.206  XTI=1.538  XTB=1.538  BF=137.5
+ IKF=6.974E-3  NF=1  VAF=159.4  ISE=36E-16  NE=1.713
+ BR=0.7258  IKR=2.198E-3  NR=1  VAR=10.73  ISC=0  NC=2
+ TF=0.425E-9  TR=0.425E-8  CJE=0.214E-12  VJE=0.5
+ MJE=0.28  CJC=0.983E-13  VJC=0.5  MJC=0.3  XCJC=0.034
+ CJS=0.913E-12  VJS=0.64  MJS=0.4  FC=0.5
```

PNP TRANSISTOR

```
* PR100N-1X  PNP  TRANSISTOR
.MODEL P PNP  RB=327  IRB=0  RBM=24.55  RC=50  RE=3
+ IS=73.5E-18  EG=1.206  XTI=1.7  XTB=1.866  BF=110.0
+ IKF=2.359E-3  NF=1  VAF=51.8  ISE=24.1E-16  NE=1.650
+ BR=0.4745  IKR=6.478E-3  NR=1  VAR=9.96  ISC=0  NC=2
+ TF=0.610E-9  TR=0.610E-8  CJE=0.180E-12  VJE=0.5
+ MJE=0.28  CJC=0.164E-12  VJC=0.8  MJC=0.4  XCJC=0.037
+ CJS=1.03E-12  VJS=0.55  MJS=0.35  FC=0.5
```

APPENDIX B

B.1 Current Transfer Function of First-Order Allpass Section of Figure 3.1

Consider the circuit configuration of figure B.1. It can be seen that CDTA1 performs the current-variable resistor as explained in section 2.4.1, and CDTA2 is now connected as the current differencer. Therefore, the current transfer function characteristic of the circuit can be derived as follows.

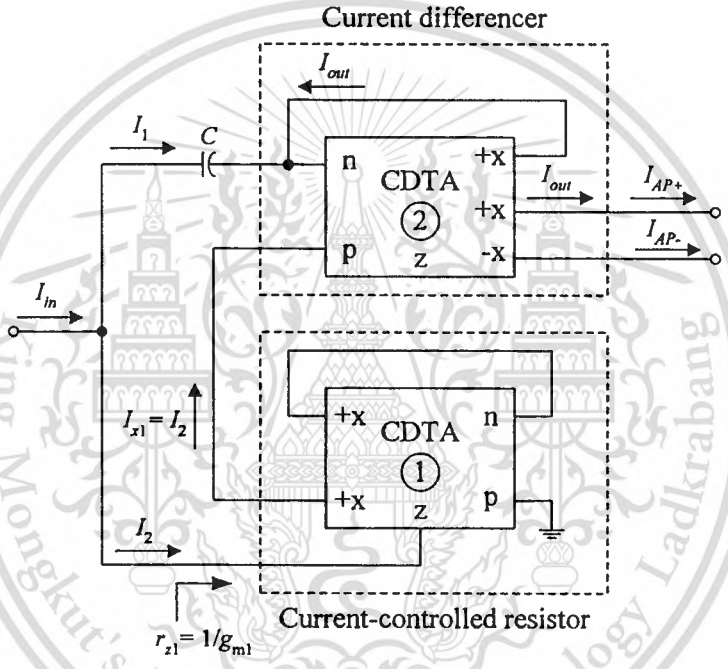


Figure B.1 : Configuration for determining the current transfer function of figure 3.1.

Owing to the CDTA1 performs as a grounded resistance simulation circuit; its input resistance looking into the z-terminal (r_{z1}) is thus equal to

$$r_{z1} = \frac{1}{g_{m1}} \tag{B.1}$$

Considering $I_2 = -i_{z2} = i_{n2} = i_{x2}$, and applying the current division at an input node, the currents I_1 and I_2 are

$$I_1 = \left[\frac{\frac{sC}{g_{m1}}}{1+\frac{sC}{g_{m1}}}\right] I_{in} \tag{B.2}$$

and

$$I_2 = \left[\frac{1}{1+\frac{sC}{g_{m1}}}\right] I_{in} \tag{B.3}$$

where g_m is the transconductance gain of the i-th CDTA (i = 1, 2).

Consider the CDTA2, we have for the output current (I_{out}) at the terminal +x as :

$$I_{out} = i_{x2} = g_{m2} R_{z2} i_{z2} = g_{m2} R_{z2} (I_2 - I_1 - I_{out}) \ ,$$

so

$$I_{out}\left(\frac{1}{R_{z2}} + g_{m2}\right) = g_{m2}(I_2 - I_1) \ .$$

However, under the condition with an open circuit at the terminal z ($R_{z2} \rightarrow \infty$), the above equation can reduce to

$$I_{out} = I_2 - I_1 \tag{B.4}$$

Substituting I_1 from equation (B.2) and I_2 from equation (B.3) into equation (B.4) gives

$$\frac{I_{out}}{I_{in}} = \frac{1 - s\left(\frac{C}{g_{m1}}\right)}{1 + s\left(\frac{C}{g_{m1}}\right)} \tag{B.5}$$

Since $I_{out} = I_{AP+} = -I_{AP-}$, we also obtain the following current transfer functions.

$$\frac{I_{AP+}}{I_{in}} = -\frac{I_{AP-}}{I_{in}} = \frac{1 - s\left(\frac{C}{g_{m1}}\right)}{1 + s\left(\frac{C}{g_{m1}}\right)} \tag{B.6}$$

B.2 Non-Ideal Current Transfer Function of First-Order Allpass Section of Figure 3.1

In this section, the effect of CDTA non-idealities on the performance of the current-mode first-order allpass filter in figure 3.1 is analyzed. The characteristics of the non-ideal CDTA circuit were considered previously in section 2.2.2. Therefore, taking into account the non-ideal CDTA behavior and its parasitic elements as depicted in figure 2.2, the simplified circuit of figure 3.1 for determining the non-ideal current transfer characteristic can be represented in figure B.2(a). In analyzing this circuit, r_{z1} represents the equivalent input resistance looking into the z-terminal of the CDTA1. Here, the circuit for calculating the resistance r_{z1} can be illustrated in figure B.2(b). By inspection of figure B.2(b), we found that

$$I_2 = -i_{z1} = -(-\alpha_{n1} i_{n1}) \tag{B.7}$$

and

$$i_{n1} = \beta_1 g_{m1} v_{z1} \tag{B.8}$$

which gives the equivalent input resistance

$$r_{z1} = \frac{v_{z1}}{I_2} = \frac{1}{\alpha_{n1}\beta_1 g_{m1}} \tag{B.9}$$

Consider the simplified circuit shown in figure B.2(a). The current at the x-terminal is determined by

$$i_{o1} = \beta_2 g_{m2} v_{z2} = \beta_2 g_{m2}(\alpha_{p2} i_{p2} - \alpha_{n2} i_{n2}) Z_{z2}$$

Now $i_{p2} = I_2$ and $i_{n2} = I_1 + i_{o1}$, gives

$$\frac{i_{o1}}{Z_{z2}} + \alpha_{n2}\beta_2 g_{m2} i_{o1} = \beta_2 g_{m2}(\alpha_{p2} I_2 - \alpha_{n2} I_1) \tag{B.10}$$

where

$$Z_{z2} = R_{z2} // C_{z2} = \frac{R_{z2}}{1 + sR_{z2}C_{z2}} \tag{B.11}$$

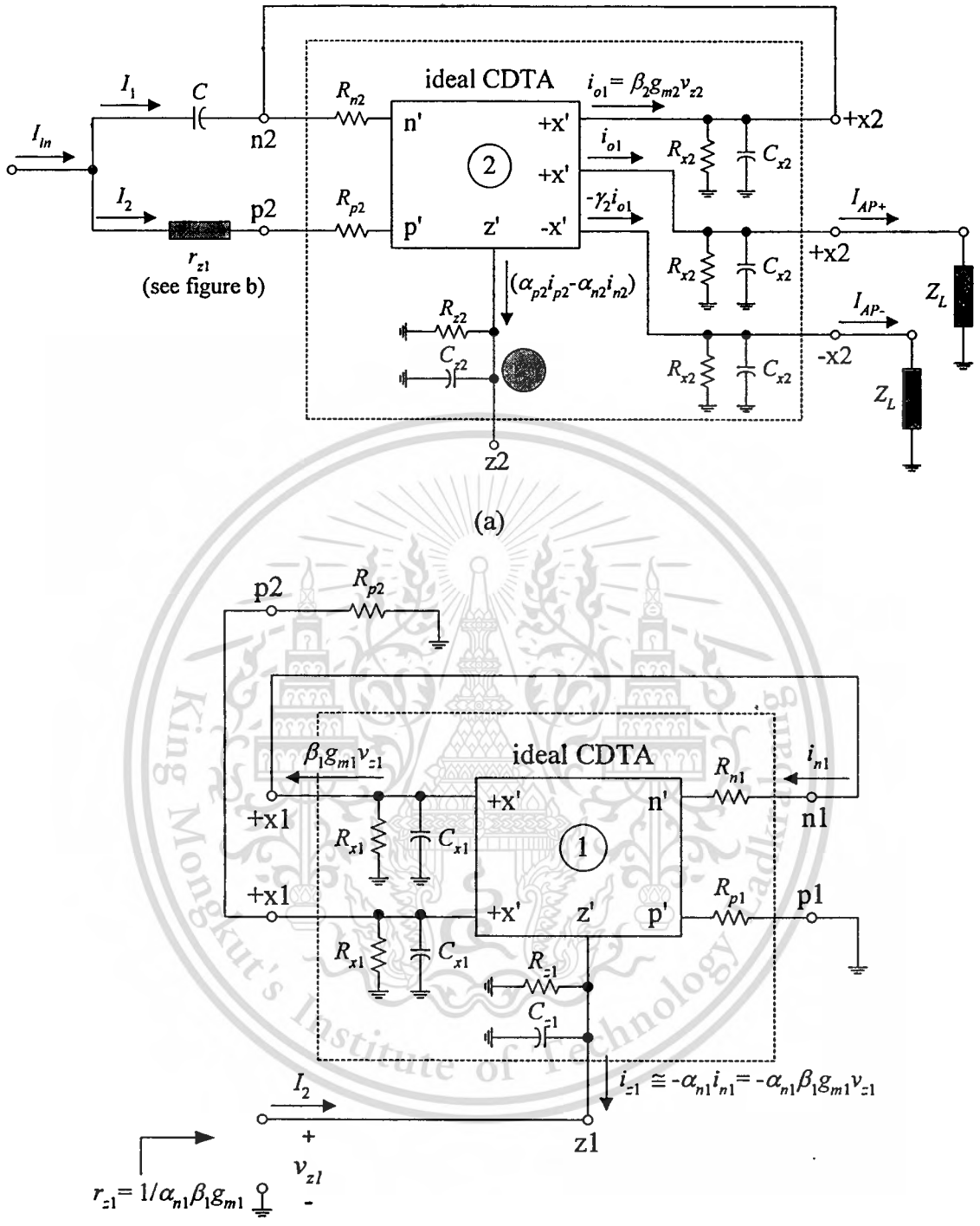


Figure B.2 : (a) Simplified circuit for determining the non-ideal current transfer function of figure 3.1.

(b) Circuit for calculating the equivalent resistance r_{z1}.

Combining equation (B.10) and (B.11), we find that

$$i_{o1} = \left[\frac{1}{1+\dfrac{1}{\alpha_{n2}\beta_2 g_{m2} R_{z2}} + \dfrac{sC_{z2}}{\alpha_{n2}\beta_2 g_{m2}}}\right]\left(\frac{\alpha_{p2} I_2}{\alpha_{n2}} - I_1\right) \tag{B.12}$$

Because $1 >> \dfrac{1}{\alpha_{n2}\beta_2 g_{m2} R_{z2}}$, the above equation reduces to

$$i_{o1} \cong \left[\frac{1}{1+\dfrac{sC_{z2}}{\alpha_{n2}\beta_2 g_{m2}}}\right]\left(\frac{\alpha_{p2} I_2}{\alpha_{n2}} - I_1\right) \tag{B.13}$$

Next, at the input of figure B.2(a),

$$v_C = \left(\frac{1}{sC}\right) I_1 = \left(\frac{\dfrac{1}{sC}}{\dfrac{1}{sC} + Z_{n2}}\right) v_{in} = \left[\frac{1}{1+sZ_{n2}C}\right] v_{in} \tag{B.14}$$

where $$Z_{n2} = R_{n2} // R_{x2} // C_{x2} = \frac{(R_{n2} // R_{x2})}{1+s(R_{n2} // R_{x2})C_{x2}} \tag{B.15}$$

and $$v_{in} = (r_{z1} + R_{p2}) I_2 \tag{B.16}$$

which combines to obtain

$$I_1 = \left[\frac{s(r_{z1}+R_{p2})C}{1+sZ_{n2}C}\right] I_2 = \left\{\frac{[s(r_{z1}+R_{p2})C][1+s(R_{n2} // R_{x2})C_{x2}]}{1+s(R_{n2} // R_{x2})(C_{x2}+C)}\right\} I_2 \tag{B.17}$$

Normally, $R_{n2} << R_{x2}$ and $C_{x2} << C$, in which case equation (B.17) reduces to

$$I_1 \cong \left[\frac{s(r_{z1}+R_{p2})C}{1+sR_{n2}C}\right] I_2 \tag{B.18}$$

Here, $I_2 = i_{in} - I_1$, thus we have

$$I_1 \cong \left[\frac{s(r_{z1}+R_{p2})C}{1+s(r_{z1}+R_{p2}+R_{n2})C}\right] i_{in} \tag{B.19}$$

Also, taking $I_2 = i_{in} - I_1$, and substituting I_1 from equation (B.19) yields

$$I_2 = \left[\frac{1-sR_{n2}C}{1+s(r_{z1}+R_{p2}+R_{n2})C}\right] i_{in} \tag{B.20}$$

Now, substituting I_1 and I_2 from equations (B.19) and (B.20) into equation (B.13) and rearranging leads to

$$\begin{aligned} i_{o1} &= \left[\frac{1}{1+\dfrac{sC_{z2}}{\alpha_{n2}\beta_2 g_{m2}}}\right]\left\{\frac{\alpha_{p2}}{\alpha_{n2}}\left(\frac{1-sR_{n2}C}{1+s(r_{z1}+R_{p2}+R_{n2})C}\right)-\left(\frac{s(r_{z1}+R_{p2})C}{1+s(r_{z1}+R_{p2}+R_{n2})C}\right)\right\} I_{in} \\ &= \left[\frac{\left(\dfrac{\alpha_{p2}}{\alpha_{n2}}\right)}{1+\dfrac{sC_{z2}}{\alpha_{n2}\beta_2 g_{m2}}}\right]\left\{\frac{1-s\left(\dfrac{\alpha_{n2}}{\alpha_{p2}}\dfrac{1}{\alpha_{n1}\beta_1 g_{m1}}+\dfrac{\alpha_{n2}R_{p2}}{\alpha_{p2}}-R_{n2}\right)C}{1+s\left(\dfrac{1}{\alpha_{n1}\beta_1 g_{m1}}+R_{p2}+R_{n2}\right)C}\right\} I_{in} \end{aligned} \tag{B.21}$$

Usually, $1/g_{m1}$ is >> R_{p2}, R_{n2}, equation (B.20) can then be approximated to

$$i_{o1} \cong \left[\frac{\left(\dfrac{\alpha_{p2}}{\alpha_{n2}}\right)}{1+s\left(\dfrac{C_{z2}}{\alpha_{n2}\beta_2 g_{m2}}\right)}\right]\left[\frac{1-s\left(\dfrac{C}{\alpha_{n1}\beta_1 g_{m1}}\dfrac{\alpha_{n2}}{\alpha_{p2}}\right)}{1+s\left(\dfrac{C}{\alpha_{n1}\beta_1 g_{m1}}\right)}\right] I_{in} \tag{B.22}$$

Finally, since $I_{AP+} \cong i_{o1}$ and $I_{AP-} \cong -\gamma_2 i_{o1}$, the two output currents of the circuit are thus

$$I_{AP+} = \left[\frac{\left(\dfrac{\alpha_{p2}}{\alpha_{n2}}\right)}{1+s\left(\dfrac{C_{z2}}{\alpha_{n2}\beta_2 g_{m2}}\right)}\right]\left[\frac{1-s\left(\dfrac{C}{\alpha_{n1}\beta_1 g_{m1}}\dfrac{\alpha_{n2}}{\alpha_{p2}}\right)}{1+s\left(\dfrac{C}{\alpha_{n1}\beta_1 g_{m1}}\right)}\right] I_{in} \tag{B.23}$$

and
$$I_{AP-} = -\left[\frac{\left(\frac{\alpha_{p2}\gamma_2}{\alpha_{n2}}\right)}{1+s\left(\frac{C_{z2}}{\alpha_{n2}\beta_2 g_{m2}}\right)}\right]\left[\frac{1-s\left(\frac{C}{\alpha_{n1}\beta_1 g_{m1}}\frac{\alpha_{n2}}{\alpha_{p2}}\right)}{1+s\left(\frac{C}{\alpha_{n1}\beta_1 g_{m1}}\right)}\right]I_{in} \tag{B.24}$$

It is apparent from equations (B.23) and (B.24) that the pole frequency ω_o of the circuit is slightly deviated from the ideal case by the factor $\alpha_{n1}\beta_1$. Also, one extra pole ($\omega_p = \alpha_{n2}\beta_2 g_{m2}/C_{z2}$) due to the parasitic elements appears in the filter characteristic.

In this case, the filter gains of both types of allpass sections are obtained as :

$$H_{AP+} = \frac{\alpha_{p2}}{\alpha_{n2}} \tag{B.25}$$

and
$$H_{AP-} = -\frac{\alpha_{p2}\gamma_2}{\alpha_{n2}} \tag{B.26}$$

which are dependent on the parasitic current gains α_{p2}, α_{n2} and γ_2 of the CDTA2.

Furthermore, the phase responses obtained from equations (B.23) and (B.24) are respectively calculated as:

$$\begin{aligned}\phi_{AP+} &= \tan^{-1}\left(-\frac{\omega C}{\alpha_{p1}\beta_1 g_{m1}}\frac{\alpha_{n2}}{\alpha_{p2}}\right) - \tan^{-1}\left(\frac{\omega C}{\alpha_{p1}\beta_1 g_{m1}}\right) \\ &= -\left[\tan^{-1}\left(\frac{\omega C}{\alpha_{p1}\beta_1 g_{m1}}\frac{\alpha_{n2}}{\alpha_{p2}}\right) + \tan^{-1}\left(\frac{\omega C}{\alpha_{p1}\beta_1 g_{m1}}\right)\right]\end{aligned} \tag{B.27}$$

and
$$\begin{aligned}\phi_{AP-} &= -\left[\tan^{-1}\left(-\frac{\omega C}{\alpha_{p1}\beta_1 g_{m1}}\frac{\alpha_{n2}}{\alpha_{p2}}\right) - \tan^{-1}\left(\frac{\omega C}{\alpha_{p1}\beta_1 g_{m1}}\right)\right] \\ &= \tan^{-1}\left(\frac{\omega C}{\alpha_{p1}\beta_1 g_{m1}}\frac{\alpha_{n2}}{\alpha_{p2}}\right) + \tan^{-1}\left(\frac{\omega C}{\alpha_{p1}\beta_1 g_{m1}}\right)\end{aligned} \tag{B.28}$$

B.3 Sensitivity Analysis of Figure 3.1 with Respect to Active and Passive Elements

The term "sensitivity" is used to express the degree of influence of a variation in the value of one (or more) component on the performance of the circuit in which it is embedded. In general, the relative sensitivity of a parameter G to the component of variation x can be defined as:

$$S_x^G = \frac{\%\text{change in G}}{\%\text{change in } x} = \frac{(\Delta G/G)\times 100\%}{(\Delta x/x)\times 100\%} \tag{B.29}$$

which can also be written as follows :

$$S_x^G = \frac{\partial G/G}{\partial x/x} = \frac{x}{G}\frac{\partial G}{\partial x} \tag{B.30}$$

To show this, let us consider the current-mode first-order allpass filters using CDTAs depicted in figure 3.1, where its parameters H_{AP+} and H_{AP-} are obtained from equations (B.25) and (B.26) as :

$$H_{AP+} = \frac{\alpha_{p2}}{\alpha_{n2}} \tag{B.31}$$

and

$$H_{AP-} = -\frac{\alpha_{p2}\gamma_2}{\alpha_{n2}} \tag{B.32}$$

For example, from equation (B.31), the active sensitivity of the filter gain H_{AP+} to the variations in α_{p2} is therefore given by

$$S_{\alpha_{p2}}^{H_{AP+}} = \frac{\alpha_{p2}}{H_{AP+}}\frac{\partial(H_{AP+})}{\partial(\alpha_{p2})} \tag{B.33}$$

Substituting H_{AP+} from equation (B.31) into (B.33), we get

$$S_{\alpha_{p2}}^{H_{AP+}} = \left[\frac{\alpha_{p2}}{\left(\frac{\alpha_{p2}}{\alpha_{n2}}\right)}\right]\left[\frac{\partial\left(\frac{\alpha_{p2}}{\alpha_{n2}}\right)}{\partial(\alpha_{p2})}\right] = \frac{\alpha_{n2}}{\alpha_{n2}} = 1 \tag{B.34}$$

Equation (B.34) readily shows that the H_{AP+} sensitivity with respect to α_{p2} is equal to unity. In a similar way, it is easy to show that the sensitivities of the filter parameters H and ω_o with respect to active and passive components are found to be :

$$S_{\alpha_{p2}}^{H} = -S_{\alpha_{n2}}^{H} = S_{\gamma_2}^{H} = 1 \tag{B.35}$$

$$S_{\alpha_{p1},\alpha_{n1},\beta_1,\beta_2,g_{m1}}^{H} = S_C^H = 0 \tag{B.36}$$

$$S_{\alpha_{n1},\beta_1,g_{m1}}^{\omega_o} = -S_C^{\omega_o} = 1 \tag{B.37}$$

and

$$S_{\alpha_{p1},\alpha_{p2},\alpha_{n2},\beta_2}^{\omega_o} = 0 \tag{B.38}$$

It is clearly observed from equations (B.34)-(B.38) that the active and passive sensitivities of the parameters H and ω_o are less than unity.

APPENDIX C

C.1 Characteristic Equations of Two Integrator Loop Structures of Figures 4.1(a) and 4.1(b)

According to the two integrator loop structures of figure 4.1, the configurations of figure 4.1(a) and (4.1(b) can be redrawn as illustrated in figure C.1. Therefore, a detailed analysis for determining the characteristic equations of both schemes is as follows.

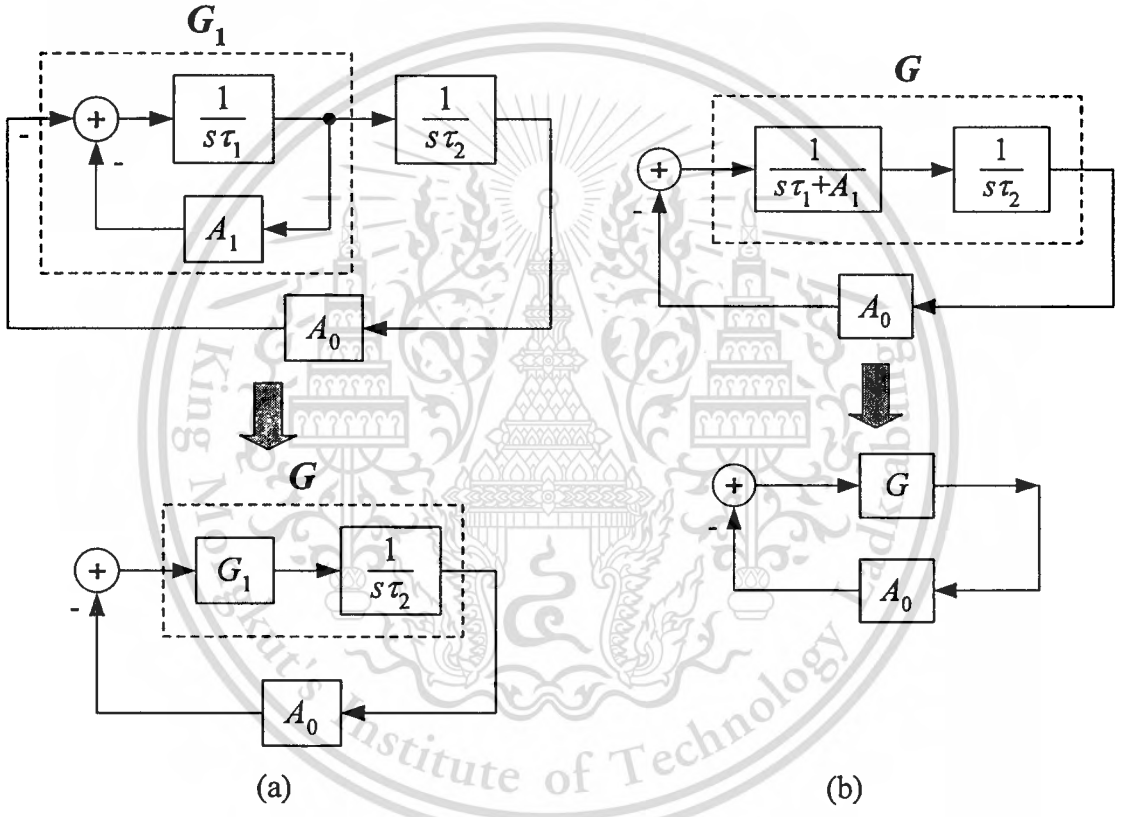


Figure C.1 : Two integrator loop structures of figures 4.1(a) and 4.1(b).
(a) Configuration A (b) Configuration B

Referring to the configuration A of figure C.1(a), the equivalent gain block (G_1) can be obtained from the closed-loop system principle as follows.

$$G_1 = \frac{\left(\frac{1}{s\tau_1}\right)}{1+\left(\frac{1}{s\tau_1}A_1\right)} = \frac{1}{s\tau_1 + A_1} \quad . \tag{C.1}$$

Because the two blocks (G_1 and $1/s_{r1}$) are connected in cascade, then we have

$$G(s) = G_1\left(\frac{1}{s\tau_2}\right) = \frac{1}{(s\tau_1 + A_1)(s\tau_2)} \qquad \text{(C.2)}$$

With the same principle, the closed-loop transfer function ($T_1(s)$) of the whole system can be found from

$$T_1(s) = \frac{N_1(s)}{D_1(s)} = \frac{G}{1 + A_0 G} = \frac{\left[\dfrac{1}{(s\tau_1 + A_1)(s\tau_2)}\right]}{1 + A_0\left[\dfrac{1}{(s\tau_1 + A_1)(s\tau_2)}\right]} = \frac{1}{s^2\tau_1\tau_2 + s\tau_2 A_1 + A_0} \qquad \text{(C.3)}$$

In the above equation, the denominator polynomial $D_1(s)$ is called the characteristic equation. Then, the characteristic equation for this structure may be written as :

$$D_1(s) = s^2\tau_1\tau_2 + s\tau_2 A_1 + A_0 = 0 \qquad \text{(C.4)}$$

Similarly, in considering the configuration B of figure C.1(b), we may also obtain

$$G(s) = \frac{1}{(s\tau_1 + A_1)(s\tau_2)} \qquad \text{(C.5)}$$

and

$$T_1(s) = \frac{N_1(s)}{D_1(s)} = \frac{G}{1 + A_0 G} = \frac{1}{s^2\tau_1\tau_2 + s\tau_2 A_1 + A_0} \; . \qquad \text{(C.6)}$$

which gives

$$D_1(s) = s^2\tau_1\tau_2 + s\tau_2 A_1 + A_0 = 0 \qquad \text{(C.7)}$$

It is of interest to note that equation (C.7) is identical to the characteristic equation obtained from the configuration of figure C.1(a).

The standard expression for the denominator of the general biquadratic transfer function may be written in the following form :

$$D(s) = s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2 = s^2 + (BW)s + \omega_o^2 \qquad \text{(C.8)}$$

where ω_o (= $2\pi f_o$) is the natural angular frequency in radian per second, the ratio ω_o/Q is the bandwidth (BW) and Q is the quality factor of the function. Thus, by comparing equations (C.4) and (C.7) to the standard form of equation (C.8), we respectively identify the important filter parameters as :

$$\omega_o = \sqrt{\frac{A_0}{\tau_1\tau_2}} \qquad \text{(C.9)}$$

$$BW = \frac{A_1}{\tau_1} \qquad \text{(C.10)}$$

and

$$Q = \frac{1}{A_1}\sqrt{\frac{A_0\tau_1}{\tau_2}} \,. \qquad \text{(C.11)}$$

This reveals that we can now determine the component values to satisfy the given design parameters.

C.2 Characteristic Equations of Two Integrator Loop Structures of Figures 4.1(c) and 4.1(d)

In the same way, the two integrator loop structures of figures 4.1(c) and 4.1(d) are redrawn as shown in figures C.2(a) and C.2(b), respectively. The block diagram shown in figure C.2(a) can be simplified as shown in the lower part of the figure, giving

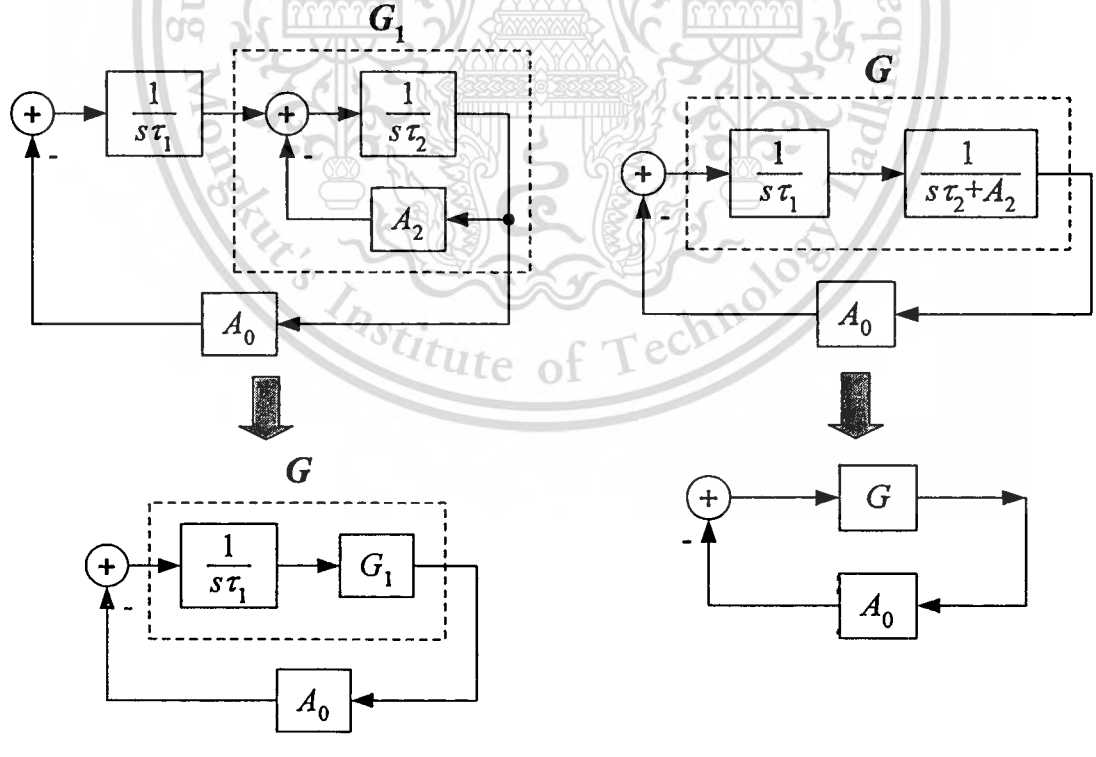
$$G(s) = \left(\frac{1}{s\tau_1}\right) G_1 = \frac{1}{(s\tau_1)(s\tau_2 + A_2)} \tag{C.12}$$

and

$$T_2(s) = \frac{N_2(s)}{D_2(s)} = \frac{G}{1 + A_0 G} = \frac{1}{s^2\tau_1\tau_2 + s\tau_1 A_2 + A_0} \quad . \tag{C.13}$$

From equation (C.13), the characteristic equation of figure C.2(a) is

$$D_2(s) = s^2\tau_1\tau_2 + s\tau_1 A_2 + A_0 = 0 \quad . \tag{C.14}$$



(a) (b)

Figure C.2 : Two integrator loop structures of figures 4.1(c) and 4.1(d).

(a) Configuration C (b) Configuration D

Also, from figure C.2(b), we have

$$T_2(s) = \frac{N_2(s)}{D_2(s)} = \frac{G}{1 + A_0 G} = \frac{1}{s^2\tau_1\tau_2 + s\tau_1 A_2 + A_0} \quad . \tag{C.15}$$

where $G(s) = \dfrac{1}{(s\tau_1)(s\tau_2 + A_2)}$. Thus, the characteristic equation of figure C.2(b) is then

$$D_2(s) = s^2\tau_1\tau_2 + s\tau_1 A_2 + A_0 = 0 \quad . \tag{C.16}$$

which is identical to equation (C.14) obtained from figure C.2(a).

Comparing equations (C.14) and (C.16) with equation (C.8), we see that

$$\omega_o = \sqrt{\frac{A_0}{\tau_1\tau_2}} \tag{C.17}$$

$$BW = \frac{A_2}{\tau_2} \tag{C.18}$$

and

$$Q = \frac{1}{A_2}\sqrt{\frac{A_0\tau_2}{\tau_1}} \quad . \tag{C.19}$$

APPENDIX D

D.1 Current Transfer Function of Configuration A of Figure 4.2(a)

Reconsider the proposed CDTA-based biquadratic filter shown in figure 4.2(a). In this calculation of the current transfer function, we have redrawn the circuit diagram as shown in figure D.1. By straightforward analysis, the current transfer function of this circuit can be derived as follows.

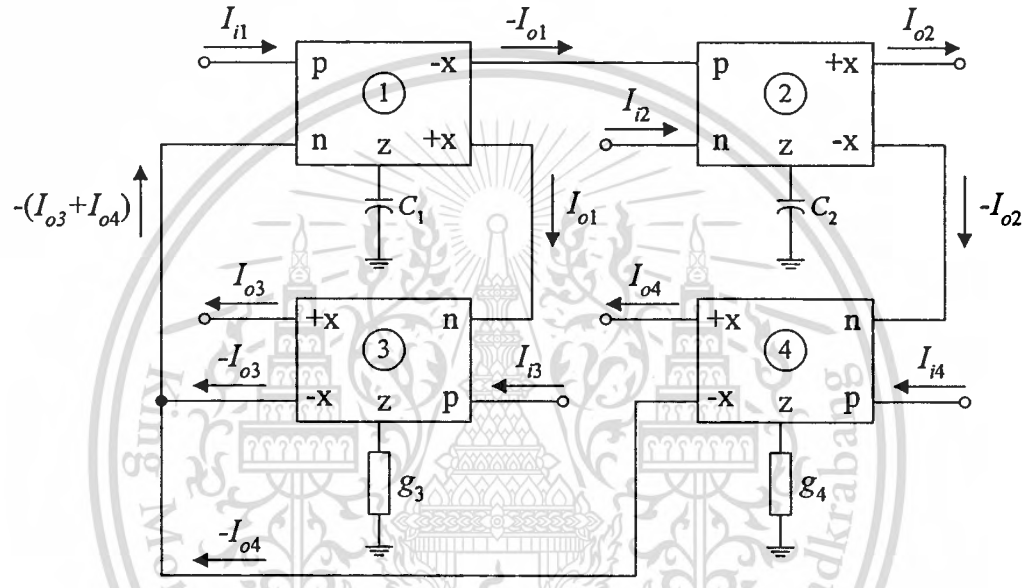


Figure D.1 : CDTA-based biquadratic filter of figure 4.2(a).

By inspection of figure D.1, the currents at the x-terminals of all the CDTAs can respectively be given by :

$$I_{o1} = \left(\frac{g_{m1}}{sC_1}\right)(I_{i1} + I_{o3} + I_{o4}) \tag{D.1}$$

$$I_{o2} = -\left(\frac{g_{m2}}{sC_2}\right)(I_{o1} + I_{i2}) \tag{D.2}$$

$$I_{o3} = \left(\frac{g_{m3}}{g_3}\right)(I_{i3} - I_{o1}) \tag{D.3}$$

and $$I_{o4} = \left(\frac{g_{m4}}{g_4}\right)(I_{i4} + I_{o2}) \quad . \tag{D.4}$$

Substituting equations (D.1), (D.3) and (D.4) into equation (D.2) gives

$$I_{o2} = -\left[\frac{I_{i1} + (s\tau_1 + A_1)I_{i2} + A_3 I_{i3} + A_0 I_{i4}}{D_1(s)}\right] \tag{D.5}$$

where $$D_1(s) = s^2\tau_1\tau_2 + s\tau_2 A_1 + A_0 = s^2\left(\frac{C_1 C_2}{g_{m1}g_{m2}}\right) + s\left(\frac{C_2 g_{m3}}{g_{m2}g_3}\right) + \left(\frac{g_{m4}}{g_4}\right) \tag{D.6}$$

and $$\tau_1 = \frac{C_1}{g_{m1}}, \quad \tau_2 = \frac{C_2}{g_{m2}}, \quad A_1 = \frac{g_{m3}}{g_3}, \text{ and } \quad A_0 = \frac{g_{m4}}{g_4} \tag{D.7}$$

Further, by substituting equations (D.2) and (D.4) into equation (D.1) then we have

$$I_{o1} = \frac{(s\tau_2)I_{i1} - A_0 I_{i2} + (s\tau_2 A_0)I_{i4} + (s\tau_2)I_{o3}}{(s^2\tau_1\tau_2 + A_0)}$$

Substituting I_{o1} from above equation into equation (D.3) results in

$$I_{o3} = \frac{-(s\tau_2 A_1)I_{i1} + (A_1 A_0)I_{i2} + A_1(s^2\tau_1\tau_2 + A_0)I_{i3} - (s\tau_2 A_1 A_0)I_{i4}}{D_1(s)} \tag{D.8}$$

From equations (D.1) and (D.3), we find that

$$(s\tau_1)I_{o1} = I_{i1} + I_{o3} + I_{o4} = I_{i1} + A_1(I_{i3} - I_{o1}) + I_{o4}$$

or $$I_{o1} = \frac{I_{i1} + A_1 I_{i3} + I_{o4}}{(s\tau_1 + A_1)} \tag{D.9}$$

Using equations (D.9) and (D.2) in equation (D.4) gives

$$I_{o4} = \frac{-A_0 I_{i1} - A_0(s\tau_1 + A_1)I_{i2} - (A_0 A_1)I_{i3} + A_0(s^2\tau_1\tau_2 + s\tau_2 A_1)I_{i4}}{D_1(s)} \tag{D.10}$$

Similarly as we did earlier in Appendix C, by equating like terms of equation (D.6) and equation (C.8), we also find that

$$\omega_o = \sqrt{\frac{A_0}{\tau_1 \tau_2}} = \sqrt{\frac{g_{m1} g_{m2} g_{m4}}{g_4 C_1 C_2}} \tag{D.11}$$

$$BW = \frac{A_1}{\tau_1} = \frac{g_{m1} g_{m3}}{g_3 C_1} \tag{D.12}$$

and

$$Q = \frac{1}{A_1} \sqrt{\frac{A_0 \tau_1}{\tau_2}} = \frac{g_3}{g_{m3}} \sqrt{\frac{g_{m2} g_{m4} C_1}{g_{m1} g_4 C_2}} \quad . \tag{D.13}$$

D.2 Current Transfer Function of Configuration B of Figure 4.2(b)

Consider the proposed CDTA-based biquadratic filter of figure 4.2(b). Its circuit diagram has been redrawn as shown in figure D.2. The derivation for the current transfer characteristic of this configuration proceeds as follows.

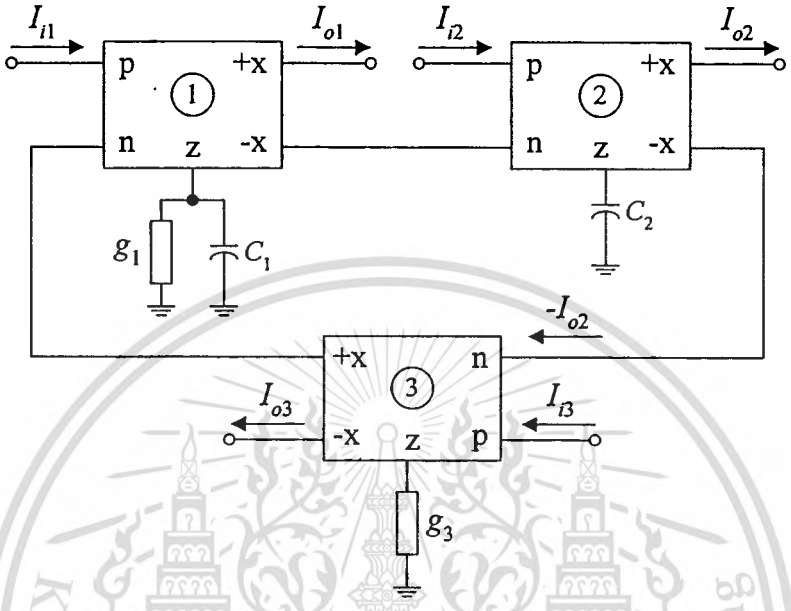


Figure D.2 : CDTA-based biquadratic filter of figure 4.2(b).

In figure D.2, the output currents flowing out from the x-terminals are respectively found as:

$$I_{o1} = \left(\frac{g_{m1}}{g_1 + sC_1}\right)(I_{i1} - I_{o3}) \tag{D.14}$$

$$I_{o2} = \left(\frac{g_{m2}}{sC_2}\right)(I_{o1} + I_{i2}) \tag{D.15}$$

and

$$I_{o3} = \left(\frac{g_{m3}}{g_3}\right)(I_{i3} + I_{o2}) \tag{D.16}$$

Inserting equations (D.15) and (D.16) into equation (D.14), and solving this for I_{o1} gives

$$I_{o1} = \frac{(s\tau_2)I_{i1} - A_0 I_{i2} - (s\tau_2 A_0)I_{i3}}{D_1(s)} \tag{D.17}$$

where $$D_1(s) = s^2\tau_1\tau_2 + s\tau_2 A_1 + A_0 = s^2\left(\frac{C_1C_2}{g_{m1}g_{m2}}\right) + s\left(\frac{C_2g_1}{g_{m1}g_{m2}}\right) + \left(\frac{g_{m3}}{g_3}\right) \tag{D.18}$$

and $$\tau_1 = \frac{C_1}{g_{m1}} \quad , \quad \tau_2 = \frac{C_2}{g_{m2}} \quad , \quad A_1 = \frac{g_1}{g_{m1}} \quad \text{, and} \quad A_0 = \frac{g_{m3}}{g_3} \tag{D.19}$$

Substitution of equation (D.14) into (D.15) yields I_{o2} as

$$I_{o2} = \frac{I_{i1} + (s\tau_1 + A_1)I_{i2} - A_0 I_{i3}}{D_1(s)} \tag{D.20}$$

Again, substituting I_{o1} and I_{o2} from equations (D.14) and (D.15) into equation (D.16), and rearranging gives

$$I_{o3} = \frac{A_0 I_{i1} + A_0(s\tau_1 + A_1)I_{i2} + A_0(s^2\tau_1\tau_2 + s\tau_2 A_1)I_{i3}}{D_1(s)} \tag{D.21}$$

Finally, comparing equations (D.18) and (C.8) reveals that the important parameters ω_o, BW and Q for this configuration are :

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}g_{m3}}{g_3C_1C_2}} \tag{D.22}$$

$$BW = \frac{g_1}{C_1} \tag{D.23}$$

and $$Q = \frac{1}{g_1}\sqrt{\frac{g_{m1}g_{m2}g_{m3}C_1}{g_3C_2}} \quad . \tag{D.24}$$

D.3 Current Transfer Function of Configuration C of Figure 4.2(c)

Consider the proposed CDTA-based biquadratic filter of figure 4.2(c). Here, to derive the current transfer function, its configuration is shown again in figure D.3. From complementary circuit analysis, the x-terminal currents of the CDTA are characterized by the following equations:

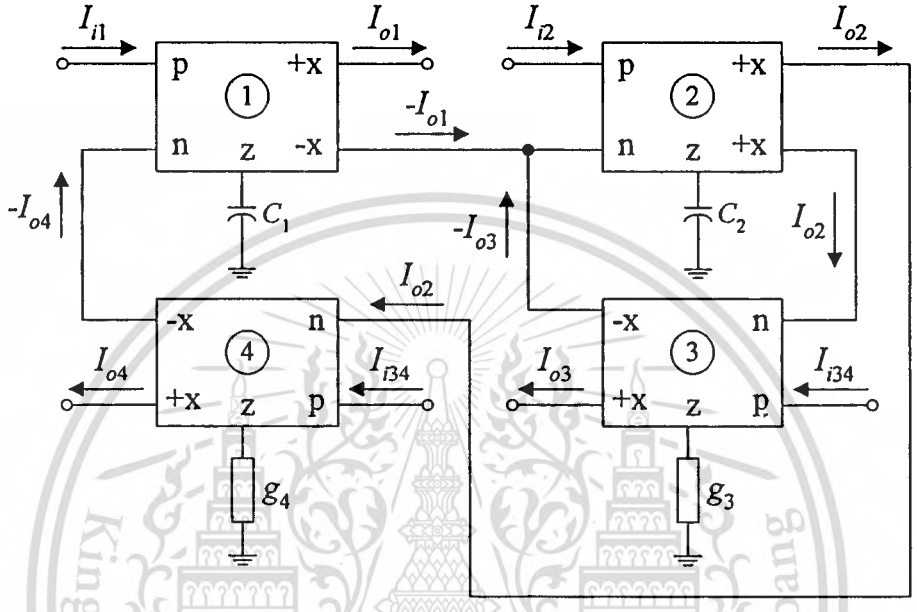


Figure D.3 : CDTA-based biquadratic filter of figure 4.2(c).

$$I_{o1} = \left(\frac{g_{m1}}{sC_1}\right)(I_{i1} + I_{o4}) \tag{D.25}$$

$$I_{o2} = \left(\frac{g_{m2}}{sC_2}\right)(I_{i2} + I_{o1} + I_{o3}) \tag{D.26}$$

$$I_{o3} = \left(\frac{g_{m3}}{g_3}\right)(I_{i34} - I_{o2}) \tag{D.27}$$

and

$$I_{o4} = \left(\frac{g_{m4}}{g_4}\right)(I_{i34} - I_{o2}) \ . \tag{D.28}$$

Substituting equations (D.26) and (D.27) into equation (D.28), and rearranging gives

$$I_{o4} = A_0 I_{i34} - A_0\left[\frac{I_{i2} + A_2 I_{i34} + I_{o1}}{(s\tau_2 + A_2)}\right]$$

Further substituting I_{o4} into equation (D.25), we have, after simplification,

$$I_{o1} = \frac{(s\tau_2 + A_2)I_{i1} - A_0 I_{i2} + (s\tau_2 A_0)I_{i34}}{D_2(s)} \tag{D.29}$$

where $$D_2(s) = s^2\tau_1\tau_2 + s\tau_1 A_2 + A_0 \tag{D.30}$$

and $$\tau_1 = \frac{C_1}{g_{m1}}\ ,\quad \tau_2 = \frac{C_2}{g_{m2}}\ ,\quad A_2 = \frac{g_{m4}}{g_4}\ ,\text{ and }\quad A_0 = \frac{g_{m3}}{g_3} \tag{D.31}$$

Solving for I_{o2} by inserting equations (D.25) and (D.28) into equation (D.26), we get

$$(s^2\tau_1\tau_2)I_{o2} = I_{i1} + (s\tau_1)I_{i2} + A_0 I_{i34} - A_0 I_{o2} + (s\tau_1)I_{o3} \tag{D.32}$$

which, after substituting I_{o3} from equation (D.27), gives

$$I_{o2} = \frac{I_{i1} + (s\tau_1)I_{i2} + (s\tau_1 A_2 + A_0)I_{i34}}{D_2(s)} \tag{D.33}$$

Also, solving for I_{o3} by inserting equation (D.32) into equation (D.27), we get

$$I_{o3} = \frac{-A_2 I_{i1} - (s\tau_1)I_{i2} + (s^2\tau_1\tau_2 A_2)I_{i34}}{D_2(s)} \tag{D.34}$$

Doing the same by inserting equations (D.25)-(D.27) into equation (D.28), we then obtain

$$I_{o4} = \frac{-A_0 I_{i1} - (s\tau_1 A_0)I_{i2} + (s^2\tau_1\tau_2 A_0)I_{i34}}{D_2(s)} \tag{D.35}$$

Finally, by comparing equation (D.30) with equation (C.8), we can identify the important parameters ω_o, BW and Q as following expressions :

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}g_{m4}}{g_4 C_1 C_2}} \tag{D.36}$$

$$BW = \frac{g_{m2}g_{m3}}{g_3 C_2} \tag{D.37}$$

and

$$Q = \frac{g_3}{g_{m3}}\sqrt{\frac{g_{m1}g_{m4}C_2}{g_{m2}g_4 C_1}} \quad . \tag{D.38}$$

D.4 Current Transfer Function of Configuration D of Figure 4.2(d)

Figure D.4 shows the proposed CDTA-based biquadratic filter of figure 4.2(d) that will be used for the determining the current transfer relations. From this circuit, we find that :

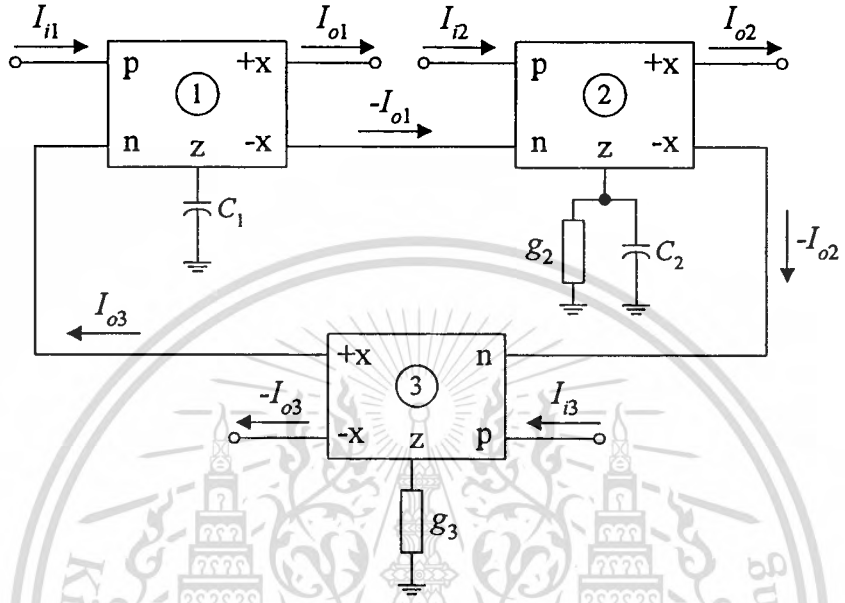


Figure D.4 : CDTA-based biquadratic filter of figure 4.2(d).

$$I_{o1} = \left(\frac{g_{m1}}{sC_1}\right)(I_{i1} - I_{o3}) \tag{D.39}$$

$$I_{o2} = \left(\frac{g_{m2}}{g_2 + sC_2}\right)(I_{o1} + I_{i2}) \tag{D.40}$$

and

$$I_{o3} = \left(\frac{g_{m3}}{g_3}\right)(I_{i3} + I_{o2}) \tag{D.41}$$

Insertion of equations (D.40) and (D.41) into equation (D.39), and solving this for I_{o1} gives

$$I_{o1} = \frac{(s\tau_2 + A_2)I_{i1} - A_0 I_{i2} - (s\tau_2 + A_2)A_0 I_{i3}}{D_2(s)} \tag{D.42}$$

where $$D_2(s) = s^2\tau_1\tau_2 + s\tau_1 A_2 + A_0 \quad \text{(D.43)}$$

and $$\tau_1 = \frac{C_1}{g_{m1}}, \quad \tau_2 = \frac{C_2}{g_{m2}}, \quad A_2 = \frac{g_2}{g_{m2}}, \text{ and } \quad A_0 = \frac{g_{m3}}{g_3} \quad \text{(D.44)}$$

Then, the current I_{o2} is simply derived by substituting I_{o1} from equation (D.39) and I_{o3} from equation (D.41) into equation (D.40), yielding

$$I_{o2} = \frac{I_{i1} + (s\tau_1)I_{i2} - A_0 I_{i3}}{D_2(s)} \quad \text{(D.45)}$$

In the same manner, the current I_{o3} is also obtained by substituting I_{o1} from equation (D.39) and I_{o2} from equation (D.40) into equation (D.41), yielding

$$I_{o3} = \frac{A_0 I_{i1} + (s\tau_1)I_{i2} + (s^2\tau_1\tau_2 + s\tau_1 A_2)A_0 I_{i3}}{D_2(s)} \quad \text{(D.46)}$$

Finally, comparing equations (D.43) and (C.8) results in the following important parameters.

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}g_{m3}}{g_3 C_1 C_2}} \quad \text{(D.47)}$$

$$BW = \frac{g_2}{C_2} \quad \text{(D.48)}$$

and $$Q = \frac{1}{g_2}\sqrt{\frac{g_{m1}g_{m2}g_{m3}C_2}{g_3 C_1}} \; . \quad \text{(D.49)}$$

APPENDIX E

E.1 Current Transfer Function of Configuration A (when $A_0 = 1$) of Figure 4.3(a)

According to figure 4.1(a), if we setting A_0 = 1, then the configuration can be reduced to figure 4.3(a). To derive the current transfer function, let us consider the configuration represented in figure E.1, where the currents at the x-terminals of the CDTAs are found as :

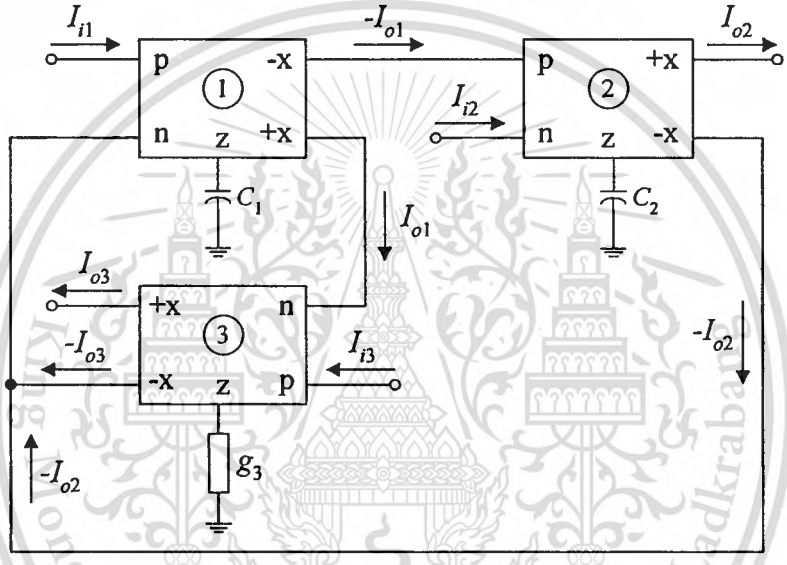


Figure E.1 : CDTA-based biquadratic filter of figure 4.3(a).

$$I_{o1} = \left(\frac{g_{m1}}{sC_1}\right)(I_{i1} + I_{o3} + I_{o4}) \tag{E.1}$$

$$I_{o2} = -\left(\frac{g_{m2}}{sC_2}\right)(I_{o1} + I_{i2}) \tag{E.2}$$

and

$$I_{o3} = \left(\frac{g_{m3}}{g_3}\right)(I_{i3} - I_{o1}) \ . \tag{E.3}$$

Substituting I_{o2} from equation (E.2) and I_{o3} from equation (E.3) into equation (E.1), and solving for I_{o1} gives

$$I_{o1} = \frac{(s\tau_2)I_{i1} - I_{i2} + (s\tau_2 A_1)I_{i3}}{D_1(s)} \tag{E.4}$$

where $D_1(s) = s^2\tau_1\tau_2 + s\tau_2 A_1 + 1$, $\tau_1 = \frac{C_1}{g_{m1}}$, $\tau_2 = \frac{C_2}{g_{m2}}$ and $A_1 = \frac{g_{m3}}{g_3}$ (E.5)

Similarly, by substituting equations (E.1) and (E.3) into equation (E.2), we have

$$I_{o2} = \frac{-I_{i1} + (s\tau_1 + A_1)I_{i2} - A_1 I_{i3}}{D_1(s)} \tag{E.6}$$

Using equations (E.1) and (E.2) in equation (E.3) gives

$$I_{o3} = \frac{-(s\tau_2 A_1)I_{i1} + A_1 I_{i2} + A_1(s^2\tau_1\tau_2 + 1)I_{i3}}{D_1(s)} \tag{E.7}$$

In this case, by equating like terms of equation (E.7) and equation (C.8), we also obtain that

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{E.8}$$

$$BW = \frac{g_{m1}g_{m3}}{g_3C_1} \tag{E.9}$$

and

$$Q = \frac{g_3}{g_{m3}}\sqrt{\frac{g_{m2}C_1}{g_{m1}C_2}} \quad . \tag{E.10}$$

E.2 Current Transfer Function of Configuration A (when $A_1 = 1$) of Figure 4.3(b)

Consider the configuration of figure E.2 obtained from figure 4.1(a) when setting $A_1 = 1$. For this case, the output currents I_{o2} and I_{o4} can be calculated by the following steps.

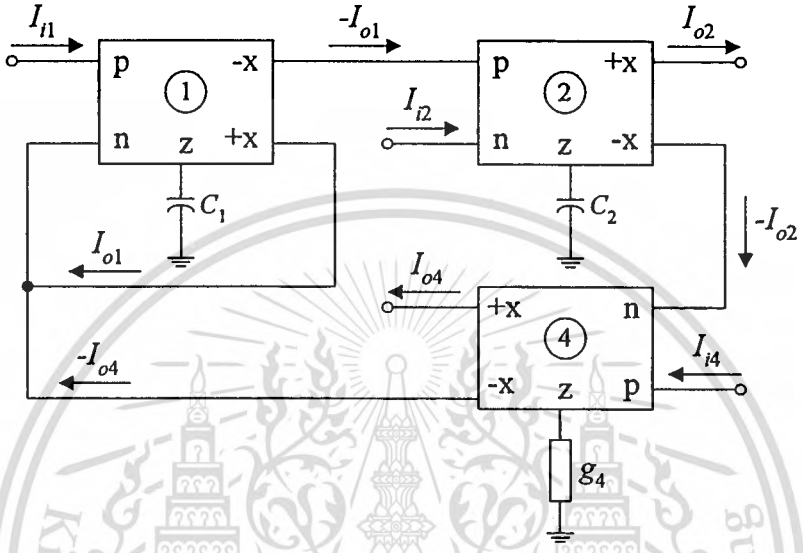


Figure E.2 : CDTA-based biquadratic filter of figure 4.3(b).

From the circuit,

$$I_{o1} = \left(\frac{g_{m1}}{sC_1}\right)(I_{i1} - I_{o1} + I_{o4}) \tag{E.11}$$

$$I_{o2} = \left(\frac{g_{m2}}{sC_2}\right)(I_{o1} + I_{i2}) \tag{E.12}$$

and

$$I_{o4} = -\left(\frac{g_{m4}}{g_4}\right)(I_{i4} + I_{o2}) \tag{E.13}$$

Inserting equations (E.12) and (E.13) into equation (E.11), and solving this for I_{o1} gives

$$I_{o1} = \frac{(s\tau_2)I_{i1} - A_0 I_{i2} - (s\tau_2 A_0)I_{i4}}{D_1(s)} \tag{E.14}$$

where $D_1(s) = s^2\tau_1\tau_2 + s\tau_2 + A_0$, $\tau_1 = \frac{C_1}{g_{m1}}$, $\tau_2 = \frac{C_2}{g_{m2}}$ and $A_0 = \frac{g_{m4}}{g_4}$ (E.15)

Again, substituting I_{o1} and I_{o4} from equations (E.14) and (E.13) into equation (E.12), and rearranging gives

$$I_{o2} = \frac{I_{i1} + (s\tau_1 + 1)I_{i2} - A_0 I_{i4}}{D_1(s)} \tag{E.16}$$

and also solving for I_{o4} by substituting equations (E.11) and (E.12) into (E.13), we have

$$I_{o4} = \frac{-A_0 I_{i1} - A_0(s\tau_1 + 1)I_{i2} - A_0(s^2\tau_1\tau_2 + s\tau_2)I_{i4}}{D_1(s)} \tag{E.17}$$

At last, by comparing equations (E.15) and (C.8), the important parameters ω_o, BW and Q for this configuration are found as :

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}g_{m4}}{g_4 C_1 C_2}} \tag{E.18}$$

$$BW = \frac{g_{m1}}{C_1} \tag{E.19}$$

and

$$Q = \sqrt{\frac{g_{m2}g_{m4}C_1}{g_4 g_{m1} C_2}} \quad . \tag{E.20}$$

E.3 Current Transfer Function of Configuration A (when $A_0 = A_1 = 1$) of Figure 4.3(c)

Consider the configuration of figure E.3 obtained from figure 4.1(a) when setting $A_0 = A_1 = 1$. In this configuration, the currents I_{o1} and I_{o2} are

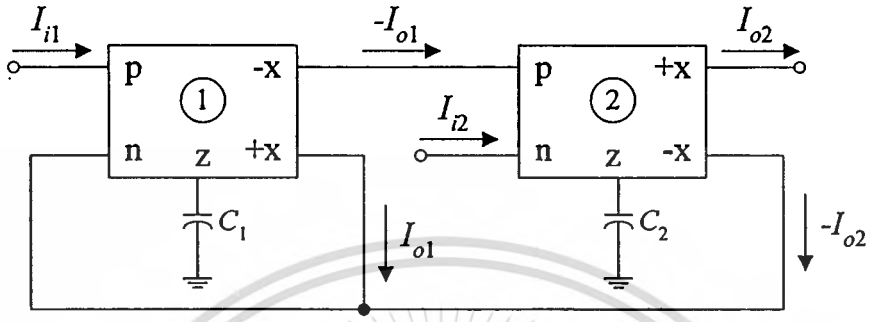


Figure E.3 : CDTA-based biquadratic filter of figure 4.3(c).

$$I_{o1} = \left(\frac{g_{m1}}{sC_1}\right)(I_{i1} - I_{o1} + I_{i2}) \tag{E.21}$$

and

$$I_{o2} = -\left(\frac{g_{m2}}{sC_2}\right)(I_{i2} + I_{o1}) \tag{E.22}$$

Combining equations (E.21) and (E.22), the currents I_{o1} and I_{o2} becomes

$$I_{o1} = \frac{(s\tau_2)I_{i1} - I_{i2}}{D_1(s)} \tag{E.23}$$

$$I_{o2} = \frac{-I_{i1} - (s\tau_1 + 1)I_{i2}}{D_1(s)} \tag{E.24}$$

where $D_1(s) = s^2\tau_1\tau_2 + s\tau_2 + 1$, $\tau_1 = \frac{C_1}{g_{m1}}$ and $\tau_2 = \frac{C_2}{g_{m2}}$ (E.25)

Comparing equation (E.25) with (C.8), we obtain

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad , \quad BW = \frac{g_{m1}}{C_1} \quad \text{and} \quad Q = \sqrt{\frac{g_{m2}C_1}{g_{m1}C_2}} \; . \tag{E.26}$$

E.4 Current Transfer Function of Configuration B (when $A_0 = 1$) of Figure 4.3(d)

With reference to figure 4.3(d), it is shown again in figure E.4. The output currents I_{o1} and I_{o2} are

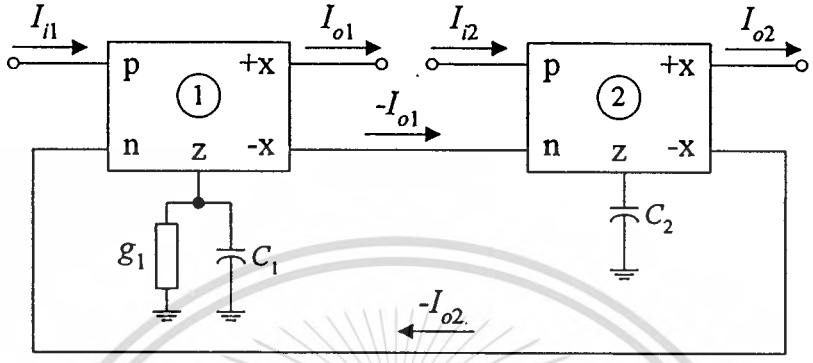


Figure E.4 : CDTA-based biquadratic filter of figure 4.3(d).

$$I_{o1} = \left(\frac{g_{m1}}{g_1 + sC_1}\right)(I_{i1} - I_{i2}) \tag{E.27}$$

and

$$I_{o2} = \left(\frac{g_{m2}}{sC_2}\right)(I_{i2} + I_{o1}) \tag{E.28}$$

Using equations (E.27) and (E.28), we thus have

$$I_{o1} = \frac{(s\tau_2)I_{i1} - I_{i2}}{D_1(s)} \tag{E.29}$$

$$I_{o2} = \frac{I_{i1} + (s\tau_1 + 1)I_{i2}}{D_1(s)} \tag{E.30}$$

where $D_1(s) = s^2\tau_1\tau_2 + s\tau_2 A_1 + 1$, $\tau_1 = \frac{C_1}{g_{m1}}$, $\tau_2 = \frac{C_2}{g_{m2}}$ and $A_1 = \frac{g_1}{g_{m1}}$ (E.31)

and compared with equation (C.8), giving

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad , \quad BW = \frac{g_1}{C_1} \quad \text{and} \quad Q = \sqrt{\frac{g_{m1}g_{m2}C_1}{C_2}} \ . \tag{E.32}$$

E.5 Current Transfer Function of Configuration D (when $A_0 = 1$) of Figure 4.3(e)

As shown in figure E.5, the block diagram is the configuration D shown in figure 4.3(e) when $A_0 = 1$.

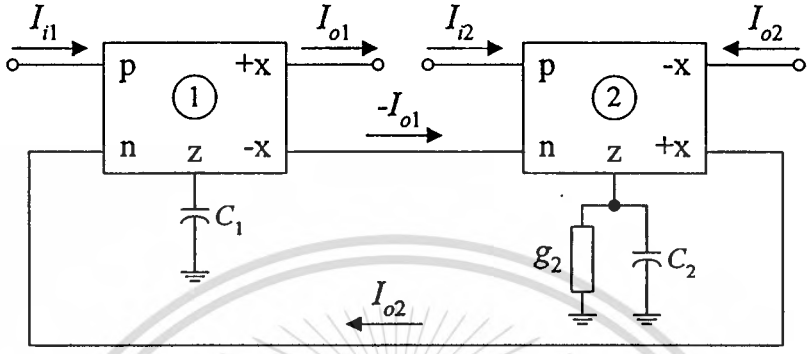


Figure E.5 : CDTA-based biquadratic filter of figure 4.3(e).

For this configuration,

$$I_{o1} = \left(\frac{g_{m1}}{sC_1}\right)(I_{i1} - I_{o2}) \tag{E.33}$$

and

$$I_{o2} = \left(\frac{g_{m2}}{g_2 + sC_2}\right)(I_{i2} + I_{o1}) \tag{E.34}$$

Equations (E.33) and (E.34) lead to

$$I_{o1} = \frac{(s\tau_2 + A_2)I_{i1} - I_{i2}}{D_2(s)} \tag{E.35}$$

$$I_{o2} = \frac{I_{i1} + (s\tau_1)I_{i2}}{D_2(s)} \tag{E.36}$$

where $D_1(s) = s^2\tau_1\tau_2 + s\tau_2 A_2 + 1$, $\tau_1 = \frac{C_1}{g_{m1}}$, $\tau_2 = \frac{C_2}{g_{m2}}$, $A_2 = \frac{g_2}{g_{m2}}$ (E.37)

and $\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$, $BW = \frac{g_2}{C_2}$, $Q = \frac{1}{g_2}\sqrt{\frac{g_{m1}g_{m2}C_2}{C_1}}$ (E.38)

APPENDIX F

The research leads the papers that can be published in international journals and conferences. The list of publication papers is listed below.

F.1 Publication Papers in International Journals

1) W. Tangsrirat, W. Tanjaroen and **T. Pukkalanun**, "Current-mode multiphase sinusoidal oscillator using CDTA-based allpass sections", *International Journal of Electronics and Communications*, vol.63, no.7, pp.616-622, 2009.
2) W. Tangsrirat, **T. Pukkalanun** and W. Surakampontorn, "Resistorless realization of current-mode first-order allpass filter using current differencing transconductance amplifiers", *Microelectronics Journal*, vol.41, no.2-3, pp.178-183, 2010.
3) W. Tangsrirat and **T. Pukkalanun**, "Structural generation of two integrator loop filters using CDTAs and grounded capacitors", *International Journal of Circuit Theory and Applications*, Published Online: Jul 10, 2009, DOI: 10.1002/cta.616.

F.2 Publication Papers in International Conferences

1) **T. Pukkalanun** and W. Tangsrirat, "CDTA-based current limiters and applications", *Proceedings of 2008 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS-2008)*, Macao, China, November 30 - December 3, pp. 1070-1073, 2008.
2) **T. Pukkalanun** and W. Tangsrirat, "Current-mode two integrator loop CDTA filters", *Proceedings of The 5th International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC 2010)*, Pattaya, Thailand, July 4-7, pp. 1164-1167, 2010.

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Current-mode multiphase sinusoidal oscillator using CDTA-based allpass sections

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Abstract

In this work, a current tunable current-mode multiphase sinusoidal oscillator (MSO) employing current differencing transconductance amplifier (CDTA)-based first-order allpass sections is presented. The proposed MSO circuit, which uses only two CDTAs and one virtually grounded capacitor for each phase, can generate arbitrary $2n$-phase current-output signals ($n = 2, 3, 4, \ldots$) equally spaced in phase, all at high output impedance terminals. The oscillation condition and the oscillation frequency can be controlled electronically and independently by adjusting the bias current of the CDTA. The oscillator has low-sensitivity performance. Simulation results are also given to verify the functionality of the proposed oscillator.

Keywords: Current differencing transconductance amplifier (CDTA); Multiphase sinusoidal oscillator (MSO); Allpass filter; Current-mode circuits

1. Introduction

Multiphase sinusoidal oscillators (MSOs) are widely used in instrumentation control, power electronics and signal processing and measurement systems. As a result, a number of MSO circuits have been reported in the technical literature [1–9]. In [1–4], several MSO circuits, using a second-generation current conveyor (CCII) as an active component, have been proposed. Most of the reported circuits suffer from the use of more passive components and the lack of the electronic controllability. In addition, they operate in voltage-mode. The current feedback operational amplifier (CFOA)-based MSO circuit proposed in [5] exploits the internal pole of the device to operate at relatively high frequencies, but this approach requires access to the device compensation terminal. Recently, the techniques to realize the voltage-mode MSO using operational amplifiers (op-amps) were developed [6,7]. However, the drawback of these circuits is the well-known limitations of the op-amps. Moreover, they utilize too many external passive components and a number of them float. In recent years, the current-mode approach of signal processing has offered elegant solutions for analog circuit problems. The main advantages of this operation mode are wide signaling bandwidth, high slew rate and low-power consumption. Thus considering this fact, the current follower-based MSO structure operating in current-mode has then been proposed [8]. It employs two current followers, one floating resistor and one floating capacitor for each stage, and does not provide electronic tunability. More recently, the current-mode MSO circuit based on current-controlled conveyors (CCCIIs) has been reported [9]. This method utilizes the parasitic resistance (R_x) of the conveyor that makes electronic tunability possible through the bias current. However, it still requires an excessive number of external passive capacitors, i.e., two grounded capacitors for

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each stage. Moreover, its oscillation condition is adjusted by tuning the ratio of external passive capacitors, which is not well controlled. In viewpoint of integrated circuits (ICs), controlling circuit parameters electronically is much easier to realize than by changing the values of passive components.

Recently, a new current-mode active element with two current inputs and two kinds of current output, which is called a current differencing transconductance amplifier (CDTA), has been introduced [10]. This device is a synthesis of the well-known advantages of the current differencing buffered amplifier (CDBA) [11] and a multiple-output transconductance amplifier to facilitate the implementation of current-mode analog signal processing. As a result, many applications and advantages in the design of various current-mode circuits using CDTAs as active elements have received considerable attention [12–17]. These applications have proven that the CDTA is a versatile active building block for current-mode signal processing applications. Until now, there is only current-mode quadrature oscillator circuit based on CDTAs, which is recently reported in [16]. However, it produces two sinusoidal output currents with only 90° phase difference.

In view of the above explanations, a novel current-controlled current-mode MSO topology realized by using CDTA-based first-order allpass sections is proposed. The proposed oscillator circuit can produce $2n$-phase output current signals ($n = 2, 3, \ldots$) of identical frequency and equally spaced in phase. Benefits of the proposed circuit are the absence of passive resistors, and the capacity for orthogonal electronic tuning of the oscillation condition and oscillation frequency (ω_o) through the bias current of the CDTA. It also exhibits low active and passive sensitivities, and possesses high output impedance that can be easily cascaded for current-mode systems. Simulation results verifying theoretical analyses are included.

2. Basic principle

2.1. Current differencing transconductance amplifier (CDTA)

The circuit representation and the equivalent circuit of the CDTA are shown in Fig. 1. The terminal relation of the CDTA can be characterized by the following set of equations [10]:

$$v_p = v_n = 0$$
$$i_z = i_p - i_n \quad \text{and}$$
$$i_x = g_m v_z = g_m Z_z i_z \tag{1}$$

where p and n are input terminals, z and $\pm x$ are output terminals, g_m is the transconductance gain, and Z_z is an external impedance connected at the terminal z. According to above equations and an equivalent circuit of Fig. 1(b),

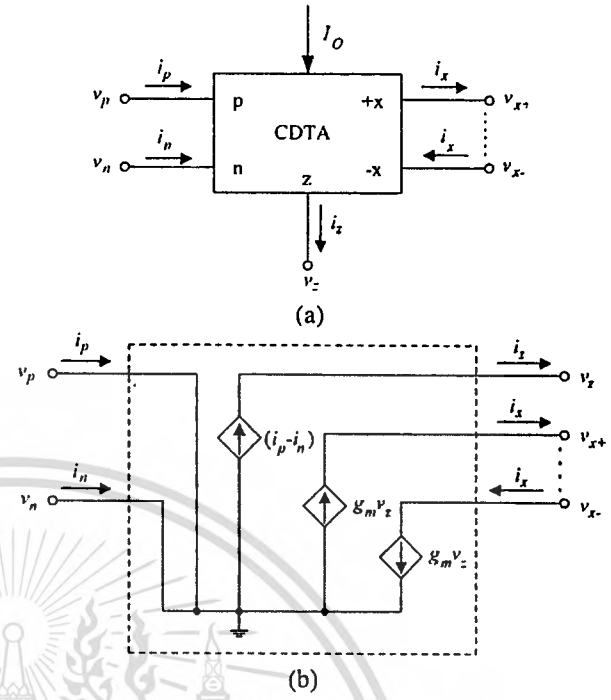

Fig. 1. CDTA. (a) Circuit representation; (b) equivalent circuit.

the current flowing out of the terminal z (i_z) is a difference between the input currents through the terminals p and n ($i_p - i_n$). The voltage drop at the terminal z is transferred to a current at the terminal x (i_x) by a transconductance gain (g_m), which is electronically controllable by an external bias current (I_O). These currents, which are copied to a general number of output current terminals x, are equal in magnitude but flow in opposite directions.

Although there are several techniques to realize the CDTA, one possible bipolar realization is shown in Fig. 2 [17]. It mainly comprises a current differencing circuit formed by two current followers Q_1–Q_9, a basic current mirror Q_{10}–Q_{11}, and a multiple-output transconductance amplifier Q_{12}–Q_{30}. In this case, the transconductance gain g_m of the CDTA is directly proportional to the external bias current I_O, which can be written by

$$g_m = \frac{I_O}{2V_T} \tag{2}$$

where $V_T \cong 26\,\text{mV}$ at 27 °C is the thermal voltage.

2.2. CDTA-based current-mode first-order allpass section

Fig. 3 shows the resistorless current-mode first-order allpass section employing only two CDTAs and one virtually grounded capacitor. Routine analysis using the defined equations in (1), the current transfer function of the circuit in Fig. 3 can be characterized as

$$\frac{i_{out}}{i_{in}} = \frac{1 - s(C/g_{ma})}{1 + s(C/g_{ma})} \tag{3}$$

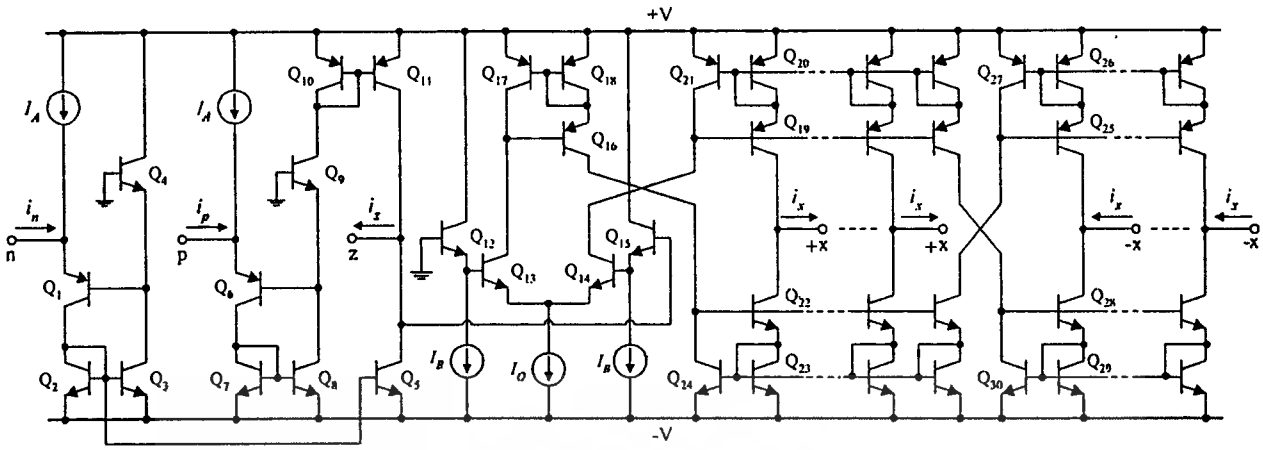

Fig. 2. Possible bipolar realization of the CDTA.

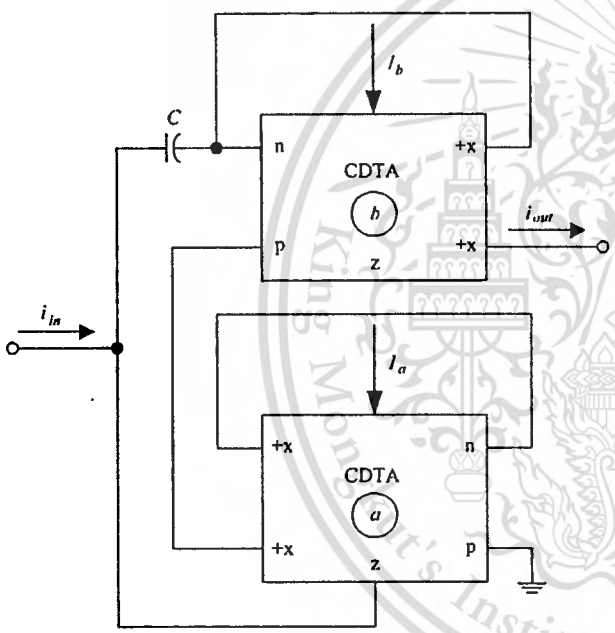

Fig. 3. CDTA-based current-mode first-order allpass section.

where g_{ma} is the transconductance gain of the CDTA$_a$. As it is demonstrated in Fig. 3, the CDTA-based circuit does not require any external passive resistor, and does not require any matching condition for realizing first-order allpass function. The phase response (ϕ) of this section is expressed as

$$\phi = -2\tan^{-1}\left(\frac{\omega C}{g_{ma}}\right) \tag{4}$$

which varies from 0° to −180° as ω goes from zero (DC) to infinity. An examination of Eq. (4) reveals that the shifted phase value can be controlled electronically by adjusting the transconductance g_{ma}.

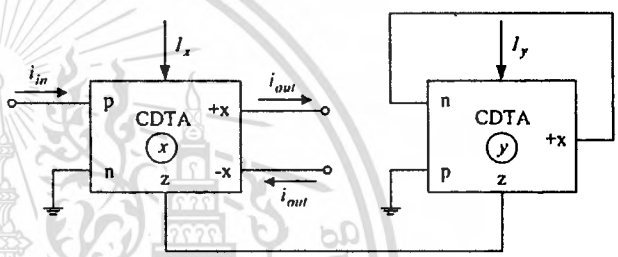

Fig. 4. CDTA-based current-controlled current amplifier.

2.3. CDTA-based current-controlled current amplifier

Fig. 4 illustrates a current tunable current amplifier, which is composed of only two CDTAs without the use of external passive elements. In this case, the current gain (K) of this circuit can be expressed as

$$\frac{i_{out}}{i_{in}} = K = \frac{g_{mx}}{g_{my}} \tag{5}$$

where g_{mx} and g_{my} represent the transconductance gains of CDTA$_x$ and CDTA$_y$, respectively. Note from Eq. (5) that the amplifier gain K can be tuned linearly and electronically by adjusting the ratio of the bias current I_x/I_y.

3. Proposed current-mode MSO circuit

The proposed current-mode MSO topology is given in Fig. 5. It consists of n cascaded CDTA-based allpass sections of Fig. 3. The output current i_{on} of the nth stage is fed back to the input of the first stage through the current amplifier of Fig. 4. Note that the current amplifier performing a feedback path has the gain of $-K$. An attractive benefit offered by this configuration is the absence of the external passive resistor, which is suitable for integration point of

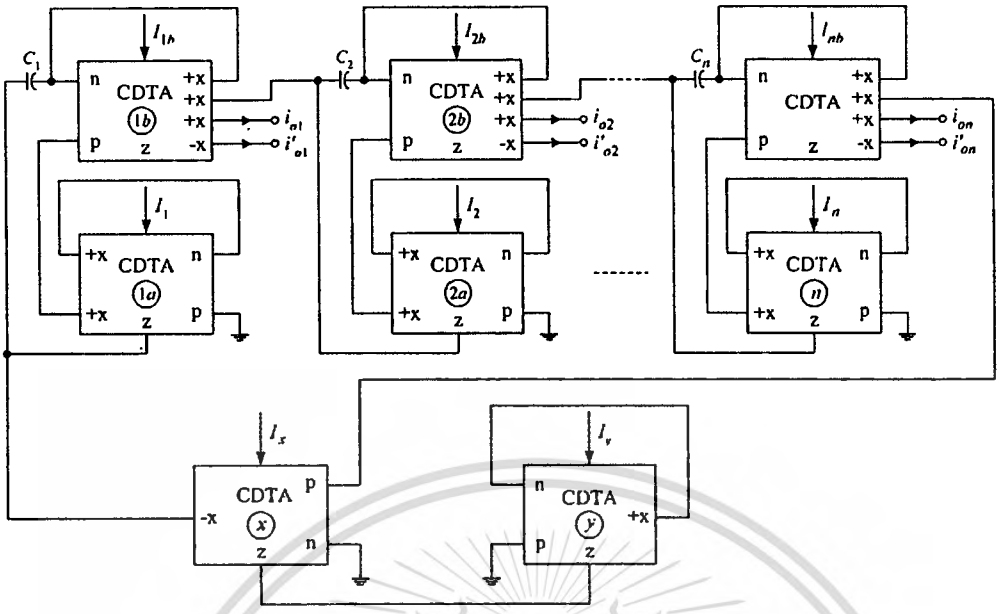

Fig. 5. Proposed current-mode MSO circuit.

view [18,19]. Assuming that $g_{m1a} = g_{m2a} = \cdots = g_{mn} = g_m$ and $C_1 = C_2 = \cdots = C_n = C$, the loop gain $L(s)$ of the proposed structure in Fig. 5 can be given by

$$L(s) = -K\left[\frac{1-s(C/g_m)}{1+s(C/g_m)}\right]^n = -\left(\frac{g_{mx}}{g_{my}}\right)\left[\frac{1-s(C/g_m)}{1+s(C/g_m)}\right]^n \quad (6)$$

According to the Barkhausen criterion, the condition for the proposed MOS circuit of Fig. 5 to produce and sustain sinusoidal oscillations of frequency $\omega_o(=2\pi f_o)$ is that

$$L(j\omega_o) = -\left(\frac{g_{mx}}{g_{my}}\right)\left[\frac{1-j\omega_o(C/g_m)}{1+j\omega_o(C/g_m)}\right]^n = 1 \quad (7)$$

and

$$\phi = \frac{\pi}{n} \quad (8)$$

where $n \geqslant 2$. Eq. (8) shows that there are n outputs i_{oi} ($i = 1, 2, \ldots, n$) of each shifted in phase by $180°/n$ available from the topology. Eq. (7) provides the oscillation condition and the oscillation frequency (ω_o) for values of n (i.e., $n = 2, 3, 4, \ldots$) as

$$\frac{g_{mx}}{g_{my}} = 1 \quad (9)$$

and

$$\omega_o = \left(\frac{g_m}{C}\right)\tan\left(\frac{\pi}{2n}\right) \quad (10)$$

Further, by substituting Eq. (2) into Eqs. (9) and (10), the oscillation condition and the oscillation frequency can now be rewritten as

$$\frac{I_x}{I_y} = 1 \quad (11)$$

and

$$\omega_o = \left(\frac{I_O}{2V_T C}\right)\tan\left(\frac{\pi}{2n}\right) \quad (12)$$

According to Eqs. (11) and (12), it is concluded that the ω_o can be tuned electronically and linearly through the bias current I_O without affecting the condition of oscillation, which can also be controlled electronically by the ratio of I_x/I_y without influencing the ω_o. Therefore, the circuit provides attractive feature of independent linear-current control of the frequency and the condition of oscillations. Additionally, by the use of an inverted version of the output current of the CDTA, the $2n$-phase output currents ($i'_{o1}, i'_{o2}, \ldots, i'_{on}$) are also obtained from the same topology.

4. Effects of CDTA non-idealities

In this section, the effect of CDTA non-idealities on the performance of the proposed circuit is studied. Fig. 6 shows the simplified equivalent circuit that will be used to represent the behavior of the non-ideal CDTA. These mainly result from its finite parasitic elements and non-ideal current transfers. As can be seen, there are parasitic resistances (R_p and R_n) at terminals p and n, and parasitic resistances and capacitances (R_z, C_z and R_x, C_x) from terminals z and x to the ground. In the same figure, $\alpha_p = 1-\varepsilon_p$, $|\varepsilon_p| \ll 1$ is the current transfer error from p to z terminals, $\alpha_n = 1-\varepsilon_n$, $|\varepsilon_n| \ll 1$ is the current transfer error from n to z terminals, and β

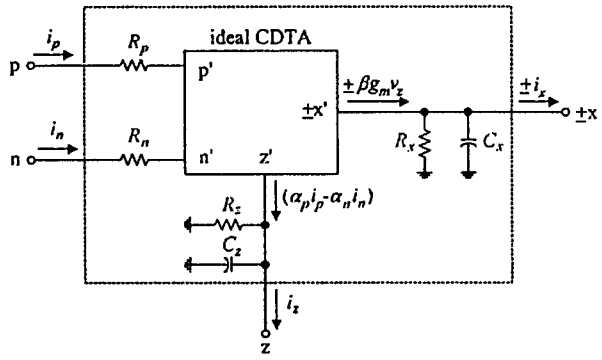

Fig. 6. Simplified equivalent circuit of the non-ideal CDTA.

is the transconductance inaccuracy factor from z to x terminals. Taking into account the non-ideal CDTA characteristics, the modified current transfer functions of Figs. 3 and 4 can respectively be rewritten as

$$\frac{i_{out}}{i_{in}} = \left[\frac{(\alpha_p/\alpha_n)}{1+s(C_z/\alpha_n\beta g_{mb})}\right] \times \left[\frac{1-s(C/\alpha_p\beta g_{ma}+\alpha_n R_p/\alpha_p - R_n)}{1+s(C/\alpha_n\beta g_{ma}+R_p+R_n)}\right] \quad (13)$$

and

$$\frac{i_{out}}{i_{in}} = K = \frac{(\alpha_p/\alpha_n)(g_{mx}/g_{my})}{(1+2sC_z/\alpha_n\beta g_{my})(1+sR_xC_x)} \quad (14)$$

Therefore, re-analysis of the proposed MSO circuit in Fig. 5 using Eqs. (13) and (14) with $C \gg C_z, C_x$ and $1/g_{ma} \gg R_p, R_n$, the modified oscillation condition and ω_o can be described, respectively, by the following relations:

$$\left(\frac{g_{mx}}{g_{my}}\right) = \left(\frac{\alpha_n}{\alpha_p}\right)^{n+1} \quad (15)$$

and

$$\omega_o = \left(\frac{\alpha_n\beta g_m}{C}\right)\tan\left(\frac{\pi}{2n}\right) \quad (16)$$

It should be mentioned here that the oscillation condition is mainly affected by the current transfer errors (α_p and α_n) of the CDTAs. However, the effect of these errors can be easily accommodated by tuning the ratio of g_{mx}/g_{my} (or I_x/I_y). Also, one can see that ω_o is slightly deviated from the ideal case by the factor of $\alpha_n\beta$. Therefore, to compensate this effect, it can be done by slightly adjusting the g_m-value.

The ω_o-sensitivity analysis with respect to the parameters of the active and passive element used can be given by:

$$S_{\alpha_p}^{\omega_o} = 0 \quad (17)$$

$$S_{\alpha_n}^{\omega_o} = S_{\beta}^{\omega_o} = S_{g_m}^{\omega_o} = 1 \quad (18)$$

and

$$S_C^{\omega_o} = -1 \quad (19)$$

Eqs. (17)–(19) show that the sensitivity values are within the range of $|S| \leqslant 1$ and, therefore, are low.

5. Simulation results

In order to validate the operation of the proposed current-mode MSO topology in Fig. 5, a six-phase MSO ($n = 3$) has been designed. The circuit was simulated using PSPICE program. The CDTA was performed by the schematic bipolar implementation given in Fig. 2 with the transistor model parameters of PR100N (PNP) and NP100N (NPN) of the bipolar arrays ALA400 from AT&T [20]. The power supply voltages were chosen to be $+V = -V = 3$ V and the values of the bias currents were equal to $I_A = 100\,\mu A$ and $I_B = 50\,\mu A$.

The output waveforms and frequency spectrums obtained from the proposed MSO structure of Fig. 5 are, respectively, shown in Figs. 7 and 8 with $I_O = 100\,\mu A$ and $C = 1$ nF. The simulated frequency of the oscillation was found to be 180 kHz, while the theoretically calculated frequency using Eq. (12) was 183 kHz. From the simulation results, the phase differences of i_{o2}, i_{o3}, i'_{o1}, i'_{o2} and i'_{o3} comparing with i_{o1} were respectively measured as 62°, 121°, 181°, 241° and 300°, which are very close to the corresponding predicted values. The total harmonic distortion (THD) in the output waveforms i_{o1}, i_{o2} and i_{o3} were approximated to 1.4%.

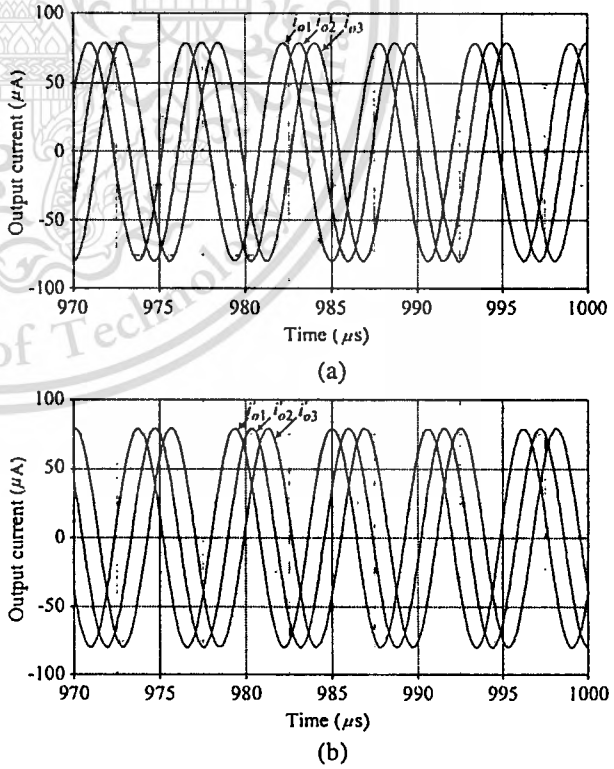

Fig. 7. Simulated output waveforms of the proposed current-mode MSO of Fig. 5. (a) i_{o1}, i_{o2}, i_{o3}; (b) i'_{o1}, i'_{o2}, i'_{o3}.

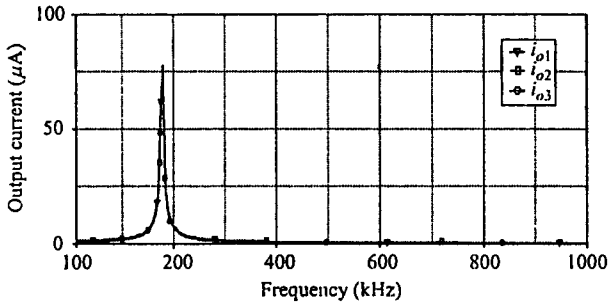

Fig. 8. Simulated frequency spectrums i_{o1}, i_{o2} and i_{o3}.

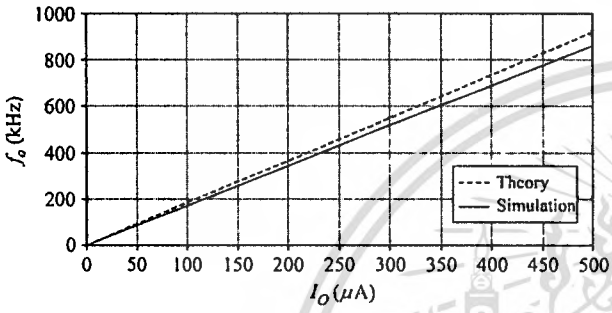

Fig. 9. Oscillation frequency (f_o) as a function of the bias currents I_O.

The variability of the oscillation frequency (f_o) as a function of the bias current (I_O) is shown in Fig. 9. It can be seen that the circuit exhibits a large tuning range. The difference between the theoretical and the simulation results especially in high bias current value region is mainly attributed to the deviation of the g_m-value that differs from the calculation value.

6. Concluding remarks

In this paper, an electronically controllable current-mode MSO topology is presented. The proposed MSO is implemented through the proposed CDTA-based current-mode first-order allpass filters and current-controlled current amplifier as the building blocks. The circuit can produce $2n$-phase of equally spaced in-phase output currents, and all of them have high output impedance, which can be directly cascaded in current-mode operations. Moreover, it provides the attractive feature of independent electronic control of the oscillation frequency (ω_o) and the oscillation condition by varying the bias current of the CDTA. It is demonstrated from PSPICE simulation that the results agree well with the theoretical analysis.

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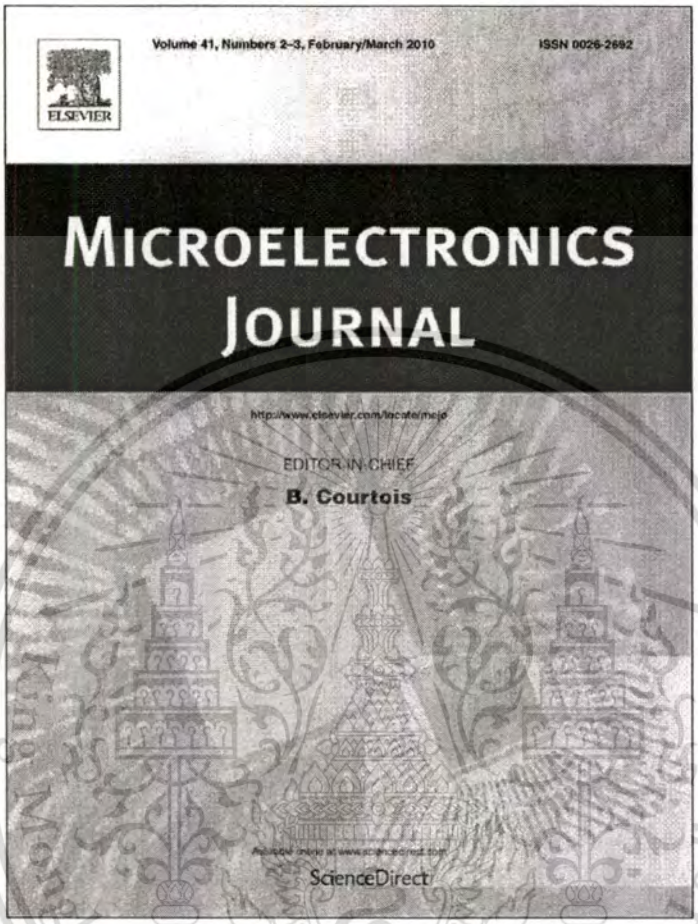

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Resistorless realization of current-mode first-order allpass filter using current differencing transconductance amplifiers

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ABSTRACT

This paper presents a realization of a current-mode first-order allpass filter using two current differencing transconductance amplifiers (CDTAs) as the active components and one virtually grounded capacitor as the only passive component. The proposed filer requires no external resistor and is electronically adjustable by varying the external bias current of the CDTA. No component-matching constraints are required. The circuit realizes both inverting and non-inverting types of allpass filters, and also exhibits high-output impedances, which are easy cascading in the current-mode operation. As an application of the proposed CDTA-based allpass section, a current-mode quadrature oscillator is realized. PSPICE simulation results are given to confirm the theoretical analysis.

1. Introduction

It is well known that the first-order allpass filter is widely used in several analog signal-processing applications. In general, it is used for phase shifting from 0° to 180° or from 180° to 0°, while keeping the amplitude of the signal constant over the frequency range of interest. It can also be used to realize universal biquadratic filters, to synthesize quadrature and multiphase oscillators, and to implement high quality-factor frequency selective filters. Current-mode circuits are receiving much attention because of their potential advantages such as wider bandwidth, wider dynamic range, simpler circuitry and lower power consumption. As a result, a number of current-mode first-order allpass filter realizations using different active building blocks were reported in the technical literature [1–12]. However, some of these networks suffer from the use of floating resistors or capacitors [1–6]. The networks reported in [6–8] use a number of passive elements with matching conditions, but provide high impedance outputs suited for current-mode cascading. Furthermore, most of the existed realizations do not include electronically tunability property [1–3,6–11]. Although first-order allpass sections with electronic tuning properties were reported in [4,5,13–15], the current-mode configurations of [4,5] do not exhibit high-output impedance while the works in [13–15] operated in voltage-mode. In [12], an electronically tunable current-mode first-order allpass filter realization was presented, which requires only current differencing transconductance amplifier (CDTA) and three passive components. Moreover, most of them usually realize either non-inverting or inverting types of allpass function [1–5,7–14]. For the realization of the complementary type, they need to change the circuit configuration. In view of above explanation, none of the earlier circuits are able to achieve all the desirable features simultaneously.

This paper presents the resistorless and cascadable current-mode first-order allpass filter employing only two CDTAs and a single-virtually grounded capacitor, which contains a minimum number of components. Due to electronically tunability property of the CDTA, the phase response of the proposed circuit can be adjusted by an external bias current. No component-matching conditions for realizing the allpass functions are required. The circuit can realize both inverting and non-inverting types of current-mode first-order allpass filters without changing circuit topology. The proposed circuit also exhibits high-output impedance, which is easy cascading in the current-mode operation. In view of the literature surveys, a comparison of the previously reported realizations from [1–12] and the proposed circuit introduced in this work is summarized in Table 1. It reveals that the proposed circuit is capable of achieving all the above-mentioned important parameters simultaneously. In order to illustrate the design utility of the proposed CDTA-based allpass section, an application in realizing of a current-mode quadrature sinusoidal oscillator is also given.

2. Circuit description

As shown in Fig. 1, the CDTA is a versatile current-mode active building block where p and n are input terminals, and z and x are

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Table 1
Comparison of proposed allpass filter with previously reported ones.

Allpass filters	Number of active elements	Number of passive elements	Without constraints/ conditions	High output impedance	Grounded/virtually grounded capacitors	Resistorless circuit	Electronically tunable	Realisability of both the allpass types
[1]	1	4	×	✓	×	×	×	×
[2]	1	3	×	×	✓	×	×	×
[3]	1	2	✓	×	✓	×	×	×
[4]	1/2	1	×/✓	×	×	✓	✓	×
[5]	1	2	×	×	×	✓	✓	×
[6]	1	5	×	✓	×	×	×	✓
[7]	2	4	×	✓	✓	×	×	×
[8]	2	3	×	✓	✓	×	×	×
[9]	1	2	✓	✓	✓	×	×	×
[10]	1	2	✓	✓	✓	×	×	×
[11]	1	2	✓	✓	✓	×	×	×
[12]	1	3	✓	✓	✓	×	✓	×
Proposed	2	1	✓	✓	✓	✓	✓	✓

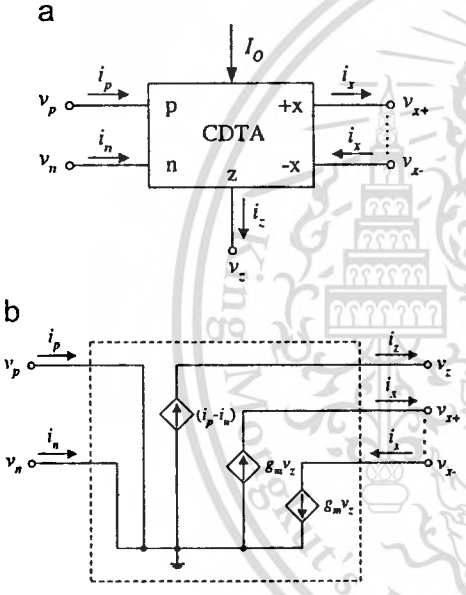


Fig. 1. CDTA: (a) circuit representation, (b) equivalent circuit.

output terminals. The port relations characterizing this device can be described by the following expressions [12,16]:

$$v_p = v_n = 0, \quad i_z = i_p - i_n \quad \text{and} \quad i_x = g_m v_z = g_m Z_z i_z \tag{1}$$

where g_m is the transconductance gain of the CDTA, and Z_z is an impedance connected at the terminal z. From Eq. (1) and Fig. 1(b), the current through the terminal z (i_z) follows the difference of the currents through the terminals p and n ($i_p - i_n$), and flows from the terminal z into an outside impedance Z_z. The voltage drop at the terminal z (v_z) is then transferred to a current at the terminal x (i_x) by a transconductance gain (g_m), which is generally controllable by an external bias current.

One possible bipolar realization of the CDTA circuit used in this work can be shown in Fig. 2 [17,18]. From the circuit diagram, transistors $Q_1 - Q_{11}$ function as an input stage (i.e., the current differencing circuit) followed by a multiple-output transconductance amplifier implemented by using transistors $Q_{12} - Q_{30}$. Thus, in this case, the transconductance gain g_m is directly proportional to the external bias current I_O, which can be written by:

$$g_m = \frac{I_O}{2V_T} \tag{2}$$

where $V_T \cong 26$ mV at 27 °C is the thermal voltage.

Fig. 3 shows the proposed resistorless current-mode first-order allpass filter with electronic tuning properties employing only two CDTAs and one virtually grounded capacitor. Due to internally grounded input terminals of the CDTA, one end of the capacitor C connected in the structure is effectively grounded and the problem associated with this capacitor is not expected. Therefore, the proposed configuration is a canonical structure and is compatible with monolithic implementation. A routine analysis of the circuit using the describing equations given in Eq. (1) yields the following current transfer function:

$$\frac{I_{AP+}}{I_{in}} = -\frac{I_{AP-}}{I_{in}} = \frac{1 - s\left(\frac{C}{g_{m1}}\right)}{1 + s\left(\frac{C}{g_{m1}}\right)}. \tag{3}$$

From Eq. (3), it can be seen that the circuit can realize both non-inverting and inverting type first-order allpass functions. As it is demonstrated in Fig. 3, the proposed CDTA-based allpass section does not require any external passive resistor, and any matching conditions for realizing first-order allpass function. Here, the pole frequency of the circuit is expressed as:

$$\omega_o = \frac{g_{m1}}{C} = \frac{I_{O1}}{2V_T C}, \tag{4}$$

and the phase responses are respectively given by:

$$\phi_{AP+} = -2\tan^{-1}\left(\frac{\omega C}{g_{m1}}\right) \tag{5}$$

and

$$\phi_{AP-} = 180^\circ - 2\tan^{-1}\left(\frac{\omega C}{g_{m1}}\right). \tag{6}$$

Eqs. (5) and (6) show that the proposed allpass filter can provide phase shifting both between $0-180^\circ$ and $180^\circ-0^\circ$. Moreover, the shifted phase value can be controlled electronically by adjusting I_{O1}.

3. Effects of non-ideal CDTA

In this section, the proposed allpass circuit is studied taking into account the non-idealities of the CDTA. Considering the parasitics and transfer errors, the simplified equivalent circuit

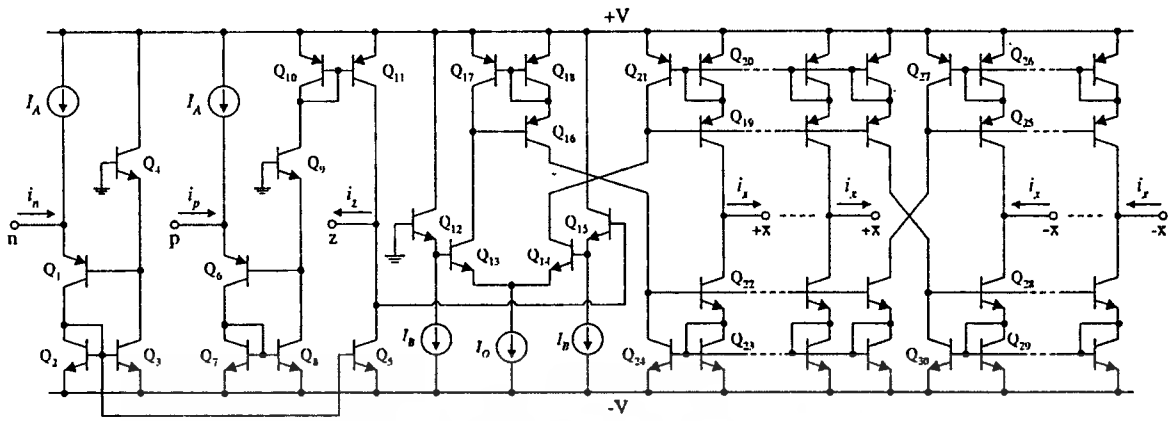


Fig. 2. Possible bipolar realization of the CDTA.

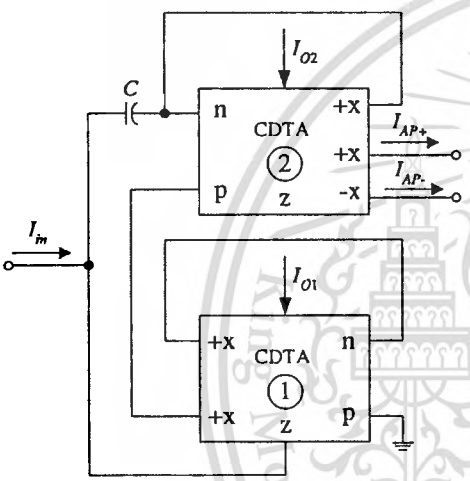


Fig. 3. Proposed CDTA-based current-mode first-order allpass filter.

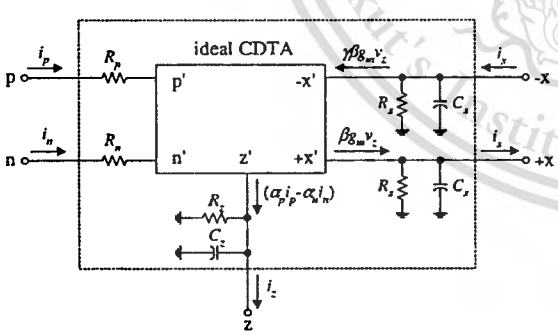


Fig. 4. Simplified equivalent circuit of the non-ideal CDTA.

represented the behavior of the non-ideal CDTA can be illustrated in Fig. 4 [19]. These result from the series input resistances R_p and R_n at terminals p and n, and the shunt output impedances ($R_z//C_z$ and $R_x//C_x$) at terminals z and x, respectively. More specifically, α_p, α_n, γ and β are the parasitic current gains between the p–z, n–z, and $+x$ to $-x$ terminals, and transconductance inaccuracy factor between the z to $+x$ terminals of the CDTA, respectively. Normally, the parameters α_p, α_n, γ and β are deviated from their idea unity values by the tracking errors. Thus, by taking these effects into consideration, the non-ideal current transfer functions for the proposed circuit of Fig. 3 can be expressed as:

$$\frac{I_{AP+}}{I_{in}} = \left[\frac{\left(\frac{\alpha_{p2}}{\alpha_{n2}}\right)}{1+\left(\frac{1}{\alpha_{n2}\beta_2 g_{m2} R_{z2}}\right)+s\left(\frac{C_{z2}}{\alpha_{n2}\beta_2 g_{m2}}\right)}\right]\left[\frac{1-sC\left(\frac{\alpha_{n2}}{\alpha_{p2}\alpha_{n1}\beta_1 g_{m1}}+\frac{\alpha_{n2}R_{p2}}{\alpha_{p2}}-R_{n2}\right)}{1+sC\left(\frac{1}{\alpha_{n1}\beta_1 g_{m1}}+R_{p2}+R_{n2}\right)}\right] \tag{7}$$

and

$$\frac{I_{AP-}}{I_{in}} = \left[\frac{-\left(\frac{\alpha_{p2}\gamma_2}{\alpha_{n2}}\right)}{1+\left(\frac{1}{\alpha_{n2}\beta_2 g_{m2} R_{z2}}\right)+s\left(\frac{C_{z2}}{\alpha_{n2}\beta_2 g_{m2}}\right)}\right]\left[\frac{1-sC\left(\frac{\alpha_{n2}}{\alpha_{p2}\alpha_{n1}\beta_1 g_{m1}}+\frac{\alpha_{n2}R_{p2}}{\alpha_{p2}}-R_{n2}\right)}{1+sC\left(\frac{1}{\alpha_{n1}\beta_1 g_{m1}}+R_{p2}+R_{n2}\right)}\right] \tag{8}$$

where R_{pi}, R_{ni}, R_{zi}, α_{pi}, α_{ni}, γ_i, β_i and C_{zi} denote the parameters R_p, R_n, R_z, α_p, α_n, γ, β and C_z of the i-th CDTA (i=1, 2), respectively. Since usually $R_{z2} \gg 1$ and $(1/\alpha_{n1}\beta_1 g_{m1}) \gg R_{p2}$, R_{n2}, Eqs. (7) and (8) are approximately

$$\frac{I_{AP+}}{I_{in}} \cong \left[\frac{\left(\frac{\alpha_{p2}}{\alpha_{n2}}\right)}{1+s\left(\frac{C_{z2}}{\alpha_{n2}\beta_2 g_{m2}}\right)}\right]\left[\frac{1-s\left(\frac{C}{\alpha_{n1}\beta_1 g_{m1}}\right)\left(\frac{\alpha_{n2}}{\alpha_{p2}}\right)}{1+s\left(\frac{C}{\alpha_{n1}\beta_1 g_{m1}}\right)}\right] \tag{9}$$

and

$$\frac{I_{AP-}}{I_{in}} \cong \left[\frac{-\left(\frac{\alpha_{p2}\gamma_2}{\alpha_{n2}}\right)}{1+s\left(\frac{C_{z2}}{\alpha_{n2}\beta_2 g_{m2}}\right)}\right]\left[\frac{1-s\left(\frac{C}{\alpha_{n1}\beta_1 g_{m1}}\right)\left(\frac{\alpha_{n2}}{\alpha_{p2}}\right)}{1+s\left(\frac{C}{\alpha_{n1}\beta_1 g_{m1}}\right)}\right] \tag{10}$$

It is apparent from Eqs. (9) and (10) that the filter gain (H) is now dependent on the parasitic current gains α_{p2}, α_{n2} and γ_2 of the CDTA2. To eliminate this effect, a careful circuit realization of CDTA, which provides $\alpha_p \cong \alpha_n \cong \gamma \cong 1$, should be strictly considered. Similarly, the pole frequency ω_o of the proposed circuit is slightly deviated from the ideal case by the factor $\alpha_{n1}\beta_1$. However, we can also alleviate the effect of this factor by trimming the g_{m1}-value. It is further noted that one extra pole ($\omega_p = \alpha_{n2}\beta_2 g_{m2}/C_{z2}$) due to the parasitic elements appears in the filter characteristic. For a practical CDTA, $C_{z2} \ll C$, the frequency of ω_p is sufficiently higher than ω_o of the proposed allpass circuit ($\omega_p \gg \omega_o$), thus the influence of ω_p on the frequency response can be ignored.

The incremental sensitivities of H and ω_o to active and passive components for the proposed allpass filter described by Eqs. (9) and (10) are analyzed and also found as:

$$S^H_{\alpha_{p2}} = -S^H_{\alpha_{n2}} = S^H_{\gamma_2} = 1, \quad S^H_{\alpha_{p1},\alpha_{n1},\beta_1,\beta_2,g_{m1}} = S^H_C = 0 \tag{11}$$

and

$$S^{\omega_o}_{\alpha_{n1},\beta_1,g_{m1}} = -S^{\omega_o}_C = 1, \quad S^{\omega_o}_{\alpha_{p1},\alpha_{p2},\alpha_{n2},\beta_2} = 0 \tag{12}$$

It is evident that the H and ω_o sensitivities are within unity in magnitude. Also, note from the sensitivity results that H is only sensitive to variations of tracking errors of the CDTA2. On the

other hand, these errors have no influence on ω_o. To further illustrate this point, for instance, let us assume that $\alpha_{p2}=\alpha_{n2}=\gamma_2\cong 0.99$ (a -1% change from their theoretical values, i.e., the unity value). From the defining relation for H sensitivity in Eq. (11), we can find

$$\frac{\Delta H}{H}=\left(\frac{\Delta\alpha_{p2}}{\alpha_{p2}}\right)S^H_{\alpha_{p2}}+\left(\frac{\Delta\alpha_{n2}}{\alpha_{n2}}\right)S^H_{\alpha_{n2}}+\left(\frac{\Delta\gamma_2}{\gamma_2}\right)S^H_{\gamma_2}$$
$$=(-0.01)(1)+(-0.01)(-1)+(-0.01)(1)=-0.01$$

We may conclude, therefore, that the total effect of a -1% change in the values of α_{p2}, α_{n2} and γ_2 will produce a -1% change in the gain H. Clearly, in this case, H is reduced by 1%, a -1% error.

4. Simulation results

PSPICE program was carried out to check the workability of the proposed circuit of Fig. 3. For the simulation purpose, the CDTA given in Fig. 2 was constructed with the transistor model parameters of PR100N (PNP) and NP100N (NPN) [20] and DC supply voltages of ± 2 V. The designed capacitor value and the bias currents of the CDTAs were chosen as: $C=1$ nF, $I_{O1}=100\,\mu$A and $I_{O2}=10\,\mu$A, which leads to achieve $f_o=\omega_o/2\pi\cong 318$ kHz, $\phi_{AP-}\cong 90°$ and $\phi_{AP+}\cong 270°$. Fig. 5 shows the time domain responses of the proposed filters in which 100 μA peak sinusoidal input current at 318 kHz is applied. This causes the time shifts of 805 nS and 2.38 μS at the filter outputs corresponding to the phase shifts of about 92.3° and 271.1°, respectively, which are in good agreement with the theoretical analysis. In Fig. 6, the simulated frequency domain responses of the proposed filters are also shown for the designed component values as given above. The simulated phase-frequency plots of both types of the allpass filters for three different bias current values are depicted in Fig. 7. It can be observed that the electronically controllability of the phase response can be achieved through I_{O1}.

With the above designed component values, the variation of the total power consumption with the pole frequency f_o for the proposed allpass filter of Fig. 3 is shown in Fig. 8. It is obvious from the curve that the total power consumption is found low and remains within 9 mW through the wide frequency range 10 kHz–1 MHz. Thus, the results confirm the practical low-power operation of the circuit.

As an application example, a current-mode quadrature sinusoidal oscillator is realized by cascading the proposed allpass filter of Fig. 3 and CDTA-based lossless integrator (CDTA3 and C_2),

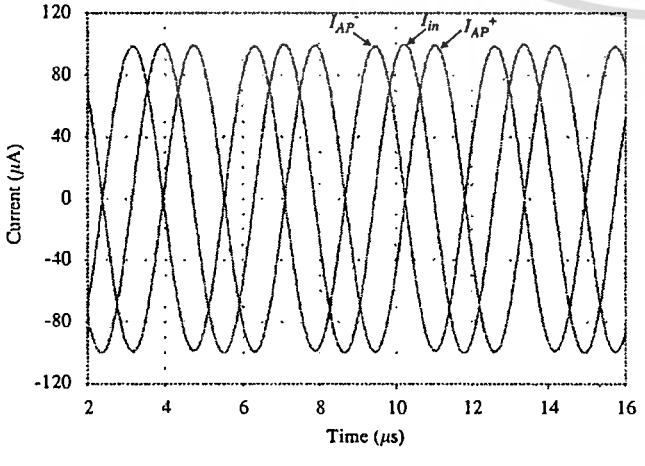
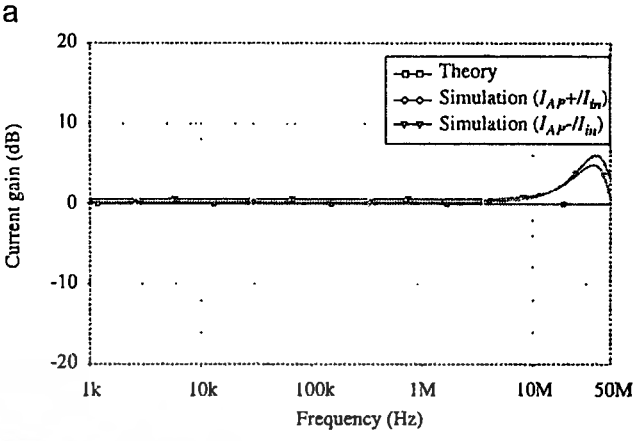


Fig. 5. Time domain responses of the proposed allpass filter.



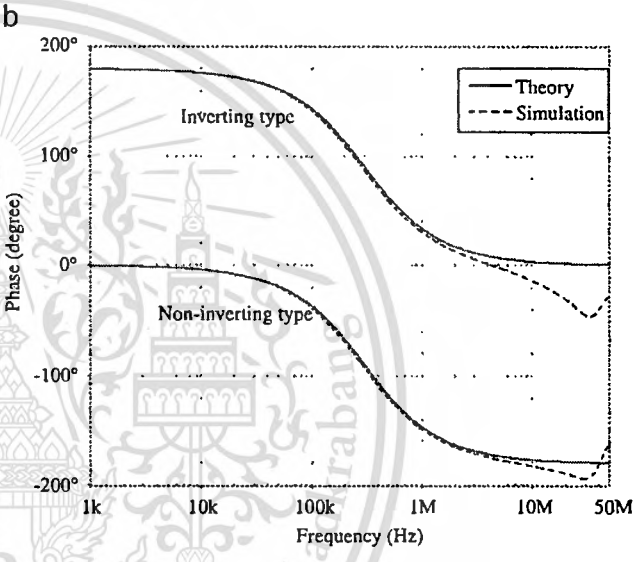


Fig. 6. Frequency responses of the proposed allpass filter: (a) magnitude–frequency responses, (b) phase-frequency responses.

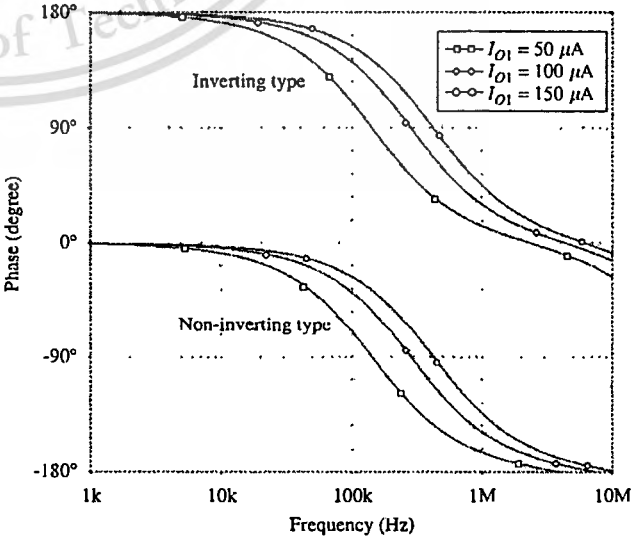


Fig. 7. Simulated phase responses of the proposed allpass filters when I_{o1} is varied.

and closing the circuit's loop to provide a unity loop gain at the pole frequency [21]. The resulting circuit is shown in Fig. 9. In this case, the oscillation condition and the oscillation frequency (ω_{osc}) obtained from the circuit can respectively be found as:

$$g_{m1}C_2 = g_{m3}C_1 \tag{13}$$

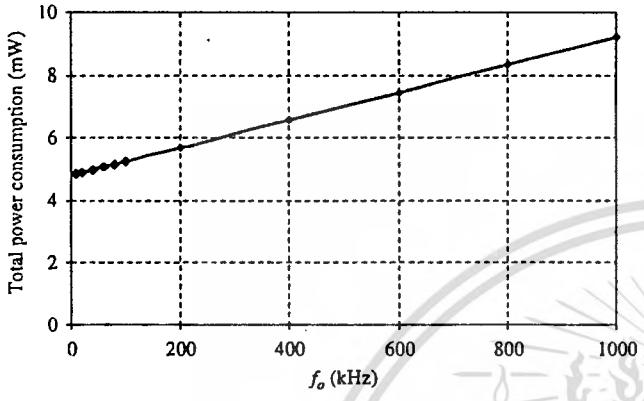


Fig. 8. Variation of total power consumption as a function of f_o.

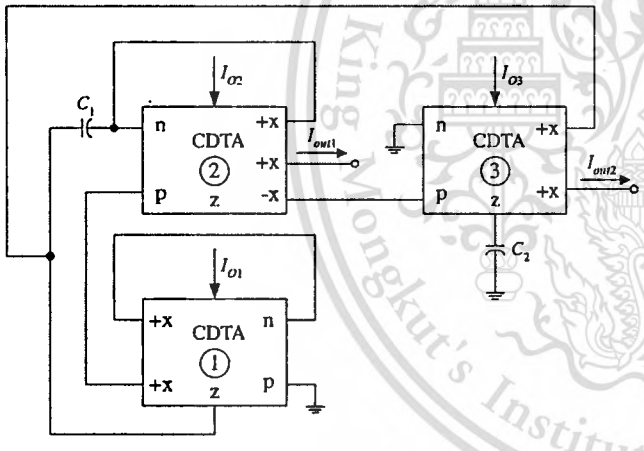


Fig. 9. Application example of current-mode quadrature oscillator realized by cascading the proposed allpass filter and lossless integrator.

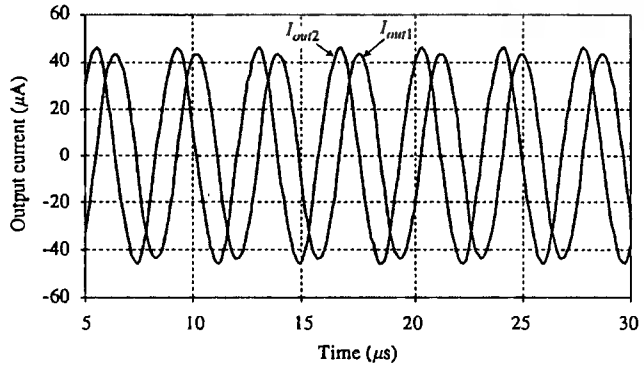


Fig. 10. Simulated output currents of the current-mode quadrature oscillator of Fig. 9.

and

$$\omega_{osc} = \sqrt{\frac{g_{m1}g_{m3}}{C_1C_2}} \tag{14}$$

Fig. 10 shows simulated time domain responses of the quadrature output currents I_{out1} and I_{out2}, which demonstrates the 90° phase-shift waveforms. For this purpose, the designed component values are chosen as: $I_{O1}=I_{O2}=I_{O3}=100\,\mu A$ and $C_1=C_2=1$ nF, which results in the oscillation frequency of $f_{osc}=\omega_{osc}/2\pi \cong 318$ kHz. From the simulation results, the circuit gives the oscillation frequency as $f_{osc}=283$ kHz, and the total harmonic distortion (THD) is found as 1.69%. Also, the total power consumption is found to be less than 9.89 mW.

5. Conclusion

In this work, a canonical current-mode first-order allpass filter is presented. It can realize both inverting and non-inverting type allpass filtering functions by using only two CDTAs and one virtually grounded capacitor. The proposed circuit has following advantages: (a) the phase shift can be electronically tuned by an external bias current; (b) no matching condition is imposed for realizing the allpass functions; (c) since all the outputs are provided through high-output impedance terminals, it can be directly connected to the next stage without any impedance matching requirement. The important features of the propose circuit are compared with those of previous works in Table 1.

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Structural generation of two integrator loop filters using CDTAs and grounded capacitors

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SUMMARY

A versatile family of two integrator loop filter structures using current differencing transconductance amplifiers (CDTAs) and grounded capacitors is generated. The basic filter building blocks consist of current proportional blocks, current lossless integrators and a current lossy integrator based on the use of CDTAs as the major active components. It is demonstrated that the derived filter structures can realize a general class of second-order current transfer functions. Since the resulting structures contain only CDTAs and grounded capacitors, they are general and very appropriate for integration, cascading and electronic tuning. The influences of the CDTA non-idealities are also discussed. The functionality of the resulting filters has been verified by simulation results. Copyright © 2009 John Wiley & Sons, Ltd.

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KEY WORDS: current differencing transconductance amplifier (CDTA); integrator loop; biquad filters; current-mode circuits

1. INTRODUCTION

Recently, a new current-mode active building block with two current inputs and two kinds of current outputs, namely current differencing transconductance amplifier (CDTA), was first introduced by Biolek in 2003 [1]. The CDTA is composed of a unity-gain current source controlled by the difference of two input currents and a multi-output transconductance amplifier providing electronic tuning ability through its transconductance gain (g_m). Therefore, this device is quite suitable for the synthesis of current-mode filters with electronically tunability properties. Moreover, the use of the CDTA as an active element provides the circuit implementations with a reduced number

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of passive elements, thereby leading to compact structures in some applications [2, 3]. All these advantages together with its current-mode operation nature make the CDTA a promising choice for implementing the current-mode continuous-time signal processing circuits. Consequently, a number of CDTA applications have been reported in the technical literature [1–10].

Two integrator loop structures are very popular and useful blocks to realize biquad filters [11–14]. Nawrocki and Klein proposed a two-integrator loop universal biquad with single-input and single-output using eight operational transconductance amplifiers (OTAs) and two grounded capacitors [11]. In 1988, Sanchez-Sinencio *et al.* have systematically summarized and extended the work on the two-integrator loop OTA-C filters based on the block diagram method [12]. In [13], the author developed the Nawrocki and Klein biquad to derive many new filter structures. However, all the above-mentioned methods are based on the voltage-mode approach. Moreover, some obtained filter structures in [12] need the capacitor injection of excitation signals in the circuit design, which are not suitable for cascade implementation, and the resulting floating capacitors are not suitable for the integrated circuit (IC) implementation [15, 16]. In 1996, a comprehensive set of current-mode continuous-time two integrator loop filter structures incorporating dual-output OTA and capacitors was developed in [14]. However, the structures also require capacitor injection of excitation signals, which do not exhibit the feature of low-impedance inputs.

Of the various methods of current-mode biquad filter design, those based upon second-generation current conveyors (CCIIs) have been reported in the literature [17–24]. However, most of them still require capacitor injection of input signal currents [17–19, 21, 23, 24], whereas the others also require an input current injection into the external grounded resistance or internal parasitic resistance connected at the input terminal [17, 18, 20, 22, 23]. Thus, the low-input impedance characteristic is not recommended for these structures. Ideally, it is preferred that the current-mode filters should provide low-input and high-output impedances for easy cascadability to implement the higher-order filter and generation of additional filter responses by simply connecting two or more responses.

Therefore, this paper largely focuses on presenting a structural generation to synthesize the two integrator loop filters with CDTAs. The proposed configurations employ the current proportional blocks and current integrators based on CDTAs as the basic building units. By suitably selecting the input and output currents, the derived filters can realize all the standard biquadratic filters from the same configuration. The resulting filter characteristics can be electronically adjusted with separate tunable transconductances. All the filter structures contain only grounded capacitors, which are helpful for easing the IC implementation. In addition, all the proposed filters exhibit both low-input and high-output impedance levels, thus permitting easy cascadability.

2. CURRENT DIFFERENCING TRANSCONDUCTANCE AMPLIFIER (CDTA)

Using the standard notation for the CDTA whose electrical symbol is shown in Figure 1, it can be characterized by the following constitutive equations:

$$v_p = v_n = 0, \quad i_z = i_p - i_n \quad \text{and} \quad i_x = g_m v_z = g_m Z_z i_z \tag{1}$$

where p and n are input terminals, z and $\pm x$ are output terminals, g_m is the transconductance gain, and Z_z is an external impedance connected at the terminal z. According to Equation (1), the current flowing out of the terminal z (i_z) is a difference between the input currents through

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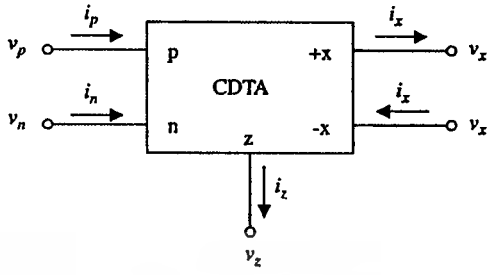

Figure 1. An electrical symbol for the CDTA.

the terminals p and n (i_p–i_n). The voltage drop at the terminal z is transferred to a current at the terminal x (i_x) by a transconductance gain (g_m) of the CDTA.

3. BASIC CDTA-BASED BUILDING BLOCKS

This section introduces the basic CDTA-based building blocks involved for the synthesis procedures. Figure 2 illustrates the current proportional block and current integrators, based on the realization with a single CDTA [6, 9], which will be used as essential units to construct the proposed filter structures. In Figure 2(a), the current transfer relationship of the unit is found to be:

$$I_o = \left(\frac{g_m}{Y}\right)(I_{i1} - I_{i2}) \tag{2}$$

It should be emphasized from Equation (2) that the current proportional block and the current lossless integrator correspond to the conditions: $Y = g_1$ (conductance) and $Y = sC_1$, respectively.

In Figure 2(b), the current lossy integrator is realized with the following transfer function:

$$I_o = \left(\frac{g_m}{g_2 + sC_2}\right)(I_{i1} - I_{i2}) \tag{3}$$

In a practical viewpoint, the conductances g_1 and g_2 in the structures of Figures 2(a) and (b) may be realized by the proper connection of the CDTA as shown in Figure 3 [9]. Therefore, by replacing g_1 and g_2 of Figure 2 with the controlled resistance of Figure 3, the usage of external passive resistors is not necessary for these filter structures, which is especially important for achieving the higher integration.

4. GENERATION OF TWO INTEGRATOR LOOP CDTA FILTER STRUCTURES

Basically, the two integrator loop structures consist of a lossless integrator and a lossy integrator. Figure 4 shows four different block diagram representations of the basic two-integrator loop operation that will be used to illustrate the proposed approach. Observe that Figures 4(a) and (c) contain two negative-feedback loops including two lossless integrators ($1/s\tau_1$ and $1/s\tau_2$) and two proportional gain blocks (A_0, A_1 and A_0, A_2), while Figures 4(b) and (d) contain a single

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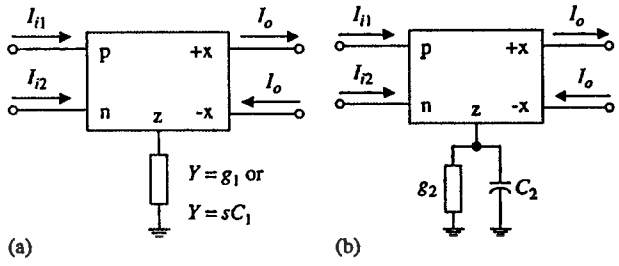

Figure 2. Basic CDTA-based building blocks.

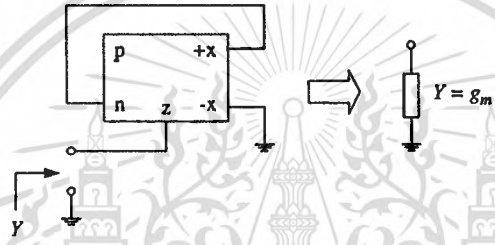

Figure 3. CDTA-based controlled resistance.

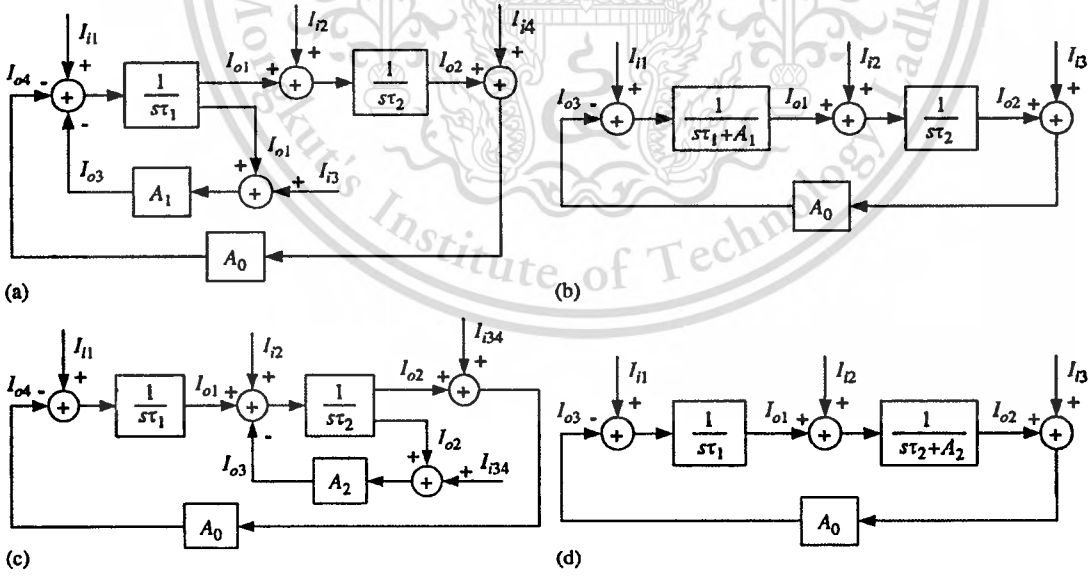

Figure 4. Two integrator loop structures: (a) configuration A; (b) configuration B; (c) configuration C; and (d) configuration D.

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negative-feedback loop consisting of one lossy integrator, one lossless integrator and one proportional gain block. In considering two-integrator loop configurations of Figures 4(a) and (b), the characteristic equation is identical and can be given by

$$D_1(s)=s^2\tau_1\tau_2+s\tau_2A_1+A_0 \tag{4}$$

where τ_1 and τ_2 are the integrator time constants. Hence, the natural angular frequency (ω_o), bandwidth (BW) and quality factor (Q) for both configurations, respectively, become

$$\omega_o=\sqrt{\frac{A_0}{\tau_1\tau_2}} \tag{5}$$

$$\mathrm{BW}=\frac{A_1}{\tau_1} \tag{6}$$

and

$$Q=\frac{1}{A_1}\sqrt{\frac{A_0\tau_1}{\tau_2}} \tag{7}$$

In a similar way, we can obtain the same characteristic equation for both two-integrator loop configurations of Figures 4(c) and (d), written by:

$$D_2(s)=s^2\tau_1\tau_2+s\tau_1A_2+A_0 \tag{8}$$

The parameters ω_o, BW and Q are, respectively, obtained as

$$\omega_o=\sqrt{\frac{A_0}{\tau_1\tau_2}} \tag{9}$$

$$\mathrm{BW}=\frac{A_2}{\tau_2} \tag{10}$$

and

$$Q=\frac{1}{A_2}\sqrt{\frac{A_0\tau_2}{\tau_1}} \tag{11}$$

Let us now consider the CDTA-based circuit implementations of architectures of Figure 4. By employing the basic current building blocks in Figure 2, we can realize Figure 4 in the current-mode domain. The corresponding circuits derived from four block diagram structures of Figures 4(a)–(d) are shown in Figures 5(a)–(d), respectively. The mathematical expressions for the corresponding parameters ω_o, BW and Q, given in Equations (5)–(7) and (9)–(11), for all the derived realizations are summarized in Table I. All the possible current transfer functions derived from Figures 5(a)–(d)

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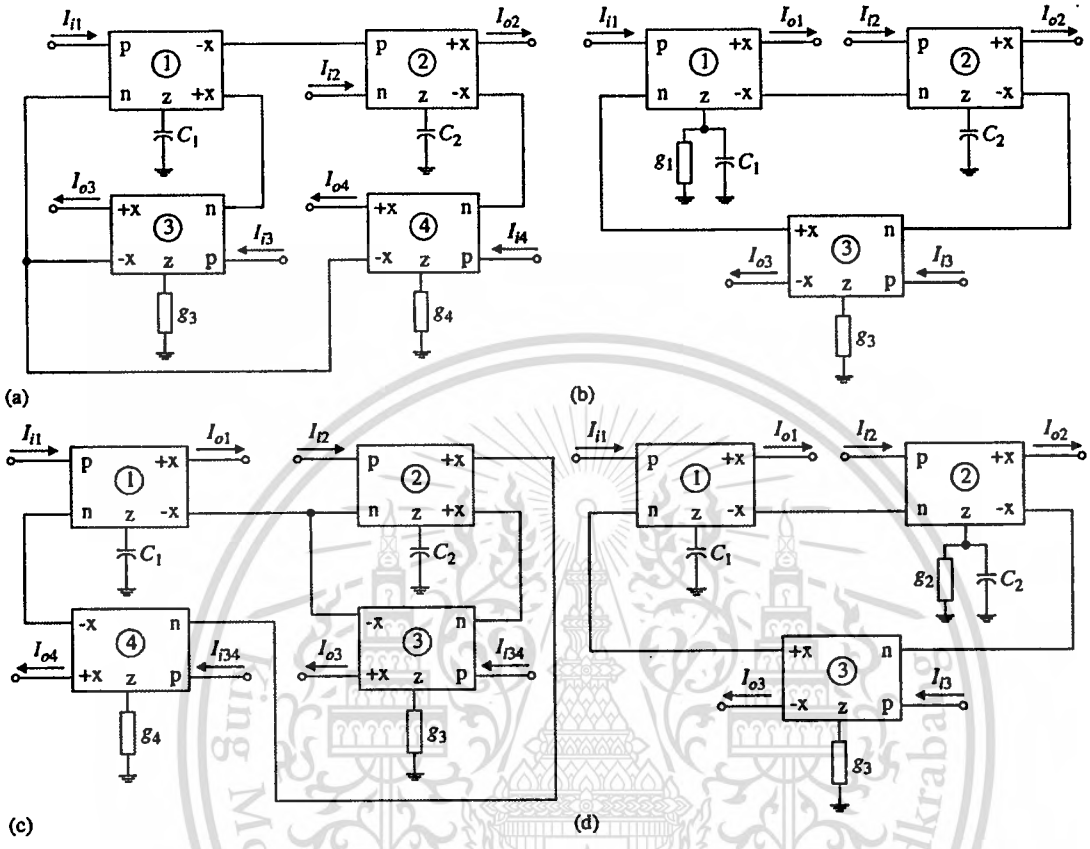

Figure 5. Generation of CDTA-based biquadratic filter configurations based on two integrator loop structures of Figure 4: (a) configuration A; (b) configuration B; (c) configuration C; and (d) configuration D.

are formulated by the following expressions, where $D_1(s)$ and $D_2(s)$ are the same as Equations (4) and (8), respectively.

For Figure 5(a),

$$
\begin{aligned}
I_{o2} &= \frac{-I_{i1}+(s\tau_1+A_1)I_{i2}-A_1I_{i3}-A_0I_{i4}}{D_1(s)} \\
I_{o3} &= \frac{-(s\tau_2A_1)I_{i1}+(A_0A_1)I_{i2}+A_1(s^2\tau_1\tau_2+A_0)I_{i3}-(s\tau_2A_0A_1)I_{i4}}{D_1(s)} \\
I_{o4} &= \frac{-A_0I_{i1}-A_0(s\tau_1+A_1)I_{i2}-(A_0A_1)I_{i3}-s\tau_2A_0(s\tau_1+A_1)I_{i4}}{D_1(s)} \\
I_{o3}+I_{o4} &= \frac{-(s\tau_2A_1+A_0)I_{i1}-(s\tau_1A_0)I_{i2}+(s^2\tau_1\tau_2A_1)I_{i3}+(s^2\tau_1\tau_2A_0)I_{i4}}{D_1(s)}
\end{aligned}
\tag{12}
$$

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Table I. Expressions for the filter parameters of Figure 5.

Configurations	A_0	A_1	A_2	τ_1	τ_2	ω_o	BW	Q
Configuration A, Figure 5(a)	$\frac{g_{m4}}{g_4}$	$\frac{g_{m2}}{g_3}$	–	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}g_{m4}}{g_4C_1C_2}}$	$\frac{g_{m1}g_{m2}}{g_3C_1}$	$\frac{g_2}{g_{m3}}\sqrt{\frac{g_{m2}g_{m4}C_1}{g_{m1}g_4C_2}}$
Configuration B, Figure 5(b)	$\frac{g_{m3}}{g_3}$	$\frac{g_1}{g_{m1}}$	–	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}g_{m3}}{g_3C_1C_2}}$	$\frac{g_1}{C_1}$	$\frac{1}{g_1}\sqrt{\frac{g_{m1}g_{m2}g_{m3}C_1}{g_3C_2}}$
Configuration C, Figure 5(c)	$\frac{g_{m4}}{g_4}$	–	$\frac{g_{m3}}{g_3}$	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}g_{m4}}{g_4C_1C_2}}$	$\frac{g_{m2}g_{m3}}{g_3C_2}$	$\frac{g_2}{g_{m3}}\sqrt{\frac{g_{m1}g_{m4}C_2}{g_{m2}g_4C_1}}$
Configuration D, Figure 5(d)	$\frac{g_{m3}}{g_3}$	–	$\frac{g_2}{g_{m2}}$	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}g_{m3}}{g_3C_1C_2}}$	$\frac{g_2}{C_2}$	$\frac{1}{g_2}\sqrt{\frac{g_{m1}g_{m2}g_{m3}C_2}{g_3C_1}}$

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For Figure 5(b),

$$I_{o1} = \frac{(s\tau_2)I_{i1} - A_0 I_{i2} - (s\tau_2 A_0)I_{i3}}{D_1(s)}$$
$$I_{o2} = \frac{I_{i1} + (s\tau_1 + A_1)I_{i2} - A_0 I_{i3}}{D_1(s)} \tag{13}$$
$$I_{o3} = \frac{A_0 I_{i1} + A_0(s\tau_1 + A_1)I_{i2} + s\tau_2 A_0(s\tau_1 + A_1)I_{i3}}{D_1(s)}$$

For Figure 5(c),

$$I_{o1} = \frac{(s\tau_2 + A_2)I_{i1} - A_0 I_{i2} - (s\tau_2 A_0)I_{i34}}{D_2(s)}$$
$$I_{o3} = \frac{-A_2 I_{i1} - (s\tau_1 A_2)I_{i2} + (s^2\tau_1\tau_2 A_2)I_{i34}}{D_2(s)} \tag{14}$$
$$I_{o4} = \frac{-A_0 I_{i1} - (s\tau_1 A_0)I_{i2} + (s^2\tau_1\tau_2 A_0)I_{i34}}{D_2(s)}$$

For Figure 5(d),

$$I_{o1} = \frac{(s\tau_2 + A_2)I_{i1} - A_0 I_{i2} - A_0(s\tau_2 + A_2)I_{i3}}{D_2(s)}$$
$$I_{o2} = \frac{I_{i1} + (s\tau_1)I_{i2} - A_0 I_{i3}}{D_2(s)} \tag{15}$$
$$I_{o3} = \frac{A_0 I_{i1} + (s\tau_1 A_0)I_{i2} + s\tau_1 A_0(s\tau_2 + A_2)I_{i3}}{D_2(s)}$$

It should be noted from Equations (12)–(15) that, by suitably connecting the input current terminals, all five standard biquadratic filtering signals can be realized. From Equation (12), it can readily be seen that the proposed filter configuration of Figure 5(a) can provide lowpass (LP), highpass (HP), bandpass (BP), bandstop (BS) and allpass (AP) current responses with different inputs and outputs. It is further noted from Equation (12) that the output current $I_{o3} + I_{o4}$ can easily be obtained by connecting two corresponding terminals together. Equations (13) and (15) also show that the configurations in Figures 5(b) and (d) realize LP and BP characteristics, while Equation (14) indicates that Figure 5(c) provides LP, HP and BP characteristics. It may be stated here that all of the above multifunction biquadratic filters can be realized without any constraints on the component values, and all the proposed configurations exhibit both low-input and high-output impedance characteristics, which will be more convenient in terms of cascading and connecting to other networks.

Furthermore, special types of CDTA-based biquadratic filters can be realized from Figure 4 by appropriately setting the proportional gain $A_i = 1$ $(i = 0, 1)$. Recall that when A_0 or A_1 becomes unity, they can simply be replaced by the short-circuit connection. The CDTA-based filter realizations derived from the configuration A of Figure 4(a) with $A_0 = 1$, $A_1 = 1$ and $A_0 = A_1 = 1$ are, respectively, shown in Figures 6(a)–(c). The realizations of Figures 6(d) and (e) are constructed with $A_0 = 1$ of Figures 4(b) and (d), respectively. Table II summarizes the expressions for all the

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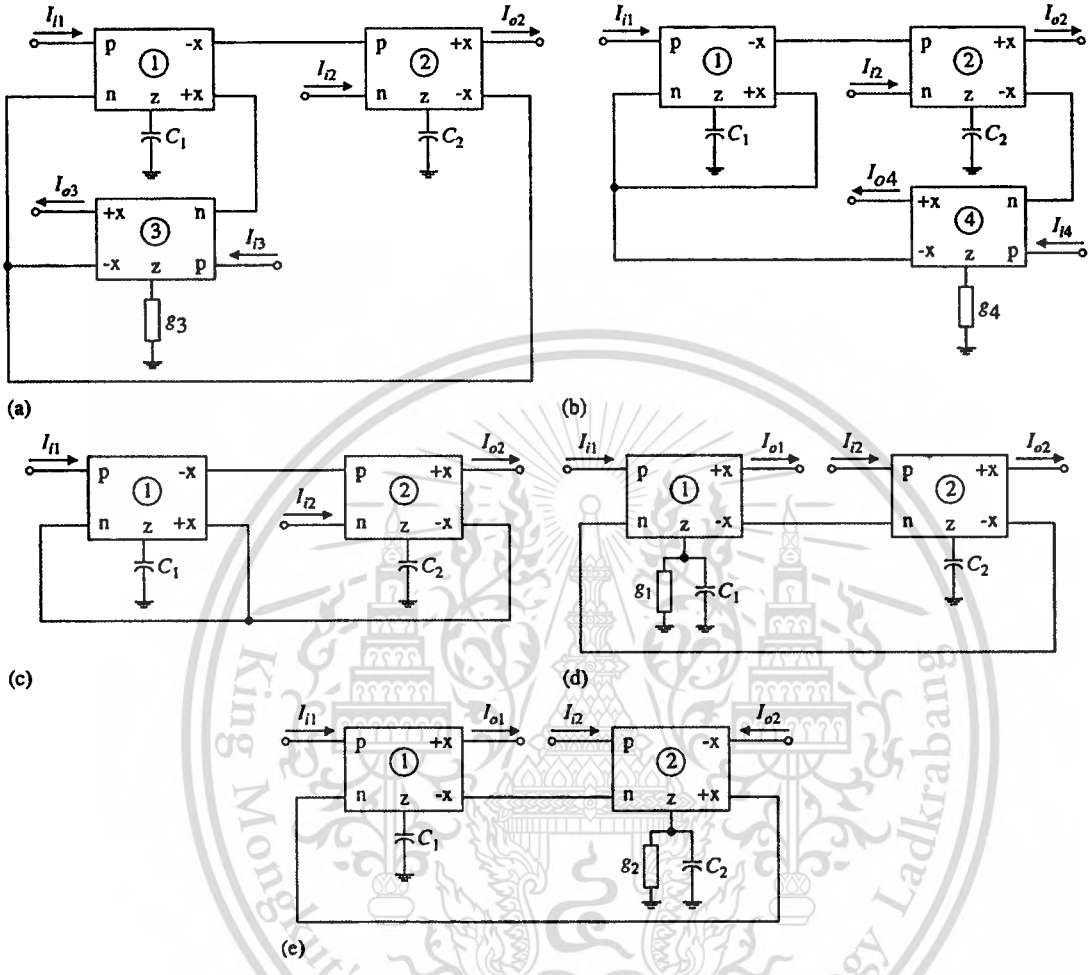

Figure 6. Special types of CDTA-based biquadratic filters of Figure 4: (a) configuration A (when $A_0=1$); (b) configuration A (when $A_1=1$); (c) configuration A (when $A_0=A_1=1$); (d) configuration B (when $A_0=1$); and (e) configuration D (when $A_0=1$).

filter parameters for the derived structures obtained from Figure 6. According to Figures 6(a)–(e), the explicit expressions for the current transfer functions can be derived as follows:

For Figure 6(a),

$$I_{o2}=\frac{-I_{i1}-(s\tau_1+A_1)I_{i2}-A_1I_{i3}}{D_1(s)}$$

$$I_{o3}=\frac{-(s\tau_2A_1)I_{i1}+A_1I_{i2}+A_1(s^2\tau_1\tau_2+1)I_{i3}}{D_1(s)} \tag{16}$$

$$I_{o2}+I_{o3}=\frac{-(s\tau_2A_1+1)I_{i1}-(s\tau_1)I_{i2}+(s^2\tau_1\tau_2A_1)I_{i3}}{D_1(s)}$$

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Table II. Expressions for the filter parameters of Figure 6.

Configurations	A_0	A_1	A_2	τ_1	τ_2	ω_o	BW	Q
Configuration A, ($A_0=1$) Figure 6(a)	1	$\frac{g_{m2}}{g_3}$	–	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$	$\frac{g_{m1}g_{m3}}{g_3C_1}$	$\frac{g_3}{g_{m3}}\sqrt{\frac{g_{m2}C_1}{g_{m1}C_2}}$
Configuration A, ($A_1=1$) Figure 6(b)	$\frac{g_{m4}}{g_4}$	1	–	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}g_{m4}}{g_4C_1C_2}}$	$\frac{g_{m1}}{C_1}$	$\sqrt{\frac{g_{m2}g_{m4}C_1}{g_{m1}g_4C_2}}$
Configuration A, ($A_0=A_1=1$) Figure 6(c)	1	1	–	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$	$\frac{g_{m1}}{C_1}$	$\sqrt{\frac{g_{m2}C_1}{g_{m1}C_2}}$
Configuration B, ($A_0=1$) Figure 6(d)	1	$\frac{g_1}{g_{m1}}$	–	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$	$\frac{g_1}{C_1}$	$\frac{1}{g_1}\sqrt{\frac{g_{m1}g_{m2}C_1}{C_2}}$
Configuration D, ($A_0=1$) Figure 6(e)	1	–	$\frac{g_2}{g_{m2}}$	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$	$\frac{g_2}{C_2}$	$\frac{1}{g_2}\sqrt{\frac{g_{m1}g_{m2}C_2}{C_1}}$

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For Figure 6(b),

$$I_{o2} = \frac{I_{i1} + (s\tau_1 + 1)I_{i2} - A_0 I_{i4}}{D_1(s)}$$
$$I_{o4} = \frac{-A_0 I_{i1} - A_0(s\tau_1 + 1)I_{i2} - s\tau_2 A_0(s\tau_1 + 1)I_{i4}}{D_1(s)} \quad (17)$$

For Figure 6(c),

$$I_{o2} = \frac{-I_{i1} - (s\tau_1 + 1)I_{i2}}{D_1(s)} \quad (18)$$

For Figure 6(d),

$$I_{o1} = \frac{(s\tau_2)I_{i1} - I_{i2}}{D_1(s)}$$
$$I_{o2} = \frac{I_{i1} + (s\tau_1 + A_1)I_{i2}}{D_1(s)} \quad (19)$$

For Figure 6(e),

$$I_{o1} = \frac{(s\tau_2 + A_2)I_{i1} - I_{i2}}{D_2(s)}$$
$$I_{o2} = \frac{I_{i1} + (s\tau_1)I_{i2}}{D_2(s)} \quad (20)$$

Clearly, Equation (16) shows that the realization of LP, BP, HP and BS functions can be obtained from Figure 6(a) by connecting the appropriate terminals. In a similar way, Equations (17)–(20) indicate that the realizations can directly offer LP and BP functions.

From the mathematical expressions in Tables I and II, we can see that the filter characteristics (ω_o, BW and Q) provide electronic tunability through an adjustment of the associated transconductance g_{mi} of the CDTA. From Table I, it can be seen that, for all the proposed configurations in Figure 5, the quality factor Q can be controlled without disturbing the natural angular frequency ω_o. Hence, all the configurations of Table I support an independent electronic control of Q and ω_o. Similarly, it can also be seen in Table II that the proposed configurations of Figures 6(a), (d) and (e) enjoy independent control of the parameters Q and ω_o.

The relative sensitivities of the filter parameters G ($=\omega_o$, BW, Q) to the element of variation $x(=g_i, g_{mi}, C_i)$ may be defined as:

$$S_x^G = \left(\frac{x}{G}\right)\left(\frac{\partial G}{\partial x}\right) \quad (21)$$

Thus, using this definition, the sensitivities for the configurations in Figures 5 and 6 with respect to transconductances g_i, g_{mi}, and capacitors C_1, C_2 are calculated as either 0, or ± 0.5, or ± 1. This implies that the proposed filter configurations have low active and passive sensitivities.

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5. ANALYSIS OF NON-IDEAL EFFECTS

In practice, the performance of the proposed circuits may deviate from the ideal by the non-ideal characteristic of the CDTA being used. For the non-ideal case, the terminal relations of the CDTA describing in Equation (1) can be rewritten by

$$v_p = v_n = 0, \quad i_z = \alpha_p i_p - \alpha_n i_n \quad \text{and} \quad i_x = \beta g_m v_z = \beta g_m Z_z i_z \tag{22}$$

where α_p and α_n denote the parasitic current gains between p-z and n-z terminals, and β represents the transconductance inaccuracy factor between z-x terminals, respectively. These parasitic values slightly differ from their ideal unit values by the effect of the CDTA tracking errors, those absolute values being much less than unity. Therefore, using the above equation, all the proposed configurations of Figures 5 and 6 are reanalyzed and the mathematical expressions for the non-ideal filter parameters are, respectively, illustrated in Tables III and IV, where α_{pi}, α_{ni} and β_i are the parameters α_p, α_n and β of the ith CDTA ($i = 1, 2, 3, 4$).

From Tables III and IV, it can be observed that the tracking errors of the CDTA may cause small deviations of the values of the filter parameters. In addition from Tables III and IV, and according to Equation (21), the sensitivity analysis of the filter characteristics with respect to the CDTA tracking errors can be calculated, and reveals that they are found to be not more than unity in magnitude.

6. EFFECTS OF PARASITIC IMPEDANCES

This section presents a study on the effects of parasitic impedances of the CDTA used in the proposed filters. A non-ideal CDTA model including parasitic resistors and capacitors is shown in Figure 7 [9]. As shown, the real CDTA has parasitic low-value series resistors (R_p and R_n) at the input terminals p and n, and also parasitic resistors and capacitors from the terminals z and x to the ground ($R_z // C_z$ and $R_x // C_x$), respectively. Therefore, taking into account the CDTA parasitics with $\alpha_p = \alpha_n = \beta \cong 1$, the frequency range of operation for the proposed filters can be considered as follows.

First, consider each z terminal of the CDTA in the proposed configurations of Figures 5 and 6, which are terminated with the external grounded impedances. It is to be noted that the frequency responses of the filters strongly depend on the external grounded impedances and the parasitic impedances at the z terminal. Therefore, the filter frequency responses associated with this influence can be summarized as three following cases.

Case (1): Consider the case of a parallel impedance $R_i // C_k$ connected at the terminal z, where $R_i = 1/g_i$ and $k = 1, 2$. In the practical CDTA, the parasitic resistance R_z is normally much greater than the value of R_i ($R_z \gg R_i$), while the parasitic capacitance C_z is very much smaller than the grounded capacitance C_k ($C_z \ll C_k$). Hence, in this case, it can be evaluated that the parasitic impedances of the z terminal are not found to severely affect the filter performance.

Case (2): If a grounded capacitor C_k is connected at the terminal z of the CDTA, there is a low-frequency limitation due to the capacitor C_k and the z terminal parasitic resistance R_z. In this case, the frequency range at low frequencies can be defined as

$$f \geqslant \left(\frac{1}{2\pi R_z C_k}\right) = f_{L1} \tag{23}$$

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Table III. Expressions for the non-ideal filter parameters of Figure 5.

Configurations	ω_o	BW	Q
Configuration A, Figure 5(a)	$\sqrt{\frac{g_{m1}g_{m2}g_{m4}z_{n1}z_{n4}z_{p2}\beta_1\beta_2\beta_4}{g_4C_1C_2}}$	$\frac{g_{m1}g_{m3}z_{n1}z_{n3}\beta_1\beta_3}{g_3C_1}$	$(\frac{g_3}{g_{m3}z_{n3}\beta_3})\sqrt{\frac{g_{m2}g_{m4}C_1z_{n4}z_{p2}\beta_4}{g_{m1}g_4C_2z_{n1}\beta_1}}$
Configuration B, Figure 5(b)	$\sqrt{\frac{g_{m1}g_{m2}g_{m3}z_{n1}z_{n2}z_{n3}\beta_1\beta_2\beta_3}{g_3C_1C_2}}$	$\frac{g_1}{C_1}$	$\frac{1}{g_1}\sqrt{\frac{g_{m1}g_{m2}g_{m3}C_1z_{n1}z_{n2}z_{n3}\beta_1\beta_2\beta_3}{g_3C_2}}$
Configuration C, Figure 5(c)	$\sqrt{\frac{g_{m1}g_{m2}g_{m4}z_{n1}z_{n2}\beta_1\beta_2\beta_4}{g_4C_1C_2}}$	$\frac{g_{m2}g_{m3}z_{n2}z_{n3}\beta_2\beta_3}{g_3C_2}$	$(\frac{g_3}{g_{m3}z_{n3}\beta_3})\sqrt{\frac{g_{m1}g_{m4}C_2z_{n1}\beta_1\beta_4}{g_{m2}g_4C_1z_{n2}\beta_2}}$
Configuration D, Figure 5(d)	$\sqrt{\frac{g_{m1}g_{m2}g_{m3}z_{n1}z_{n2}z_{n3}\beta_1\beta_2\beta_3}{g_3C_1C_2}}$	$\frac{g_2}{C_2}$	$\frac{1}{g_2}\sqrt{\frac{g_{m1}g_{m2}g_{m3}C_2z_{n1}z_{n2}z_{n3}\beta_1\beta_2\beta_3}{g_3C_1}}$

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Table IV. Expressions for the non-ideal filter parameters of Figure 6.

Configurations	ω_o	BW	Q
Configuration A, ($A_0=1$) Figure 6(a)	$\sqrt{\frac{g_{m1}g_{m2}\tau_{n1}\tau_{p2}\beta_1\beta_2}{C_1C_2}}$	$\frac{g_{m1}g_{m3}\tau_{n1}\tau_{n3}\beta_1\beta_3}{g_3C_1}$	$(\frac{g_3}{g_{m3}\tau_{n3}\beta_3})\sqrt{\frac{g_{m2}C_1\tau_{p2}\beta_2}{g_{m1}C_2\tau_{n1}\beta_1}}$
Configuration A, ($A_1=1$) Figure 6(b)	$\sqrt{\frac{g_{m1}g_{m2}g_{m4}\tau_{n1}\tau_{p2}\tau_{p4}\beta_1\beta_2\beta_4}{g_4C_1C_2}}$	$\frac{g_{m1}\tau_{n1}\beta_1}{C_1}$	$\sqrt{\frac{g_{m2}g_{m4}C_1\tau_{p2}\tau_{p4}\beta_2\beta_4}{g_{m1}g_4C_2\tau_{n1}\beta_1}}$
Configuration A, ($A_0=A_1=1$) Figure 6(c)	$\sqrt{\frac{g_{m1}g_{m2}\tau_{n1}\tau_{p2}\beta_1\beta_2}{C_1C_2}}$	$\frac{g_{m1}\tau_{n1}\beta_1}{C_1}$	$\sqrt{\frac{g_{m2}C_1\tau_{p2}\beta_2}{g_{m1}C_2\tau_{n1}\beta_1}}$
Configuration B, ($A_0=1$) Figure 6(d)	$\sqrt{\frac{g_{m1}g_{m2}\tau_{n1}\tau_{n2}\beta_1\beta_2}{C_1C_2}}$	$\frac{g_1}{C_1}$	$\frac{1}{g_1}\sqrt{\frac{g_{m1}g_{m2}C_1\tau_{n1}\tau_{n2}\beta_1\beta_2}{C_2}}$
Configuration D, ($A_0=1$) Figure 6(e)	$\sqrt{\frac{g_{m1}g_{m2}\tau_{n1}\tau_{n2}\beta_1\beta_2}{C_1C_2}}$	$\frac{g_2}{C_2}$	$\frac{1}{g_1}\sqrt{\frac{g_{m1}g_{m2}C_2\tau_{n1}\tau_{n2}\beta_1\beta_2}{C_1}}$

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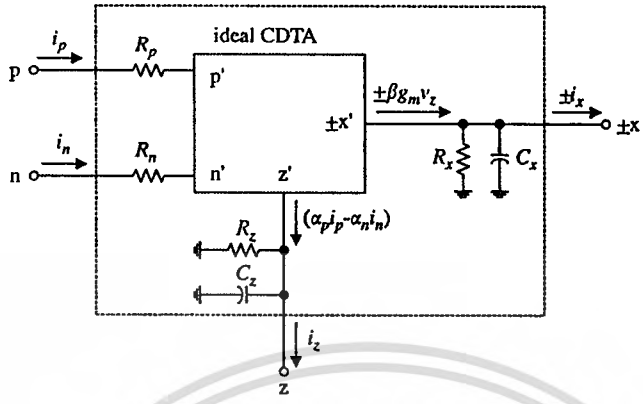

Figure 7. Non-ideal CDTA model.

Case (*3*): If a grounded resistor R_i is connected at the terminal z, the high-frequency range of operation is limited by this resistor and the z terminal parasitic capacitance C_z. Thus, the high-frequency limitation of the filters can be defined as

$$f \leqslant \left(\frac{1}{2\pi R_i C_z}\right) = f_{H1} \tag{24}$$

Second, consider the n and x terminals in Figures 5 and 6, which are connected together. It should be mentioned that there are double x terminals connected to the n terminal, and a single x terminal connected to the n terminal of the CDTA. Here, two cases for determining the frequency responses of the proposed filters can be considered.

Case (*1*): Consider the configurations A and C, where the n terminal is connected with two x terminals. In this case, the parasitic resistance R_n will connect in parallel with the parasitic impedances at two x terminals, i.e. $(R_n // R_x // R_x // 2C_x)$. Since $R_n \ll R_x$, the pole frequency that limits the high-frequency operation of these filters can thus be approximated to

$$f \leqslant \left(\frac{1}{4\pi R_n C_x}\right) = f_{H2} \tag{25}$$

Case (*2*): Consider the configurations B and D, where each n terminal is directly connected with only x terminal. In this case, the maximum frequency attributed to the parasitic resistance R_n and the parasitic impedances at the x terminal $(R_x // C_x)$ can be given by

$$f \leqslant \left(\frac{1}{2\pi R_n C_x}\right) = f_{H3} \tag{26}$$

Finally, to achieve idea responses, the frequency range of operation of the proposed configurations A and C should be restricted to the following conditions [25]:

$$f \leqslant f_{H(A,C)} = 0.1 \times \min\{f_{H1}, f_{H2}\} \tag{27}$$

and

$$f \geqslant f_L = 10 \times \max\{f_{L1}\} \tag{28}$$

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or we can conclude that the overall frequency range of the configurations A and C can be defined as $f_L \leqslant f \leqslant f_{H(A,C)}$.

Similarly, for a proper operation at high frequencies, the operating frequency of the proposed configurations B and D should be selected as

$$f \leqslant f_{H(B,D)} = 0.1 \times \min\{f_{H1}, f_{H3}\} \tag{29}$$

Therefore, the overall frequency range of these configurations can be defined as $f_L \leqslant f \leqslant f_{H(B,D)}$.

7. SIMULATION RESULTS

To confirm the theoretical analysis, the proposed circuits were simulated by PSPICE program. At present, there are several techniques to implement the CDTA active element in IC form [5–10]. Nevertheless, the simulation results reported here were obtained by using the CMOS realization of the CDTA proposed in [10], and shown in Figure 8. This realization, design details of which are also given in [10], was adopted because it provides very low-input impedances at the p and n terminals (i.e. $r_p = r_n \cong 1.92\Omega$), and very high-frequency operation. To perform the CDTA element in simulations, TSMC 0.35 μm n-well CMOS process was performed with dimensions of NMOS and PMOS transistors as that of [10]. The supply voltages are $\pm V = \pm 1.8V$, and the bias current is $I_B = 40\,\mu A$.

As an example, the proposed circuit of Figure 5(a) was designed with the transconductance values of $g_{mi} = g_i = 0.88\,mA/V$ and the capacitance values of $C_1 = C_2 = 10\,pF$. This setting was selected to obtain the LP, BP and HP filters with unity gain at $f_o = \omega_o/2\pi \cong 14\,MHz$ and $Q = 1$. Figure 9 illustrates the simulated magnitude frequency responses, which are the same as expected characteristics. From the simulation results, the power dissipation is approximately 19 mW.

To test the large signal behavior of the proposed filter, the total harmonic distortion (THD) at the output of the BP response for sinusoidal input signal of 14 MHz was obtained. The THD results

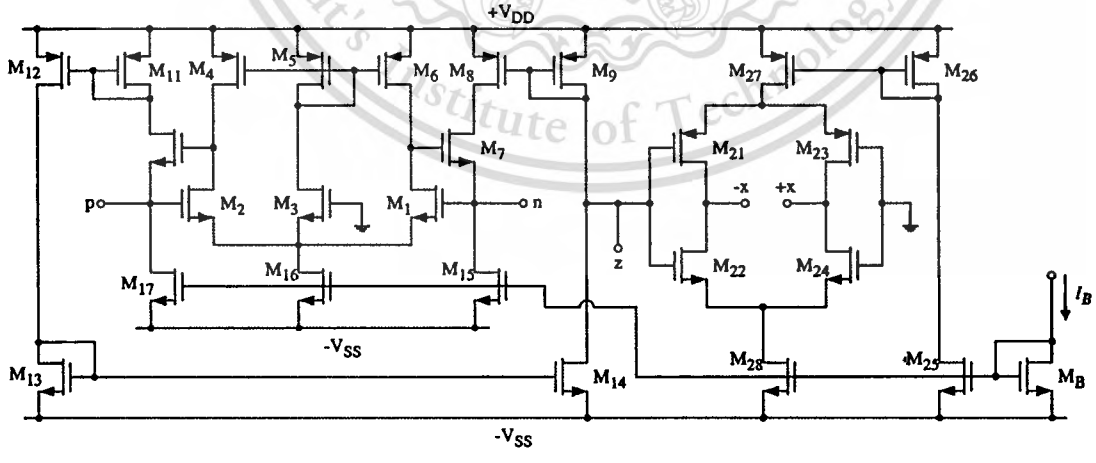

Figure 8. CMOS implementation of the CDTA used in simulations.

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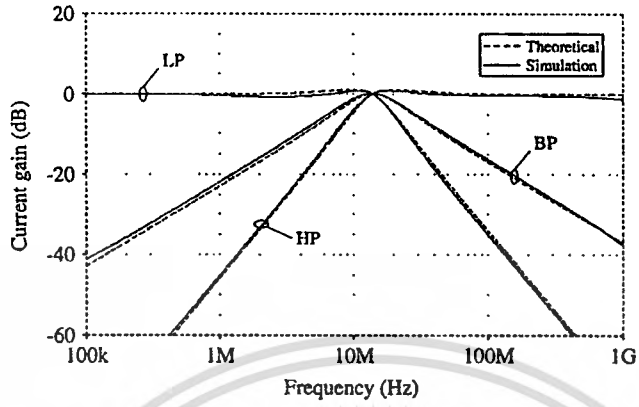

Figure 9. Theoretical and simulation frequency plots for LP, BP and HP characteristics of Figure 5(a).

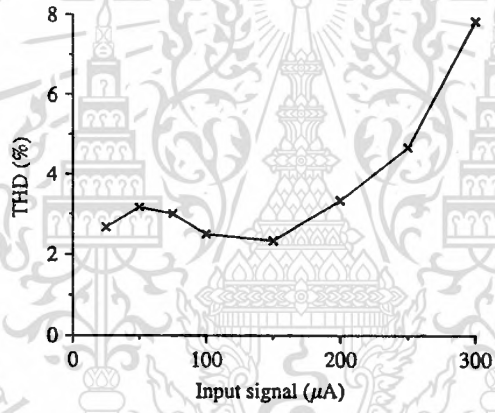

Figure 10. Dependence of % THD on the input signal amplitude of BP filter.

are depicted in Figure 10, which clearly shows that the percentage THD (%THD) is less than 4% for the input signal amplitude lower than 200 μA.

8. CONCLUSIONS

In this paper, an approach for the structural generation of two integrator loop filters using CDTAs and grounded capacitors has been presented. All of the proposed filters have the following advantages: (i) realization of all standard biquadratic filtering functions, (ii) making the filter characteristics electronically tunable in frequency response using external bias current, (iii) the capacitors in the structures are all grounded, which are highly suitable for integrated implementation, (iv) cascading can easily be achieved since they have low-input and high-output impedance characteristics, (v) low sensitivity performance. On the whole, this approach is convenient for monolithic integration, and suitable for cascading and electronic tuning.

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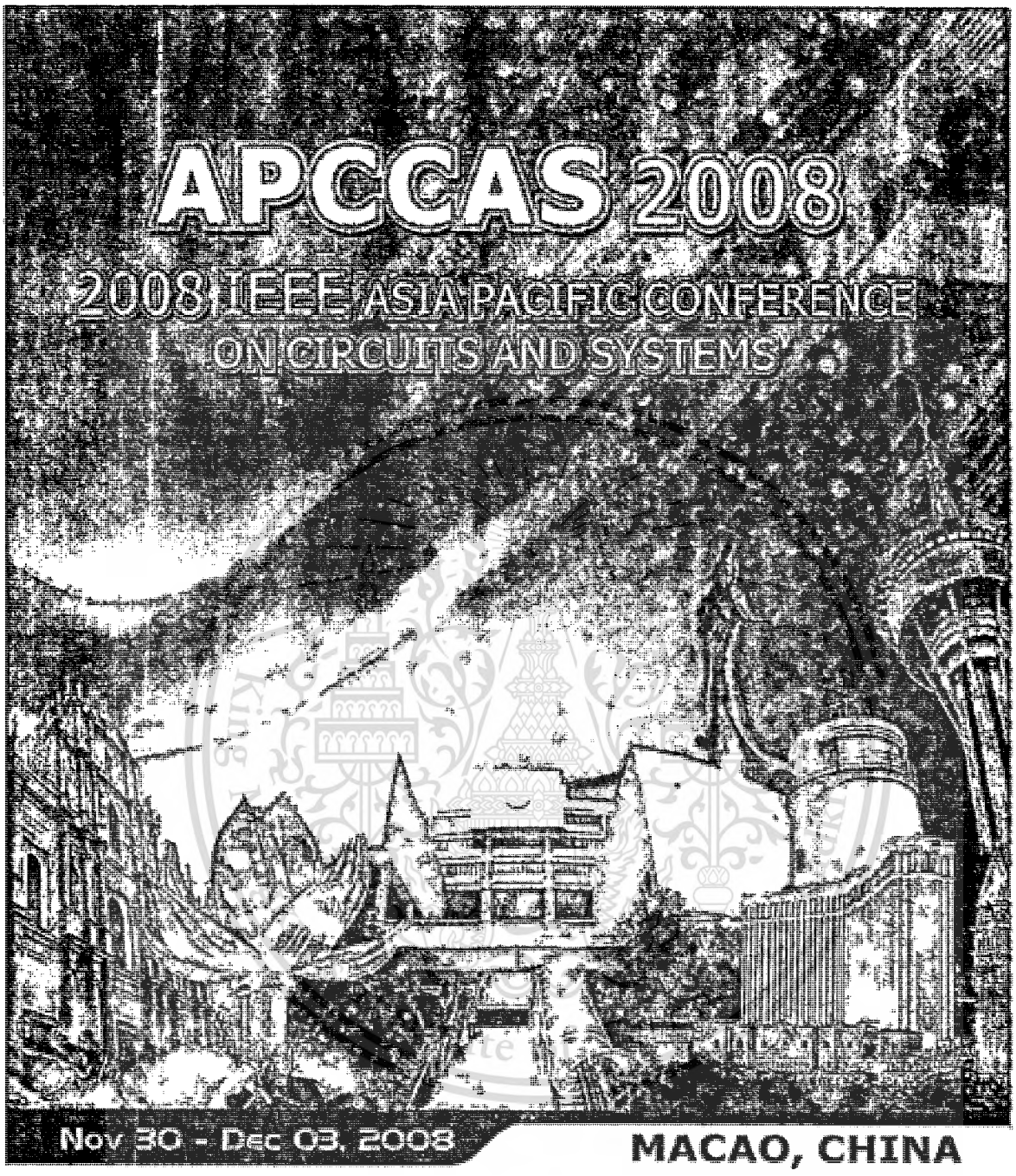

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CDTA-Based Current Limiters and Applications

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***Abstract*—In this paper, a synthesis of analog current limiter (CL) building blocks based on a current differencing transconductance amplifier (CDTA) is proposed. The breakpoint and the slope of the resulting transfer characteristic obtained from the proposed CDTA-based CLs are electronically programmable through the external bias currents. To demonstrate versatility of the proposed electronically tunable CLs, some nonlinear applications to programmable current-mode precision full-wave rectifier and piecewise-linear function approximation generators are also presented. SPICE simulations confirm the effectiveness of the proposed circuits.**

I. INTRODUCTION

Recently, a new current-mode active element, which is called as a current differencing transconductance amplifier (CDTA), was first introduced [1]. This device is synthesized using the current differencing nature of the modified differential current conveyor and a transconductance amplifier to facilitate the implementation of current-mode analog signal processing. As a result, several implementations have emerged, such as active filters, oscillator, and amplifiers using CDTAs as active components [1]-[5]. Nonlinear CDTA applications are also expected, in particular precision rectifiers, current-mode Schmitt triggers, and current-mode multipliers, etc. Unfortunately, there is not much reported in the literature on the use of CDTA's for synthesizing current limiter circuits. In general, the current limiter (CL) is an alternative way to handle nonlinear problems. In the area of analog signal processing applications, it can be widely found as the basic element in the design of nonlinear components and networks, such as nonlinear resistors, chaotic oscillators, precision rectifiers, and piecewise-linear function approximation generators [6]-[9].

Our objective in this paper is to present the applicability of CDTA's as the fundamental active elements for designing the simple CL building blocks. The breakpoints and slopes of the realized transfer curves can be electronically programmed by the external bias currents. Furthermore, based on the proposed CDTA-based CL building blocks, some application examples, i.e. programmable current-mode precision full-wave rectifier and piecewise-linear (PWL) function approximation generators, are also presented to demonstrate their versatility as well as flexibility. Simulation results are included to verify the feasibility of the proposed approach.

II. CURRENT DIFFERENCING BUFFERED AMPLIFIER

The circuit representation of the CDTA is shown in Fig.1. The terminal relation of this device can be characterized by the following set of equations [1]-[5] :

$$v_p = v_n = 0\ ,\ i_z = i_p - i_n \text{ and } i_x = g_m v_z = g_m Z_z i_z \qquad (1)$$

where p and n are input terminals, z and x are output terminals, g_m is the transconductance gain, and Z_z is an external impedance connected at the terminal z. From eq.(1), the current i_z follows the difference of the currents through the terminals p and n (i_p-i_n), and flows from the terminal z into an impedance Z_z. The voltage drop at the terminal z is transferred to a current at the terminal x (i_x) by a transconductance gain (g_m), which is generally controllable by electronic means.

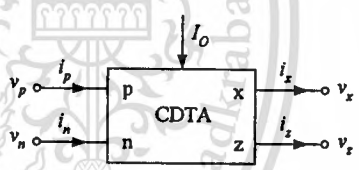

Fig. 1 : Circuit representation of the CDTA.

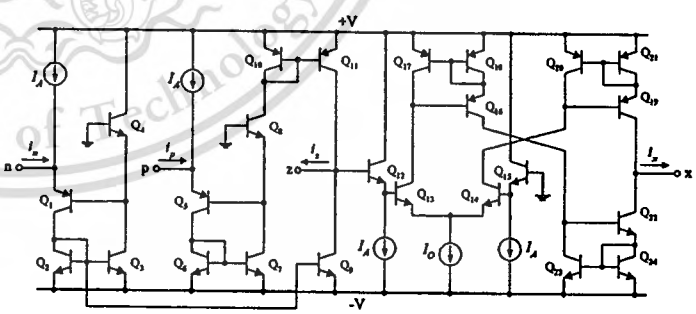

Fig.2 : Possible bipolar realization of the CDTA.

The possible bipolar realization of the CDTA used in this work is shown in Fig.2 [5]. The circuit consists of a current differencing circuit Q_1-Q_{11} and a transconductance amplifier Q_{12}-Q_{24}. Therefore, in this case, the transconductance gain g_m

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of the CDTA is directly proportional to the external bias current I_O, which can be written by

$$g_m = \frac{I_O}{2V_T} \qquad (2)$$

where $V_T \cong 26$ mV at 27°C is the thermal voltage.

III. Proposed CDTA-based Current Limiters

The proposed CDTA-based CLs and their corresponding transfer characteristic curves are shown in Fig.3. The complementary diode combination (D_1 and D_2) is configured to steer the output current i_{out} either into load R_L or bypass it to ground, depending on the polarity of the input current i_{in}. First, consider the proposed circuit depicted in Fig.3(a), where i_{in} is an input current and I_B is the breakpoint current. If $i_{in} \le I_B$, the diode D_1 is turned off and the diode D_2 is turned on. Since no current flows through D_1 ($I_{D1} = 0$), the output current becomes zero ($i_{out} = 0$). For the case of $i_{in} > I_B$, the output current i_{out} will flow through the diode D_1. Therefore, the output current i_{out} of the circuit related to the breakpoint current I_B and the gain g_m can be given as :

$$i_{out} = \begin{cases} 0 & \text{for } i_{in} \le I_B \\ g_m R(i_{in} - I_B) & \text{for } i_{in} > I_B \end{cases} \qquad (3)$$

From above equation, we will simply state that both breakpoint and slope of the transfer characteristic curve can be electronically controlled by changing the values of the current I_B and the gain g_m, which gives an additional flexibility in the nonlinear function approximation design problem. In addition, by the same principle, the remaining proposed circuits shown in Figs.3(b) will give similar transfer characteristics to eq.(3), depending on the terminal connections of the CDTA and the diode. In addition, by reversing the connection of both complementary diodes, the inverting output current characteristics can easily be obtained.

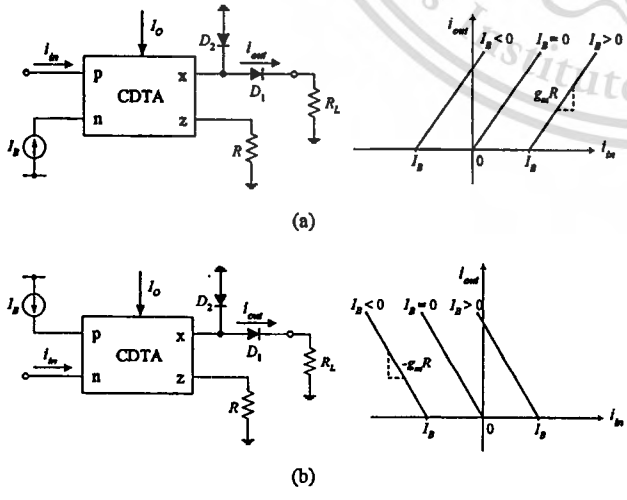
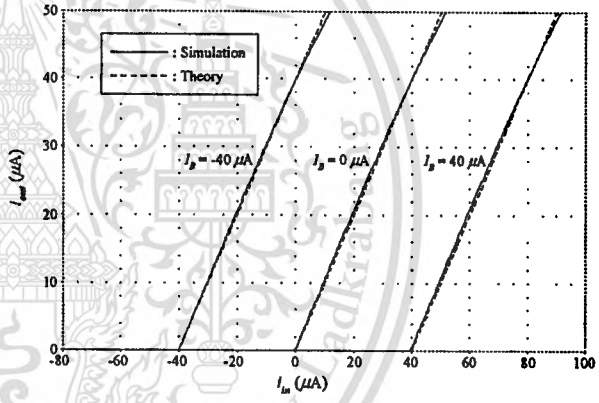


Fig.3 : Proposed CDTA-based CL building blocks.

IV. Simulation Results

To verify the theoretical study, the proposed CDTA-based CL circuits were constructed and simulated using PSPICE simulations. For this purpose, the CDTA given in Fig.2 is performed with the model parameters of the bipolar transistors PR100N (PNP) and NP100N (NPN) from AT&T. The DC bias conditions are chosen as : ±V = 3 V and I_A = 100 μA. For the diode implementation, it can be done by using the NPN transistor with its base and collector connected together.

Fig.4 shows the current transfer characteristics comparison between simulation and theoretical results for the proposed CL block of Fig.3(a). Fig.4(a) shows the plots of i_{out} against i_{in} for three different values of I_B, i.e. I_B = -40, 0 and 40 μA, with g_m = 2 mS (I_O = 100 μA) and R = 500 Ω, while Fig.4(b) shows the plots for three different values of g_m, i.e. g_m = 2, 4 and 6 mS (I_O = 100, 200 and 300 μA), and I_B = 20 μA. From the simulations, the maximum error in i_{out} was found to be less than 8%. Owing to similar transfer curves and performances between the circuit discussed above and the remaining circuits in Fig.3(b), the plots for those circuits will not be reported here.



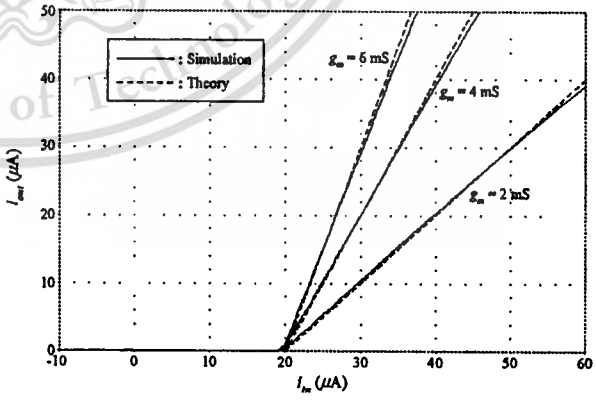


Fig.4 : Current transfer characteristics of the proposed CL of Fig.3(a)
(a) for three different values of I_B (b) for three different values of g_m

V. Application Examples

A. Programmable Current-Mode Full-Wave Rectifier

Based on the use of the proposed CDTA-based CLs of Fig.3, an application for realizing programmable current-mode full-wave rectifier can be illustrated in Fig.5. The multiple-output current follower (MO-CF) stage is the circuit that generates, from the input current (i_{in}), multiple output currents in the same direction. It can be realized by using a low-input resistance input stage with multi-output terminals as shown in Fig.6 [10]. By setting $g_{m1} = g_{m2} = g_m$, the relations between the input and the output currents can be expressed as :

$$i_{out} = |g_m R(i_{in} - I_B)| \qquad (4).$$

Note that the slopes of the transfer curves can still be controlled electronically by tuning the transconductance gain of the CDTA1 for the negative slope and by tuning the transconductance gain of the CDTA2 for the positive slope.

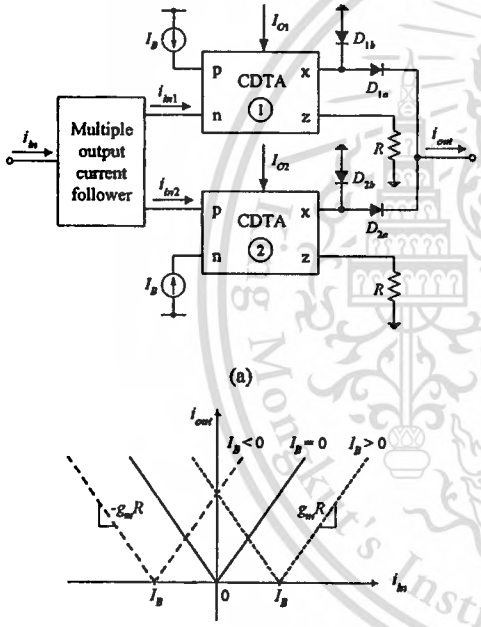


Fig.5 : Programmable current-mode full-wave rectifier.

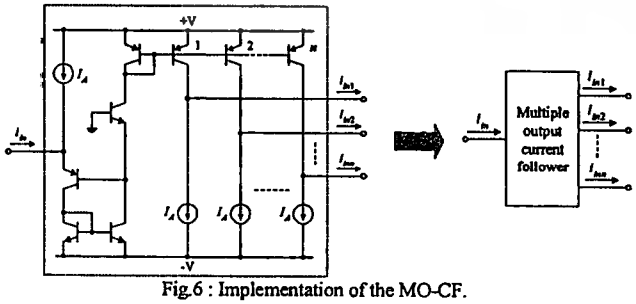


Fig.6 : Implementation of the MO-CF.

Fig.7 shows the rectified waveforms obtained from the circuit of Fig.5 for $R = 500\ \Omega$, $I_B = 0\ \mu A$, and g_m varied from 1 mS to 3 mS. In this case, a sinusoidal input with $i_{in} = 50\ \mu A$ peak and $f = 1$ MHz was applied to the circuit. It appears from the results that the imperfections in the output waveforms contributing to the non-ideal properties of the CDTA and diode can be observed. However, some amplitude errors caused mainly by possible current transfer errors as well as the offset currents of the MO-CF and CDTA can be compensated by properly adjusting the g_m-value.

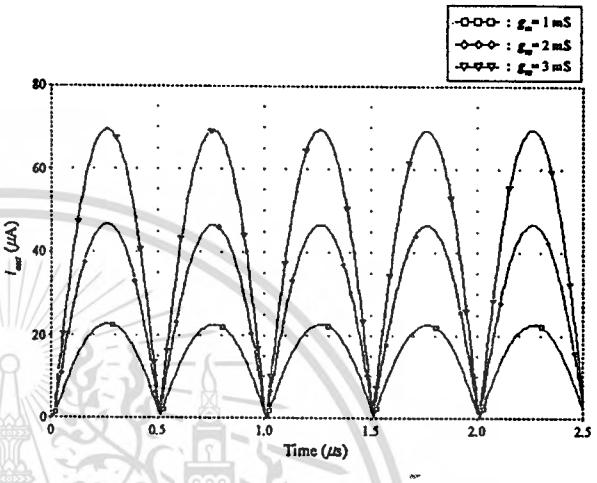


Fig.7 : Transient responses of Fig.5 for various values of g_m.

B. Piecewise-Linear Function Approximation Synthesis

To further demonstrate the approximation of an arbitrary nonlinear function, another useful application of the proposed CLs for realizing the PWL function circuit is discussed. As an example, the desired transfer characteristic consisting of three linear segments is shown in the upper part of Fig.8(a). The required individual slopes due to each CDTA-based CL of Fig.3 are indicated in the lower part of Fig.8(a), and the actual circuit implementation can be shown in Fig.8(b). In this case, the corresponding slopes can be expressed as :

$$S_0 = g_{m1}R_1 \ , \ i_{out} = S_0(i_{in} - I_{B1}) \ , \text{for} \ I_{B1} > i_{in}$$

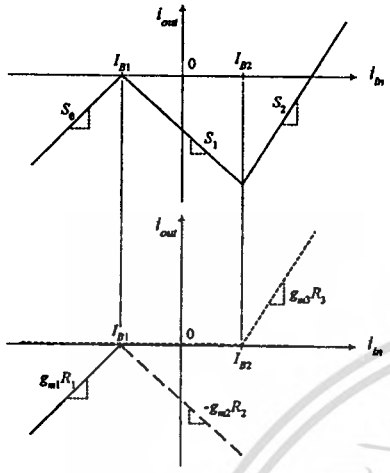
$$S_1 = -g_{m2}R_2 \ , \ i_{out} = S_1(i_{in} - I_{B1}) \ , \text{for} \ I_{B2} > i_{in} \geq I_{B1}$$

and

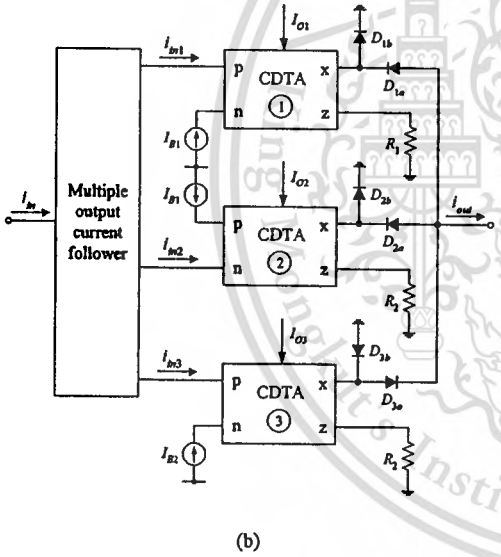
$$S_2 = (g_{m3}R_3 - g_{m2}R_2), \ i_{out} = S_2(i_{in} - I_{B2}) + S_1(I_{B2} - I_{B1}) \ , \text{for} \ i_{in} \geq I_{B2} \qquad (5).$$

It should be noted that the slopes S_0, S_1 and S_2 of the composed resulting transfer characteristics can be easily determined by adjusting the values of $g_{m1}R_1$, $g_{m2}R_2$ and $g_{m3}R_3$, respectively. From the above discussions, it is further apparent that a class of arbitrary nonlinear current generators with variable positive and negative slopes and breakpoints can be synthesized. Fig.9 illustrates the simulated current transfer characteristic curve of Fig.8(b), when the bias current values of I_{B1} = -20 μA, I_{B2} = 20 μA, I_{O1} = 50 μA, I_{O2} = 100 μA, and I_{O3} = 300 μA and the resistance values of $R_1 = R_2 = R_3 = 500\ \Omega$ are chosen. From Fig.9, the simulation results agree fairly

well with the theoretical results. At this point, it is also verified that the realization of the nonlinear current function of Fig.8(a) can be accurately carried out by employing the proposed CDTA-based CLs.



(a)



(b)

Fig.8 : PWL function approximation

(a) desired transfer characteristic curve (b) circuit implementation

VI. Conclusion

In this paper, a simple approach for the syntheses of the current limiters using the CDTA as an active element is proposed. The proposed CDTA-based CLs were then used as fundamental circuit building blocks to implement integrable nonlinear function circuits, such as current-mode precision full-wave rectifier, and piecewise-linear function approximation circuits. All the resulting synthetic building blocks will also posses desirable properties, namely, the slopes of the linear segments and breakpoints can be electronically adjusted through the external DC bias currents of the CDTA. The proposed building blocks and their applications have been confirmed using PSPICE simulation.

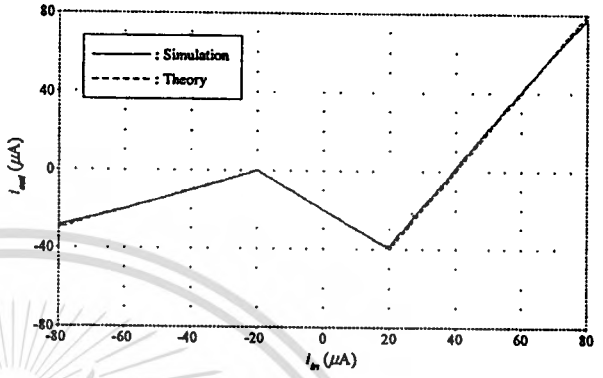


Fig.9 : Simulated current transfer characteristic of the PWL function approximation synthesizer of Fig.8.

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CURRENT-MODE TWO INTEGRATOR LOOP CDTA FILTERS

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ABSTRACT

A versatile family of current-mode two integrator loop filter structures using current differencing transconductance amplifiers (CDTAs) and grounded capacitors is generated. The basic filter building blocks consist of current proportional blocks, current lossless integrators and a current lossy integrator based on the use of CDTAs as the major active components. It is demonstrated that the derived filter structures can realize a general class of second-order current transfer functions. Since the resulting structures contain only CDTAs and grounded capacitors, they are general and very appropriate for integration, cascading and electronic tuning.

Index Terms—Current Differencing Transconductance Amplifier (CDTA), two integrator loop, current-mode circuit

1. INTRODUCTION

Two integrator loop structures are very popular and useful block to realize biquad filters [1]-[4]. Nawrocki and Klein proposed a two-integrator loop universal biquad with single-input and single-output using eight operational transconductance amplifiers (OTAs) and two grounded capacitors [1]. In 1988, Sanchez-Sinencio et. al. have systematically summarized and extended the work on the two-integrator loop OTA-C filters based on the block diagram method [2]. In [3], the author developed the Nawrocki and Klein biquad to derive many new filter structures. However, all the above methods are based on the voltage-mode approach. Moreover, some obtained filter structures in [2] need the capacitor injection of excitation signals in the circuit design, which are not suitable for cascade implementation, and the resulting floating capacitors are not suitable for integrated circuit (IC) implementation. In 1996, a comprehensive set of current-mode continuous-time two integrator loop filter structures incorporating dual-output OTA (DO-OTA) and capacitors was developed in [4]. However, the structures also require capacitor injection of excitation signals. They do not exhibit the feature of low-impedance inputs. For cascadability to implement higher-order current-mode filters, it is preferred that the structure should exhibit low-input and high-output impedances.

This paper largely focuses on presenting a structural generation to synthesis the current-mode two integrator loop filters with current differencing transconductance amplifiers (CDTAs) [5]-[6]. The proposed configurations employ the current proportional blocks and current integrators based on CDTAs as the basic building units. By suitably selecting the input and output currents, the derived filters can realize all the standard biquadratic filters from the same configuration. The resulting filter characteristics can electronically adjust with separate tunable transconductances. All the filter structures contain only grounded capacitors, which can absorb parasitic capacitances and require the small chip areas. In addition, all the proposed filters exhibit both low-input and high-output impedance levels, thus permitting easy cascadability.

2. CURRENT DIFFERENCING TRANSCONDUCTANCE AMPLIFIER (CDTA)

Using the standard notation for the CDTA whose electrical symbol is shown in Fig.1, it can be characterized by the following constitutive equations [5]-[6] :

$$v_p = v_n = 0 \ , \ i_z = i_p - i_n \ \text{ and } \ i_x = g_m v_z = g_m Z_z i_z \qquad (1)$$

where p and n are input terminals, z and ±x are output terminals, g_m is the transconductance gain, and Z_z is an external impedance connected at the terminal z.

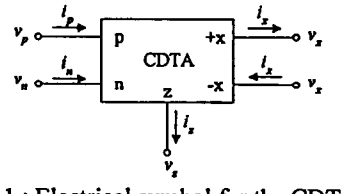


Fig.1 : Electrical symbol for the CDTA.

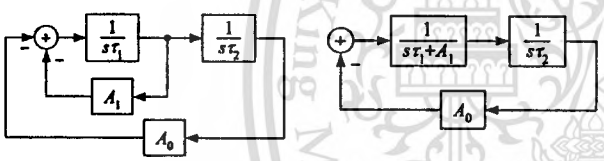
3. CURRENT-MODE TWO INTEGRATOR LOOP CDTA FILTERS

Fig.2 shows two different block diagram representations of the basic two-integrator loop operation that will be used to illustrate the proposed approach. Observe that Fig.2(a) contains two negative-feedback loops including two lossless integrators ($1/s\tau_1$ and $1/s\tau_2$) and two proportional gain blocks (A_0 and A_1), while Fig.2(b) contain a single negative-feedback loop consisting of one lossy integrator, one lossless integrator and one proportional gain block. In considering two-integrator loop configurations of Figs.2(a) and 2(b), the characteristic equation is identical and can be given by :

$$D_1(s) = s^2\tau_1\tau_2 + s\tau_2 A_1 + A_0 \qquad (2)$$

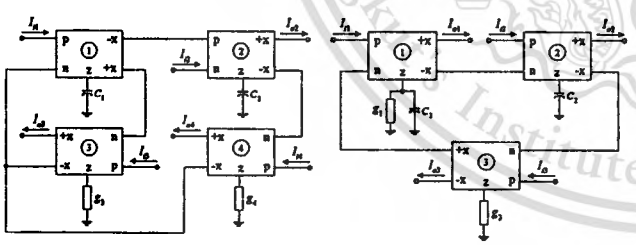
Hence, the natural angular frequency (ω_o), bandwidth (BW) and quality factor (Q) for both configurations, respectively, become :

$$\omega_o = \sqrt{\frac{A_0}{\tau_1\tau_2}}\ ,\quad BW = \frac{A_1}{\tau_1} \quad \text{and} \quad Q = \frac{1}{A_1}\sqrt{\frac{A_0\tau_1}{\tau_2}} \qquad (3)$$



(a) (b)

Fig.2: Two integrator loop structures.
(a) configuration A (b) configuration B



(a) (b)

Fig.3: CDTA-based current-mode biquad filters based on two integrator loop structures of Fig.2..
(a) configuration A (b) configuration B

The corresponding CDTA-based circuits derived from block diagram structures of Figs.2(a) and 2(b) can be shown in Figs.3(a) and 3(b), respectively. The mathematical expressions for the corresponding parameters ω_o, BW and Q, for both derived realizations are summarized in Table 1. All the possible current transfer functions derived from Figs.3(a) and 3(b) are formulated by the following expressions.

For Fig.3(a),

$$\left.\begin{aligned} I_{o2} &= \frac{-I_{i1} + (s\tau_1 + A_1)I_{i2} - A_1 I_{i3} - A_0 I_{i4}}{D_1(s)} \\ I_{o3} &= \frac{-(s\tau_2 A_1)I_{i1} + (A_0 A_1)I_{i2} + A_1(s^2\tau_1\tau_2 + A_0)I_{i3} - (s\tau_2 A_0 A_1)I_{i4}}{D_1(s)} \\ I_{o4} &= \frac{-A_0 I_{i1} - A_0(s\tau_1 + A_1)I_{i2} - (A_0 A_1)I_{i3} - s\tau_2 A_0(s\tau_1 + A_1)I_{i4}}{D_1(s)} \\ I_{o3} + I_{o4} &= \frac{-(s\tau_2 A_1 + A_0)I_{i1} - (s\tau_1 A_0)I_{i2} + (s^2\tau_1\tau_2 A_1)I_{i3} + (s^2\tau_1\tau_2 A_0)I_{i4}}{D_1(s)} \end{aligned}\right\} \qquad (4)$$

For Fig.3(b),

$$\left.\begin{aligned} I_{o1} &= \frac{(s\tau_2)I_{i1} - A_0 I_{i2} - (s\tau_2 A_0)I_{i3}}{D_1(s)} \\ I_{o2} &= \frac{I_{i1} + (s\tau_1 + A_1)I_{i2} - A_0 I_{i3}}{D_1(s)} \\ I_{o3} &= \frac{A_0 I_{i1} + A_0(s\tau_1 + A_1)I_{i2} + s\tau_2 A_0(s\tau_1 + A_1)I_{i3}}{D_1(s)} \end{aligned}\right\} \qquad (5)$$

As inspection of equations (4)-(5) reveals that, by suitably connecting the input current terminals, all the variety of standard biquadratic filtering functions can be obtained. From equation (4), it can readily be seen that the proposed filter configuration of Fig.3(a) can provide lowpass (LP), highlass (HP), bandpass (BP), bandstop (BS), and allpass (AP) current responses with different inputs and outputs. It is further noted from equation (4) that the output current $I_{o3} + I_{o4}$ can easily be obtained by connecting two corresponding terminals together. Equations (5) also shows that the configurations in Fig.2(b) realizes LP and BP characteristics. It may be stated here that all of the above multifunction biquadratic filters can be realized without any constraints on the component values, and all the proposed configurations exhibit both low-input and high-output impedance characteristics, which will be more convenient in terms of cascading and connecting to other networks. Moreover, the use of only grounded capacitors is helpful for easing the IC implementation.

From Table 1, we can see that the filter characteristics (ω_o, BW and Q) provide electronic tunability through an adjustment of the associated transconductance g_{mi} of the CDTA. It can also be seen that, for all the proposed filters in Fig.3, the quality factor Q can be controlled without disturbing the natural angular frequency ω_o. Hence, all the configurations of Table 1 support an independent electronic-control of Q and ω_o.

Table 1 : Expressions for the filter parameters of Fig.3.

Configurations	A_0	A_1	τ_1	τ_2	ω_o	BW	Q
Configuration A, Fig.3(a)	$\frac{g_{m4}}{g_4}$	$\frac{g_{m3}}{g_3}$	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}g_{m4}}{g_4C_1C_2}}$	$\frac{g_{m1}g_{m3}}{g_3C_1}$	$\frac{g_3}{g_{m3}}\sqrt{\frac{g_{m2}g_{m4}C_1}{g_{m1}g_4C_2}}$
Configuration B, Fig.3(b)	$\frac{g_{m3}}{g_3}$	$\frac{g_1}{g_{m1}}$	$\frac{C_1}{g_{m1}}$	$\frac{C_2}{g_{m2}}$	$\sqrt{\frac{g_{m1}g_{m2}g_{m3}}{g_3C_1C_2}}$	$\frac{g_1}{C_1}$	$\frac{1}{g_1}\sqrt{\frac{g_{m1}g_{m2}g_{m3}C_1}{g_3C_2}}$

Table 2 : Expressions for the non-ideal filter parameters of Fig.3.

Configurations	ω_o	BW	Q
Configuration A, Fig.3(a)	$\sqrt{\frac{g_{m1}g_{m2}g_{m4}\alpha_{n1}\alpha_{n4}\alpha_{p2}\beta_1\beta_2\beta_4}{g_4C_1C_2}}$	$\frac{g_{m1}g_{m3}\alpha_{n1}\alpha_{n3}\beta_1\beta_3}{g_3C_1}$	$\left(\frac{g_3}{g_{m3}\alpha_{n3}\beta_3}\right)\sqrt{\frac{g_{m2}g_{m4}C_1\alpha_{n4}\alpha_{p2}\beta_2\beta_4}{g_{m1}g_4C_2\alpha_{n1}\beta_1}}$
Configuration B, Fig.3(b)	$\sqrt{\frac{g_{m1}g_{m2}g_{m3}\alpha_{n1}\alpha_{n2}\alpha_{n3}\beta_1\beta_2\beta_3}{g_3C_1C_2}}$	$\frac{g_1}{C_1}$	$\frac{1}{g_1}\sqrt{\frac{g_{m1}g_{m2}g_{m3}C_1\alpha_{n1}\alpha_{n2}\alpha_{n3}\beta_1\beta_2\beta_3}{g_3C_2}}$

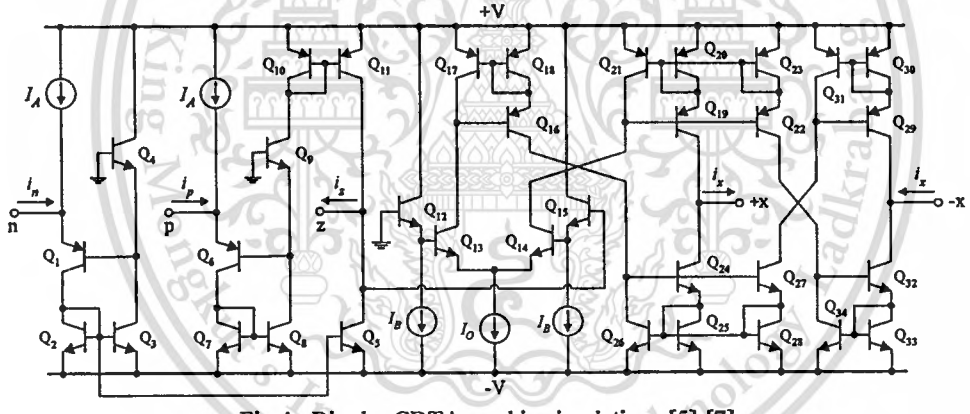


Fig.4 : Bipolar CDTA used in simulations [5]-[7].

The relative sensitivities of the filter parameters G (= ω_o, BW, Q) to the element of variation x (= g_1, g_{m1}, C_1) may be defined as :

$$S_x^G = \left(\frac{x}{G}\right)\left(\frac{\partial G}{\partial x}\right) . \qquad (6)$$

Using this definition, the sensitivities for the structures in Fig.3 with respect to transconductances g_1, g_{m1}, and capacitors C_1, C_2 are calculated as either 0, or ±0.5, or ±1. This implies that the proposed filter configurations have low active and passive sensitivities.

4. NON_IDEAL ANALYSIS

In practice, the performance of the proposed circuits may be deviated from the ideal by the non-ideal characteristic of the CDTA being used. For the non-ideal case, the terminal relations of the CDTA describing in equation (1) can be rewritten by [7] :

$$v_p = v_n = 0 \ , \ i_z = \alpha_p i_p - \alpha_n i_n \text{ and } i_x = \beta g_m v_z = \beta g_m Z_z i_z \quad (7)$$

where α_p and α_n denote the parasitic current gains between p-z and n-z terminals, and β represents the transconductance inaccuracy factor between z-x terminals, respectively. These parasitic values slightly differ from their ideal unit values by the effect of the CDTA tracking errors, those

absolute values being much less than unity. Therefore, using the above equation, all the proposed configurations of Fig.3 are reanalyzed and the mathematical expressions for the non-ideal filter parameters are respectively illustrated in Table 2, where α_{pi}, α_{ni} and β_i are the parameters α_p, α_n and β of the i-th CDTA (i = 1, 2, 3, 4).

From Table 2, it can be observed that the tracking errors of the CDTA may cause small deviations of the values of the filter parameters. However, these deviations should not be seen as a drawback, as we can compensate these effects as low as possible by appropriately tuning transconductance values. Also from Table 2, and according to equation (6), the sensitivity analysis of the filter characteristics with respect to the CDTA tracking errors can be calculated, and reveals that they are found to be not more than unity in magnitude.

5. SIMULATION RESULTS

To confirm the theoretical analysis, the proposed circuits were simulated by PSPICE program. The simulation results reported here were obtained by using the bipolar realization of the CDTA proposed in [5]-[7], and shown in Fig.4. This realization was adopted because it provides very low-input impedances at the p and n terminals, and its g_m-value can controllable linearly by I_O (i.e., $g_m = I_O/2V_T$, where $V_T \cong 26$ mV at 27°C is the thermal voltage). To perform the CDTA in simulations, it was achieved using transistor model parameters of PR100N (PNP) and NP100N (NPN) of the bipolar arrays ALA400 from AT&T [8], with ±V = ±3V, I_A = 100 μA, and I_B = 50 μA.

As an example, the proposed circuit of Fig.3(a) was designed with the transconductance values of $g_{mi} = g_i = 1$ mS and the capacitance values of $C_1 = C_2 = 1$ nF. This setting was selected to obtain the LP, BP, and HP filters with unity gain at $f_o = \omega_o/2\pi \cong 159$ kHz and $Q = 1$. Fig.5 illustrates the simulated magnitude frequency responses, which are the same as expected characteristics.

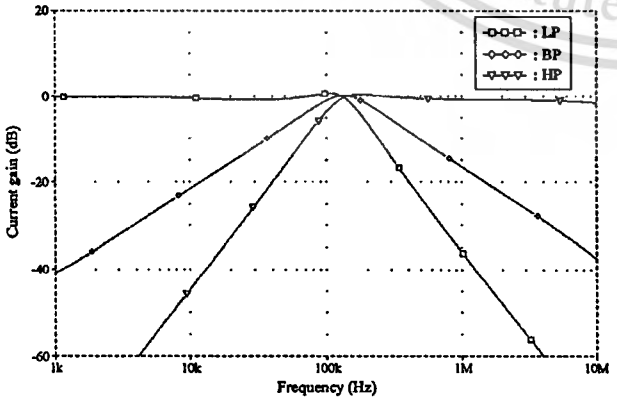


Fig.5: Simulated frequency plots for LP, BP and HP current characteristics of Fig.3(a).

6. CONCLUSION

An approach for the structural generation of current-mode two integrator loop filters using CDTAs and grounded capacitors has been presented. All of the proposed filters have the following advantages : (i) realization of all standard biquadratic filtering functions without component matching conditions; (ii) making the filter characteristics electronically tunable in frequency response using external bias current; (iii) the capacitors in the structures are all grounded, which are highly suitable for integrated implementation and require smaller chip areas than floating ones; (iv) cascading can easily be achieved since they have low-input and high-output impedance characteristics; (v) low sensitivity performance. On the whole, this approach is convenient for monolithic integration, and suitable for cascading and electronic tuning.

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