ELECTRONICALLY TUNABLE ANALOG FILTERS FOR BASEBAND APPLICATIONS

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หัวข้อวิทยานิพนธ์	การออกแบบวงจรกรองสัญญาณที่ปรับค่าได้ด้วยวิธีทางอิเล็กทรอนิกส์สำหรับการประยุกต์ใช้งานช่วงความถี่ฐาน
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บทคัดย่อ

วิทยานิพนธ์นี้นำเสนอการออกแบบวงจรกรองสัญญาณไฟฟ้าในช่วงความถี่ฐาน ซึ่งเป็นวงจรส่วนสำคัญในระบบสื่อสารยุคปัจจุบัน โดยช่วงความถี่ปฏิบัติการนั้นได้ออกแบบให้สามารถปรับค่าได้เพื่อชดเชยผลความผิดพลาดอันเนื่องมาจากกระบวนการผลิตและสภาพแวดล้อม สำหรับผลการศึกษาสามารถแบ่งออกได้เป็นสองส่วนหลักด้วยกัน ส่วนแรกคือเทคนิคการออกแบบวงจรกรองสัญญาณไฟฟ้าที่ทำงานในโหมดกระแส โดยได้เสนอเทคนิคการแบ่งส่วนย่อยวงจรโครงข่ายของวงจรกรองสัญญาณพาสซีฟแอลซีแบบขั้นบันได จากนั้นจึงทำการจำลองความสัมพันธ์ของแรงดันและกระแสภายในส่วนย่อยเหล่านั้นด้วยวงจรสายพานกระแสควบคุมยุคที่สองแบบหลายขั้วสัญญาณออก แล้วจึงนำส่วนย่อยที่แปลงเป็นวงจรแอกทีฟแล้วนั้นกลับมาต่อรวมกันอีกครั้งหนึ่ง วิธีนี้สามารถช่วยลดความยุ่งยากในการออกแบบวงจรกรองขนาดใหญ่ได้เป็นอย่างดี ในขณะที่ยังคงรักษาคุณลักษณะที่ดีของวงจรกรองพาสซีฟแอลซีไว้ได้ นอกจากนี้ ค่าอิมพีแดนซ์ภายในตัววงจรสายพานกระแสยังถูกนำมาประยุกต์ใช้เพื่อทดแทนตัวต้านทานภายนอก ทำให้สามารถลดจำนวนอุปกรณ์ต่อร่วมลง อีกทั้งยังช่วยให้ค่าความถี่คุณลักษณะของวงจรกรองสัญญาณเปลี่ยนแปลงได้ตามค่ากระแสไบอัสอีกด้วย วงจรกรองสัญญาณแบบต่างๆ อันได้แก่ วงจรกรองความถี่ต่ำผ่านแบบบัตเตอร์เวิร์ธอันดับที่สาม วงจรกรองความถี่ต่ำผ่านแบบแอลลิฟติกอันดับที่สาม และวงจรกรองแถบความถี่ผ่านแบบเชบีเชฟอันดับที่หก ได้ถูกเลือกมาแสดงเป็นตัวอย่างในการประยุกต์ใช้เทคนิคที่นำเสนอนี้ เพื่อออกแบบวงจรกรองสัญญาณได้อย่างมีประสิทธิภาพ โดยผลลัพธ์ได้แสดงอยู่ในรูปผลการจำลองการทำงานด้วยโปรแกรมสไปซ์

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ABSTRACT

This thesis presents the design and implementation of tunable analog baseband filters, which are crucial parts of modern communication and computer systems. The cut-off frequency of the filters must be tunable in order to overcome the component variations due to the integration process and environment. The consequences can be divided into two different filter design techniques. A current-mode filter design methodology using component partitioning technique is first discussed, in which the prototype passive LC filter is firstly divided into subsections, and then a signal-flow graph (SFG) of each subsection is individually simulated one by one using multi-output second generation current controlled conveyors (MCCCIIs). This leads to a simple and easy to design active filter implementation including the realization of finite transmission zero since the complexity of a large SFG diagram is avoided, while the low sensitivity properties are still promised. Moreover, a tunable internal impedance of the MCCCII is utilized to make the cut-off frequency of the filters electronically adjustable by the bias current. Some design examples, i.e., a 5 MHz third-order Butterworth low-pass, a 1 MHz third-order elliptic low-pass, and a 1 MHz sixth-order Chebyshev band-pass filters are employed to demonstrate the proposed realization scheme. These simulated filters retain minimum requirement of passive and active elements and provide the filter corner frequency tunability. Moreover, the method also allows an implementation of the elliptic filters by simply adding floating capacitors to its corresponding all-pole filter structures.

The other technique aims for implementing low-distortion voltage-mode active-RC filters under a low-voltage constraint. A switch is placed in series with a resistor to modify the effective resistance, hence the RC time-constant is tunable via the duty cycle of controlling clock. With this timing control, there is no requirement of excessive voltage, thus the gate oxide reliability problems are

avoided. The characteristics of the switched-resistor networks that employ both one set and two sets of such switch and resistor combination are thoroughly analyzed including their slew rate induced distortion, frequency translation and noise performance. In order to extend the tuning range, a switched-resistor bank scheme is also presented. Experimental results of 100 kHz prototype first-order switched-resistor filters implemented from discrete elements confirm the feasibility of this technique. Simulation results of 10 MHz fifth-order switched-resistor elliptic low-pass filters in standard 0.18-μm CMOS process operating at 1.5-V supply exhibit the low-voltage operation capability.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Although information processing is migrating continuously to digital domain, analog circuits and filters have still been found in wide range of applications as an integral part of external interfaces used in most telecommunication and signal processing systems [1, 2]. In wireless systems, for example, they need some analog filters to separate the desired channel from undesired ones and from interference, whereas the analog filters can also be used to perform equalization which corrects the phase distortion smearing the digital pulses in high-speed digital links. Moreover, a similar job inside computer magnetic disk drives also requires such analog filtering circuits, and so on. Indeed, since we live in an analog physical world, analog circuits are a necessary part in the interface system of all digital processors, whether this interface is an antenna, a magnetic head, or a transmission line [1, 3–5].

The analog parts tend to dominate over the digital parts in terms of both design effort and design risk, and they are often the performance bottleneck of the integrated system. As the sizes of integrated devices decrease, the maximum voltage ratings also rapidly shrink. Although decreased supply voltages do not restrict the design of digital circuits, it brings trouble to design high performance analog integrated circuits using these new processes. Moreover, increasing the signal-to-noise ratio (SNR) in digital signal processing techniques can easily be done by simply expanding the data word length, but it is not the case for analog circuit techniques [5, 6]. However, there exists a large number of important functions that yield superior performance and lower cost when implemented with analog circuit techniques. It is also true that there are many cases, in which digital techniques are not applicable at all [2, 4, 5].

Fig. 1.1 shows a simple work flow of a typical wireless communication receiver. An RF band-select filter passes the appropriate band and applies it to the front-end, which includes a low-noise amplifier, mixer(s), and in some cases additional filters. The input to the analog-to-digital (A/D) converter (ADC) can be a baseband signal or an intermediate frequency signal. In either case, an analog filtering operation precedes the A/D conversion. This essential analog function is

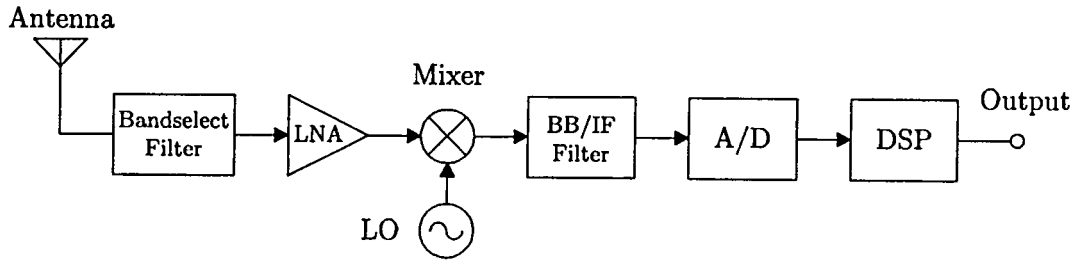


Figure 1.1 A receiver block diagram.

necessary to reject undesirable components, which may be orders of magnitude larger than the desired signal. Accomplishing the same job without analog filters would require ADCs and digital signal processors (DSPs) with a much larger number of bits to properly digitize and process large interfering signals, while keeping the quantization noise well below the desired signal. In most practical cases, power dissipation constraints, and difficulty of implementation prohibit the use of such ADCs and DSPs. Analog filters are needed, in both transmitters and receivers, following mixing operations, in order to reduce undesirable frequency components. This is a good example to show that analog filters are so far the best choice for an application, in which high speed operation, moderate accuracy, medium dynamic range and low-power dissipation are the answer [4, 5].

Since the introduction of integrated circuits, the operational amplifier (op-amp) has served as the fundamental building block in analog circuit design. In the meantime, several new integrated analog building blocks have emerged as a candidate in modern analog circuit applications, where the voltage-mode opamp circuits cannot reach the specification due to its limited bandwidth at high closed-loop gains. Furthermore, the limited slew-rate of the operational amplifier affects the large-signal, high-frequency operation.

When wide bandwidth, low power consumption, and low-voltage operation are needed simultaneously, the voltage-mode operational amplifier easily becomes too complex, whereas some extra performances are sometimes unnecessary, for example, DC accuracy. One procedure for finding the alternatives, preferably simpler circuit realizations, is to use current signals rather than voltage signals for signal processing [7, 8]. Designing circuit in current domain owns several advantages. First, because current-mode circuits have lower parasitics at internal nodes, they normally face less problems of speed limitation and power consumption. More important, when the signal is conveyed as a current, the voltages in MOS transistor circuits are proportional to the square-root of the signal by assuming saturation region operation at all devices. Therefore, a compression of voltage signal swing and a reduction of supply voltage are possible. Unfortunately, as a consequence of

the device mismatches this nonlinear operation may generate an excessive amount of distortion, linearization techniques are thus required in certain applications in which high linearity is principal. In addition, advanced processes, e.g., a complementary bipolar or a double-well CMOS integration process, are usually demanded in order to realize a high performance system [9].

On the other hand, the opamps still dominate the market not only because their well-developed and robust design techniques are common but also that their superior dynamic range performance makes them very hard to be defeated by the other structures. If high quality passive element, i.e., highly linear resistors and capacitors, are available on-chip, the active-RC filters can offer excellent linearity. Moreover, noise of the opamp can be made relatively low by designs, so that the resistors mainly contribute the noise performance. The passive resistor produces less noise than the other linearized active resistors or transconductors, thus the wider dynamic range is evident [1, 5, 10]. By incorporating the other advantages of the opamps that are the insensitivity to parasitics and possibility to be operated at low supply voltages (with a dedicated technique), the active-RC is a promising choice for applications where high performance and moderate speed are required. Indeed, the best performance analog filters at baseband frequency available now use the opamps as their crucial active devices [11, 12]

1.2 Purpose and Scope of the Study

Because the development of modern integration technologies is driven by the needs of digital integrated circuit design, deep-submicron CMOS technologies will be the main integration technology in the near future. Furthermore, because the high density of integration leads to low supply voltages, digital circuits will no longer benefit from the use of bipolar transistors. Consequently, the significance of BiCMOS integration technology is diminishing. Thus, in this work, predominantly standard low-cost N-well CMOS processes are used to realize the developed tunable analog baseband filters.

This thesis does not cover the entire field of analog filter design, which is extensive indeed. We concentrate on the design of high-order active filters deriving from functional emulation of the passive LC ladder filters, which are well known for their low passband sensitivity to component variations and component spreads. Most important, the time-constant of the active filters have to be made adjustable by means of an electronic control in order to automatically redeem the frequency characteristic errors from the process and temperature variations. The developed techniques have been carried out under two distinct categories, the resulting filters

of which are different both in signal mode of operation and in design philosophy.

The first methodology aims at an efficient implementation of the current-mode filter using an intuitive device partitioning procedure. Rather than converting the whole passive network to a large signal-flow graph (SFG) equivalent diagram, the network is first divided into subsections, and then realize SFG of each subsection one by one. This leads to a simple active filter implementation similar to the cascaded biquad technique, whereas the low sensitivity properties are still promised. This method possesses many advantages. In addition, each individual subsection SFG is simulated using a multi-output second-generation current controlled conveyor (MCCCII), the tunable internal impedance of which is utilized to electronically adjust the cut-off frequency of the filters and the multi-output structure is also suitable to the multi-loop feedback topology. Subsequently, all capacitors can be made grounded and no external resistors are required, thereby minimizing silicon area in IC implementation. Simulation results are given to denote the characteristics of the proposed scheme.

The other technique to be described herein focuses on the compensation of RC time-constant variation in the active-RC filters by investigating a tunable technique that is nearly free from the influence of the nonlinearities typically resulting from tunable elements. This results in a linear time-varying technique, in which a switch is placed in series with a passive resistor and the resulting effective resistance is made tunable via the duty cycle of the controlling clock. Since the switches' on-resistance can be designed to have relatively small in comparison to the linear passive resistors, their nonlinearities can be minimized. Operation principle and design parameters are formulated both for the systems that employ one set and two sets of the switch and resistor combination network. Their detailed analysis on the opamp slew rate induce distortion, frequency translation and cyclostationary noise are also given. This tuning fashion is extremely appropriate for very linear and very low-voltage applications since the tuning process occurs in time domain rather than voltage or current domain. Their performances are compared to the corresponding continuous-time filter both in terms of measurement and simulation results.

1.3 Thesis outline

This thesis consists of five chapters presenting the design aspects for a various kind of tunable active filters at baseband frequency. The organization of the thesis is outlined as follows:

Chapter 1 gives a motivation and historical perspective of the analog filter

synthesis development. The future direction, how to survive at present digital kingdom, is an interesting topic. The framework and objective of conducting this research work are included.

Chapter 2 reviews background theory of analog filter synthesis. Major active filter synthesis methods, for example, cascaded biquad and LC ladder simulation, and the continuous-time implementation of the integrator, e.g., active-RC, MOSFET-C, G_m-C and CCII-RC, will be discussed. The current-mode vs. voltage-mode issue, the dynamic range optimization of the filter, and the automatic tuning technique are also reported in brief.

Chapter 3 presents an efficient technique to simulate the operation of passive ladder prototype filter by using component partitioning method, so that the active filter can simply be realized by effectively implementing each partition. The implementation of every possible combinations up to two LC elements using multi-output second-generation current controlled conveyor are listed in tabular form, this thus makes it fairly easy to be executed. Several high-order filter realizations are adopted as examples, and their characteristics are shown via SPICE simulation results.

Chapter 4 provides a detailed analysis of the switched-resistor technique. The operation principle and design parameters of the switched-resistor network both employing one set and two sets of the switch and resistor combination are described, whereas the comparison between them will be demonstrated in term of the opamp slew rate induced distortion, frequency translation, and noise performance. Experimental results of the first-order filters and simulation results of the fifth-order elliptic filters are utilized to verify the theoretical analysis.

Finally, thesis conclusions and possible topics for future research are given in Chapter 5.

CHAPTER 2

ANALOG FILTER SYNTHESIS

2.1 Introduction

In the last decades many filters synthesis methods have been studied and made public [13–19]. Some methods show potential for very high frequency applications than the others since all internal node of the filter structure has a desired capacitance to ground [20]. In most cases, a second-order filter cannot provide an adequate selectivity, higher-order filter functions therefore have to be realized in order to satisfy the stringent selectivity requirements in telecommunication systems, signal processing circuits, special instrumentation, and many other applications.

In this chapter, a brief introduction of the popular filter synthesis and continuous-time active filter implementation techniques is given. The later sections also include general overviews on the dynamic range optimization and automatic tuning method, which are important aspects to the realization of high performance integrated filters.

2.2 Synthesis Methods

A simple way to realize high-order filter functions is to cascade the biquadratic circuits by connecting the output of each section to the input of the following one. This method has the advantages of simplicity in designing and aligning the filter, provided that the output of each section has very low impedance or practically zero [17]. Alternatively, there is another entirely different approach, which takes a passive filter and simulates it by means of active devices and circuits. LC filters have superior dynamic ranges and very low sensitivity in the passband, and these advantages can be expected to be carried out over to the active simulated network. In addition, there is a plenty of available tools for designing passive filters both in form of published tables and computer software. It is very easy to obtain a suitable passive filter that satisfies a desired specification and then simulate it with an active circuit. However, inductors in integrated circuits are feasible components at only the gigahertz range, LC ladder filter at baseband frequency therefore have to be simulated, typically, using two fundamental methods. The first one is the *element replacement* method, in which all inductors are

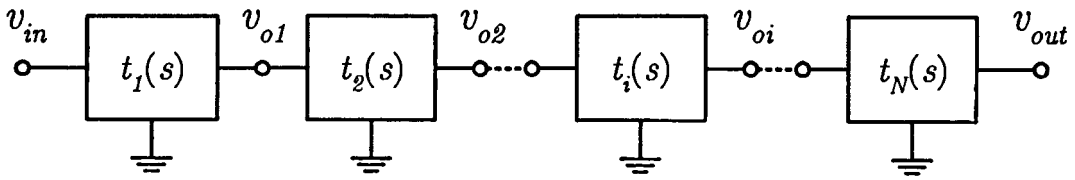


Figure 2.1 Cascade of low-order sections to realize a high-order transfer function.

replaced with simulated inductances either one by one or group by group, using active elements such as the gyrator, the generalized impedance converters (GICs) or the frequency-dependent negative resistances (FDNRs) [14, 16, 19]. The other one is that the internal node voltages and branch currents relationship of the LC ladder is first studied and then converted into an equivalent signal-flow graph (SFG). After some graph manipulations, the SFG diagram can be implemented using active circuits, basically the integrators [20]. This *functional simulation* technique has very low sensitivities to component mismatches since all errors due to passive or active elements tend to be distributed across the filter instead of concentrated at a specific section. This generally makes it more robust and, consequently, being widely used [12, 14, 16, 21–27].

2.2.1 Cascaded Biquad

As mentioned earlier, the simplest way for a high-order filter function realization is to factor both the numerator and denominator polynomials and then formulate it as a cascade connection of lower-order stages, which are preferably biquadratic, as shown in Fig. 2.1. If the function under realization is an odd order, there will be a first-order term, which can be realized according to the type of $T(s)$, i.e., whether it is low-pass, high-pass, etc. The circuit realization of such sub-blocks can be found in several modern filter design literatures [13–19].

Thus, the high-order filter function $T(s)$ can be written in the form

$$T(s) = t(s)\prod_{i=1}^{N} t_i(s), \tag{2.1}$$

where N is number of stages of the cascading structure. $t(s)$ is a first-order term for odd n order filter ($n = 2N+1$) or simply unity for even n filter ($n = 2N$), and $t_i(s)$ is a general biquadratic function,

$$t_i(s) = \frac{a_{i2}s^2 + a_{i1}s + a_{i0}}{s^2 + b_{i1}s + b_{i0}}. \quad (2.2)$$

Depending on $T(s)$, one or two of the numerator coefficients in (2.2) may be zero, whereas in the case of an all-pass function, the numerator coefficients will be equal to the corresponding coefficients of the denominator, with the additional constraint that $a_{i1} = -b_{i1}$, where $b_{i1} > 0$.

In forming each biquadratic term $t_i(s)$ and then cascading the biquad sections to obtain the overall circuit realizing $T(s)$, there are three degrees of freedom arising to all designer as are listed in the following:

- Pole-zero pairing, i.e., which poles with which zeros of $T(s)$ will be paired to form each $T_i(s)$.
- Distribution of the overall gain to various biquadratic sections.
- Physical position of each biquad in the cascade chain.

Clearly, the pole-zero pairing greatly affects the dynamic range of the corresponding biquad and consequently that of the whole filter. Also, the distribution of the filter gain among the various biquads influences their dynamic range, while the biquad sequence in the cascade chain has a significant effect on the total noise generation in the filter.

Because the total prescribed transfer function $T(s)$ is simply the product of $t_i(s)$, the choices in these three degrees of freedom are quite arbitrary as far as $T(s)$ is maintained. However, they determine significantly the dynamic range, i.e., the distance between the maximum possible undistorted signal (limited by the linearity of active devices) and the noise floor, because the maximum and minimum signal levels throughout the cascade filter depend on the pole-zero pairings, cascading sequence, and gain assignment. Consequently, the filter designer should take the advantages of these degrees of freedom in order to optimize the design with highly concerns on two main criteria: maximum of dynamic range (DR) and maximum of the signal-to-noise ratio (SNR) [16, 17].

2.2.2 Element Replacement

LC ladders that are in the form of an LC ladder terminated by a resistor at both ends as shown in Fig. 2.2 are known to yield low-sensitivity filters with excellent performance, but high-quality inductors cannot be implemented in integrated

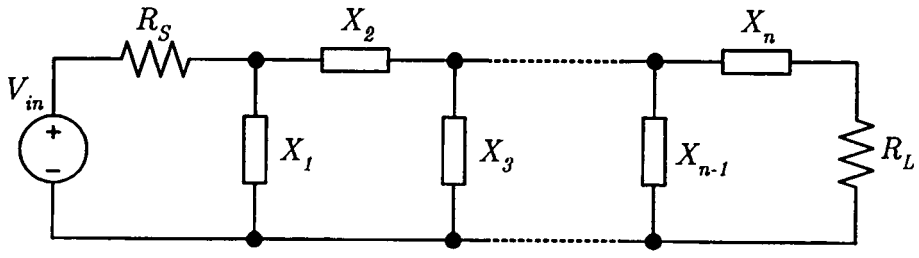


Figure 2.2 A doubly terminated ladder network.

circuit form at baseband frequency. An appealing solution to the filter design problem is, therefore, to retain the ladder structure and to simulate the behavior of the inductors by circuits consisting of resistors, capacitors, and active elements. A proven technique uses impedance converters, electronic circuits whose input impedance is proportional to frequency when loaded by an appropriate element at the output.

The best-known impedance converter is the gyrator or positive impedance inverter (PIV), a two-port circuit whose input impedance is inversely proportional to the load impedance. Its port relation is defined according to Fig. 2.3 by the transmission matrix of

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & r \\ 1/r & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}, \tag{2.3}$$

where the parameter r is called the gyration resistance [16, 20]. When the gyrator is loaded by an impedance Z_L as shown in Fig. 2.3, the input impedance seen at port 1 will become

$$Z_{in}(s) = \frac{V_1}{I_1} = \frac{r^2}{Z_L(s)}. \tag{2.4}$$

Clearly, when the load is a capacitor, $Z_L(s) = 1/(sC)$, $Z_{in}(s) = sr^2C$ is the impedance of an inductor of value $L = r^2C$. Gyrators are very easy to realize with transconductors (voltage-to-current converters) and are widely used in transconductance-C filters [16]. After converting a passive prototype filter into a gyrator-based circuit, the active filter can be further improved by using network transformation technique to eliminate all nodes with an undesired capacitance to ground. This improvement thus makes the gyrator filter particularly suitable for higher frequency applications [20].

If opamps are chosen to be the main active element, a more practical method would be the impedance converter technique. The general concept of various impedance converters can be represented by the generalized impedance

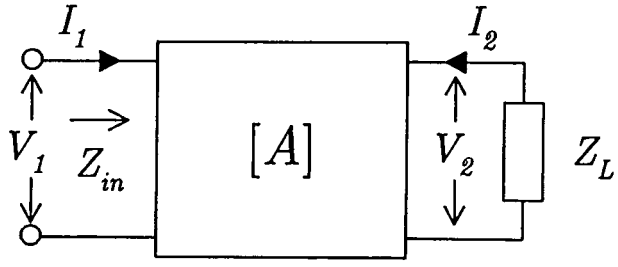


Figure 2.3 Basic two-port symbol with terminated impedance at port 2.

converter (GIC), a two-port network whose its transmission matrix $[A]$ is defined according to Fig. 2.3 as [17]

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} k & 0 \\ 0 & k/f(s) \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}. \tag{2.5}$$

where k is a positive constant and $f(s)$ is the impedance conversion function. Then, the input impedance at port 1 is of the following:

$$Z_{in}(s) = f(s)Z_L(s). \tag{2.6}$$

The GIC is very useful in LC ladder filter device substitution by active-RC networks. Among several GIC circuits, the most practical, versatile, and easy implementation is the one that was proposed by Antoniou [16–19], and it is shown in Fig. 2.4. After performing circuit analysis, the general input impedance of the circuit can be obtained as

$$Z_{in}(s) = \frac{Z_1(s)Z_3(s)}{Z_2(s)Z_4(s)}Z_L(s). \tag{2.7}$$

For a typical configuration to realize the GIC, either Z_2 or Z_4 is chosen to be a capacitor while the others are resistors [16–18]. When this circuit is terminated by a resistance R, the GIC will act as a positive-impedance converter (PIC) and the input impedance of which will be

$$Z_{in}(s) = \frac{sC_2R_1R_3}{R_4}R_L. \tag{2.8}$$

This is recognized as the impedance of an inductance $C_2R_1R_3R_L/R_4$, in henries. On the other hand, if Z_1 or Z_3 is chosen to be a capacitor while the others are resistors and a capacitor C is connected across port 2, the input impedance at port 1 will be

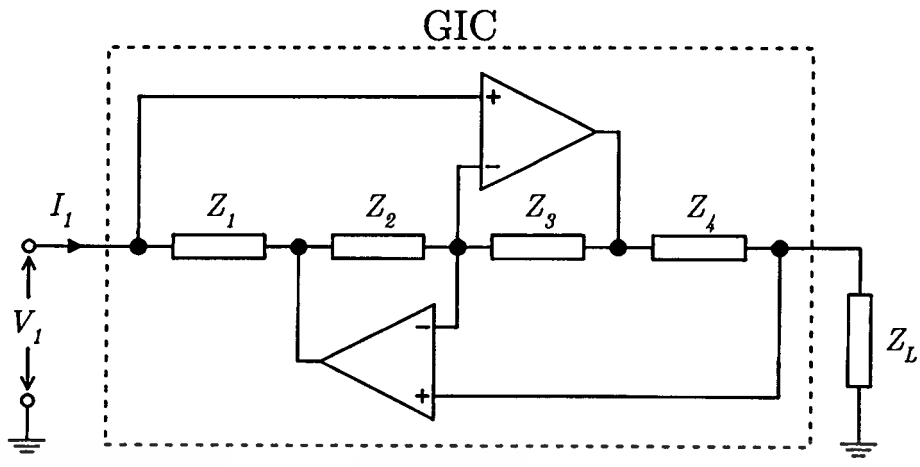


Figure 2.4 The most practical GIC circuit.

$$Z_{in}(s) = \frac{R_3}{sC_1R_2R_4}\frac{1}{sC_L} = \frac{R_3}{s^2C_1C_LR_2R_4}. \tag{2.9}$$

Substituting $s = j\omega$ gives

$$Z_{in}(\omega) = -\frac{R_3}{\omega^2C_1C_LR_2R_4}, \tag{2.10}$$

which is clearly a negative resistance dependent on frequency, hence the name frequency-dependent negative resistance (FDNR) of type-D (D-FDNR).

Refer back to Fig. 2.2, each grounded inductor is now ready to be replaced by a gyrator loaded with a capacitor or a GIC loaded with a resistor. In case of the floating inductor, an additional active element (gyrator or GIC) has to be placed back-to-back to the former simulated grounded inductor circuit in order to realize a floating structure. The FDNR procedure, however, is not as simple as the other two. The LC ladder filter requires a network transformation before the substitution, which is done by converting the resistor to the capacitor, the inductor to the resistor, and the capacitor to the FDNR. Even the source and load resistors are also converted to capacitors, so the resistive source and load terminations disappear. If these terminations are allocated outside the filter, they have to be reinserted into the filter without disturbing the overall transfer function, for example, using a unity gain buffer. In addition, the FDNR replacement is quite useful only for low-pass filters, where all capacitors are grounded, since floating FDNR structures cannot work well in practice [16–18].

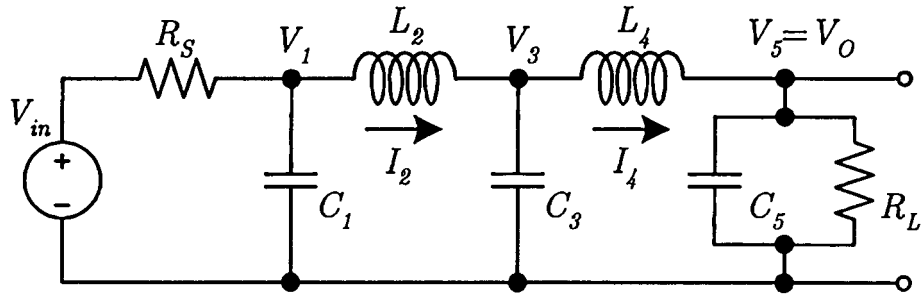


Figure 2.5 Fifth-order low-pass filter.

2.2.3 Functional Simulation

Another different approach for emulating the performance of passive LC ladders and inheriting their low sensitivities is to simulate the "operation" of the LC ladder, i.e., the equations that describe the topology of the LC ladder, rather than simulate the impedance of the inductances. Starting from an existing LC prototype ladder, the operational simulation models the internal operation of the ladder by simulating the circuit equations, that are the Kirchhoff's voltage and current laws and the $I - V$ relationship of the ladder arms. Fundamentally, this procedure simulates the signal-flow graph (SFG) of the ladder where all voltages and all currents are considered signals, which are integrated on the inductors and capacitors, respectively. Consider the fifth-order low-pass filter shown in Fig. 2.5, the relationships connecting the branch currents and the node voltages can be written in form of the integrating function as follow

$$\left.\begin{aligned} V_1 &= \frac{1}{sC_1}\left(\frac{V_{in}-V_1}{R_S} - I_2\right), \\ I_2 &= \frac{1}{sL_2}(V_1 - V_3), \\ V_3 &= \frac{1}{sC_3}(I_2 - I_4), \\ I_4 &= \frac{1}{sL_4}(V_3 - V_5), \\ V_5 &= \frac{1}{sC_5}\left(I_4 - \frac{V_5}{R_L}\right). \end{aligned}\right\} \tag{2.11}$$

It can be seen that all operations are represented in form of the integrator function. However, the input and output signals of each relation are still in different domain. This problem can be overcome by appropriately scaling or multiplying each equation with a resistor R_p. This procedure does not introduce any change to the overall transfer function, and it is usually chosen that $R_P = R_S = R_L$ to satisfy the power maximum transfer condition and maintain unity branch gain [20]. In fact, all signal parameters can be converted into either voltages or currents. This section shows a conversion example of voltage-mode filters, while the current domain circuits will appear later in Chapter 3. Applying the factor R_p into (2.11) results in

$$\left.\begin{aligned} -V_1 &= -\frac{1}{sC_1R_p}\left(\frac{V_{in}-V_1}{R_S}R_p - I_2R_p\right), \\ -I_2R_p &= \frac{R_p}{sL_2}(V_3 - V_1), \\ V_3 &= -\frac{1}{sC_3R_p}(I_4R_p - I_2R_p), \\ I_4R_p &= \frac{R_p}{sL_4}(V_3 - V_5), \\ -V_5 &= -\frac{1}{sC_5R_p}\left(I_4R_p - \frac{V_5}{R_L}R_p\right). \end{aligned}\right\} \tag{2.12}$$

Note that each signal polarity is also rearranged, so that only the summing operations take place and no inverter is required in the feedback path. In order to realize the overall active filter, it is usually helpful to produce it first in block diagram form and then insert the integrators and the other components in the places of the corresponding blocks. This results in a block diagram as shown in Fig. 2.6. This prototype filter will also be used as an implementation example in Chapter 3, where the current signals are mainly considered for an efficient implementation of current-mode filters using multi-output second-generation current controlled conveyors.

Although the network is already manipulated to avoid an inverter in the feedback path, there still some noninverting integrators exist. Since the implemen-

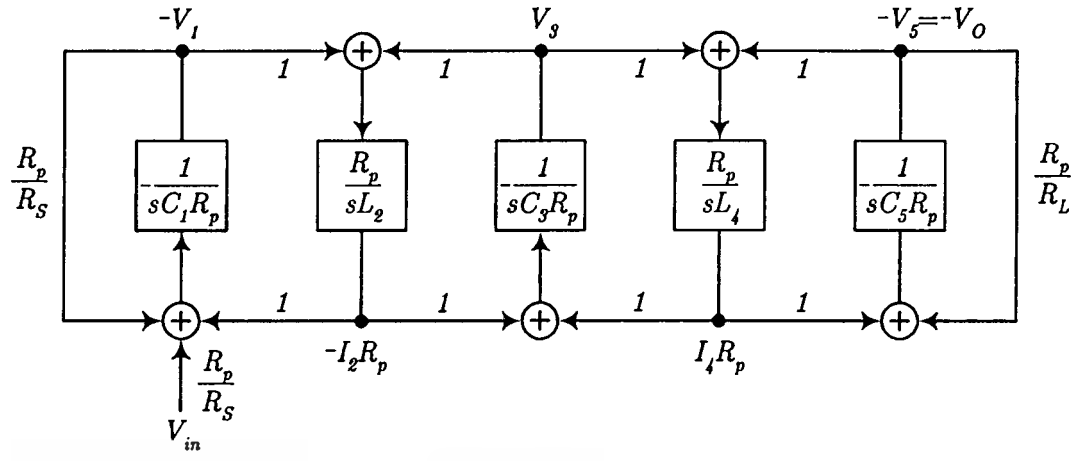


Figure 2.6 Block diagram of the active ladder simulating the operation of the fifth-order low-pass filter.

tation of a single-ended noninverting active-RC integrator requires two opamps, the balanced structure is practically used in high performance applications due to the fact that its output terminals can be exchanged in order to realize a noninverting function and it also offers a better dynamic range. Alternatively, the other active elements, for example, transconductors (G_m) and second-generation current conveyors (CCII), whose the inverting or noninverting operation is easily obtained by little change, can be used to realize the filter more efficiently. Because of the whole filter can be simulated in form of the integrator network, the performance of the filter then is limited by the employed integrators. Several circuit techniques to implement an integrator are given in Chapter 2.4.

2.3 Current-Mode versus Voltage-Mode

A considerable debate has arisen surrounding the term "current-mode processing." Several works in the past have usually claimed that there are fundamental advantages of the circuits using current-mode technique over the voltage-mode counterparts [7]. Though it is true that many current-mode circuits help break performance barrier in various applications, the reason does not come from that their signals are processed in current form, but because circuit simplicity, lower parasitic, and lower power consumption are often achieved with the cost of higher distortion, higher gain variation, and so on. This argument was discussed both in technical and philosophical terms, and it can be shown that there is no such performance difference due to the mode of signal to be found. Those different performances appear in literatures are owing to their different design structures

of current-mode and voltage-mode circuits [28].

Specifically, there are some physical properties that can be adopted to describe their difference in nature between current-mode and voltage-mode circuits. First of all, when signals are widely distributed as voltages, parasitic capacitances are charged and discharged with full voltage swings, which limit the speed and increase the power consumption of voltage-mode circuits. Current-mode circuits cannot avoid nodes with high voltage swings either, but these are usually local nodes with less parasitic capacitances. Therefore, it is possible to reach higher speed and lower dynamic power consumption with current-mode circuit techniques. Moreover, current-mode interconnection circuits particularly show promising performance in high speed applications [9]. As the signal is conveyed in form of a current, the voltages in MOS transistor circuits are proportional to the square-root of the signal if saturation region operation is assumed for the devices. Similarly, the voltages are proportional to the logarithm of the signal in bipolar transistor circuits. Therefore, a compression of voltage signal swing and a reduction of supply voltage are possible although it may face large out-of-band signal problems. This feature is utilized, for example, in log-domain filters [29], switched current filters [30], and the other nonlinear current-mode circuits in general. Unfortunately, as a consequence of device mismatches, these nonlinear operations may generate an excessive amount of distortion for applications with high linearity requirements. Thus, in certain current-mode circuits, linearization techniques are utilized to reduce the nonlinearity of the transistor transconductance without further limit on the voltage signal swing.

However, new solutions invariably entail new problems. The compression of the voltage signal swing, for example, increases sensitivity to mismatches. Similarly, a large amount of reported current-mode circuits demand advanced fabrication processes, for instance, a complementary bipolar integration processes utilizing vertical npn- and pnp-transistors with a high f_T is usually required, and an excessively high supply voltages is also necessary in order to be useful in most applications. Furthermore, some current-mode techniques such as the current-feedback are very old (compare to cathode-feedback in electron tube amplifiers) and are used as enhanced voltage-mode signal processing building blocks rather than as true current-mode signal processing building blocks [9].

Nevertheless, filters are not able to be exactly classified into voltage- or current-mode operation since both voltages and currents in the filters must be taken into account simultaneously. However, in this thesis the term *voltage-mode filter* simply refers to a filter that has voltage as its input and output processing signals. Similarly, a filter in which its transfer function is determined in current

domain is considered a *current-mode filter.*

2.4 Continuous-Time Active Filter Techniques

This section discusses four circuit techniques to implement an active integrator: Active-RC, MOSFET-C, Gm-C, and CCII-RC. Discrete-time analog filters, such as switched capacitor (SC) structures, are excluded in this thesis. For simplicity, single-ended configuration of the integrators are shown. However, balanced and differential topologies are usually employed in practice since they possess lower sensitivity to substrate and supply noise, and their even-order distortion is effectively suppressed. Moreover, their supply currents are less dependent on the signal thereby generating less supply noise. Although balanced filters approximately double the silicon area and power dissipation compared to single-ended counterparts, they achieve a 3-dB enhancement in SNR [31]. In other words, the area of balanced filters can be halved for the comparable SNR with the single-ended circuits.

2.4.1 Active-RC

The most widely known active filter technique uses operational amplifiers, resistors, and capacitors to perform integrator and filter functions. In an opamp-RC integrator, the opamp input forms a virtual ground and the input resistor then transforms the input voltage into current. Since there is no current flowing to the opamp input, the feedback capacitor integrates all the input current. In addition, input current signals can be summed at the opamp input node without any additional amplifier. An inverting opamp-RC integrator (Miller integrator) is shown in Fig. 2.7(a). A lossy integrator or a first-order filter can be built by adding a parallel resistor to the integrating capacitor, so there is no additional current required. A single-ended noninverting integrator requires an additional inverting amplifier in cascade with the Miller integrator, while balanced or differential topologies offer the signal polarity change by alternating the output signal lines. Owing to the fact that the opamp has to drive resistor loads, a voltage buffer like an emitter or source follower is usually required at the output. An OTA with high output impedance and sufficiently large transconductance gain g_m can also be used in active-RC filters instead of the buffered output opamps [4]. In the OTA-RC integrator shown in Fig. 2.7(b), the OTA forms a right-half-plane zero at g_m/C. This zero can be compensated using a resistor in series with the integrating capacitor. BiCMOS technology may be used in order to achieve a large g_m [4].

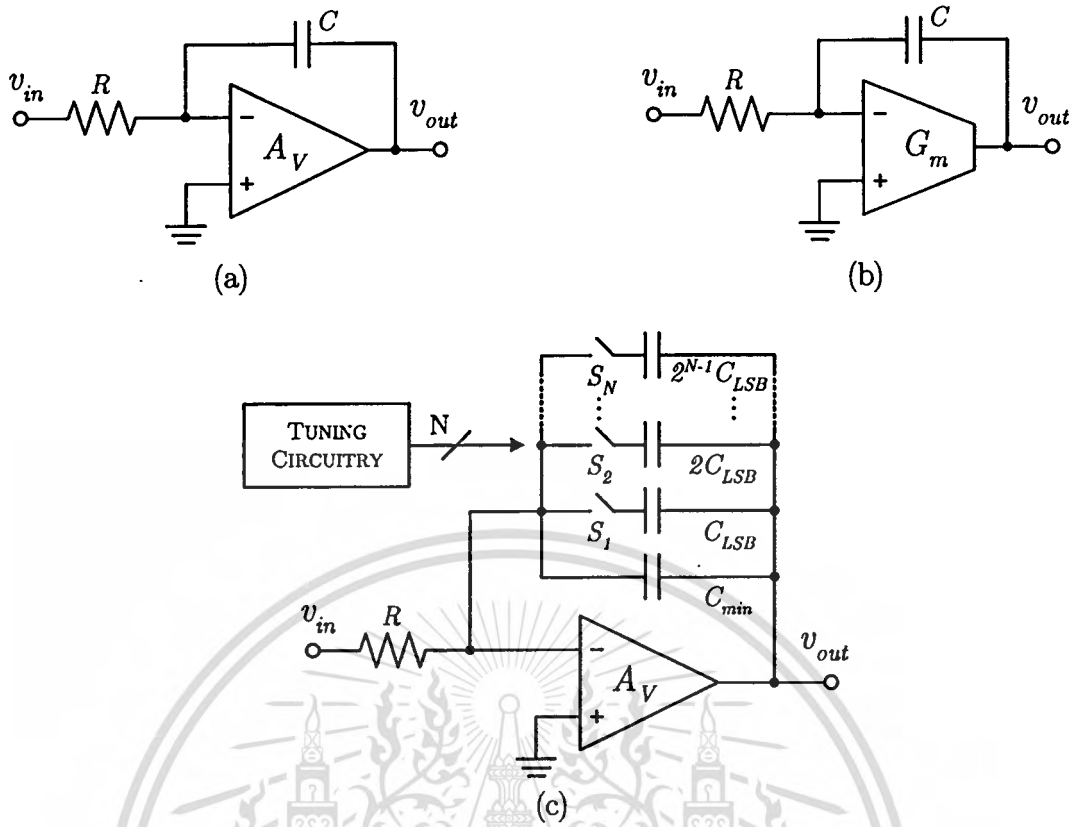


Figure 2.7 Active-RC integrator. (a) Opamp-RC. (b) OTA-RC. (c) tunable time-constant using parallel capacitor array.

The opamp-RC technique is insensitive to parasitic capacitances since the parasitic capacitances at the negative input and output of the opamp are driven by a voltage source or are connected to a virtual ground if an ideal opamp is assumed. Therefore, these capacitances do not affect the integrator transfer function in the ideal case. However, due to the finite DC gain, unity gain bandwidth, and non-zero output resistance of the opamp, the parasitic capacitances slightly affect the transfer function of the actual integrator.

In most CMOS processes, there are high quality polysilicon or metal capacitors available, whereas high quality resistors are available in few dedicated analog CMOS processes or with an additional cost. Even when both high quality capacitors and resistors are available in the process, the RC time-constant may vary by almost ±50% or even as much as a factor of 3–4 from the typical value when both process and temperature variations are taken into account [4, 5, 32, 33]. The integrated resistors in particular have large process variations and temperature dependencies, and these variations do not correlate with the variations of the capacitors. Since the time-constants could have significant fluctuation while most

applications do not allow large tolerances for the corner frequency of the filter, automatic tuning techniques have evolved in which elements are controlled by an additional tuning circuit.

The time-constant of an opamp-RC integrator is possible to be tuned using either series or parallel of capacitor or resistor arrays. Nevertheless, the series resistor and parallel capacitor arrays occupy less area than the other two options. Typically the parallel capacitors like the one shown in Fig. 2.7(c) are always used since the switch on-resistance is in series with the integrating capacitor resulting in a phase lead at high frequency. This phase lead tends to compensate the high frequency phase lag due to limited bandwidth of the opamp without shifting the integrator time-constant. This is an advantage that makes the parallel capacitor array having a better high frequency performance than the series resistor configuration [4, 32, 33]. Size of the parallel switched capacitors are binary-weighted to simplify the digital control signal. The location of MOS switches is dependent on the applications. When they are placed at input node of the opamp, their on-resistance contributes insignificant distortion, but the additional parasitic capacitances at the input of the opamp introduce phase lag. Alternatively, if the switches are placed to the output of the opamp, the parasitic capacitances have a minimal effect on the integrator performance when using a buffered opamp, but the voltage dependency of the switch on-resistance degrades linearity [9]. In addition, the bottom plate of the capacitor is usually placed to the opamp output to minimize the variation of the capacitive loading of the opamp [31].

Noise performance of an active-RC integrator is regularly determined by the resistors since the noise contribution from the opamp can be made small by a proper design. Therefore, an active-RC filter can achieve superior dynamic range compared to G_m-C and CCII-RC structures even in the case of a linearized transconductor that uses an internal feedback. This is because a resistor produces less noise than a transconductor that is built up from several transistors [5].

Indeed, due to several advantages of the opamp-RC filter technique, that are the insensitivity to parasitics, suitability for low supply voltages, excellent linearity, and large dynamic range, it is appropriate for applications where high performance and moderate speed are required. A tuning technique that makes use of the switching resistors, whose on-off period is controlled via a tunable-duty-cycle clock, to adjust the effective resistance in the active-RC filter will be discussed in Chapter 4. This timing control has been proved to be a promising tuning method for very linear and low-voltage applications.

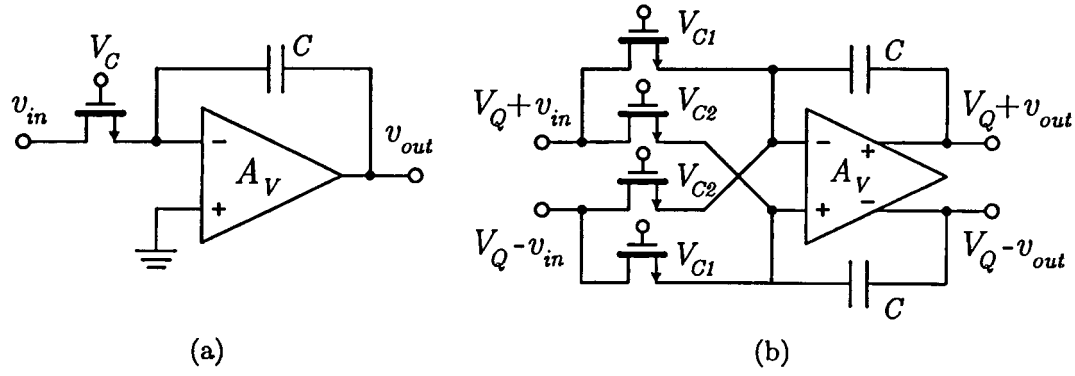


Figure 2.8 MOSFET-C integrator. (a) single-ended structure. (b) cross-coupled balanced structure.

2.4.2 MOSFET-C

An active-RC filter can also be implemented using a MOS transistor operated in triode region as a voltage-controlled resistor [21]. A basic single-ended MOSFET-C integrator is shown in Fig. 2.8(a), in which its time-constant can be made tunable via the gate voltage V_C. Since no capacitor array is required for tuning, the area can be reduced in comparison to the traditional active-RC integrators. However, the strong nonlinearity of the MOSFETs especially their significant second-order terms limit the use of large signals. Thus, the fully balanced structures are commonly used in these filters in order to suppress even-order distortion. The distortion can be further reduced by using four cross-coupled MOSFETs configuration as shown in Fig. 2.8(b) instead of two MOSFETS in a typical balanced integrator [34, 35]. A difference between two control voltages is used to control the resistance, resulting in an extended tuning range as the resistance increases to infinity when both control voltages become identical if ideally matched MOS-transistors are assumed. However, very high resistance values cannot be used in practice due to device mismatches and noise. A higher linearity can be achieved if a combination of passive resistors and current-steering MOSFETs are used [24], but this comes with a lack of insensitivity to parasitics source/drain capacitances [36].

Typically a large gate voltage is necessary for high linearity and to keep the MOSFETs in the triode region. This thus makes it difficult to achieve a large signal swing at low supply voltages. The control voltage can be driven over the positive supply with a charge-pump or bootstrapping circuit to improve the dynamic range of a MOSFET-C filter and to mitigate the sensitivity of the transfer function to DC offsets and variations in the common-mode level in the

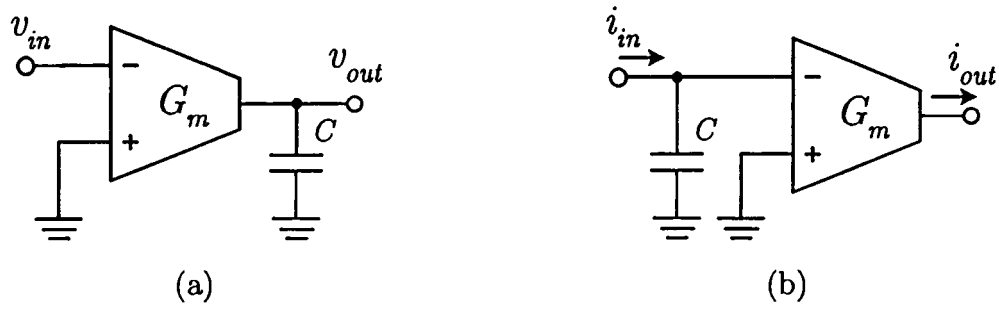


Figure 2.9 G_m-C integrator. (a) voltage-mode integrator. (b) current-mode integrator.

filter [4, 12]. The performance is enhanced at the expense of additional power dissipation in the charge-pump and a reliability problem due to device breakdown [37, 38]. In principle, the noise performance of a MOSFET-C integrator equals that of an equivalent active-RC structure, so does the dynamic range. Moreover, the speed and the parasitic insensitivity of the MOSFET-C technique are also correspondent to that of the active-RC filter.

2.4.3 G_m-C

Another widely used continuous-time filtering technique is a G_m-C filter, in which the transconductance g_m and the integration capacitor C are used to determine the unity-gain frequency of the integrator. The voltage-mode and current-mode inverting G_m-C integrators are shown in Figs. 2.9(a) and 2.9(b), respectively. g_m and the output conductance g_o of the transconductance cell define the DC gain of the integrator, while the internal time-constants of the transconductor form high-frequency poles and zeros. These nondominant poles usually occur at a much higher frequency than that of an opamp resulting in a much higher bandwidth of the G_m-C filter over the active-RC structure. In other words, the gain-bandwidth product (GBW) of the opamp has to be lower than the first parasitic pole determined by the load capacitance to avoid instability problem. This causes a limitation of the usable frequency range of the technique. In the G_m-C technique, the filter bandwidth is limited by the internal poles of the transconductor, which can approach the transistor f_T [4]. Moreover, the filter bandwidth can be maximized using transconductors without any internal pole at all [20].

While the first-order active-RC filter can simply be realized by adding a resistor in parallel with the integrating capacitor, the first-order G_m-C filters require an additional transconductor as an active load resistor. In addition, since the signals have to be summed as currents, a separate integrator is needed for

each input signal in the voltage-mode G_m-C filter technique. Similarly, additional integrators or multi-output devices are required for multi-loop feedback topologies in the current-mode G_m-C filter. On the other hand, the implementation of a single-ended noninverting active-RC integrator requires two opamps, whereas a noninverting G_m-C integrator can be obtained by just swapping the inputs of the transconductor or by feeding signal to both inputs and thus realizing the inverting and the noninverting integrators simultaneously with the same transconductor.

Because the integrating capacitor is grounded, all parasitic capacitances connected to the same node augment the total integration capacitance and thus displace the integrator time-constant from the desired value. Although the integrating capacitances can be slightly decreased to take into account the parasitic capacitances, the accurate value of the parasitics may not be known, so the capacitance matching accuracy is degraded. Moreover, the parasitic capacitances are nonlinear and do not track the actual capacitor values. The best performance is achieved when the relation between the different parasitic capacitances and integrating capacitances is equal in all integrators. However, this causes an additional source of inaccuracy in the frequency response of the G_m-C filter when compared to the active-RC technique.

A cascoded output stage is typically used to enhance the DC gain to a sufficiently high value, but it also significantly limits the output swing. In addition, the input stage experiences full signal swings, which also means that the input stage limits the minimum supply voltage. Therefore, the G_m-C filter cannot have a high dynamic range at a low supply. If a cascoded output stage is not used, a negative conductance circuit can be added in parallel to the output to make the load conductance sufficiently small. In that case, the achievable DC gain is limited to a few hundred for a predictable result [4].

Typically, the time-constant of a G_m-C integrator is tuned by adjusting the bias current of the transconductor or the gate-source voltage of triode-region MOSFET in an analog manner. Therefore, the tuning accuracy can be higher than that of a digitally controlled active-RC integrator, and the silicon area is minimized since there is no need of the passive element array. The continuous tuning of transconductors is performed at the expense of large signal handling capability [5]. The correct control signal, a current or voltage, can be derived using the master-slave tuning scheme [4].

In a balanced G_m-C filter, the integrating capacitors, or part of them, can be replaced with floating capacitors, which decrease the capacitance and silicon area by a factor of four. However, the bottom plate parasitic capacitances are also summed up to the integrating capacitance. This effect can be avoided by

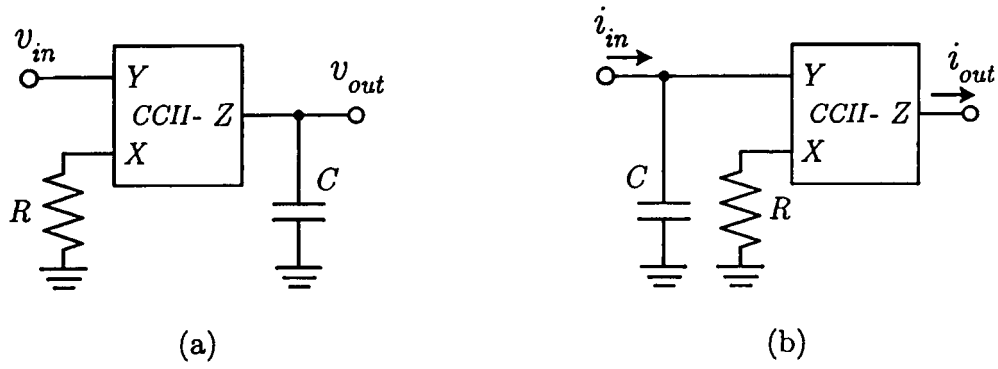


Figure 2.10 CCII-RC integrator. (a) voltage-mode integrator. (b) current-mode integrator.

separating the capacitor connection to ground [31].

The open-loop nature of G_m-C integrators means higher nonlinearity compared to active-RC filters. Although the feedback loops of the filter may reduce low frequency distortion in the passband, particulary in low-pass filters [9], this distortion suppression almost vanish at the passband edge in which the signals at filter nodes typically have the maximum values and the feedback gains are at the minimum. A large number of different circuits to improve the linearity of MOS transconductors have been published [39], and a simple one is to use an internal feedback, like in current conveyors [9]. However, they are still sensitive to parasitic capacitances at the integrator level. Typically, G_m-C filters consume less power and silicon area than the corresponding active-RC filters, but the in-band and out-of-band dynamic ranges are higher in the active-RC technique. Since several transistors, and possibly a few resistors, are required to build a linear transconductor, this thus makes a G_m-C integrator typically produces higher noise than an active-RC integrator, whose the resistor value equals to an inverse of g_m, by a factor of 2–3 [5].

2.4.4 CCII-RC

An inverting CCII-RC integrator based on a negative second-generation current conveyor is presented in Fig. 2.10. In order to reject even order nonlinearities, differential integrators may be used, where an additional common-mode feedback circuit is required to set the DC level at the outputs. For most negative second-generation current conveyors, the frequency dependencies of the forward voltage and current gains can be neglected because the parasitic capacitances at conveyor terminals dominate the frequency behavior [9]. However, the distortion

will still increase due to internal loop gain reduction at high frequency. A non-inverting CCII-RC integrator is simply obtained by using the positive type of second-generation current conveyors.

The resistance R should be considerably larger than the X-terminal impedance Z_X in order to keep the distortion and time-constant temperature drift low. The linearity of the CCII-based implementations is better than in the open-loop G_m-C structures, but the high-frequency performance is degraded although it is still good in comparison with the active-RC integrators [9]. For certain applications that the linearity is not a major concern, a MOS transistor operating in the triode region or even an intrinsic impedance at the X-terminal Z_X of the translinear loop CCII implementation [8, 40, 41] can be used instead of the passive resistor. These nonlinear devices introduce tuning capability to the CCII-RC filters with a cost of higher distortion. The X-terminal impedance has been applied to design tunable active ladder filters with the minimum requirement of the passive and active components, details of which will be discussed in Chapter 3.

2.5 Dynamic Range Optimization

The dynamic range of a signal processing system is defined as a ratio of the maximum and minimum signal levels that the system can efficiently process. The minimum signal level is determined by the noise floor of the system, while the distortion sets the maximum level. The dynamic range consideration of integrated continuous-time analog filters is important due to the fact that the filters have to be made tunable, thus the nonlinear elements are introduced in their circuits. Since all filters can be implemented using only integrator as a basic building block, the dynamic range of a filter is dependent on the dynamic range of the integrator and the filter network architecture [42]. Numerous attentions have been paid for optimizing the dynamic range of continuous-time active filters over the last decades. The most common approach is to assume that the filter saturates abruptly when any of its node voltages exceeds a certain maximum level V_{clip}, and the common procedure to achieve maximum dynamic range is done by scaling the filter components so that the same maximum voltage swing occurs at all nodes [16, 43–45].

After node-voltage scaling, the dynamic range in an active filter can be further improved by simply increasing all capacitances and reducing all resistances by the same proportion to maintain the identical frequency response. However, the chip area could grow larger due to the increasing of the capacitors especially in low frequency filters. This kind of dynamic range improvement thus may not

bring a real benefit. A better focus then is to maximize the dynamic range per total chip area (approximately the total capacitance). The silicon area taken up by the resistors is usually neglected in comparison to the area occupied by the capacitors. This optimization problem naturally leads to a linear programming problem [46].

The linearity performance, however, is usually evaluated with the IP3 (third-order intercept point) level of the filter or a similar figure of merit. Recently, it has been proven that the nonlinear elements of the filter give distortion contributions that "propagate" to the output with different gains. These individual distortion contributions therefore have a different effect on IP3, depending on where they are generated within the filter. Furthermore, these distortion components can tend to reinforce or cancel each other, depending on whether they add up in-phase or out-of-phase. As a result, it is not necessarily true that equating the voltage swings across the filter will lead to a maximum IP3 level [45].

In general, the distortion generated by a weakly nonlinear active filter can be analyzed using a Volterra series representation [47, 48]. The Volterra series theory is an extension of the theory of linear time invariant systems to weakly nonlinear systems, and it has been developed to describe the generation of additional tones occurring from the nonlinearities of the system. Volterra series is quite complicated, so its usage is rather limited in practical applications. Meanwhile, a simplified technique has been proposed in which the distortion is considered as a small signal disturbance generated by the nonlinear elements of the filter [45, 49]. It enables the optimization of the IP3 level of the system or a similarly defined figure of merit to be done easier. This method can be used for active filter implementations of any transfer function with any filter design technique. Moreover, both in-band and out-of-band signals are naturally taken into account [45].

2.6 Tuning in Active Filters

In order to control the RC time-constant of a filter accurately, an electronically tunable component is automatically tuned to a fixed reference of a known accuracy. Automatic tuning methods may be separated into two categories: *direct* and *indirect*. Indirect tuning is typically employed in practice, and there are several well-known implementations that use this method [23, 32, 50, 51]. This is because the indirect tuning process occurs in background, thus the filter operation needs not to be interrupted.

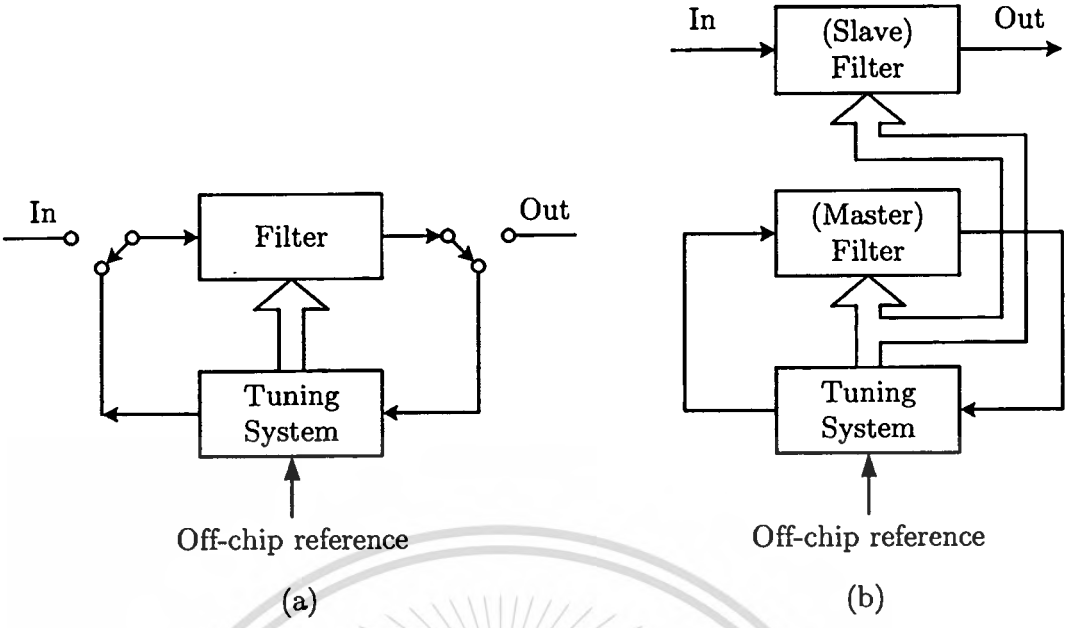


Figure 2.11 Automatic tuning. (a) Direct. (b) Indirect.

2.6.1 Direct Tuning Method

The principle of automatic tuning is shown in Fig. 2.11(a) [5, 16]. A filter is placed in a feedback loop, and its frequency response is adjusted until it becomes locked to an off-chip stable reference such as a clock frequency, which may be derived from the system clock at no extra cost. Another possible choice is making the filter resistances to be locked with an off-chip low-temperature-coefficient resistor [22]. The proper filter control voltage (or current) achieved by automatic tuning is then held while the filter is processing the signal [5]. This method gives a very precise frequency response since the filter is tuned directly to the accurate reference. However, due to temperature variation and aging, the filter has to be periodically taken out of the signal path by on-chip switches, and placed in an automatic tuning loop again for re-tuning. This thus causes an interruption of the filter operation. Therefore, such technique is suitable for applications that the filtering of input signals is only needed for certain period of time. Otherwise, a redundant circuit block is needed to mask the circuit to appear as if the operation is uninterrupted, which would require an extra circuit implementation with higher cost [46].

2.6.2 Indirect Tuning Method

If uninterrupted filtering is necessary, two identically on-chip filters may be used in time-interleaved fashion between tuning and system operation as shown

in Fig. 2.11(b) [5, 16]. As seen in the figure, the *master* filter is automatically tuned continuously, and the resulting control signal is also applied to the main (or *slave*) filter. Only the master section is used to compare to the accurate reference, allowing the main filter to operate at all times. The drawback resides in the master-slave matching relationship itself, which relies heavily on good component matching between the two circuit blocks. Any mismatch between the master and the slave will directly affect the accuracy of the desired corner frequency for the main filter [46]. A good matching is possible by placing both circuits in physical proximity on chip such that they undergo practically identical fabrication steps and are at practically the same temperature. This natural capability of integrated circuits to accurately match components gives fully integrated designs a fundamental advantage over discrete or partially integrated implementations [5].

Many conventional approaches reveal the use of a phase-locked loop in a master-slave configuration [4, 20, 23, 51]. The master is often a voltage-controlled oscillator (VCO) or a small low-order filter that is tuned by phase locking to an external reference frequency. This master is then used to indirectly tune the slave filter. This method has successfully demonstrated reliable performance, but with an unnecessary complexity [46].

2.7 Conclusions

In this chapter, the fundamental of filter implementation has been explained. Several major filter synthesis methods were summed up in brief. Although cascade filters behave relatively well, the passband sensitivities to component variations tend to become too large for many applications. The simulation of a doubly resistor-terminated ladder LC filter is therefore desirable, because it leads to active RC filters with very low sensitivity in the passband. This simulation can be achieved either by simulating the inductances by means of active elements, resistors and capacitors, or by simulating the operation of the ladder. The active elements in the first case are used to realize gyrators (PIVs), GICs (PICs), or D-FDNRs, whereas the integrator is an essential part of the second case. However, many active structures, which are not based on integrators, despite their popularity in discrete-component filters, cannot be used on chips. The reason is that the significant parasitic capacitances presented at every node in integrated circuits deteriorate the performance, unless such parasitics happen to be connected across ports with a well-controlled voltage. Indeed, the majority of high-order integrated active filters with demanding specifications have been designed with the operational simulation of LC ladders using integrators.

Four continuous-time integrator realizations were concisely introduced. The active-RC filter, although was founded in the early date, is still found the advantages in several modern applications. In fact, every technique has a merit of its own depending on how designer can exploit its best part to reach the requirement.

A debate of whether the voltage-mode or current-mode is really suitable to the high performance filter realization has arisen in many places, but the conclusion seems to be that their different performance does not originate from the difference in mode of signal, but from the deriving circuit techniques. Moreover, the good and bad properties are bunched up together in every architecture as a trade-off that are not entirely avoidable.

A traditional dynamic range optimization is usually done by scaling all filter nodes to face the same maximum voltage swing. This, however, is probably not adequate, and a more general optimization algorithm should be used to achieve the maximum dynamic range under the power dissipation and total chip area constraints.

Finally, since passive elements possess several sources of deviation, a tuning system is necessary in order to adjust all parameters into desired values in high performance filter implementations.

CHAPTER 3

CURRENT-MODE MCCCII-BASED FILTERS

3.1 Introduction

Current-mode signal processing has been substantially considered since it offers several alternative choices for circuit designers. Although there is no fundamental advantage found from considering current signals as principal, designing circuit under current-mode point of view may show an accessible way to achieve a better performance. For instance, current-mode circuit design usually has low internal nodes impedance, which gives a potential to achieve a large bandwidth. This simply allows us to burn more power for higher performance with less effort. As signals are represented by current, internal voltages are compressed so that a low-voltage operation can be accomplished [7, 8]. Furthermore, summation and subtraction of signal currents can be directly performed at circuit nodes, resulting in a simple structure. Consequently, many suggestions of the current-mode techniques to convert a passive filter prototype to a signal flow graph employing multiple output operational transconductance amplifiers (OTAs) and second-generation current conveyors (CCIIs) have been published [17, 52–56]. However, most of them realize the simulated transfer function in rather complicated ways, and they do not possess the optimal or efficient employment of active and passive elements. Also the realization may not have a direct connection to the prototype RLC filters, thus the sensitivity may not be necessarily low. Recently, the linear transformation has been adopted to realize the active ladder filters with some good results [55, 56]. But, complex synthesis equations as well as some external resistors are required, and the utilized frequency is fixed by their determined passive elements.

Rather than converting the whole network to a large SFG equivalent diagram, this chapter describes an intuitive idea to divide the original ladder network into subsections, and then realize an individual SFG of each subsection one by one. Therefore, the low sensitivity basis is guaranteed, and the complexity of a large SFG diagram is avoided. This methodology possesses many advantages. First of all, the structure is very simple and easy to design including realization of the

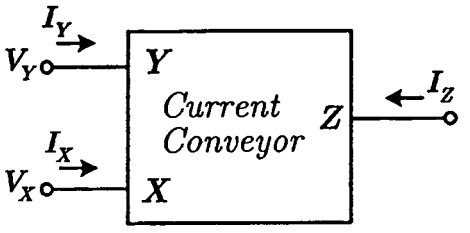


Figure 3.1 Current conveyor symbol and its signal definitions.

finite transmission zero. Next, each individual subsection SFG is simulated using multi-output second-generation current controlled conveyors (MCCCIIs), the tunable internal impedance of which is utilized to electronically adjust the cut-off frequency of the filters. Subsequently, all capacitors are grounded and no external resistors are required, thereby saving chip area in IC implementation.

3.2 Multi-Output Second-Generation Current Controlled Conveyor

3.2.1 Principle of Current Conveyors

The concept of current conveyors was first presented in 1968 [57] and further developed to a second-generation current conveyor in 1970 [58]. The current conveyor is intended to be a general building block as the operational amplifier (opamp). Because of the opamp concept has been current since the late 1940's, it is difficult to get any other similar concept widely accepted. However, opamps do not perform well in applications where a current output signal is needed and consequently there is an application field for current conveyor circuits. In addition, current conveyors usually operate without any global feedback, so a higher frequency behavior compared to opamp circuits is achieved.

Current conveyors are three-port networks with terminals X, Y, and Z as represented in Fig. 3.1. The network of the first-generation current conveyor (CCI) is defined by its terminal currents and voltages in a matrix form as follow

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}. \tag{3.1}$$

In other words, the CCI forces both the currents and the voltages in ports X and Y to be equal, and a replica of the currents is mirrored (or conveyed) to the output port Z.

In many applications, only one of virtual grounds in terminals X and Y of the CCI is used and the other unused terminal must be grounded or otherwise connected to a suitable potential. This grounding must be done carefully since a poorly grounded input terminal may cause an unwanted negative impedance at the other input terminal [9]. Moreover, a high impedance input terminal is required in many applications. For these reasons, the second-generation current conveyor (CCII) was developed. It has one high and one low impedance inputs rather than the two low impedance inputs of the CCI [58]. The matrix representation of the CCII is

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}. \tag{3.2}$$

This current conveyor differs from the CCI in that the terminal Y is a high impedance port, i.e., there is no current flowing into Y. While the Y-terminal of the CCII is a voltage input and the Z-terminal is a current output, the X-terminal can be used both as a voltage output or as a current input. Therefore, this current conveyor can easily be used to process both current and voltage signals unlike the CCI or the opamp. A further enhancement to the CCII is that there are two types of conveyors: in the positive current conveyor CCII+, the currents I_X and I_Z have the same direction like a current-mirror and in the negative current-conveyor CCII– the currents I_X and I_Z have opposite direction like a current buffer.

Yet another current conveyor was proposed in 1995 [59]. It was named a third-generation current conveyor (CCIII) and can be formulated in a matrix form as

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}. \tag{3.3}$$

The operation of the CCIII is similar to that of the CCI, with the exception that the currents in ports X and Y flow in opposite directions.

Due to several advantages of the CCII over the other types of current conveyors, it has been extensively applied in a wide range of applications such as amplifiers, filters, or more generally signal processing circuits [7, 8, 13, 54–56]. By implementing the CCII with a mixed translinear loop composed of complimentary transistor [8, 40, 41], its intrinsic impedance at port X can be made tunable via the bias current, hence the name second-generation current controlled conveyor [60].

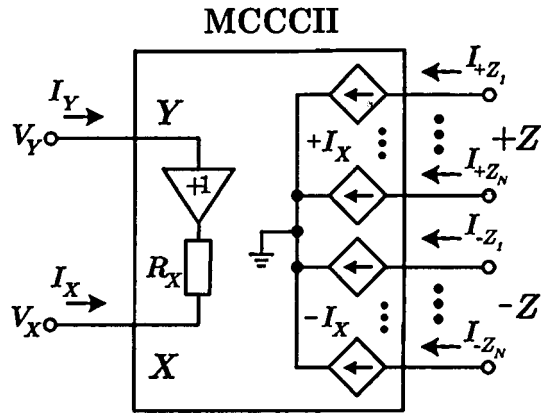


Figure 3.2 Equivalent circuit of MCCCII.

3.2.2 Multi-Output Characteristic

Typically, current conveyors have only one output current terminal, whose signal is available only once for each feedback path. Therefore, in multi-loop feedback topologies, which require several duplicated signals, multi-output configuration will gain more advantages. Moreover, it gives a possibility to implement both the positive– and the negative–type CCII within one building block. The equivalent circuit of MCCCII is shown in Fig. 3.2, and its port relations can be described by a matrix form as follow

$$\begin{bmatrix} I_Y \\ V_X \\ I_{+z} \\ I_{-z} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & R_X & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_{+z} \\ V_{-z} \end{bmatrix}, \tag{3.4}$$

where R_X is an intrinsic resistance of the current input port X, and it is possible to be controlled by varying the external bias current [60, 61].

3.2.3 Circuit Implementation

The implementation of a current conveyor based on a complementary push-pull class-AB has gained popularity in many applications since its structure is as simple as a basic OTA but consumes less power [60, 61]. Although the bipolar technologies provide higher gain, greater linearity, and wider frequency bandwidth, CMOS technologies have been in wide spread use in almost all areas of applications when low power consumption, low cost, and suitability for mixed analog/digital implementations are of major concerns. Circuit schematic of a CMOS multi-output push-pull MCCCII is shown in Fig. 3.3. All transistors are biased to operate

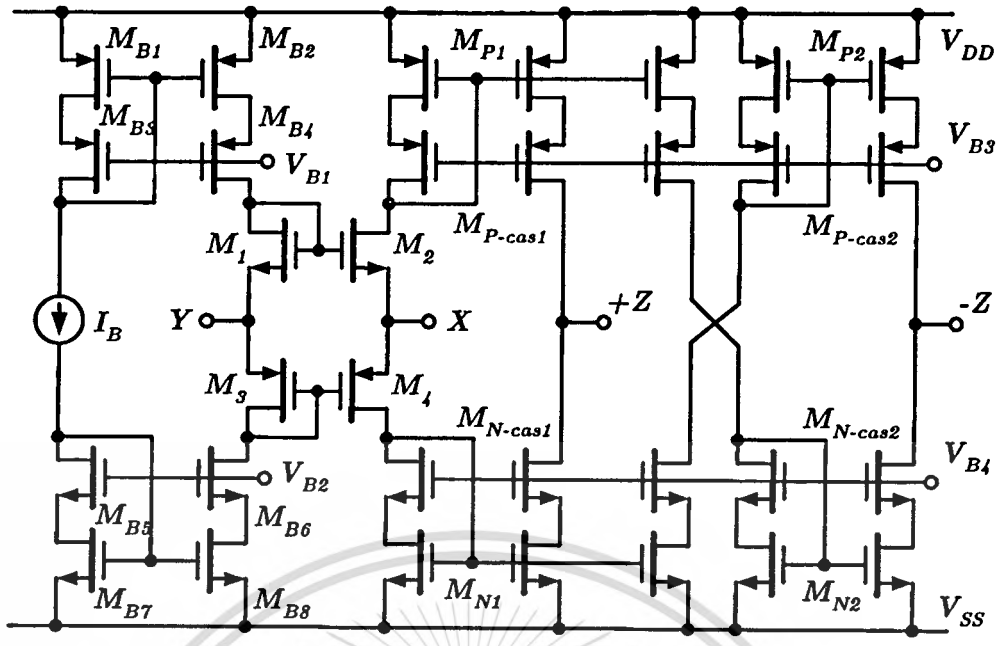


Figure 3.3 Circuit schematic of a CMOS MCCCII.

in saturation region. The multi-output topology can be easily implemented by appending additional output transistors to the current mirrors at port +Z and –Z as required. However, having more utilized output ports comes with cost, that the frequency performance is compromised as will be evident in later section.

3.2.4 Nonlinearity Consideration

Nonlinearity of two major circuit operations are considered: transconductor, in which the X-terminal is grounded, and current buffer, in which the Y-terminal is grounded. Both the Y-terminal-voltage-induced current and the input current that directly flows into the X-terminal have been nonlinearly divided into two paths flowing through the output NMOS and PMOS current mirrors, before they are duplicated and summed up again at the +Z and –Z-outputs. Therefore, this current division must be analyzed as mismatches in these signal paths. First, consider an input voltage applying to Y-terminal of the transconductor. This voltage will induce a current at the X-terminal, which in turn flow into the upper and lower transistors, M_2 and M_4, respectively. Assuming that $K_1 = K_2 = K_N, K_3 = K_4 = K_P, V_{T1} = V_{T2} = V_{TN}$ and $V_{T3} = V_{T4} = V_{TP}$, the divided currents that are induced from input voltage at Y-terminal can be written as

$$i_{D2-Y} = \begin{cases} I_B + 2v_Y\sqrt{K_N I_B} + K_N v_Y^2 & \text{for} \quad v_Y > -\sqrt{\dfrac{I_B}{K_N}} \\ 0 & \text{for} \quad v_Y < -\sqrt{\dfrac{I_B}{K_N}} \end{cases}, \tag{3.5a}$$

$$i_{D4-Y} = \begin{cases} I_B - 2v_Y\sqrt{K_P I_B} + K_P v_Y^2 & \text{for} \quad v_Y < +\sqrt{\dfrac{I_B}{K_P}} \\ 0 & \text{for} \quad v_Y > +\sqrt{\dfrac{I_B}{K_P}} \end{cases}, \tag{3.5b}$$

where I_B is the bias current and MOSFET parameter $K_{N(P)} = \mu_{N(P)} C_{OX}(W/L)/2$. Combining these two branch currents in (3.5a) and (3.5b) results in the total current flowing *out* of the X-terminal as

$$\begin{aligned} i_{X-Y} &= i_{D2-Y} - i_{D4-Y} \\ &= 2\sqrt{I_B}\left(\sqrt{K_N} + \sqrt{K_P}\right) v_Y + (K_N - K_P)\, v_Y^2. \end{aligned} \tag{3.6}$$

Note that the short transition to weak inversion before the complete transistor turn-off is neglected, as this current does not normally contribute to a large error in the total current in the X-terminal if the bias current I_B is sufficiently large. Then the X-terminal current could be a linear function of the Y-input voltage, and the intrinsic resistance R_X can be considered as a linear resistor of $1/4\sqrt{KI_B}\ \Omega$, as long as $K_N = K_P = K$ and $|i_X| < 4I_B$ are assumed [9]. This also implies that all transistors in the push-pull current conveyor will remain in saturation region until X-current signal is almost four times larger than the bias current I_B. Thus, its class-A operation range is nearly four times greater than that of a typical class-A current conveyor. It is also evident that R_X is made tunable via the bias current since it is inversely proportional to $\sqrt{I_B}$.

This is also true for the input current directly flowing *into* the X-terminal in the current buffering operation, in which the currents in two divided paths are

$$i_{D2-X} = \begin{cases} I_B - 2v_X\sqrt{K_N I_B} + K_N v_X^2 & \text{for} \quad v_X < +\sqrt{\dfrac{I_B}{K_N}} \\ 0 & \text{for} \quad v_X > +\sqrt{\dfrac{I_B}{K_N}} \end{cases}, \tag{3.7a}$$

$$i_{D4-X} = \begin{cases} I_B + 2v_X\sqrt{K_P I_B} + K_P v_X^2 & \text{for} \quad v_X > -\sqrt{\dfrac{I_B}{K_P}} \\ 0 & \text{for} \quad v_X < -\sqrt{\dfrac{I_B}{K_P}} \end{cases}, \tag{3.7b}$$

and the total current at the X-terminal is

$$\begin{aligned} i_{X-X} &= i_{D4-X} - i_{D2-X} \\ &= 2\sqrt{I_B}\left(\sqrt{K_N} + \sqrt{K_P}\right)v_X + (K_P - K_N)\,v_X^2. \end{aligned} \tag{3.8}$$

The wide swing cascode current mirrors are chosen in order to minimize the current transfer error and raise the output impedance. The cascode transistors M_{P-cas} and M_{N-cas} help control the drain-source voltage v_{DS} between transistors within the current mirrors M_P and M_N. The difference of drain-source voltages between the mirror transistors is in the order of a few millivolts for a proper design, hence the distortion from the channel length modulation effect is insignificant. However, the wide swing cascode structure means that a high supply voltage is required, and it will also limit an usable tuning range of the bias current since a very large bias current will push the mirror transistors into non-saturation region, while the cascode transistors will enter non-saturation region instead for too low bias current.

3.2.5 Frequency Limitation

Small-signal equivalent circuit of the upper half from Y-terminal to +Z-terminal of the MCCCII operating as a transconductor is presented in Fig. 3.4, in which the transistor output conductance g_{ds} is assumed to be much smaller than the transconductance g_m and the conductance g_l (in the load admittance $y_l = g_l + sC_l$). For simplicity, all current mirrors are considered as simple MOS current mirrors since the cascode transistors barely contribute to the overall frequency response limitation. The capacitance C_{+Zn} consists of the gate-source capacitances C_{gsP} of the mirror transistors M_P and all other parasitic capacitances at node

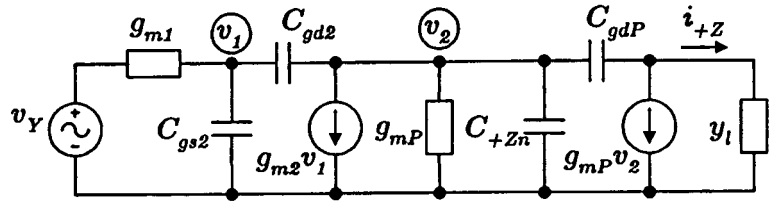


Figure 3.4 The upper half small-signal equivalent circuit of MCCCII-based transconductor.

v_2, excluding the gate-drain capacitances C_{gd2} and C_{gdP}. Typically, the current mirror transistors usually have relatively large gate areas in order to minimize the current transfer error. Therefore, the gate-source capacitances are dominant and consequently the approximated C_{+Zn} can be determined as

$$C_{+Zn} \approx (n+2)C_{gsP} = (n+2)\frac{2}{3}C_{ox}W_PL_P, \tag{3.9}$$

where n is the number of the output +Z ports, and all mirror transistors have the same size. Note that the number $n+2$ in the parenthesis will become $n+1$ if the –Z-terminal is absent.

Suppose that the gate-drain capacitances C_{gd} are far smaller than the capacitances C_{+Zn} and C_l, the upper half v_Y-to-i_{+Z} transconductance function therefore can be shown as

$$\left.\frac{i_{+Z}}{v_Y}\right|_{\text{upper half}} \approx g_{m2}\frac{\left(s\frac{C_{gd2}}{g_{m2}}-1\right)\left(s\frac{C_{gdP}}{g_{mP}}-1\right)}{\left(s\frac{C_{gs2}}{g_{m1}}+1\right)\left(s\frac{C_{+Zn}}{g_{mP}}+1\right)}. \tag{3.10}$$

The transfer function has two poles and two right half-plane (RHP) zeros. The first pole is the product of NMOS parameters that usually results in a much higher frequency than the second pole, which is originated from PMOS current mirror M_{P1}, especially for the multi-output circuits. The RHP zeros do not contribute a great deal to the amplitude response near the corner frequency, but the phase response can be degraded due to phase shift from the zeros. Furthermore, the relatively insignificant Miller effect of C_{gd} can be reduced even further by incorporating the cascode transistors into the current-mirrors. Accordingly, the second pole can be assumed as the dominant pole that limits the frequency response of the upper half circuit, and the corner frequency can be expressed as a function of device dimensions, number of +Z ports, and bias current in form of

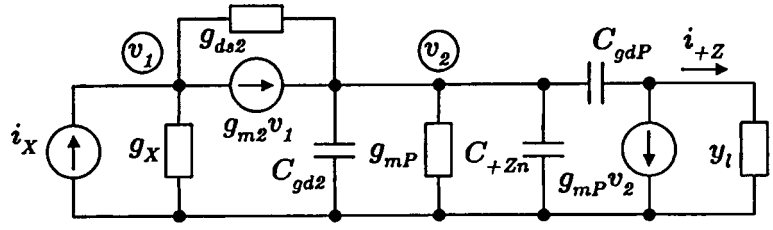


Figure 3.5 The upper half small-signal equivalent circuit of MCCCII-based current buffer.

$$\omega_0 = \frac{3}{n+2}\sqrt{\frac{\mu_P I_B}{2C_{ox}W_P L_P^3}}. \tag{3.11}$$

This equation shows a trade-off between bandwidth and number of ports. Therefore, the port numbers must be minimized in order to use in higher frequency applications. As the corner frequency strongly depends on the channel length, there is also a strong trade-off between bandwidth and gain accuracy as well as bandwidth and distortion [9].

Frequency response of the lower half circuit of the +Z-terminal can be derived in similar way. It then results in a dominant pole at the current mirror M_{N1}. However, such pole frequency is almost three times larger than that of the upper half circuit due to the greater mobility of NMOS over PMOS transistors. In addition, frequency response of the –Z-terminal possess some additional poles and RHP zeros due to the current mirrors M_{P2} and M_{N2}. As a result, the number of the –Z-ports must be reduced to minimum in order to prevent further limitation on the operating frequency.

In case of the current buffering operation, small-signal equivalent circuit of the upper half from X-terminal to +Z-terminal is shown in Fig. 3.5 by assuming that all current mirror transistors are matched and g_{ds} is much smaller than g_m and g_l. If C_{gd} is also far smaller than C_{+Zn} and C_l, the upper half i_X-to-i_{+Z} current transfer can be shown as

$$\left.\frac{i_{+Z}}{i_X}\right|_{\text{upper half}} \approx \frac{g_{mP}}{g_{mP}-g_{ds2}} \frac{\left(s\frac{C_{gdP}}{g_{mP}}-1\right)}{\left(s\frac{C_{+Zn}}{g_{mP}-g_{ds2}}+1\right)}. \tag{3.12}$$

The same conclusion is obtained, that the PMOS current mirror M_{P1} causes the dominant frequency limitation. Thus, (3.11) is also applicable to approximately determine the corner frequency of the buffer as well as the number of output port

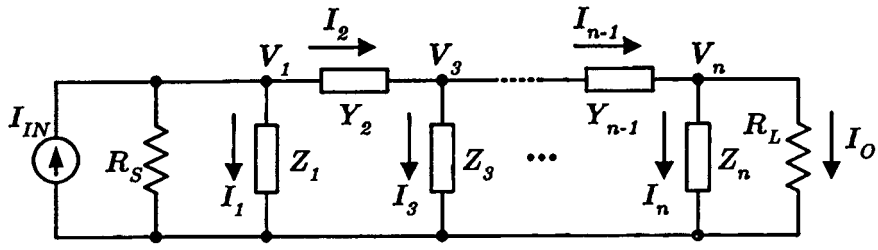


Figure 3.6 General doubly terminated ladder network

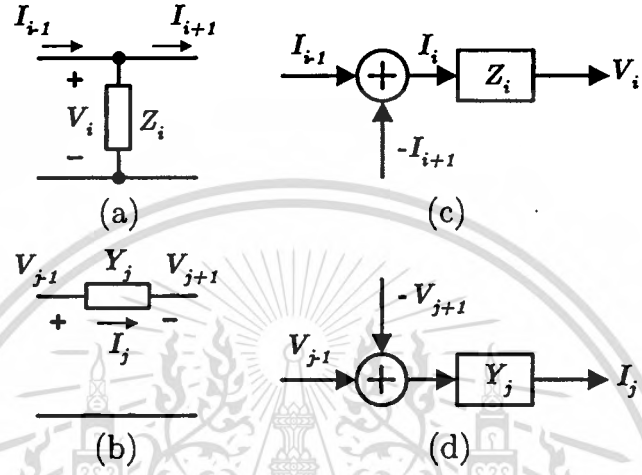


Figure 3.7 Fundamental operations (a) shunt branch (b) equivalent shunt branch (c) series branch (d) equivalent series branch

should be kept small.

3.3 Efficient Filter Implementation

The traditional SFG simulation technique emulates voltage-current relationship of all elements in the prototype ladder filters as one diagram. For a large network, however, this appears to be a roundabout and impractical way [18]. In this section, a new viewpoint will be described. The idea is based on a partitioning of a large network into individual basic sections and then realize each subsection by an appropriate active circuit.

3.3.1 Current-Domain Ladder Component Partitioning

Consider a general doubly terminated lossless passive ladder network in Fig. 3.6. Such a network can be partitioned into two basic sections: shunt and

series (as depicted in Figs. 3.7(a) and 3.7(b), respectively), the corresponding SFG equivalent block diagrams of which are shown in Figs. 3.7(c) and 3.7(d). The block diagram in Fig. 3.7(c) (and Fig. 3.7(d)) represents the output voltage (current) as a result of the product of the impedance (admittance) and the subtraction between corresponding current (voltage) of the previous and next stages. Therefore, the overall equivalent structure can be constructed by a proper cascading of these two equivalent branches. With these two basic operations, the branch relationship for the entire structure can be rewritten in form of

$$\left.\begin{aligned} V_1 &= Z_1\left(I_{IN} - I_2 - \frac{V_1}{R_S}\right), \\ I_2 &= Y_2\left(V_1 - V_3\right), \\ V_3 &= Z_3\left(I_2 - I_4\right), \\ &\vdots \\ V_n &= Z_n\left(I_{n-1} - I_o\right), \\ I_o &= \frac{V_n}{R_L}. \end{aligned}\right\} \tag{3.13}$$

Since the summation or subtraction of current signals can be implemented at circuit nodes, converting all variables into current forms will lead to design simplicity. The conversion is simply performed by either normalizing or scaling the equations with resistance R_p. All relations in (3.13) are then transformed into their corresponding current transfer functions as

$$\left.\begin{aligned}
\frac{V_1}{R_p} &= \frac{Z_1}{R_p}\left(I_{IN} - I_2 - \frac{V_1}{R_S}\right), \\
I_2 &= Y_2 R_p \left(\frac{V_1}{R_p} - \frac{V_3}{R_p}\right), \\
\frac{V_3}{R_p} &= \frac{Z_3}{R_p}\left(I_2 - I_4\right), \\
&\vdots \\
\frac{V_n}{R_p} &= \frac{Z_n}{R_p}\left(I_{n-1} - I_o\right), \\
I_o &= \frac{R_p}{R_L}\frac{V_n}{R_p}.
\end{aligned}\right\} \tag{3.14}$$

After the separated shunt and series portions have been created for the prototype ladder network, they will be subsequently implemented using the MC-CCIIs. Each block of them has two outputs: a positive output for the forward path and a negative output for the feedback path. Finally, cascading every portion of branches back together with proper connections of the feed forward and feedback paths will result in the complete equivalent circuit. This method is as easy as the synthetic element replacement, yet maintaining the benefit of low sensitivity of the ladder structure.

3.3.2 Synthesis of Branch Elements using MCCCII

After the separated shunt and series portions have been created for the prototype ladder network, they will be subsequently implemented using the MC-CCIIs. Each block of them has two outputs: a positive output for the forward path and a negative output for the feedback path. Finally, cascading every portion of branches back together with proper connections of the feed forward and feedback paths will result in the complete equivalent circuit. This method is as easy as the synthetic element replacement, yet maintaining the benefit of low sensitivity of the ladder structure.

The equivalent MCCCII-based components for simulating the two fundamental operations in Fig. 3.7 and the use of R_X as a tunable parameter fall into 4 categories namely (1) single passive element (2) single passive element with source

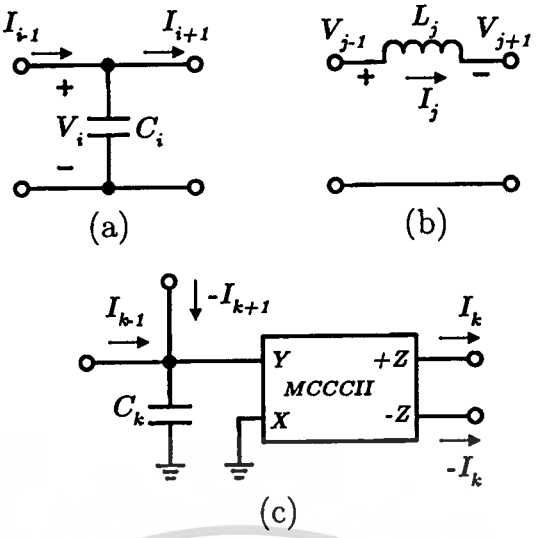


Figure 3.8 Single passive element (a) shunt C (b) series L (c) equivalent MCCCII structure

or load resistor (3) double passive elements and (4) double passive elements with source or load resistor, details of which will be described in the following sections.

3.3.3 Simulation of Single Passive Element

The first two basic single passive element frames: a shunt capacitor branch and a series inductor branch, are shown in Figs. 3.8(a) and 3.8(b), respectively. With all voltage signals transformed into their current counterparts by a scaling resistance R_p as mentioned in Chapter 3.3.1, their voltage and current relations in form of current transfer functions can be shown as

$$\frac{V_i}{R_p} = \frac{1}{sC_iR_p}(I_{i-1} - I_{i+1}), \tag{3.15a}$$

$$I_j = \frac{R_p}{sL_j}\left(\frac{V_{j-1}}{R_p} - \frac{V_{j+1}}{R_p}\right). \tag{3.15b}$$

Obviously, both equations represent an integrating function. Hence, they can be simulated by an equivalent MCCCII integrator in Fig. 3.8(c), which has the current transfer function of

$$I_k = \frac{1}{sC_kR_X}(I_{k-1} - I_{k+1}). \tag{3.16}$$

Mapping the equivalent circuit to the shunt capacitor by letting $I_k = V_i/R_p$,

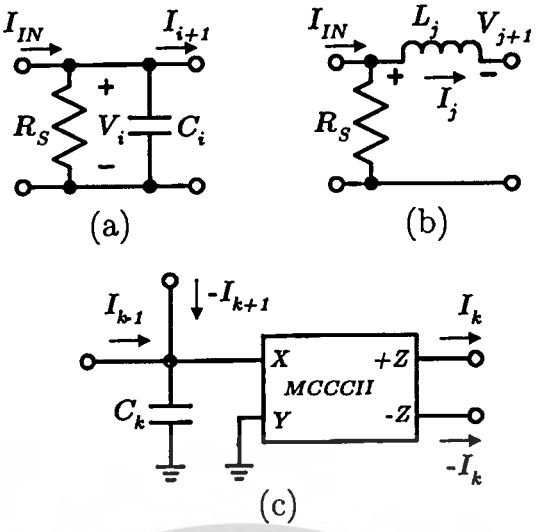


Figure 3.9 Single passive element with source resistor (a) shunt C (b) series L (c) equivalent MCCCII structure

$I_{k-1} = I_{i-1}$ and $I_{k+1} = I_{i+1}$ results in the design parameter $C_k = (C_i R_p)/R_X$. Similarly, the design parameter for the series inductor branch is $C_k = L_j/(R_p R_X)$, which is deduced from mapping the circuit variables $I_k = I_j$, $I_{k-1} = V_{j-1}/R_p$ and $I_{k+1} = V_{j+1}/R_p$. Since after the transformation, all variables are related to R_X, the adjustment of R_X will tune the corner frequency of the filters.

The shunt inductor and the series capacitor can be treated in the same way. For ease of reference, all single passive element syntheses are summarized and listed in Table 3.1.

3.3.4 Simulation of Single Passive Element with Source or Load Resistor

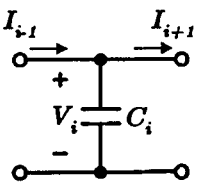
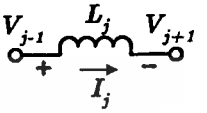
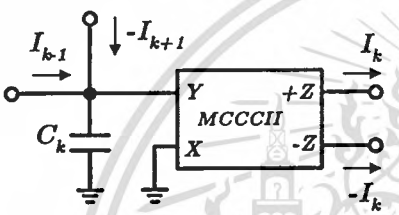
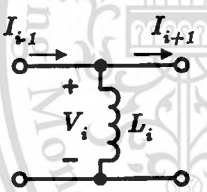
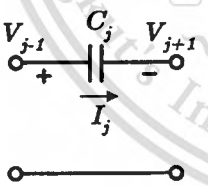
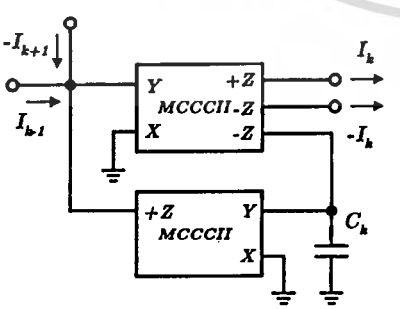
A shunt capacitor branch and a series inductor branch with source resistor are shown in Figs. 3.9(a) and 3.9(b), respectively. Their voltage and current relations in form of current transfer functions can be shown as

$$\frac{V_i}{R_S} = \frac{1}{sC_iR_S+1}(I_{IN} - I_{i+1}), \tag{3.17a}$$

$$I_j = \frac{1}{sL_j/R_S+1}\left(I_{IN} - \frac{V_{j+1}}{R_S}\right). \tag{3.17b}$$

Both equations have a characteristic of the lossy integrator or the first-order filter.

Table 3.1 Single passive element syntheses.

Equivalent elements	Voltage-Current relations
	$\frac{V_i}{R_p} = \frac{1}{sC_iR_p}(I_{i-1} - I_{i+1})$
	$I_j = \frac{R_p}{sL_j}\left(\frac{V_{j-1}}{R_p} - \frac{V_{j+1}}{R_p}\right)$
	$I_k = \frac{1}{sC_kR_X}(I_{k-1} - I_{k+1})$ $C_k = (C_iR_p)/R_X$ for shunt C $C_k = L_j/(R_pR_X)$ for series L
	$\frac{V_i}{R_p} = \frac{sL_i}{R_p}(I_{i-1} - I_{i+1})$
	$I_j = sC_jR_p\left(\frac{V_{j-1}}{R_p} - \frac{V_{j+1}}{R_p}\right)$
	$I_k = sC_kR_X(I_{k-1} - I_{k+1})$ $C_k = L_i/(R_pR_X)$ for shunt L $C_k = (C_jR_p)/R_X$ for series C

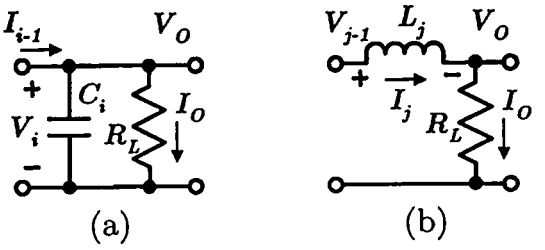


Figure 3.10 Single passive element with load resistor (a) shunt C (b) series L

Therefore, an equivalent MCCCII circuit in Fig. 3.9(c), which has the current transfer function of

$$I_k = \frac{1}{sC_kR_X + 1}(I_{k-1} - I_{k+1}), \tag{3.18}$$

can be used to realize those functions. Notice that similar current transfer equations as in the single passive element can be obtained when choosing $R_S = R_p$. By mapping the MCCCII equivalent circuit to the passive branch elements, the design parameter $C_k = (C_iR_S)/R_X$ for shunt capacitor and $C_k = L_j/(R_SR_X)$ for series inductor are acquired. Note that it is also possible to realize these functions using an additional MCCCII connected as a resistor together with the circuits in Chapter 3.3.3 [25, 26], but this will unnecessarily require some extra MCCCIIs.

For single passive elements with *load* resistor in Fig. 3.10, their current transfer functions can be found as

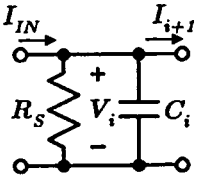
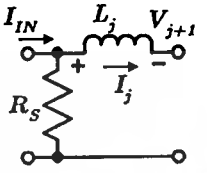
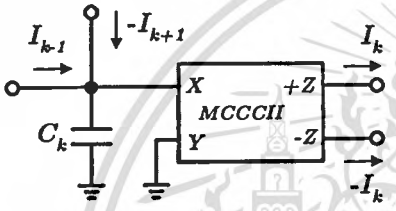
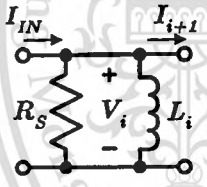
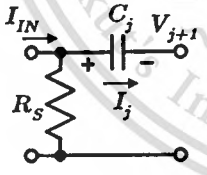
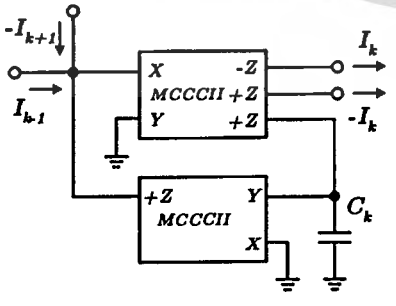
$$\frac{V_i}{R_L} = \frac{1}{sC_iR_L + 1}I_{i-1}, \tag{3.19a}$$

$$I_j = \frac{1}{sL_j/R_L + 1}\frac{V_{j-1}}{R_L}. \tag{3.19b}$$

These show similar response to the single passive elements with *source* resistor. Therefore, the equivalent MCCCII circuit remains unchanged, so does the design parameter C_k for $R_L = R_S$. This is also true for the rest of passive elements with either *source* or *load* resistor. Filter designs in Chapter 3.4 will clearly illustrate their usages in actual applications.

All single passive element syntheses with a source or load resistor are summarized in Table 3.2. By comparing the circuits in Table 3.1 and Table 3.2, the single passive elements with and without *source/load* resistor have nearly identical equivalent MCCCII circuits, except for a few different port arrangements of

Table 3.2 Single passive element syntheses with source or load resistor.

Equivalent elements	Voltage-Current relations
	$\frac{V_i}{R_S} = \frac{1}{sC_iR_S+1}(I_{IN} - I_{i+1})$
	$I_j = \frac{1}{s\frac{L_j}{R_S}+1}\left(I_{IN} - \frac{V_{j+1}}{R_S}\right)$
	$I_k = \frac{1}{sC_kR_X+1}(I_{k-1} - I_{k+1})$ $C_k = (C_iR_S)/R_X$ for shunt C $C_k = L_j/(R_SR_X)$ for series L
	$\frac{V_i}{R_S} = \frac{s\frac{L_i}{R_S}}{s\frac{L_i}{R_S}+1}(I_{IN} - I_{i+1})$
	$I_j = \frac{sC_jR_S}{sC_jR_S+1}\left(I_{IN} - \frac{V_{j+1}}{R_S}\right)$
	$I_k = \frac{sC_kR_X}{sC_kR_X+1}(I_{k-1} - I_{k+1})$ $C_k = L_i/(R_SR_X)$ for shunt L $C_k = (C_jR_S)/R_X$ for series C

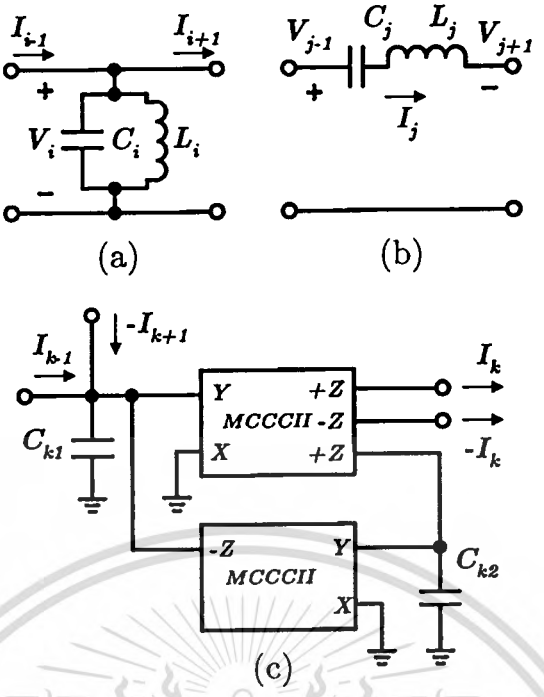


Figure 3.11 Double passive element (a) shunt parallel LC (b) series series LC (c) equivalent MCCCII structure

MCCCIIs. This is due to the flexibility of the multi-output structure and the utilization of the intrinsic resistance R_X to directly simulate the *source/load* resistor.

3.3.5 Simulation of Double Passive Elements

Two basic double passive element frames: a shunt parallel inductor-capacitor branch and a series series inductor-capacitor branch, are shown in Figs. 3.11(a) and 3.11(b), respectively. With all voltage signals transformed into their current counterparts by a scaling resistance R_p, their voltage and current relations in form of current transfer functions can be shown as

$$\frac{V_i}{R_p} = \frac{s\frac{L_i}{R_p}}{s^2 C_i R_p \frac{L_i}{R_p} + 1}\left(I_{i-1} - I_{i+1}\right), \tag{3.20a}$$

$$I_j = \frac{sC_j R_p}{s^2 C_j R_p \frac{L_j}{R_p} + 1}\left(\frac{V_{j-1}}{R_p} - \frac{V_{j+1}}{R_p}\right). \tag{3.20b}$$

An equivalent MCCCII circuit that can represent these functions is shown in

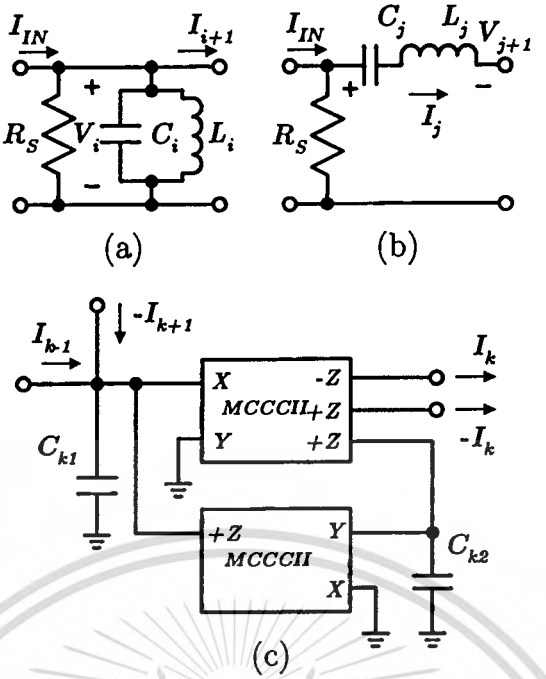


Figure 3.12 Double passive element with source resistor (a) shunt parallel LC (b) series series LC (c) equivalent MCCCII structure

Fig. 3.11(c) and has the current transfer function of

$$I_k = \frac{sC_{k2}R_X}{s^2C_{k1}C_{k2}R_X^2+1}(I_{k-1}-I_{k+1}). \tag{3.21}$$

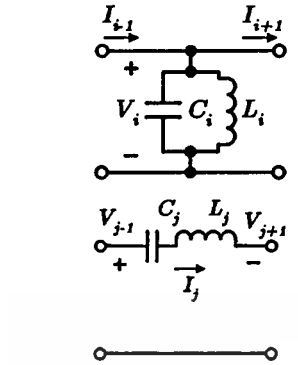
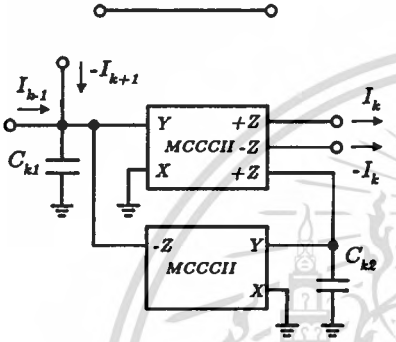
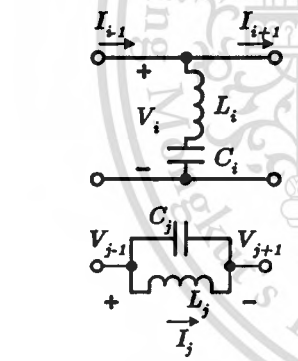
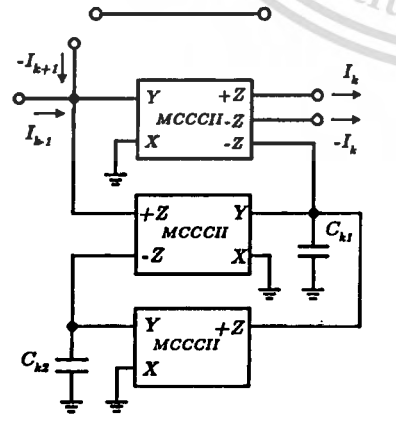
Mapping the equivalent MCCCII circuit to the double passive LC elements results in the design parameter $C_{k1} = (C_iR_p)/R_X$ and $C_{k2} = L_i/(R_pR_X)$ for shunt parallel LC branch and $C_{k1} = L_j/(R_pR_X)$ and $C_{k2} = (C_jR_p)/R_X$ for series series LC branch.

The shunt series inductor-capacitor and the series parallel inductor-capacitor can be treated in the same way, and all double passive element syntheses are summarized and listed in Table 3.3.

3.3.6 Simulation of Double Passive Elements with Source or Load Resistor

A shunt parallel capacitor branch and a series series inductor branch with source resistor are shown in Figs. 3.12(a) and 3.12(b), respectively. Their voltage and current relations in form of current transfer functions can be shown as

Table 3.3 Double passive element syntheses.

Equivalent elements	Voltage-Current relations
	$\frac{V_i}{R_p} = \frac{s\frac{L_i}{R_p}}{s^2C_iL_i+1}(I_{i-1}-I_{i+1})$ $I_j = \frac{sC_jR_p}{s^2C_jL_j+1}\left(\frac{V_{j-1}}{R_p}-\frac{V_{j+1}}{R_p}\right)$
	$I_k = \frac{sC_{k2}R_X}{s^2C_{k1}C_{k2}R_X^2+1}(I_{k-1}-I_{k+1})$ $C_{k1} = (C_iR_p)/R_X$ $C_{k2} = L_i/(R_pR_X)$ for shunt parallel LC $C_{k1} = L_j/(R_pR_X)$ $C_{k2} = (C_jR_p)/R_X$ for series series LC
	$\frac{V_i}{R_p} = \frac{s^2C_iL_i+1}{sC_iR_p}(I_{i-1}-I_{i+1})$ $I_j = \frac{s^2C_jL_j+1}{s\frac{L_j}{R_p}}\left(\frac{V_{j-1}}{R_p}-\frac{V_{j+1}}{R_p}\right)$
	$I_k = \frac{s^2C_{k1}C_{k2}R_X^2+1}{sC_{k2}R_X}(I_{k-1}-I_{k+1})$ $C_{k1} = L_i/(R_pR_X)$ $C_{k2} = (C_iR_p)/R_X$ for shunt series LC $C_{k1} = (C_jR_p)/R_X$ $C_{k2} = L_j/(R_pR_X)$ for series parallel LC

$$\frac{V_i}{R_S} = \frac{s\frac{L_i}{R_S}}{s^2 C_i R_S \frac{L_i}{R_S} + s\frac{L_i}{R_S} + 1}(I_{IN} - I_{i+1}), \tag{3.22a}$$

$$I_j = \frac{sC_j R_S}{s^2 C_j R_S \frac{L_j}{R_S} + sC_j R_S + 1}\left(I_{IN} - \frac{V_{j+1}}{R_S}\right). \tag{3.22b}$$

Then an equivalent MCCCII circuit in Fig. 3.12(c), which has the current transfer function of

$$I_k = \frac{sC_{k2}R_X}{s^2 C_{k1}C_{k2}R_X^2 + sC_{k2}R_X + 1}(I_{k-1} - I_{k+1}), \tag{3.23}$$

can be used to realize those functions. Again, similar current transfer equations as in the double passive elements can be obtained when choosing $R_S = R_p$. By mapping the MCCCII equivalent circuit to the passive branch elements, the design parameter $C_{k1} = (C_i R_S)/R_X$ and $C_{k2} = L_i/(R_S R_X)$ for shunt parallel LC branch and $C_{k1} = L_j/(R_S R_X)$ and $C_{k2} = (C_j R_S)/R_X$ for series series LC branch are obtained.

It can be shown that double passive elements with a *load* resistor also share the same structures. All double passive element syntheses with a source or load resistor are summarized in Table 3.4, and the similarity of the double passive elements with and without *source/load* resistor, except for a few different port arrangements of MCCCIIs, can also be noticed.

3.4 Filters Design and Simulation Results

Passive filter synthesis has been well-developed for several decades. A prototype passive RLC filter can be obtained either by using design table [15–18] or using a computer software. The performances of the active filters designed with the component partitioning technique were examined through HSPICE circuit simulator using AMIS 0.5-μm level 49 CMOS model. For the MCCCII circuit in Fig. 3.3, the aspect ratio of all transistors are listed in Table 3.5. The nominal bias current I_B was set to 50 μA under the supply voltage of $V_{sup} = \pm 2.0$ V. The simulated open-loop transconductance gain (g_m) and –3-dB bandwidth are 0.53 mA/V and 183 MHz, respectively, when using the dual output MCCCII as a transconductance cell.

Table 3.4 Double passive elements syntheses with source or load resistor.

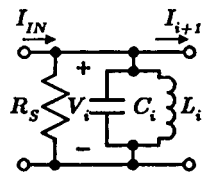
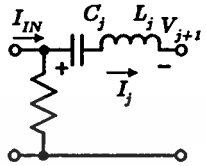
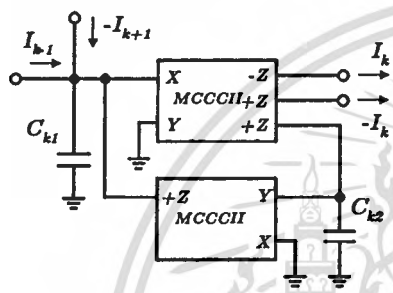
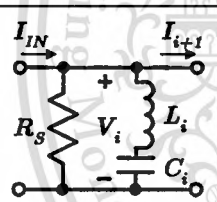
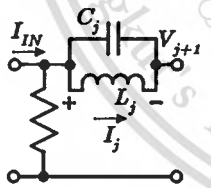
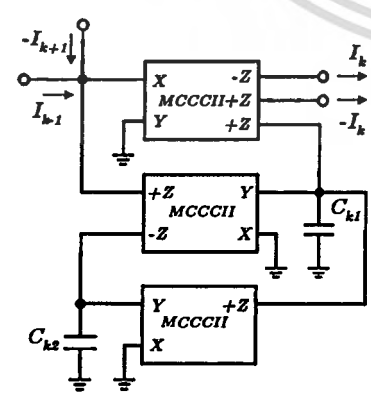
Equivalent elements	Voltage-Current relations
	$\frac{V_i}{R_S} = \frac{s\frac{L_i}{R_S}}{s^2C_iL_i + s\frac{L_i}{R_S} + 1}(I_{IN} - I_{i+1})$
	$I_j = \frac{sC_jR_S}{s^2C_jL_j + sC_jR_S + 1}\left(I_{IN} - \frac{V_{j+1}}{R_S}\right)$
	$I_k = \frac{sC_{k2}R_X \cdot (I_{k-1} - I_{k+1})}{s^2C_{k1}C_{k2}R_X^2 + sC_{k2}R_X + 1}$ $C_{k1} = (C_iR_S)/R_X$ $C_{k2} = L_i/(R_SR_X)$ for shunt parallel LC $C_{k1} = L_j/(R_SR_X)$ $C_{k2} = (C_jR_S)/R_X$ for series series LC
	$\frac{V_i}{R_S} = \frac{s^2C_iL_i + 1}{s^2C_iL_i + sC_iR_S + 1}(I_{IN} - I_{i+1})$
	$I_j = \frac{s^2C_jL_j + 1}{s^2C_jL_j + s\frac{L_j}{R_S} + 1}\left(I_{IN} - \frac{V_{j+1}}{R_S}\right)$
	$I_k = \frac{(s^2C_{k1}C_{k2}R_X^2 + 1) \cdot (I_{k-1} - I_{k+1})}{s^2C_{k1}C_{k2}R_X^2 + sC_{k2}R_X + 1}$ $C_{k1} = L_i/(R_SR_X)$ $C_{k2} = (C_iR_S)/R_X$ for shunt series LC $C_{k1} = (C_jR_S)/R_X$ $C_{k2} = L_j/(R_SR_X)$ for series parallel LC

Table 3.5 Transistor dimensions of the MCCCII circuit.

Transistors	W/L	Transistors	W/L
M_1, M_2	5/0.5	M_3, M_4	18.5/0.5
M_{B1}, M_{B2}	90/2	M_{B3}, M_{B4}	90/0.5
M_{B5}, M_{B6}	30/2	M_{B7}, M_{B8}	30/0.5
M_P	60/1	M_{P-cas}	100/1
M_N	60/1	M_{N-cas}	50/1

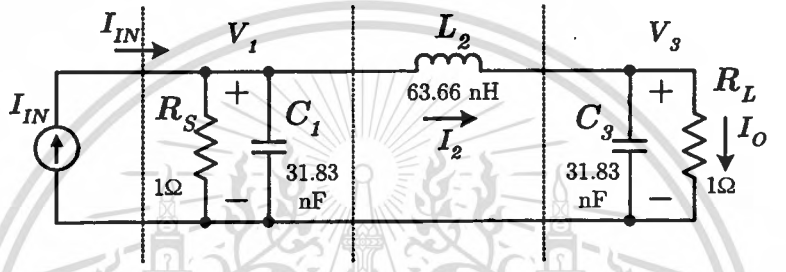


Figure 3.13 Prototype 3^{rd}-order Butterworth low-pass RLC ladder filter.

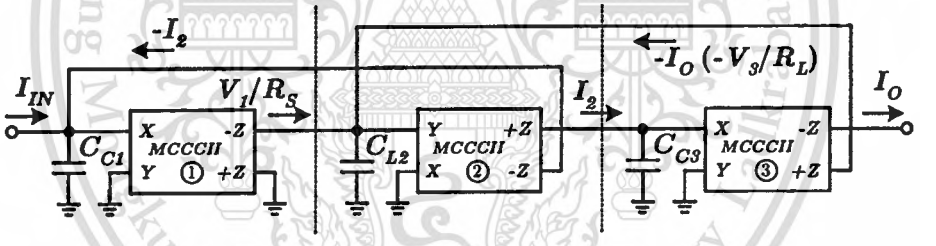


Figure 3.14 MCCCIIs-based current-mode 3^{rd}-order Butterworth low-pass filter.

3.4.1 Third-order Butterworth Low-Pass Filter

A third-order Butterworth low-pass ladder filter is adopted as the first design example. A prototype passive filter is shown in Fig. 3.13 and component values for 5 MHz cutoff frequency are also listed in the figure. By using the component partitioning technique, the filter can be easily divided into three sections of branch elements: the first shunt capacitor with the source resistor, the second series inductor and the third shunt capacitor with the load resistor. Refer to Table 3.2 for implementing the shunt capacitor with source and load resistors and Table 3.1 for the series inductor. The final equivalent MCCCII-based circuit

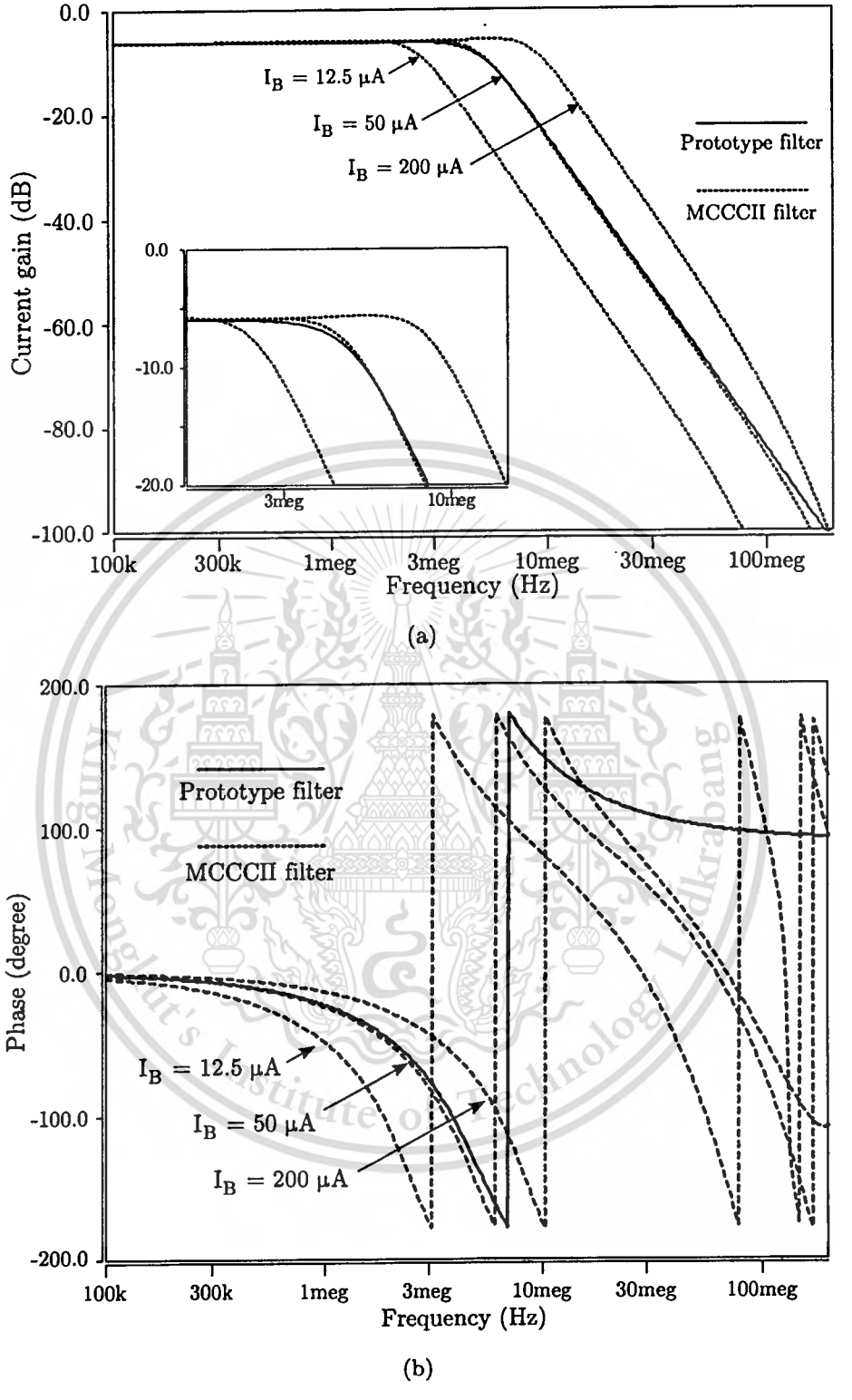


Figure 3.15 Simulated frequency response of the MCCCIIs-based current-mode 3^{rd}-order Butterworth low-pass filter. (a) Gain response. (b) Phase response.

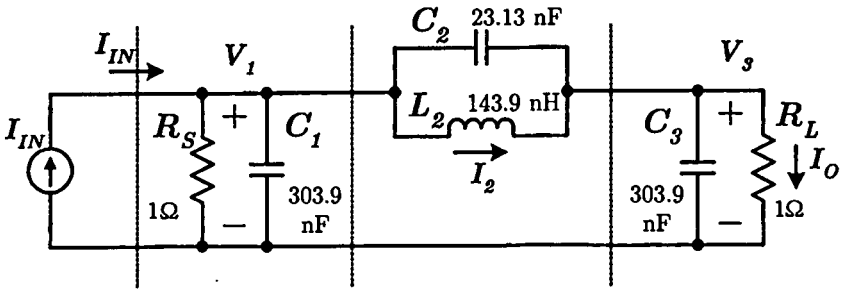


Figure 3.16 Prototype 3^{rd}-order elliptic low-pass RLC ladder filter.

is shown in Fig. 3.14. Obviously, only three MCCCIIs and three grounded capacitors are needed for realizing the third-order filter. It can be concluded that merely n MCCCIIs and n capacitors are required for the n^{th}-order all-pole low-pass filters implementation with no requirement of external resistors. Therefore, this structure delivers a truly minimum requirement of active and passive components. However, this does not mean a minimum number of transistors since it also depends on the implementation of the active building block.

Refer to Table 3.1 and Table 3.2 for finding the design parameters C_k of the MCCCII-based subsection. By choosing $R_p = R_S = 1\ \Omega$ for simplicity and MCCCIIs' $R_X(1/g_m)$ of 1,887 Ω, the capacitor values can be found as $C_{C1} = C_{C3} = 17.506$ pF and $C_{L2} = 35.013$ pF. The simulated frequency responses of the designed circuit and the prototype RLC filter are shown together in Fig. 3.15. The tuning ability is performed by varying bias current to 12.5 μA and 200 μA. The simulated corner frequencies are 2.65 MHz, 5.09 MHz and 9.34 MHz, which are corresponding to the calculated frequencies of 2.5 MHz, 5 MHz and 10 MHz, respectively. The frequency accuracy is within about 6%. The proposed structure shows almost identical characteristic with the passive prototype filter before the signals begin to deviate especially the phase response at frequency beyond 100 MHz due to the frequency limitation of the MCCCIIs.

3.4.2 Third-order Elliptic Low-Pass Filter

A third-order elliptic low-pass filter is shown in Fig. 3.16. The prototype filter has been designed to have the corner frequency of 1 MHz with 1 dB pass band ripple and 40 dB stop band attenuation. All component values are already included in the figure. The filter that has transmission zero like this example is also possible to be separated into three sections. By using the circuits in Table 3.3 for implementing the middle parallel LC elements while the first and the last blocks are, again, adopted from Table 3.2, the complete equivalent filter using only MCCCIIs and grounded capacitors is shown in Fig. 3.17. For $R_p = R_S = 1\ \Omega$ and

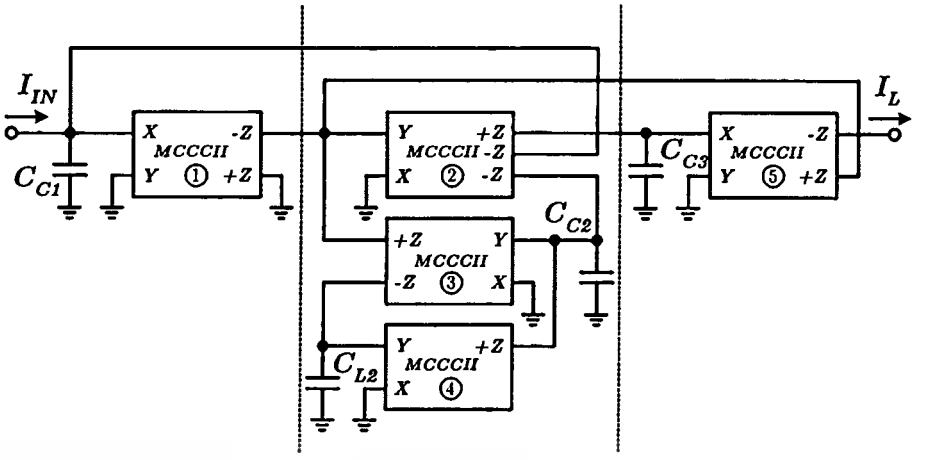


Figure 3.17 MCCCIIs and only grounded capacitor current-mode 3^{rd}-order elliptic low-pass filter.

$R_X = 1,887\Omega$, the design parameters can be found as $C_{C1} = C_{C3} = 161.067$ pF, $C_{C2} = 12.259$ pF and $C_{L2} = 76.267$ pF. The simulated frequency responses are depicted in Fig. 3.18. The large variation of MCCCIIs-filter in high frequencies is noticed. This comes from the frequency restriction of the multi-output current controlled conveyor especially the second current conveyor with three output ports, as predicted in Chapter 3.2.5. Note that the notch position is not as deep as in the prototype filter due to the limitation of quality factor of simulated LC components.

Because this proposed technique derives each element with one-by-one replacement concept, it is possible to separate the floating capacitor C_2 from the passive filter in Fig. 3.16 and then realize the canonical MCCCII-based all-pole low-pass ladder filter first. After that, adding the scaled capacitor C_2 to the synthesized circuit at the corresponding node will result in a circuit shown in Fig. 3.19, in which all design parameters are exactly the same value as of the grounded capacitor filter. The simulated frequency responses of the floating capacitor MCCCIIs-based filter is given in Fig. 3.20. It is clearly seen that a better performance than the previous circuit using only grounded capacitors is achieved. It is worth noting that the peaking magnitude at the corner frequency due to phase lag is also smaller by 0.2 dB comparing to Fig. 3.18. This is because the use of low frequency three output ports MCCCII is avoided. Furthermore, this structure has the filter capacitances presented at all nodes and is suitable for high frequency operation. Therefore, this solution is preferable for realizing the elliptic filters when the floating capacitor is permitted [20, 62].

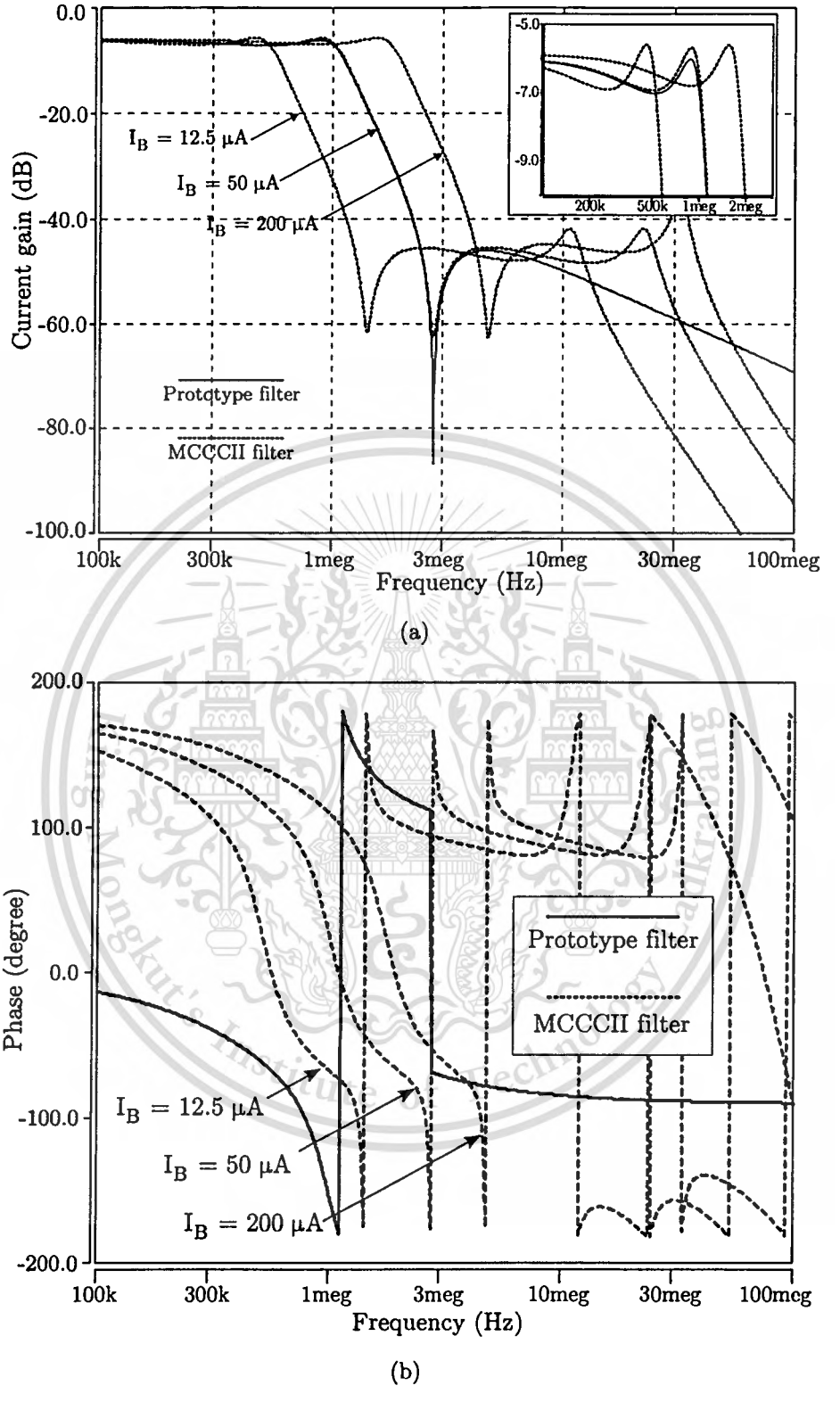


Figure 3.18 Simulated frequency response of the grounded capacitor elliptic low-pass filter. (a) Gain response. (b) Phase response.

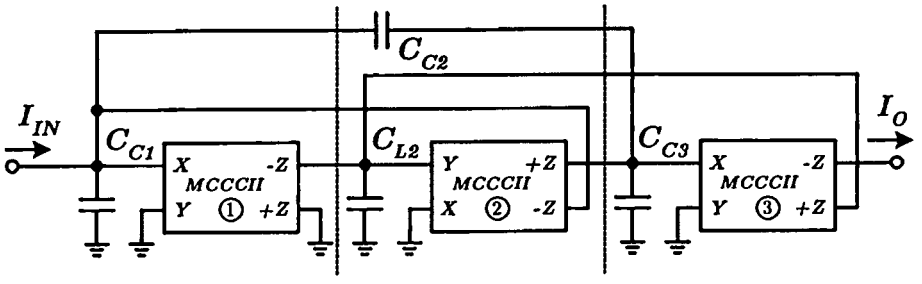


Figure 3.19 MCCCIIs and floating capacitor current-mode 3^{rd}-order elliptic low-pass filter.

3.4.3 Sixth-order Chebyshev Band-Pass Filter

The last example is a sixth-order Chebyshev band-pass filter that is shown in Fig. 3.21. The prototype filter has been designed to have 1 MHz center frequency f_c and 1 MHz bandwidth, so the quality factor (Q) defined by f_c/BW of the filter is 1 and the highest individual Q of the transfer function is 2.424. All passive component values are already included in the figure. The band-pass filter can also be separated into three sections. The first shunt parallel LC branch with source resistor and the last shunt parallel LC branch with load resistor can be implemented with the same MCCCII-based circuit in Table 3.4, while the middle series series LC branch is listed in Table 3.3. Combining these three sections together results in the complete MCCCII-based band-pass filter as shown in Fig. 3.22, and the scaled capacitor values are $C_{C1} = C_{C3} = 87.026$ pF, $C_{L1} = C_{L3} = 81.779$ pF, $C_{C2} = 73.511$ pF and $C_{L2} = 96.778$ pF. The simulated frequency response of the filter is shown in Fig. 3.23. There is a noticeable peaking due to the Q-enhancement effect. However, since every separated section can be tuned electronically, incorporating a suitable Q-control circuit will help adjust the filter to the desired specification [20, 23].

3.5 Conclusions

An efficient implementation of the current-mode ladder filters at any order using the multi-output second-generation current controlled conveyors has been discussed. The design methodology is very simple and covers all types of precedent passive LC ladder filters. This technique requires the minimum number for both passive and active components. There are only n MCCCIIs needed for realizing the n^{th}-order all-pole filter and elliptic low-pass filter with an absence of the external resistor provided that floating capacitors are permitted. However, $2n - 1$ and

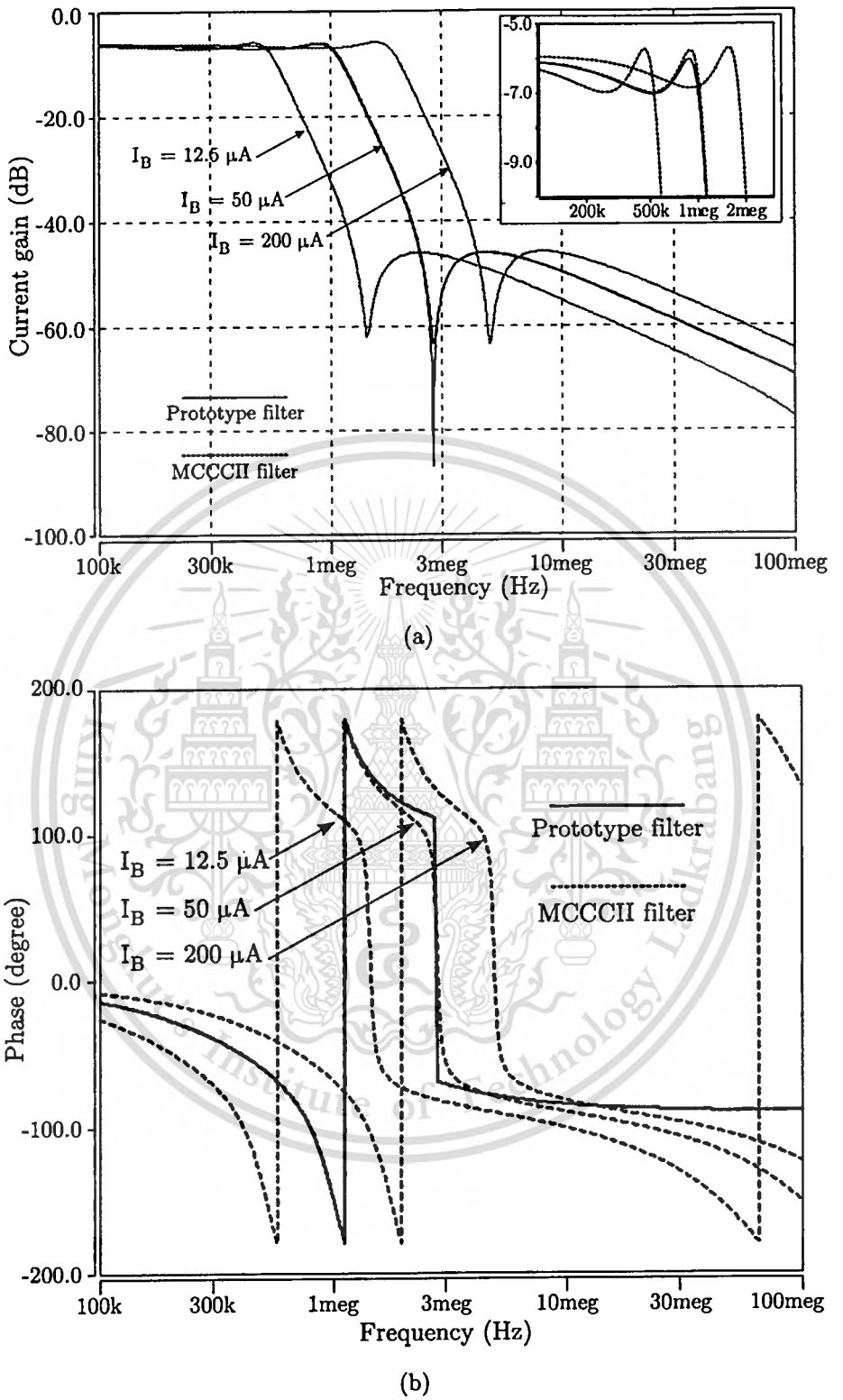


Figure 3.20 Simulated frequency response of the floating capacitor elliptic low-pass filter. (a) Gain response. (b) Phase response.

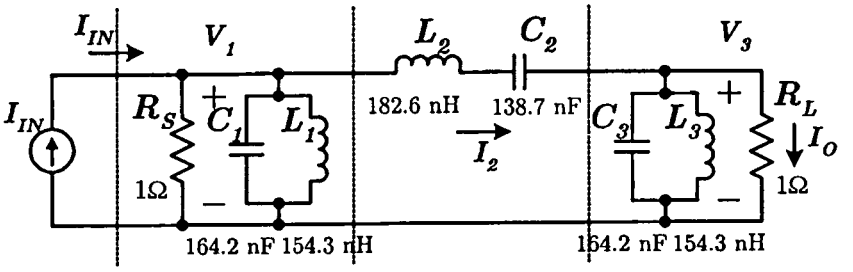


Figure 3.21 Prototype 6^{th}-order Chebyshev band-pass RLC ladder filter.

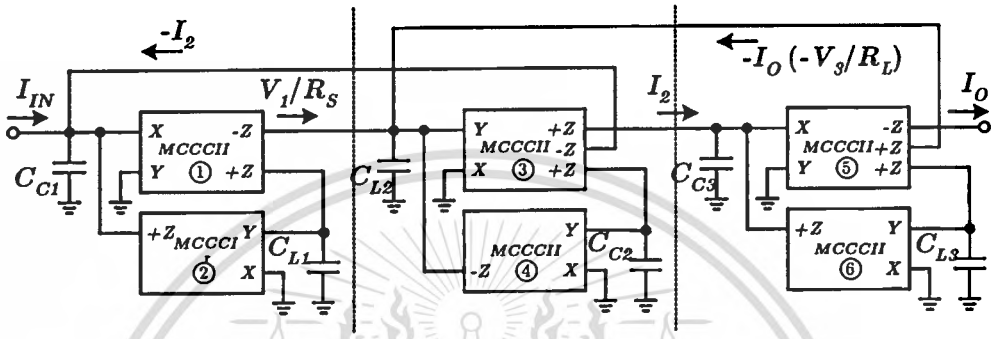


Figure 3.22 MCCCIIs and only grounded capacitor current-mode 6^{th}-order Chebyshev band-pass filter.

$2n-2$ MCCCIIs are required to achieve odd and even n^{th}-order elliptic filters, respectively, when implementing with only grounded capacitors.

The characteristic frequency of the filters can be made electronically tunable by incorporating the intrinsic impedance at port X of the MCCCIIs into filter design parameter. The value of this impedance can be controlled via the bias current of the circuit, however, with a limited linear operation range. The dynamic range optimization from [45] may be adopted to obtain the highest dynamic range under power dissipation constraints. In addition, the number of the output port of the MCCCIIs should be minimized in order to reduce the frequency and noise limitations.

Third-order Butterworth low-pass filter, third-order elliptic low-pass filter and sixth-order Chebyshev band-pass filter were chosen as design examples. HSPICE simulation results yield good agreement with the theoretical expectation.

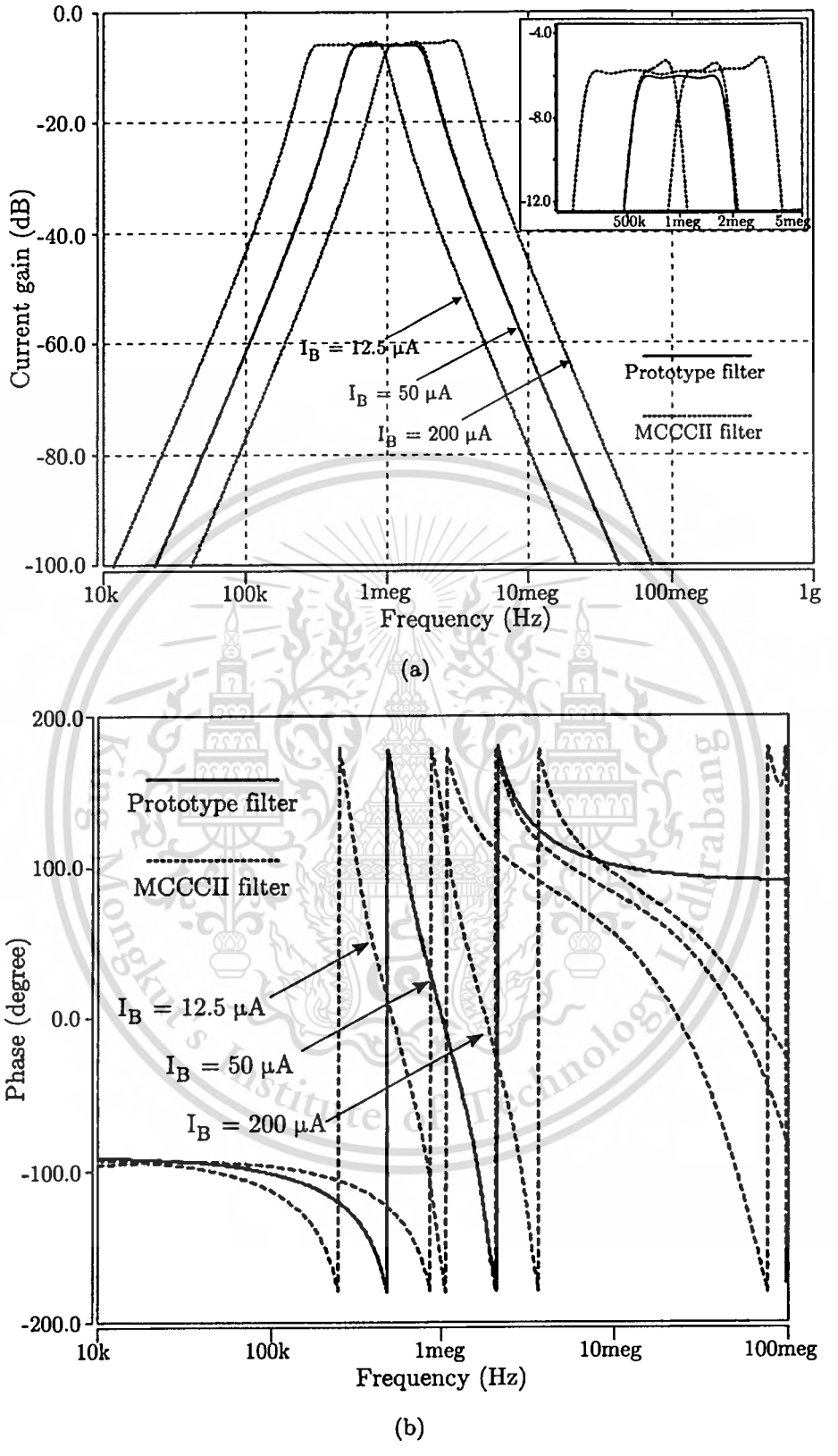


Figure 3.23 Simulated frequency response of the Chebyshev band-pass filter. (a) Gain response. (b) Phase response.

CHAPTER 4

HIGH-LINEARITY SWITCHED-RESISTOR TECHNIQUE

4.1 Introduction

Active-RC filters comprising operational amplifiers (opamps) and highly linear passive resistors and capacitors have superior linearity properties for base-band applications. One critical issue with these filters is the RC time-constant variation due to process uncertainty, temperature drift, and aging. In extreme conditions, a maximum variation of ±50% in the 3-dB cutoff frequency is typical in integrated filters. Although this problem can be overcome by making the RC time-constant tunable through a digital trimming weighted resistor or capacitor array [32, 33], it is only practical for coarse and low precision tuning. Fine tuning is possible using a linearized model behavior of a MOS transistor operating in triode region as a variable resistor [22, 34, 51], and its linearity can be improved by using a combination of passive resistors and current-steering MOS transistors [24]. However, this kind of tuning technique requires a gate-source on-voltage substantially larger than the input voltage swing in order to achieve adequate linearity and tuning range. As a result, a gate voltage bootstrapping circuit is usually required in low supply voltage environment, that may affect long term reliability of circuits due to gate oxide stress and breakdown [37, 38]. For a reliable design, all the terminal-to-terminal voltages of the MOS transistors used in the design should always be limited to the maximum supply voltage assigned by the employed process at any point of time during operation. This thus makes the MOS resistor tuning techniques impractical in modern deep-submicron CMOS processes.

For a low supply voltage operation, a more practical approach is to use a passive resistor that is switched on and off by a clock with tunable duty cycle. Several works employing this timing variable technique to adjust circuit time-constant or transfer function coefficients have been proposed [63–66], and its potential to overwhelm the low-voltage constraints was introduced in form of the switched-R-MOSFET-C (SRMC) filter [67]. Moreover, recent research work describing IC implementation and measurement results of the SRMC filter confirmed its high linearity performance at supply voltage as low as 0.6-V [68]. This is because such

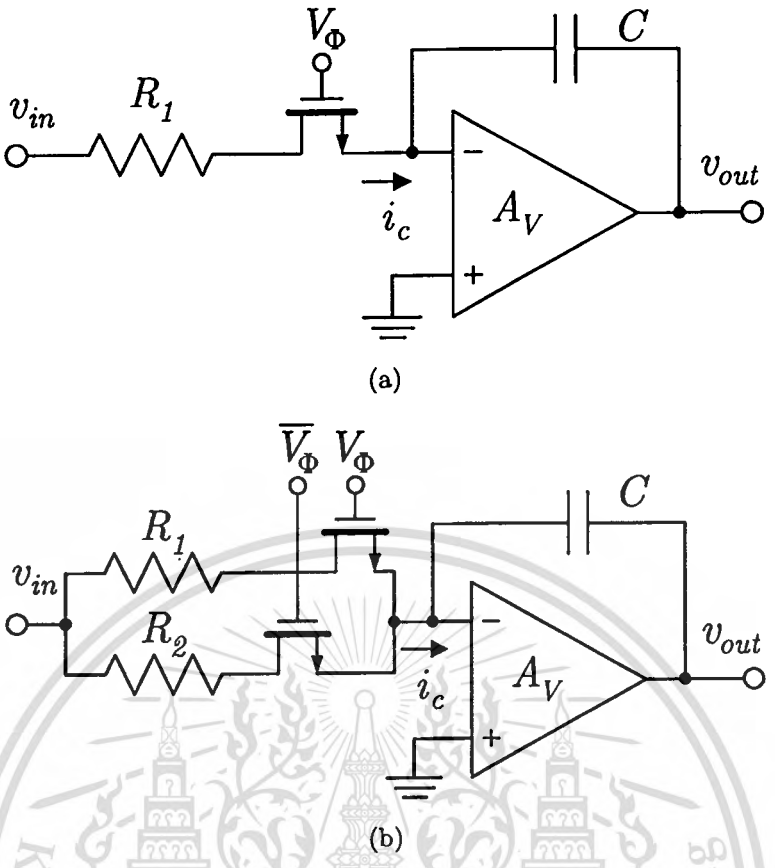


Figure 4.1 Switched-resistor integrators. (a) Switched-1R. (b) Switched-2R.

a tuning approach relies upon clock timing, so its performance is not compromised by a low supply voltage. In addition, a relatively large value of linear resistor in series with the switch handles most of the input signal swing. This thus keeps the actual voltage drop over the MOS switch down to the virtual ground, and its non-linearity contribution is minimized. However, the resulting switching operation in one set of the switched-resistor network, that is employed in the SRMC filter and its basic integrator cell is shown in Fig. 4.1(a), poses a stringent requirement on the slew rate of the opamp. The network employing two sets of switched-resistors as shown in Fig. 4.1(b) then has been developed and proved to have less sensitivity to slewing problems, so that the slew rate specification can be relaxed [69].

This chapter discusses a detailed analysis of the switched-resistor techniques through the operation of switched-resistor integrators and first-order filters based on one set (Switched-1R) and two sets (Switched-2R) of the switch and resistor combination. Their design parameters and slew rate induced distortion are studied, and since the switched-resistor networks are linear time-varying (LTV) circuits, their frequency translation and cyclostationary noise properties are also analyzed. Furthermore, experimental results extracted from breadboard prototype

of 100 kHz first-order filters and simulation results of 10 MHz fifth-order elliptic low-pass filters in standard 0.18-μm CMOS process operating with supply voltage at 1.5 V are given to verify the theoretical analysis and compare the performance between the Switched-1R and Switched-2R filters.

4.2 Operation Principle of Switched-Resistor Circuit

Fig. 4.1(a) shows a Switched-1R integrator, which has 2 phases of operations: tracking integration and holding. The MOS switch at the inverting input of the opamp is completely turned on and off by the controlling clock V_Φ. Alternatively, a Switched-2R integrator in Fig. 4.1(b) is controlled by non-overlapping clocks, V_Φ and $\overline{V_\Phi}$. Unlike the track and hold operation in the Switched-1R, there is always a signal current charging the capacitor, but the magnitude is dependent on which of the switched-resistor, R_1 or R_2, is conducted. In either case, the variation of the clock duty cycle effectively modulates the charging currents of the capacitors, which are in turn dependent on the input signal v_{in}. This thus makes the average resistance adjustable, so does the unity-gain frequency of the switched-resistor integrators.

4.2.1 Fundamental Characteristic Analysis

To simplify the description, first consider the operation of the Switched-2R integrator. Assume that the non-linear on-resistances of the MOS switches are much smaller than the linear passive resistors and the opamp has a very large gain, the charging current i_c can be written as

$$i_c(t) = \frac{v_{in}(t)}{R_1} \cdot p(t) + \frac{v_{in}(t)}{R_2} \cdot \overline{p}(t), \tag{4.1}$$

where the resistor value $R_2 > R_1$ is assigned and periodic waveforms of the non-overlapping clock functions toggling between 0 and 1 are

$$p(t) = m + \Phi(m,t), \tag{4.2a}$$
$$\overline{p}(t) = (1-m) - \Phi(m,t), \tag{4.2b}$$

where m and $(1-m)$ are duty cycle, which is defined as the ratio of on-time to clock period, of the clocks $V_\Phi(t)$ and $\overline{V_\Phi}(t)$, respectively. $\Phi(m,t)$ can be written

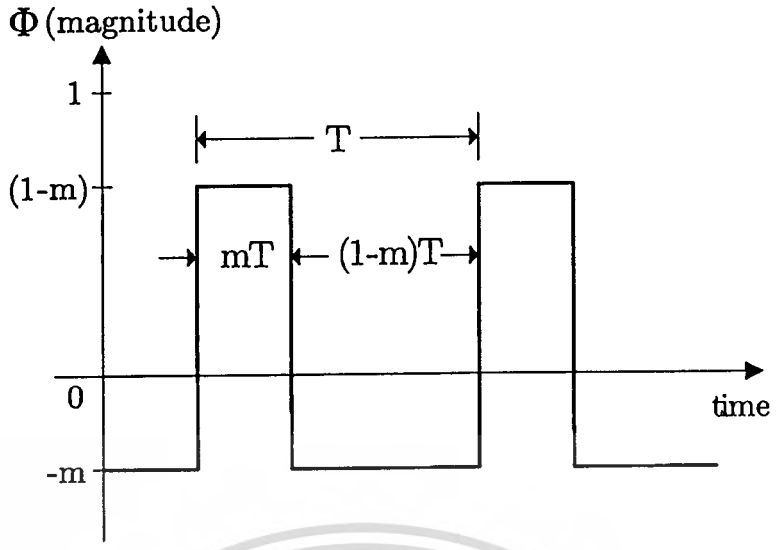


Figure 4.2 Wave form of square wave with varied duty cycle factor, $\Phi(m,t)$.

in the form of the Fourier expansion of a square wave signal with the duty cycle of m,

$$\Phi(m,t) = \sum_{n=1}^{\infty} \frac{2}{n\pi} \sin(mn\pi)\cos(n\omega_{clk}t - mn\pi), \tag{4.3}$$

where ω_{clk} is the clock radian frequency. A plot of $\Phi(m,t)$ is shown in Fig. 4.2 where T is the clock period and is equal to $2\pi/\omega_{clk}$. Notice that both timing and magnitude of the clock depend on the duty cycle parameter m. Total magnitude is always 1, but not the average, so the positive and negative extreme values do change (but not the peak-to-peak value, which is fixed). This fact will provide a useful insight into the operation of the switched-resistor networks as to be discussed later. Taking the integration of the charging current i_c results in the output voltage at

$$\begin{aligned} v_{o-2R,int}(t) &= -\left(\frac{m}{R_{1-2R}} + \frac{1-m}{R_{2-2R}}\right)\frac{1}{C}\int_0^t v_{in}(t)dt \\ &\quad -\left(\frac{1}{R_{1-2R}} - \frac{1}{R_{2-2R}}\right)\frac{1}{C}\int_0^t \Phi(m,t)v_{in}(t)dt. \end{aligned} \tag{4.4}$$

Note that (4.1) – (4.4) are also applicable to the Switched-1R integrator by simply setting the value of R_2 to infinite.

From (4.4), if only baseband characteristic is considered, the second term incorporating the clock function $\Phi(m,t)$ can be neglected. Note that this term

will be examined later when discuss the slew rate induced distortion and frequency translation characteristics of the switched-resistor networks. By considering the first component in (4.4) that represents the integrating function of the input signal, it is clearly seen that the time-constant and the unity-gain frequencies of the switched-resistor integrators in Fig. 4.1 are dependent on the duty cycle parameter m and can be written as

$$\omega_{u-1R}(m) = \frac{1}{R_{eq1R}C} = \frac{m}{R_{1-1R}C}, \tag{4.5a}$$

$$\omega_{u-2R}(m) = \frac{1}{R_{eq2R}C} = \left(\frac{m}{R_{1-2R}} + \frac{1-m}{R_{2-2R}}\right)\frac{1}{C}, \tag{4.5b}$$

where R_{eq1R} and R_{eq2R} are the equivalent tunable resistances of the Switched-1R and the Switched-2R integrators, respectively. The unity-gain frequency of the Switched-1R integrator can be theoretically tuned between 0 and $1/R_1C$ while that of the Switched-2R integrator is between $1/R_2C$ and $1/R_1C$. This implies that the Switched-2R arrangement exhibits a narrower frequency tuning range, but it offers higher tuning resolution for the same duty cycle steps.

The first-order switched-resistor filters having feedback resistors from the output to the input of the MOS switches are shown in Fig. 4.3. This configuration embeds the non-linear on-resistance of the MOS switches into a feedback loop, and thus its non-linear effect is negligibly small [24, 67–69]. In this case, the output voltage of the first-order Switched-2R filter can be given as

$$\begin{aligned} v_{o-2R,fil}(t) = &-\left(\frac{m}{R_{1-2R}} + \frac{1-m}{R_{2-2R}}\right)\frac{1}{C}\int_0^t \big(v_{o,fil}(t) + v_{in}(t)\big)dt \\ &-\left(\frac{1}{R_{1-2R}} - \frac{1}{R_{2-2R}}\right)\frac{1}{C}\int_0^t \Phi(m,t)\big(v_{o,fil}(t) + v_{in}(t)\big)dt. \end{aligned} \tag{4.6}$$

Again, when considering only the baseband frequency, the second term containing the clock function $\Phi(m,t)$ is omitted. By using (4.6), it can be shown that the 3-dB cutoff frequency of the first-order switched-resistor filter is identical to the unity-gain frequency of the corresponding integrator as given in (4.5).

It should be noted that mismatch between input resistor and feedback resistor may introduce a gain error and a frequency shift to the filters in term of these resistor values ratio (see Appendix A.1). However, since the resistor ratio in integrated circuit can be made very accurate within ±0.25% [70] or even better with improved area allocation strategies [71], this effect can be abandoned. Finite

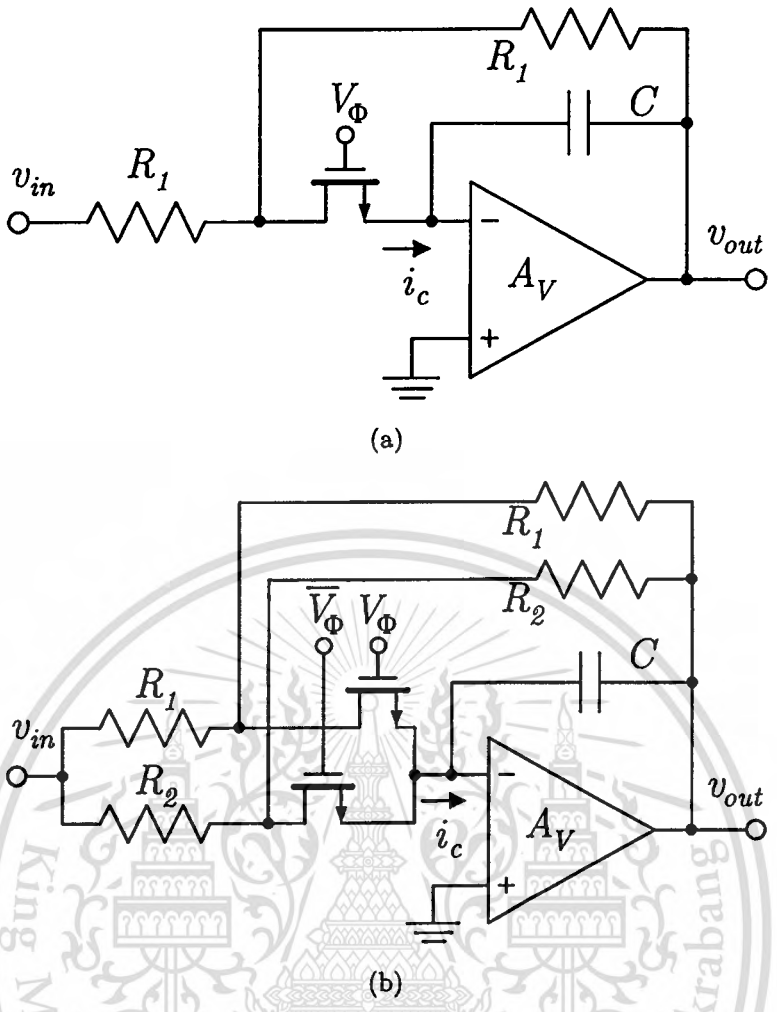


Figure 4.3 First-order switched-resistor filters. (a) Switched-1R. (b) Switched-2R.

on-resistance of the MOS switch is also a possible cause of frequency error (see Appendix A.2). Fortunately, by incorporating a tuning circuit with an accurate reference time period, the negative feedback loop will adjust the duty cycle of the controlling clock to compensate any fault and the filter time-constant will be set precisely [67, 68].

4.2.2 Design Parameters

The choice of resistor value for R_1 and R_2 in a Switched-2R integrator is important since there is a trade-off between the tuning range and the maximum slope of the output, which in turn determines the distortion performance [69]. From (4.5b), if R_2 is selected at x times larger than R_1, the unity-gain frequency of the Switched-2R integrator can be determined in the term of R_1 as

$$\omega_{u-2R}(m) = \frac{1+(x-1)m}{xR_{1-2R}C}. \tag{4.7}$$

Assume that the nominal frequency has been assigned at the duty cycle of 50% or $m = 0.5$, the tuning range $\triangle f$ of the Switched-2R integrator derived from (4.7) is

$$\triangle f_{-2R}(\pm\%) = \frac{(x-1)(m_{max/min}-0.5)}{1+(x-1)0.5} \times 100\%, \tag{4.8}$$

where $m_{max/min}$ is either the maximum or the minimum duty cycle of the clock signal. On the other hand, the unity-gain frequency of the Switched-1R integrator is directly proportional to the duty cycle as indicated in (4.5a), thus the tuning range will be directly dependent on m as

$$\triangle f_{-1R}(\pm\%) = \frac{m_{max/min}-0.5}{0.5} \times 100\%. \tag{4.9}$$

The tuning range ratio between these two switched circuits is then determined by

$$\frac{\triangle f_{-1R}}{\triangle f_{-2R}} = \frac{x+1}{x-1}. \tag{4.10}$$

Ideally, the duty cycle can be tuned from 0%–100% for $m = 0.0$ to 1.0 but, in practice, the range should be limited because of problems relating to implementing very small or very high duty cycle clocks [67, 68].

For the same unity-gain frequency $\omega_{u-1R} = \omega_{u-2R}$ at $m = 0.5$ and the same capacitor value C, the relation between the resistor values of the Switched-1R and Switched-2R integrators is obtained by using (4.5a) and (4.7) and this is given as

$$R_{1-1R} = \frac{x}{x+1}R_{1-2R} = \frac{1}{x+1}R_{2-2R}. \tag{4.11}$$

From (4.8) – (4.11), since $x > 1$ ($R_{2-2R} > R_{1-2R}$), it can be concluded that the tuning range of the Switched-2R integrator is always smaller than that of the Switched-1R integrator while the resistor value R_{1-2R} and R_{2-2R} is always larger than R_{1-1R}, when both circuits are designed for the same ω_u at $m = 0.5$. Note that this is also true for the first-order switched-resistor filters because they share the same relationship for the 3-dB cutoff frequencies.

4.3 Slew Rate Induced Distortion

Since passive resistors and capacitors can be very linear, the main causes of distortion in the switched-resistor circuits are the non-linear resistance of the MOS switches and non-idealities in the opamps. The MOS switches are in series with linear resistors, which take most of the input voltage over them, provided that the on-resistance of MOS switches is chosen much smaller than the (linear) resistor value. On the contrary, the opamp may introduce significant distortion, especially if a fast opamp response to large input signal changes is needed, and slew limitation takes place. During slewing, the feedback loop is effectively broken for some time, and it is instructive to predict when slewing occurs, so that its effect can be minimized [69]. To derive the slew rate requirements for the opamps, the largest slope of the output that can occur has to be found.

4.3.1 Maximum Slope Derivation

The rate of change of an output voltage signal is shown in form of a slope function, $S(t)$, which can be derived by taking the derivative of v_o, $dv_o(t)/dt$. In the case of integrators, the slope functions can be shown in terms of the unity-gain frequency and the RC time-constant based on (4.4), (4.5) and (4.11) as follows

$$S_{-1R}(t) = -\left[\omega_{u-1R}(m) + \frac{\Phi(m,t)}{R_{1-1R}C}\right] v_{in}(t), \tag{4.12a}$$

$$\begin{aligned} S_{-2R}(t) &= -\left[\omega_{u-2R}(m) + \left(\frac{1}{R_{1-2R}} - \frac{1}{R_{2-2R}}\right)\frac{\Phi(m,t)}{C}\right] v_{in}(t) \\ &= -\left[\omega_{u-2R}(m) + \left(\frac{x-1}{x+1}\right)\frac{\Phi(m,t)}{R_{1-1R}C}\right] v_{in}(t). \end{aligned} \tag{4.12b}$$

It is clear that the second term in the square brackets containing $\Phi(m,t)$ determines the output slope limits of the Switched-1R and Switched-2R circuits. For the same unity-gain frequency ω_u and $x > 1$, (4.12) suggests that the Switched-1R integrator always produces higher output signal slope magnitude than that of the Switched-2R counterpart, i.e. $|S_{-1R}| > |S_{-2R}|$, since $(x-1)/(x+1) < 1$ for $x > 1$.

The point with the maximum slope, S_{max}, can be determined by solving $dS(t)/dt = 0$ to find t_{max} and then substitute this value into (4.12) to estimate the maximum slope value. For a sinusoidal input signal of $v_{in}(t) = V_p \sin(\omega_{in} t)$, the maximum *input current* charging the capacitor occurs periodically at the peak of the input signal or at $t_{max} = ((2k-1)/\omega_{in})(\pi/2)$ for $k = 1, 2, 3, \ldots$. These points are correspondent to zero crossing at the *output voltage* of the integrator.

The maximum slope equations can be further simplified by making an assumption that they will reach the largest value when the input signal and $\Phi(m,t)$ are at their peaks at the same time. Under this condition, the maximum slope can be obtained by substituting the input signal $v_{in}(t)$ with the peak voltage V_p, the function $\Phi(m,t)$ with its highest magnitude $(1-m)$ (see Fig. 4.2) and the unity-gain frequency from (4.5), and this gives

$$\begin{aligned} S_{max-1R} &\cong V_p\left[\frac{m}{R_{1-1R}C}+\frac{1-m}{R_{1-1R}C}\right] \\ &= \frac{V_p}{R_{1-1R}C}, \end{aligned} \tag{4.13a}$$

$$\begin{aligned} S_{max-2R} &\cong V_p\left[\left(\frac{m}{R_{1-2R}}+\frac{1-m}{R_{2-2R}}\right)\frac{1}{C}+\left(\frac{1}{R_{1-2R}}-\frac{1}{R_{2-2R}}\right)\frac{1-m}{C}\right] \\ &= \frac{V_p}{R_{1-2R}C}. \end{aligned} \tag{4.13b}$$

Interestingly, from (4.13), the output maximum slopes are independent on the duty cycle m, the input signal frequency ω_{in}, and the clock frequency ω_{clk}. They are determined only by the physical RC product and the input signal amplitude. The output maximum slope ratio between the Switched-1R and Switched-2R integrators then becomes the inverse ratio of their resistor R_1 values. According to the relation in (4.11), the maximum slope ratio can be simply given by

$$\frac{S_{max-1R}}{S_{max-2R}} = \frac{R_{1-2R}}{R_{1-1R}} = \frac{x+1}{x}. \tag{4.14}$$

For the integrators that have the nominal unity-gain frequency ω_u of $2\pi\cdot 10$ Mrad/s at $m = 0.5$ and the integrating capacitor of 3.183 pF, resistor $R_1 = 2.5$ kΩ is obtained for the Switched-1R integrator. By selecting the resistor ratio x at 2 in Switched-2R, R_1 and R_2 can be calculated, and takes the value of 3.75 kΩ and 7.5 kΩ, respectively. Calculation of S_{max} directly from (4.12) for the input signal with $V_p = 0.1$ V magnitude gives a constant maximum slope at 12.57 V/μs for the Switched-1R integrator and 8.37 V/μs for the Switched-2R integrator regardless of the parameters m, ω_{in}, and ω_{clk}. The ratio of the resulting maximum slopes is 1.5018, comparing to the slope ratio at 1.5 as obtained from (4.14) at $x = 2$.

A closed form of the maximum slope of the first-order switched-resistor filters however can not be found by solving an ordinary differential equation (4.6), so it is necessary to resort to numerical approximation. In contrary to the integrators, they are dependent on m, ω_{in}, and ω_{clk}. Fig. 4.4 shows the numerical plot of the maximum slope S_{max} in the first-order filters as a function of m and ω_{clk}, based

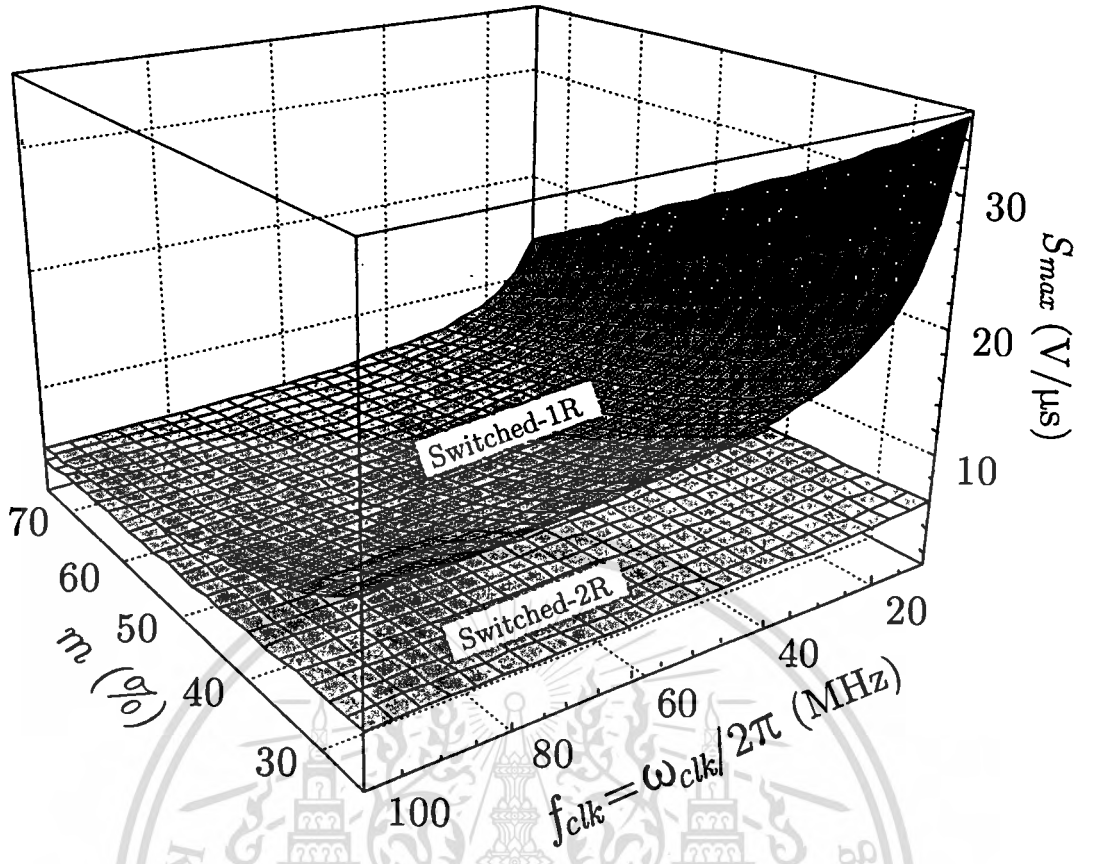


Figure 4.4 Maximum slope variation versus clock duty cycle and clock frequency in the first-order switched-resistor filters.

on the same component parameters as given before in case of the integrators, and ω_{in} at $2\pi \cdot 5$ Mrad/s. A large variation in the Switched-1R maximum slope over the tuning parameters is observed, while that of the Switched-2R is nearly flat. This demonstrates an important advantage in term of a relaxed slew requirement in the opamp for Switched-2R circuits.

4.3.2 Graphical Approximation of the Maximum Slope

Another method that can be used to find the maximum slope of the first-order switched-resistor filters is to utilize a graphical approximation [69]. This method yields a closed form equation of the maximum slope that shows a direct relation to V_p, m, ω_{in}, and ω_{clk}.

4.3.2.1 Qualitative Analysis

As mentioned in Chapter 4.3.1 that the maximum output slope of a sinusoidal signal occurs at the zero crossing. So, for the sake of analysis, a ramp

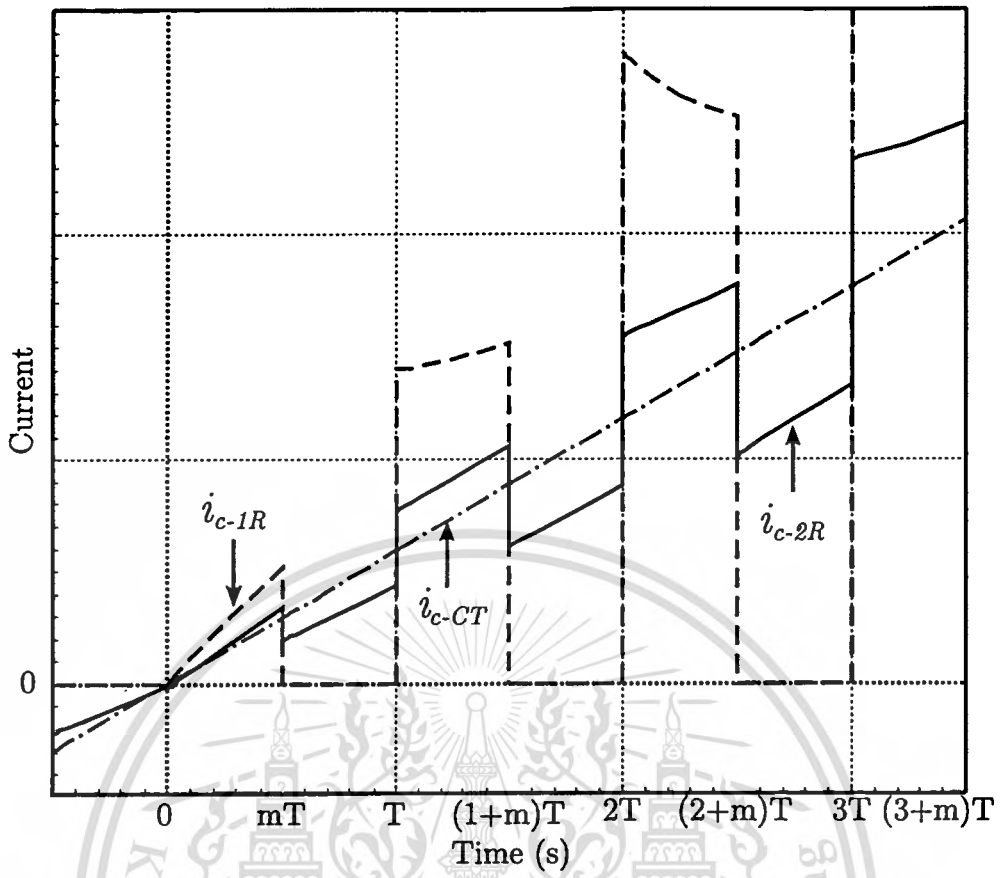


Figure 4.5 Capacitor currents of the first-order filters

signal with a constant slope of $V_p\omega_{in}$ is applied to the input for analyzing slew behavior of the first-order filter. Fig. 4.5 shows the capacitor current of the first-order Switched-1R (i_{c-1R}) and Switched-2R (i_{c-2R}) filters for 50% duty cycle and identical effective time-constants. For comparison, the current of a continuous-time filter i_{c-CT} is also included. It should be noted that the *average* current of the switched-resistor circuits must be equal to the current in the continuous-time circuit in order to produce equivalent frequency response characteristics. Since the rate of change of the output voltage dv_o/dt is the same as the voltage change over the capacitor, this value is also directly proportional to the applied current and inversely proportional to its capacitor value. The capacitor value is fixed, and therefore only the current determines the voltage.

By considering the current plots in Fig. 4.5, in the Switched-1R case, the MOS switch will conduct current only during the tracking integration phase while there is zero current flow during the holding phase. A large current is therefore needed in the turn-on stage to make the average current equivalent with the continuous-time circuit. On the other hand, Switched-2R has two non-zero current flows depending on whether resistor R_1 or R_2 is conducted. They both

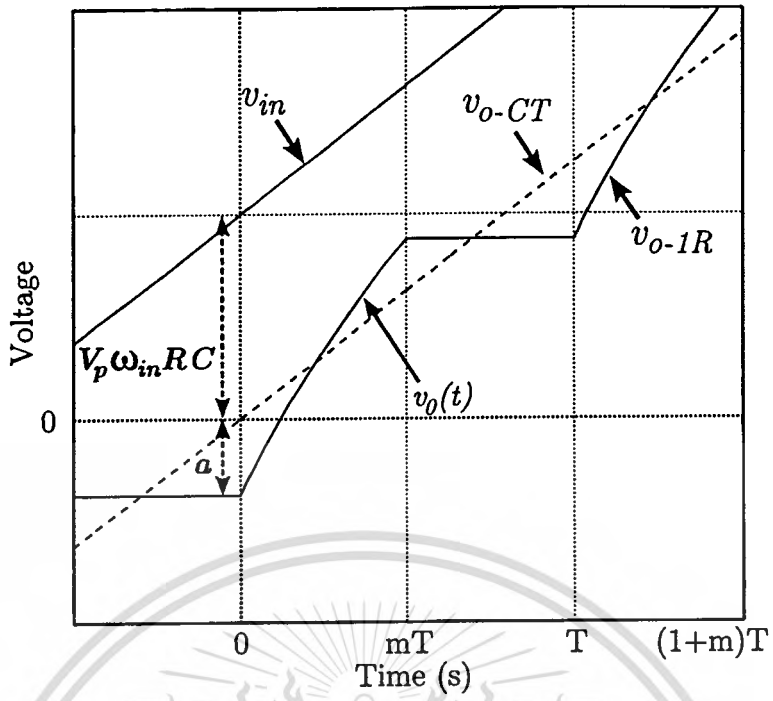


Figure 4.6 Output voltage response of the Switched-1R filter

share the duty on conveying the current, thus lower peak current magnitudes are observed. This is another perspective to the reason why one would expect a larger voltage change and higher maximum slope in the Switched-1R case than that of the Switched-2R.

4.3.2.2 Detailed Analysis

The output voltages of the first-order Switched-1R and continuous-time filters are plotted together with the input ramp signal in Fig. 4.6 (the outputs are inverted for ease of comparison with the input signal). The Switched-1R output voltage response tracks the continuous-time circuit well, except for a sawtooth-like waveform. This is because its average current has to be equal to the continuous-time current as mentioned in the previous section. It can be seen that there is a high slope response in the tracking period and zero slope in the holding period. Finding the maximum slope in the tracking period by considering at time $t = 0$ as the starting point gives an observation that the Switched-1R lags the continuous-time output by an amount a (see Fig. 4.6). Following this, the response curve within the clock period mT can be considered as a transient response of the first-order continuous-time filter with resistor R_{1-1R} value, that has been stimulated by a unit-step signal of $(V_p\omega_{in}R_{eq}C + a)$ magnitude superimposing a ramp input with slope $V_p\omega_{in}$. As a result, the complete output response will be the sum of the

individual responses to the unit-step and ramp signal together since this circuit is a linear and time-invariant system within the time period of interest. It can be derived that the output response in the tracking phase (v_0) is (see Appendix B.1)

$$\begin{aligned} v_0(t) &= \left[(V_p\omega_{in}R_{eq}(m)C + a)\left(1 - e^{\frac{-t}{R_{1-1R}C}}\right)\right] + \\ &\quad \left[V_p\omega_{in}\left(t - R_{1-1R}C\left(1 - e^{\frac{-t}{R_{1-1R}C}}\right)\right)\right] - a, \end{aligned} \tag{4.15}$$

where $R_{eq}(m)$ is the equivalent resistance from (4.5) and the magnitude of a, which is a function of the duty cycle m and the clock period T, is

$$a = V_p\omega_{in}\frac{(1-m)T + (R_{1-1R} - R_{eq}(m))Ce^{\frac{-mT}{R_{1-1R}C}}}{1 - e^{\frac{-mT}{R_{1-1R}C}}}. \tag{4.16}$$

The components in the first square brackets of (4.15) constitute the unit-step response. The second is the response to the ramp, and the last term is the initial condition. The maximum slope values of this response, which is determined by finding its derivative, is

$$S_{max-1R} = \frac{V_p\omega_{in}R_{eq}(m)C + a}{R_{1-1R}C}. \tag{4.17}$$

The output voltage of the Switched-2R filter exhibits two slopes as shown in Fig. 4.7. Remind here that $R_{1-2R} < R_{2-2R}$, and the moment at $t = 0$ refers to the state that R_{2-2R} just switches to R_{1-2R}. At that instant, the Switched-2R response is lower than the continuous-time response by an amount b. On the other hand, at the end of time period mT, the output response of the Switched-2R filter is higher than the continuous-time response by an amount c. In the same analysis manner as for the Switched-1R filter, it can be derived that the output response for the low value resistor R_{1-2R} phase ($v_1(t)$) and for the high value resistor R_{2-2R} phase ($v_2(t)$) are:

$$\begin{aligned} v_1(t) &= \left[(V_p\omega_{in}R_{eq}(m)C + b)\left(1 - e^{\frac{-t}{R_{1-2R}C}}\right)\right] + \\ &\quad \left[V_p\omega_{in}\left(t - R_{1-2R}C\left(1 - e^{\frac{-t}{R_{1-2R}C}}\right)\right)\right] - b, \end{aligned} \tag{4.18a}$$

$$\begin{aligned} v_2(t) &= \left[(V_p\omega_{in}R_{eq}(m)C - c)\left(1 - e^{\frac{-t}{R_{2-2R}C}}\right)\right] + \\ &\quad \left[V_p\omega_{in}\left(t - R_{2-2R}C\left(1 - e^{\frac{-t}{R_{2-2R}C}}\right)\right)\right] + c, \end{aligned} \tag{4.18b}$$

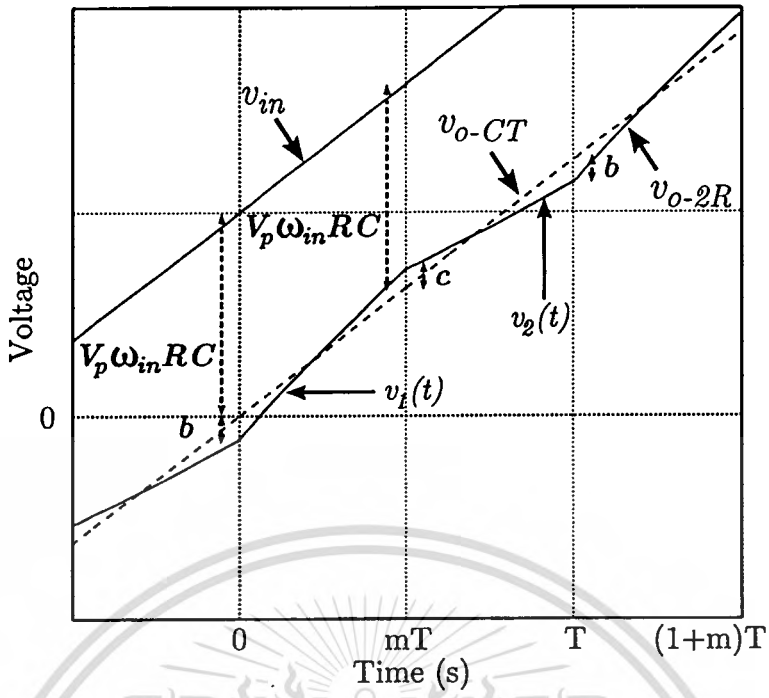


Figure 4.7 Output voltage response of the Switched-2R filter

where b and c are also functions of m and T,

$$b = \frac{V_p\omega_{in}C}{1-e^{\frac{-T}{R_{eq}(m)C}}}\left[(R_{1-2R}-R_{2-2R})e^{\frac{-(1-m)T}{R_{2-2R}C}}+ (R_{eq}(m)-R_{1-2R})e^{\frac{-T}{R_{eq}(m)C}}+(R_{2-2R}-R_{eq}(m))\right], \quad (4.19)$$

$$c = \frac{V_p\omega_{in}C}{1-e^{\frac{-T}{R_{eq}(m)C}}}\left[(R_{1-2R}-R_{2-2R})e^{\frac{-mT}{R_{1-2R}C}}+ (R_{2-2R}-R_{eq}(m))e^{\frac{-T}{R_{eq}(m)C}}+(R_{eq}(m)-R_{1-2R})\right]. \quad (4.20)$$

As a result, the maximum slopes that the opamp has to follow will be:

$$S_{max-2R-low} = \frac{V_p\omega_{in}R_{eq}(m)C+b}{R_{1-2R}C}, \quad (4.21a)$$

$$S_{max-2R-hi} = \frac{V_p\omega_{in}R_{eq}(m)C-c}{R_{2-2R}C}e^{\frac{-(1-m)T}{R_{2-2R}C}}+V_p\omega_{in}\left(1-e^{\frac{-(1-m)T}{R_{2-2R}C}}\right). \quad (4.21b)$$

Note that the occurred maximum slope of the Switched-2R filter operating with the low value resistor R_{1-2R} is always higher than that with high valued resistor

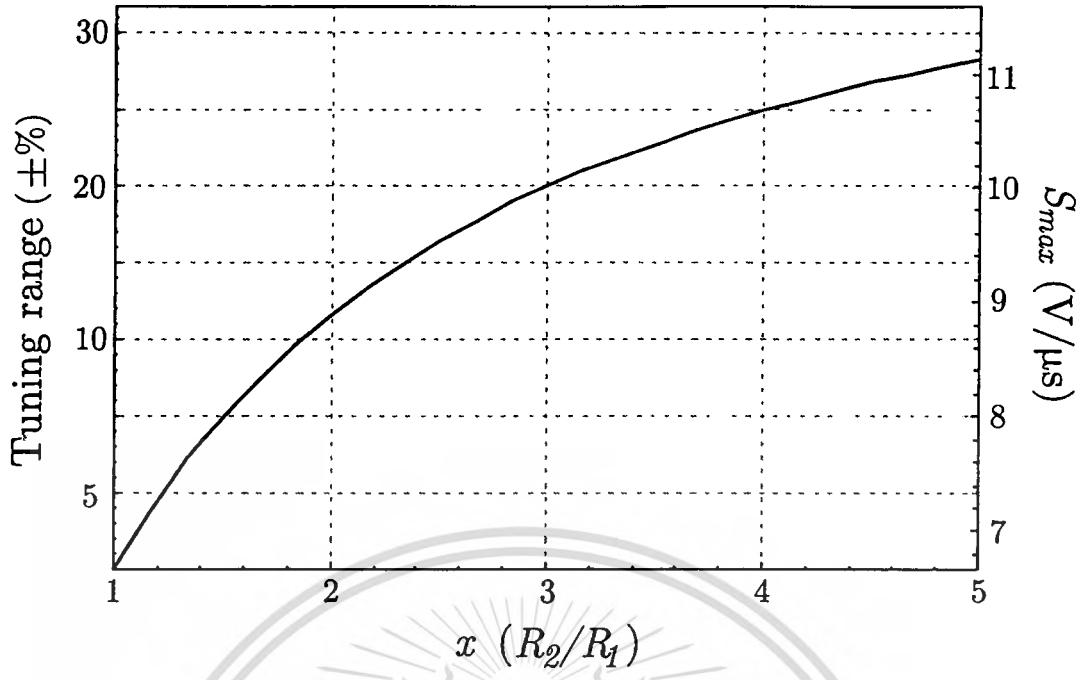


Figure 4.8 Tuning range for m between 25%–75% and the maximum slope of Switched-2R integrator vs. resistor ratio.

R_{2-2R}, the low resistance phase therefore determines the slew rate requirement of the Switched-2R filter [69].

(4.17) and (4.21) show a direct relation between the output maximum slope of the switched-resistor filters and parameters V_p, m, ω, and ω_{clk} (via T). This gives a similar fashion with the numerical results getting from (4.6). Moreover, plots of these maximum slope equations as a function of m and f_{clk} under the same condition that is used with the numerical method result in nearly identical graphs to those shown in Fig. 4.4.

4.4 Tuning Range Extension

Fig. 4.8 shows the plots of the frequency tuning range using (4.8) and the maximum slope using (4.13b) of the Switched-2R integrator versus the resistor ratio x for the duty cycle variation between 25%–75%, which is typical in practical implementation of the duty cycle control circuit [67, 68]. For the Switched-1R integrator, it has a constant tuning range of ±50% and a constant maximum slope of 12.57 V/μs for the same parameters as in Chapter 4.3. Clearly, a larger ratio x results in a wider tuning range, but the maximum slope increases accordingly. Eventually at a very large x, both the tuning range and S_{max} approach those of

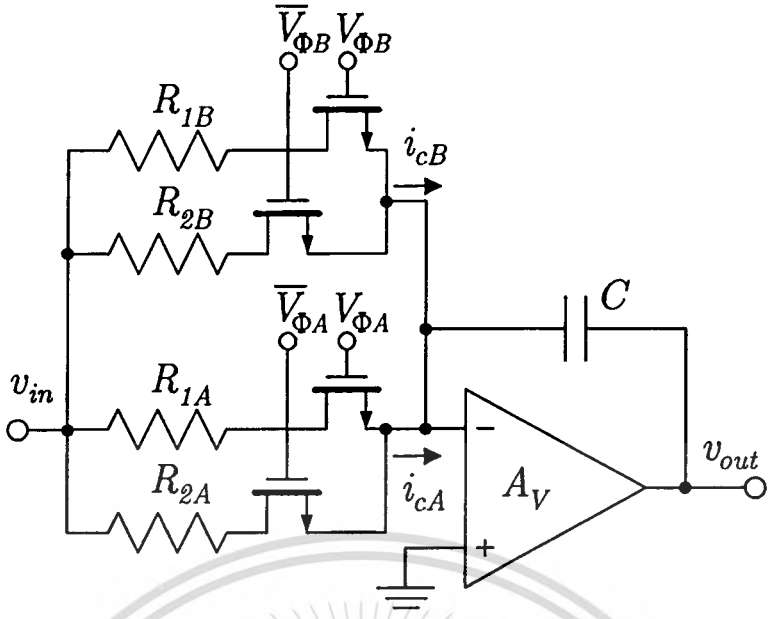


Figure 4.9 Switched-2R integrator using resistor-bank scheme.

Table 4.1 Resistor values for 10 MHz switched-resistor integrators with integrating capacitor of 3.183 pF

Resistor	Switched-1R	Switched-2R		
		bank-A	bank-B	bank-C
R_1	2.5 kΩ	11.0 kΩ	8.25 kΩ	6.19 kΩ
R_2	-	22.0 kΩ	16.5 kΩ	12.38 kΩ

the Switched-1R counterpart at ±50% and 12.57 V/μs, respectively.

An appropriate means to extend the tuning range while barely touching the maximum slew requirement is to use a resistor-bank scheme. Fig. 4.9 shows the schematic of the Switched-2R integrator using two resistor banks. The bank A and B will be operated upon whether the clock signals $V_{\Phi A}$–$\overline{V_{\Phi A}}$ or $V_{\Phi B}$–$\overline{V_{\Phi B}}$ is applied. In addition, these two control clocks can also be applied simultaneously to execute both of the resistor-bank and, in this case, the total effective resistances will become their parallel value. In this way, the value of resistor-bank A and B can be designed to have continuous frequency tuning range and then use their parallel operation to further extend the upper frequency limit.

In fact, changing the resistor value will also affect the output maximum slope according to (4.13). Fig. 4.10 shows the overall tuning range obtained from the use of three resistor banks in the Switched-2R integrator, where the resistor

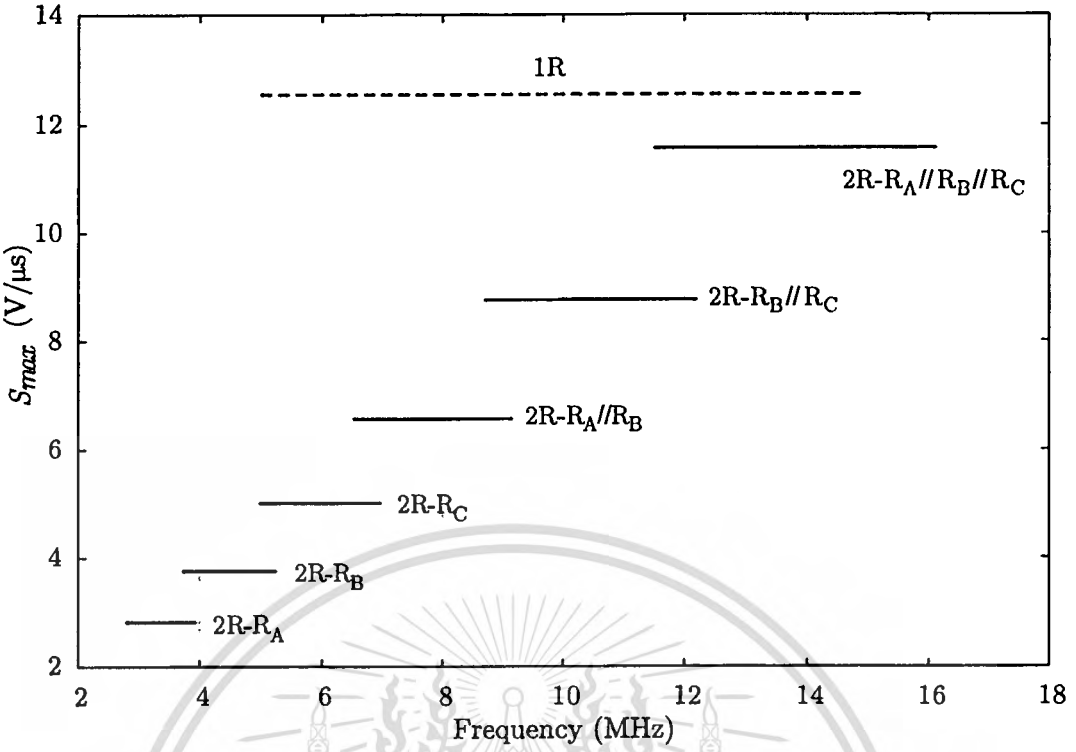


Figure 4.10 Tuning range for m between 25%–75% and the maximum slope of Switched-1R and resistor-bank-employed Switched-2R integrators.

order is $R_A > R_B > R_C$ and each of the banks has the ratio $x = 2$. For the sake of comparison, the dashed line in Fig. 4.10 shows the tuning range of the single resistor set of the Switched-1R integrator, where the duty cycle change is between 25%–75%. The resistors in each bank are designed to have at least 10% overlapping frequency to the next bank in order to cover some component variations, and their values are summarized in Table 4.1. It can be seen that the worse output maximum slope occurs when the resistor value is reduced, but the resulting excessive maximum slope per tuning range is much lower than that obtained by changing the resistor ratio directly in a single bank scheme. Moreover, it gives a total tuning range of nearly ±70% for the adjustment of m between 0.25 and 0.75, which can surpass that of the Switched-1R integrator while maintaining the smaller output maximum slopes. In other words, for an equivalent tuning range with the Switched-1R, the resistor ratio x in the Switched-2R circuits can be reduced so that a further reduction in the output maximum slope is obtained. This offers another choice to trade between the tuning range, distortion, and the number of elements or die area.

4.5 Frequency Translation

Since the switched-resistor networks exhibit a periodic time-varying nature, there exists frequency translation of input signals which can give rise to interferences at the output. The most important issue is the down-conversion of the inputs outside the baseband frequency, particularly those with spectral components around the clock frequency and its harmonics. This is because the down-converted signals directly interfere with baseband inputs. To suppress these spurs, it is necessary to include an input pre-filter in the switched-resistor networks. Although there is also an up-conversion of baseband inputs to frequencies near the clock spectral lines, this is not severe because the limited bandwidth of the switched-resistor network itself as well as the following stages help suppress such high-frequency interferences. In addition, some of the inputs that cause the up-conversion components are already attenuated by the input pre-filter. If this is not adequate, a dedicated smoothing filter may be employed. Therefore, the up-conversion analysis is disregarded in this section.

The effect of the frequency translation can be analyzed by focusing on the second term of the output voltage expression for the switched-resistor integrator in (4.4) involving the product of $\Phi(m,t)$ and $v_{in}(t)$. Recall that this term was omitted in the analysis of the baseband characteristic in Chapter 4.2. For a sinusoidal input $v_{in}(t) = V_p \sin(\omega_{in} t)$ with the peak magnitude at V_p, the second term in (4.4) yields the output voltage of

$$v_{o-2R,int}(t) = -\left(\frac{1}{R_1} - \frac{1}{R_2}\right)\frac{V_p}{\pi C}\sum_{n=1}^{\infty}\left[\frac{\sin(mn\pi)\cos((n\omega_{clk}-\omega_{in})t - mn\pi)}{n(n\omega_{clk}-\omega_{in})} - \frac{\sin(mn\pi)\cos((n\omega_{clk}+\omega_{in})t - mn\pi)}{n(n\omega_{clk}+\omega_{in})}\right]. \tag{4.22}$$

By using (4.22), the voltage conversion gains of the down-converted spur components, i.e., from ω_{in} to $n\omega_{clk} - \omega_{in}$, of the Switched-1R and the Switched-2R integrators can be derived in terms of their corresponding unity-gain frequencies as

$$A_{int-1R} = \frac{\omega_{u-1R}(m)}{|n\omega_{clk} - \omega_{in}|} \cdot \left|\frac{\sin(mn\pi)}{mn\pi}\right|, \tag{4.23a}$$

$$A_{int-2R} = \frac{\omega_{u-2R}(m) - \omega_{2-2R}}{|n\omega_{clk} - \omega_{in}|} \cdot \left|\frac{\sin(mn\pi)}{mn\pi}\right|, \tag{4.23b}$$

where $\omega_{2-2R} = 1/R_{2-2R}C$. Similarly, the conversion gains for the first-order

switched-resistor filters can be analyzed from the second term in (4.6), and these are given by

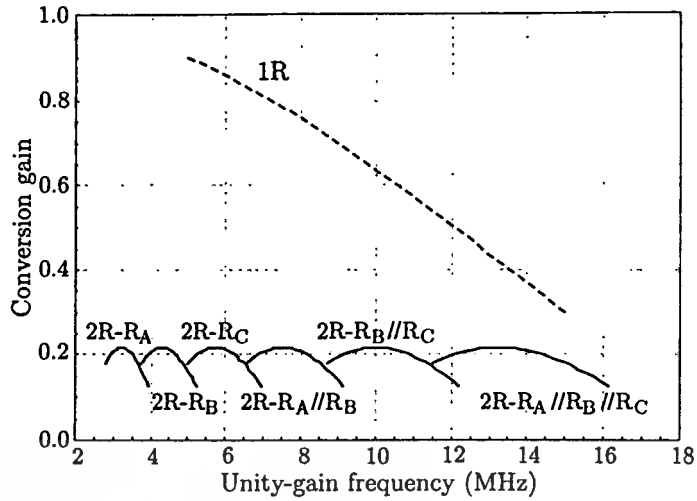
$$A_{fil-1R} = \frac{1}{\sqrt{1+\left(\frac{n\omega_{clk}-\omega_{in}}{\omega_{u-1R}(m)}\right)^2}} \cdot \left|\frac{\sin(mn\pi)}{mn\pi}\right|, \tag{4.24a}$$

$$A_{fil-2R} = \frac{1-\frac{\omega_{2-2R}}{\omega_{u-2R}(m)}}{\sqrt{1+\left(\frac{n\omega_{clk}-\omega_{in}}{\omega_{u-2R}(m)}\right)^2}} \cdot \left|\frac{\sin(mn\pi)}{mn\pi}\right|. \tag{4.24b}$$

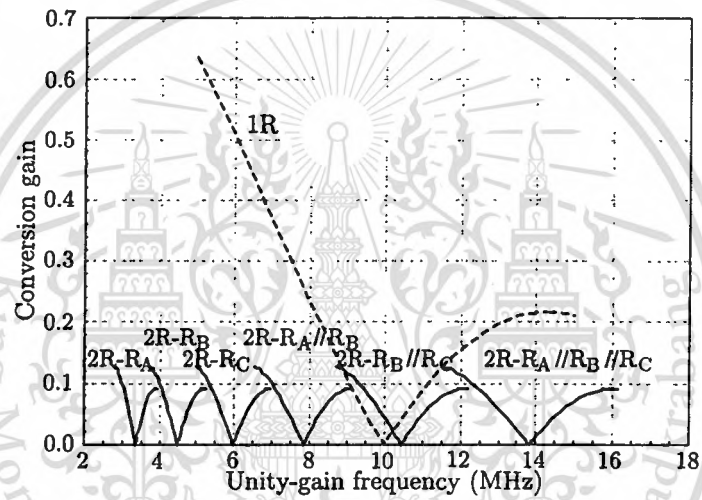
Note that the 3-dB cutoff frequencies ω_c of the first-order filters are represented by the unity-gain frequencies ω_u of their corresponding integrators for simplicity since they are identical as mentioned in Chapter 4.2.

By using (4.23) and the RC bank values listed in Table 4.1, the plots of the down-conversion gain from ω_{in} to the unity-gain frequency $\omega_u(m)$, i.e., under condition $|n\omega_{clk} - \omega_{in}| = \omega_u(m)$ in (4.23a) and (4.23b), at n = 1, 2, 3, are given in Fig. 4.11 for both the Switched-1R and Switched-2R integrators. The duty cycle change between 25%–75% for each band of the resistor-bank is assumed. For the case of first-order switched-resistor filters under the condition that the down-converted components $|n\omega_{clk} - \omega_{in}|$ are well below their 3-dB cutoff frequencies, it can be shown from (4.24) that the same plots in Fig. 4.11 are also a representative of their conversion gains. These gains will continuously reduce when the translating frequency increases and will drop with 3 dB at the cutoff frequency following the filter characteristic. In the plots, similarity between the variations of the conversion gain for the same m at each resistor-bank is noticed. This is because, under the applied condition, the frequency-related coefficients in (4.23)–(4.24) are made constant regardless of the choice of the resistor bank, and thus the conversion gain only depends on m and n through the *sinc* function. Also observed from the figure is that the Switched-2R circuit generally exhibits smaller overall conversion gain and this is due to the existence of the minus term, ω_{2-2R}, in the Switched-2R equations. [See (4.23b) and (4.24b)]

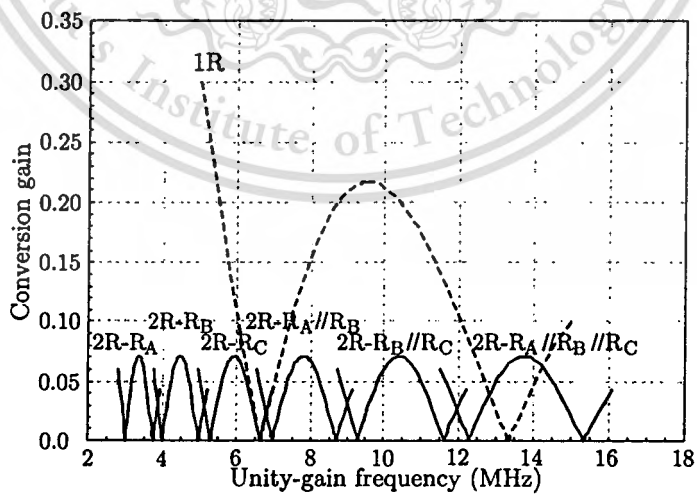
Fig. 4.11 is useful for order selection of the pre-filter. For instance, assume that the first-order switched-resistor filters require an in-band signal-to-interference ratio (SIR) better than –40 dB. From Fig. 4.11, the largest conversion gain of the Switched-1R filter occurs at n = 1 and m = 0.25 with a value of 0.902 or –0.89 dB. By including possible cutoff frequency variation at ±50%, it can be found that a third-order 20 MHz continuous-time pre-filter is required to satisfy the SIR requirement. In case of the Switched-2R filter, the largest gain of 0.217



(a)



(b)



(c)

Figure 4.11 Voltage conversion gains of the switched-resistor integrators at unity-gain frequency. (a) $n = 1$. (b) $n = 2$. (c) $n = 3$.

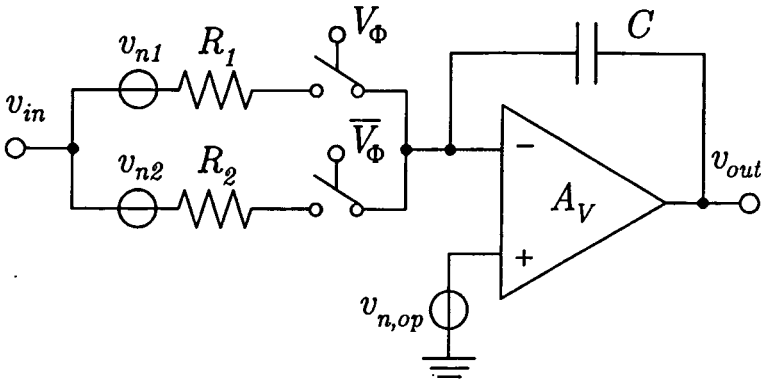


Figure 4.12 Noise sources in the Switched-2R integrator.

or −13.27 dB at $m = 0.5$ is found. Since the conversion gain is smaller, the pre-filter order requirement is reduced to second-order for the same 20 MHz cutoff frequency with ±50% variation. It can then be deduced that the Switched-2R circuits require less pre-filter order with consequent benefits to less complexity and less power consumption.

4.6 Noise Analysis

A Switched-2R integrator with two major noise sources from resistors and opamp is shown in Fig. 4.12. Thermal noise from the channel conductance g_{ds} of the MOS switches are omitted since they are negligible as compared to the passive resistors. Flicker noise caused by a non-zero time-varying drain current in the switches and noise from clock jitter are also negligible when the control signals approach square wave [72, 73]. It is worth noting that since Switched-2R circuits have currents flowing through the capacitor C in both switching phases, they possess no hold mode in their operation. As a consequence, they are deprived of noise folding. By contrast, the Switched-1R circuits incorporate hold phase, but since their output noise spectrum exhibit bandwidths much lower than the clock frequency, only a small noise portion is folded down from high frequencies to the baseband. This results in negligible noise contribution due to sample-and-hold operation in the Switched-1R circuits and it is omitted in the following analysis.

First, consider the noise component $v_{n1}(t)$ of the resistor R_1 in the Switched-2R integrator, which can be considered as wide sense stationary (WSS) with power spectral density (PSD) $S_{n1} = 4kT_jR_1$ where k is Boltzmann's constant and T_j is the absolute temperature. The noise current due to R_1 that flows into the capacitor C after switching is a cyclostationary noise process

$$i_{c,n1}(t) = \frac{v_{n1}(t)}{R_1} \cdot p(t), \tag{4.25}$$

and its time-average PSD is [73]

$$S_{c,n1}(f) = \sum_{n=-\infty}^{\infty} |p_n|^2 \frac{S_{n1}(f - nf_{clk})}{R_1^2}. \tag{4.26}$$

Since $S_{n1}(f)$ is constant, it can be moved out of summation. After being shaped by the capacitive impedance, the PSD of the output voltage noise power is given by

$$\begin{aligned} S_{n1}^o(f) &= \left|\frac{1}{j2\pi fC}\right|^2 \frac{S_{n1}(f)}{R_1^2} \sum_{n=-\infty}^{\infty} |p_n|^2 \\ &= \frac{4kT_jR_1}{(2\pi fR_1C)^2} m, \end{aligned} \tag{4.27}$$

where

$$\sum_{n=-\infty}^{\infty} |p_n|^2 = \frac{1}{T_{clk}} \int_0^{T_{clk}} (p(t))^2 dt = m, \tag{4.28}$$

is the power of the periodic waveform $p(t)$.

Secondly, for the opamp noise which is modeled by an equivalent input referred noise source $v_{n,op}(t)$ as shown in Fig. 4.12, it is also cyclostationary due to the periodic switching. By following a similar analysis as above, the output noise density from the opamp when the R_1 branch is on, is expressed by

$$S_{n,op1}^o(f) = \overline{v_{n,op}^2} \left(1 + \frac{1}{(2\pi fR_1C)^2}\right) m. \tag{4.29}$$

Next, the output noise contribution from R_2 and the opamp when the R_2 branch is on can be also explained in similar way to (4.27) and (4.29), respectively, with R_2 replacing R_1 and $(1-m)$ replacing m. Finally, if uncorrelated noise sources are assumed, the total output noise PSD of the Switched-2R integrator is

$$\begin{aligned} S_{n-2R,int}^o(f) &= \frac{4kT_jR_1}{(2\pi fR_1C)^2} m + \frac{4kT_jR_2}{(2\pi fR_2C)^2} (1-m) \\ &\quad + \overline{v_{n,op}^2} \left(\frac{m}{(2\pi fR_1C)^2} + \frac{1-m}{(2\pi fR_2C)^2} + 1\right). \end{aligned} \tag{4.30}$$

The rearrangement of the noise expression in terms of its equivalent resistor R_{eq2R}, unity-gain frequency ω_{u-2R} and $\omega_{1-2R} = 1/R_{1-2R}C$ is

$$\begin{aligned} S^o_{n-2R,int}(f) &= 4kT_jR_{eq2R}\left(\frac{\omega_{u-2R}(m)}{2\pi f}\right)^2 \\ &\quad + \overline{v^2_{n,op}}\left(\frac{(m+(1-m)/x^2)\,\omega^2_{1-2R}}{(2\pi f)^2}+1\right), \end{aligned} \tag{4.31}$$

where the output noise shaping by the integrator frequency characteristic is evident. In the case of Switched-1R integrator, the total output noise can be simply expressed using (4.31) by discarding the terms multiplied by $(1-m)$ as well as replacing R_{eq2R} with R_{eq1R}, ω_{u-2R} with ω_{u-1R}, and ω_{1-2R} with $\omega_{1-1R} = 1/R_{1-1R}C$, and it results in

$$S^o_{n-1R,int}(f) = 4kT_jR_{eq1R}\left(\frac{\omega_{u-1R}(m)}{2\pi f}\right)^2 + \overline{v^2_{n,op}}\left(\frac{m\omega^2_{1-1R}}{(2\pi f)^2}+1\right). \tag{4.32}$$

The same analysis procedure can be applied to the first-order switched-resistor filters where the total output noise of the Switched-2R and the Switched-1R are respectively given in (4.33) and (4.34).

$$\begin{aligned} S^o_{n-2R,fil}(f) &= 2\cdot\frac{4kT_jR_{eq2R}}{1+\left(\dfrac{2\pi f}{\omega_{u-2R}(m)}\right)^2} \\ &\quad + \overline{v^2_{n,op}}\frac{4+\left(\dfrac{2\pi f}{\omega_{u-2R}(m)}\right)^2}{\omega^2_{u-2R}(m)}\cdot\frac{(m+(1-m)/x^2)\,\omega^2_{1-2R}}{1+\left(\dfrac{2\pi f}{\omega_{u-2R}(m)}\right)^2}, \end{aligned} \tag{4.33}$$

$$\begin{aligned} S^o_{n-1R,fil}(f) &= 2\cdot\frac{4kT_jR_{eq1R}}{1+\left(\dfrac{2\pi f}{\omega_{u-1R}(m)}\right)^2} \\ &\quad + \overline{v^2_{n,op}}\frac{4+\left(\dfrac{2\pi f}{\omega_{u-1R}(m)}\right)^2}{\omega^2_{u-1R}(m)}\cdot\frac{m\omega^2_{1-1R}}{1+\left(\dfrac{2\pi f}{\omega_{u-1R}(m)}\right)^2}. \end{aligned} \tag{4.34}$$

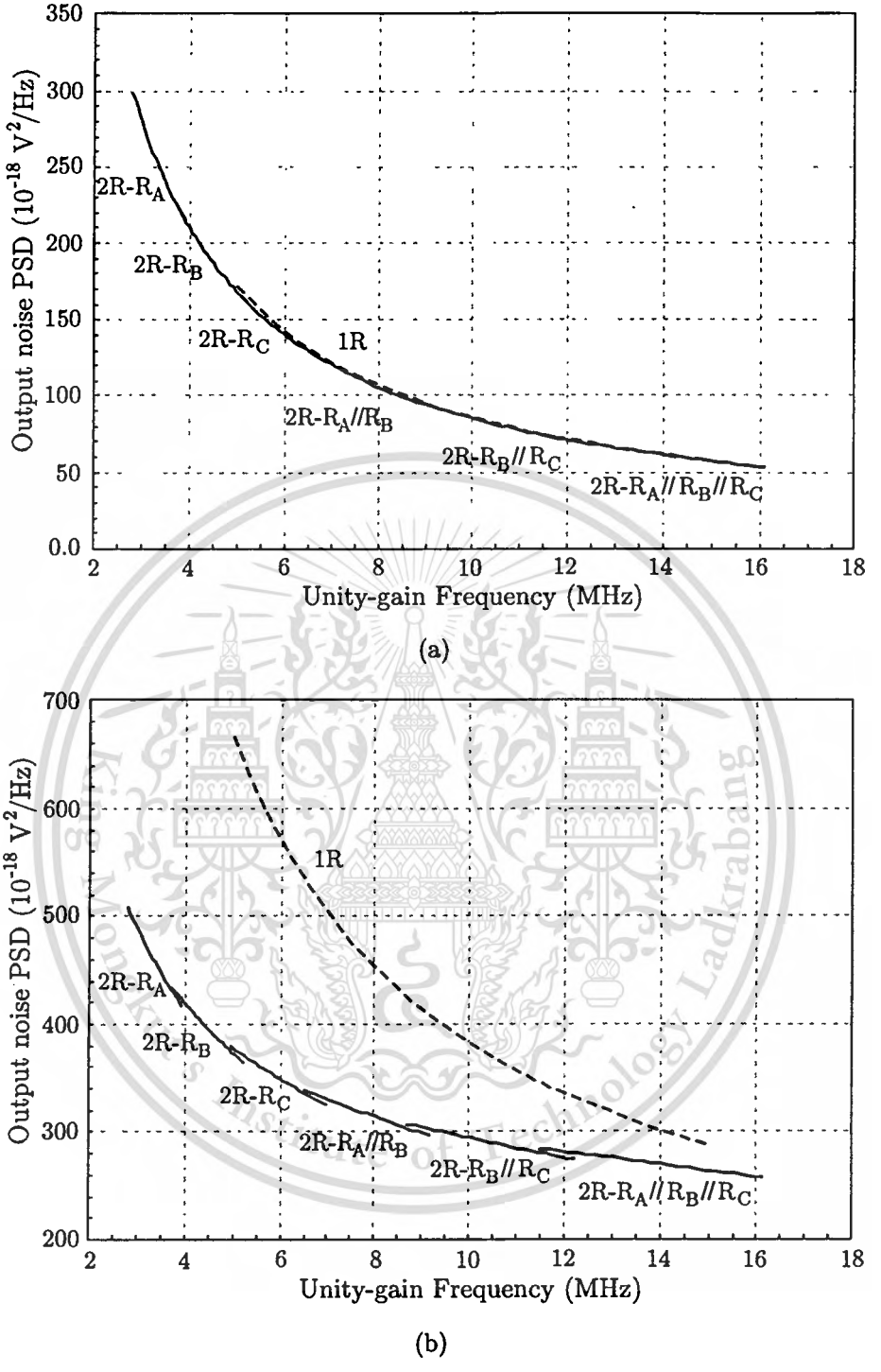


Figure 4.13 Output noise PSD of the switched-resistor integrators within unity-gain frequency tuning range. (a) Small opamp input referred noise (at one-tenth of resistor noise). (b) Large opamp input referred noise (comparable to resistor noise).

Table 4.2 Resistor values in the experimental board

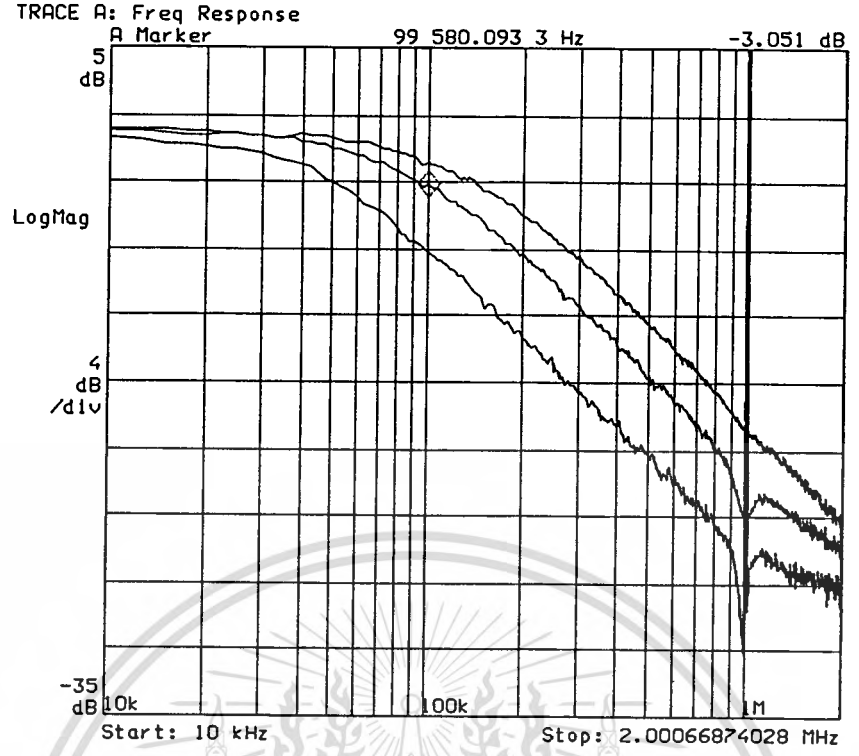
Resistor	Cont.-time	Switched-1R	Switched-2R		
			bank-A	bank-B	bank-C
R_1	10kΩ	5.1kΩ	22kΩ	16.5kΩ	12.4kΩ
R_2	-	-	44kΩ	33kΩ	24.8kΩ

By using the parameters in Table 4.1, the plots of the output noise PSD at the unity-gain frequency over the tuning range of the Switched-1R integrator and the Switched-2R integrators with resistor-bank are shown in Fig. 4.13. Fig. 4.13(a) is for the case that the opamp input referred noise is negligibly small compared to noise from the resistors which is a typical case in IC implementation. It can be observed from (4.31)–(4.34) that when the opamp's noise is negligible, the total output noise is directly proportional to the equivalent resistance and the unity-gain frequency, which are identical for the Switched-1R and Switched-2R integrators. On the other hand, Fig. 4.13(b) shows the plots when the opamp's noise and the resistors' noise are comparable, such as in the case of breadboard implementation in Chapter 4.7. It is evident from the opamp noise term in (4.31) to (4.34) that since ω_{1-2R} is always smaller than ω_{1-1R}, the output noise PSD of the Switched-2R integrator/filter are lower than that of the Switched-1R circuits especially at low frequency region of the resistor-bank set.

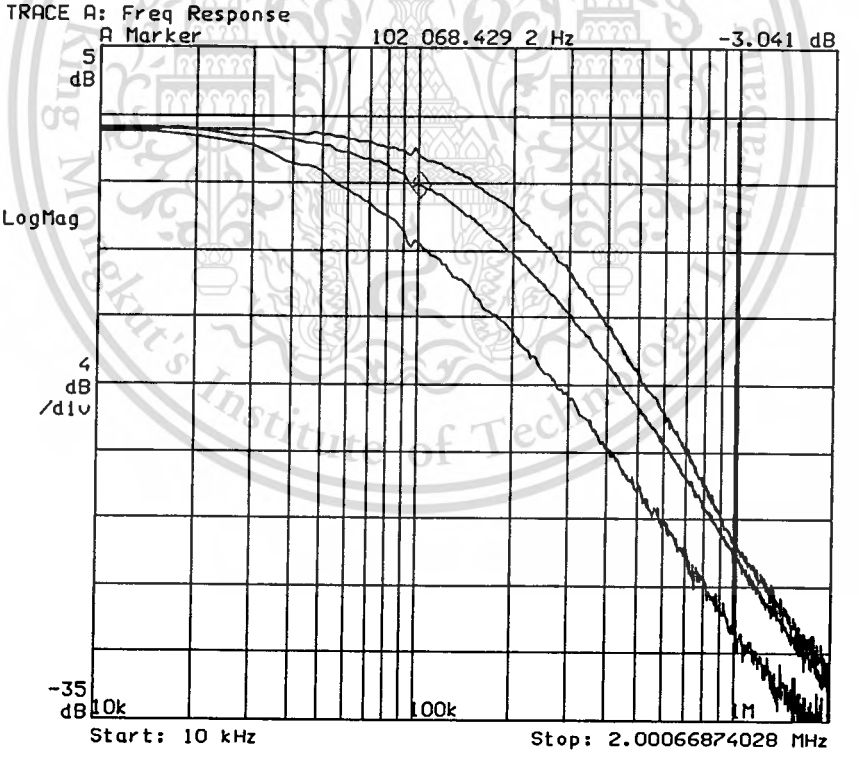
4.7 Experimental Results of First-Order Filters

Three first-order filters based on the Switched-1R, the Switched-2R and the conventional continuous-time circuits, were constructed for measurement. The opamp OPA2348, with the DC gain of 98 dB, the gain-bandwidth product (GBW) of 1.0 MHz, and the slew rate of 0.5 V/μs, and the analog switch ADG711 were selected for operating at a 5-V single supply. The clock frequency was set to 1.0 MHz unless stated otherwise. By defining the nominal 3-dB cutoff frequency ω_c to 100 kHz with the integrating capacitor C at 150 pF, the resistors values can be listed in Table 4.2.

The resistor value in the Switched-1R filter was designed to exhibit 100 kHz cutoff frequency when it is operated at 50% clock duty cycle or $m = 0.5$. The resistor-bank scheme was implemented in the Switched-2R circuit with the resistor ratio $x = 2$ (see Chapter 4.4) to cover the same frequency range of the Switched-1R filter.



(a)



(b)

Figure 4.14 Measured tuning capability of the first-order switched-resistor filters. (a) Switched-1R. (b) Switched-2R with resistor-bank.

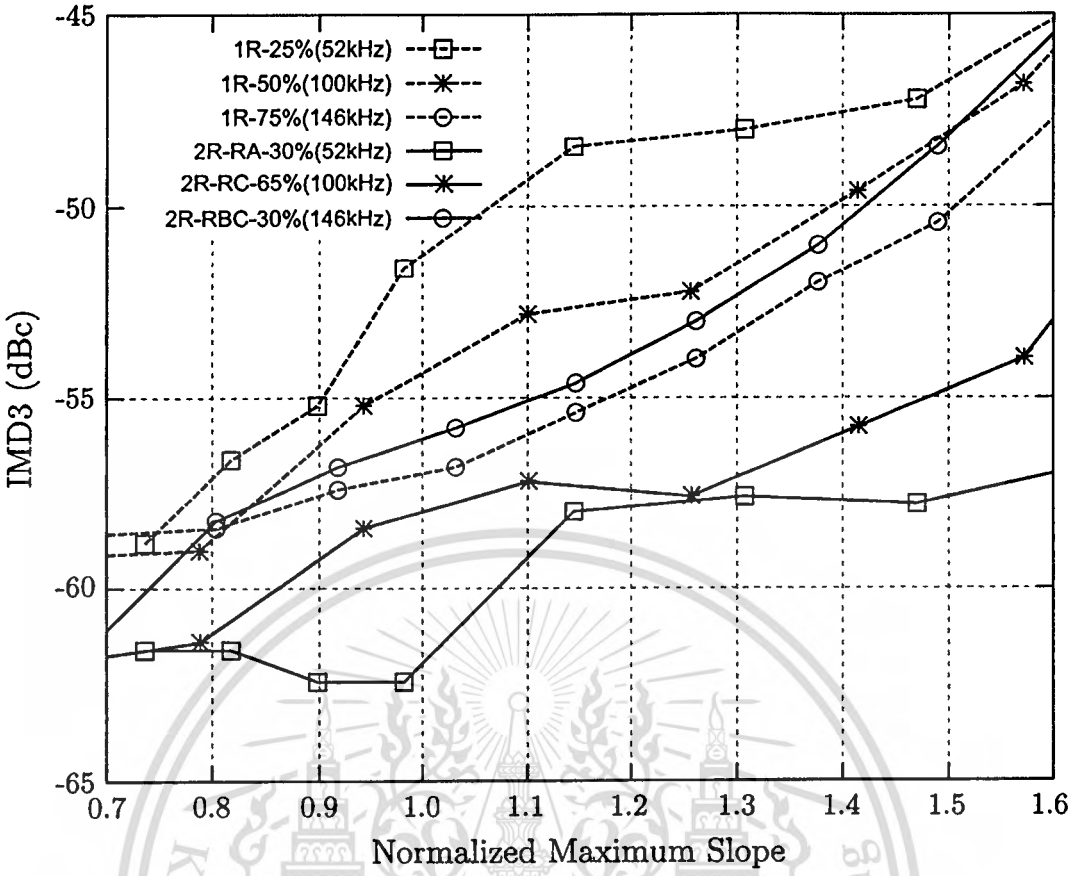


Figure 4.15 Measured distortion comparison between the first-order Switched-1R and the Switched-2R filters.

4.7.1 Frequency Response

The measured frequency tuning characteristics of the first-order switched-resistor filters are shown in Fig. 4.14. Fig. 4.14(a) shows the Switched-1R responses at $m = 0.25$, 0.50, and 0.75, which yield the cutoff frequencies about 52kHz, 100kHz and 146kHz, respectively. Fig. 4.14(b) indicates the same corresponding cutoff frequencies in the Switched-2R filter obtained by selecting the resistor-bank to R_A at $m = 0.30$, R_C at $m = 0.65$, and $R_B \parallel R_C$ at $m = 0.30$. The clock spectral lines in the frequency responses for both circuits can be noticed. However, it is more pronounced in the Switched-1R case.

4.7.2 Distortion

The measured in-band third-order intermodulation distortion (IMD3) versus the normalized maximum slope of the switched-resistor filters are shown in Fig. 4.15 under the two-tone signals, one at the cutoff frequency and the other at

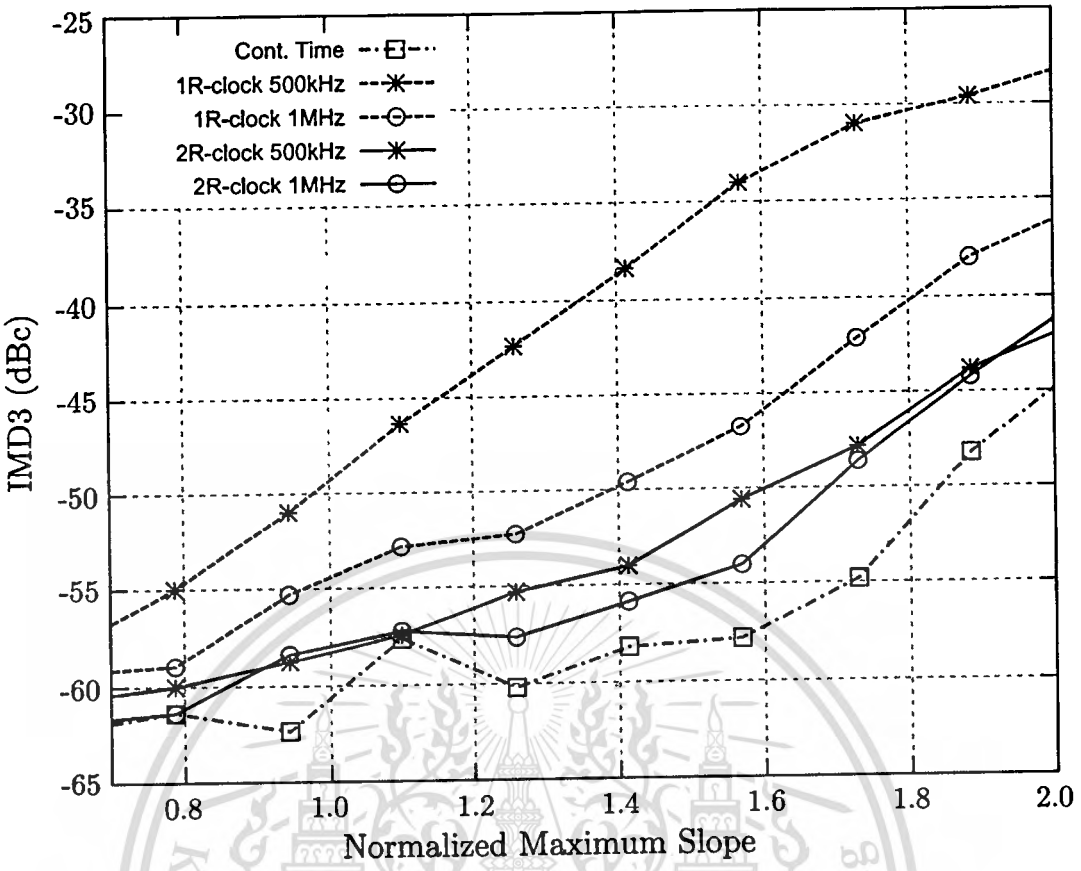


Figure 4.16 Measured distortion comparison of the first-order switched-resistor filters at 100kHz cutoff frequency with clock of 1.0 MHz and 500 kHz.

10 kHz apart. The dashed lines represent the distortion products of the Switched-1R filter, while the solid lines describe the Switched-2R results. Note that the normalized maximum slope is defined as the maximum rate of change in the input voltage divided by the slew rate parameter of the opamp. Such a normalization is introduced to allow an examination of the general circuit performances regardless of the slew performance of the employed opamp. This also helps indicate how large the input rate of change, as compared to the slew rate of opamp, the circuits can handle for a given distortion level.

By considering the IMD3 curves in Fig. 4.15, a similar level of all distortion curves at small normalized maximum slopes are observed since none of the circuits has yet reached the slew limit. It should be noted that the distortion is measured through the FFT function of a digital oscilloscope, so the minimum IMD3 is limited to about -60dBC by the resolution of the equipment. All the curves start to rise when the normalized maximum slope increases (by increasing input magnitude),

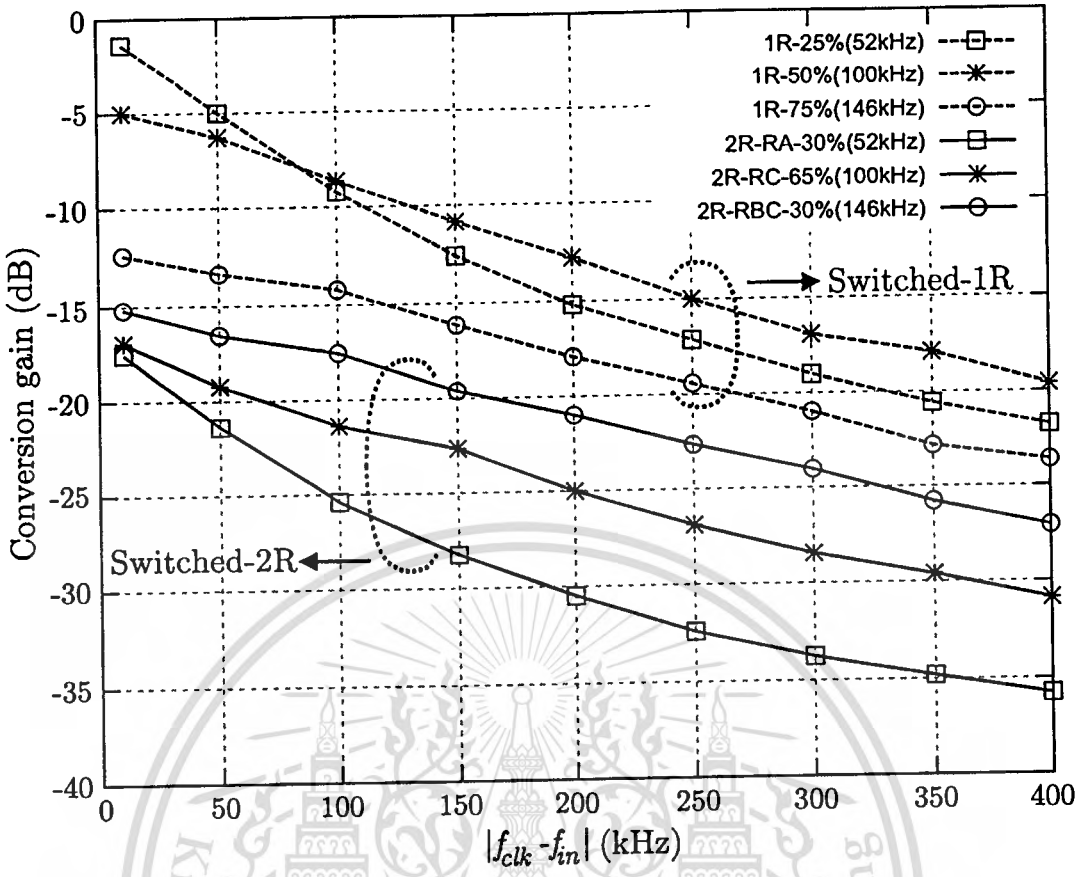


Figure 4.17 Measured conversion gains of the first-order switched-resistor filters for $n = 1$.

and a rapid growth in the IMD3 of the Switched-1R filter is evident. Moreover, the distortion of the Switched-1R filter increases at $m = 0.25$ and decreases at $m = 0.75$. This is because the output maximum slope of the Switched-1R filter is strongly proportional to m, as predicted from the numerical plot in Fig. 4.4. For the case of Switched-2R filter, the distortion is practically unchanged with m for the same resistor-bank. However, as the output maximum slope is proportional to physical RC time-constant, there is a change in the distortion curves when the filter switches to the other resistor-bank. It should be noted that the distortion is worse when the smaller resistor-bank is selected for a higher cutoff frequency. This is in contrast to the Switched-1R filter, which obtains smaller distortion level when move to a higher cutoff frequency by increasing the duty cycle m. This as a consequence results in similar distortion performances between the Switched-2R and the Switched-1R filters at high cutoff frequencies. Nevertheless, the Switched-2R filter still provides an overall better performance than the Switched-1R filter. For instance, consider the plots in Fig. 4.15 at the unity normalized maximum

slope, the distortion level of the Switched-2R filter is about 3.8 dB lower than that of the Switched-1R filter at 100 kHz cutoff frequency ω_c and this difference increases to 10.7 dB at $\omega_c = 52$ kHz although the distortion is 0.9 dB higher at $\omega_c = 146$ kHz. This implies that one can employ the opamp with lower slew rate specification in the Switched-2R filters, which gives it a possibility for a lower noise and power consumption [74] compared with those of the Switched-1R counterparts.

The clock reduction tolerance in the switched-resistor filters was also verified by measurement. Fig. 4.16 shows the measured IMD3 of the switched-resistor filters for 100 kHz cutoff frequency at 1.0 MHz and 500 kHz clock frequencies. The IMD3 result of the continuous-time filter is also included for comparison. It can be seen that while the distortion of the Switched-1R filter is degraded by the reduction of the clock frequency, the Switched-2R results remain close to those of the continuous-time filter even when the clock frequency is reduced by half. This shows another potential to operate the Switched-2R circuits at a lower clock frequency hence reducing the overall power consumption.

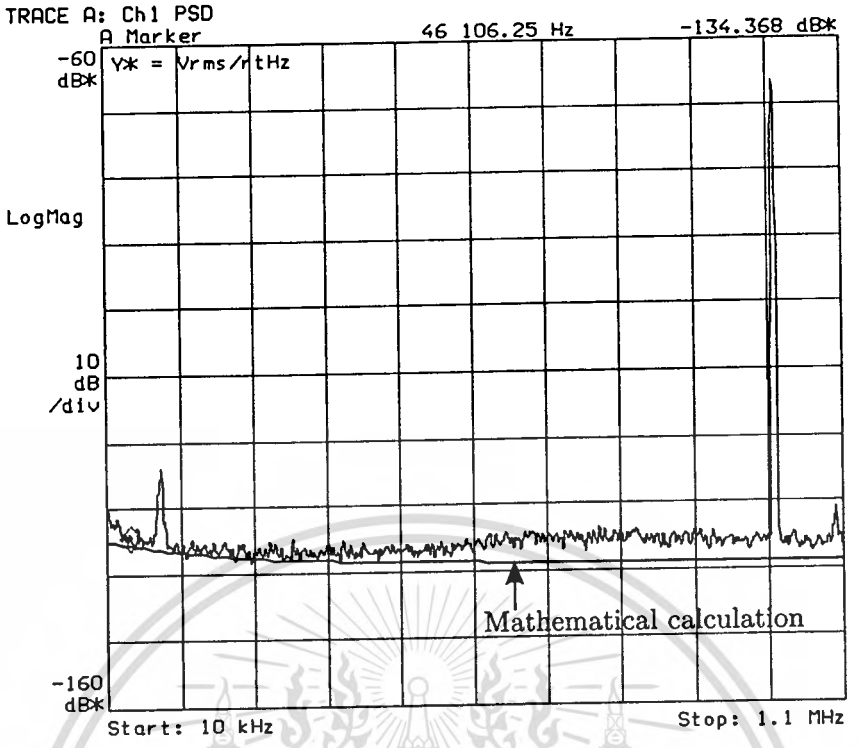
The measured voltage conversion gains versus the translating frequencies for $n = 1$ of the switched-resistor circuits are shown in Fig. 4.17. The measured conversion gains at small translating frequency agree well with the mathematical calculations plotted in Fig. 4.11(a). Moreover, the Switched-2R conversion gains are always lower than those of the Switched-1R filter as expected.

4.7.3 Noise

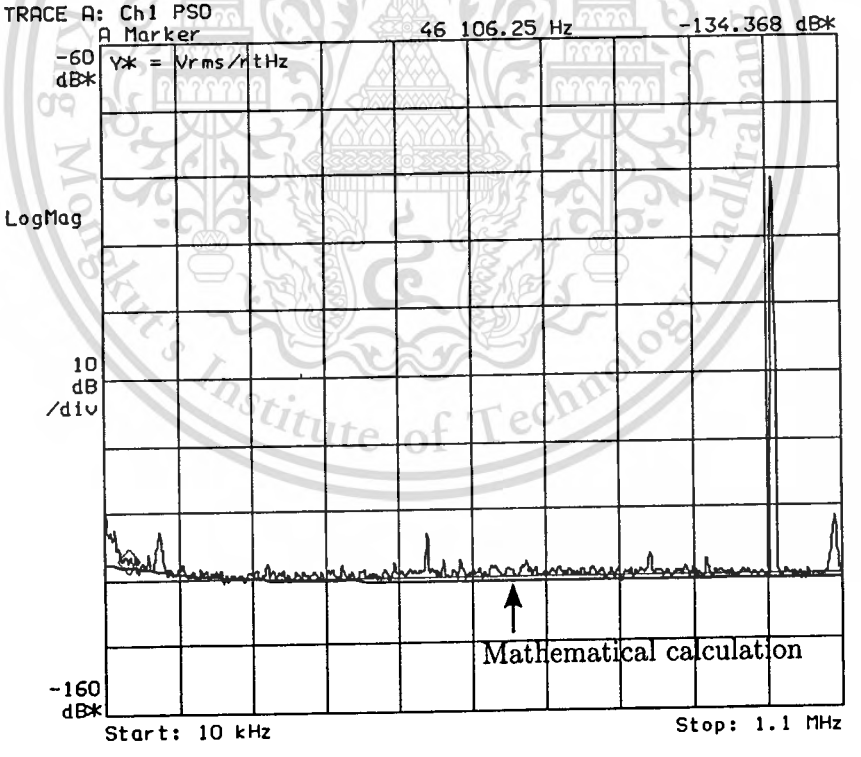
The measured output noise for the 100 kHz switched-resistor filters are compared to the calculated plots using (4.33) and (4.34) including noise floor of the equipment in Fig. 4.18. The opamp equivalent input referred noise of 35 $\text{nV}/\sqrt{\text{Hz}}$ was used in the calculations. It can be seen that a larger by about 3 dB in the output noise of the Switched-1R filter is observed at low frequencies. Also noticed is the clock spectral lines component at the output of both circuits, and it is more than 10 dB larger in the Switched-1R filter.

4.8 Design Example: Fifth-Order Elliptic Filter

Fifth-order fully differential switched-resistor elliptic low-pass filters were designed to demonstrate the capabilities and synergy of the proposed technique. The designs are based on a prototype passive RLC filter with 10 MHz cutoff frequency, 0.1 dB pass-band ripple, and 50 dB stop-band attenuation. For minimum sensitivity requirement, a leap-frog topology was used. A fully differential two-stage Miller-compensated unbuffered opamp was designed using UMC 0.18-μm



(a)



(b)

Figure 4.18 Measured output noise of the first-order switched-resistor filters at 100 kHz cutoff frequency. (a) Switched-1R. (b) Switched-2R.

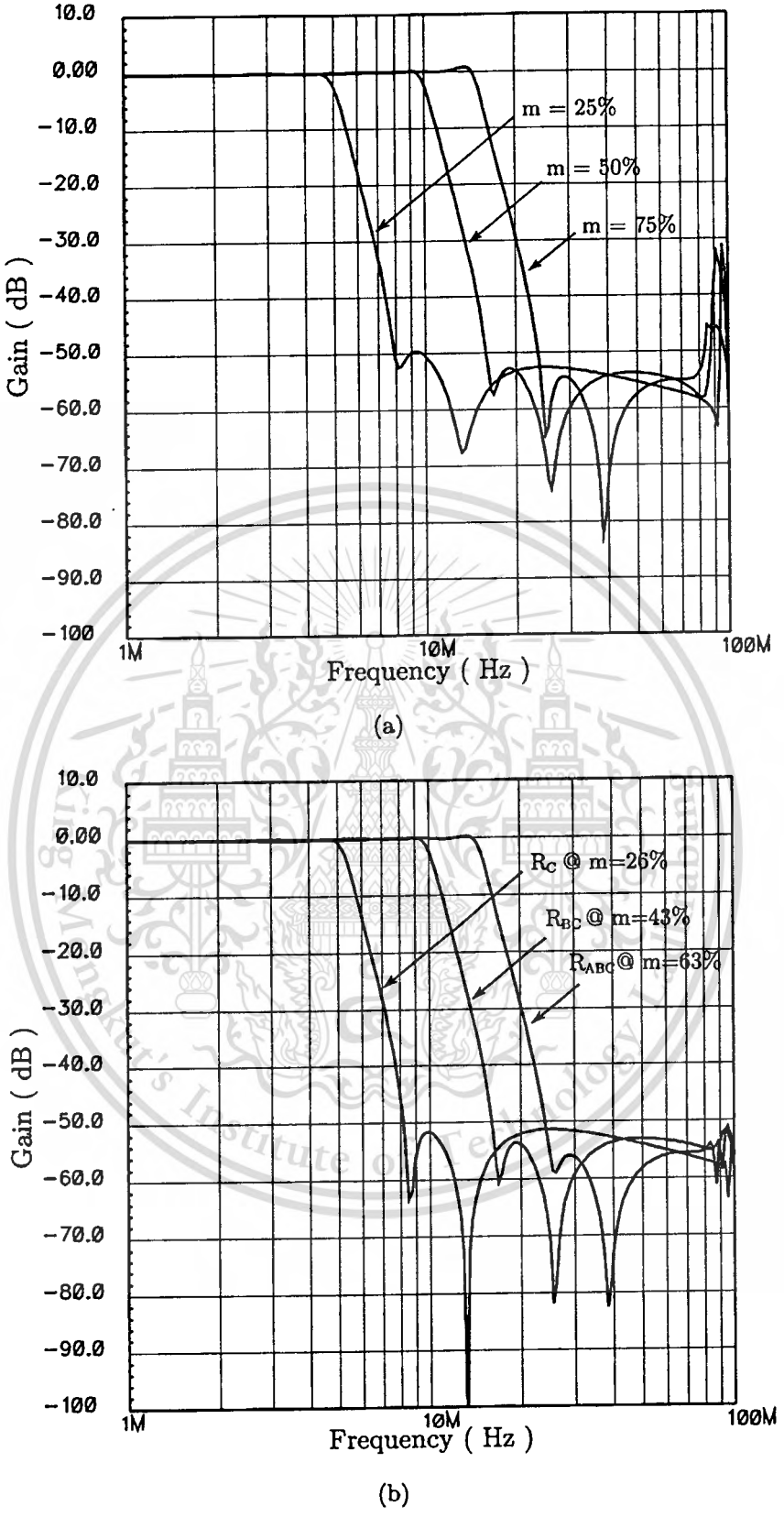


Figure 4.19 Simulated frequency response of the fifth-order switched-resistor filters. (a) Switched-1R. (b) Switched-2R with resistor-bank.

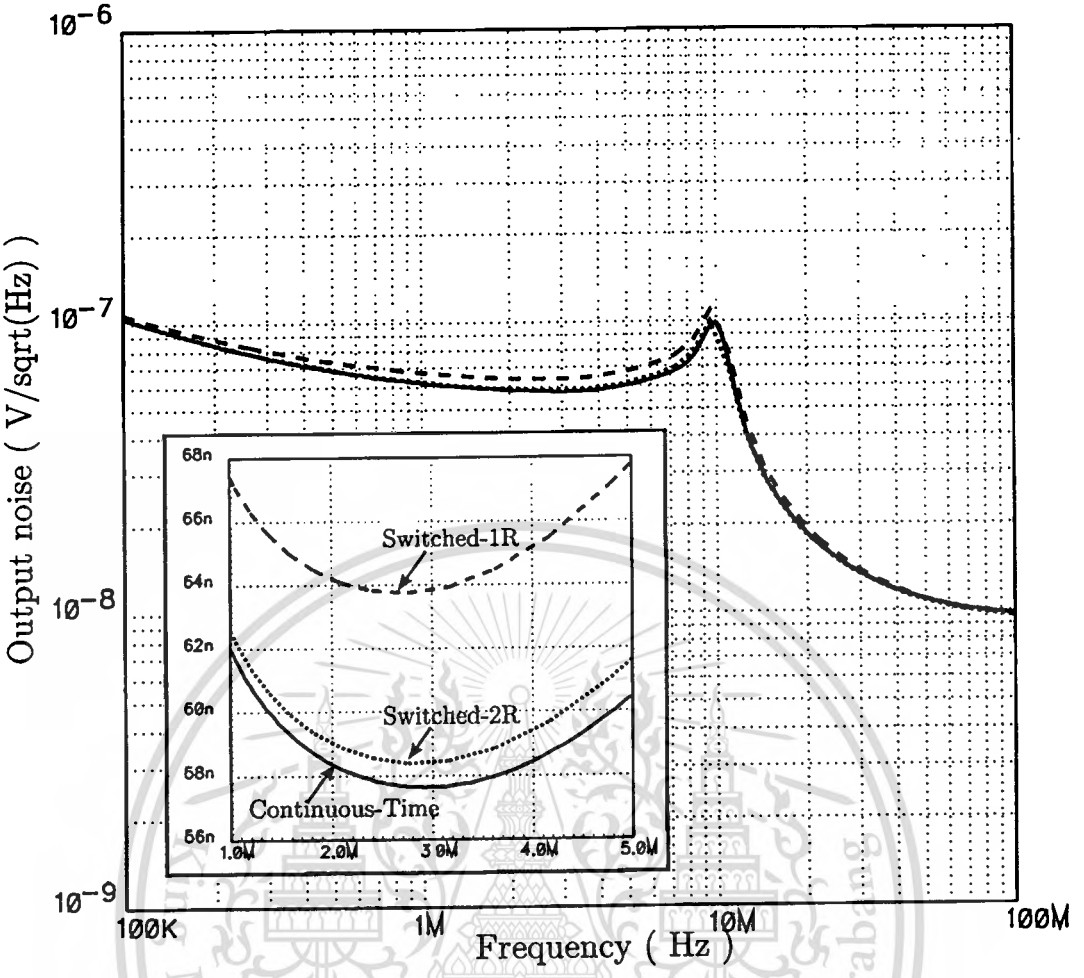


Figure 4.20 Simulated output noise of the 1.5-V fifth-order filters

CMOS process, and its simulated specifications of 53.2 dB DC gain, 340 MHz unity-gain frequency, 55.7 degree phase margin, and 103 V/μs slew rate are obtained under 1.5-V supply. All integrating capacitors are fixed at 3 pF, and the filter resistors are scaled such that the signal amplitude maxima at all opamp outputs are at the same level.

The simulated frequency responses of the fifth-order switched-resistor filters under 100 MHz clock frequency are shown in Fig. 4.19. Besides the frequency response of the filters, large clock components in the Switched-1R filter can also be observed. It should be noted that the Switched-1R filter and the Switched-2R filter with the resistor-bank were configured to have a comparable tuning range similar to Fig. 4.10 within the duty cycle change between 25%–75%. Fig. 4.20 shows the simulated output noise of the switched-resistor filters together with a result from the corresponding continuous-time filter. Those all are in the same level, only a small difference is noticed. The output noise is dominated by $1/f$ noise from the opamp at low frequencies, and the white noise from filter resistors

dominantly contribute the small flat region in the pass-band of the filters. The latter peaking at around 10 MHz is a result of filter topology and transfer function. The observed $1/f$ noise corner frequency is about 700 kHz.

The simulated in-band third-order input intercept points (IIP3), out-of-band IIP3 and integrated input referred noise of the continuous-time and the switched-resistor filters are summarized in Table 4.3. The simulation results were obtained from the nominal cutoff frequency f_c = 10 MHz and its ±50% tuning edge, i.e., 5 MHz and 15 MHz. Moreover, the results of the switched-resistor filters for both operating under 100 MHz and 50 MHz clock frequencies are included. Note that the cutoff frequency in the continuous-time filter was tuned by directly scaling all resistors in the filter.

The in-band IIP3 simulations were performed at two conditions. The first results were taken from a fixed in-band two-tone signal at 2.49 and 2.50 MHz for all cutoff frequencies f_c, and the other were taken when one tone was set to $f_c/2$ and the other tone was at 10 kHz apart. In the first condition where the input maximum voltage change is fixed, the IIP3s of the Switched-2R filter are almost identical to those of the continuous-time filter and they are nearly unchanged for all f_c. This implies that the designed opamp's slew rate is adequate to handle the output voltage change at these frequencies over the whole tuning range. On the other hand, the IIP3s of the Switched-1R filter are typically lower than the others due to its resulting large excessive output voltage change, which can cause slew limitation. Since the excessive output voltage change is inversely proportional to the duty cycle, the IIP3 of the Switched-1R filter is comparable to those of the other filters at only the upper tuning frequency edge (15 MHz).

In the latter condition, the two-tone test signal was moved up to the half of each f_c, so the input maximum voltage change would also increase. The IIP3s of the Switched-2R and the continuous-time are again almost identical, and they are reduced for increasing f_c. This is because the increased input maximum voltage change at higher f_c are beyond the opamp's slew capability. In case of the Switched-1R filter, the IIP3s also tend to reduce, but they are compensated by the reducing in excessive output voltage change. Therefore, their IIP3s seem to be nearly unchanged with f_c.

For the out-of-band IIP3 simulations, one input tone was fixed at 30 MHz and the other tone was varied to the frequency that their 3^{rd}-order intermodulation components occurred at the half of its corresponding f_c, which are 62.5 MHz, 65.0 MHz, and 67.5 MHz for f_c = 5 MHz, 10 MHz, and 15 MHz, respectively. The results show similar trend to the in-band IIP3 at varied two-tone.

Finally, the simulated input referred noises of the filters, which were inte-

Table 4.3 Simulated input intercept points (IIP3) and input referred noise

5^{th}-order filters	C-T	Sw-1R @ f_{clk}		Sw-2R @ f_{clk}	
		100 MHz	50 MHz	100 MHz	50 MHz
In-band IIP3 [dBm]					
• Fixed two-tone†					
- $f_c = 5$ MHz	38.56	31.74	30.86	38.97	37.82
- $f_c = 10$ MHz	38.99	35.72	36.19	38.16	38.02
- $f_c = 15$ MHz	38.49	38.05	37.20	37.50	37.25
• Varied two-tone‡					
- $f_c = 5$ MHz	38.56	31.74	30.86	38.97	37.82
- $f_c = 10$ MHz	35.77	30.50	30.27	34.39	34.24
- $f_c = 15$ MHz	32.54	30.33	29.58	31.04	30.89
Out-of-band IIP3 [dBm]					
• Varied two-tone§					
- $f_c = 5$ MHz	43.30	29.02	27.02	43.55	41.55
- $f_c = 10$ MHz	34.47	27.22	26.58	32.73	32.30
- $f_c = 15$ MHz	29.25	26.44	26.33	27.56	27.50
Noise* [μV rms]					
- $f_c = 5$ MHz	194.7	248.0	247.2	198.8	199.0
- $f_c = 10$ MHz	222.3	255.1	254.6	231.5	232.0
- $f_c = 15$ MHz	248.9	262.0	261.8	255.8	255.6

† : two-tone is fixed at 2.49-2.50 MHz

‡ : two-tone is varied, one at half of the cutoff frequency f_c and the other at 10 kHz apart

§ : two-tone is varied, one at 30 MHz and the other at 62.5 MHz, 65.0 MHz or 67.5 MHz corresponding to the tuned f_c

* : Input-referred, differential, integrated over 100 kHz to f_c

grated value over 100 kHz to the corresponding f_c, are almost on the same level. This results have the same direction as the plots in Fig. 4.20. It should be noted that the noises in the Switched-1R filter are slightly greater than the others especially at low f_c. This is because noises from the opamps are not sufficiently low enough comparing to the filter resistors, and they contribute to this difference in noise performance.

4.9 Conclusions

Detailed analysis of the switched-resistor technique has been studied, and it shows several potentials to very high linearity and low-voltage applications. Because the tuning process takes place in time-domain, it is not compromised by a low supply voltage. This method is also suitable for a reliable design since all nodes in the circuits stay within the power rails.

The operation principle and design parameters of the switched-resistor filters are given, whereas the slew rate induced distortion, frequency translation characteristic, and noise analysis of the switched-resistor circuits have been thoroughly analyzed.

The performance comparisons between the Switched-1R and Switched-2R filters were experimentally performed through the prototype breadboards of the first-order filter, and their results follow the theoretical predictions very well. The comparisons show that, while requiring a larger die area for implementing larger resistors, the Switched-2R filters give a better performance than the Switched-1R filters in many aspects. Applications in low-voltage environment were shown via the performance simulation of the fifth-order elliptic low-pass filters operating at only 1.5-V supply. Both the experimental and simulation results confirm that the switched-resistor technique provides a cutoff frequency tunability under low supply voltage while offering comparable performances to the continuous-time active-RC circuits.

CHAPTER 5

CONCLUSIONS

5.1 Summary and discussions

This thesis deals with the design of analog baseband active filters, which are important parts of modern communication and computer systems. Integrating such filters onto mixed-signal chips eliminates the requirement for off-chip filters, thus comes several important advantages in terms of cost, physical size, pin count, and design flexibility. One of the most importance characteristics of the integrated filters is the tunability of their time-constant, which can extremely deviate from the desired values due to process variations, environment, and aging. The development of modern integration technologies is normally driven by the needs of digital CMOS circuit design. Therefore, we proposed some techniques for realizing tunable analog baseband filters using standard CMOS technologies.

First of all, the introduction and motivation of this research were addressed in Chapter 1. Some examples showed a strong position of the analog circuits as crucial parts in digital systems. Thus, a considerable amount of efforts has been spent over the last decades for breaking the performance barrier to the design of a high performance analog filter in modern integration processes.

Chapter 2 gives a brief review of the fundamental theory of analog filters and their relate topics. Since LC ladder filters possess very low sensitivities to component variations in the passband, the simulation of their operation are expected to deliver good properties to the deriving active filters as well. The functional simulation using integrator networks has some merits over the device replacement method in the terms of design robustness and lower sensitivity to parasitic capacitances. In addition, several building block architectures for the integrator implementation, for instance, active-RC and CCII-RC, were also discussed. Some of them can be used in both voltage-mode and current-mode filter designs, however, their differences in performance are proven to occur from circuit structures usually obtained by the design and not from the mode of the processing signal. A high performance filter typically requires a dynamic range optimization execution in order to achieve the maximum signal handling. Above all, an automatic tuning circuit is an essential part of the integrated filters since the integrated technologies cannot offer sufficiently accurate passive elements by nature.

In Chapter 3, an efficient implementation of the current-mode ladder filters at any order using multi-output second-generation current controlled conveyors were discussed. The design methodology is very simple and requires the minimum number for both passive and active components. This is due to the multi-output structure that provides as many output currents as invoked by the feedback loops, so that no excessive device is required. Moreover, no external resistor is employed either since all resistance functions are replaced by the intrinsic impedance at port X of the MCCCII, and the value of which is adjustable via the bias current, resulting in a tunable corner frequency of the filter. Unfortunately, they have numerous shortcomings in practice due to body effect and device matching between PMOS and NMOS transistors unless the differential structure is employed. Moreover, the frequency response and noise performance are degraded with the additional output stages of the MCCCIIs. This thus limits the technique to low or medium speed and dynamic range applications. Some filter design examples were also included, and their characteristic were shown through the SPICE circuit simulation.

For a low supply voltage environment, the dynamic range is severely restricted from above by limited voltage swing, whereas it is being bounded from below by random noise (plus interference from digital circuits). To diminish thermal noise generated by the transconductors or MOSFET resistors, the impedance level must be decreased, thus raising the total capacitance of the filter. Unfortunately, this instantaneously leads to large chip areas, especially in high-Q applications. A more promising technique that is deprived of this limitation is the switched-resistor filter, which can be considered as an appropriate extension for the active-RC circuit. The operation principle and detailed analysis of this method were described in Chapter 4. By placing a MOS switch in series with a passive resistor and making it turns on and off abruptly with a controlling clock, the resulting effective resistance of the network is then modulated by the duty cycle of the clock. The nonlinear on-resistance of the MOS switch can be made relatively small compared to the highly linear passive resistor, so the distortion is kept at minimum. Moreover, noise from resistor also dominate the performance for a proper design of the opamp, thus the switched-resistor roughly gives a comparable dynamic range as of the continuous-time active-RC counterparts. However, the opamp may introduce a significant distortion when the slew limitation occurs. This dilemma was thoroughly studied and it was proven that the switched-resistor filters employing two sets (Switched-2R) of the switch and resistor combination has nearly identical performance to the continuous-time circuit, which is so far better than that of the filter employing one set (Switched-1R) of such switching network. However, the Switched-2R filters require a larger die area for implement-

ing resistors as a trade-off. The other problem due to its linear time-varying nature is the frequency translation. This means that some undesirable signals occurring at the out-of-band can be translated down to interfere with the in-band data, thus a prefilter should be acquired to suppress such unwanted signals. In addition, the theoretical analysis was verified by both the measurement and computer simulation results. Finally, because the tuning process takes place in time-domain, it is not compromised by a low supply voltage. This thus makes this technique perfectly suitable for a reliable, very linear, and very low-voltage application.

5.2 Interesting Topics for Future Study

Design of analog filters has several challenges in many aspects in order to reach the state-of-the-art performance. A simple suggestion one is, of course, using a more advanced CMOS precess, but the ultra-deep submicron CMOS processes also bring more troubles to analog circuit designs so that a special consideration is required. According to our works, the current-mode filters can get an improvement by applying a linearlization technique to the MCCCII circuit to stretch the linear range of the internal impedance. Alternatively, if the complementary bipolar integration technology is available, it is probably the most appropriate choice to implement the push-pull cell of the MCCCII for low-distortion current-mode signal processing applications when supply voltages are relatively large. Moreover, not only that the internal signal voltage swing is compressed by square-root function of MOS transistor working in saturation region, but also the tuning range of the MCCCII. The linearized tuning range technique can be investigated in order to extend the tuning range of the filters. Since the MCCCII uses bias current to adjust its internal resistance in similar way to the transconductor in G_m-C filter, the tuning techniques of which may be simply adopted to use with our filters with little change.

In the case of switched-resistor filters, we assume that the main source of distortion comes from slewing in the opamp. However, weakly nonlinear analysis, perhaps using the Volterra series, of this dynamic switching network may give an insight in the distortion mechanism and may disclose a secret to further reduce the overall distortion of the filters. The static switching analysis of the switched-resistor network has already been published, so it can be used as a starting point to overcome this topic. Another problem is the frequency translation, so that a prefilter is required. A challenging question is that how we can eliminate the need of this prefilter or seamlessly merge it into the main switched-resistor filter without degrading the performance of the system. On the other hand, one may exploit the

frequency translation characteristic to realize a highly linear multiplier/divider circuit as well. The switched-resistor and switched-capacitor techniques share some common properties in some manners, whereas they are quite different in the others. It is interesting to know that what is analogous and what is not. Above all, a proper duty cycle tuning circuit at high cut-off frequency is still in question. The published switched-resistor filters have the corner frequency at best of 100 kHz, while we believe that it has a potential to work at those higher frequency.

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APPENDIX A

OUTPUT RESPONSE OF THE FIRST-ORDER FILTER

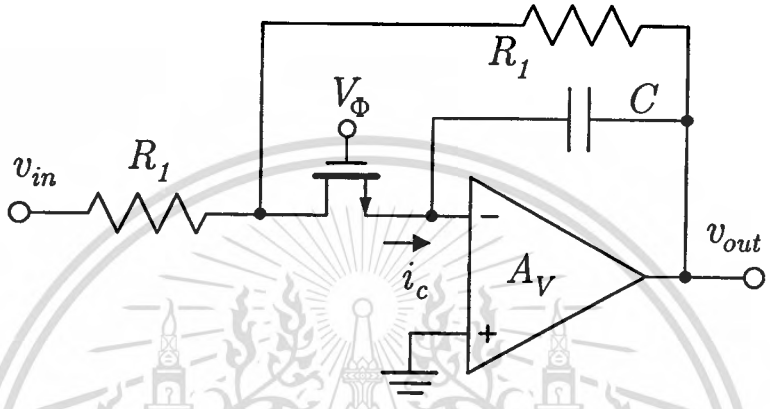

Figure A.1 The first-order Switched-1R filter

The first-order Switched-1R filter is shown in Fig. A.1. Consider when CMOS switch is closed, the charging capacitor current can be determined by the excited input voltage and the feedback output voltage as

$$i_c(t) = \frac{v_{in}(t) - v_d(t)}{R_{1a}} + \frac{v_{out}(t) - v_d(t)}{R_{1b}}. \tag{A.1}$$

This current is then passing through the CMOS switch and can be shown in form of

$$i_c(t) = \frac{v_d(t) - \frac{v_{out}(t)}{A_V}}{R_{on}}, \tag{A.2}$$

where A_V is an open-loop voltage gain of the opamp and R_{on} is an on-resistance of the MOS switch. Solving for $i_c(t)$ from (A.1) and (A.2) results in

$$
\begin{aligned}
i_c(t) &= \frac{v_{in}(t) - i_d(t)R_{on} - v_{out}(t)}{R_{1a}} + \frac{v_{out}(t) - i_d(t)R_{on} - \dfrac{v_{out}(t)}{A_V}}{R_{1b}} \\
&= \frac{R_{1b}}{D}v_{in}(t) + \frac{R_{1a}}{D}\left(1 - \frac{1 + \dfrac{R_{1b}}{R_{1a}}}{A_V}\right)v_{out}(t), \qquad \text{(A.3)}
\end{aligned}
$$

where $D = R_{1a}R_{1b} + (R_{1a} + R_{1b})R_{on}$. Moreover, $i_c(t)$ can also be shown as a rate of change of the voltage over the capacitor, that is

$$
i_c(t) = C\frac{dv_o(t)}{dt}\left(1 - \frac{1}{A_V}\right). \qquad \text{(A.4)}
$$

After taking a Laplace transform to (A.3) and (A.4), the output voltage response in s-domain can be shown as

$$
V_{out}(s) = \frac{-1}{s\dfrac{DC}{R_{1b}}\left(1 - \dfrac{1}{A_V}\right) + \dfrac{R_{1a}}{R_{1b}}\left(1 - \dfrac{1 + \dfrac{R_{1b}}{R_{1a}}}{A_V}\right)}V_{in}(s). \qquad \text{(A.5)}
$$

For $A_V \gg 1$ and $R_{1b} = R_{1a} = R \gg R_{on}$ (or $R_{on} = 0$ in case of the continuous-time filter), the response will become

$$
V_{out}(s) \cong -\frac{1}{sRC + 1}V_{in}(s). \qquad \text{(A.6)}
$$

A.1 Effect of Resistor Mismatch

To determine the effect of mismatch between input resistance R_{1a} and feedback resistance R_{1b}, $A_V \gg 1$, $R_{1b} = \alpha R_{1a}$ and $R_{on} = 0$ are assumed. Substitute these assumptions into (A.5) results in

$$V_{out}(s) = -\frac{1}{sR_{1a}C + \frac{R_{1a}}{R_{1b}}}V_{in}(s)$$
$$= -\frac{\alpha}{s\alpha R_{1a}C + 1}V_{in}(s). \quad \text{(A.7)}$$

It is obviously seen that the resistance mismatch affects both gain and cut-off frequency of the first-order filter.

A.2 Effect of Finite On-Resistance

To determine the effect of finite on-resistance, $A_V \gg 1$ and $R_{1b} = R_{1a} = R_1$ are assumed. Substitute these assumptions into (A.5) results in

$$V_{out}(s) = -\frac{1}{s\frac{(R^2 + 2RR_{on})C}{R} + 1}V_{in}(s)$$
$$= -\frac{1}{s(R + 2R_{on})C + 1}V_{in}(s). \quad \text{(A.8)}$$

In this case, the finite on-resistance only introduces a shift in cut-off frequency to the first-order filter.

A.3 Transient Response to Input Ramp Signal

For an input ramp signal $v_{in}(t) = kt$ (or $V_{in}(s) = k/s^2$), where k is slope of the ramp, the output voltage of the first-order filter can be determined from (A.6) as

$$V_{out}(s) = -\frac{1}{sRC + 1}\frac{k}{s^2}$$
$$= \frac{kRC}{s} - \frac{kRC}{s + \frac{1}{RC}} - \frac{k}{s^2}. \quad \text{(A.9)}$$

After performing an Inverse Laplace transform, the output voltage of the first-order filter in time domain response is

$$v_{out}(t) = kRC(1 - e^{\frac{-t}{RC}}) - kt. \quad \text{(A.10)}$$

APPENDIX B

GRAPHICAL APPROXIMATION OF THE MAXIMUM SLOPE

B.1 Switched-1R Filter

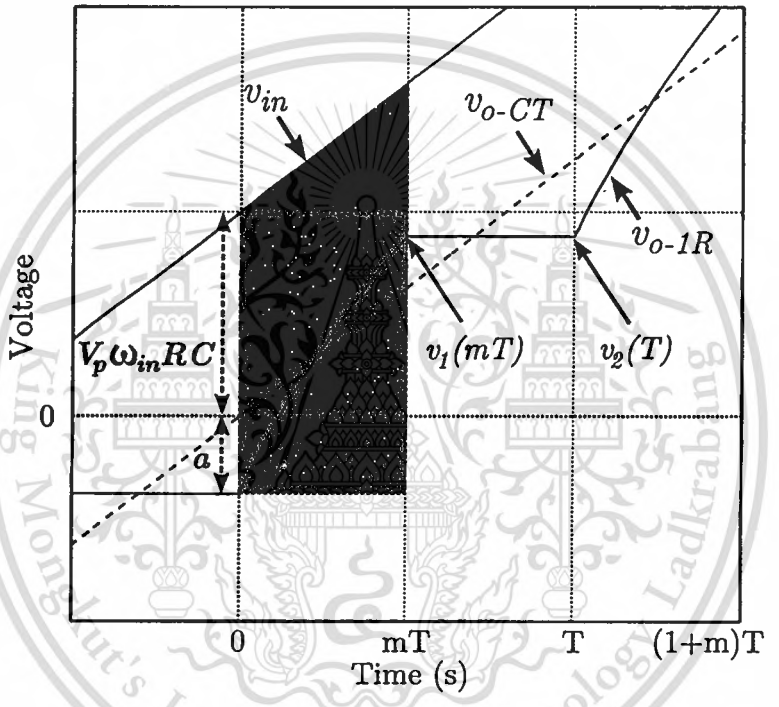

Figure B.1 Output voltage response of the Switched-1R filter

Output voltage response to input ramp signal of the first-order Switched-1R filter is shown in Fig. B.1. There is only one slope in the tracking integration phase while maintaining zero slope in the holding phase. The output voltage response of the continuous-time filter (v_{o-CT}) is included as an average of the Switched-1R response (v_{o-1R}). According to (A.10), the continuous-time response in steady state ($t \gg RC$) has a constant magnitude difference from the input signal with an amount of kRC. For an input ramp with slope of $V_p\omega_{in}$ like in this studying case, this value then becomes $V_p\omega_{in}RC$. Finding the maximum slope in tracking integration phase can be investigated by considering Fig. B.1. For the point at $t = 0$ when the switch starts to close, the output response of the Switched-1R filter

is *lower* than that of the continuous-time filter by a quantity a. Since the filter is dynamically switched, the final point within the clock period mT ($v_1(mT)$) can be considered as a result of the transient response of the first-order continuous-time filter with resistor R_{1-1R}, under the excitation of input v_{in} and the initial condition $-(V_p\omega_{in}RC + a)$. By using the graphical manipulation, it can be seen that the stimulation signal comprises a unit-step signal with magnitude of $V_p\omega_{in}R_{eq}C + a$ superimposing a ramp signal of slope $V_p\omega_{in}$ (same as the input signal) under the same period mT. Therefore, the complete output response can be obtained by summing the individual response of unit-step and ramp signals together.

The transient response to ramp input signal of the first-order filter is given in (A.10), and the unit-step response is simply $A\left(1 - exp(-\frac{t}{RC})\right)$ where A is the magnitude of the unit-step. Therefore, the output response between $0-mT$ period of the Switched-1R filter, $v_1(t)$, can be shown as

$$\begin{aligned} v_1(t) &= (V_p\omega_{in}R_{eq}(m)C + a)\left(1 - e^{\frac{-t}{R_{1-1R}C}}\right) + \\ & \quad V_p\omega_{in}\left(t - R_{1-1R}C\left(1 - e^{\frac{-t}{R_{1-1R}C}}\right)\right) - a, \end{aligned} \tag{B.1}$$

and the value at the end of period can be found from

$$\begin{aligned} v_1(mT) &= (V_p\omega_{in}R_{eq}(m)C + a)\left(1 - e^{\frac{-mT}{R_{1-1R}C}}\right) + \\ & \quad V_p\omega_{in}\left(mT - R_{1-1R}C\left(1 - e^{\frac{-mT}{R_{1-1R}C}}\right)\right) - a, \end{aligned} \tag{B.2}$$

where $R_{eq}(m)$ is the equivalent resistance of the Switched-1R filter and equal to the resistor R of the continuous-time filter. After that, the next period response between $mT - T$ ($v_2(t - mT)$) has to be found, and it appears to maintain the final value of $v_1(t)$ at time mT, so that

$$v_2(t - mT) = v_1(mT). \tag{B.3}$$

Further investigation from Fig. B.1 shows that v_{o-CT}, which has the same slope $V_p\omega_{in}$ as v_{in}, will has magnitude of $V_p\omega_{in}T$ larger than that of the origin (0,0) at the end of clock period time T. Therefore, the output response at the end of period T is $v_2(T - mT) = V_p\omega_{in}T - a$. By using this relation, (B.2) and (B.3), a can be found as

$$a = V_p\omega_{in}\frac{(1-m)T + C(R_{1-1R} - R_{eq}(m))e^{\frac{-mT}{R_{1-1R}C}}}{1 - e^{\frac{-mT}{R_{1-1R}C}}}. \quad \text{(B.4)}$$

The slope of this response can be determined by finding a derivative of the output response $v_1(t)$ from (B.1), that is

$$\frac{dv_1(t)}{dt} = \frac{V_p\omega_{in}R_{eq}(m)C + a}{R_{1-1R}C}e^{\frac{-t}{R_{1-1R}C}} + V_p\omega_{in}\left(1 - e^{\frac{-t}{R_{1-1R}C}}\right). \quad \text{(B.5)}$$

There are two boundary conditions: $t \to 0$ and $t \to mT$. By calculating (B.5), the maximum slope of the first-order Switched-1R filter occurs at $t \to 0$ and has the value of

$$S_{max-1R} = \frac{V_p\omega_{in}CR_{eq}(m) + a}{R_{1-1R}C}. \quad \text{(B.6)}$$

B.2 Switched-2R Filter

Output voltage response to input ramp signal of the first-order Switched-2R filter is shown in Fig. B.2. There are two slopes that represent two stages, that are when the filter is operated with low value resistor and high value resistor. The output voltage response of the continuous-time filter (v_{o-CT}) is also presented as an average of the Switched-2R response (v_{o-2R}).

B.2.1 Low value resistor phase

Finding maximum slope when the first-order Switch-2R filter is operated in low value resistor phase can be investigated by considering Fig. B.2(a). For $R_{1-2R} < R_{2-2R}$, point at $t = 0$ refers to a state that the switches just change from R_{2-2R} to R_{1-2R}, and the output response of the Switched-2R filter having *lower* magnitude than that of the continuous-time filter by a quantity b is observed. It can be shown that the final point within the time period $0 - mT$ ($v_1(mT)$) is a result of the transient response of the first-order continuous-time filter with resistor R_{1-2R} value, under the excitation of input v_{in} and the initial condition $-(V_p\omega_{in}R_{eq}C + b)$. By using the graphical manipulation, it can be seen that

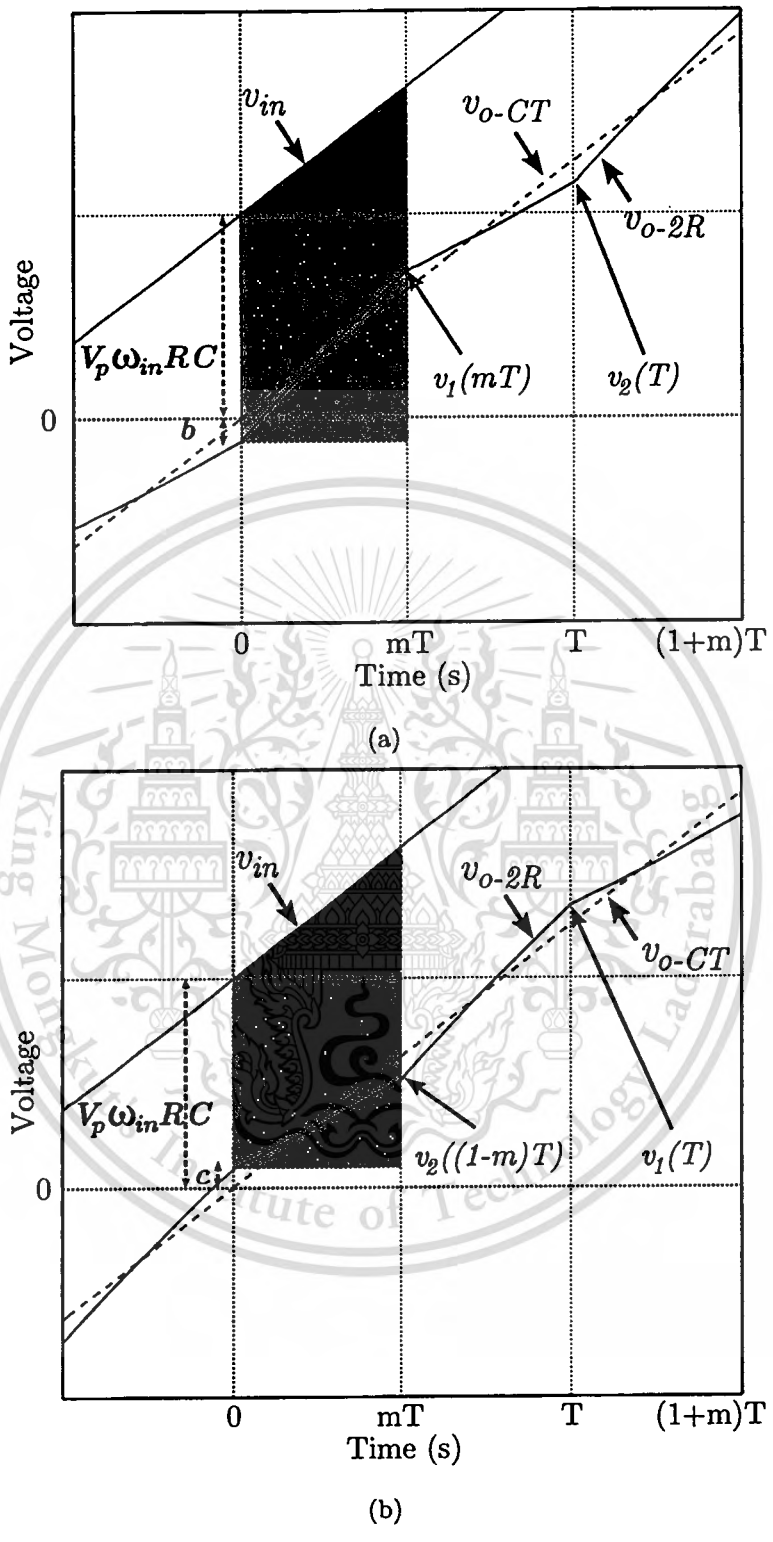

Figure B.2 Output voltage response of the Switched-2R filter (a) Low value resistor phase (b) High value resistor phase

the stimulation signal comprises a unit-step signal of magnitude $V_p\omega_{in}R_{eq}C + b$ superimposing a ramp signal with $V_p\omega_{in}$ slope under the same period time mT. Therefore, the complete output response can be obtained in similar way as of the Switched-1R filter by summing the individual response of unit-step and ramp signals together.

In case of the Switched-2R filter operating in low value resistor phase, the output voltage response, $v_1(t)$, can be shown as

$$\begin{aligned} v_1(t) &= (V_p\omega_{in}R_{eq}(m)C + b)\left(1 - e^{\frac{-t}{R_{1-2R}C}}\right) + \\ &\quad V_p\omega_{in}\left(t - R_{1-2R}C\left(1 - e^{\frac{-t}{R_{1-2R}C}}\right)\right) - b, \end{aligned} \tag{B.7}$$

and the value at the end of period can be found from

$$\begin{aligned} v_1(mT) &= (V_p\omega_{in}R_{eq}(m)C + b)\left(1 - e^{\frac{-mT}{R_{1-2R}C}}\right) + \\ &\quad V_p\omega_{in}\left(mT - R_{1-2R}C\left(1 - e^{\frac{-mT}{R_{1-2R}C}}\right)\right) - b, \end{aligned} \tag{B.8}$$

where this time $R_{eq}(m)$ is the equivalence resistance of the Switched-2R filter. Subsequently, the next period response between $mT - T$ ($v_2(t - mT)$) has to be found by taking $v_1(mT)$ as an initial, that is

$$\begin{aligned} v_2(t - mT) &= (V_p\omega_{in}(mT + R_{eq}(m)C) - v_1(mT))\left(1 - e^{-\frac{t-mT}{R_{2-2R}C}}\right) + \\ &\quad V_p\omega_{in}\left(t - mT - R_{2-2R}C\left(1 - e^{-\frac{t-mT}{R_{2-2R}C}}\right)\right) + v_1(mT), \end{aligned} \tag{B.9}$$

and the value at the end of period can be found from

$$\begin{aligned} v_2(T) &= V_p\omega_{in}C\left(R_{eq}(m) - R_2\right) + V_p\omega_{in}\left(T + C(R_{2-2R} - R_{1-2R})e^{\frac{-(1-m)T}{R_{2-2R}C}}\right) - \\ &\quad (V_p\omega_{in}C(R_{eq}(m) - R_1) + b)\, e^{\frac{-mT}{R_1C}} e^{\frac{-(1-m)T}{R_2C}}. \end{aligned} \tag{B.10}$$

Further investigation from Fig. B.2(a) shows that v_{o-CT}, which has the same slope $V_p\omega_{in}$ as v_{in}, will has magnitude of $V_p\omega_{in}T$ larger than that of the origin (0,0) at the end of clock period time T. Therefore, the value at the end of period T is $V_p\omega_{in}T - v_2(T) = b$. By using this relation and (B.10), b can be found as

$$b = \frac{V_p\omega_{in}C}{1-e^{\frac{-T}{R_{eq}(m)C}}}\left[(R_{1-2R}-R_{2-2R})e^{\frac{-(1-m)T}{R_{2-2R}C}}+ (R_{eq}(m)-R_{1-2R})e^{\frac{-T}{R_{eq}(m)C}}+(R_{2-2R}-R_{eq}(m))\right]. \quad \text{(B.11)}$$

The slope of this response can be determined by finding a derivative of the output response $v_1(t)$ from (B.7), that is

$$\frac{dv_1(t)}{dt} = \frac{V_p\omega_{in}R_{eq}(m)C+b(m,T)}{R_1C}e^{\frac{-t}{R_1C}}+V_p\omega_{in}\left(1-e^{\frac{-t}{R_1C}}\right). \quad \text{(B.12)}$$

There are two boundary conditions: $t \rightarrow 0$ and $t \rightarrow mT$. By calculating from (B.12), the maximum slope of the first-order Switched-2R filter at low resistor value phase occurs when $t \rightarrow 0$ and has the value of

$$S_{max-2R-low} = \frac{V_p\omega_{in}CR_{eq}(m)+b}{R_{1-2R}C}. \quad \text{(B.13)}$$

B.2.2 High value resistor phase

Another maximum slope when the Switched-2R filter is operated in high value resistor phase can be obtained by considering Fig. B.2(b). In the same manner, point at $t = 0$ refers to the state that the switches just change from R_{1-2R} to R_{2-2R}, and the output response of the Switched-2R filter is *higher* than that of the continuous-time filter by a quantity c. The final point within the time period $0-(1-m)T$ ($V_2((1-m)T)$) then will be a result of the transient response of the first-order continuous-time filter with resistor R_{2-2R} value, under the excitation of input v_{in} and the initial condition $-(V_p\omega_{in}R_{eq}C-c)$. The output response in high value resistor phase of the Switched-2R filter, $v_2(t)$, then can be shown as

$$v_2(t) = (V_p\omega_{in}R_{eq}(m)C-c)\left(1-e^{\frac{-t}{R_{2-2R}C}}\right)+ V_p\omega_{in}\left(t-R_{2-2R}C\left(1-e^{\frac{-t}{R_2C}}\right)\right)+c, \quad \text{(B.14)}$$

and the value at the end of period can be found from

$$v_2\left((1-m)T\right) = \left(V_p\omega_{in}R_{eq}(m)C - c\right)\left(1 - e^{\frac{-(1-m)T}{R_{2-2R}C}}\right) + V_p\omega_{in}(1-m)T - V_p\omega_{in}R_{2-2R}C\left(1 - e^{\frac{-(1-m)T}{R_{2-2R}C}}\right) + c. \quad \text{(B.15)}$$

The next period response between $(1-m)T - T$ $(v_1\left(t-(1-m)T\right))$ of the filter with $v_2\left((1-m)T\right)$ as an initial can be shown as

$$v_1\left(t-(1-m)T\right) = V_p\omega_{in}R_{eq}(m)C\left(1 - e^{-\frac{t-(1-m)T}{R_{1-2R}C}}\right) + V_p\omega_{in}\left(t-(1-m)T - R_{1-2R}C\left(1 - e^{-\frac{t-(1-m)T}{R_{2-2R}C}}\right)\right) + \left(v_2((1-m)T) - V_p\omega_{in}(1-m)T\right)e^{-\frac{t-(1-m)T}{R_{1-2R}C}}, \quad \text{(B.16)}$$

and the value at the end of period can be found from

$$v_1(T) = V_p\omega_{in}\left(R_{eq}(m)C - R_{1-2R}C + T + C(R_{1-2R} - R_{2-2R})e^{\frac{-mT}{R_{1-2R}C}}\right) - \left(V_p\omega_{in}C(R_{eq}(m) - R_2) + c\right)e^{\frac{-mT}{R_1C}}e^{\frac{-(1-m)T}{R_2C}}. \quad \text{(B.17)}$$

Fig. B.2(b) gives another relation, that is $v_1(T) - V_p\omega_{in}T = c$. By using this relation and (B.17), c can be found as

$$c = \frac{V_p\omega_{in}C}{1 - e^{\frac{-T}{R_{eq}(m)C}}}\left[R_{1-2R} - R_{2-2R}e^{\frac{-mT}{R_{1-2R}C}} + (R_{2-2R} - R_{eq}(m))e^{\frac{-T}{R_{eq}(m)C}} + (R_{eq}(m) - R_{1-2R})\right]. \quad \text{(B.18)}$$

The slope of this response can be determined by finding a derivative of the output response $v_2(t)$ from (B.14) as

$$\frac{dv_2(t)}{dt} = \frac{V_p\omega_{in}R_{eq}(m)C - b}{R_{2-2R}C}e^{\frac{-t}{R_{2-2R}C}} + V_p\omega_{in}(1 - e^{\frac{-t}{R_{2-2R}C}}). \quad \text{(B.19)}$$

Two boundary conditions, $t \rightarrow 0$ and $t \rightarrow (1-m)T$, are verified with (B.19) and result in the maximum slope at $t \rightarrow (1-m)T$. Then the maximum slope of the first-order Switched-2R filter at high resistor value phase is

$$S_{max-2R-hi} = \frac{V_p \omega_{in} C R_{eq}(m) - c}{R_{2-2R} C} e^{\frac{-(1-m)T}{R_{2-2R}C}} + V_p \omega_{in} (1 - e^{\frac{-(1-m)T}{R_{2-2R}C}}). \quad \text{(B.20)}$$

LIST OF PUBLICATIONS

Works Concerning This Thesis

1. A. Jiraseree-amornkun, N. Fujii, and W. Surakampontorn, "Realization of electronically tunable ladder filters using multi-output current controlled conveyors," in **Proceedings of the 2003 IEEE International Symposium on Circuits and Systems (ISCAS 2003)**, Bangkok, Thailand, vol. 1, May 2003, pp. I-541–I-544.

2. A. Jiraseree-amornkun, W. Tangsrirat, and W. Surakampontorn, "Tunable elliptic filters using multioutput current controlled conveyors," in **Proceedings of the 2004 IEEE Region 10 Conference (TENCON 2004)**, Chiang Mai, Thailand, vol. 4, Nov. 2004, pp. 229–232.

3. A. Jiraseree-amornkun, A. Worapishet, E.A.M. Klumperink, B. Nauta, and W. Surakampontorn, "Slew rate induced distortion in switched-resistor integrators," in **Proceedings of the 2006 IEEE International Symposium on Circuits and Systems (ISCAS 2006)**, Island of Kos, Greece, May 2006, pp. 2485–2488.

4. A. Jiraseree-amornkun, and W. Surakampontorn, "Efficient implementation of tunable ladder filters using multi-Output current controlled conveyors," **International Journal of Electronics and Communication (AEÜ) (2007)**, doi:10.1016/j.aeue.2007.01 .005.

Related Works

1. A. Jiraseri-amornkun, B. Chipipop, and W. Surakampontorn, "Novel translinear-based multi-output FTFN," in **Proceedings of the 2001 IEEE International Symposium on Circuits and Systems (ISCAS 2001)**, Sydney, Australia, vol. 1, May 2001, pp. I-180–I-183.

2. A. Jiraseree-amornkun, W. Tangsrirat, and W. Surakampontorn, "CMOS multi-output FTFN: a translinear approach," in **Proceedings of the 2001 IEEJ International Analog VLSI Workshop (AVLSIWS 2001)**, Bangkok, Thailand, May 2001, pp. 62–67.

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4. A. Jiraseree-amornkun, and W. Surakampontorn, "Constant-g_m rail-to-rail CMOS multi-output FTFN ," in **Proceedings of the 2002 International Technical Conference on Circuits/Systems, Computers and Communnications (ITC-CSCC 2002)**, Phuket, Thailand, vol. 1, July 2002, pp. 333–336.

5. A. Jiraseree-amornkun, and W. Surakampontorn, "Dual translinear loop multi-output FTFN," in **Proceedings of the 2002 IEEJ Internaltional Analog VLSI Workshop (AVLSIWS 2002)**, Singapore, Sep. 2002, pp. 94–98.

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Efficient implementation of tunable ladder filters using multi-output current controlled conveyors

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Abstract

A methodology to realize continuous-time current-mode tunable ladder filters of any order has been presented. This proposed technique individually simulates signal flow graph (SFG) of each branch element from passive filter prototype using only multi-output second generation current controlled conveyors (MCCCIIs) and grounded capacitors. This leads to simple structure, ease of design and suitability for IC fabrication. A third-order Butterworth low-pass filter, a third-order elliptic low-pass filter and a sixth-order Chebyshev band-pass filter are employed to demonstrate the proposed realization scheme. These simulated filters retain minimum requirement of passive and active elements and provide the filter corner frequency tunability. Moreover, the method allows an implementation of the elliptic filters by simply adding floating capacitors to all-pole filter structures.

Keywords: Tunable ladder filter; Current-mode; Multi-output current controlled conveyors

1. Introduction

Although information processing is migrating continuously to digital domain, analog filters have still been found in wide range of applications as a medium connecting digital processors and analog signals often found in nature. This paper concentrates on functional emulation of high-order passive RLC ladder filters, which are well known for their low pass-band sensitivity to component variations and component spreads. There have been numerous developed methods to enjoy these benefits using Op-amp-RC and OTA-C circuits [1]. Among these methods, the signal flow graph (SFG) simulation has gained better popularity than the synthetic elements replacement as it shares the low sensitivity and low component spreads of the precedent RLC filters. Traditionally, the SFG simulation is based on a modeling of the circuit characteristic using voltage signals. However, interests in current-mode signal processing are substantially expanding since it possesses a large number of good properties such as low internal nodes impedance, which gives a potential to achieve a large bandwidth. As signals are represented by current, a much lower voltage is required as compared with the voltage-mode signal processing. This makes the current-mode circuits suitable for low voltage designs. Furthermore, summation and subtraction of signal currents can be directly performed at circuit nodes, resulting in a simple structure. Consequently, many suggestions of the current-mode active ladder filters employing multiple output OTAs and CCIIs have been published [2–4]. However, most of them showed the realizations of the simulated transfer function in rather complicated ways and do not possess the optimal or efficient employment of active and passive elements. Furthermore, the realization may not have a direct connection to the prototype RLC filters. Thus, the sensitivity may not be

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necessarily low. Recently, the linear transformation has been adopted to realize the active ladder filters with some good results [5,6]. But, complex synthesis equations as well as some external resistors are required. Moreover, the utilized frequency is fixed by their determined passive elements.

Rather than converting the whole network to a large SFG equivalent diagram, this paper shows an intuitive idea to divide the original ladder network into subsections, and then realize SFG of each subsection one by one. Hence the low sensitivity basis is guaranteed while reducing the complexity of a large SFG diagram. This proposed scheme possesses many advantages. First, the structure is very simple and easy to design including realization of the finite transmission zero. All capacitors are grounded and no external resistors are required, thereby saving chip area in IC implementation. In addition, each individual subsection SFG is simulated using the multi-output second generation current controlled conveyor (MCCCII), the tunable internal impedance of which can be utilized to electronically adjust the frequency characteristics of the filters. This will be useful to reconfigure the system or to compensate for component deviations using automatic tuning system in IC integration [7].

The next section briefly describes the current-mode ladder structure and the idea of individual component synthesis. An introduction to the multi-output current controlled conveyor and how to use it to implement each component of current-mode active filters using the proposed structure are discussed in Section 3. The circuit design of MCCCII is shown in Section 4. Section 5 explains some filter examples and their simulation results and Section 6 contains our conclusions.

2. Current-domain ladder component partitioning

The traditional SFG simulation technique emulates voltage–current relationships of all elements in the prototype ladder filters. For a large network, however, this appears to be a roundabout and impractical way [1]. In this paper, a new viewpoint has been proposed. The idea is based on a partitioning of a large network into individual basic sections. Consider a general doubly terminated lossless passive ladder network in Fig. 1. Such a network can be partitioned into two basic sections: shunt and series (as depicted in Figs. 2(a) and (b), respectively), the corresponding SFG equivalent block diagrams of which are shown in Figs. 2(c) and (d). The block diagram in Fig. 2(c) (and Fig. 2(d)) represents the output voltage (current) as a result of the product of the impedance (admittance) and the subtraction between corresponding current (voltage) of the previous and next stages. Therefore, the overall equivalent structure can be constructed by a proper cascading of these two equivalent branches. With these two basic operations, the branch relationships for the entire structure can be

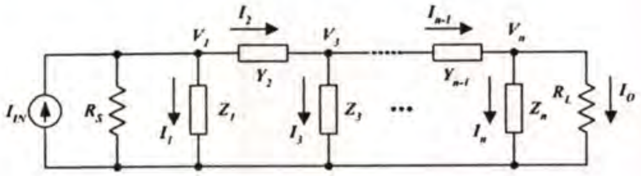


Fig. 1. General doubly terminated ladder network.

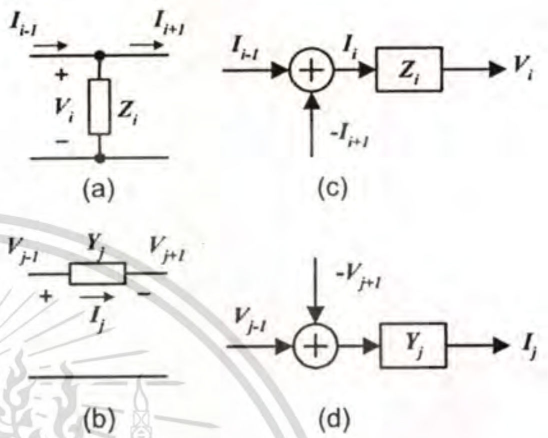


Fig. 2. Fundamental operations: (a) shunt branch, (b) equivalent shunt branch, (c) series branch, and (d) equivalent series branch.

rewritten in form of

$$\left.\begin{aligned} V_1 &= Z_1\left(I_{IN} - I_2 - \frac{V_1}{R_S}\right),\\ I_2 &= Y_2(V_1 - V_3),\\ V_3 &= Z_3(I_2 - I_4),\\ &\vdots\\ V_n &= Z_n(I_{n-1} - I_o),\\ I_o &= \frac{V_n}{R_L}. \end{aligned}\right\} \quad (1)$$

Since the summation or subtraction of current signals can be implemented at circuit nodes, converting all variables into current forms will lead to design simplicity. The conversion is simply performed by either normalizing or scaling the equations with resistance R_p. All relations in Eq. (1) are then transformed into their corresponding current transfer functions as

$$\left.\begin{aligned} \frac{V_1}{R_p} &= \frac{Z_1}{R_p}\left(I_{IN} - I_2 - \frac{V_1}{R_S}\right),\\ I_2 &= Y_2R_p\left(\frac{V_1}{R_p} - \frac{V_3}{R_p}\right),\\ \frac{V_3}{R_p} &= \frac{Z_3}{R_p}(I_2 - I_4),\\ &\vdots\\ \frac{V_n}{R_p} &= \frac{Z_n}{R_p}(I_{n-1} - I_o),\\ I_o &= \frac{R_p}{R_L}\frac{V_n}{R_p}. \end{aligned}\right\} \quad (2)$$

. Synthesis of branch elements using MCCCII

After the separated shunt and series portions have been reated for the prototype ladder network, they will be subequently implemented using the MCCCIIs. Each block of iem has two outputs: a positive output for the forward path nd a negative output for the feedback path. Finally, casading every portion of branches back together with proper onnections of the feed forward and feedback paths will reult in the complete equivalent circuit. This method is as asy as the synthetic element replacement, yet maintaining ie benefit of low sensitivity of the ladder structure.

.1. Characteristic of MCCCII

Typically, current conveyor has only one output current erminal, whose signal is available only once for each feedack path. Therefore, in multi-loop feedback topologies, vhich require several duplicated signals, multi-output conguration will gain more advantages. The equivalent circuit f MCCCII is shown in Fig. 3 and its port relations can be escribed by the following matrix equation:

$$\begin{bmatrix} \cdot I_Y \\ V_X \\ I_{+Z} \\ .I_{-Z} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & R_X & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_{+Z} \\ V_{-Z} \end{bmatrix}, \quad (3)$$

vhere R_X is an intrinsic resistance of the current input port : and it is possible to be controlled by varying the external ias current [8]. The equivalent MCCCII-based components or simulating the two fundamental operations in Fig. 2 and ie use of R_X as a tunable parameter fall into 3 categories amely (1) single passive element, (2) single passive element vith source or load resistor, and (3) double passive elements, etails of which will be described in the following sections.

.2. Simulation of single passive element

The first two basic single passive element frames: a shunt apacitor branch and a series inductor branch, are shown n Figs. 4(a) and (b), respectively. With all voltage signals ransformed into their current counterparts by a scaling reistance R_p as mentioned in Section 2, their voltage and urrent relations in form of current transfer functions can be hown as

$$\frac{V_i}{R_p} = \frac{1}{sC_iR_p}(I_{i-1} - I_{i+1}), \quad (4a)$$

$$_j = \frac{R_p}{sL_j}\left(\frac{V_{j-1}}{R_p} - \frac{V_{j+1}}{R_p}\right). \quad (4b)$$

)bviously, both equations represent an integrating function. lence, they can be simulated by an equivalent MCCCII

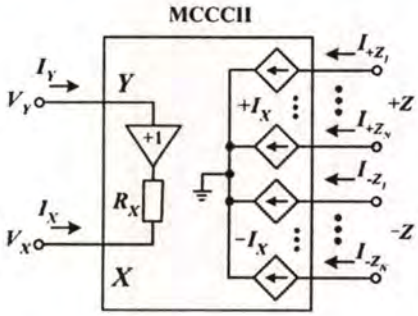


Fig. 3. Equivalent circuit of MCCCII.

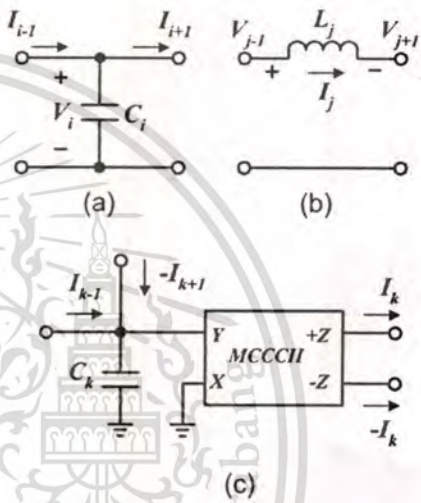


Fig. 4. Single element: (a) shunt C, (b) series L, (c) equivalent MCCCII structure.

integrator in Fig. 4(c), which has the current transfer function of

$$I_k = \frac{1}{sC_kR_X}(I_{k-1} - I_{k+1}). \quad (5)$$

Mapping the equivalent circuit to the shunt capacitor by letting $I_k = V_i/R_p$, $I_{k-1} = I_{i-1}$ and $I_{k+1} = I_{i+1}$ results in the design parameter $C_k = (C_iR_p)/R_X$. Similarly, the design parameter for the series inductor branch is $C_k = L_j/(R_pR_X)$, which is deduced from mapping the circuit variables $I_k = I_j$, $I_{k-1} = V_{j-1}/R_p$ and $I_{k+1} = V_{j+1}/R_p$. Since after the transformation, all variables are related to R_X, the adjustment of R_X will tune the corner frequency of the filters.

The shunt inductor and the series capacitor can be treated in the same way. For ease of reference, all single passive element syntheses are summarized and listed in Table 1.

3.3. Simulation of single passive element with source or load resistor

By using the same concept as in Section 3.2, all single passive element syntheses with a source resistor are summarized in Table 2. Notice that similar current transfer

Table 1. Single passive element syntheses

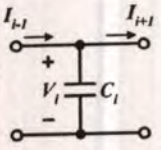
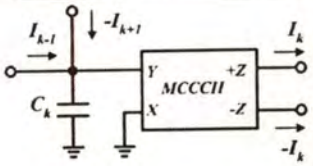
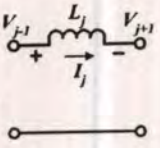
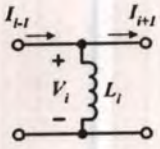
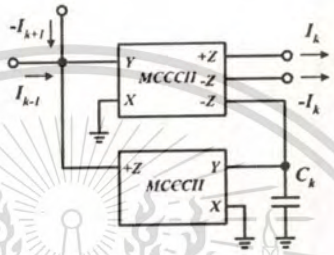
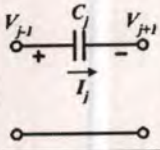
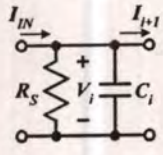
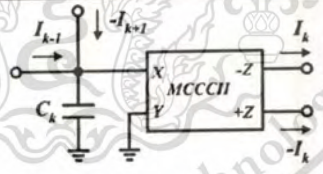
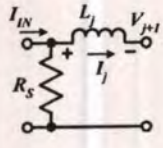
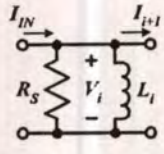
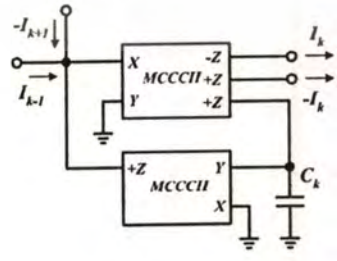
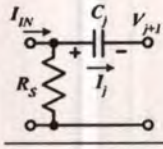
Passive elements	Voltage–current relations	MCCCII-based circuits	
	$\frac{V_i}{R_p} = \frac{1}{sC_iR_p}(I_{i-1} - I_{i+1})$		$C_k = (C_iR_p)/R_X$ for shunt C
	$I_j = \frac{R_p}{sL_j}\left(\frac{V_{j-1}}{R_p} - \frac{V_{j+1}}{R_p}\right)$	$I_k = \frac{1}{sC_kR_X}(I_{k-1} - I_{k+1})$	$C_k = L_j/(R_pR_X)$ for series L
	$\frac{V_i}{R_p} = \frac{sL_i}{R_p}(I_{i-1} - I_{i+1})$		$C_k = L_i/(R_pR_X)$ for shunt L
	$I_j = sC_jR_p\left(\frac{V_{j-1}}{R_p} - \frac{V_{j+1}}{R_p}\right)$	$I_k = sC_kR_X(I_{k-1} - I_{k+1})$	$C_k = (C_jR_p)/R_X$ for series C

Table 2. Single passive element syntheses with source or load resistor

Passive elements	Voltage–current relations	MCCCII-based circuits	
	$\frac{V_i}{R_S} = \frac{1}{sC_iR_S + 1}(I_{IN} - I_{i+1})$		$C_k = (C_iR_S)/R_X$ for shunt C
	$I_j = \frac{1}{s\frac{L_j}{R_S} + 1}\left(I_{IN} - \frac{V_{j+1}}{R_S}\right)$	$I_k = \frac{1}{sC_kR_X + 1}(I_{k-1} - I_{k+1})$	$C_k = L_j/(R_SR_X)$ for series L
	$\frac{V_i}{R_S} = \frac{s\frac{L_i}{R_S}}{s\frac{L_i}{R_S} + 1}(I_{IN} - I_{i+1})$		$C_k = L_i/(R_SR_X)$ for shunt L
	$I_j = \frac{sC_jR_S}{sC_jR_S + 1}\left(I_{IN} - \frac{V_{j+1}}{R_S}\right)$	$I_k = \frac{sC_kR_X}{sC_kR_X + 1}(I_{k-1} - I_{k+1})$	$C_k = (C_jR_S)/R_X$ for series C

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equations as in the single passive element can be obtained when choosing $R_S = R_p$. Again, mapping I_k, I_{k-1} and I_{k+1} of the MCCCII equivalent circuits to the passive branch elements result in the same design parameters $C_k = (C_i R_S)/R_X$ for the shunt capacitor and $C_k = L_j/(R_S R_X)$ for the series inductor. Note that it is also possible to realize these functions using an additional MCCCII connected as a resistor together with the circuits in Section 3.2 [9,10], but this will unnecessarily require some extra MCCCIIs. Comparing the circuits in Tables 1 and 2, the single passive elements with and without *source* resistor have nearly identical equivalent MCCCII circuits, except for a few different port arrangements of MCCCIIs. This is because we directly use R_X to simulate the *source* resistor and employ the potential of the multi-output structure.

Furthermore, it can be shown that single passive elements with a *load* resistor also share the same structures. However, we have to consider the input signals coming into the right-hand side of the passive RC/RL instead and the current I_{IN} is absent since load devices are considered. The equivalent MCCCII circuit remains unchanged, so does the design parameter C_k. This is also true for the rest of passive elements with either *source* or *load* resistor. Filter designs in Section 5 will clearly illustrate their usages in actual applications.

3.4. Simulation of double passive elements

Double LC passive elements, both with and without *source/load* resistor(s), can also be considered in a similar way as in the case of the single passive elements. Their results are shown in Table 3.

4. MCCCII implementation

4.1. Circuit description

The implementation of a current conveyor based on a complementary push–pull class-AB has gained popularity in many applications since its structure is as simple as a basic OTA but consumes less power [8]. Although the bipolar technologies provide higher gain, greater linearity and wider frequency bandwidth, CMOS technologies have been in wide spread use in almost all areas of applications when low power consumption, low cost and suitability for mixed analog/digital implementations, are of major concerns. A circuit schematic of a CMOS push–pull MCCCII is shown in Fig. 5. All transistors are biased to operate in saturation region. The multi-output topology can be easily implemented by appending additional output transistors to the current mirrors at port +Z and −Z as required.

4.2. Nonlinearity consideration

From the proposed MCCCII-based filter topology, there are two major circuit functions: voltage-to-current converter and current buffer. Nevertheless, both the Y-terminal-voltage-induced current and the input current that directly flows into the X-terminal have been nonlinearly divided into two paths flowing through the output NMOS and PMOS current mirrors, before they are duplicated and summed up again at the +Z and −Z outputs. Their transfer linearities can be shown in term of R_X. First, consider an input voltage applying to Y-terminal. This voltage will induce a current at the X-terminal, which in turn flow into the upper and lower transistors, M_2 and M_4, respectively. Assuming $K_1 = K_2 = K_N$, $K_3 = K_4 = K_P$, $V_{T1} = V_{T2} = V_{TN}$ and $V_{T3} = V_{T4} = V_{TP}$, we can write the following current relations:

$$i_{D2} = \begin{cases} I_B + 2v_Y\sqrt{K_N I_B} + K_N v_Y^2 & \text{for } v_Y > -\sqrt{\dfrac{I_B}{K_N}}, \\ 0 & \text{for } v_Y < -\sqrt{\dfrac{I_B}{K_N}}. \end{cases} \tag{6a}$$

$$i_{D4} = \begin{cases} I_B - 2v_Y\sqrt{K_P I_B} + K_P v_Y^2 & \text{for } v_Y < +\sqrt{\dfrac{I_B}{K_P}}, \\ 0 & \text{for } v_Y > +\sqrt{\dfrac{I_B}{K_P}}. \end{cases} \tag{6b}$$

where I_B is the bias current and MOSFET parameter $K_{N(P)} = \mu_{N(P)} C_{OX}(W/L)/2$. Combining these two branch currents in Eqs. (6a) and (6b) results in the total current flowing out of the X-terminal as

$$\begin{aligned} i_X &= i_{D2} - i_{D4} \\ &= 2\sqrt{I_B}(\sqrt{K_N} + \sqrt{K_P})v_Y + (K_N - K_P)v_Y^2. \end{aligned} \tag{7}$$

Note that the short transition to weak inversion before the complete transistor turn-off is neglected, as this current does not normally contribute to a large error in the total current in the X-terminal if the bias current I_B is sufficiently large. Then the X-terminal current could be a linear function of the Y-input voltage and we can consider R_X as a linear resistor of $1/4\sqrt{KI_B}\ \Omega$, as long as $K_N = K_P = K$ and $|i_X| < 4I_B$ are assumed [11]. This also implies that all transistors in the push–pull current conveyor will remain in saturation region until X-current signal is almost four times larger than the bias current I_B. Thus, its class-A operation range is nearly four times greater than a typical class-A current conveyor. This is also true for the input current directly flowing into the X-terminal in the current buffering operation. Eq. (7) is still valid with v_X replacing v_Y and the last parenthesis becomes $(K_P - K_N)$. The wide swing cascode current mirror has been chosen in order to minimize the current transfer error and raise the output impedance. The cascode transistor M_{P-cas} and M_{N-cas} help control the drain-source voltage,

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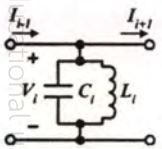
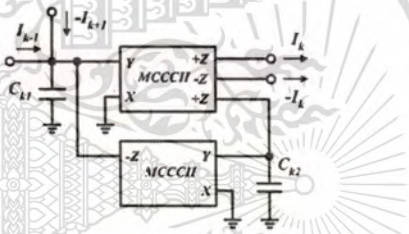
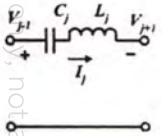
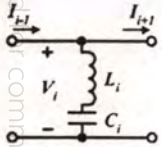
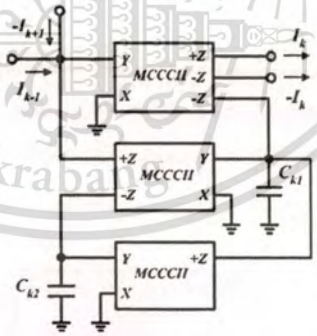
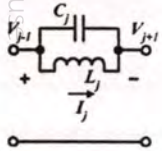
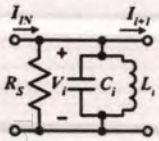
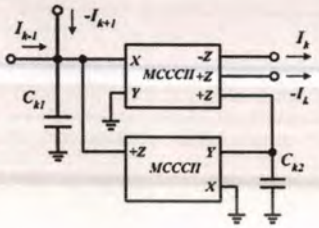
Table 3. Double passive element syntheses

Passive elements	Voltage–current relations	MCCCII-based circuits	
Double passive elements			
	$\frac{V_i}{R_p} = \frac{s\frac{L_i}{R_p}}{s^2 C_i R_p \frac{L_i}{R_p} + 1}(I_{i-1} - I_{i+1})$		$C_{k1} = (C_i R_p)/R_X$ $C_{k2} = L_i/(R_p R_X)$ for shunt parallel LC
	$I_j = \frac{sC_j R_p}{s^2 C_j R_p \frac{L_j}{R_p} + 1}\left(\frac{V_{j-1}}{R_p} - \frac{V_{j+1}}{R_p}\right)$	$I_k = \frac{sC_{k2}R_X}{s^2 C_{k1}C_{k2}R_X^2 + 1}(I_{k-1} - I_{k+1})$	$C_{k1} = L_j/(R_p R_X)$ $C_{k2} = (C_j R_p)/R_X$ for series series LC
	$\frac{V_i}{R_p} = \frac{s^2 C_i R_p \frac{L_i}{R_p} + 1}{sC_i R_p}(I_{i-1} - I_{i+1})$		$C_{k1} = L_i/(R_p R_X)$ $C_{k2} = (C_i R_p)/R_X$ for shunt series LC
	$I_j = \frac{s^2 C_j R_p \frac{L_j}{R_p} + 1}{s\frac{L_j}{R_p}}\left(\frac{V_{j-1}}{R_p} - \frac{V_{j+1}}{R_p}\right)$	$I_k = \frac{s^2 C_{k1}C_{k2}R_X^2 + 1}{sC_{k2}R_X}(I_{k-1} - I_{k+1})$	$C_{k1} = (C_j R_p)/R_X$ $C_{k2} = L_j/(R_p R_X)$ for series parallel LC

Double passive elements with source or load resistor

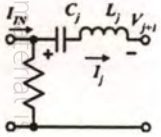


$$\frac{V_i}{R_S} = \frac{s\frac{L_i}{R_S}\cdot(I_{IN}-I_{i+1})}{s^2C_iR_S\frac{L_i}{R_S}+s\frac{L_i}{R_S}+1}$$



$$C_{k1} = (C_iR_S)/R_X$$

$$C_{k2} = L_i/(R_SR_X) \text{ for shunt parallel LC}$$

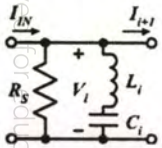


$$I_j = \frac{sC_jR_S\cdot\left(I_{IN}-\frac{V_{j+1}}{R_S}\right)}{s^2C_jR_S\frac{L_j}{R_S}+sC_jR_S+1}$$

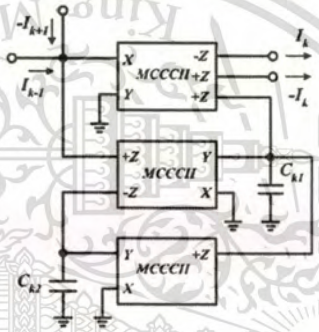
$$I_k = \frac{sC_{k2}R_X\cdot(I_{k-1}-I_{k+1})}{s^2C_{k1}C_{k2}R_X^2+sC_{k2}R_X+1}$$

$$C_{k1} = L_j/(R_SR_X)$$

$$C_{k2} = (C_jR_S)/R_X \text{ for series series LC}$$

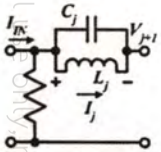


$$\frac{V_i}{R_S} = \frac{\left(s^2C_iR_S\frac{L_i}{R_S}+1\right)\cdot(I_{IN}-I_{i+1})}{s^2C_iR_S\frac{L_i}{R_S}+sC_iR_S+1}$$



$$C_{k1} = L_i/(R_SR_X)$$

$$C_{k2} = (C_iR_S)/R_X \text{ for shunt series LC}$$



$$I_j = \frac{\left(s^2C_jR_S\frac{L_j}{R_S}+1\right)\cdot\left(I_{IN}-\frac{V_{j+1}}{R_S}\right)}{s^2C_jR_S\frac{L_j}{R_S}+s\frac{L_j}{R_S}+1}$$

$$I_k = \frac{(s^2C_{k1}C_{k2}R_X^2+1)\cdot(I_{k-1}-I_{k+1})}{s^2C_{k1}C_{k2}R_X^2+sC_{k2}R_X+1}$$

$$C_{k1} = (C_jR_S)/R_X$$

$$C_{k2} = L_j/(R_SR_X) \text{ for series parallel LC}$$

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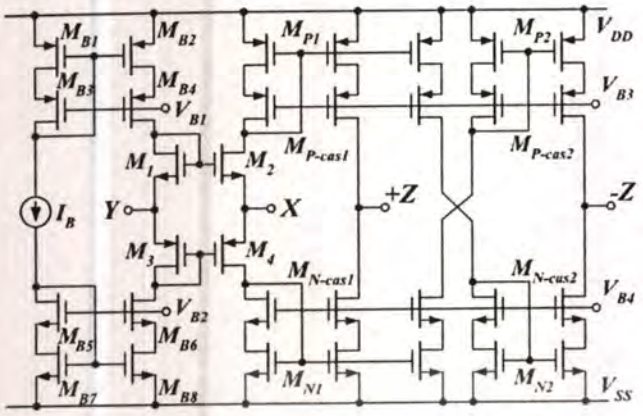

Fig. 5. Circuit schematic of a CMOS MCCCII.

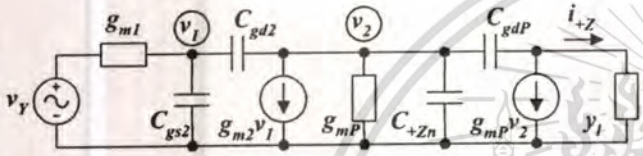

Fig. 6. Small-signal equivalent circuit of the upper half of MCCCII.

v_{DS}, between transistors within the current mirrors M_P and M_N. The difference of drain-source voltages between the mirror transistors is in the order of a few millivolts for a proper design, hence the distortion from the channel length modulation effect is insignificant.

4.3. Frequency limitation

The small-signal equivalent circuit of the upper half from Y-terminal to +Z-terminal of the MCCCII is presented in Fig. 6, assuming that the transistor output conductance g_{ds} is much smaller than the transconductance g_m and the conductance g_1 in the load admittance $y_1 = g_1 + sC_1$. For simplicity, all current mirrors are considered as simple MOS current mirrors since the cascode transistors barely contribute to the overall frequency response limitation. The capacitance C_{+Zn} consists of the gate-source capacitances C_{gsP} of the mirror transistors M_P and all other parasitic capacitances at node v_2, excluding the gate-drain capacitances C_{gd2} and C_{gdP}. Typically, the current mirror transistors usually have relatively large gate areas in order to minimize the current transfer error. Therefore, the gate-source capacitances are dominant and consequently the approximated C_{+Zn} can be determined as

$$C_{+Zn} \approx (n+2)C_{gsP} = (n+2)\tfrac{2}{3}C_{ox}W_P L_P, \tag{8}$$

where n is the number of output +Z ports and all mirror transistors have the same size. Note that the number $n+2$ in the parenthesis will become $n+1$ if there is no −Z-terminal.

Suppose that the gate-drain capacitances C_{gd} are far smaller than the capacitances C_{+Zn} and C_1, therefore the upper half v_Y-to-i_{+Z} transconductance function can be determined as

$$\left.\frac{i_{+Z}}{v_Y}\right|_{\text{upper half}} = g_{m2}\frac{\left(s\frac{C_{gd2}}{g_{m2}}-1\right)\left(s\frac{C_{gdP}}{g_{mP}}-1\right)}{\left(s\frac{C_{gs2}}{g_{m1}}+1\right)\left(s\frac{C_{+Zn}}{g_{mP}}+1\right)}. \tag{9}$$

The transfer function has two poles and two right half-plane (RHP) zeros. The first pole is the product of NMOS parameters that usually results in a much higher frequency than the second pole, which is originated from PMOS current mirror M_{P1} especially for the multi-output circuits. The RHP zeros do not contribute a great deal to the amplitude response near the corner frequency. Furthermore, the relatively insignificant Miller effect of C_{gd} can be reduced even further by incorporating the cascode transistors into the current-mirrors. Accordingly, we can assume the second pole as the dominant pole that limits the frequency response of the upper half circuit. Therefore, the corner frequency can be expressed as a function of device dimensions, number of +Z ports and bias current in form of

$$\omega_0 = \frac{3}{n+2}\sqrt{\frac{\mu_P I_B}{2C_{ox}W_P L_P^3}}. \tag{10}$$

The above equation shows a trade-off between bandwidth and number of ports. Therefore, the port numbers must be minimized in order to use in higher frequency applications. As the corner frequency strongly depends on the channel length, there is also a strong trade-off between bandwidth and gain accuracy as well as bandwidth and distortion.

The lower half circuit of +Z-terminal can be similarly derived. This will show a dominant pole at the current mirror M_{N1}. However, such a pole frequency is almost three times larger due to the greater mobility of NMOS over PMOS. The frequency response of the −Z-terminal will have the additional poles and RHP zeros due to the current mirrors M_{P2} and M_{N2}. Therefore, the number of −Z ports must be reduced as much as possible in order to prevent further limitation on the operating frequency.

5. Filter designs and simulation results

The performance of filters designed by using the proposed methodology has been examined through HSPICE circuit simulator using AMIS 0.5-μm level 49 CMOS model. For the MCCCII circuit in Fig. 5, the aspect ratio of all transistors are listed in Table 4. The bias current I_B is set to 50 μA under the voltage supply of $V_{sup} = \pm 2.0$ V. The simulated open-loop transconductance gain (g_m) and 3-dB cutoff bandwidth are 0.53 mA/V and 183 MHz, respectively, when using the dual output MCCCII as a transconductance cell.

Table 4. W/L area of MOS in MCCCII circuit

Transistors	W/L	Transistors	W/L
M_1, M_2	5/0.5	M_3, M_4	18.5/0.5
M_{B1}, M_{B2}	90/2	M_{B3}, M_{B4}	90/0.5
M_{B5}, M_{B6}	30/2	M_{B7}, M_{B8}	30/0.5
M_P	60/1	M_{P-cas}	100/1
M_N	60/1	M_{N-cas}	50/1

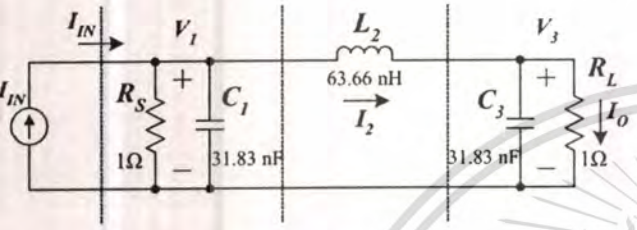

Fig. 7. Prototype current-mode 3rd-order Butterworth low-pass RLC ladder filter.

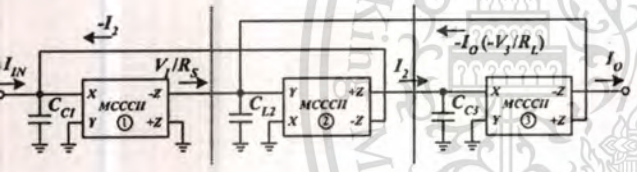

Fig. 8. MCCCIIs-based current-mode 3rd-order Butterworth low-pass filter.

A current-mode third-order Butterworth low-pass ladder filter in Fig. 7 is adopted as the first design example. From the prototype passive filter, we can easily divide it into three sections of branch elements, comprising with the first shunt capacitor with the source resistor, the second series inductor and the third shunt capacitor with the load resistor. Refer to Table 2 for implementing the shunt capacitor with source and load resistors and Table 1 for the series inductor. The final equivalent MCCCII-based circuit is shown in Fig. 8. Obviously, only three MCCCIIs and three grounded capacitors are needed for realizing the third-order filter. It can be concluded that merely n MCCCIIs and n capacitors are required for the nth-order all-pole low-pass filters implementation with no requirement of external resistors. Therefore, this structure delivers a truly minimum requirement of active and passive components.

To picture out the feasibility of the proposed technique, the filter has been designed with the cutoff frequency $f_{-3\,dB}$ of 5 MHz. Refer to Tables 1 and 2 for the design parameters C_k. Let $R_p = R_S = 1\,\Omega$ for simplicity and MCCCII $R_X(1/g_m)$ of 1887 Ω, the capacitor values become $C_{C1} = C_{C3} = 17.506$ pF and $C_{L2} = 35.013$ pF. The simulated frequency responses of the designed circuit and the prototype RLC filter are shown together in Fig. 9. The tuning ability is performed by varying bias current to 12.5 and 200 μA. The corner frequencies are 2.65, 5.09 and 9.34 MHz relating to the calculated frequencies of 2.5, 5 and 10 MHz, respectively. The frequency accuracy is within about 6%. The proposed structure shows almost identical characteristic with the passive prototype filter before the signals begin to deviate at frequency beyond 100 MHz due to the frequency limitation of the MCCCIIs.

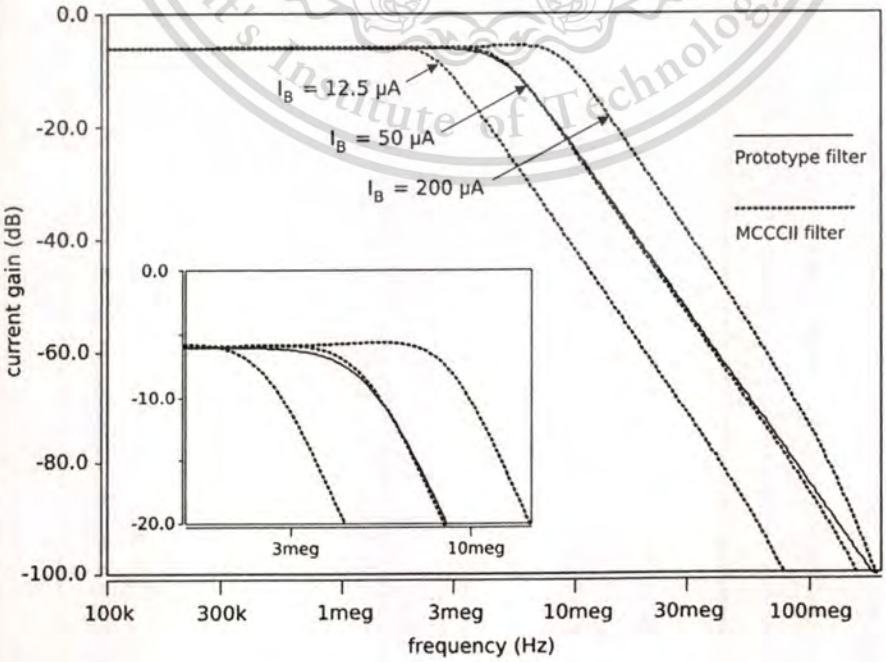

Fig. 9. Simulated frequency response of the 3rd-order Butterworth low-pass filter.

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Filters including transmission zeroes like a third-order elliptic low-pass filter in Fig. 10 is also possible to be separated into three sections. By using the circuits in Table 3 for implementing the middle parallel LC elements while the first and the last blocks are, again, adopted from Table 2, the complete equivalent filter using only MCCCIIs and grounded capacitors is shown in Fig. 11. The prototype corner frequency has been selected to be 1 MHz with 1 dB pass band ripple and 40 dB stop band attenuation. The simulated frequency responses are depicted in Fig. 12. The large variation of MCCCIIs-filter in high frequencies is noticed. This comes from the frequency restriction of the multi-output current controlled conveyor especially the second current conveyor with three output ports, as predicted in Section 4.3. Note that the notch position is not as deep as in the prototype filter due to the limitation of quality factor of simulated LC components.

Because this proposed technique derives each element with one-by-one replacement concept, it is possible to separate the floating capacitor C_2 from the passive filter in Fig. 10 and then realize the canonical MCCCII-based all-pole low-pass ladder filter first. After that, adding the scaled capacitor C_2 to the synthesized circuit at the corresponding node will result in a circuit shown in Fig. 13. Simulated frequency responses of the floating capacitor MCCCIIs-based filter is shown in Fig. 14. It is clearly seen that a better performance than the previous circuit using only grounded

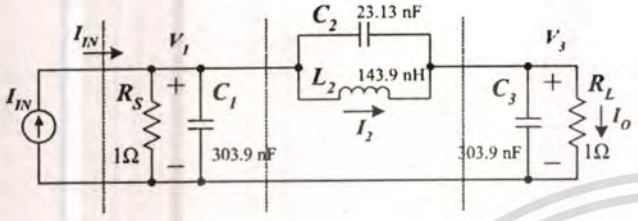

Fig. 10. Prototype current-mode 3rd-order elliptic low-pass RLC ladder filter.

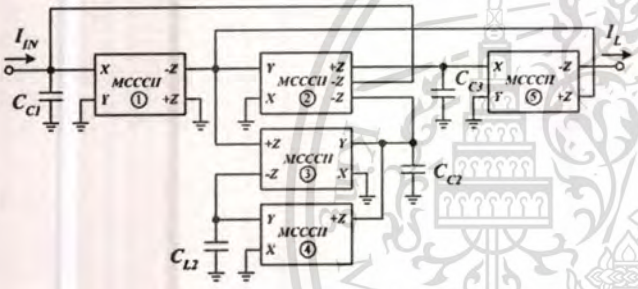

Fig. 11. MCCCIIs and only grounded capacitor current-mode 3rd-order elliptic low-pass filter.

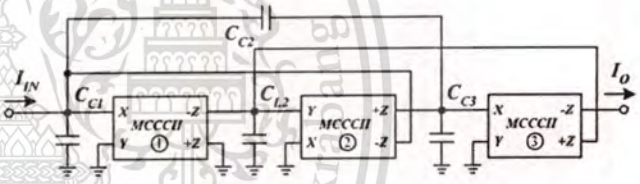

Fig. 13. MCCCIIs and floating capacitor current-mode 3rd-order elliptic low-pass filter.

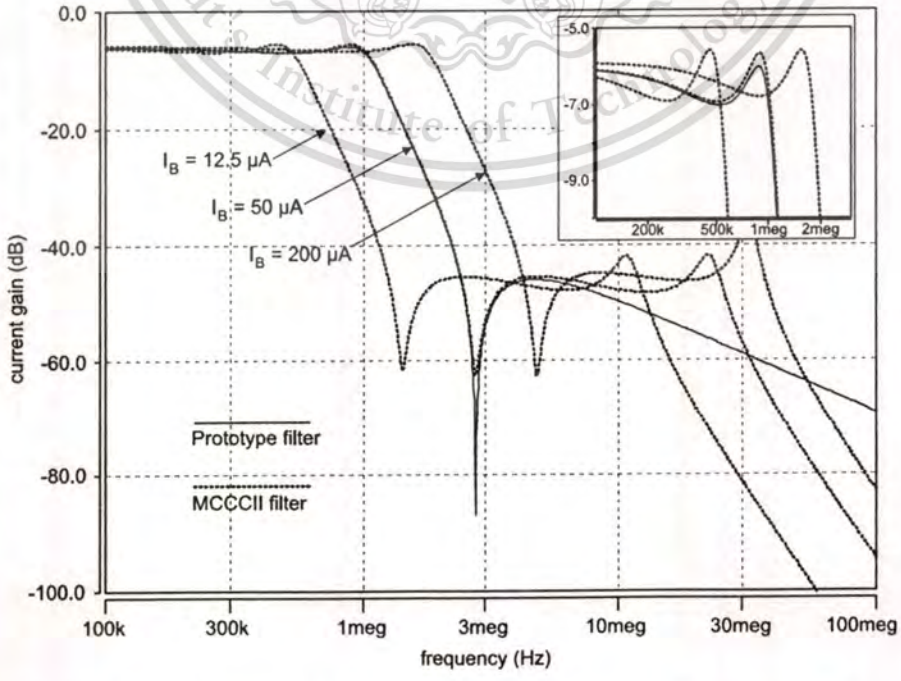

Fig. 12. Simulated frequency response of the grounded capacitor elliptic low-pass filter.

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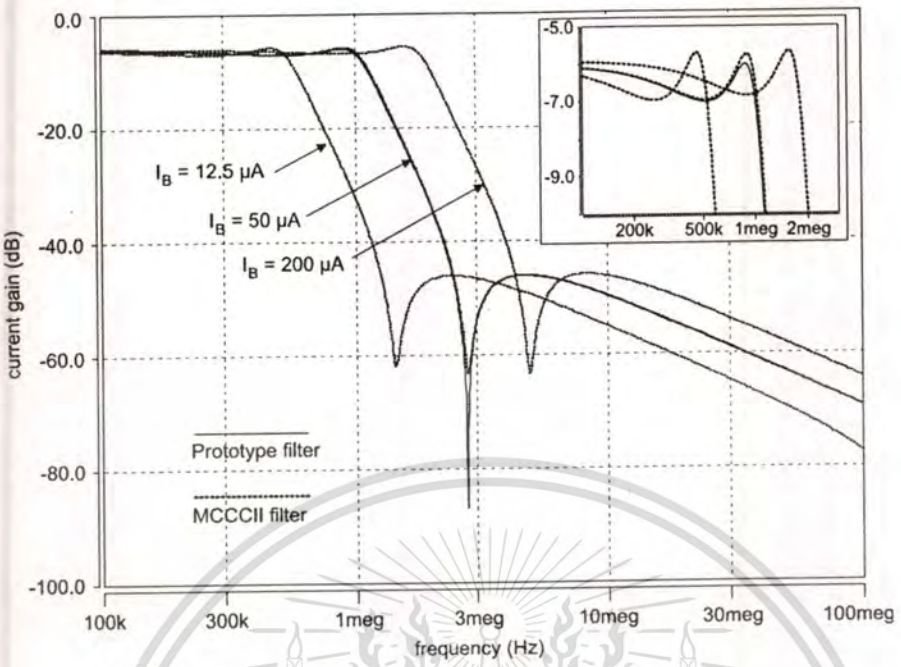

Fig. 14. Simulated frequency response of the floating capacitor elliptic low-pass filter.

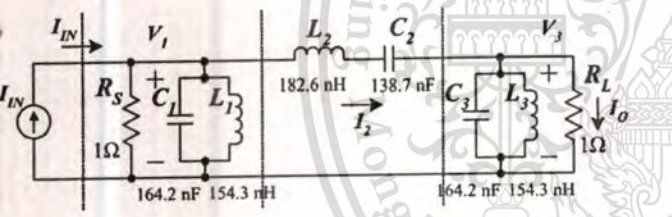

Fig. 15. Prototype current-mode 6th-order Chebyshev band-pass RLC ladder filter.

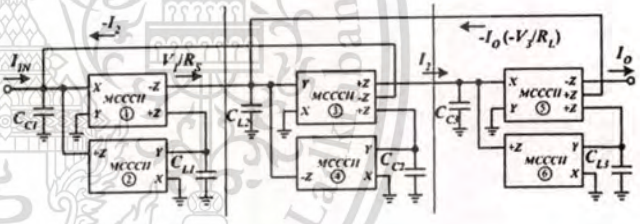

Fig. 16. MCCCIIs and only grounded capacitor current-mode 6th-order Chebyshev band-pass filter.

capacitors is achieved. It is worth noting that the peaking magnitude at the corner frequency due to phase lag is also smaller by 0.2 dB comparing to Fig. 12. This is because the use of low frequency three output ports MCCCII is avoided. Furthermore, this structure has the filter capacitances presented at all nodes and is suitable for high frequency operation. Therefore, this solution is preferable for realizing the elliptic filters when the floating capacitor is permitted.

The last example is a sixth-order Chebyshev band-pass filter shown in Fig. 15 with 1 MHz center frequency and 1 MHz bandwidth. Its three branch sections are all listed in Table 3. The complete MCCCII-based band-pass filter appearing in Fig. 16 has the frequency response as shown in Fig. 17. There is a noticeable peaking due to the Q-enhancement effect. Since every separated section can be tuned electronically, incorporating a suitable Q-control circuit will help adjust the filter to the desired center frequency [7].

6. Conclusions

The current-mode ladder filter synthesis using multi-output current controlled conveyors has been proposed. The design method is very simple and covers all types of precedent passive LC ladder filters. This technique requires the minimum number for both passive and active components. There are only n MCCCIIs needed for realizing the nth-order all-pole filter and elliptic low-pass filter with an absence of the external resistor provided that floating capacitors are permitted. However, $2n - 1$ and $2n - 2$ MCCCIIs are required to achieve odd and even nth-order elliptic filters, respectively, when implementing with only grounded capacitors. The characteristic frequency can be tuned electronically by controlling the bias current of MCCCIIs. Third-order Butterworth and elliptic low-pass filter and sixth Chebyshev band-pass filter were chosen as design examples. HSPICE simulation results yield good agreement with the theoretical expectation.

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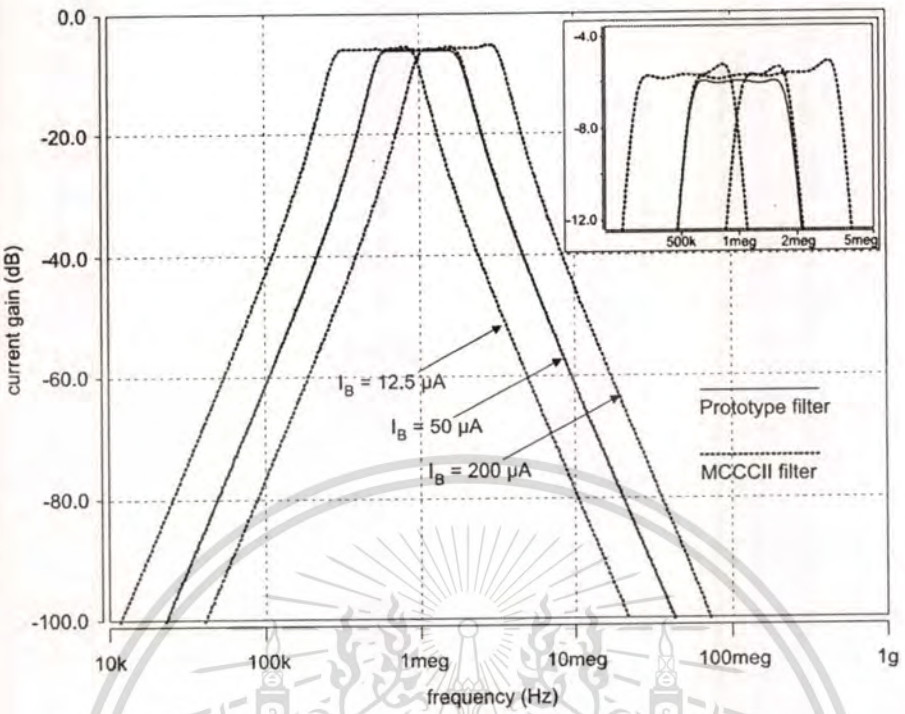

Fig. 17. Simulated frequency response of the Chebyshev band-pass filter.

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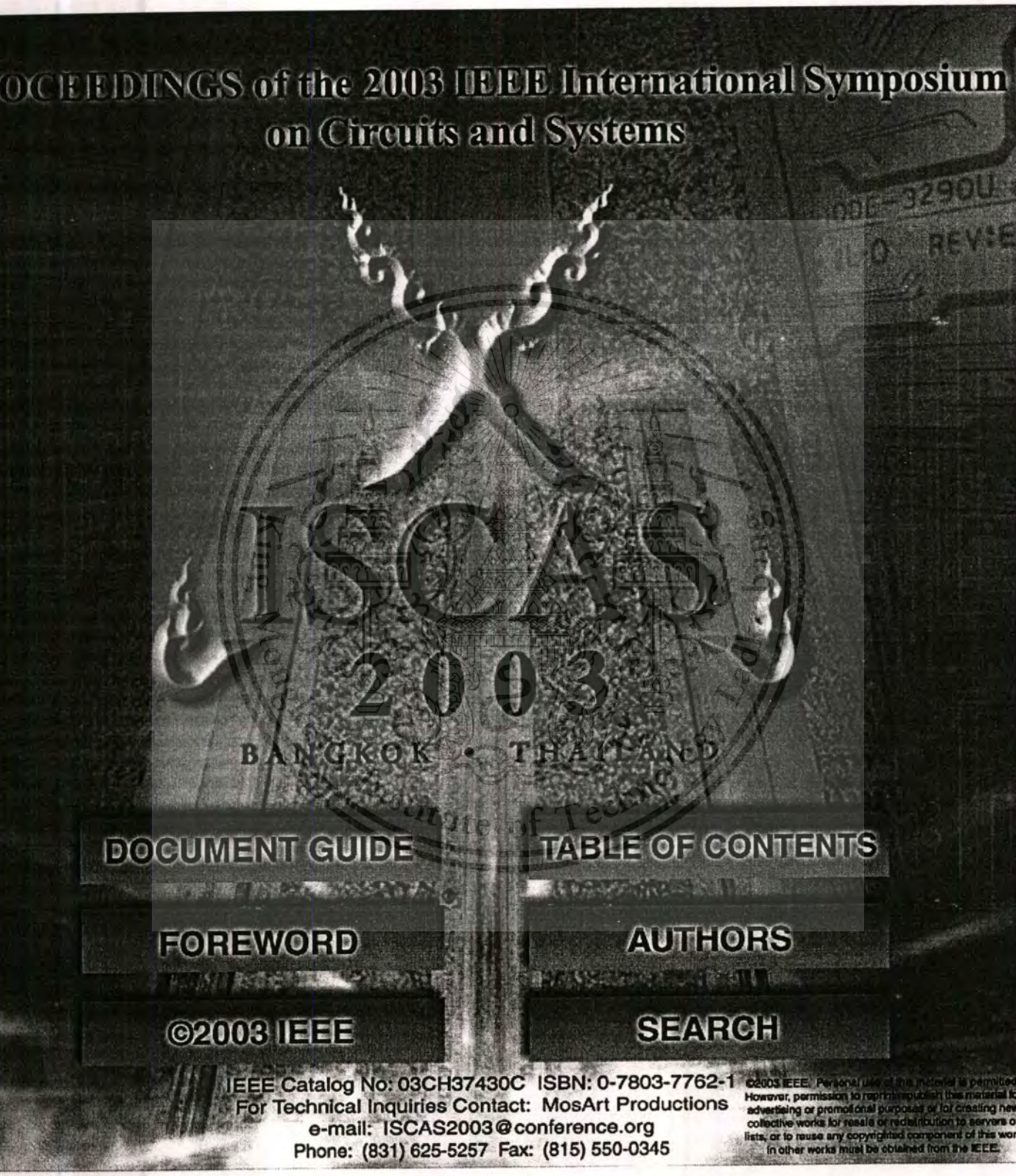
Dr. Surakampontorn received the Outstanding Scientist of Thailand Award in 1996 and The National Award for Distinguished Researcher, Thailand, in 1998. He is a Senior Member of the IEEE and is a Member of the IEICE.



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REALIZATION OF ELECTRONICALLY TUNABLE LADDER FILTERS USING MULTI-OUTPUT CURRENT CONTROLLED CONVEYORS

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ABSTRACT

A systematic realization of continuous-time current-mode ladder filter using multi-output second generation current controlled conveyor (MCCCII) has been presented. The proposed technique is based on leapfrog simulation of RLC ladder filter using only MCCCIIs and capacitors that lead to simple structure, easy to design and suitable for IC fabrication. A fifth-order Butterworth low-pass filter and a sixth-order Chebyshev band-pass filter which retain a minimum requirement of passive elements and have an advantage of electronically tunable will be introduced. The feasibility of realization strategy is confirmed through HSPICE circuit simulations.

1. INTRODUCTION

Double terminated passive RLC ladder filters are well known on having an inherent advantage over active filter in terms of their sensitivity to component tolerances. There are several methods to extract this benefit from the prototype passive filter using the op-amp-based RC-active and OTA-C-based circuits [1]. The leapfrog structure seem to receive more popular due to it share all the low sensitivity characteristic and low component spread of the precedent RLC filter. Traditionally, the simulation is based on modeling all circuit equations as voltage signals [1]. Recently, current-mode signal processing has been received substantial consideration owing to its higher performance properties. Consequently, many suggestions of current-mode leapfrog ladder filter had been published employing OTAs [2] and CCIIs [3] as the active building blocks. However, all of them are established from simulating the operation of the ladder by mean of realizing the transfer function, which require a lot of active and passive elements and sometime the sensitivity may not necessitate being low. In very recent, the implementation of leapfrog filter using current differential buffered amplifies or CDBAs has been proposed [4], which can perform high frequency and low voltage supply operation. This scheme can simplify the signal flow graph of leapfrog filter and then realize each circuit element one by one, hence the low sensitivity basis is promised. Unfortunately, several floating resistors are required for voltage to current conversion and the utilized frequency is exactly fixed by determined passive elements.

This paper follows the idea of realizing the voltage-current relationships of each element corresponding to the prototype RLC filters one by one. Current controlled conveyor is chosen to function as a V-to-I converter cell regenerating all voltage parameter into current form. This proposed scheme possesses many advantages. Firstly, the structure is very simple and easy to design. No any external resister is required, which can safe the area in case of fabricating in a silicon chip. Moreover, the center frequency can be tuned electronically by adjusting the bias current of MCCCIIs. This will be useful in redeeming when the values of passive devices are deviated; including changing the system's characteristic is also very comfortable.

2. CURRENT CONTROLLED CONVEYOR

Second generation current conveyors (CCIIs) have found useful applications especially in current-mode world. Based on a complementary translinear loop, the current conveyor will be possible to operate at high frequency in class AB. In addition, the translinear current conveyor has a structure as simple as basic OTA but take less power consumption [5]. Despite this, it has only one output terminal and a current signal is available only once for each signal feed back. Therefore, in the multi-loop feedback path topology like leapfrog, multi-output characteristic seem to play an important role. The circuit symbol of multi-output current controlled conveyor is shown in figure1, which has both positive output terminal represented by $+Z$ and negative output terminal by -Z.

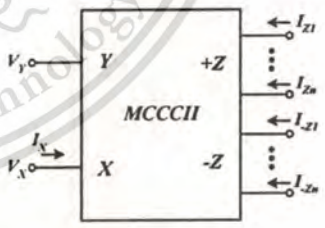

Figure 1. Circuit symbol of MCCCII

The schematic implementation of BiCMOS translinear MCCCII is shown in figure 2, which the ports relation can be described by the following matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_{+Z} \\ I_{-Z} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & R_X & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \times \begin{bmatrix} V_Y \\ I_X \\ V_{+Z} \\ V_{-Z} \end{bmatrix} \quad (1)$$

where $R_X = V_T/2I_{BI}$ is an intrinsic small signal resistance of the equivalent voltage follower. It is possible to control R_X by

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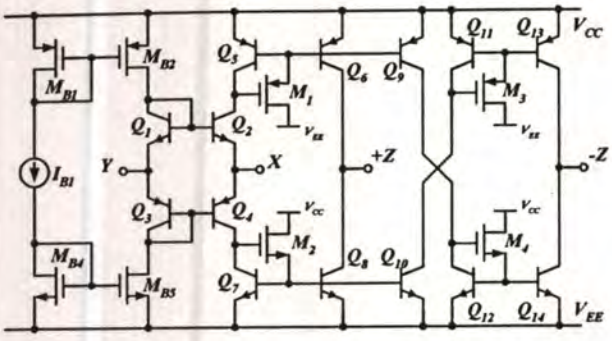

Figure 2. BiCMOS implementation of MCCCII

varying the bias current I_{B1}. Note that since the main contribution in noise is coming from current mirrors, the employment of MOS transistors in the biasing circuit is to minimize noise [5]. The multi-output topology can be easily implemented by adding the further output transistors. MOS transistors, M_1-M_4, are used to supply base current to all output transistors for accurate current transfer.

3. FILTER DESIGN METHODOLOGY

In order to develop the simulation procedure, consider the general ladder structure in figure 3. Here we focus on the realizing of the doubly terminated RLC filter. The characteristic of this structure can be expressed as following:

$$
\begin{aligned}
I_1 &= I_S - \frac{V_1}{R_S} - I_2, \\
V_1 &= Z_1 I_1, \\
I_2 &= Y_2 (V_1 - V_3), \\
V_3 &= Z_3 (I_2 - I_4), \\
&\vdots
\end{aligned}
$$

and

$$
\begin{aligned}
I_{n-1} &= Y_{n-1} (V_{n-2} - V_n), \\
V_n &= Z_n (I_{n-1} - I_O)
\end{aligned}
\qquad (2)
$$

where Z_i and Y_i stand for the impedance and admittance, respectively. These equations can be represented with block diagram in form of leapfrog structure as shown in figure 4. It can be observed that the diagram comprises of 2 operations, current to voltage and voltage to current conversion, as sketched in figure 5(a) and 5(c). Then if we convert the variables to be processed in only one type, the current variable, the execution would be simpler and ease in design. As seen in figure 5(b) and 5(d), with transforming all voltage to its current counterpart using MCCCIIs, these two operators can then be implemented using the same circuit. It should be noted that R_X is intrinsic resistance at port X of MCCCII introduced in the previous section. Since after the transformation, all variables are related to R_X, altering on R_X can also varying the characteristic of the filter that is the key of electronically tunable property.

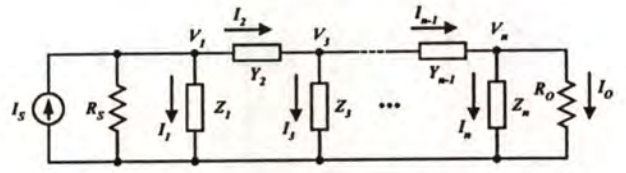

Figure 3. General doubly terminated ladder network

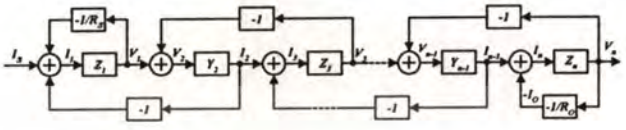

Figure 4. Block diagram redrawn from figure 3

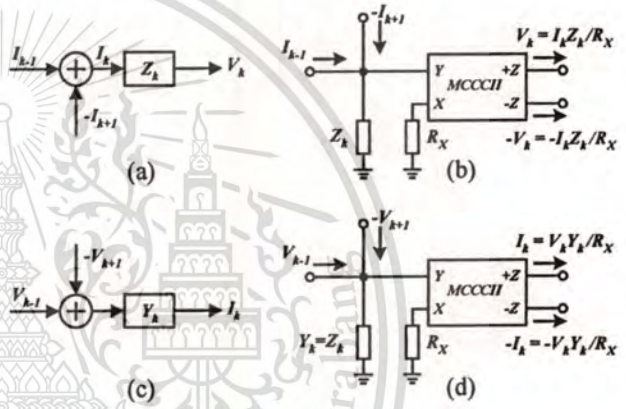

Figure 5. Basic blocks and the realization using MCCCIIs

A current-mode fifth-order Butter-worth low-pass RLC ladder filter shown in figure 6 is adopted as an example and the consequent circuit is shown in figure 7. It comprises of the minimum requirement of MCCCIIs and capacitors. As it is clearly seen that only five MCCCIIs and five capacitors are needed for realizing the fifth-order filter. There is no obligation of any external resistor, even the terminated resistor, R_S and R_O, are also implementing using MCCCIIs. Not only the attempt to eliminate the passive components, it is the necessary for tuning center frequency feature. Then, in general, merely $n+2$ MCCCIIs and n capacitors are required for the n^{th}-order filters implementation. Furthermore, this composition has several high impedance outputs, which allow to be easily cascaded without any additional matching circuits.

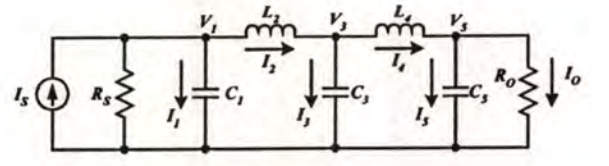

Figure 6. Prototype current-mode fifth-order Butterworth low-pass RLC ladder filter

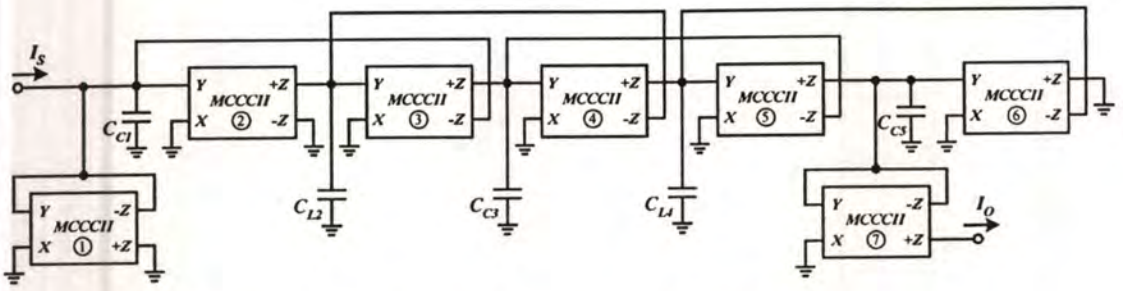

Figure 7. Current-mode tunable fifth-order Butterworth low-pass filter using MCCCIIs

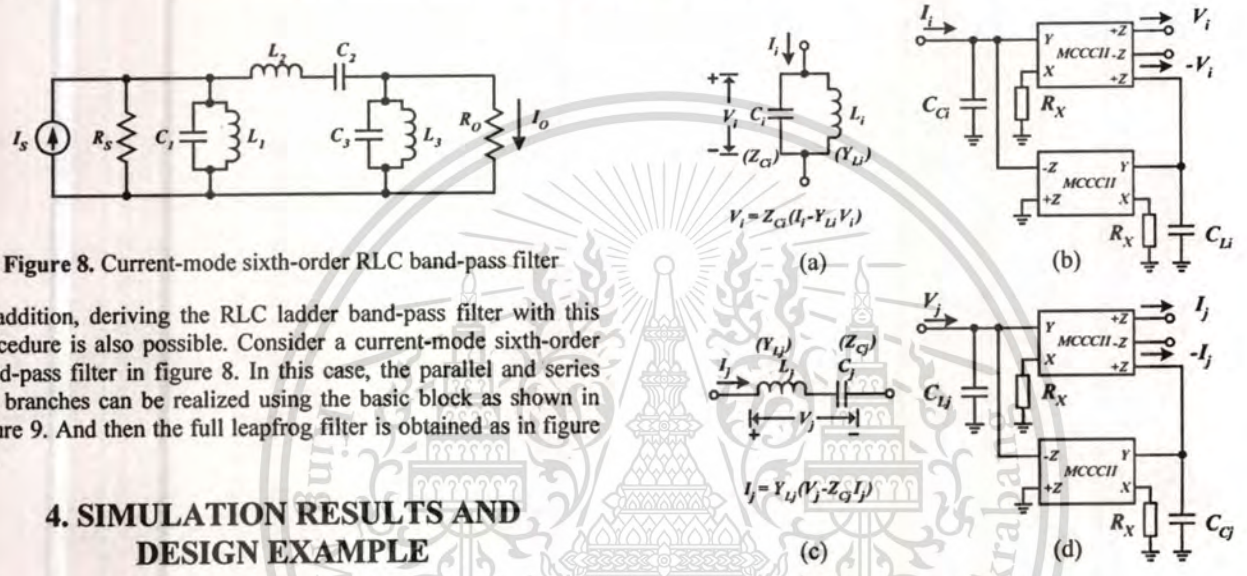

Figure 8. Current-mode sixth-order RLC band-pass filter

In addition, deriving the RLC ladder band-pass filter with this procedure is also possible. Consider a current-mode sixth-order band-pass filter in figure 8. In this case, the parallel and series LC branches can be realized using the basic block as shown in figure 9. And then the full leapfrog filter is obtained as in figure 10.

4. SIMULATION RESULTS AND DESIGN EXAMPLE

The performance of the proposed filter is verified through HSPICE circuit simulation based on 0.8-μm BiCMOS process technology supplied by AMS. The emitter areas for bipolar transistors are all equaled while set the W/L ratio of CMOS bias circuit, M_{b1} - M_{b4}, to 10μm/1μm and current mirror CMOS transistors, M_1 - M_4, to 5μm/1μm. The bias current is set to I_{B1} = 100 μA under the voltage supply of ±V = ±2 V. The basic characteristics of the MCCCII as a transconductance cell are listed in table1.

To picture out the feasibility of the proposed filter technique, a current-mode fifth-order Butterworth low-pass filter has been designed with a half-power frequency ω_{-3dB} of 100 Mrad/s (15.9 MHz). The terminated resistances are chosen to 1 Ω in prototype RLC filter. Then after scaling with MCCCII's intrinsic resistance

Figure 9. Basic blocks of filter in fig. 8 using MCCCIIs

Table1. Transconductance cell characteristic of MCCCII

Parameter	Simulated val.	Unit
Open loop G_m	5	mA/V
-3 dB Bandwidth	306	MHz
Input resistance	5.72	kΩ
Output resistance	140	kΩ

R_X ($1/G_m$), the capacitances' values are C_{C1} = C_{C5} = 30.9 pF, C_{L2} = C_{L4} = 80.9 pF and C_{C3} = 100 pF. The simulated frequency

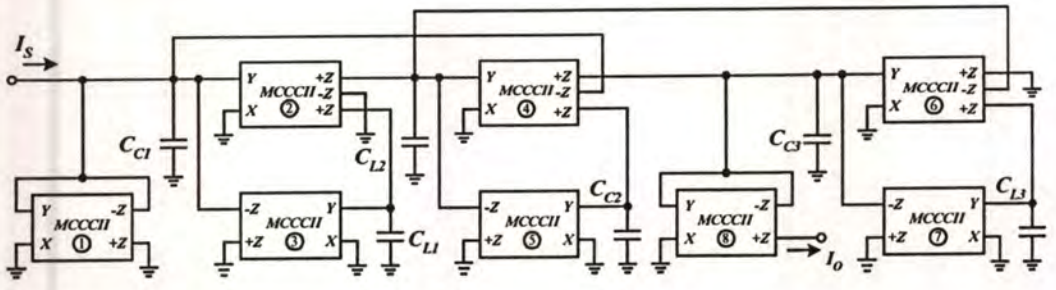

Figure 10. Current-mode sixth-order Chebyshev band-pass filter using MCCCIIs

esponse of the designed circuit and prototype RLC filter are ompared in figure 11. Tuning ability is also simulated and hown in figure 12 by varying bias current to 25 μA and 400 μA.

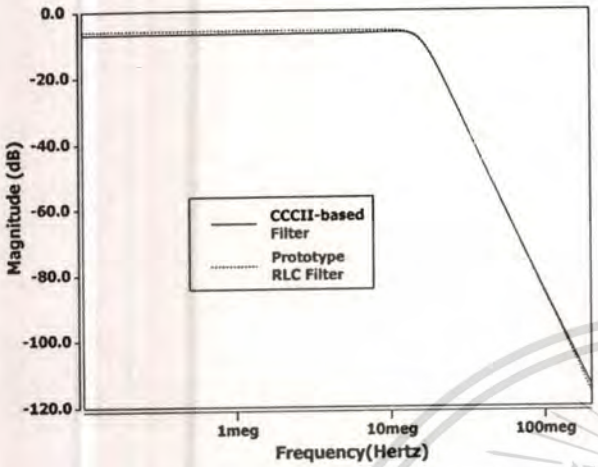

Figure 11. Simulated frequency response of the fifth-order low-pass filter

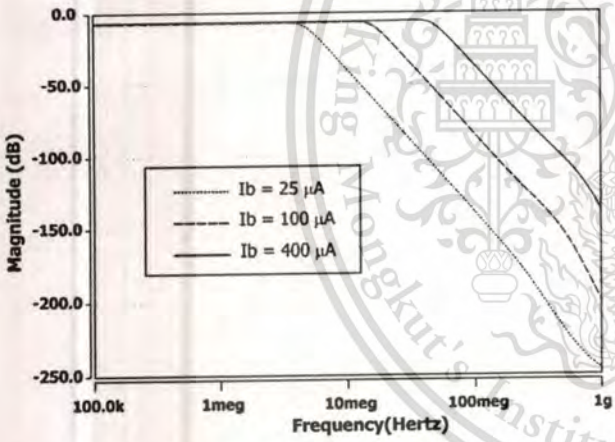

Figure 12. Simulated response of tuning cutoff frequency

A sixth-order Chebyshev band-pass filter deriving from RLC grouping as shown in figure 8 has been designed as well with the center frequency of 100 Mrad/s (15.9 MHz). The passive components are set to $C_{C1} = C_{C3} = 114.5$ pF, $C_{L1} = C_{L3} = 21.8$ pF, $C_{C2} = 19.6$ pF and $C_{L2} = 127.5$ pF. Adjust the bias current to 10 μA and 30 μA as the example of tunable ability. The simulated results are shown in figure 13.

It can be observed the well agreement with the passive prototype in low-pass filter implementation. However, there are some deviations in realizing band-pass filter especially in the higher frequency range. This is due to the conversion resistance R_X is not pure resistance but combined from both RLC, since the simulation using ideal MCCCII with genuine R_X have the exact response to the passive filter one as shown in dash line of figure 13. The high frequency compensation can be worked out to improve the efficiency in the future work.

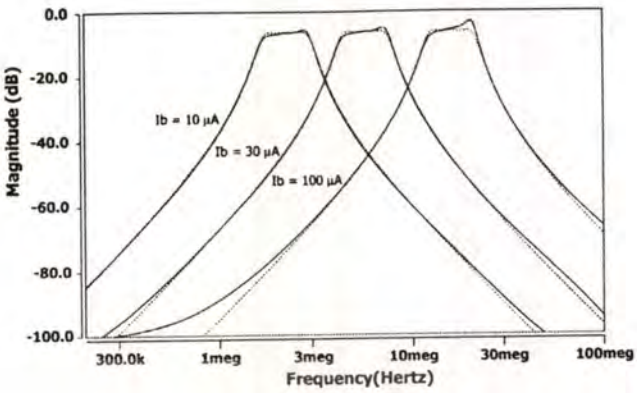

Figure 13. Simulated frequency response of tuning the sixth-order band-pass filter

5. SUMMARY

A realization of leapfrog ladder filter using multi-output current controlled conveyor is proposed. The design strategy is very simple and requires the minimum passive components. The center frequency can be tuned electronically by controlling the bias current of current conveyor, which is very helpful in compensating unmatched components as well as varying the characteristic without changing any device. Fifth-order Butterworth low-pass filter and sixth-order Chebyshev band-pass filter are derived as examples. HSPICE simulation results give a good agreement with the theoretical expectation. Nevertheless, the frequency compensation should be done on implementing current conveyor for serving the filters' responses much more perfect.

6. ACKNOWLEDGEMENT

The first author would like to thank Mr. Worapong Tangsirat for useful discussions on ladder filter design. This work is partly funded by the Thailand Research Fund (TRF) under the Senior Research Scholar Program grant number RTA/04/2543. The support provided by the Japan International Cooperation Agency (JICA) is also acknowledged.

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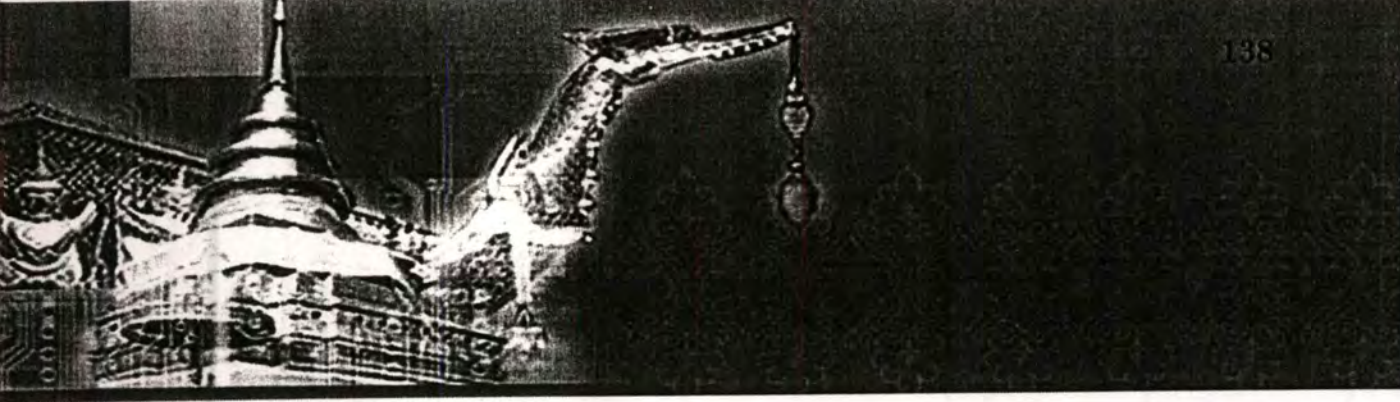

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TUNABLE ELLIPTIC FILTERS USING MULTI-OUTPUT CURRENT CONTROLLED CONVEYORS

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ABSTRACT

The circuit topologies are proposed for realizing the continuous time current-mode ladder filter of any order. The derived technique is based on the attractive features of the leapfrog simulation implementing using only multi-output second generation current controlled conveyor (MCCCII) and grounded capacitors that lead to simple structure, easy to design and suitable for IC fabrication. An example of the third-order elliptic low-pass filter which retains a minimum requirement of passive and active elements, as well as, possess the advantage of electronically tunable in cut-off frequency has been introduced. Moreover, this method can also be implemented by adding floating capacitors to the relative all-pole filter. Simulation results are provided to compare against the prototype passive RLC filter.

1. INTRODUCTION

Double terminated passive RLC ladder filters have received well acceptance on their inherent advantage over active filter in terms of insensibility to component tolerances. Many methods are developed to extract this benefit from the prototype passive filter using the op-amp-based RC-active and OTA-C-based circuits [1]. Among these procedures, the leapfrog structure seem to have being more popular and welcome than the synthetic elements replacement techniques due to it share all the low sensitivity nature and low component spread of the prototype RLC filter. Traditionally, the simulation is based on modeling all circuit equations as voltage signals [1], however, interest in current-mode signal processing has been growing due to the fact that it possesses many good properties i.e. retain low impedance internal node; therefore, achieve larger bandwidth, require low voltage swing that suit for low supply voltage operation, and perform summing of current signal at a circuit node result in simplicity structure. Consequently, many suggestions of current-mode leapfrog ladder filter had been published employing multiple output OTAs [2] and CCIIs [3] as the active building blocks. All of them are established from simulating the operation of the ladder by mean of realizing the transfer function, which require a lot of active and passive elements and sometime the sensitivity may not necessitate being low.

In recent, linear transformation is acquired to realized active ladder filters with good results [4], but this method requires many math equations and the utilized frequency is exactly fixed by determined passive elements. On the other hand, the implementation of leapfrog filter using current differential buffered amplifies or CDBAs [5], which perform high frequency and low voltage supply operation, can simplify the signal flow graph of leapfrog filter and then realize each element one by one, hence the low sensitivity basis is promised. Unfortunately, several floating resistors are needed for voltage to current conversion and frequency also can't be tuned. Moreover, it has found hard time in implementing transmission zero.

This paper follows the idea of realizing the voltage-current relationships of each element corresponding to the prototype RLC filters one by one. Current controlled conveyor is chosen to function as a V-to-I converter cell regenerating all voltage parameter into current form. This proposed scheme possesses many advantages. Firstly, the structure is very simple and easy to design including realization of the transmission zero. No any external resister is required and all capacitors are grounded, which can safe area in case of fabrication. Moreover, the cut-off frequency can be tuned electronically by adjusting the bias current of MCCCIIs that is useful in redeeming when the values of passive devices are deviated; including changing the system's characteristic is also very comfortable.

2. PRINCIPLE OF LEAPFROG FILTER

Consider the general ladder structure in figure 1. Here we focus on the realizing of the doubly terminated RLC filter. The characteristic of this structure can be expressed as following:

$$\begin{aligned} I_1 &= I_S - \frac{V_1}{R_S} - I_2 \quad , \\ V_1 &= Z_1 I_1 \quad , \\ I_2 &= Y_2(V_1 - V_3) \quad , \\ &\vdots \\ \text{and} & \\ I_{n-1} &= Y_{n-1}(V_{n-2} - V_n) \quad , \\ V_n &= Z_n(I_{n-1} - I_o) \end{aligned} \tag{1}$$

where Z_i and Y_i are the impedance and admittance, respectively.

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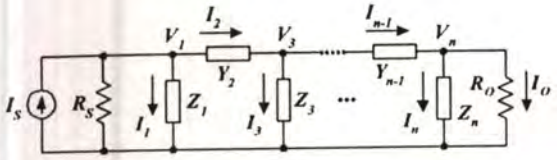

Fig. 1. General doubly terminated ladder network.

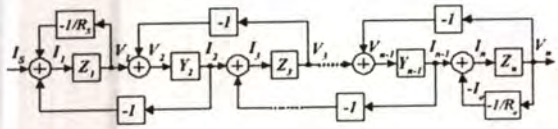

Fig. 2. Block diagram redrawn from figure 1.

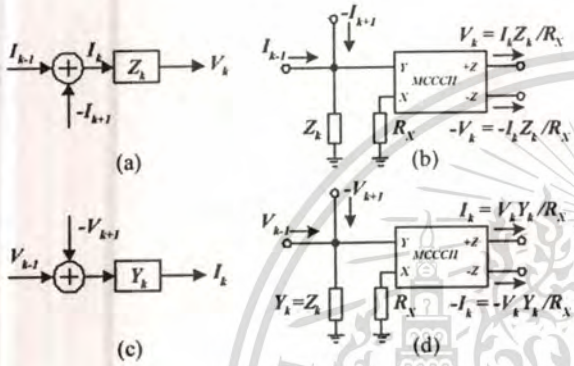

Fig. 3. Basic blocks and the realization using MCCCIIs.

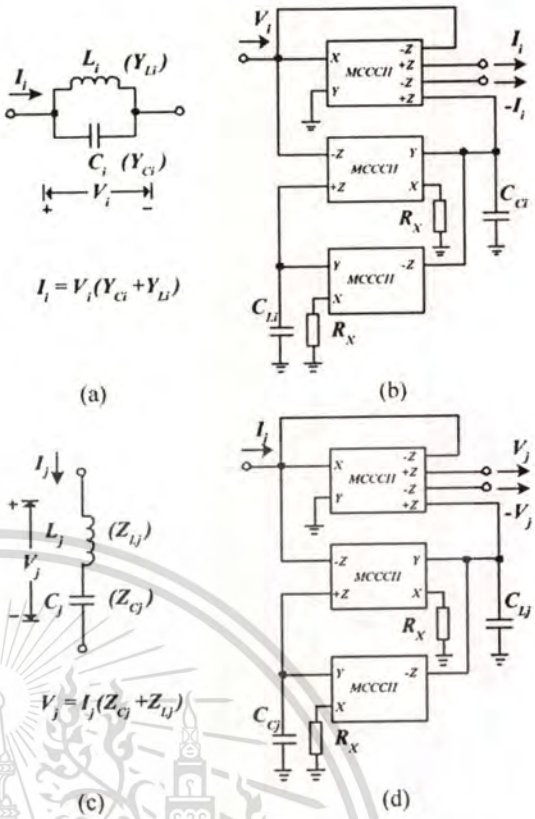

Fig. 4. Proposed blocks using MCCCIIs.

3. MCCCII-BASED STRUCTURE

From above equation, fig. 1 can be represented with block diagram in form of leapfrog structure as shown in figure 2. It is clearly seen that the diagram comprises of 2 operations, current to voltage and voltage to current implication, as redrawn in fig. 3(a) and 3(c). Then if we convert the variables to be processed in only one type, either voltage or current, the execution would be simpler. Transforming all voltage to its current counterpart using MCCCIIs will let these two operations to be implemented using the same circuit as seen in fig. 3(b) and 3(d) that lead to ease of design. Since after the transformation, all variables are related to R_X, therefore, altering on R_X will effect to the characteristic of the filter. Fortunately, MCCCII has an intrinsic resistance at port X, which can be controlled by its bias current that brings about electronically tune ability.

Useful examples, which are employing this technique, can be found in literature in form of ladder low-pass and band-pass filter [6]. For completion, we have proposed the remaining missing blocks in implementing the finite transmission zero here. The parallel LC in branch and series LC in shunt tree are sketched in fig. 4(a) and 4(c), respectively. Their correspondent MCCCII-based blocks are shown in fig. 4(b) and 4(d), which obtain the voltage-current relationship as equation (2) and (3). The simple structure is still promised as well as the tunable characteristic through the resistors at port X. It is worth noting that just one additional MCCCII is needed from the previous series LC in branch and parallel LC in shunt arm [6].

$$I_i = V_i\,(sR_XC_{Ci} + 1/sR_XC_{Li}) \qquad (2)$$

$$V_j = I_j\,(1/sR_XC_{Cj} + sR_XC_{Lj}) \qquad (3)$$

4. MCCCII CIRCUIT DESIGN

Second generation current conveyors (CCIIs) have found useful applications especially in current-mode world. Based on a complementary translinear loop, the current conveyor will be possible to operate at high

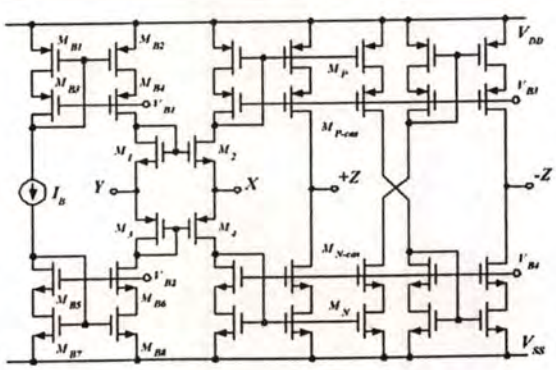

Fig. 5. CMOS implementation of MCCCII.

frequency in class AB. In addition, the translinear current conveyor has a structure as simple as basic OTA but take less power consumption [6]. Despite this, it has only one output terminal, so only one current signal is available only once for each signal feed back. Therefore, in multi-loop feedback path topology like leapfrog, multi-output characteristic seems to play an important role [3][4][6].

Although bipolar technology provides higher gain, wider linearity and frequency bandwidth, CMOS technology have beaten in almost all area of applications when the low power consumption, cost effective and suitability for implementing the mixed analog/digital circuit, are concerned. Accordingly, the CMOS translinear MCCCII has come in our attention and it schematic is shown in figure 5, which the ports relation can be described by the matrix equation in equation (4).

$$\begin{bmatrix} I_Y \\ V_X \\ I_{+Z} \\ I_{-Z} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & R_X & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_{+Z} \\ V_{-Z} \end{bmatrix} \quad (4)$$

where $R_X = \left(4\sqrt{KI_B}\right)^{-1}$ is an intrinsic small signal resistance of the equivalent voltage follower cell and $K = 0.5(\mu C_{OX})(W/L)$ of transistor $M_1 - M_4$, which have to be matched for both NMOS and PMOS. Obviously, It is possible to control R_X by varying the bias current I_B. The multi-output topology can be easily implemented by adding the further output transistors to the port +Z and -Z as required.

5. SIMULATION RESULTS

The performance of the proposed filter is verified through HSPICE circuit simulation based on AMI 0.5-μm standard CMOS process technology. The W/L ratios of CMOS transistors are listed in table 1. The bias current is set to I_B = 50 μA under the voltage supply of $\pm$V = $\pm$2.5 V. This configuration leads to open-loop transconductance gain (G_m) of 0.734 mA/V and 183 MHz -3 dB cut-off bandwidth when using the MCCCII as a transconductance cell.

Table1: W/L area of MOS in MCCCII circuit

Transistors	W/L	Transistors	W/L
M_1, M_2	5/0.5	M_3, M_4	18.5/0.5
M_{B1}, M_{B2}	90/2	M_{B3}, M_{B4}	90/0.5
M_{B5}, M_{B6}	30/2	M_{B7}, M_{B8}	30/0.5
M_P	30/1	M_{P-cas}	60/0.5
M_N	10/1	M_{N-cas}	20/0.5

To picture out the efficiency and flexibility of the proposed filter technique, a current-mode third-order RLC elliptic low-pass filter showing in fig. 6 has been selected and yield

$$\frac{I_o(s)}{I_s(s)} = \frac{s^2C_2L_2+1}{s^3RL_2(C_1C_2+C_2C_3+C_3C_1)+s^2L_2(C_1+2C_2+C_3)+s(C_1R+C_3R+L_2/R)+2} \quad (5)$$

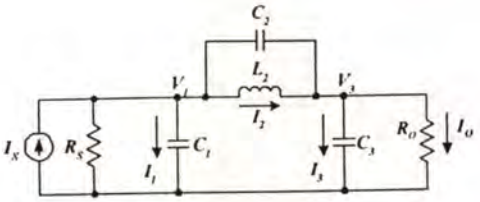

Fig. 6. Prototype current-mode 3^{rd}-order elliptic low-pass RLC ladder filter.

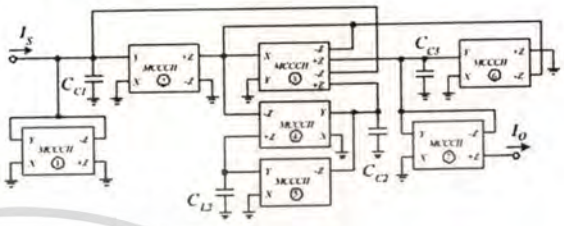

Fig. 7. Synthesized elliptic filter using MCCCIIs and only ground capacitors.

where $R = R_S = R_O$ are the terminated resistances and chosen to be 1 Ω in prototype RLC filter. The filter has been designed with a half-power frequency ω_{-3dB} of 2π(5 MHz). Firstly, the proposed method using only MCCCIIs and grounded capacitors is applied and turn into the complete circuit in fig. 7. The minimum MCCCIIs and grounded capacitors are used without any external resistor. The overall transfer function of proposed filter is

$$\frac{I_o(s)}{I_s(s)} = \frac{s^2R_x^2C_{C2}C_{L2}+1}{s^3R_x^4C_{L2}(C_{C1}C_{C2}+C_{C2}C_{C3}+C_{C3}C_{C1})+s^2R_x^2C_{L2}(C_{C1}+2C_{C2}+C_{C3})+s\left(C_{C1}R_x^2+C_{C3}R_x^2+C_{L2}\right)+2} \quad (6)$$

Even the terminated resistors, R_S and R_O, are also implementing using MCCCIIs and equal to R_X of the current conveyors. This is not only the attempt to eliminate the passive components, it is the necessary key for tuning cut-off frequency feature. Furthermore, this composition has several high impedance output ports, which allow to be easily cascaded without any additional matching circuits.

After scaling by dividing all original passive device values with MCCCII's intrinsic resistance R_X (or $1/G_m$), the corresponding capacitances become C_{C1} = C_{C3} = 28.106 pF, C_{L2} = 22.485 pF and C_{C2} = 4.71 pF. The simulated frequency response of the designed circuit and prototype RLC filter are compared. Test of electronic tuning ability by varying bias current to 6.25 μA, 50 μA and 400 μA is also performed and shown together in figure 9. From the results we can see the well agreement between the proposed structure and the passive prototype before signals have reached the deviation at frequency beyond 100 MHz. This is due to the frequency limitation of MCCCII itself, which can be improved later.

Because this technique derives each element with one-by-one replacement concept. We can separate the

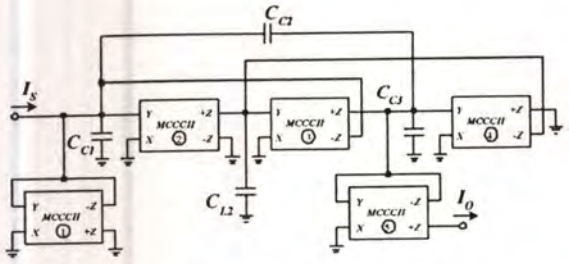

Fig. 8. Synthesized elliptic filter using MCCCIIs with a floating capacitor.

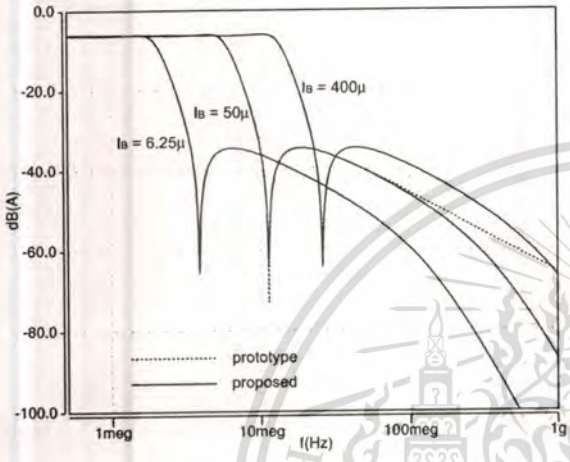

Fig. 9. Simulated frequency response of fig. 7

floating capacitor C_2 from the passive filter figure 6 and then realize the canonical MCCCII-based low-pass ladder filter first [6], afterward, adding the capacitor C_2 to the synthesized circuit at corresponding node will give result as complete circuit in figure 8 with the transfer function of

$$\frac{I_o(s)}{I_s(s)} = \frac{s^2 R_x^2 C_{C2} C_{L2} + 1}{s^3 R_x^3 C_{L2}(C_{C1}C_{C2} + C_{C2}C_{C3} + C_{C3}C_{C1}) + s^2 R_x^2 C_{L2}(C_{C1} + 2C_{C2} + C_{C3}) + sR_x(C_{C1} + C_{C3} + C_{L2}) + 2} \quad (7)$$

The simulation outcome in figure 10 shows the even better performance. This structure is very attractive when the floating capacitor is allowed.

6. CONCLUSIONS

A method for the synthesis of leapfrog ladder filter using multi-output current controlled conveyors is presented. The design strategy is very simple and covers all type of precedent passive LC ladder filter. This strategy requires the minimum passive and active components. The characteristic frequency can be tuned electronically by adjusting the bias current of current controlled conveyors, which is very helpful in compensating unmatched components as well as varying the characteristic without changing any device. Besides using only MCCCIIs and all grounded capacitors, the high frequency elliptic filter can also be efficiently realized by adding floating capacitors to the relative all-pole filter. Third-order elliptic low-pass filter is derived as an example. HSPICE simulation results give a good agreement with the theoretical expectation.

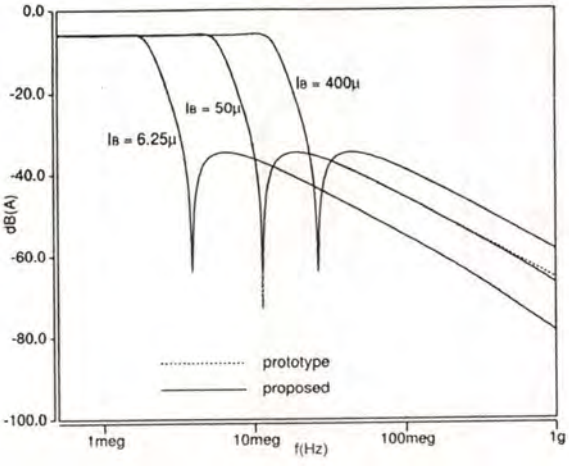

Fig. 10. Simulated frequency response of fig. 8

7. ACKNOWLEDGEMENT

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Slew Rate Induced Distortion in Switched-Resistor Integrators

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***Abstract*— OPAMP-RC integrators built with linear resistors and capacitors can achieve very high linearity. By means of a switched resistor, tuning of the RC time-constant is possible via the duty-cycle of the clock controlling the switched resistor. This paper analyzes the effect of OPAMP slew rate limitations on the distortion of a switched-resistor lossy OPAMP-RC integrator. We show via analysis and simulations that the use of two sets of switched resistors instead of one relaxes the OPAMP slew rate requirements, and reduces the resulting distortion significantly.**

I. Introduction

OPAMP-RC filters with highly linear passive resistors and capacitors have superior linearity properties for baseband filter applications, if OPAMPs with sufficient gain can be realized. Such filters can be made tunable using resistive or capacitive arrays [1], but this is only practical for coarse tuning. Fine tuning is possible using a MOSFET as variable resistor, and good linearity has been achieved in the past via this approach [2]. However, this requires a gate-source on-voltage which is substantially larger than the input voltage swing, which is impractical in low-voltage deep submicron CMOS processes. For low-voltage conditions a more practical approach is the use of a passive resistor, switched on and off by a clock with tunable duty cycle [3]. Figure 1 shows a simple lossy integrator using such a tuning technique with a single switched resistor. The resistor is in the feedback loop and hardly adds distortion. However, as will be evident, the resulting switching operation poses more stringent requirement on the slew rate of the OPAMP. This paper analyzes the slew rate limitations of the single switched resistor lossy integrator, and the resulting distortion. We also propose a network employing two switched resistors that is less sensitive to slewing problems.

II. Circuit Operation

A lossy integrator with one switched resistor ("Switched-1R") is shown in Fig. 1. The MOS switch before the OPAMP input is alternatingly turned on and off to select whether the current can pass to the capacitor or not. Like a track and hold circuit, it has 2 phases: tracking integration and holding. The variation in the on-time of the switch, determined by the duty cycle of the clock, effectively changes the resistance and hence

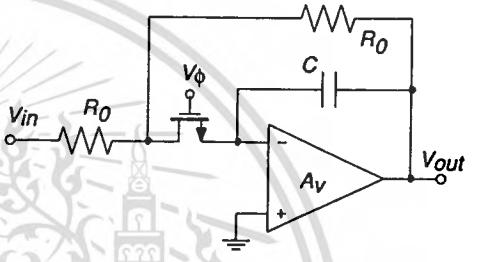

Fig. 1. Switched-1R Lossy Integrator

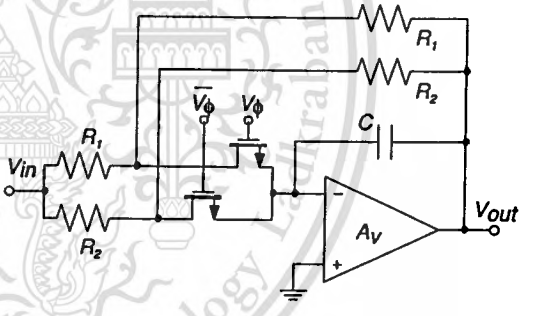

Fig. 2. Switched-2R Lossy Integrator

the lossy integrators cut-off frequency. If m is the duty cycle, then the effective resistance becomes:

$$R_{eff} = \frac{R_0}{m} \tag{1}$$

Thus we can theoretically tune the integrator time-constant between 0 and R_0C. However, in many cases we do not need this large tuning range, but only need about ±20% range to correct for technology and temperature variations, or ±50% to "bridge the gap" between coarse tuning steps. With this in mind, we propose an alternative circuit with two switched resistors (so called Switched-2R) in Fig. 2. If two sets of resistors are controlled by non-overlapping clocks, to realize a time constant ranging from R_1C up to R_2C, it will turn out that this circuit has less sensitivity to OPAMP slew rate problems.

Possible causes of distortion in a switched resistor lossy integrator are the non-linear on-resistance of the MOS switch

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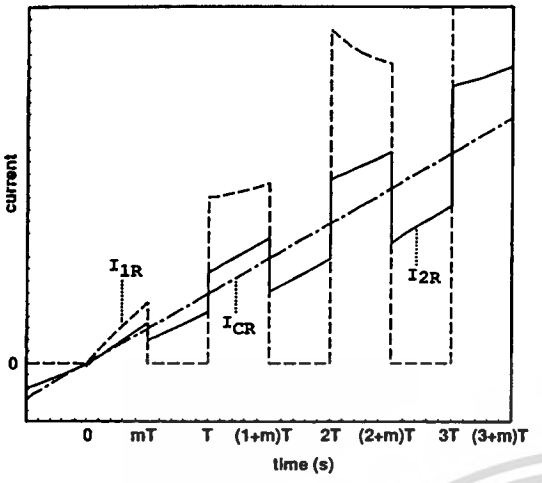


Fig. 3. Capacitor currents of lossy integrators

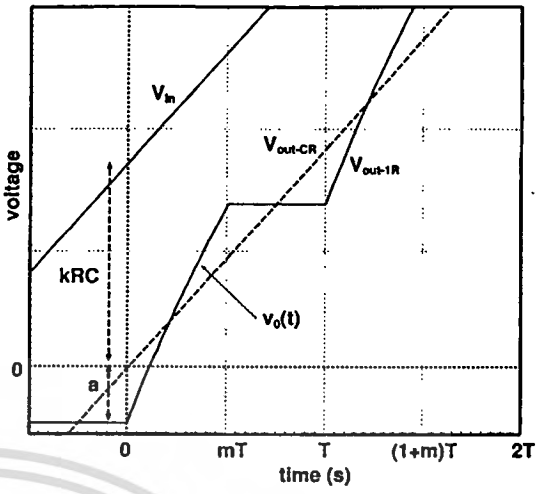


Fig. 4. Switched-1R output voltage response

and OPAMPs non-idealities. As the MOS switch is in series with a much higher linear resistor, while it is also embedded in the negative feedback loop, its non-linearity contribution can be very small. However, the OPAMP may introduce significant distortion, especially if a fast OPAMP response to large input signal changes is needed, and slew limitation occurs in the OPAMP. During slewing, the feedback loop is effectively broken for some time, and it is instructive to predict when slewing occurs, so that its effect can be minimized. We will analyze this in the next section.

III. Slew Rate Analysis

A. Qualitative Analysis

It is known that the highest slope in a sinusoidal signal occurs at the zero crossing. So, for the sake of analysis, the input signal can be approximated as a ramp with a constant slope of $V_p\omega_{max}$. We will use a ramp signal to analyze slewing behavior of the lossy integrator. Figure 3 shows the capacitor current of the Switched-1R (I_{1R}) and Switched-2R (I_{2R}) lossy integrators for 50% duty cycle and identical effective time constants. For comparison, the current for a continuous-time integrator I_{CR} is also shown. It should be noted that the average current of the switched resistor circuits must be equal to the current in the continuous-time circuit in order to produce equivalent frequency response characteristics. Since the rate of change of the output voltage, $\frac{dV_o}{dt}$, is the same as the voltage change over the capacitor, this value is also directly proportional to the applied current and inversely proportional to its capacitor value. The capacitor value is fixed, and therefore only the current determines the voltage.

Consider the current plots in Fig. 3. In the Switched-1R case, the MOS switch will conduct current only during the integration phase while there is zero current flow during the hold phase. A larger current is therefore needed in the turn-on stage. On the other hand, Switched-2R has two non-zero current flows depending on whether system is operating in low-value resistor or high-value resistor mode. Hence, we should expect more voltage changes and higher slopes occuring in the Switched-1R case than for Switched-2R. Accordingly, we should also expect the higher OPAMP slew rate requirement for the Switched-1R case.

B. Detailed Analysis

The output voltages of the Switched-1R and Continuous-R integrators are plotted together with the input ramp signal in Fig. 4 (the outputs are inverted for ease of comparison with the input signal). The Switched-1R output voltage response tracks the continuous-time circuit well, except for a sawtooth-like waveform. This is because its average current has to be equal to the continuous-time current as mentioned in the previous section. It can be seen that there is a high slope response in the tracking period and zero slope in the holding period. Finding the maximum slope in the tracking period by considering $t = 0$ as the starting point, gives the observation that the Switched-1R lags the Continuous-R output by an amount "a" (see Fig. 4). Following this, the response curve within the clock period mT can be considered as the response of a lossy integrator with resistor R_0 value, under the excitation of a ramp input $V_{in} = kt$ and an initial condition at $t = 0$ of "$-a$". As illustrated in Fig. 4, this is equivalent to the lossy integrator that has been stimulated by a unit-step signal of $(kRC + a)$ magnitude superimposing a ramp signal with slope k within the period time mT. Hence, the complete output response will be the sum of the individual responses to the unit-step and ramp signal together since this circuit is linear and time-invariant system. It can be derived that the output response in the tracking phase (v_0) is

$$v_0 = \left[(kRC+a)\left(1-e^{\frac{-t}{R_0C}}\right)\right]+\left[kt-kR_0C\left(1-e^{\frac{-t}{R_0C}}\right)\right]-a \quad (2)$$

where R is the equivalent resistance equal to the the one used in the Continuous-R and the magnitude of a is a function of duty cycle m and clock period T.

$$a = k\frac{(1-m)T+(R_0-R)Ce^{\frac{-mT}{R_0C}}}{1-e^{\frac{-mT}{R_0C}}}$$

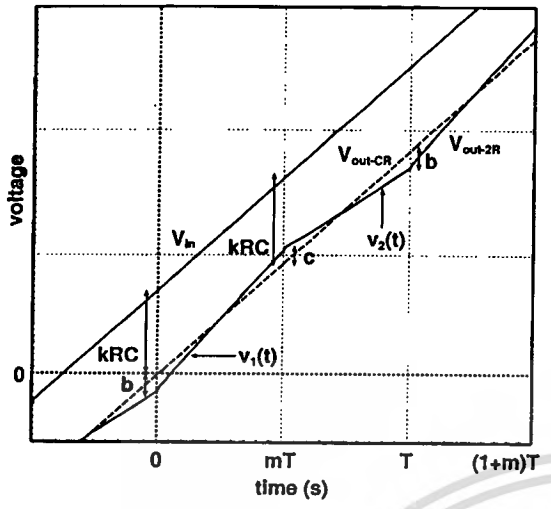


Fig. 5. Switched-2R steady output voltage response

The components in the first square brackets of Eqn. (2) constitute the unit-step response. The second is the response to the ramp and the last term is the initial condition. The maximum slope values of this response, which is determined by finding its derivative, is

$$S-1R = \frac{kRC+a}{R_0C} \quad (3)$$

The Switched-2R's output response exhibits two slopes as shown in Fig. 5. By assigning resistor value $R_1 < R_2$, the moment $t = 0$ will refer to the state that R_2 just switches to R_1. At that instant, the Switched-2R response is lower than the Continuous-R response by an amount "b". On the other hand, at the end of time period mT, the output response of the Switched-2R is higher than the Continuous-R by an amount "c". In the same analysis manner as for the Switched-1R, it can be derived that the output response for the low value resistor R_1 phase (v_1) and for the high value resistor R_2 phase (v_2) are:

$$v_1 = \left[(kRC+b)(1-e^{\frac{-t}{R_1C}})\right]+\left[kt-kR_1C(1-e^{\frac{-t}{R_1C}})\right]-b \quad (4)$$

$$v_2 = \left[(kRC-c)(1-e^{\frac{-t}{R_2C}})\right]+\left[kt-kR_2C(1-e^{\frac{-t}{R_2C}})\right]+c \quad (5)$$

where b and c are also functions of m and T.

$$b = kC\frac{(R_1-R_2)e^{\frac{-(1-m)T}{R_2C}}+(R-R_1)e^{\frac{-T}{RC}}+(R_2-R)}{1-e^{\frac{-T}{RC}}}$$

$$c = kC\frac{(R_1-R_2)e^{\frac{-mT}{R_1C}}+(R_2-R)e^{\frac{-T}{RC}}+(R-R_1)}{1-e^{\frac{-T}{RC}}}$$

As a result, the maximum slopes that the OPAMP has to follow will be:

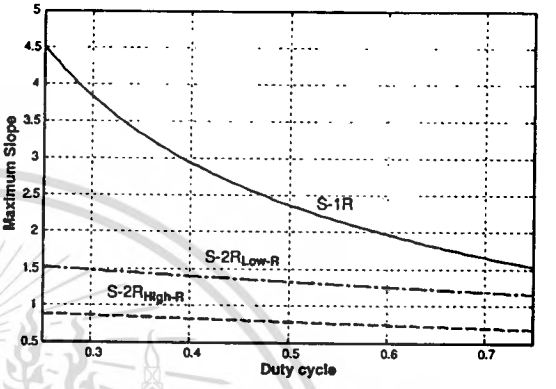
$$S-2R_{Low-R} = \frac{kRC+b}{R_1C} \quad (6)$$

$$S-2R_{High-R} = \frac{kRC-c}{R_2C}e^{\frac{-(1-m)T}{R_2C}}+k(1-e^{\frac{-(1-m)T}{R_2C}}) \quad (7)$$

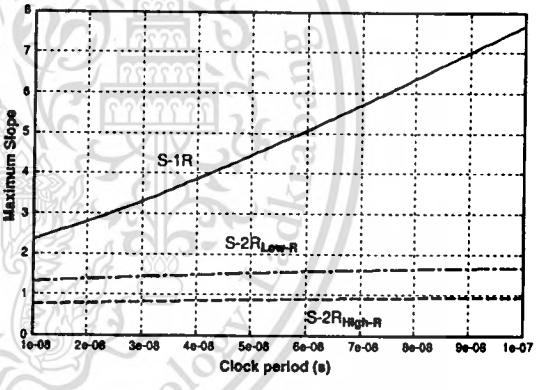
TABLE I

MAXIMUM SLOPE COMPARISON

	m = 0.43		m = 0.5		m = 0.56	
	Math	Sim	Math	Sim	Math	Sim
$S-1R$	4.527	4.518	2.370	2.368	1.527	1.526
	m = 0.25		m = 0.5		m = 0.75	
$S-2R_{Low-R}$	1.521	1.520	1.331	1.330	1.160	1.160
$S-2R_{High-R}$	0.869	0.867	0.760	0.755	0.663	0.656



(a) varied with m (at T=10 ns)



(b) varied with T (at m=0.5)

Fig. 6. Maximum slope variation with duty cycle and clock period

The above equations show the relationship between maximum slope and duty cycle "m" and clock period "T". This relation was verified by comparing the mathematical results with simulation results under the same condition. The maximum input slope, k, is set to 1 for simplicity. The cut-off frequency is chosen to be 10 MHz, consequently yielding capacitor C at 3 pF, R_0 for Switched-1R at 2.5 kΩ, R_1 and R_2 for Switched-2R at 4kΩ and 7kΩ, respectively. Table I shows the results of the two systems by varying m = 0.43, 0.5, 0.56 in Switched-1R and m = 0.25, 0.5, 0.75 in Switched-2R at 10 ns clock period for the same corresponding cut-off frequencies.

The plots of the maximum slope as a function of "m" and "T" are shown in Fig. 6. Fig. 6(a) shows the slope change at varying duty cycles when the clock period is fixed at 10 ns (f_{clk} = 100 MHz) and Fig. 6(b) shows the slope change

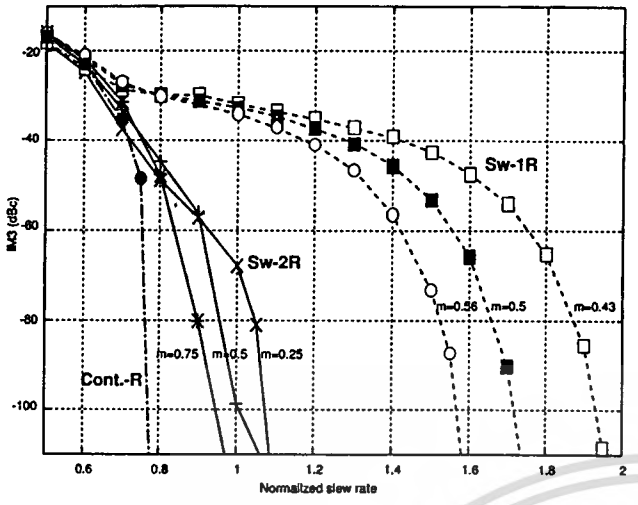


Fig. 7. 3^{rd}-order Intermodulation Distortion

with clock period adjusting when the duty cycle is fixed at m = 0.5. Since the occurred maximum slope for Switched-2R operating with a low valued resistor is always higher than for a high valued resistor, the low-R region determines the slew rate requirement.

Interestingly, when increasing m, the maximum slope becomes smaller and vice versa. This is because when m is increased, more time is spent in the high current period while the low current period is shortened. Therefore, the extra current magnitude in the high current phase, needed for compensating with the low current phase, is smaller and this results in a lower maximum slope. However, since the difference between the current magnitudes in these two phases is larger for Switched-1R, changing m will affect its output response more than Switched-2R.

IV. Simulation Results

Figure 7 shows the third-order intermodulation distortion, IM_3, of the three structures, Switched-1R, Switched-2R and Continuous-R, plotted versus normalized slew rate. The normailzed slew rate is defined as the slew rate value divided by the maximum input signal slope, which is assumed to be the basic slew rate requirement for OPAMP operated in continuous-time mode. It is introduced here in order to enable the systems' performance comparison independent to their applied input signals. An OPAMP analog behavioral model and ideal switch have been used initially to investigate the linearity properties, since their parameters can be effectively controlled [4]. The lossy integrators are configured to have 10 MHz cut-off frequency under 2-tones test of 5 MHz and 6 MHz, 0.4 Vp magnitude, 100 MHz clock frequency and 80 dB OPAMP DC gain. The maximum input slope can be calculated from $V_p\omega_{max}$ = 15.08 V/μs.

From Fig. 7, it can be noticed that the Switched-2R's distortion components drop as fast as for continuous-R while roughly two times more slew rate is needed in the Switched-1R case before the distortion will drop to the minimum level. Changing duty cycle will alter the curves as expected. These results reflect the previous developed equations very well. As can be seen from Fig. 6(a), the maximum slope occurred at m = 0.5 in Switched-2R (1.3) is much closer to the continuous-time (1) than Switched-1R (2.3). Moreover, the larger variation of maximum slope to the changes of m in Switched-1R, also appears in the distortion results. It can be shown that the distance ratios of slew rate requirements between each system in Fig. 7 are quite close to the ratios of their corresponding maximum slopes in Fig. 6(a).

Simulation results of the practical systems using MOS switches and typical two-stage OPAMP circuit also show the same trend. Using OPAMP with 60 dB gain and 18.6 V/μs slew rate produces IM_3 distortion of -57.97 dBc, -54.23 dBc and -48.09 dBc for Continuous-R, Switched-2R and Switched-1R, respectively. Although these values are twice as worse as the ideal model predictions due to the other non-ideal effects, they still possess the similar ratio between each other. All the normalized systems produce the same high distortion level at the slew rate less than about 0.7. In term of noise performance, there is not any considerable difference between all the systems. On the one hand, although Switched-1R utilizes the track and hold operation, it employs the clock frequency much higher than its cut-off frequency so that the noise folding problem will not take effect. On the other hand, Switched-2R does not has any noise folding effect, therefore, this is another advantage over conventional switched-capacitor structures.

V. Conclusion

OPAMP slew rate requirements for switched-resistor lossy integrators have been analyzed. The theory along with simulation results confirm the advantage of using two sets of resistors over one set of resistors in the sense of lowering the required OPAMP slew rate at the same output's distortion level. The tuning range of two sets of resistors can be extended by increasing the difference of the constituent resistors' values, however, it trades with the higher distortion. This gives a more freedom to deal with tunable range and linearity.

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