MODELING AND CONTROL OF DC-DC CONVERTERS USING AVERAGE CURRENT MODE CONTROL

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บทคัดย่อ

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ABSTRACT

In this thesis, modeling and feedback control design of a DC-DC converter with Average Current Mode Control (ACMC) is studied. Based on the ACMC principle, two novel techniques to improve output dynamic response of the converter are proposed. The first technique uses a high-order voltage controller to compensate a high-order control-to-output transfer function of the voltage loop, where the high-order controller is realized by parallel connection of two standard controllers. The second technique uses a sensed inductor current signal, readily available in ACMC, as a feedforward signal to sum with an output signal from a voltage controller to produce a control signal. The two proposed methods essentially lead to the strengthening of the corrective action in the voltage loop and thus the improvement in dynamic response of the converter. The effectiveness of the two proposed techniques compared with the conventional ACMC is demonstrated by simulated and experimental results.

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Chapter 1

Introduction

1.1 Output voltage control of DC-DC converters

The use of a DC-DC converter is widespread in today's electronic systems, where the converter is located in the vicinity of and provides a tightly regulated voltage to its electronic load. A wide operating profile of the modern load causes a current drawn from the power supply to vary over a wide range. Changes from one load profile to another often take place in a very short time, usually accompanied by a rapid change of the current demand. It is therefore essential that the converter used in such applications possesses excellent dynamic response to the load change.

The output voltage regulation of DC-DC converters is traditionally performed by either Voltage-Mode Control (VMC) or Current-Mode Control (CMC). Though both control methods are capable of good output regulation, CMC nevertheless is known to have a faster dynamic response than VMC [1]. It is thus employed in majority of today's power supplies. Despite many good features, CMC also has several drawbacks. Most notably are the control operation is sensitive to noises and inherently unstable when operating with a duty ratio above 0.5. This instability can be prevented by adding a compensation ramp into a control signal. The inclusion of the compensation ramp circuitry, however, complicates the control implementation. Furthermore in CMC it is the peak current, not the average, which is being control; the resulting peak-to-average error prevents its usage in applications where accurate current control is required. To overcome the aforementioned problems, Average Current-Mode Control (ACMC) has recently been proposed [2]. It offers a superior performance to CMC in that no compensation slope is required, control operation is highly immune to noises, and no peak-to-average error problem exists because the average current is controlled directly in this control scheme. These appealing features have resulted in a widespread use of ACMC in today's DC-DC converters.

1.2 Literature review and research objective

In [2,3,4], operating principle, modeling, and control design of ACMC have been described. The presented ACMC small-signal model [3,4], together with the small-signal model of the converter's power stage [5], form a complete converter system, from which various transfer functions can be derived. Based on these transfer functions, the controllers in the voltage and current loops can be

designed so that the converter yields the desired output performance, i.e. having good output regulation and fast dynamic response. However, even with the well designed controllers, the converter's performance still may not meet the stringent requirements of modern electronic loads, which requires a tightly regulated voltage from the converter over a wide range of current. To enhance the performance of the conventional ACMC, the novel three-controller ACMC [6] has recently been proposed. The authors modified the voltage loop to include an auxiliary controller. The transfer function of the auxiliary controller was carefully selected and designed to increase robustness of the converters against variations in the input voltage, load current and values of *L-C* output filter. It was demonstrated experimentally that the three controllers ACMC yields a faster output voltage response than the conventional ACMC. However, its implementation of the novel three-controller requires many additional circuit components. The increased cost and circuit complexity may not justify practicality of the three controller technique.

Based on ACMC principle, this thesis proposes two novel techniques to improve the output dynamic performance of the converter: (1) ACMC with a parallel controller (ACMC-P), and (2) Current Feedforward Average Current Mode Control (CFACMC). The former method is based on the use of a high-order controller, synthesized by parallel connection of the two basic controllers, to compensate the high-order characteristics of the voltage loop. The synthesized controller contains an adequate numbers of poles and zeros that allows the converter's loop gain be tailored to have a higher gain and bandwidth than those achieved by the standard controller, thereby enhancing the converter's dynamic performance. The latter method uses the inductor current information readily available in ACMC scheme as a feedforward signal to strengthen the control action of the output voltage feedback control. The current feedforward loop, if appropriately designed, can lead to considerable improvement in the output dynamic response of the converter.

1.3 Assumption of this study

The control techniques proposed herein have been aimed to be used in a low-voltage high-current point of load DC-DC converter. In this application, the converter is located close to the electronic load it supplies, and receives a constant input voltage from the central power supply unit. The load current of the converter can typically vary over a wide range and change in a step manner. It is therefore vital that the point of load converter possesses a good output voltage regulation against the load current variations and exhibits a good output dynamic response to the step load change.

In this work, an input voltage of the converter is constant at 5V. An output voltage of the converter is regulated at 2V and a load current can vary from 1A to 5A. To verify the effectiveness of the two proposed techniques, the output voltage response of the converter is simulated and measured for a step load change of 3A (i.e. the load current is stepped from 1A to 4A).

1.4 Thesis structure

The thesis is organized as follows.

Chapter 2- Review of Control Methods – Three basic methods for controlling an output voltage of DC-DC converters are reviewed. They are Voltage Mode Control (VMC), Current Mode Control (CMC), and Average Current Mode Control (ACMC).

Chapter 3- Modeling and Control of DC-DC Converters with Average Current Mode Control – This Chapter focuses on modeling of a buck converter with ACMC. Small-signal model of the converter is derived. Various transfer functions are then determined from the obtained model for control design purposes.

Chapter 4- Two Novel Techniques to Improve Dynamic Response of the Converter – Based on the theoretical background of ACMC established in Chapter 3, this Chapter proposes two novel techniques to improve the output dynamic performance of the converter: (1) ACMC with a parallel controller (ACMC-P) and (2) Current Feedforward Average Current Mode Control (CFACMC). Principle of operation of the two techniques is followed by description of their small-signal model and design procedures.

Chapter 5- Design of the Prototype Converter – Control design of a prototype buck converter is carried out numerically based on the analytical results in the preceding two chapters. The prototype circuit has been designed to include the three control techniques under study, i.e. (1) the conventional ACMC, (2) ACMC-P and (3) CFACMC into a single circuit board. Selection of the desired control scheme is done by switch setting.

Chapter 6- Results – The first part of this Chapter describes averaged models of the converter, which have been developed for simulation with SIMULINK. The later part of the chapter presents simulated and experimental results.

Chapter 7- Conclusion- This Chapter summarized the outcomes of the research.

Chapter 2

Review of Control Method

DC-DC converters convert a DC input voltage into the desired value of DC output voltage by means of electronic switching, using a power MOSFET and diode. The converters employ feedback control to keep an output voltage constant, regardless of disturbances in an input voltage and/or the load current. The performance of the feedback control strongly determines output regulation characteristics of the converters. This Chapter reviews basic operation of a buck DC-DC converter and the commonly used output voltage control methods. The three standard control methods are Voltage Mode Control (VMC), Peak Current Mode Control (PCMC), and Average Current Mode Control (ACMC). VMC is a single-loop control with the output voltage being the only feedback variable, while both PCMC and ACMC are a two-loop control with the output voltage and inductor current being the feedback variables.

2.1 Buck converter

A buck converter's power stage is shown in Fig. 2.1. The power MOSFET is operated as an electronic switch and turned on/off by a constant-frequency Pulse-Width- Modulated (PWM) signal from the control circuit. In the figure, L and C are a filter inductor and capacitor respectively, r_c is an Equivalent Series Resistance (ESR) of the capacitor C and R is a standing load. In Continuous Conduction Mode (CCM), the inductor current flows continuously over one switching period. When the MOSFET is turned on, the inductor voltage is $V_{in} - V$, and the inductor current increases linearly. When the MOSFET is turned off, the diode conducts, the inductor voltage becomes $-V$, and the inductor current decreases linearly. Under steady state operation, the averaged inductor voltage is equal to zero, allowing the relationship between V_{in} and V to be established:

$$V=dV_{in} \tag{1.1}$$

where d is a duty ratio of the MOSFET. Since $0<d<1$, the output voltage is therefore always less than the input voltage. In most DC-DC converter applications, the regulated output voltage is required. From (1.1), V can be regulated against changes in V_{in} by adjusting d. It should be noted that (1.1) is derived from the ideal converter, where resistances of the MOSFET, inductor and print circuit board traces, etc.,

have not been accounted. These non-idealities, in effect, cause the output voltage to be dependent on the load current as well.

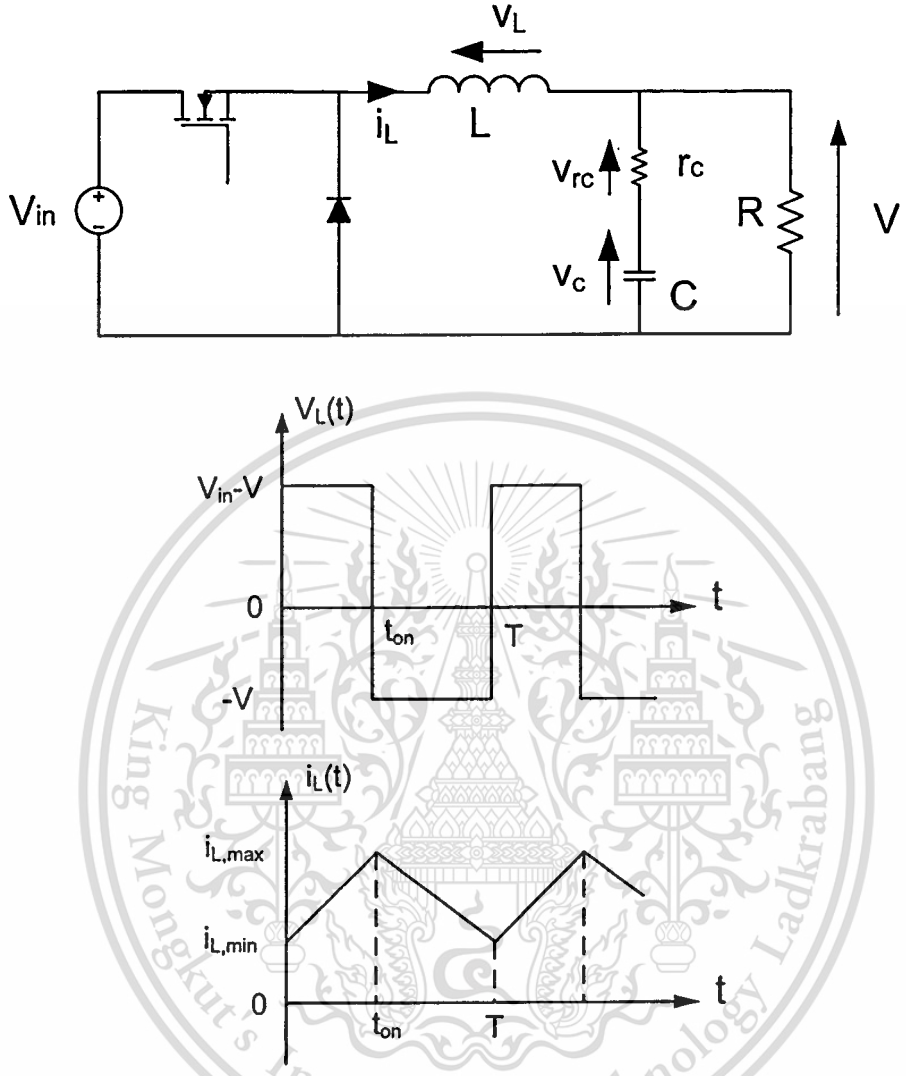


Fig 2.1 Buck converter

2.2 Control Method

2.2.1 Voltage Mode Control (VMC)

A buck converter with VMC is shown in Fig 2.2(a). The output voltage V is fed back and subtracted from the reference voltage V_{ref} to form an error voltage. The error voltage is processed by the controller to generate the control signal V_c which is compared with the fixed frequency sawtooth voltage V_{saw} at the comparator. The MOSFET is turned on whenever V_c is greater than V_{saw} and tuned off whenever V_c is lower than V_{saw}. As illustrated in Fig. 2.2(b), if there are any changes in the output voltage, e.g. the output voltage decreases due to the increase in load current, VMC will counteract by

adjusting V_c and the duty ratio of the MOSFET, until the output voltage equals to its reference value or the error voltage equal zero. However, VMC has a poor output voltage response to changes in the input voltage. It cannot immediately detect the input voltage disturbance and has to wait until the impact of the disturbance reached the output [7]. Only then, the correcting mechanism can take place.

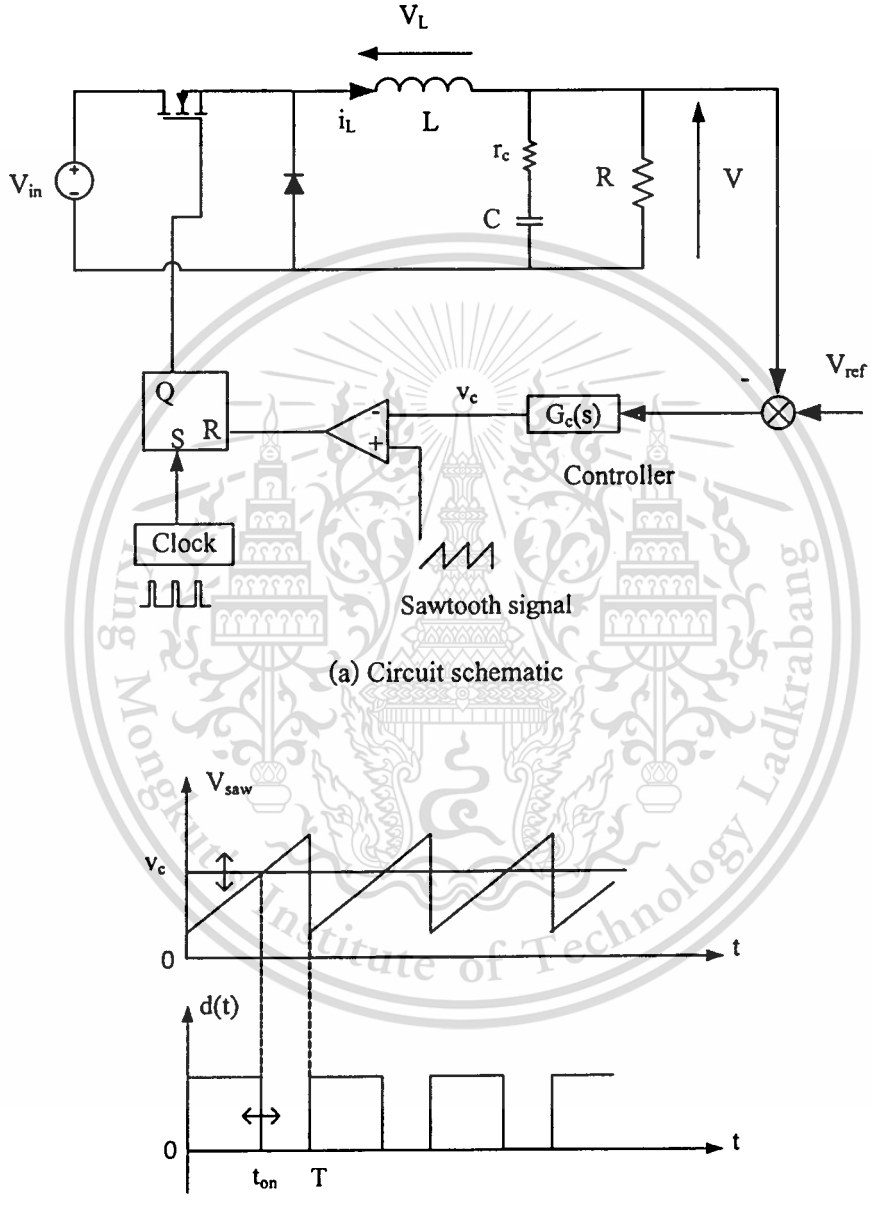


Fig 2.2 Buck converter with VMC

2.2.2 Peak Current Mode Control (PCMC)

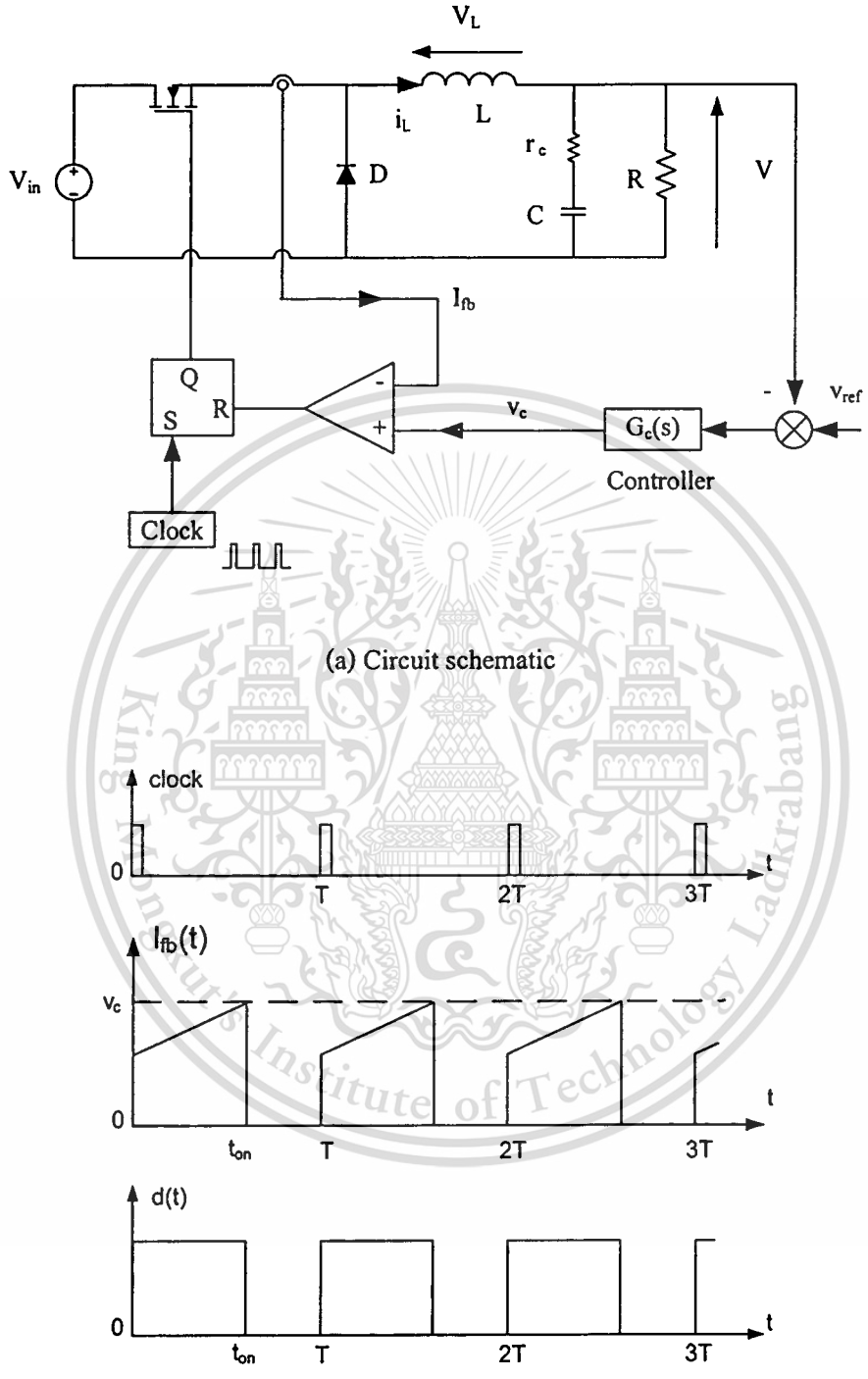


Fig 2.3 Buck converter with PCMC

A buck converter with PCMC is shown in Fig 2.3(a). At the beginning of a switching cycle, the clock signal sets the flip-flop (Q=1), turning on the MOSFET. The MOSFET current, which is equal to the inductor current during this interval, increases linearly. This current is sensed as I_{fb} and compared

with the control signal V_c from the controller. When I_{fb} reaches V_c, the output of the comparator goes high and resets the flip-flop (Q=0), thereby turning off the MOSFET. The MOSFET will be turned on again by the next clock signal and the same operation repeated.

If the output voltage decreases due to the increase in the load current, V_c will increase. The time for I_{fb} to reach V_c, therefore, will be longer, increasing the duty ratio of the MOSFET. The increased duty ratio will cause the inductor current to increase to the new load current and restore the output voltage back to its desired value. Unlike VMC, PCMC has good output voltage response to changes in the input voltage. The changes in the input voltage will be reflected directly on a slope of the inductor current which, in turn, has a direct impact on the duty ratio, as shown in Fig 2.3(b). For example, when the input voltage is increased, the slope of the MOSFET current, equal to $(V_{in}-V)/L$, will increase. This will cause the duty ratio to decrease to offset the increased input voltage.

An inductor current waveform of PCMC is shown in Fig. 2.4. Figure 2.4(a) shows the inductor current waveform when $d < 0.5$. If there is a small perturbation in the inductor current, the perturbation will be subdued and the perturbed waveform eventually converted to the steady-state waveform. Hence, there is no stability problem in PCMC with $d < 0.5$. By contrast, a small perturbation in the inductor current when $d > 0.5$ will lead to instability (Fig. 2.4(b)). Thus, PCMC is inherently unstable when operated with $d > 0.5$.

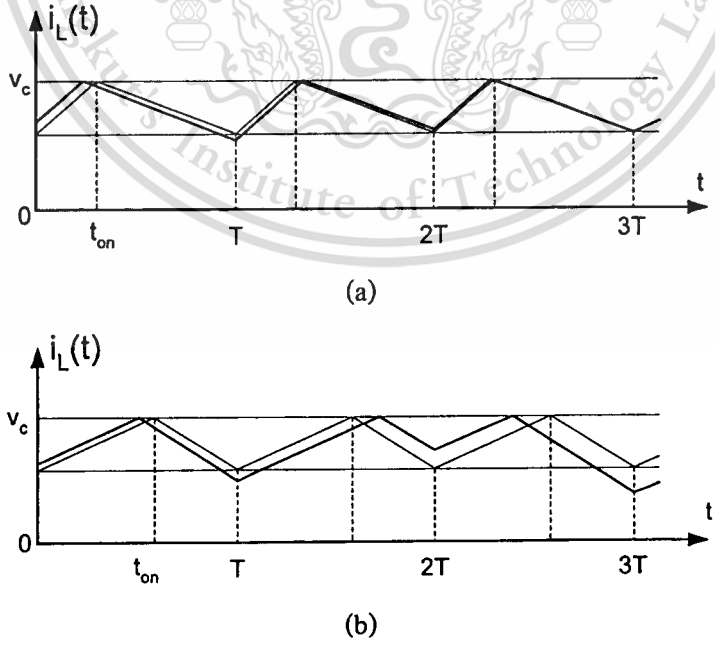
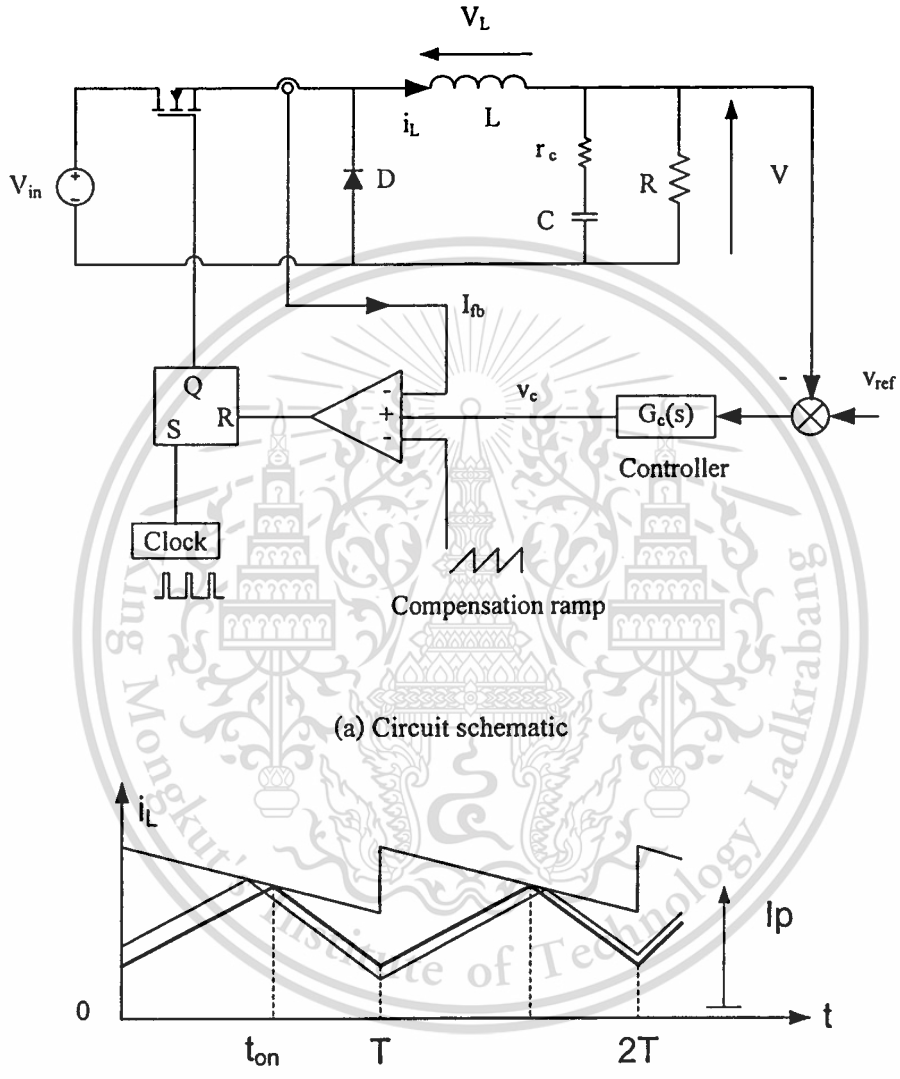


Fig 2.4 Perturbed inductor current

The solution for this instability is to use a compensation ramp as shown in Fig. 2.5. The ramp signal is subtracted from the control signal and the MOSFET now switched off, when I_{fb} is equal to v_c-v_{ramp}. The compensation ramp effectively provides a damping in the current loop, thus enhancing the loop stability [8]. With the compensation ramp, the range of stability is extended beyond d = 0.5 (Fig. 2.5(b)).



(b) Perturbed inductor current wave when d>0.5

Fig 2.5 Buck converter with PCMC using compensator ramp

Compared with VMC, PCMC provides a faster dynamic response under the input voltage and/or load current changes. The MOSFET switch is turned off when the feedback current reaches the control signal. Hence, over current protection is easy to implement by limiting a maximum value of the control signal. However, this control method needs a compensation ramp to assure the stability of the system, when operated with d>0.5.

2.2.3 Average Current Mode Control (ACMC)

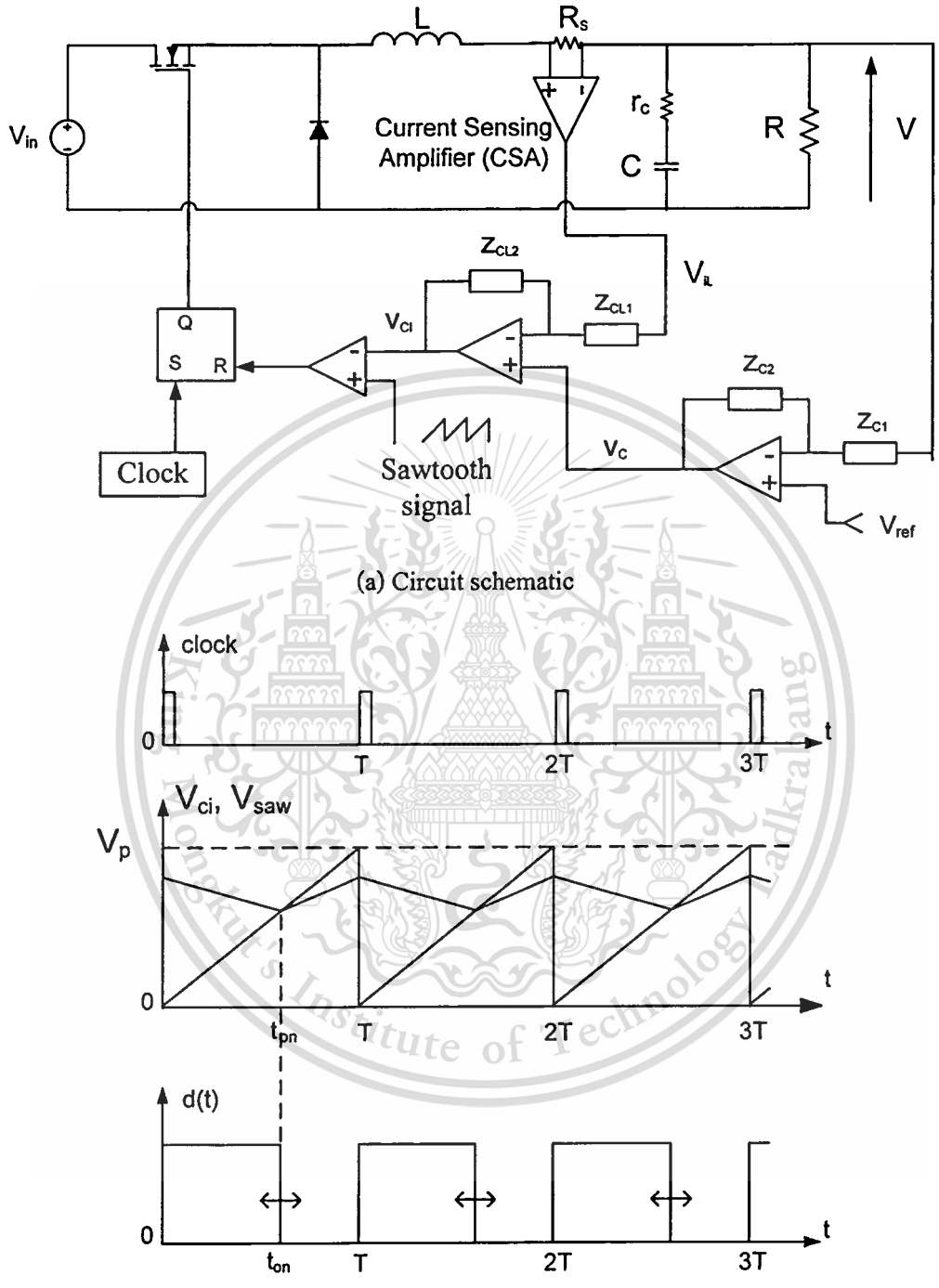


Fig 2.6 Buck converter with ACMC

A buck converter with ACMC is shown in Fig 2.6(a). At the beginning of a switching cycle, the clock signal sets the flip-flop (Q=1), turning on the MOSFET. The inductor current increases linearly during this interval. The inductor current is sensed by the resistor R_s and multiplied by a gain A_c of the

current sensing amplifier to give the sensed current signal $V_{iL} = iA_cR_s$. The difference between V_c which represents the desired current and V_{iL} which represents the actual inductor current is amplified by the current error amplifier. The resulting current error signal V_{ci} is compared with the fixed frequency sawtooth voltage V_{saw}. When V_{ci} is equal to V_{saw}, the flip flop is reset and the MOSFET turned off. The MOSFET will be turned on again by the next clock signal and the same operation repeated.

When the output voltage V deviates from V_{ref} the control signal V_c the current error signal V_{ci} and the duty ratio d will change. The change in d results in the adjustment of the average inductor current and output voltage. At a new steady-state condition V_{iL} will be again equal to V_c; that is the averaged inductor current will be at the value sufficient to maintain the constant output voltage.

In ACMC, a current error amplifier is employed in the current loop to force the inductor current to closely track the reference current, instead of directly comparing the two quantities using a comparator as in PCMC. As a result, ACMC has a better noise immunity and no stability problem when $d > 0.5$ (i.e. no compensation ramp is required). Moreover, the current error amplifier can be compensated to yield the current loop with high gain and wide bandwidth for better current tracking capability and fast dynamic. This leads to the improved performance of the converter.

Chapter 3

Modeling and Control of DC-DC Converters with Average Current Mode Control

This Chapter describes modeling of a buck converter and average current mode control. The state-space averaging technique is employed to find a small-signal model of the power stage, while a small-signal model of the control stage is adopted from the work in [3,4]. When combined together, these two models form a complete closed-loop system, from which transfer functions for control design purpose can be derived. Based on these transfer functions, the controllers in the voltage and current loops can be designed so that the converter exhibits the desired output performance, i.e. having good output regulation and fast dynamic response.

3.1 State-space averaging technique

In one switching period of DC-DC converters operating in CCM, there exists two power circuit configurations: one is when the MOSFET is conducting and the other when the diode is conducting. Each of these circuit configurations can be represented in the form of differential or state-space equations. Hence, the DC-DC converters are a time varying system over one switching period. The state space averaging technique [5] provides a means to transform this time-varying nonlinear system into the eventual time-invariant linear system. The method of state-space averaging is concisely described below.

A continuous time-varying state-space model has a general form of:

$$\begin{cases} \dfrac{dx}{dt} = A(t)x + B(t)u \\ y = C(t)x + E(t)u \end{cases} \tag{3.1}$$

where $x(n,1)$ is n×1 dimensional state vector;

$y(j,1)$ is j×1 dimensional output vector;

$u(m,1)$ is m×1 dimensional input vector;

$A(n,n)$ is n×n dimensional state matrix;

B(n,m) is n×m dimensional input matrix;

C(j,n) is j×n dimensional output matrix;

E(j,m) is j×m dimensional feedthrough matrix.

For DC-DC converters operating in CCM, the state-space equations that describe the circuit behavior when the MOSFET is turned on and off are expressed by (3.2) and (3.3), respectively.

$$\begin{cases} \dfrac{dx}{dt} = A_1 x + B_1 u \\ y = C_1 x + E_1 u \end{cases} \tag{3.2}$$

$$\begin{cases} \dfrac{dx}{dt} = A_2 x + B_2 u \\ y = C_2 x + E_2 u \end{cases} \tag{3.3}$$

According to the state-space averaging technique, equations (3.2) and (3.3) can be averaged over one switching period, resulting in a single set of state-space averaged equations

$$\begin{cases} \dfrac{dx}{dt} = Ax + Bu \\ y = Cx + Eu \end{cases} \tag{3.4}$$

where the averaged matrices *A, B, C,* and *E* are:

$$A = A_1 d + A_2 (1-d)$$

$$B = B_1 d + B_2 (1-d)$$

$$C = C_1 d + C_2 (1-d)$$

$$E = E_1 d + E_2 (1-d)$$

where *d* is the duty ratio

Equation (3.4) is a nonlinear continuous-time equation and can be linearized by introducing small-signal perturbation into the averaged state-space equations as follows:

$$x = X + \hat{x}$$

$$u = U + \hat{u}$$

$$y = Y + \hat{y}$$

$$d = D + \hat{d}$$

where $X >> \hat{x}$, $U >> \hat{u}$, $Y >> \hat{y}$, and $D >> \hat{d}$. Note that the capital variables represent a DC value and the hat variables a small-signal value.

Substitution of small-signal perturbation into (3.4) results in

$$\begin{cases} \dot{X} + \dot{\hat{x}} = [A_1(D+\hat{d}) + A_2(1-D-\hat{d})](X+\hat{x}) + [B_1(D+\hat{d}) + B_2(1-D-\hat{d})](U+\hat{u}) \\ Y + \hat{y} = [C_1(D+\hat{d}) + C_2(1-D-\hat{d})(X+\hat{x}) + [E_1(D+\hat{d}) + E_2(1-D-\hat{d})](U+\hat{u}) \end{cases} \quad (3.5)$$

Multiplying and rearranging the above equations yields

$$\begin{cases} \dot{X} + \dot{\hat{x}} = AX + BU + A\hat{x} + B\hat{u} + [(A_1 - A_2)X + (B_1 - B_2)U]\hat{d} + (A_1 - A_2)\hat{d}\hat{x} + (B_1 - B_2)\hat{d}\hat{u} \\ Y + \hat{y} = CX + EU + C\hat{x} + E\hat{u} + [(C_1 - C_2)X + (E_1 - E_2)U]\hat{d} + (C_1 - C_2)\hat{d}\hat{x} + (E_1 - E_2)\hat{d}\hat{u} \end{cases} \quad (3.6)$$

Collecting the DC terms from the equations above, we get:

$$\begin{cases} \dot{X} = AX + BU \\ Y = CX + EU \end{cases} \quad (3.7)$$

By solving (3.7), the DC solution can be found as:

$$\begin{cases} X = A^{-1}BU \\ Y = (CA^{-1}B + E)U \end{cases} \quad (3.8)$$

Collecting the small-signal terms in (3.6) and approximating that the product of two small signals can be neglected (i.e. $\hat{d}\hat{x} \approx 0, \hat{d}\hat{u} \approx 0$), we can define the small-signal state-space equations

$$\begin{cases} \dot{\hat{x}} = A\hat{x} + B\hat{u} + [(A_1 - A_2)X + (B_1 - B_2)U]\hat{d} \\ \hat{y} = C\hat{x} + E\hat{u} + [(C_1 - C_2)X + (E_1 - E_2)U]\hat{d} \end{cases} \quad (3.9)$$

or

$$\begin{cases} \dot{\hat{x}} = A\hat{x} + B\hat{u} + B_d\hat{d} \\ \hat{y} = C\hat{x} + E\hat{u} + E_d\hat{d} \end{cases} \quad (3.10)$$

where

$$B_d = (A_1 - A_2)X + (B_1 - B_2)U$$
$$E_d = (C_1 - C_2)X + (E_1 - E_2)U$$

In DC-DC converter, the input variable $\hat{u}$ is usually contains the input voltage and load current. Hence, $\hat{u}$ is express as $\hat{u} = [\hat{u}_1 \quad \hat{u}_2]^T$, the input matrix B as $B=[B_{u1}\ B_{u2}]$ and the feedthrough matrix E as $E=[E_{u1}\ E_{u2}]$. Therefore, (3.10) is rewritten as:

$$\begin{cases} \dot{\hat{x}} = A\hat{x} + \begin{bmatrix} B_{u1} & B_{u2} & B_d \end{bmatrix} \begin{bmatrix} \hat{u}_1 \\ \hat{u}_2 \\ \hat{d} \end{bmatrix} \\ \hat{y} = C\hat{x} + \begin{bmatrix} E_{u1} & E_{u2} & E_d \end{bmatrix} \begin{bmatrix} \hat{u}_1 \\ \hat{u}_2 \\ \hat{d} \end{bmatrix} \end{cases} \tag{3.11}$$

By applying the Laplace transform to (3.11), the converters' transfer functions can be determined as:

$$\begin{cases} \hat{x}(s) = \begin{bmatrix} [sI-A]^{-1}B_{u1} & [sI-A]^{-1}B_{u2} & [sI-A]^{-1}B_d \end{bmatrix} \begin{bmatrix} \hat{u}_1(s) \\ \hat{u}_2(s) \\ \hat{d}(s) \end{bmatrix} \\ \hat{y}(s) = \begin{bmatrix} C[sI-A]^{-1}B_{u1} + E_{u1} & C[sI-A]^{-1}B_{u2} + E_{u2} & C[sI-A]^{-1}B_d + E_d \end{bmatrix} \begin{bmatrix} \hat{u}_1(s) \\ \hat{u}_2(s) \\ \hat{d}(s) \end{bmatrix} \end{cases} \tag{3.12}$$

In general, the state variable of interest can be separated from (3.12)

$$\hat{x}_i(s) = C_i \hat{x}(s) \tag{3.13}$$

where

$$C_i = \begin{bmatrix} 0 & 0 & \dots & 1_{i^{th}} & \dots & 0 \end{bmatrix}$$

Collecting $\hat{x}_i(s)$ and $\hat{y}(s)$ from (3.12) and (3.13), we get:

$$\begin{cases} \hat{x}_i(s) = \begin{bmatrix} C_i[sI-A]^{-1}B_{u1} & C_i[sI-A]^{-1}B_{u2} & C_i[sI-A]^{-1}B_d \end{bmatrix} \begin{bmatrix} \hat{u}_1(s) \\ \hat{u}_2(s) \\ \hat{d}(s) \end{bmatrix} \\ \hat{y}(s) = \begin{bmatrix} C[sI-A]^{-1}B_{u1}+E_{u1} & C[sI-A]^{-1}B_{u2}+E_{u2} & C[sI-A]^{-1}B_d+E_d \end{bmatrix} \begin{bmatrix} \hat{u}_1(s) \\ \hat{u}_2(s) \\ \hat{d}(s) \end{bmatrix} \end{cases} \quad (3.14)$$

Rewriting (3.14) in matrix form

$$\begin{bmatrix} \hat{x}_i(s) \\ \hat{y}(s) \end{bmatrix} = \begin{bmatrix} G_{vi}(s) & G_{zi}(s) & G_{di}(s) \\ G_{vv}(s) & G_{zv}(s) & G_{dv}(s) \end{bmatrix} \begin{bmatrix} \hat{u}_1(s) \\ \hat{u}_2(s) \\ \hat{d}(s) \end{bmatrix} \quad (3.15)$$

where

$$G_{vv}(s) = C[sI-A]^{-1}B_{u1} + E_{u1}$$
$$G_{zv}(s) = C[sI-A]^{-1}B_{u2} + E_{u2}$$
$$G_{dv}(s) = C[sI-A]^{-1}B_d + E_d$$
$$G_{vi}(s) = C_i[sI-A]^{-1}B_{u1}$$
$$G_{zi}(s) = C_i[sI-A]^{-1}B_{u2}$$
$$G_{di}(s) = C_i[sI-A]^{-1}B_d$$

3.2 Modeling of buck converter by the state-space averaging technique

A buck converter is shown in Fig. 3.1(a). The resistor R is a standing load, the current source I_z models a load current disturbance and r_c is an Equivalent Series Resistance (ESR) of the capacitor C. In CCM, the converter exhibits two power circuit configurations in one switching period.

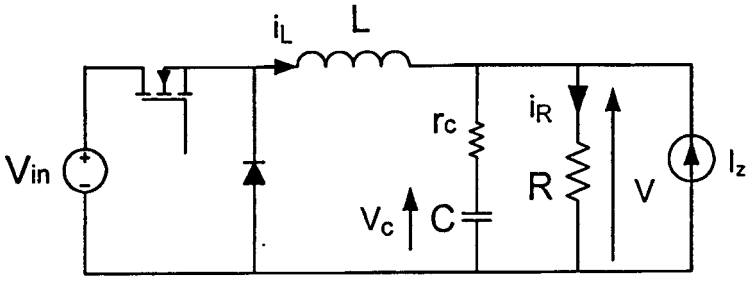
The first circuit configuration is when the MOSFET is turned on (Fig. 3.1(b)). The circuit equations for this interval can be written as follows:

$$V_L = L\frac{di_L}{dt} = V_{in} - V \quad (3.16)$$

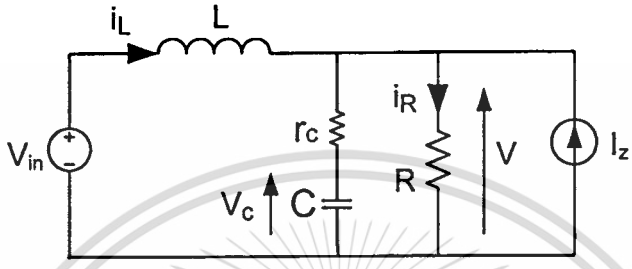
$$i_L + I_Z = i_c + i_R \quad (3.17)$$

$$i_c = C\frac{dv_c}{dt} \quad (3.18)$$

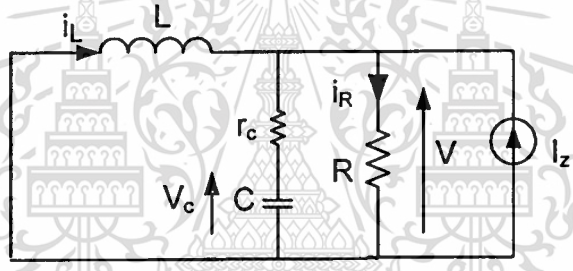
$$V = R.i_R = v_c + r_c.i_c \quad (3.19)$$



(a) Buck Converter



(b) Buck Converter when MOSFET is on



(c) Buck Converter when MOSFET is off

Fig 3.1 Modeling of buck converter

The inductor current i_L and capacitor voltage V_c are chosen as the state variables, the input voltage V_{in} and the additional load current I_z as the input variables, and the output voltage V as the output vector. By rearranging the above equations (see Appendix A for detail), we can obtain the state-space equations:

$$\begin{cases} \begin{bmatrix} i_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} \dfrac{-R.r_c}{L(R+r_c)} & \dfrac{-R}{L(R+r_c)} \\ \dfrac{R}{C(R+r_c)} & \dfrac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} & \dfrac{-R.r_c}{L(R+r_c)} \\ 0 & \dfrac{R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \\ V = \begin{bmatrix} \dfrac{R.r_c}{R+r_c} & \dfrac{R}{R+r_c} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & \dfrac{R.r_c}{R+r_c} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \end{cases} \tag{3.20}$$

The second circuit configuration is when the MOSFET is turned off (Fig. 3.1(c)). The circuit equations for this interval can be written as follows:

$$V_L = L\frac{di_L}{dt} = -V \tag{3.21}$$

$$i_L + I_Z = i_c + i_R \tag{3.22}$$

$$i_c = C\frac{dv_c}{dt} \tag{3.23}$$

$$V = R.i_R = v_c + r_c.i_c \tag{3.24}$$

Rearranging the above equations (see Appendix A for detail), the state-space equations for this second interval can be written as:

$$\begin{cases} \begin{bmatrix} \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} \frac{-R.r_c}{L(R+r_c)} & \frac{-R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & \frac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & \frac{-R.r_c}{L(R+r_c)} \\ 0 & \frac{R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \\ V = \begin{bmatrix} \frac{R.r_C}{R+r_C} & \frac{R}{R+r_C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & \frac{R.r_c}{R+r_c} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \end{cases} \tag{3.25}$$

The averaged state-space equations of the buck converter can be obtained by averaging (3.20) and (3.25) in accordance with (3.4):

$$\begin{cases} \begin{bmatrix} \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} \frac{-R.r_c}{L(R+r_c)} & \frac{-R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & \frac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{d}{L} & \frac{-R.r_c}{L(R+r_c)} \\ 0 & \frac{R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \\ V = \begin{bmatrix} \frac{R.r_C}{R+r_C} & \frac{R}{R+r_C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & \frac{R.r_c}{R+r_c} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \end{cases} \tag{3.26}$$

According to (3.8) and (3.10), the DC values and matrix B_d and E_d can be found from (3.26):

$$\begin{bmatrix} I_L \\ V_c \end{bmatrix} = \frac{R}{R+r_c} \begin{bmatrix} \frac{D}{R} & \frac{r_c - R}{R} \\ D & 0 \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix}$$

$$V = DV_{in}$$

$$B_d = \begin{bmatrix} \frac{V_{in}}{L} \\ 0 \end{bmatrix}$$

$$E_d = 0$$

Equation (3.26) is nonlinear due to the multiplication of the independent input variables d and V_{in}. Linearising (3.26) in accordance with (3.11), the linear small-signal state-space equations are obtained as:

$$\begin{cases} \begin{bmatrix} \dot{\hat{i}}_L \\ \dot{\hat{v}}_c \end{bmatrix} = \begin{bmatrix} \dfrac{-R.r_c}{L(R+r_c)} & \dfrac{-R}{L(R+r_c)} \\ \dfrac{R}{C(R+r_c)} & \dfrac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_c \end{bmatrix} + \begin{bmatrix} \dfrac{D}{L} & \dfrac{-R.r_c}{L(R+r_c)} & \dfrac{V_{in}}{L} \\ 0 & \dfrac{R}{C(R+r_c)} & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_z \\ \hat{d} \end{bmatrix} \\ \hat{v} = \begin{bmatrix} \dfrac{R.r_c}{R+r_c} & \dfrac{R}{R+r_c} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_c \end{bmatrix} + \begin{bmatrix} 0 & \dfrac{R.r_c}{R+r_c} & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_z \\ \hat{d} \end{bmatrix} \end{cases} \tag{3.27}$$

By applying the Laplace transform to (3.27) and following the steps in (3.12)-(3.14), the output voltage and the inductor current can be expressed:

$$\begin{bmatrix} \hat{i}_L(s) \\ \hat{v}(s) \end{bmatrix} = \begin{bmatrix} G_{vi}(s) & G_{zi}(s) & G_{di}(s) \\ G_{vv}(s) & G_{zv}(s) & G_{dv}(s) \end{bmatrix} \begin{bmatrix} \hat{v}_{in}(s) \\ \hat{i}_z(s) \\ \hat{d}(s) \end{bmatrix} \tag{3.28}$$

where $G_{vv}(s)$, $G_{zv}(s)$ and $G_{dv}(s)$ are the transfer functions from the input voltage $\hat{v}_{in}(s)$, load current $\hat{i}_Z(s)$ and duty ratio $\hat{d}(s)$ to the output voltage $\hat{v}(s)$, respectively. $G_{vi}(s)$, $G_{zi}(s)$ and $G_{di}(s)$ are the transfer functions from the input voltage $\hat{v}_{in}(s)$ load current $\hat{i}_Z(s)$ and duty ratio $\hat{d}(s)$ to inductor current $\hat{i}_L(s)$, respectively.

$G_{dv}(s)$ and $G_{di}(s)$ will be used in the control design of ACMC. Its transfer functions can be determined as (see Appendix A for detail):

$$G_{dv}(s) = \begin{bmatrix} \dfrac{R.r_c}{R+r_c} & \dfrac{R}{R+r_c} \end{bmatrix} \left(\begin{bmatrix} s & 0 \\ 0 & s \end{bmatrix} - \begin{bmatrix} \dfrac{-R.r_c}{L(R+r_c)} & \dfrac{-R}{L(R+r_c)} \\ \dfrac{R}{C(R+r_c)} & \dfrac{-1}{C(R+r_c)} \end{bmatrix} \right)^{-1} \begin{bmatrix} \dfrac{V_{in}}{L} \\ 0 \end{bmatrix} \tag{3.29}$$

$$G_{dv}(s) = \frac{V_{in}}{LC} \frac{1 + sr_cC}{s^2 + s\left(\dfrac{1}{RC} + \dfrac{r_c}{L}\right) + \dfrac{1}{LC}} \tag{3.30}$$

$$G_{di}(s)=\begin{bmatrix}1 & 0\end{bmatrix}\left[\begin{bmatrix}s & 0\\ 0 & s\end{bmatrix}-\begin{bmatrix}\frac{-R.r_c}{L(R+r_c)} & \frac{-R}{L(R+r_c)}\\ \frac{R}{C(R+r_c)} & \frac{-1}{C(R+r_c)}\end{bmatrix}\right]^{-1}\begin{bmatrix}\frac{V_{in}}{L}\\ 0\end{bmatrix} \tag{3.31}$$

$$G_{di}(s)=\frac{V_{in}}{LCR}\frac{1+s(R+r_c)C}{s^2+s\left(\frac{1}{RC}+\frac{r_c}{L}\right)+\frac{1}{LC}} \tag{3.32}$$

3.3 Modeling of control stage

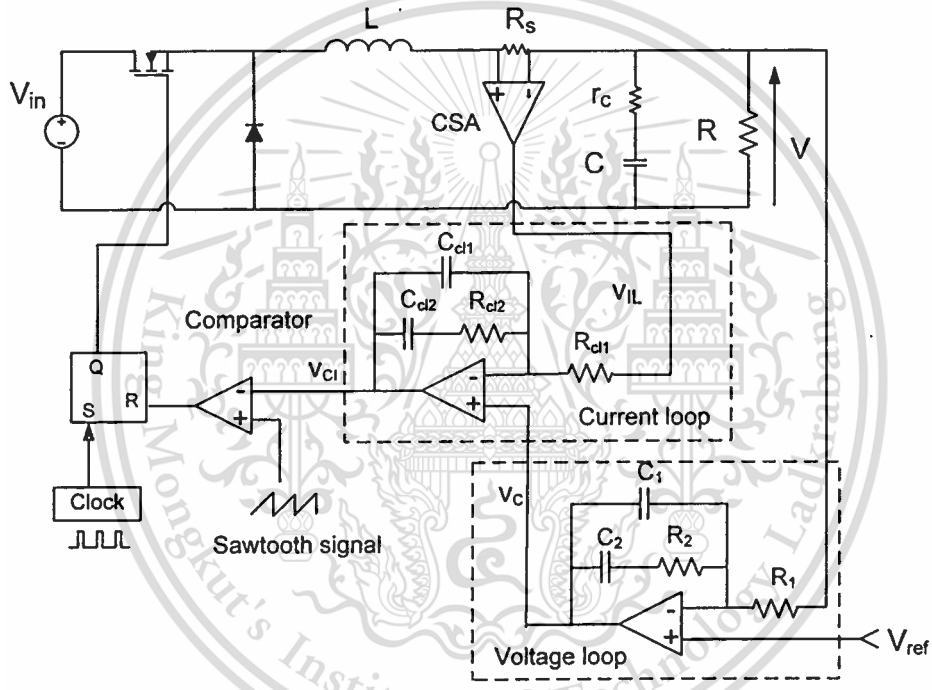


Fig 3.2 Buck converter with Average Current Mode Control

A buck converter with ACMC is shown in Fig. 3.2. The operation of ACMC has already been described in Chapter 2. Here, the focus is on small-signal modeling of this control method. As can be seen in Fig. 3.2, ACMC uses the current error amplifier and the output voltage error amplifier to force the inductor current and output voltage to track their reference values V_c and V_{ref} respectively. Connected around these amplifiers are a compensation circuit comprising of R's and C's. The compensation circuit allows the frequency response of each loop to be adjusted to meet the desired characteristics, i.e. high DC gain and wide bandwidth. From here on, the compensated current error

amplifier and compensated output voltage error amplifier will be denoted as the current controller and voltage controller respectively.

3.3.1 Small-signal model of current controller

From Fig. 3.2, the current controller output v_{ci} is related to the control signal v_c and the sensed inductor current v_{iL} as:

$$v_{ci} = v_c(1 + \frac{z_{cl2}}{z_{cl1}}) - \frac{z_{cl2}}{z_{cl1}} v_{iL} \tag{3.33}$$

where

$$z_{cl2} = \frac{1 + sR_{cl2}C_{cl2}}{s(sR_{cl2}C_{cl2}C_{cl1} + C_{cl2} + C_{cl1})}$$

$$z_{cl1} = R_{cl1}$$

V_{iL} comes from the output of Current Sensing Amplifier (CSA) which amplifies the inductor current sensed across R_s. Suppose that A_{CL} is the CSA's gain, and then V_{iL} is given by:

$$V_{iL} = R_i . i_L \tag{3.34}$$

where

$$R_i = A_{CL} . R_S$$

By introducing the perturbed signals $v_{ci} = V_{cl} + \hat{v}_{ci}$, $v_c = V_c + \hat{v}_c$, and $v_{iL} = V_{iL} + \hat{v}_{iL}$ into (3.33) and collecting only the small signal terms, the small-signal model of the current controller can be written:

$$\hat{v}_{ci} = \hat{v}_c(1 + \frac{z_{cl2}}{z_{cl1}}) - \frac{z_{cl2}}{z_{cl1}} \hat{v}_{iL} \tag{3.35}$$

$$\hat{v}_{ci} = \hat{v}_c(1 + G_{cl}(s)) - G_{cl}(s)\hat{v}_{iL} \tag{3.36}$$

where $G_{cl}(s)$ is given by:

$$G_{cl}(s) = \frac{z_{cl2}}{z_{cl1}} = \frac{w_{cl}}{s} \frac{1 + \frac{s}{w_{clz}}}{1 + \frac{s}{w_{clp}}} \tag{3.37}$$

with

$$w_{cl} = \frac{1}{R_{cl1}(C_{cl1} + C_{cl2})}$$

$$w_{clz} = \frac{1}{R_{cl2} . C_{cl2}}$$

$$w_{clp} = \frac{C_{cl1} + C_{cl2}}{R_{cl2} . C_{cl1} . C_{cl2}}$$

3.3.2 Small-signal model of voltage controller

In Fig. 3.2, the control signal v_c is related to the reference voltage V_{ref} and the output voltage v, as defined by:

$$v_c = v_{ref}\left(1+\frac{z_{c2}}{z_{c1}}\right)-\frac{z_{c2}}{z_{c1}}v \tag{3.38}$$

where

$$z_{c2} = \frac{1+sR_{c2}C_{c2}}{s(sR_{c2}C_{c2}C_{c1}+C_{c2}+C_{c1})}$$

$$z_{c1} = R_{c1}$$

By introducing the perturbed signal $v = V+\hat{v}$, $v_c = V_c+\hat{v}_c$ and V_{ref} being constant into (3.38) and collecting only the small signal terms, the small-signal model of the voltage controller can be written:

$$\hat{v}_c = -\frac{z_{c2}}{z_{c1}}\hat{v} = -G_{c(s)}\hat{v} \tag{3.39}$$

where

$$G_c(s) = \frac{z_{c2}}{z_{c1}} = \frac{w_c}{s}\frac{1+\frac{s}{w_z}}{1+\frac{s}{w_p}} \tag{3.40}$$

with

$$w_c = \frac{1}{R_1(C_1+C_2)}$$

$$w_z = \frac{1}{R_2.C_2}$$

$$w_p = \frac{C_1+C_2}{R_2.C_1.C_2}$$

3.3.3 Small-signal model of PWM modulator

The duration which the MOSFET switch conducts is determined by comparing V_{ci} and the sawtooth signal as shown in Fig. 3.3. From the figure, the following relationship can be derived

$$\frac{V_{ci}}{V_P} = \frac{t_{on}}{T} = d \tag{3.41}$$

Therefore, the small signal model of the PWM modulator is expressed as:

$$\hat{d} = F_m \hat{V}_{ci} \tag{3.42}$$

where $F_m = \frac{1}{V_P}$ is the PWM modulator gain and V_p is the peak to peak sawtooth voltage.

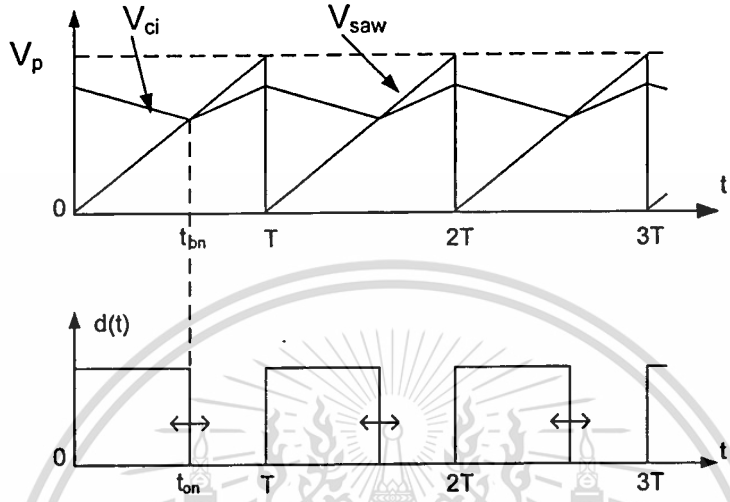


Fig 3.3 PWM control wave form of ACMC in Fig. 3.2

3.4 Small signal analysis of ACMC

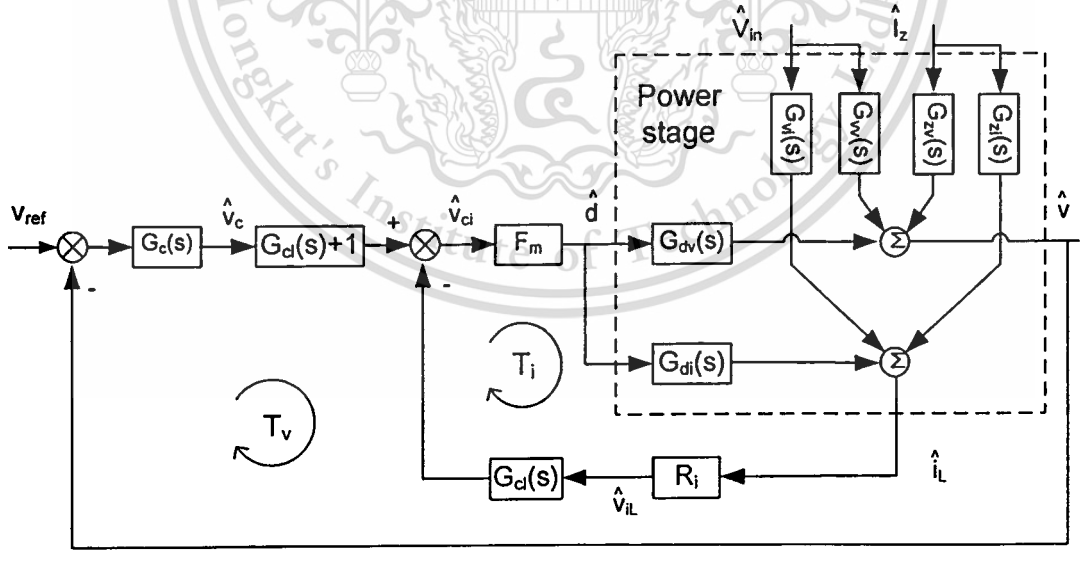


Fig 3.4 Small signal model of buck converter with ACMC

The small signal model of buck converter with ACMC is illustrated in Fig. 3.4. The power stage of buck converter is represented by the six transfer functions as given in (3.28). $\hat{v}_{in}$, $\hat{i}_z$ and $\hat{d}$ are

the input variables, and $\hat{v}$ and $\hat{i}_L$ the output variables. Whilst $\hat{d}$ is a dependent variable as it is generated by the feedback loop, $\hat{v}_{in}$ and $\hat{i}_z$ are an independent variable and can be a source of system disturbances. The control stage in Fig. 3.4 is formed by (3.34), (3.37), (3.40), and (3.42).

Since $\hat{v}_{in}$ and $\hat{i}_z$ are the independent variables, they are usually assumed to be zero to ease the control design. As a result, the model in Fig. 3.5 is obtained and used for the control design purpose. The transfer functions $G_{dv}(s)$ and $G_{di}(s)$ have been determined earlier and given in (3.30) and (3.32), respectively.

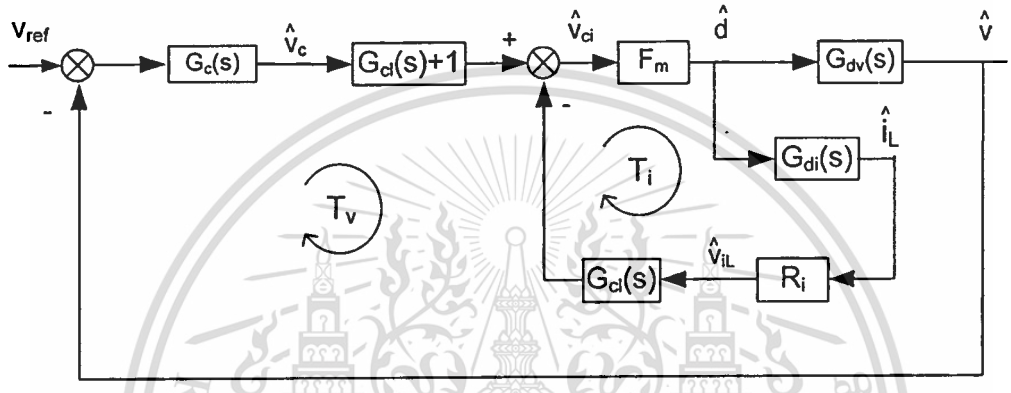


Fig 3.5 Small signal model with $\hat{v}_{in}$ and $\hat{i}_z$ set equal to zero

3.4.1 Current loop design

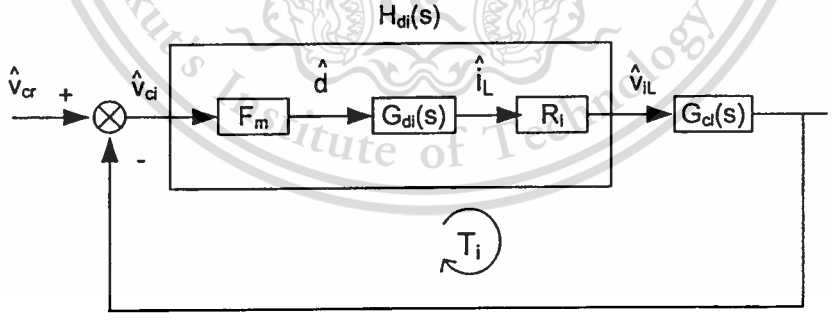


Fig 3.6 Small signal model of current loop

Fig 3.6 shows the current loop section of the small-signal model in Fig 3.5. The transfer function of $H_{di}(s)$ is defined as

$$H_{di}(s) = F_m . R_i . G_{di}(s) \tag{3.43}$$

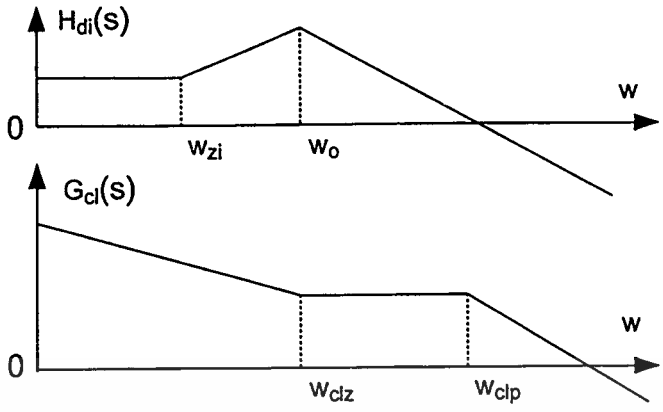


Fig 3.7 Asymptotic Bode plots of $G_{cl}(s)$ and $H_{di}(s)$

Since F_m and R_i are constant, the characteristic of $H_{di}(s)$ therefore follows that of $G_{di}(s)$ derived in (3.32). The asymptotic Bode plots of $H_{di}(s)$ and $G_{cl}(s)$ in (3.37) are shown in Fig. 3.7. The integrator (pole at origin of $G_{cl}(s)$) is used to boost the DC gain of $H_{di}(s)$, the zero of $G_{cl}(s)$ is placed at the resonant frequency of $H_{di}(s)$ and another pole of $G_{cl}(s)$ is placed at high frequency below the switching frequency f_s.

The optimum gain of $G_{cl}(s)$ at the switching frequency is defined in (3.44) [2].

$$\max |G_{cl}| = \frac{V_P.f_s.L}{V.R_i}$$
$$|G_{cl}(jw_s)| \le \max |G_{cl}| \tag{3.44}$$

where f_s is the switching frequency

V_P is a peak to peak of sawtooth voltage

In ACMC, although (3.44) is satisfied the switching instability still occurs if the input voltage is too high or the duty ratio too low. To avoid these, the current controller's gain is limited to (3.45) [3]

$$|G_{cl}(jw_s)| \le 2\frac{V_P.f_s.L}{(V_{in,\max}-V)R_i} \tag{3.45}$$

In designing the current controller, the maximum allowable current loop gain, hence, can be defined in (3.46):

$$|G_{cl}(jw_s)| \le \min\left(2\frac{V_P.f_s.L}{(V_{in,\max}-V)R_i}, \frac{V_P.f_s.L}{V.R_i}\right) \tag{3.46}$$

3.4.2 Voltage loop design

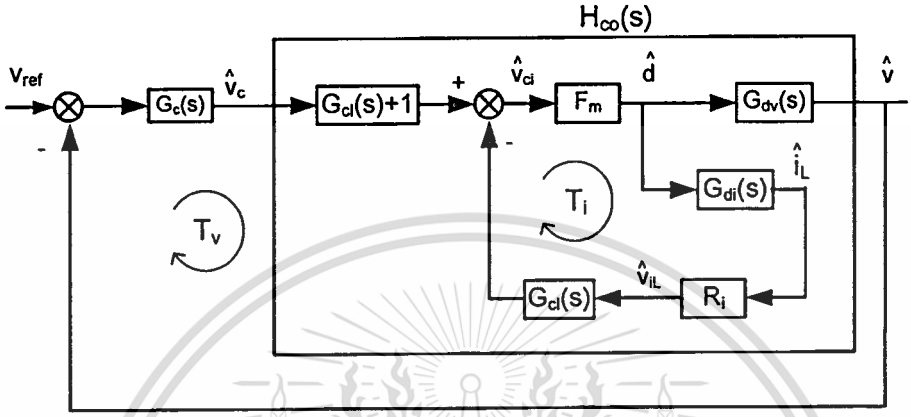


Fig 3.8 Small signal model of voltage loop

In Fig. 3.8, the output voltage of buck converter is compared with the reference signal to form an error voltage. The voltage controller $G_c(s)$ then amplifies the error voltage to generate the control signal $\hat{v}_c$ to regulate the output voltage. The output performance of the converter depends on how well $G_c(s)$ in (3.40) is designed. Good design must assure that the converter has good output regulation, fast dynamic response and stable operation. In control point of view, $G_c(s)$ must be designed to compensate the transfer function $H_{co}(s)$ to yield the open loop transfer function the desired frequency response.

From Fig. 3.8, $H_{co}(s)$ is defined as:

$$H_{co}(s) = [G_{cl}(s)+1].G_{dv}(s).T_i^{'} \tag{3.47}$$

where

$$T_i^{'} = \frac{F_m}{1+F_m R_i G_{di}(s) G_{cl}(s)}$$

The general form of $H_{co}(s)$ can be written as (see Appendix D for detail):

$$H_{co}(s) = H_c \frac{b_3 s^3 + b_2 s^2 + b_1 s + b_0}{s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{3.48}$$

where

$$H_c = \frac{F_m V_{in}}{LC}$$

$$b_3 = r_c C$$

$$b_2 = 1 + r_c C\left(w_{clp} + \frac{w_{cl} w_{clp}}{w_{clz}}\right)$$

$$b_1 = \left(w_{clp} + \frac{w_{cl} w_{clp}}{w_{clz}}\right) + r_c C w_{cl} w_{clp}$$

$$b_0 = w_{cl} w_{clp}$$

$$\alpha = \frac{F_m R_i V_{in} w_{cl}}{w_{clz}}$$

$$\beta = \frac{LCR}{w_{clp}}$$

$$a_3 = w_{clp} + \frac{1}{RC} + \frac{r_c}{L}$$

$$a_2 = w_{clp}\left(\frac{1}{RC} + \frac{r_c}{L}\right) + \frac{1}{LC} + \frac{\alpha RC}{\beta}$$

$$a_1 = \frac{w_{clp}}{LC} + \frac{\alpha\left(1 + w_{clz} RC\right)}{\beta}$$

$$a_0 = \frac{\alpha w_{clz}}{\beta}$$

$G_c(s)$ is a voltage controller shown in (3.40), and it has one zero and two poles. The integrator (pole at origin) of $G_c(s)$ is used to boost up DC gain of $H_{cv}(s)$, another pole is placed at one-third of switching frequency to attenuate high frequency noise and its zero is placed at a proper location to assure the stability of the system.

Chapter 4

Two Novel Techniques to Improve Dynamic Response of Converter

In this Chapter, two novel techniques to enhance output dynamic performance of the buck converter with ACMC are proposed. They are: (1) ACMC with a parallel controller (ACMC-P), and (2) Current Feedforward Average Current Mode Control (CFACMC). The former technique is based on the use of a high-order controller to compensate a high-order control–to–output transfer function of the voltage loop. The high-order controller is synthesized from parallel connection of a two basic controllers. The latter technique is based on feedforward of the sensed inductor current signal to add with the output signal from the voltage controller to produce the control signal. These proposed methods can lead to a considerable improvement in the dynamic response of the converter when subjected to load current disturbances.

4.1 ACMC with a parallel controller (ACMC-P)

4.1.1 Insufficiency of a conventional voltage controller

Fig. 4.1 shows a circuit configuration of the typical controller used in the current and voltage loops of ACMC.

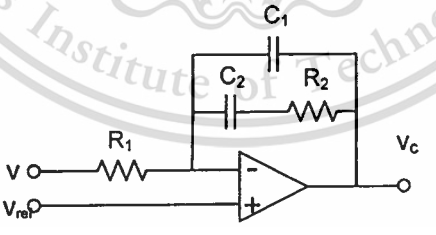


Fig 4.1 2-pole 1-zero controller

The controller has 2 poles and 1 zero and its transfer function is expressed by (3.37) and (3.40). When applied to the current loop (Section 3.4), the controller contains a sufficient number of poles and zeros to compensate the transfer function $H_{di}(s)$ as illustrated in Fig. 3.7. Therefore, good current loop performance can be expected from the use of this controller with the properly placed poles and zero. However, when applied to the voltage loop, the suitability of this controller is questionable.

Recall the control-to-output transfer function $H_{co}(s)$ of the voltage loop in (3.48), which is reproduced here in (4.1).

$$H_{co}(s) = H_c \frac{b_3 s^3 + b_2 s^2 + b_1 s + b_0}{s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{4.1}$$

where

$$H_c = \frac{F_m V_{in}}{LC}$$

$$b_3 = r_c C$$

$$b_2 = 1 + r_c C\left(w_{clp} + \frac{w_{cl} w_{clp}}{w_{clz}}\right)$$

$$b_1 = \left(w_{clp} + \frac{w_{cl} w_{clp}}{w_{clz}}\right) + r_c C w_{cl} w_{clp}$$

$$b_0 = w_{cl} w_{clp}$$

$$\alpha = \frac{F_m R_i V_{in} w_{cl}}{w_{clz}}$$

$$\beta = \frac{LCR}{w_{clp}}$$

$$a_3 = w_{clp} + \frac{1}{RC} + \frac{r_c}{L}$$

$$a_2 = w_{clp}\left(\frac{1}{RC} + \frac{r_c}{L}\right) + \frac{1}{LC} + \frac{\alpha RC}{\beta}$$

$$a_1 = \frac{w_{clp}}{LC} + \frac{\alpha\left(1 + w_{clz} RC\right)}{\beta}$$

$$a_0 = \frac{\alpha w_{clz}}{\beta}$$

$H_{co}(s)$ is a high-order transfer function which contains 4 poles and 3 zeros. Apparently, the 2-pole 1-zero controller in Fig. 4.1 does not have an enough number of poles and zeros to properly compensate $H_{co}(s)$. As a result, the output dynamic response of the converter will be somewhat limited by the use of this conventional controller.

To compensate $H_{co}(s)$ in (4.1), a high-order controller $G_{c3}(s)$ in (4.2) is proposed.

$$G_{c3}(s) = k\frac{(s + w_{cz1})(s + w_{cz2})(s + w_{cz3})(s + w_{cz4})}{s(s + w_{cp1})(s + w_{cp2})(s + w_{cp3})} \tag{4.2}$$

The controller has 4 poles and 4 zeros which are sufficient to cancel the poles and zeros of $H_{co}(s)$. Such a high-order controller is, however, difficult to realize by a single OpAmp circuit. One way to synthesize $G_{c3}(s)$ in *(4.2)* is to use two basic controllers and connect them in parallel. This is discussed in the next section. For ease of synthesis, the numerator of $G_{c3}(s)$ in (4.2) is rewritten in a polynomial form as

$$G_{c3}(s) = k\frac{s^4 + c_3 s^3 + c_2 s^2 + c_1 s + c_0}{s(s + w_{cp1})(s + w_{cp2})(s + w_{cp3})} \tag{4.3}$$

where

$$c_3 = w_{cz1} + w_{cz2} + w_{cz3} + w_{cz4}$$

$$c_2 = w_{cz1}w_{cz2} + (w_{cz1} + w_{cz2})(w_{cz3} + w_{cz4}) + w_{cz3}w_{cz4}$$

$$c_1 = w_{cz1}w_{cz2}(w_{cz3} + w_{cz4}) + w_{cz3}w_{cz4}(w_{cz1} + w_{cz2})$$

$$c_0 = w_{cz1}w_{cz2}w_{cz3}w_{cz4}$$

4.1.2 Synthesis of a parallel controller

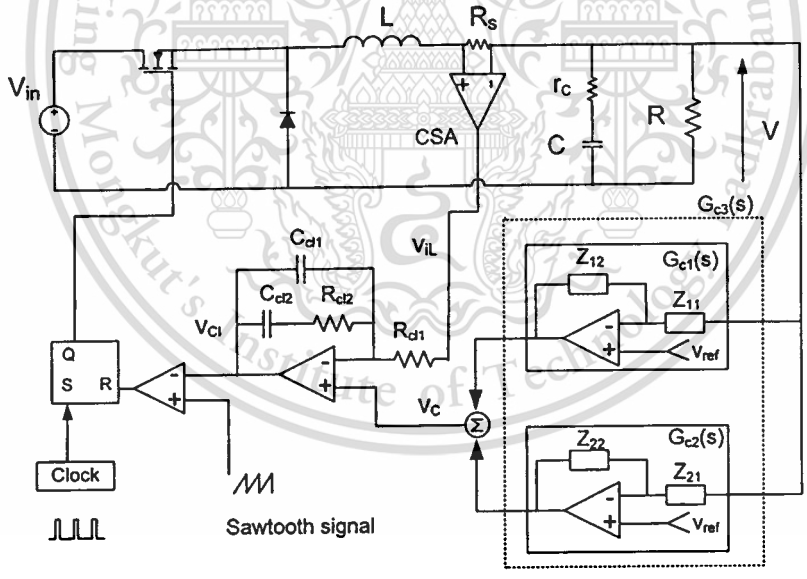
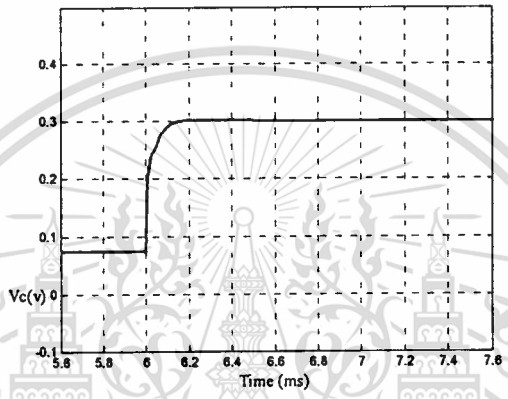


Fig 4.2 Circuit configuration of ACMC-P

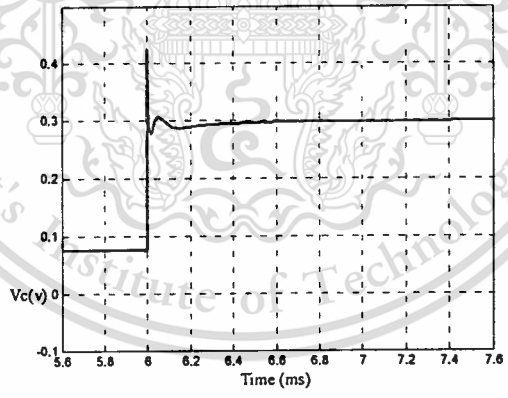
Fig. 4.2 shows the ACMC buck converter with the controller $G_{c3}(s)$ synthesized from parallel connection of a two basic controllers $G_{c1}(s)$ and $G_{c2}(s)$. The two constituent controllers receive the same feedback and reference voltages. The output signal generated by each controller is summed together to produce the control signal V_c. Because of the summation, the corrective action given by $G_{c3}(s)$ is

stronger than that would be gotten from $G_{c1}(s)$ or $G_{c2}(s)$ alone. This is analogues to PID controller, in which contribution from the P, I, D elements together results in a stronger corrective action than acting alone by the individual element.

Fig. 4.3 shows a comparison between the controls signal in the conventional ACMC and the ACMC-P. In both cases, after a step load change V_c is increased to correct the output voltage drop, but the initial magnitude of V_c in the parallel controller is higher, causing the output voltage to resettle quickly to the desired value.



(a) Control signal ACMC



(b) Control signal ACMC-P

Fig 4.3 Control signal

The strong corrective action helps fasten the system dynamic, but, if too strong, it can be a cause of instability. This trade-off must be taken into consideration when designing $G_{c3}(s)$. Hence if it's properly designed, the parallel controller is capable of yielding a faster output dynamic response than the conventional controller.

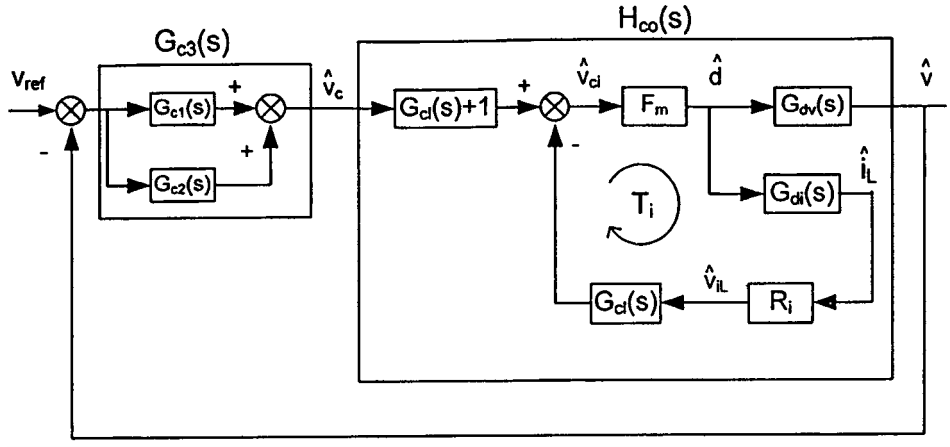
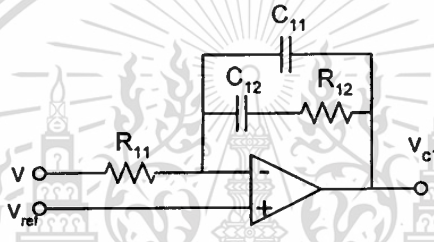
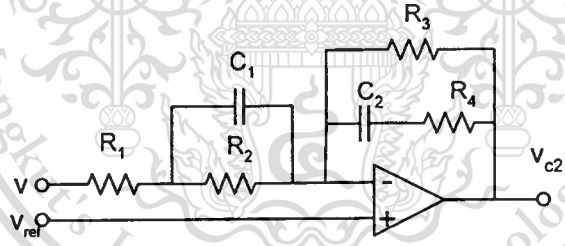


Fig 4.4 Small-signal model Buck converter with ACMC-P



(a) 2-pole 1-zero controller $G_{c1}(s)$



(b) 2-pole 2-zero controller $G_{c2}(s)$

Fig 4.5 Synthesis of parallel controller

The small-signal model of the converter in Fig. 4.2 is shown in Fig. 4.4. In control point of view, two transfer functions connected in parallel result in a new transfer function whose value is equal to the addition of the two transfer functions. The parallel controller $G_{c3}(s)$ is therefore equal to $G_{c1}(s)$ + $G_{c2}(s)$. To synthesize $G_{c3}(s)$ in (4.2) or (4.3), $G_{c1}(s)$ is chosen to be the 2-pole 1-zero controller in Fig. 4.3(a) and $G_{c2}(s)$ the 2-pole 2-zero controller in Fig. 4.3(b). $G_{c1}(s)$ is described by

$$G_{c1}(s) = \frac{v_{c1}}{v} = \frac{k_1}{s}\frac{s + w_a}{s + w_{cp2}} \tag{4.4}$$

where

$$k_1 = \frac{1}{R_{11}.C_{11}}$$

$$w_a = \frac{1}{R_{12}.C_{12}}$$

$$w_{cp2} = \frac{C_{11} + C_{12}}{R_{12}.C_{11}.C_{12}}$$

$G_{c2}(s)$ is described by

$$G_{c2}(s) = \frac{v_{c2}}{v} = k_2 \frac{(s + w_\beta)(s + w_\gamma)}{(s + w_{cp1})(s + w_{cp3})} \tag{4.5}$$

where

$$k_2 = \frac{R_3 R_4 C_1}{(R_3 + R_4) R_1 C_2}$$

$$w_\beta = \frac{1}{R_4.C_2}$$

$$w_\gamma = \frac{1}{R_2.C_1}$$

$$w_{cp1} = \frac{1}{(R_3 + R_4)C_2}$$

$$w_{cp3} = \frac{(R_1 + R_2)}{R_2.R_1.C_2}$$

Thus, $G_{c3}(s)$ is equal to

$$G_{c3}(s) = G_{c1}(s) + G_{c2}(s) = \frac{k_1}{s} \frac{s + w_a}{s + w_{cp2}} + k_2 \frac{(s + w_\beta)(s + w_\gamma)}{(s + w_{cp1})(s + w_{cp3})} \tag{4.6}$$

$$G_{c3}(s) = k_2 \frac{s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{s(s + w_{cp2})(s + w_{cp1})(s + w_{cp3})} \tag{4.7}$$

where

$$a_3 = \frac{k_2(w_\gamma + w_\beta + w_{cp2}) + k_1}{k_2}$$

$$a_2 = \frac{k_2((w_\gamma + w_\beta)w_{cp2} + w_\gamma w_\beta) + k_1(w_a + w_{cp1} + w_{cp2})}{k_2}$$

$$a_1 = \frac{k_2 w_\gamma w_\beta w_{cp2} + k_1(w_{cp1} w_{cp3} + w_a(w_{cp1} + w_{cp3}))}{k_2}$$

$$a_0 = \frac{k_1}{k_2} w_a w_{cp1} w_{cp3}$$

By matching the gain and coefficients on the numerator of (4.7) to those of (4.3), a set of equations in (4.8) is obtained.

$$\begin{cases} k_2 = k & (1) \\ \dfrac{k_1}{k_2} w_\alpha w_{cp1} w_{cp3} = c_0 & (2) \\ \dfrac{k_2 w_\gamma w_\beta w_{cp2} + k_1[w_{cp1} w_{cp3} + w_\alpha (w_{cp1} + w_{cp3})]}{k_2} = c_1 & (3) \\ \dfrac{k_2[(w_\gamma + w_\beta) w_{cp2} + w_\gamma w_\beta] + k_1 (w_\alpha + w_{cp1} + w_{cp2})}{k_2} = c_2 & (4) \\ \dfrac{k_2 (w_\gamma + w_\beta + w_{cp2}) + k_1}{k_2} = c_3 & (5) \end{cases} \tag{4.8}$$

Once the location of poles and zeros of $G_{c3}(s)$ in (4.3) has been determined, i.e. w_{cp1}, w_{cp2}, w_{cp3}, c_0, c_1, c_2, c_3, and k are known, we can find the unknown parameters of $G_{c1}(s)$ in (4.4) and $G_{c2}(s)$ in (4.5), i.e. w_{cp1}, w_{cp2}, w_{cp3}, w_α w_β, w_γ, and k_2, by solving (4.8) (see Appendix B for detail).

4.2 Current Feedforward Average Current Mode Control (CFACMC)

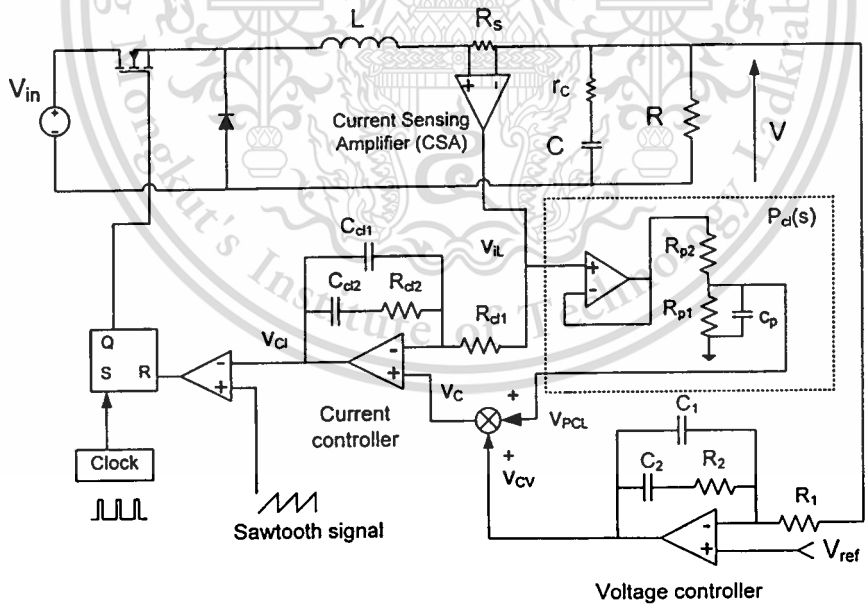
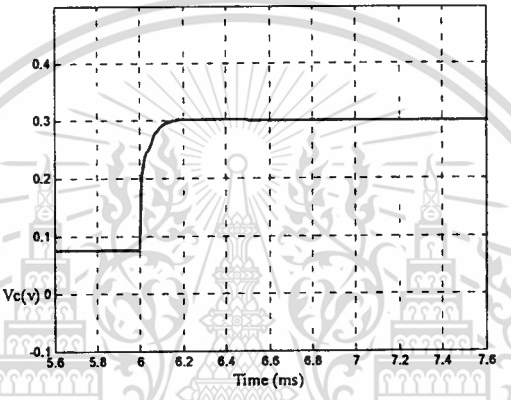


Fig 4.6 Buck converter with the proposed CFACMC

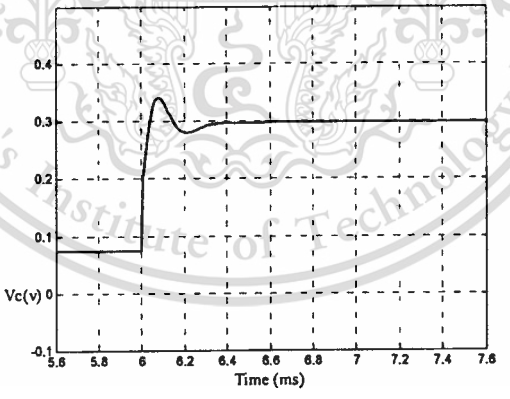
In this Section, another novel technique to improve output dynamic performance of DC-DC converters based on ACMC scheme is proposed. The technique uses the inductor current information readily available in ACMC (i.e V_{iL}), as a feedforward signal to strengthen the corrective action during

the occurrence of disturbances. Due to this feedforward nature, the technique is referred to as Current Feedforward Average Current Mode Control (CFACMC).

A circuit implementation of CFACMC is shown in Fig. 4.6. A circuit block $P_{cl}(s)$ consisting of a voltage buffer and an adjustable gain low-pass filter (R_{p1}, R_{p2}, C_p), is included into the conventional ACMC. Besides its usual role as a feedback variable to the current controller, the sensed inductor current V_{iL} is fed forward, through $P_{cl}(s)$, to add with the output signal from the voltage controller V_{CV} to produce the control signal V_C. A part from this, the rest of the control circuit is the same as the conventional ACMC.



(a) Control signal ACMC



(b) Control signal

Fig 4.7 Simulated result of CFACMC

The proposed CFACMC can improve output dynamic performance of the converter as follows. Assume that the output voltage drop is occurred due to a step load change, the voltage controller will respond by increasing V_{CV}. The increase in V_{CV} will trigger the increase in V_C, V_{CI}, d, I_L, V_{IL}, and V_{PCL}, respectively. With the contribution from V_{PCL}, V_C, which is equal to $V_{CV} + V_{PCL}$, will increase more than that in the conventional ACMC, which relies on V_{CV} alone to act. In other words, CFACMC yields the

stronger corrective action than the conventional ACMC and this can lead to the improved dynamic response of the converter. Fig. 4.7 shows a comparison between the control signals in the conventional ACMC and the CFACMC. In both cases, after a step load change V_c is increased to correct the output voltage drop, but the initial magnitude of V_c in CFACMC is higher, causing the output voltage to resettle quickly to the desired value.

However, as with the case of the parallel controller, too stronger corrective action can adversely affect the converter stability. Thus, the circuit block $P_{cl}(s)$ must be designed properly to avoid the potential of instability.

4.2.1 Small-signal analysis of CFACMC

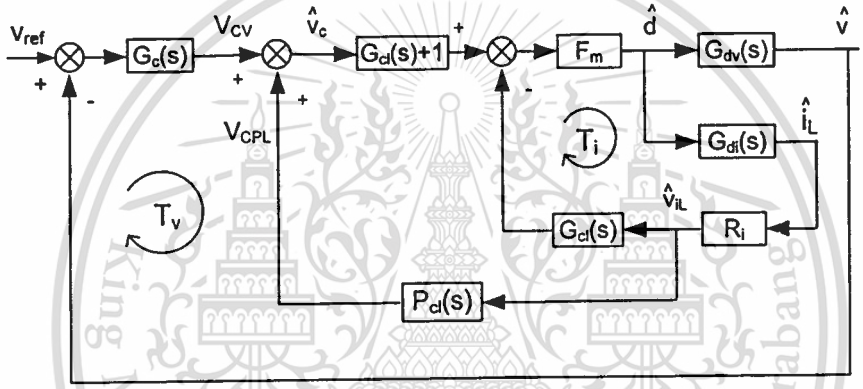


Fig 4.8 Small-signal model of CFACMC

From the control point of view, the increased corrective action caused by the summation of V_{CV} and V_{PCL} is equivalent to the increase in the voltage loop gain. As with any control systems, if the gain is increased too much, instability could result. With the current and voltage controllers in Fig. 4.8 having been prior designed and fixed from the conventional ACMC, the gain is controlled only by the low-pass filter $P_{cl}(s)$. The gain and cut-off frequency of this filter must be selected in such a way that desired output dynamic performance of the converter is achieved, while preserving system stability.

A small signal model of the buck converter with CFACMC is shown in Fig. 4.8. It is the same as the small-signal model of the buck converter with the conventional ACMC in Fig. 3.5, except the $P_{cl}(s)$ block has been included. The role that $P_{cl}(s)$ plays in forwarding V_{iL} to sum with the output from the voltage controller is evident in the model. The transfer function of $P_{cl}(s)$ is given by.

$$P_{cl}(s)=\frac{K_p}{1+\frac{s}{w_p}} \tag{4.9}$$

where

$$K_p=\frac{R_{p1}}{R_{p1}+R_{p2}}$$

$$w_p=\frac{R_{p1}+R_{p2}}{R_{p1}R_{p2}C_p}$$

To facilitate the analysis, the model in Fig. 4.8 is manipulated into the model in Fig. 4.9(a). It can be seen from Fig. 4.8 that if $P_{cl}(s)$ = 0 (thus $K_{cl}(s)$=0), the model will become the conventional ACMC model in Fig 3.5. In Fig. 4.9(a), $H_{cl}(s)$ is a transfer function from v_c to d expressed by (see Appendix D for detail)

$$H_{cl}(s)=\frac{F_m(G_{cl}(s)+1)}{1+F_mR_iG_{cl}(s)G_{di}(s)} \tag{4.10}$$

$$H_{cl}(s)=H_{ck}\frac{\left[s^2+s\left(w_{clp}+\frac{w_{cl}w_{clp}}{w_{clz}}\right)+w_{cl}w_{clp}\right]\left[s^2+s\left(\frac{1}{RC}+\frac{r_c}{L}\right)+\frac{1}{LC}\right]}{s^4+a_{H3}s^3+a_{H2}s^2+a_{H1}s+a_{H0}} \tag{4.11}$$

where

$$H_{ck}=F_m$$

$$\alpha=\frac{F_mR_iV_{in}w_{cl}}{w_{clz}}$$

$$\beta=\frac{LCR}{w_{clp}}$$

$$a_{H3}=w_{clp}+\frac{1}{RC}+\frac{r_c}{L}$$

$$a_{H2}=w_{clp}\left(\frac{1}{RC}+\frac{r_c}{L}\right)+\frac{1}{LC}+\frac{\alpha RC}{\beta}$$

$$a_{H1}=\frac{w_{clp}}{LC}+\frac{\alpha\left(1+w_{clz}RC\right)}{\beta}$$

$$a_{H0}=\frac{\alpha w_{clz}}{\beta}$$

$K_{cl}(s)$ is a transfer function from d to V_{CPL} expressed by

$$K_{cl}(s)=R_iP_{cl}(s)G_{di}(s) \tag{4.12}$$

$$K_{cl}(s) = K_{co}\frac{K_p}{\left[1+\frac{s}{w_p}\right]}\frac{1+sRC}{\left[s^2+s\left(\frac{1}{RC}+\frac{r_c}{L}\right)+\frac{1}{LC}\right]} \tag{4.13}$$

where

$$K_{co} = \frac{V_{in}R_i}{RCL}$$

Thus, the control-to-duty ratio transfer function $G_{rb}(s)$ in Fig. 4.9(b) is:

$$G_{rb}(s) = \frac{H_{cl}(s)}{1-K_{cl}(s)H_{cl}(s)} \tag{4.14}$$

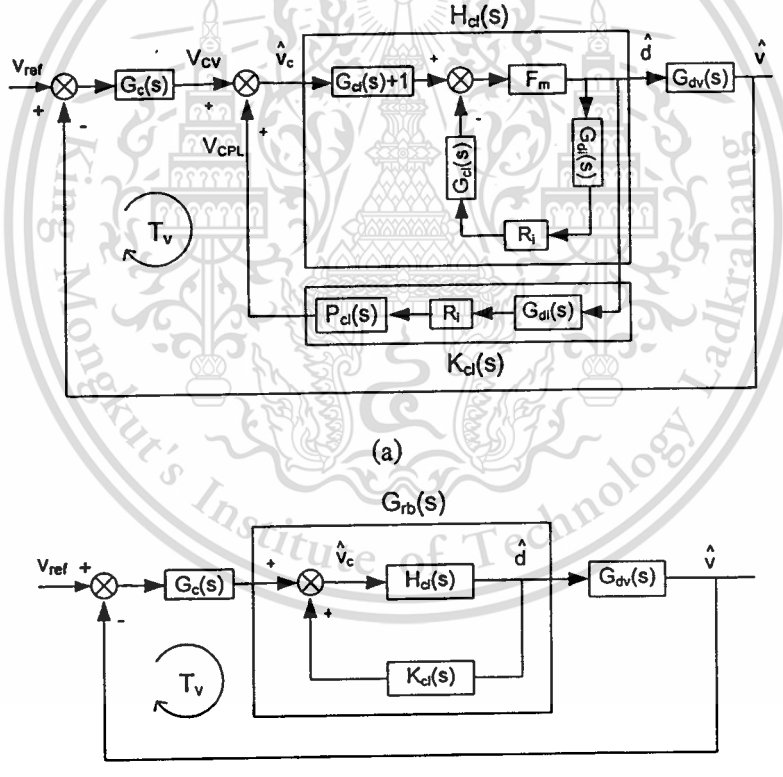


Fig 4.9 Small-signal model of manipulated CFACMC of Fig. 4.8

It can be observed from (4.14) that the inclusion of the circuit block $P_{cl}(s)$ in Fig. 4.9 has altered the original transfer function, which is $H_{cl}(s)$, by factor of $\frac{1}{1-K_{cl}(s)H_{cl}(s)}$. Note that from (4.12) the gain of $K_{cl}(s)$ is controlled by $P_{cl}(s)$. At low frequencies, the gain of $K_{cl}(s)$ should be high so that the product

of $K_{cl}(s)H_{cl}(s)$ approaches 1 to increase the loop gain $G_c(s)G_{rb}(s)G_{dv}(s)$ in Fig. 4.9(b) and thus fasten the dynamic response of the converter [9]. At high frequencies, the gain of $K_{cl}(s)$ should be low so that the product $K_{cl}(s)H_{cl}(s)$ approaches 0 then $G_{rb}(s)$ converged to $H_{cl}(s)$. In this way, the inclusion of $P_{cl}(s)$ will only serve to increase the loop gain at low frequencies and not affect system stability.

4.2.2 Gain selection for the low-pass filter

At low frequencies ($s \approx 0$), the transfer functions $G_{rb}(s)$ in (4.14), $K_{cl}(s)$ in (4.13), and $H_{cl}(s)$ in (4.11) are:

$$G_{rb}(0) = \frac{H_{cl}(0)}{1 - K_{cl}(0)H_{cl}(0)} \tag{4.15}$$

$$K_{cl}(0) = K_p \frac{V_{in}R_i}{R} \tag{4.16}$$

$$H_{cl}(0) = \frac{R}{V_{in}R_i} \tag{4.17}$$

Substituting (4.16) and (4.17) into (4.15),

$$G_{rb}(0) = \frac{H_{cl}(0)}{1 - K_p} \tag{4.18}$$

Assume that the input voltage V_{in} is constant, since from (4.17) $H_{cl}(0)$ is proportional to the load resistor R and from (4.18) $G_{rb}(0)$ is proportional to $H_{cl}(0)$, $G_{rb}(0)$ is hence proportional to R. When the load current is changed from minimum to maximum (i.e. the load resistor changed from R_{max} to R_{min}), $G_{rb}(0)$ will be reduced (Fig. 4.10). To prevent the effect of load change on $G_{rb}(0)$, from (4.18) K_p has to be increased. Suppose that $R_{max} = R$ and $R_{min} = R_{max}/n$, where n is a ratio of maximum load resistor to minimum load resistor (n>1), $H_{cl}(0)$ at R_{max} and R_{min} therefore are

$$H_{cl}(0)\big|_{R_{max}} = H_{cl}(0)\big|_{R} \tag{4.19}$$

$$H_{cl}(0)\big|_{R_{min}} = \frac{H_{cl}(0)\big|_{R}}{n} \tag{4.20}$$

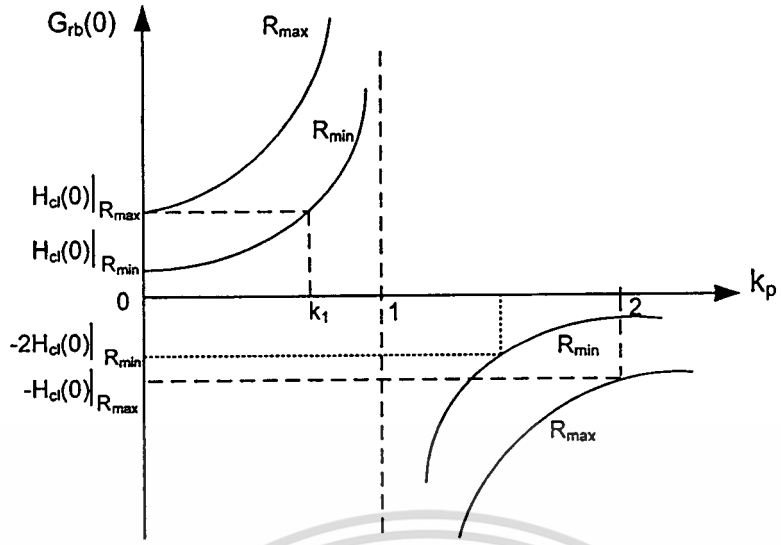


Fig 4.10 Graph of $G_{rb}(0)$ as k_p varies

Fig. 4.10 shows the plot of $G_{rb}(0)$ in (4.18) as a function of K_p at the two resistor values R_{max} and R_{min}. It can be seen that the gain of $G_{rb}(0)$ at maximum load current (R_{min}) is lower than the gain of $G_{rb}(0)$ at minimum load current (R_{max}). To prevent the effect of load change on $G_{rb}(0)$, K_p has to be increased, in this case, by the amount of k_1, which can be found by solving

$$G_{rb}(0)\big|_{R_{\min}} = \frac{H_{cl}(0)\big|_{R_{\min}}}{1-k_1} = H_{cl}(0)\big|_{R_{\max}} \tag{4.21}$$

From (4.18) and (4.20), k_p can be determined:

$$k_p = k_1 = \frac{n-1}{n} \tag{4.22}$$

As mentioned earlier, the gain of $K_{cl}(s)$ at high frequencies should be low for the product to $K_{cl}(s)H_{cl}(s)$ in (4.14) to be low, so that $G_{rb}(s)$ is converged to $H_{cl}(s)$ to avoid instability. This can be realized by the appropriate selection of the cut-off frequency of $P_{cl}(s)$. Here, **the cut off frequency is selected to be equal to the crossover frequency of the loop gain of the conventional ACMC, $G_c(s)H_{cl}(s)G_{dv}(s)$.**

Chapter 5

Design of the Prototype Converter

In this Chapter, control design of prototype buck converters is performed. Three control techniques are considered: (1) the conventional ACMC, (2) ACMC-P, and (3) CFACMC. The design is based on the analysis and equations presented in Chapters 3 and 4.

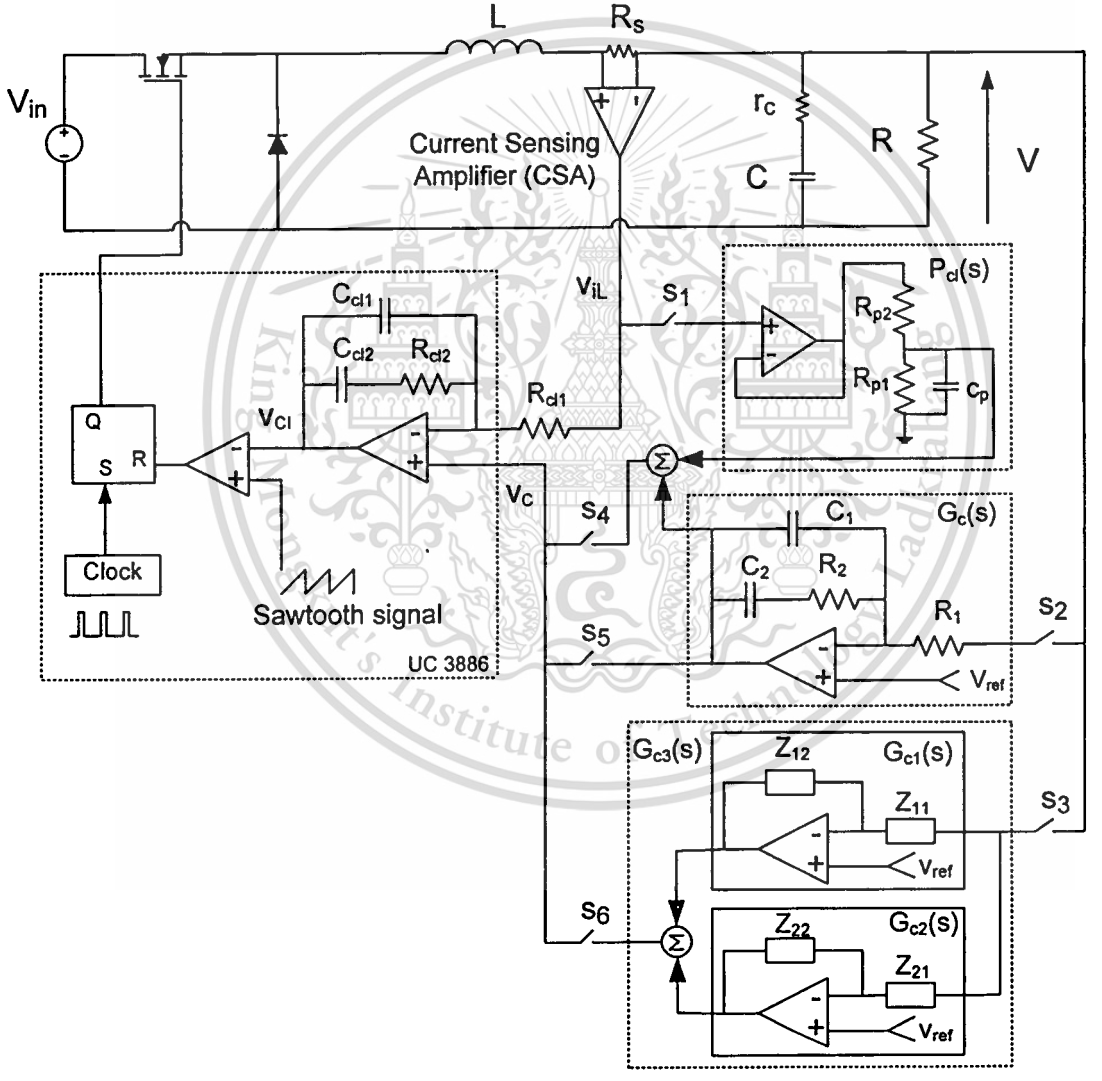


Fig 5.1 Circuit schematic of prototype buck converter

Fig. 5.1 shows a schematic diagram of the prototype buck converter. The required control technique can be chosen by selecting the appropriate switches. Table 5.1 gives the switch selection for the desired control scheme.

Table 5.1 Control mode selection

	s_1	s_2	s_3	s_4	s_5	s_6
ACMC		✓			✓	
ACMC-P			✓			✓
CFACMC	✓	✓		✓		

5.1 Transfer function of Power Stage

Circuit parameters of the prototype buck converter are listed in Table 5.2.

Table 5.2 Circuit parameters of the prototype buck converter

V_{in}	V	L	C	r_C	R	f_s
5V	2V	45.17μH	1230μF	0.015Ω	0.4-2Ω	100kHz

Substitution of the relevant parameters into (3.30) and (3.32), the duty ratio-to-output voltage transfer function $G_{dv}(s)$ and the duty ratio-to-inductor current transfer function $G_{di}(s)$ of the buck converter can be found:

$$G_{dv}(s) = 8.99\times10^{7}\,\frac{1.84\times10^{-5}s+1}{s^{2}+738.6s+1.8\times10^{7}} \tag{5.1}$$

$$G_{di}(s) = 4.5\times10^{7}\,\frac{2.5\times10^{-3}s+1}{s^{2}+738.6s+1.8\times10^{7}} \tag{5.2}$$

5.2 Conventional ACMC

The UC3886 [10] is the average current mode control IC used in the prototype circuit it has the peak-to-peak sawtooth voltage V_p of 1.8V. The sensing resistor R_s is 0.01Ω. The voltage across this

resistor is amplified by the current sensing amplifier with the gain (A_{CL}) of 7.5. From (3.42) and (3.34), F_m and R_i can be determined:

$$F_m = 1/V_p = 0.55 \tag{5.3}$$

$$R_i = R_s A_{CL} = 0.075 \tag{5.4}$$

5.2.1 Design of current controller $G_{cl}(s)$

The block diagram of the current loop in Fig. 3.6 is redrawn here in Fig. 5.2.

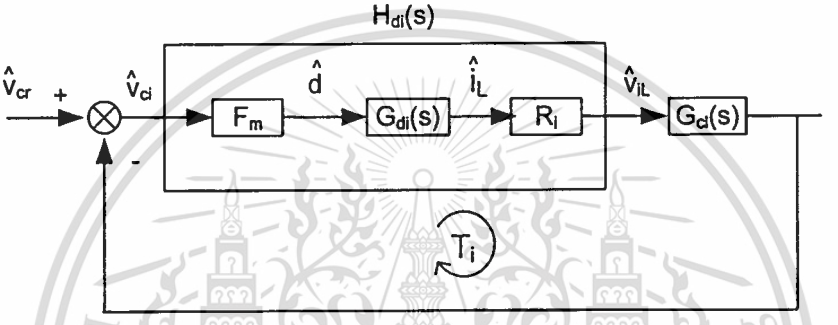


Fig 5.2 Block diagram of the current loop

From (5.2) to (5.4), $H_{di}(s)$ can be calculated:

$$H_{di}(s) = F_m R_I G_{di}(s) = 1.85\times10^6 \frac{2.5\times10^{-3}s + 1}{s^2 + 738.6s + 1.8\times10^7} \tag{5.5}$$

$H_{di}(s)$ has the double poles at w_o = 4.22×10^{3}rad/s and a zero at 400rad/sec. The current controller to compensate $H_{di}(s)$ is shown in Fig.5.3. Its transfer function was given in (3.43) and is repeated here

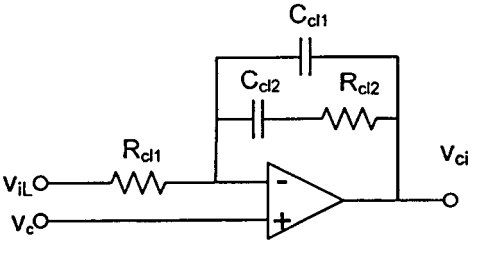


Fig 5.3 Current controller

$$G_{cl}(s)=\frac{z_{cl2}}{z_{cl1}}=\frac{w_{cl}}{s}\frac{1+\frac{s}{w_{clz}}}{1+\frac{s}{w_{clp}}} \tag{5.6}$$

where

$$w_{cl}=\frac{1}{R_{cl1}(C_{cl1}+C_{cl2})}$$

$$w_{clz}=\frac{1}{R_{cl2}.C_{cl2}}$$

$$w_{clp}=\frac{C_{cl1}+C_{cl2}}{R_{cl2}.C_{cl1}.C_{cl2}}$$

The design of the current controller was conceptually shown in Fig. 3.7. In this design, the crossover frequency is selected at 10kHz or w_c =62.8krad/sec. At this frequency, $H_{di}(s)$ has a gain of -23.9dB; therefore the required gain of $G_{cl}(s)$ is 23.9dB. The first pole of $G_{cl}(s)$ is placed at the origin, the zero at w_{clz}= w_o, and the second pole at placed at one-third of the switching frequency or w_{clp}=188.4krad/sec. Knowing the required gain of $G_{cl}(s)$ at w_c and location of its poles and zeros, the controller's component values are calculated, yielding C_{cl1}=500pF, C_{cl2}=22nF, R_{cl1}=560Ω and R_{cl2}=10kΩ. Substitution of these component values into (5.6) results in

$$G_{cl}(s)=\frac{7.93\times10^{4}}{s}\frac{1+2.2\times10^{-4}s}{1+4.89\times10^{-6}s} \tag{5.7}$$

The stability criterion of the current loop was stated in (3.46) and is repeated here

$$\left|G_{cl}(jw_s)\right| \le \min\left(2\frac{V_P.f_s.L}{(V_{in}-V)R_i},\frac{V_P.f_s.L}{V.R_i}\right) \tag{5.8}$$

Substituting relevant parameters into (5.8), we get

$$\left|G_{cl}(jw_s)\right| \le \min(72.2,\ 54.2) \tag{5.9}$$

Thus, the gain of $G_{cl}(s)$ at the switching frequency must not exceed 54.2. Referring to (5.7), the designed current controller has the gain at the switching frequency equal to

$$\left|G_{cl}(jw_s)\right|_{w_s=628\ krad/s}=\left|\frac{7.93\times10^{4}}{jw_s}\frac{1+2.2\times10^{-4}jw_s}{1+4.89\times10^{-6}jw_s}\right|_{w_s=628\ krad/s}=5.37 \tag{5.10}$$

which is well below the limit. Hence, the current loop is stable with the designed current controller.

Multiplication of (5.5) and (5.7) gives the open loop transfer function of the current loop gain:

$$T_i(s) = G_{cl}(s)H_{di}(s) \tag{5.11}$$

Bode plot of (5.11) is displayed in Fig. 5.4. It can be seen that $T_i(s)$ has high gain at low frequencies and crosses the 0dB line at about 10kHz as designed. The phase margin is 66.5°.

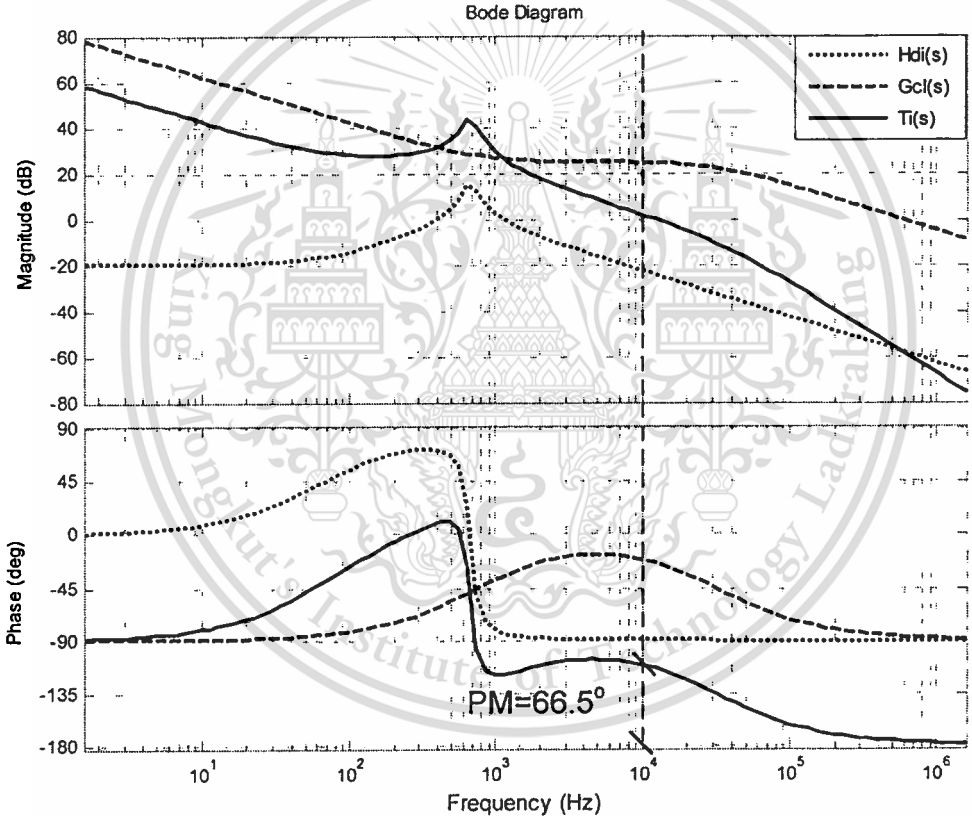


Fig 5.4 Frequency responses of $H_{di}(s)$, $G_{cl}(s)$ and $T_i(s)$

5.2.2 Design of voltage controller $G_c(s)$

The block diagram of the voltage loop in Fig. 3.8 is redrawn here in Fig. 5.5. $H_{co}(s)$ was given in (3.48) and is repeated here in (5.12)

$$H_{co}(s) = [G_{cl}(s)+1].G_{dv}(s).T_i' \tag{5.12}$$

where

$$T_i' = \frac{F_m}{1 + F_m R_i G_{di}(s) G_{cl}(s)}$$

From (5.1) to (5.4) and (5.7), $H_{co}(s)$ can be calculated:

$$H_{co}(s) = 4.999\times10^{7} \frac{1.85\times10^{-5}s^3 + 0.12\times10^{3}s^2 + 6.79\times10^{6}s + 2.7\times10^{10}}{s^4 + 3.38\times10^{5}s^3 + 2.77\times10^{10}s^2 + 1.42\times10^{14}s + 5.07\times10^{16}} \quad (5.13)$$

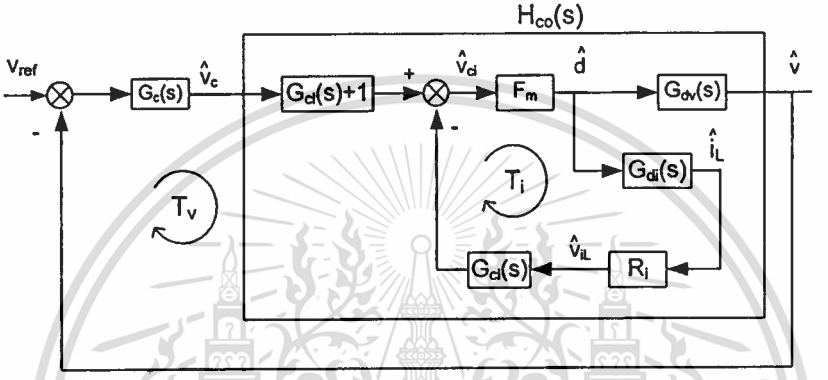


Fig 5.5 Bock diagram of the voltage loop design

$H_{co}(s)$ in (5.13) has four poles at w_{p1} = 390rad/sec, w_{p2} = 5.07×10^{3}rad/sec, w_{p3} = 1.23×10^{5}rad/sec, and w_{p4} = 2.09×10^{5}rad/sec, and three zeros at w_{z1}= 4.3×10^{3}rad/sec, w_{z2} = 5.42×10^{4}rad/sec, and w_{z3} = 6.28×10^{6}rad/sec. The voltage controller $G_c(s)$ to compensate $H_{co}(s)$ is shown in Fig. 5.6. Its transfer function was given in (3.40) and is repeated here

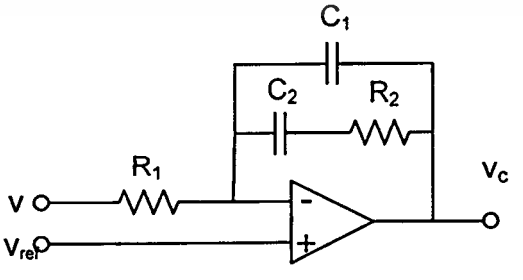


Fig 5.6 Voltage controller

$$G_c(s) = \frac{z_{c2}}{z_{c1}} = \frac{w_c}{s}\frac{1+\frac{s}{w_z}}{1+\frac{s}{w_p}} \tag{5.14}$$

where

$$w_c = \frac{1}{R_1(C_1+C_2)}$$

$$w_z = \frac{1}{R_2.C_2}$$

$$w_p = \frac{C_1+C_2}{R_2.C_1.C_2}$$

The design of the voltage controller is graphically shown in Fig. 5.7. The crossover frequency is selected at 5kHz or w_{ci}=31.4krad/sec. At this frequency, $H_{co}(s)$ has a gain of -8.12dB; therefore the required gain of $G_c(s)$ is 8.12dB. The first pole of $G_c(s)$ is placed at the origin, the zero near w_{z1} or $w_z \approx w_{z1}$, and the second pole at one-third of the switching frequency or w_p=188.4krad/sec. Knowing the required gain of $G_c(s)$ at w_c and location of its poles and zeros, the controller's component values are calculated, yielding C_1=500pF, C_2=22nF, R_1=3.9kΩ, and R_2=10kΩ. Substitution of these component values into (5.14) results in

$$G_c(s) = \frac{1.12\times10^4}{s}\frac{1+2.2\times10^{-4}s}{1+4.89\times10^{-6}s} \tag{5.15}$$

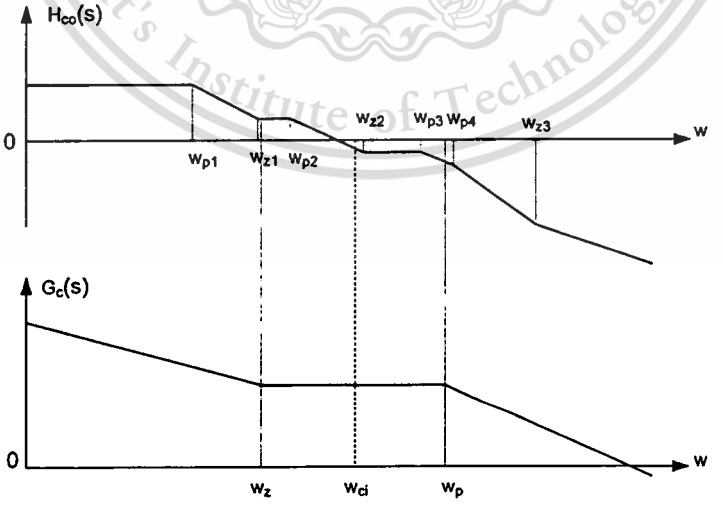


Fig 5.7 Asymptotic of $H_{co}(s)$ and $G_c(s)$

Multiplication of (5.13) and (5.15) gives the voltage loop gain:

$$T_v(s) = G_c(s)H_{co}(s) \tag{5.16}$$

Bode plot of (5.16) is displayed in Fig. 5.8. It can be seen that $T_v(s)$ has high gain at low frequencies and crosses the 0dB line at about 5kHz as designed. The phase margin is about 82°.

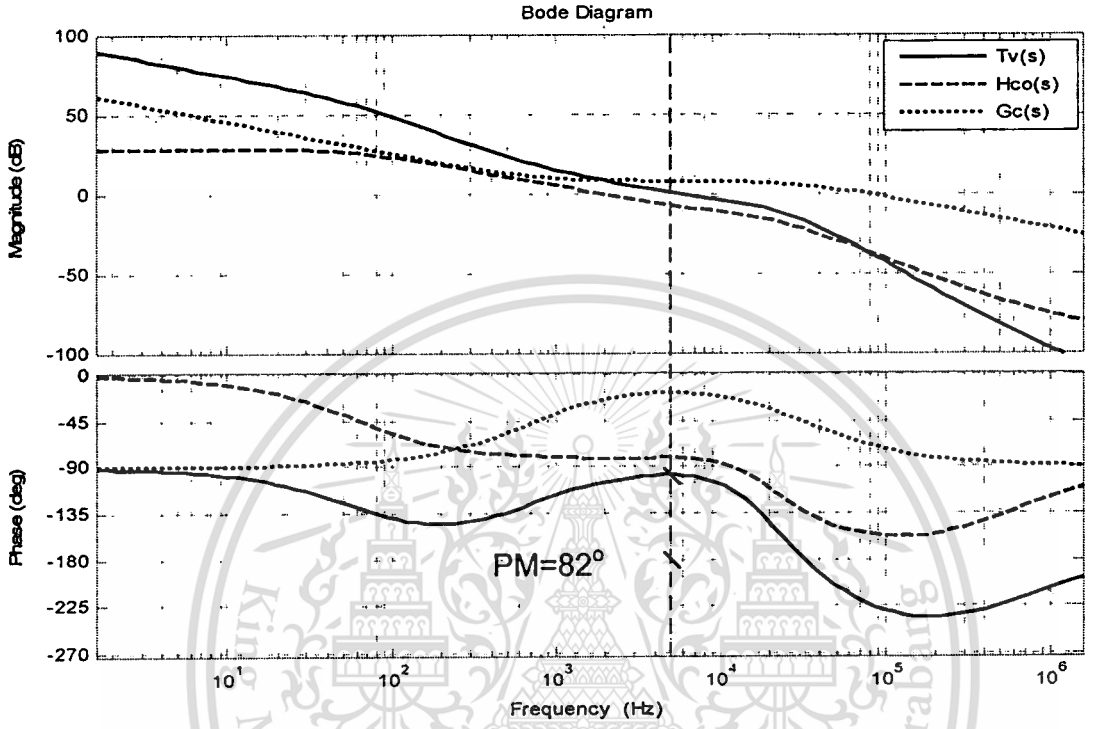


Fig 5.8 Frequency responses of $H_{co}(s)$, $G_c(s)$ and $T_v(s)$

5.3 ACMC with a parallel controller (ACMC-P)

In chapter 4, the parallel controller $G_{c3}(s)$ in (4.2) was proposed to compensate $H_{co}(s)$ in (5.13). Fig. 5.6 shows the block diagram of such scheme.

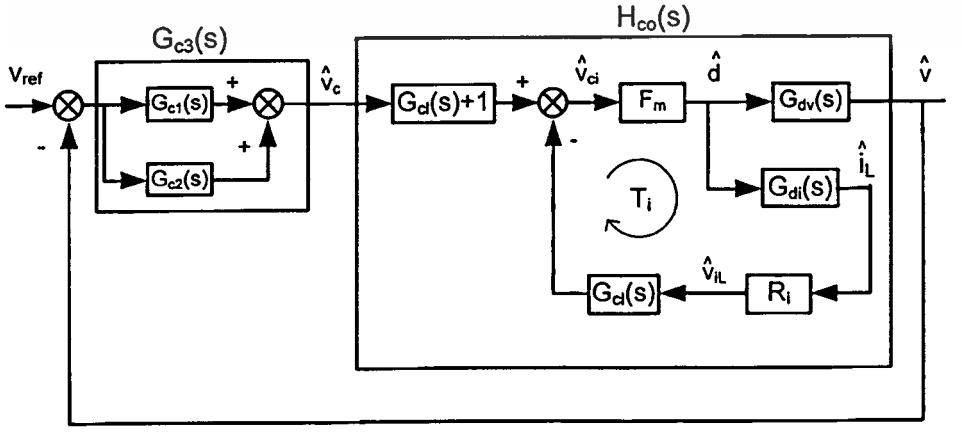


Fig 5.9 Block diagram of ACMC with a parallel control

Recall that

$$G_{c3}(s) = k\frac{(s+w_{cz1})(s+w_{cz2})(s+w_{cz3})(s+w_{cz4})}{s(s+w_{cp1})(s+w_{cp2})(s+w_{cp3})} \tag{5.17}$$

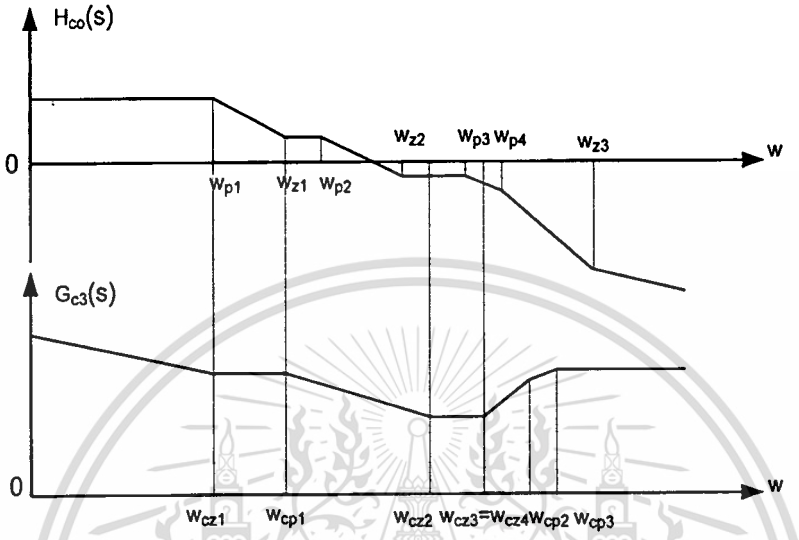


Fig 5.10 Asymptotic of $H_{co}(s)$ and $G_{c3}(s)$

Design of the parallel controller is shown graphically in Fig. 5.10. The crossover frequency is selected at 10kHz or w_c =62.8krad/sec. At this frequency, $H_{co}(s)$ has a gain of -11.5dB; therefore the required gain of $G_{c3}(s)$ is 11.5dB. The zeros of $G_{c3}(s)$ are placed at: w_{cz1}=390rad/sec, w_{cz2}=60krad/sec, w_{cz3}=180krad/sec and w_{cz4}=180krad/sec. The first pole of $G_{c3}(s)$ is placed at the origin and the remaining poles at: w_{cp1}=4.3krad/sec, w_{cp2}=250krad/sec and w_{cp3}=350krad/sec. The required gain of $G_{c3}(s)$ at w_c allows the gain K in (5.17) to be determined, which is equal to 6.8. Thus, the designed $G_{c3}(s)$ is expressed by

$$G_{c3}(s) = 6.8\frac{(s+390)(s+6\times10^4)(s+1.8\times10^5)(s+1.8\times10^5)}{s(s+4.3\times10^3)(s+2.5\times10^5)(s+3.5\times10^5)} \tag{5.18}$$

Rewriting the numerator of (5.18) into a polynomial form,

$$G_{c3}(s) = 6.8\frac{s^4+4.20\times10^5 s^3+5.41\times10^{10}s^2+1.96\times10^{15}s+7.58\times10^{17}}{s(s+4.3\times10^3)(s+2.5\times10^5)(s+3.5\times10^5)} \tag{5.19}$$

Recall $G_{c3}(s)$ in (4.7) which was synthesized from parallel connection of $G_{c1}(s)$ and $G_{c2}(s)$ which has a transfer function:

$$G_{c3}(s) = G_{c1}(s) + G_{c2}(s) = k_2 \frac{s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{s(s + w_{cp2})(s + w_{cp1})(s + w_{cp3})} \quad (5.20)$$

where

$$a_3 = \frac{k_2(w_\gamma + w_\beta + w_{cp2}) + k_1}{k_2}$$

$$a_2 = \frac{k_2((w_\gamma + w_\beta)w_{cp2} + w_\gamma w_\beta) + k_1(w_\alpha + w_{cp1} + w_{cp2})}{k_2}$$

$$a_1 = \frac{k_2 w_\gamma w_\beta w_{cp2} + k_1(w_{cp1} w_{cp3} + w_\alpha(w_{cp1} + w_{cp3}))}{k_2}$$

$$a_0 = \frac{k_1}{k_2} w_\alpha w_{cp1} w_{cp3}$$

Matching the gain and coefficients of the numerator of (5.20) to those of (5.19), the following equations are obtained:

$$\begin{cases} k_2 = 6.8 & (1) \\ \frac{k_1}{k_2} w_\alpha w_{cp1} w_{cp3} = 7.58 \times 10^{17} & (2) \\ \frac{k_2 w_\gamma w_\beta w_{cp2} + k_1[w_{cp1} w_{cp3} + w_\alpha(w_{cp1} + w_{cp3})]}{k_2} = 1.96 \times 10^{15} & (3) \\ \frac{k_2[(w_\gamma + w_\beta)w_{cp2} + w_\gamma w_\beta] + k_1(w_\alpha + w_{cp1} + w_{cp2})}{k_2} = 5.41 \times 10^{10} & (4) \\ \frac{k_2(w_\gamma + w_\beta + w_{cp2}) + k_1}{k_2} = 4.20 \times 10^5 & (5) \end{cases} \quad 5.21)$$

with

$w_{cp1} = 4.3 \times 10^3$ rad/sec

$w_{cp2} = 2.5 \times 10^5$ rad/sec

$w_{cp3} = 3.5 \times 10^5$ rad/sec

Solving the above equations (see Appendix C for detail) yields

$k_1 = 3.15 \times 10^5$

$w_\alpha = 1.08 \times 10^4$ rad/s

$k_2 = 6.8$

$w_\beta = (6.20 + 4.88j) \times 10^4$ rad/s

$w_\gamma = (6.20 - 4.88j) \times 10^4$ rad/s

Hence,

$$G_{c1}(s) = \frac{k_1}{s}\frac{s+w_a}{s+w_{cp2}} = \frac{3.15\times10^5}{s}\frac{s+1.08\times10^4}{s+2.5\times10^5} \tag{5.22}$$

$$G_{c2}(s)=k_2\frac{(s+w_\beta)(s+w_\gamma)}{(s+w_{cp1})(s+w_{cp3})}=6.8\frac{\left(s+(6.2-4.88j)\times10^4\right)\left(s+(6.2+4.88j)\times10^4\right)}{(s+4.3\times10^3)(s+3.5\times10^5)} \tag{5.24}$$

Knowing the transfer functions $G_{c1}(s)$ and $G_{c2}(s)$, their component values can be calculated: for $G_{c1}(s)$, R_{11}=8.2kΩ, R_{12}=10kΩ, C_{11}=470pF and C_{12}=4.3nF, and for $G_{c2}(s)$, R_1=180Ω, R_2=560Ω, R_3=24kΩ, R_4=1.5kΩ, C_1=22pF and C_2=10nF. Substitution of these component values into (4.4) and (4.5) results in

$$G_{c1}(s)=\frac{2.59\times10^5}{s}\frac{s+2.3\times10^4}{s+2.36\times10^5} \tag{5.26}$$

$$G_{c2}(s) = 7.8\frac{\left(s+6.66\times10^4\right)\left(s+8.11\times10^4\right)}{\left(s+3.92\times10^3\right)\left(s+3.33\times10^5\right)} \tag{5.27}$$

Addition of the above two equations gives:

$$G_{c3}(s) = 7.8\frac{s^4+4.17\times10^5 s^3+5.22\times10^{10}s^2+1.58\times10^{15}s+1.007\times10^{18}}{s\left(s+3.92\times10^3\right)\left(s+2.36\times10^5\right)\left(s+3.336\times10^5\right)} \tag{5.28}$$

Multiplication of (5.13) and (5.28) gives the open loop transfer function of voltage loop:

$$T_{v1}(s)=G_{c3}(s)H_{co}(s) \tag{5.29}$$

Bode plot of (5.29) is displayed in Fig. 5.11. It can be seen that $T_{v1}(s)$ has high gain at low frequencies and crosses the 0dB line at about 10kHz as designed. The phase margin is 73.9°. Comparison between the Bode plots of the conventional ACMC (Fig. 5.8) and ACMC-P (Fig. 5.11) is shown in Fig. 5.12. It can be seen that the loop gain of the latter is larger than the former throughout to the crossover frequency. Therefore, the better output dynamic response can be expected from the ACMC-P.

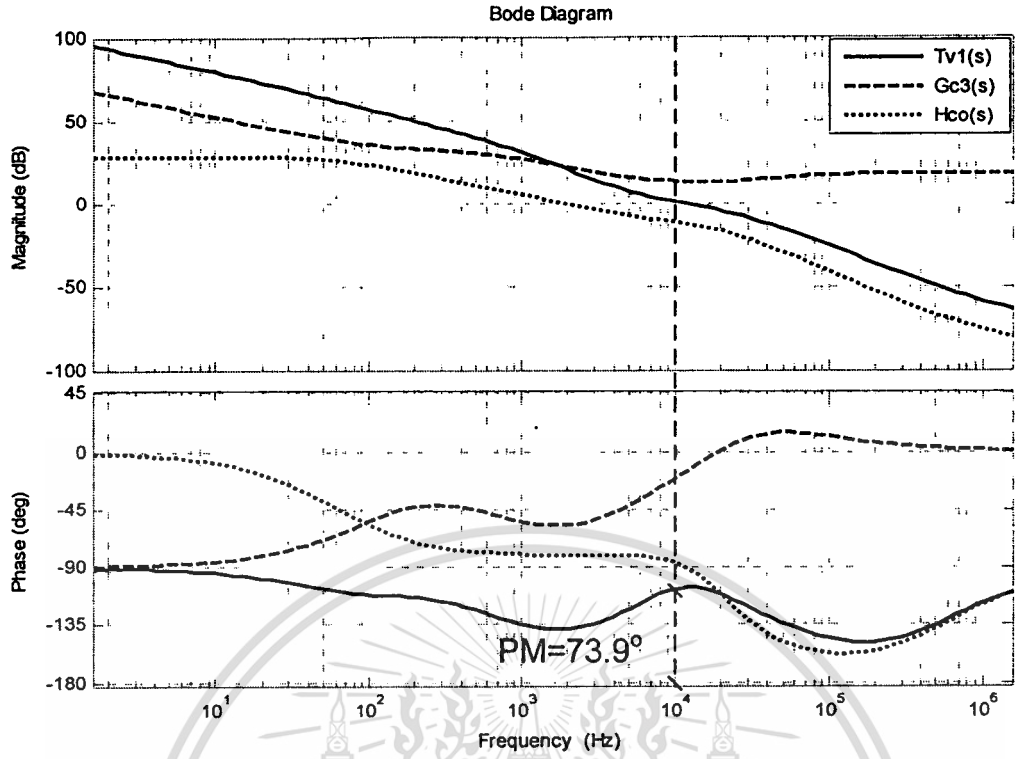


Fig 5.11 Frequency response of $H_{co}(s)$ and $G_{c3}(s)$

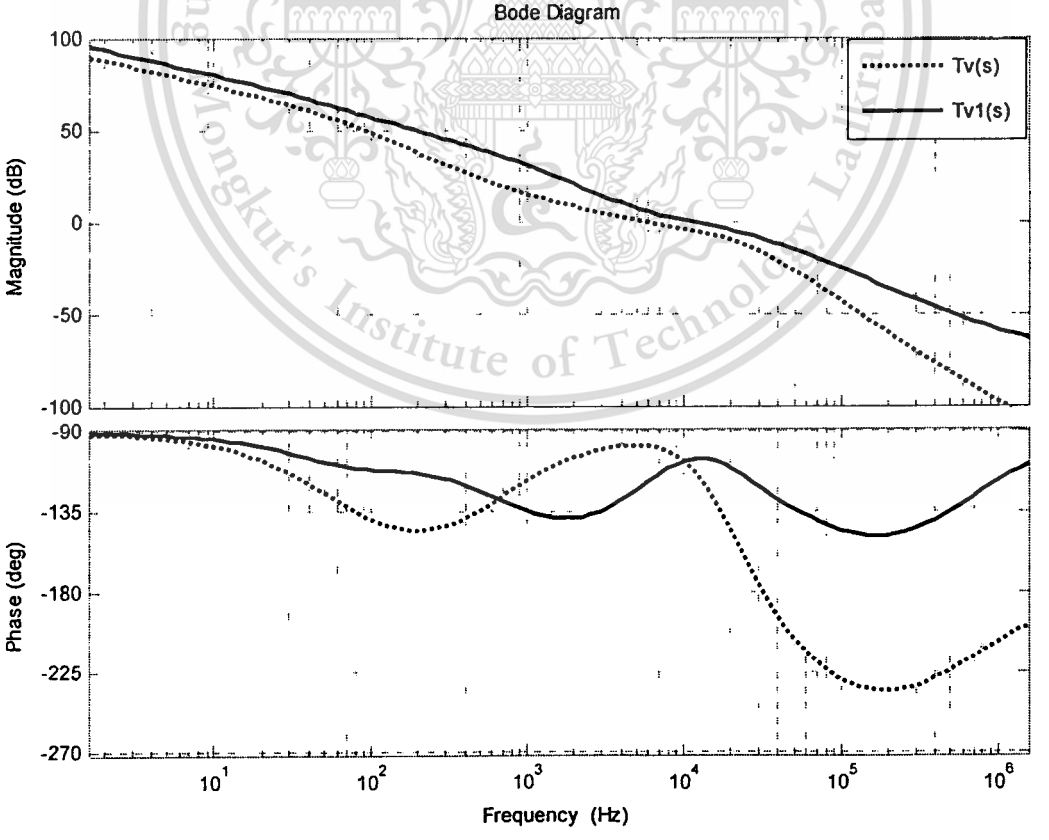


Fig 5.12 Comparison of $T_{v1}(s)$ and $T_v(s)$

5.4 Current Feedforward Average Current Mode Control (CFACMC)

In CFACMC, except a section on the adjustable gain low-pass filter $P_{cf}(s)$ the rest of the control circuit is the same as the conventional ACMC. Hence, the voltage and current controllers designed in Section 5.2 for the conventional ACMC can be readily adopted for CFACMC. The design of CFACMC is therefore reduced to selection of gain and cut-off frequency of $P_{cf}(s)$.

Gain and cut-off frequency selection for $P_{cf}(s)$

The low pass filter circuit $P_{cf}(s)$ shown in Fig. 5.13 has a transfer function described by (5.30).

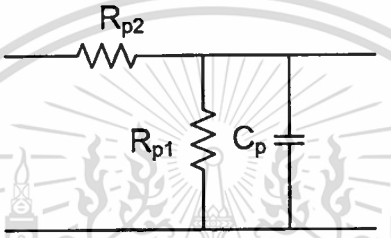


Fig 5.13 Low pass filter $P_{cf}(s)$

$$P_{cf}(s) = \frac{K_p}{1 + \frac{s}{w_p}} \tag{5.30}$$

where

$$K_p = \frac{R_{p1}}{R_{p1} + R_{p2}}$$

$$w_p = \frac{R_{p1} + R_{p2}}{R_{p1} R_{p2} C_p}$$

As shown in Table 5.2, the maximum and minimum load resistances are 2Ω and 0.4Ω, respectively. This represents the load ratio ($n = R_{max}/R_{min}$) of 5. The gain K_p can be found from (4.22):

$$K_p = \frac{n\text{-}1}{n} = 0.8 \tag{5.31}$$

As stated in Section 4.2.3, the cut-off frequency of $P_{cf}(s)$ is selected to be equal to the crossover frequency of the voltage loop gain of the conventional ACMC. In Section 5.2, this value was set at

5kHz or w_p=31.4krad/sec. Knowing K_p and w_p the filter's component values are calculated, yielding R_{p1}=4kΩ, R_{p2}=1kΩ, and C_p=38nF. Substitution of these component values into (5.30) results in

$$P_{cl}(s) = \frac{0.8}{1+3.04\times10^{-5}s} \tag{5.32}$$

The block diagram of CFACMC in Fig. 4.6 is redrawn here in Fig. 5.14

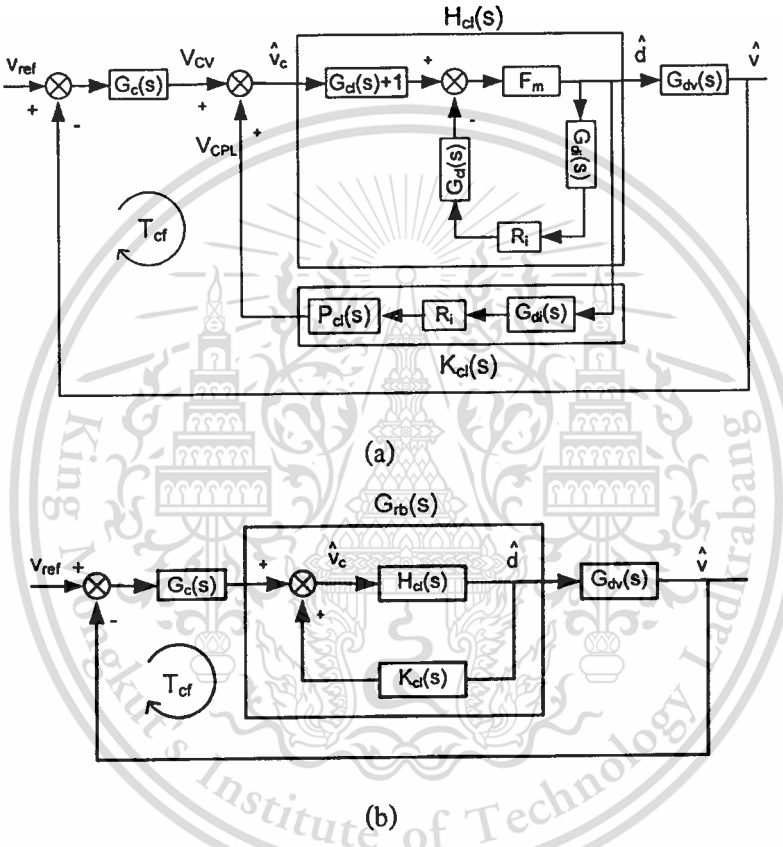


Fig 5.14 Small-signal model of the buck converter with CFACMC

From Fig. 5.14, the transfer functions $H_{cl}(s)$, $K_{cl}(s)$ and $G_{rb}(s)$ are given by

$$H_{cl}(s) = \frac{F_m(G_{cl}(s)+1)}{1+F_m R_i G_{cl}(s) G_{di}(s)} \tag{5.33}$$

$$K_{cl}(s) = R_i P_{cl}(s) G_{di}(s) \tag{5.34}$$

$$G_{rb}(s) = \frac{H_{cl}(s)}{1-K_{cl}(s)H_{cl}(s)} \tag{5.35}$$

Substitution of the relevant parameters into (5.33), (5.34) and (5.35) yields

$$H_{cl}(s) = 0.55\frac{s^4 + 6.29\times10^6 s^3 + 3.17\times10^{10} s^2 + 1.33\times10^{14} s + 4.86\times10^{17}}{s^4 + 3.38\times10^3 s^3 + 2.77\times10^{10} s^2 + 1.42\times10^{14} s + 5.07\times10^{16}} \quad (5.36)$$

$$K_{cl}(s) = 1.9\times10^8 \frac{s + 406.47}{s^3 + 3.35\times10^4 s^2 + 4.22\times10^7 s + 5.9\times10^{11}} \quad (5.37)$$

$$G_{rb}(s) = 0.55\frac{\left[\begin{matrix}\left(s^4 + 6.29\times10^6 s^3 + 3.17\times10^{10} s^2 + 1.33\times10^{14} s + 4.86\times10^{17}\right)\\ \times\left(s^3 + 3.35\times10^4 s^2 + 4.22\times10^7 s + 5.9\times10^{11}\right)\end{matrix}\right]}{\left(\begin{matrix}3.05\times10^{-5} s^7 + 1145 s^6 + 1.22\times10^6 s^5 + 1.67\times10^{10} s^4\\ + 1.197\times10^{14} s^3 + 1.777\times10^{17} s^2 + 1.36\times10^{21} s + 1.369\times10^{24}\end{matrix}\right)} \quad (5.38)$$

Multiplication of (5.1), (5.15) and (5.38) gives the open loop transfer function of CFACMC:

$$T_{cf}(s) = G_c(s)G_{rb}(s)G_{dv}(s) \quad (5.39)$$

Bode plot of (5.39) is shown in Fig. 5.15. It can be seen that $T_{cf}(s)$ has high gain at low frequencies and crosses the 0dB line at about 5kHz as designed. The phase margin is 53°.

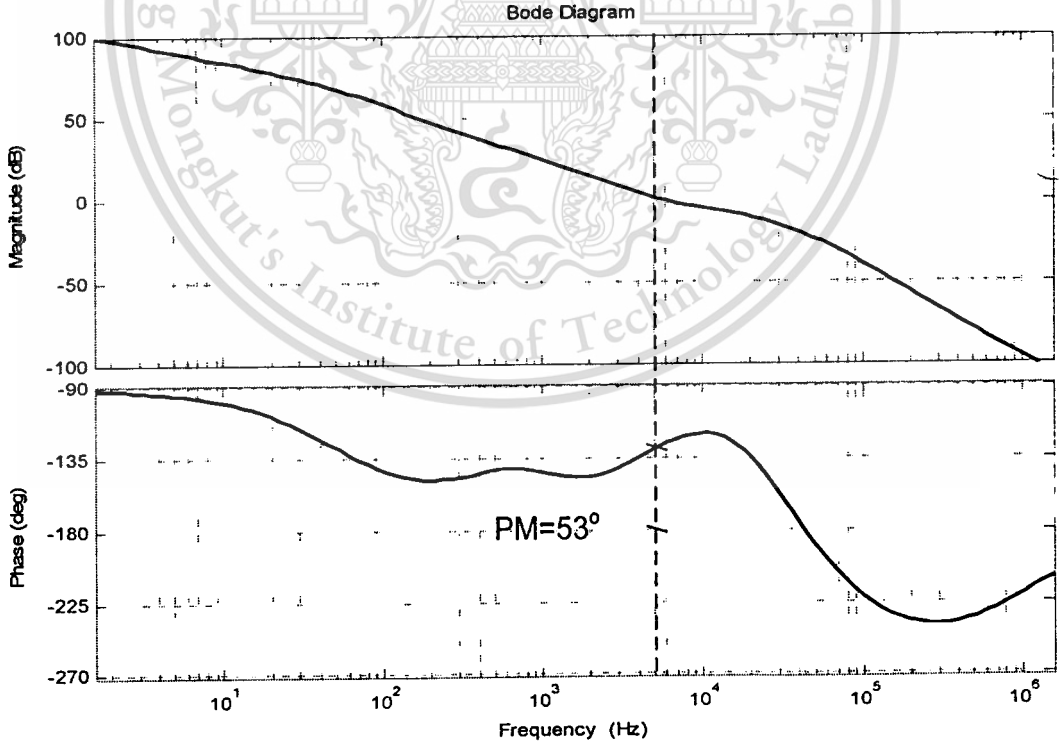


Fig 5.15 Frequency response of $T_{cf}(s)$

Comparison between Bode plot of conventional ACMC (Fig. 5.8) and CFACMC (Fig 5.15) is shown in Fig. 5.16, it can be seen (Fig. 5.16) that the loop gain of CFACMC is greater than the loop gain of the conventional ACMC up to the crossover frequency. Above the crossover frequency, the two plots are converged. This result indicates that the designed $P_{cf}(s)$ only serves to improve output dynamic response of the converter, while keeping its impact on system stability at the minimum.

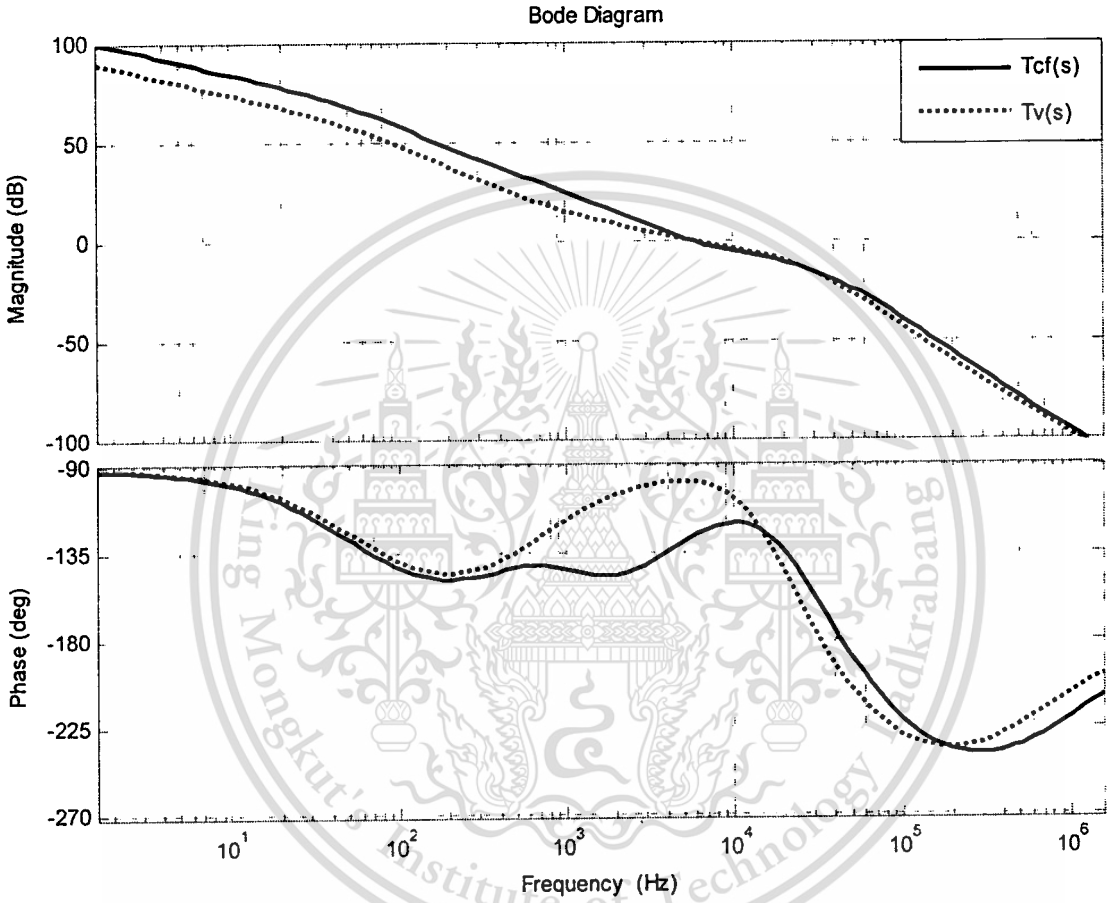


Fig 5.16 Frequency response of $T_{cf}(s)$ and $T_v(s)$

Chapter 6

Results

The first part of this Chapter describes averaged models of a buck converter with the three control schemes under study. The models are developed for simulation in SIMULINK [11]. The averaged model is chosen because it gives a faster computer run-time than the switched model [1], and is usually used to evaluate overall dynamic performance of the converter. The second part of this Chapter presents simulated and experimental results. It is shown that the two results are in good agreement for every control scheme, thus validating the accuracy of the developed models. Furthermore, the presented results show that considerable improvement in output dynamic performance is achieved with the proposed CFACMC and ACMC-P.

6.1 Averaged Models

This Section presents averaged models of the buck converter with: (1) ACMC, (2) ACMC-P and (3) CFACMC. The model descriptions for each control scheme are given below.

6.1.1 Averaged model of the buck converter with ACMC

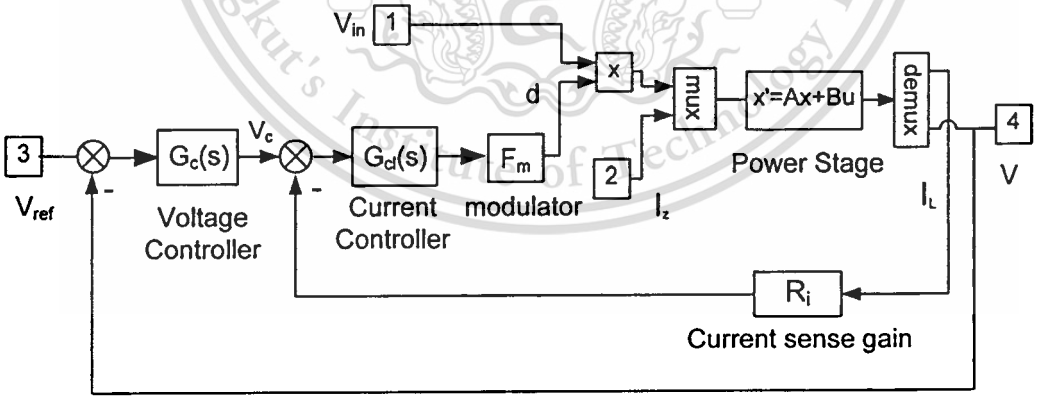


Fig 6.1 Simulink model of buck converter with ACMC

Table 6.1 Parameters of the prototype buck converter

V_{in}	V	L	C	r_C	R	f_s
5V	2V	45.17μH	1230μF	0.015Ω	2Ω	100kHz

The SIMULINK model of the buck converter with ACMC is shown in Fig. 6.1. The state-space averaged equations of the power stage (3.26) is

$$\begin{cases} \begin{bmatrix} \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} \dfrac{-R.r_c}{L(R+r_c)} & \dfrac{-R}{L(R+r_c)} \\ \dfrac{R}{C(R+r_c)} & \dfrac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \dfrac{d}{L} & \dfrac{-R.r_c}{L(R+r_c)} \\ 0 & \dfrac{R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \\ V = [\dfrac{R.r_c}{R+r_c} \quad \dfrac{R}{R+r_c}] \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & \dfrac{R.r_c}{R+r_c} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \end{cases} \tag{6.1}$$

With the power stage's parameters in Table 6.1, (6.1) becomes

$$\begin{cases} \begin{bmatrix} \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} -330 & -2.2\times10^4 \\ 807 & -403 \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 2.2\times10^4 d & -330 \\ 0 & 807 \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \\ V = [0.0149 \quad 0.9926] \begin{bmatrix} i_L \\ v_c \end{bmatrix} + [0 \quad 0.0149] \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \end{cases} \tag{6.2}$$

Equation (6.2) is modeled by the block named "power stage" in Fig 6.1, using the standard state-space format in SIMULINK. The blocks F_m, R_i, $G_{cl}(s)$ and $G_c(s)$ are modeled using the standard transfer function format. Their values, which were determined in Chapter 5, are summarized below

$$F_m = 0.55 \tag{6.3}$$

$$R_i = 0.075 \tag{6.4}$$

$$G_{cl}(s) = \frac{7.93\times10^4}{s} \frac{1+2.2\times10^{-4}s}{1+4.89\times10^{-6}s} \tag{6.5}$$

$$G_c(s) = \frac{1.12\times10^4}{s} \frac{1+2.2\times10^{-4}s}{1+4.89\times10^{-6}s} \tag{6.6}$$

In the figure, the demultiplexer (demux) block is used to separate the inductor current from the output voltage in the output vector, so that both variables can be fed back independently. The multiplexer (mux) block combines dV_{in} and I_z to be the input vector of the system. Note that d, V_{in} and I_z are the inputs variables, and V and i_L the output variables of the power stage. Since the converter's output dynamic performance under a sudden load change is of interest here, in the simulation V_{in} will be kept constant and I_z changed in a step manner.

6.1.2 Averaged model of the buck converter with ACMC-P

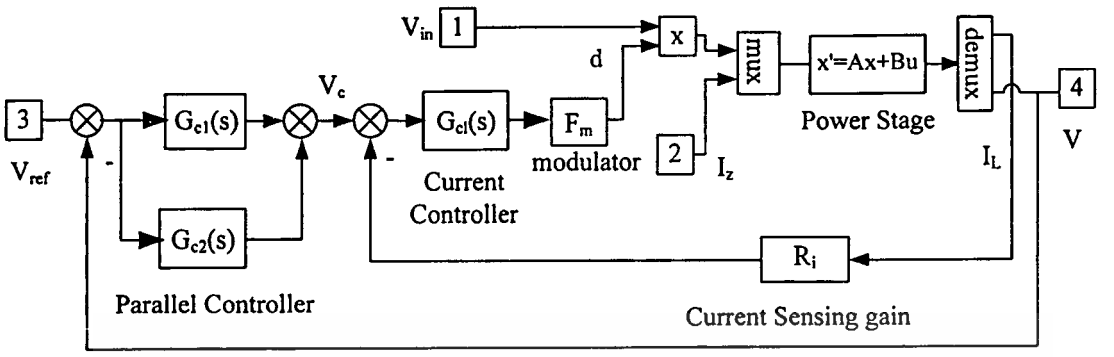


Fig 6.2 Simulink model of buck converter with ACMC-P

The SIMULINK model of the buck converter with ACMC-P is shown in Fig. 6.2. It is similar to the model in Fig. 6.1 except that the parallel controller is used instead of the two-pole one-zero voltage controller. The values of $G_{c1}(s)$ and $G_{c2}(s)$, which were determined in Chapter 5, are given below

$$G_{c1}(s) = \frac{2.59\times10^5}{s}\frac{s+2.3\times10^4}{s+2.36\times10^5} \tag{6.7}$$

$$G_{c2}(s) = 7.8\frac{\left(s+6.66\times10^4\right)\left(s+8.11\times10^4\right)}{\left(s+3.92\times10^3\right)\left(s+3.33\times10^5\right)} \tag{6.8}$$

The values of F_m, R_i and $G_{cl}(s)$ are given in (6.3) to (6.5), respectively.

6.1.3 Averaged model of the buck converter with CFACMC

The SIMULINK model of the buck converter with CFACMC is shown in Fig. 6.3. It is essentially the same as Fig. 6.1, but has included the low-pass filter block $P_{cl}(s)$. The value of $P_{cl}(s)$, which was determined in Chapter 5, is:

$$P_{cl}(s) = \frac{0.8}{1+3.04\times10^{-5}s} \tag{6.9}$$

The values of F_m, R_i, $G_{cl}(s)$ and $G_c(s)$ are given in (6.3) to (6.6), respectively.

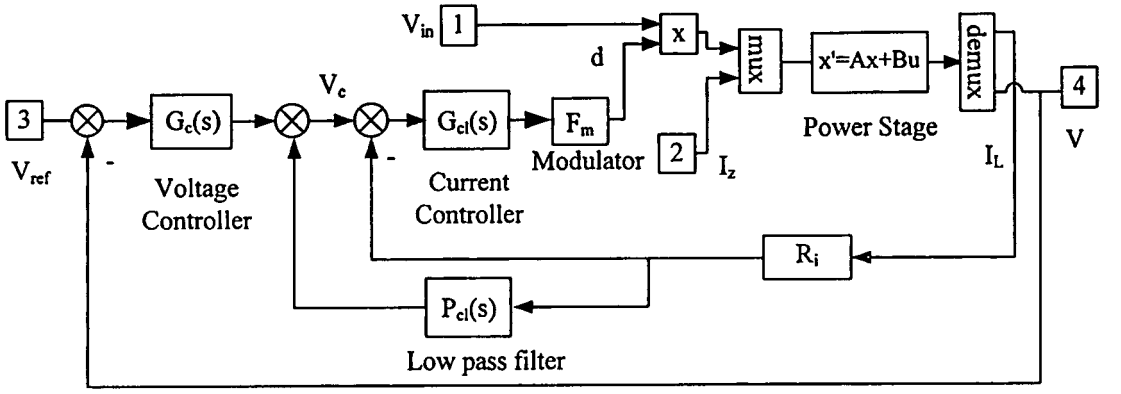


Fig 6.3 Simulink model of buck converter with CFACMC

6.2 Experimental set up

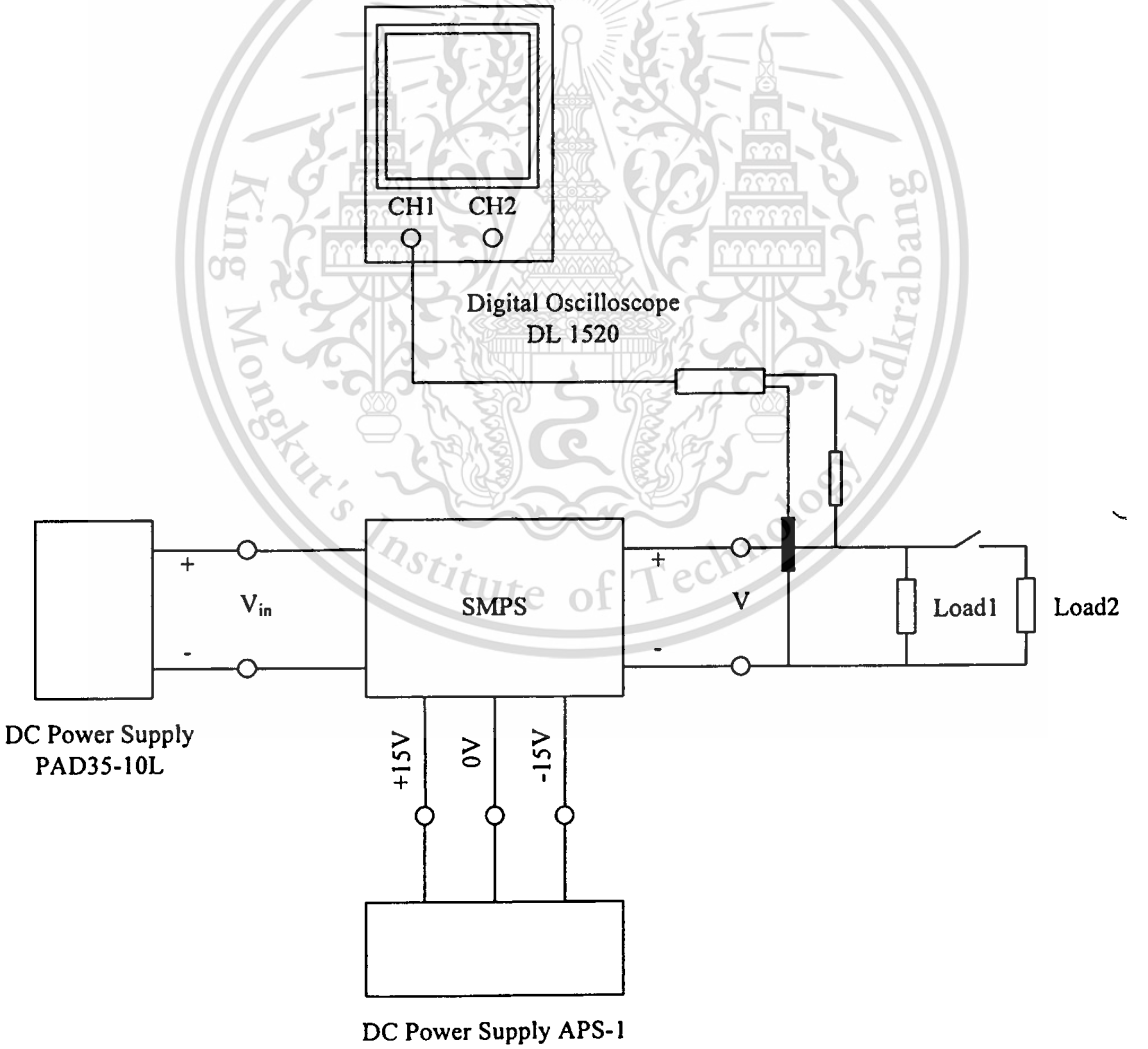


Fig 6.4 Experimental set up for a step load change

Electrical schematic of the prototype circuit was shown in Chapter 5. Three control modes, i.e. ACMC, ACMC-P, and CFACMC can be selected by connecting the relevant switches as indicated in Table 5.1. The setup for a step load change is shown in Fig 6.4, where the equipments used are:

1. Digital oscilloscope (Yokogawa) DL1520
2. DC power supply for the power circuit (Kikusui) PAD35-10L
3. DC power supply for the control circuit (Analab), APS-1
4. Digital Multi-meter (Tektronix) DMM256

The test procedure is as follows:

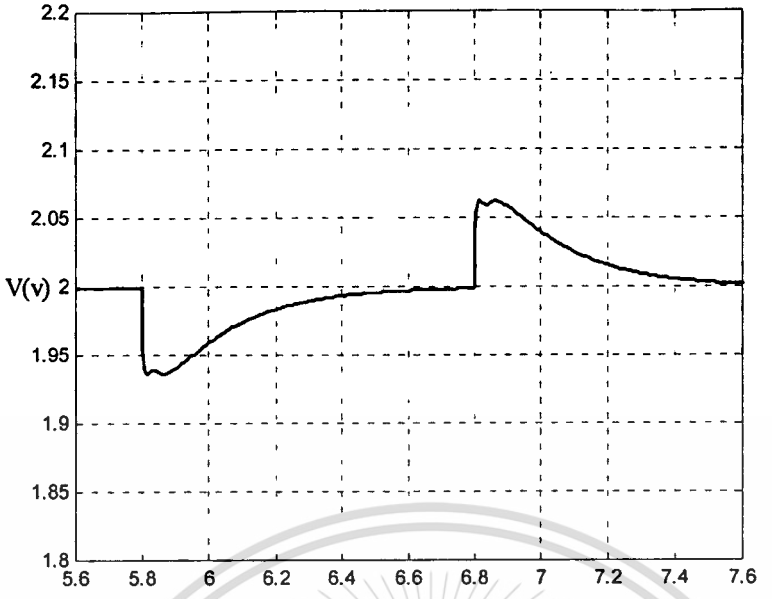
1) Supply a 5V voltage to power circuit and ±15V voltage to the control circuit.
2) After step 1, the output voltage is regulated at 2V. Load 1 is a 2Ω resistor; hence the output current is 1A.
3) Load 2, which is a 0.66Ω resistor and draws current of 3A, is switched in parallel with load 1 and stays connected for 1ms.

The output voltage of the converter during the load application/rejection is captured by the digital oscilloscope

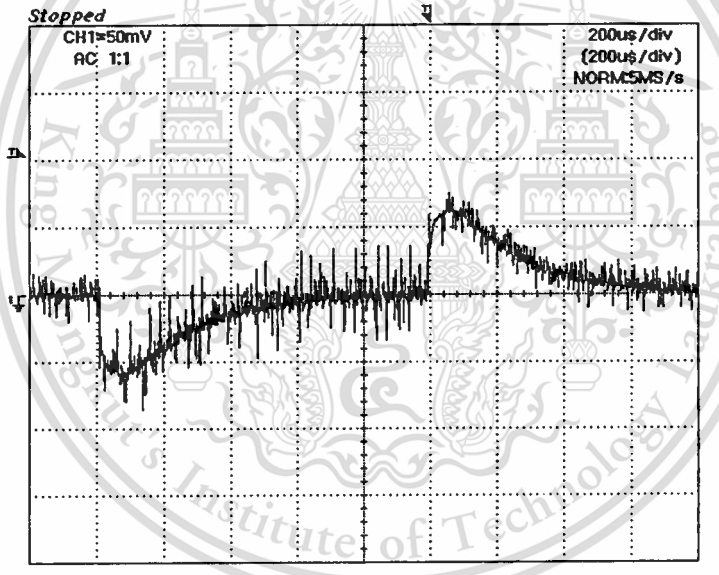
6.3 Simulated and experimental results

6.3.1 ACMC

The simulated and measured output voltage responses of the prototype converter with ACMC, when the load current is switched back and forth between 1A and 4A, are shown in Fig. 6.5. The output voltage has dropped and recovered back to 2V during the load application, and raised and recovered back to 2V during the load rejection. The maximum voltage drop/raise is about 65mV and the setting time is about 750μs. As shown in the figures, the experimental result is closely agreed with the simulated result. The similarity between the two results confirms the accuracy and validity of the developed SIMULINK model.



(a) Simulated

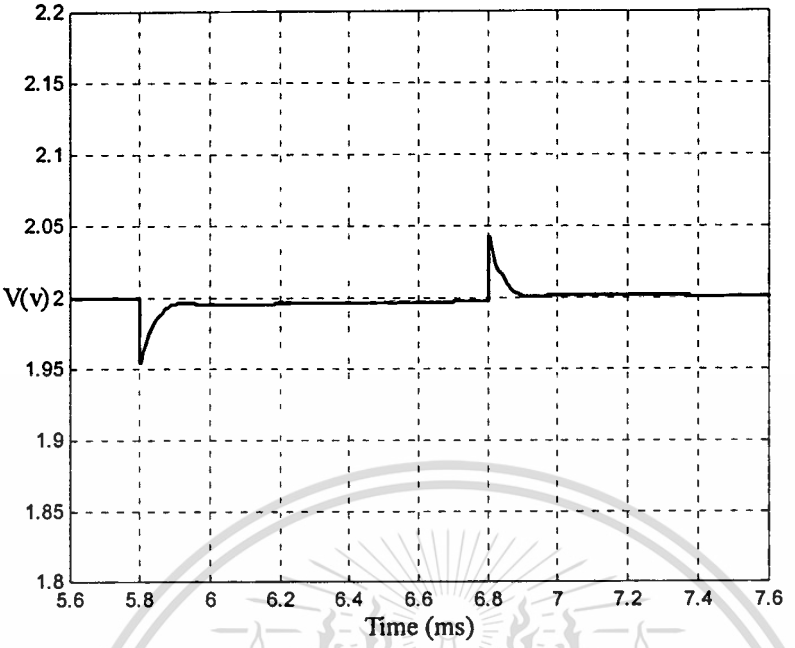


(b) Experimental

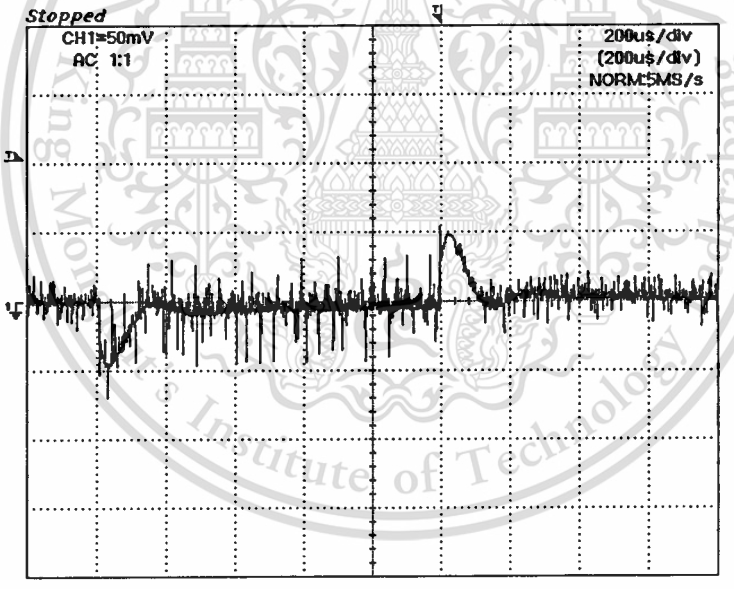
Fig 6.5 Output voltage response of buck converter with ACMC due to step load change of 3A

6.3.2 ACMC-P

The simulated and measured output voltage responses of the prototype converter with ACMC-P, when the load current is switched back and forth between 1A and 4A, are shown in Fig. 6.6. The maximum voltage drop/raise is about 47mV and the setting time is about 200μs. Compared with the results from the conventional ACMC in Fig. 6.5, the voltage drop/raise has reduced by 27% and the settling times shorten by 500μs. These represent a considerable improvement in the output dynamic performance of the converter.



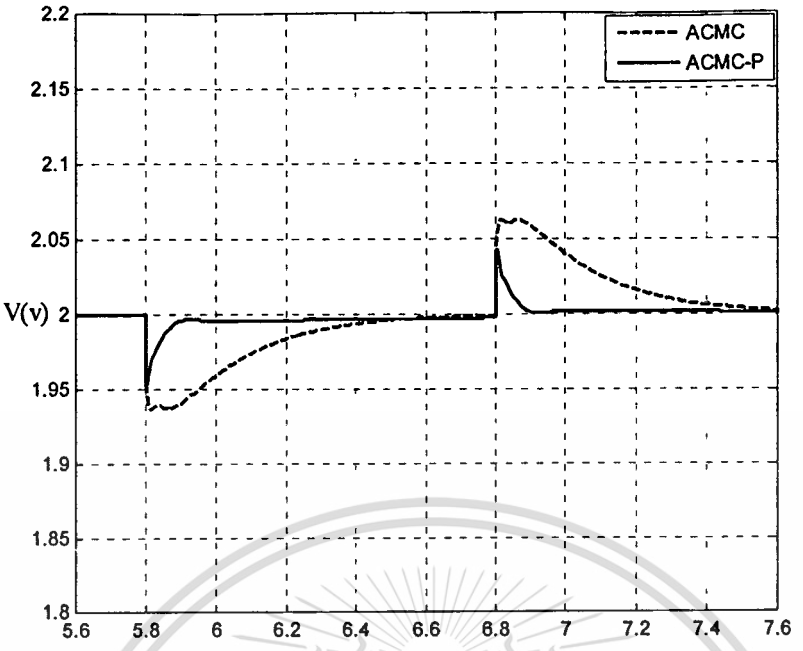
(a) Simulated



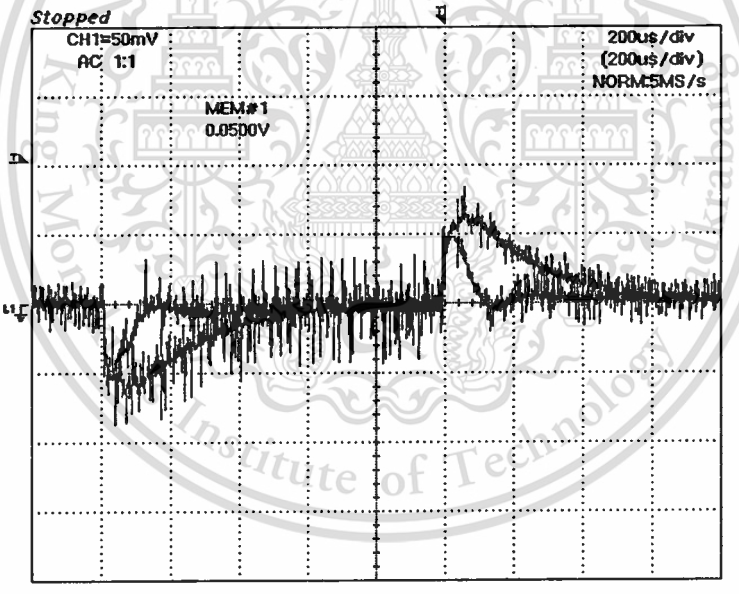
(b) Experimental

Fig 6.6 Output voltage response of buck converter with ACMC-P due to step load change of 3A

Fig. 6.7 shows the comparison of the output voltage responses of the conventional ACMC and the ACMC-P on the same scale, where the improvement yielded by the latter is evident.



(a) Simulated



(b) Experimental

Fig 6.7 Comparison between output voltage responses of buck converter with conventional ACMC and ACMC-P

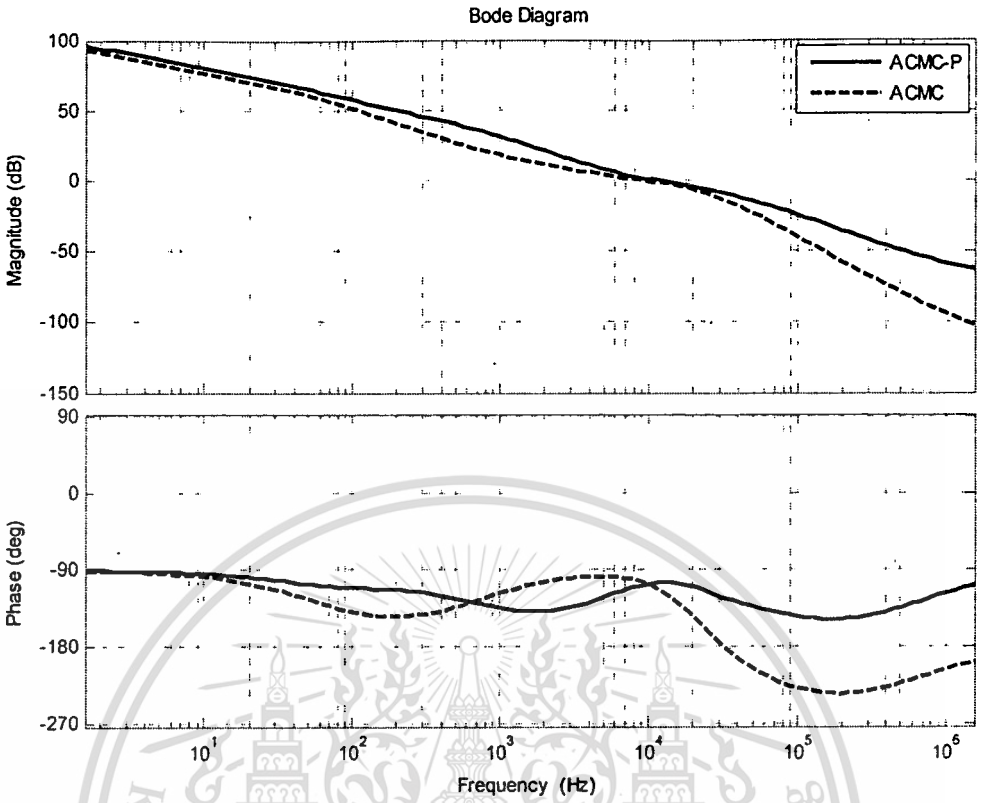
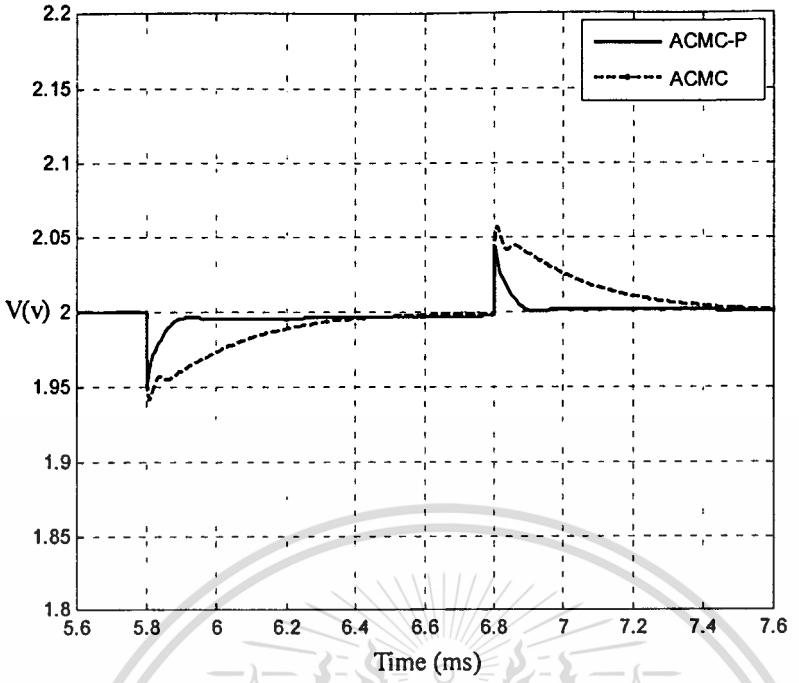
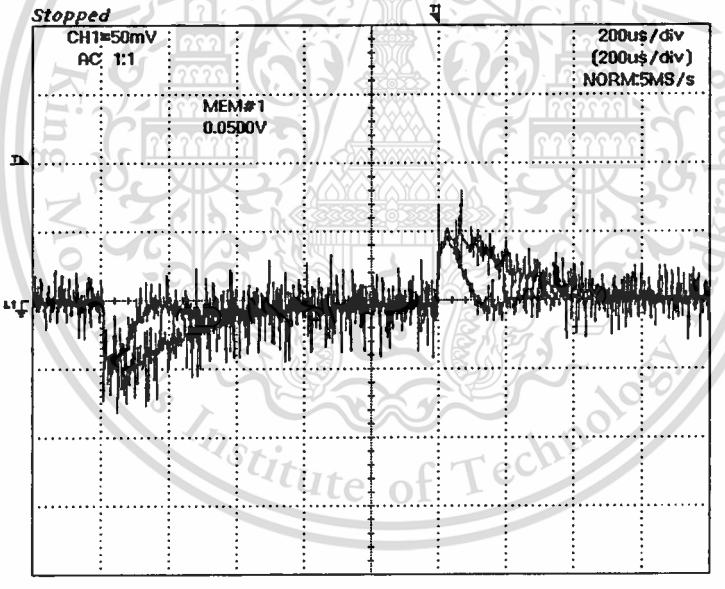


Fig 6.8 Bode diagram of ACMC and ACMC-P

For the better comparison between ACMC and ACMC-P, the voltage controller of ACMC is redesigned for a crossover frequency of 10kHz. Following the design steps in Section 5.2.2, the controller's component values are found to be: C_1=500pF, C_2=22nF, R_1=2.5kΩ, and R_2=10kΩ. Fig. 6.8 shows Bode plot of ACMC after the redesign against that of ACMC-P. It can be seen that although the crossover frequency of the two systems is now equal, ACMC-P nevertheless has a higher gain from the low up to crossover frequencies. This higher gain is attained due to that the parallel controller contains a sufficient number of poles and zeros to properly compensate the voltage loop. Fig. 6.9 compares the output voltage response of ACMC after the redesign with that of ACMC-P. Because of the higher gain, the latter exhibits a superior output performance, in which the voltage drop/rise has reduced by 7% and the settling time shorten by 350μs.



(a) Simulated



(b) Experimental

Fig 6.9 Comparison between output voltage responses of buck converter with conventional ACMC and ACMC-P

6.3.3 CFACMC

The simulated and measured output voltage responses of the prototype converter with CFACMC, when the load current is switched back and forth between 1A and 4A, are shown in Fig. 6.10. The maximum voltage drop/raise is about 60mV and the setting time is about 200μs. Compared

with the results from the conventional ACMC in Fig. 6.5, the voltage drop/raise is about 5% but the settling times shorten 400μs. These represent a considerable improvement in the output dynamic performance of the converter.

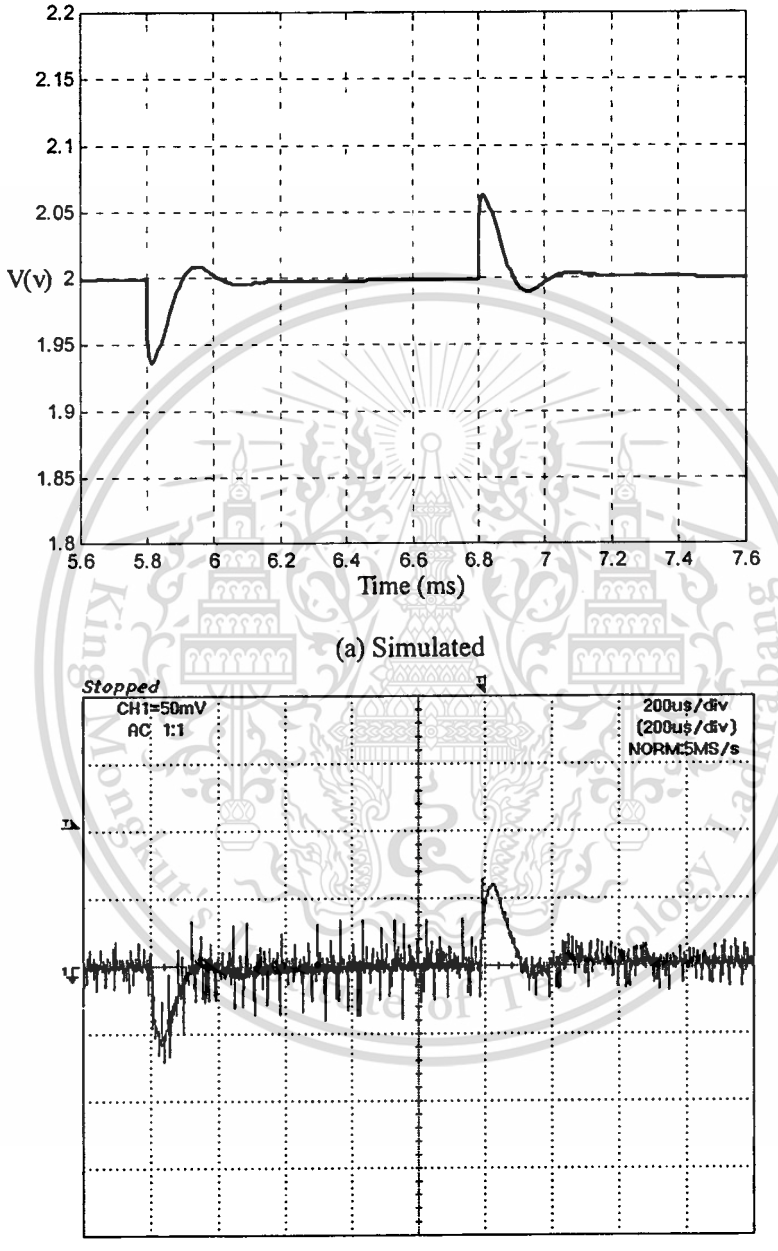
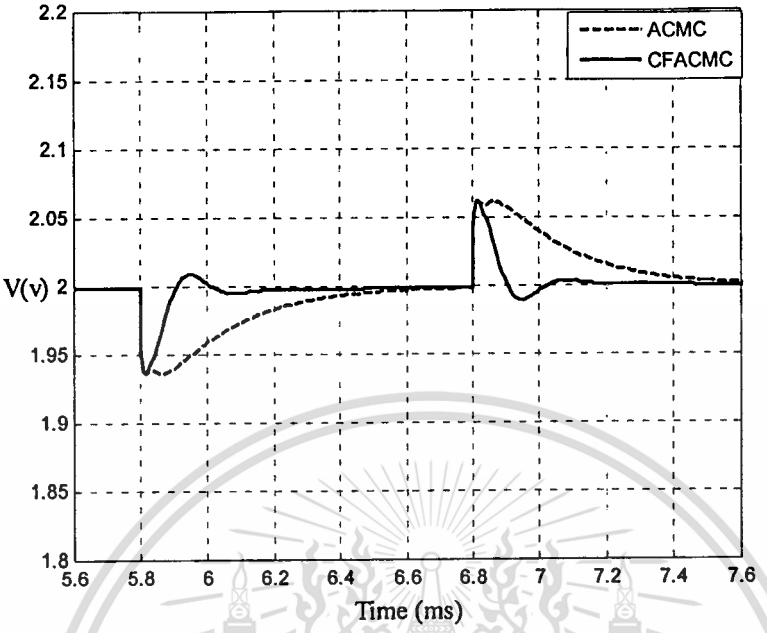
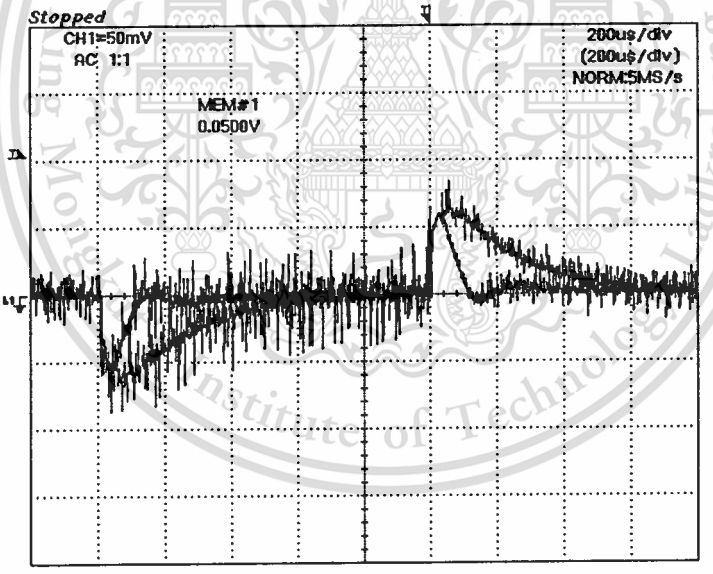


Fig 6.10 Output voltage response of buck converter with CFACMC due to step load change of 3A

Fig. 6.11 shows the comparison of the output voltage responses of the conventional ACMC and CFACMC on the same scale, where the improvement yielded by the latter is evident.



(a) Simulated



(b) Experimental

Fig 6.11 Comparison between output voltage responses of buck converter with conventional ACMC and CFACMC

Chapter 7

Conclusions

The use of a DC-DC converter as a DC power source is widespread in modern electronic applications. Besides operating at high efficiency, the converter must be able to regulate its output voltage to be within the limit desired by the load; otherwise proper operation of the load could be in jeopardy. Feedback control of the converter plays an important role in this respect since the converter's regulation characteristics depend on a control method used and how well it has been designed.

In this thesis, Average Current Mode Control (ACMC) of DC-DC converters has been studied, focusing on control, modeling, and simulation aspects. The theoretical background for ACMC was established in Chapter 3, where the converter's modeling and design voltage and current controllers discussed. Based upon ACMC principle, two novel techniques to improve output dynamic performance of the DC-DC converter have been proposed. The two proposed techniques were: (1) ACMC with a parallel controller (ACMC-P) and (2) Current Feedforward Average Current Mode Control (CFACMC). The former method was based on employment of a high-order controller to compensate the converter's voltage loop, whose behavior was mathematically described by a high-order control-to-output transfer function $H_{co}(s)$ in (3.48). In this work, the high-order controller was synthesized from parallel connection of the two standard controllers. The design and synthesizing procedures for a high-order controller were explained in Section 4.2 and illustrated in Section 5.3.

Another proposed technique was CFACMC. It was based on feedforward of the sensed inductor current, through the adjustable gain low-pass filter circuit $P_{cf}(s)$ to sum with the output signal from the voltage controller to produce the control signal. The feedforward signal helps strengthen the corrective action of the voltage loop, hence making it possible for the converter's dynamic response to be further improved from the conventional ACMC. To achieve the improved performance, an amplitude and phase of the feedforward signal must be appropriate - the wrong signal can lead to a poor response or even instability. The amplitude and phase of the feedforward signal are controlled by the low-pass filter $P_{cf}(s)$. Therefore, the gain and cut-off frequency of $P_{cf}(s)$ must be chosen such that the improved dynamic performance is attained with a minimum impact on the system stability. The design procedure for $P_{cf}(s)$ was described in Section 4.2 and illustrated in Section 5.4.

As shown by the results in Fig. 6.9 and Fig. 6.11, the two proposed techniques were capable of improving the output dynamic response of the converter subjected to a step load disturbance, compared

with the conventional ACMC. From the results, the maximum voltage drop/rise of the converter with ACMC-P and CFACMC improved only slightly from the conventional ACMC, but their settling times were about 4 times faster. This represents a considerable improvement in the dynamic response time and confirms the effectiveness of the proposed techniques in enhancing the output dynamic performance of the converter. In this thesis, Averaged models of the converter have also been developed for simulation with SIMULINK. The simulated results from the models were found to have agreed well with their experimental counterparts (Fig. 6.5-6.11). Good correspondence between these two results indicates the accuracy and validity of the developed models in predicting the converter's dynamic response. These simulation models are an indispensable tool in control design of converter.

Implementation of the proposed techniques requires only a few component added to the conventional ACMC circuit. In ACMC-P, two OpAmp circuits are required to realize the second controller and the summing circuit, while in CFACMC an *R-C* filter and two OpAmp circuits for the voltage buffer and the summing circuit are that all needed. The implementation simplicity coupled with the capability to considerably enhance the output dynamic performance of the converter makes the two proposed techniques having good potential for practical usage.

References

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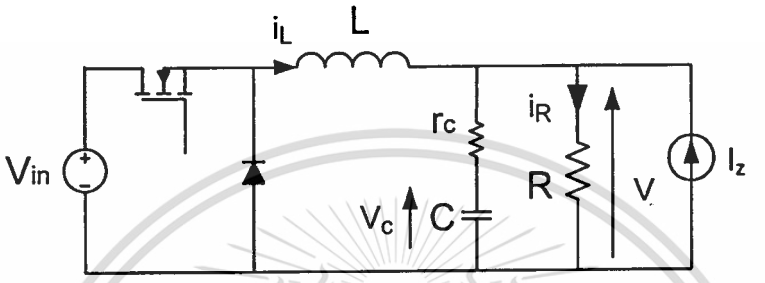
Appendices

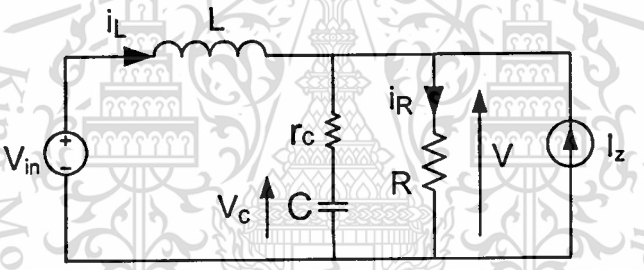
Appendix A

State-space Averaging Technique

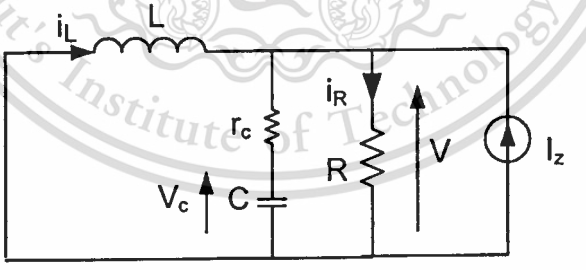
A.1 Buck converter in CCM



(a) Buck Converter



(b) Buck Converter when MOSFET is on



(c) Buck Converter when MOSFET is off

Fig. A.1 Modeling of buck converter circuit

During turning on of MOSFET, the circuit equations can be written as follows:

$$V_L = L\frac{di_L}{dt} = V_{in} - V \tag{A.1}$$

$$i_L + I_Z = i_C + i_R \tag{A.2}$$

$$i_c = C\frac{dv_c}{dt} \tag{A.3}$$

$$V = R.i_R = v_c + r_c.i_c \tag{A.4}$$

$$(A.2) \Rightarrow i_R = i_L + I_Z - i_c$$

Substituting the value of i_R into (A.4)

$$(A.4) \Rightarrow R(i_L + I_Z - i_c) = v_c + r_c.i_c$$
$$\Rightarrow (R + r_c)i_c = R.i_L - v_c + R.I_Z$$

Substituting the value of i_c into the above equation

$$(A.4) \Rightarrow (R + r_c)C\frac{dv_c}{dt} = Ri_L - v_c + R.I_Z$$
$$\Rightarrow \frac{dv_c}{dt} = \frac{R.r_c}{C(R + r_c)}i_L - \frac{1}{C(R + r_c)}v_c + \frac{R}{C(R + r_c)}I_Z$$

The output voltage V can be defined as:

$$(A.4) \Rightarrow V = v_c + r_c.i_c$$
$$\Rightarrow V = v_c + r_c.C\frac{dv_c}{dt}$$
$$= v_c + r_c.C\left[\frac{R.r_c}{C(R + r_c)}i_L - \frac{1}{C(R + r_c)}v_c + \frac{R}{C(R + r_c)}I_Z\right]$$
$$\Rightarrow V = \frac{R.r_c}{(R + r_c)}i_L + \frac{R}{(R + r_c)}v_c + \frac{R.r_c}{(R + r_c)}I_Z$$

$$(A.1) \Rightarrow \frac{di_L}{dt} = -\frac{V}{L} + \frac{V_{in}}{L}$$

Substituting the value of V into the above equation

$$\Rightarrow \frac{di_L}{dt} = -\frac{R.r_c}{(R + r_c)L}i_L - \frac{R}{(R + r_c)L}v_c + \frac{V_{in}}{L} - \frac{R.r_c}{(R + r_c)L}I_Z$$

Rearrange the related equations

$$\frac{di_L}{dt} = -\frac{R.r_c}{(R+r_c)L} i_L - \frac{R}{(R+r_c)L} v_c + \frac{V_{in}}{L} - \frac{R.r_c}{(R+r_c)L} I_Z$$

$$\frac{dv_c}{dt} = \frac{R.r_c}{C(R+r_c)} i_L - \frac{1}{C(R+r_c)} v_c + \frac{R}{C(R+r_c)} I_Z$$

$$V = \frac{R.r_c}{(R+r_c)} i_L - \frac{R}{(R+r_c)} v_c + \frac{R.r_c}{(R+r_c)} I_Z$$

Rewrite above equation in matrix form:

$$\begin{cases} \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-R.r_c}{L(R+r_c)} & \frac{-R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & \frac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{-R.r_c}{L(R+r_c)} \\ 0 & \frac{R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \\ V = \begin{bmatrix} \frac{R.r_C}{R+r_C} & \frac{R}{R+r_C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & \frac{R.r_C}{R+r_C} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \end{cases} \quad \text{(A.5)}$$

During turning off of MOSFET, the circuit equations can be written as follows:

$$V_L = L\frac{di_L}{dt} = -V \quad \text{(A.6)}$$

$$i_L + I_Z = i_C + i_R \quad \text{(A.7)}$$

$$i_c = C\frac{dv_c}{dt} \quad \text{(A.8)}$$

$$V = R.i_R = v_c + r_c.i_c \quad \text{(A.9)}$$

$$\text{(A.7)} \quad \Rightarrow \quad i_R = i_L + I_z - i_c$$

Substituting the value of i_R into (A.9)

$$\text{(A.9)} \Rightarrow R(i_L + I_Z - i_c) = v_c + r_c.i_c$$
$$\Rightarrow (R+r_c)i_c = R.i_L - v_c + R.I_z$$

Substituting the value of i_c into the above equation

$$\text{(A.9)} \Rightarrow (R+r_c)C\frac{dv_c}{dt} = Ri_L - v_c + R.I_Z$$
$$\Rightarrow \frac{dv_c}{dt} = \frac{R.r_c}{C(R+r_c)} i_L - \frac{1}{C(R+r_c)} v_c + \frac{R}{C(R+r_c)} I_Z$$

The output voltage V can be defined as:

$$(A.9) \Rightarrow V = v_c + r_c . i_c$$

$$\Rightarrow V = v_c + r_c . C \frac{dv_c}{dt}$$

$$= v_c + r_c . C \left[\frac{R.r_c}{C(R+r_c)} i_L - \frac{1}{C(R+r_c)} v_c + \frac{R}{C(R+r_c)} I_Z \right]$$

$$\Rightarrow V = \frac{R.r_c}{(R+r_c)} i_L + \frac{R}{(R+r_c)} v_c + \frac{R.r_c}{(R+r_c)} I_Z$$

$$(A.7) \Rightarrow \frac{di_L}{dt} = -\frac{V}{L}$$

Substituting the value of V into the above equation

$$\Rightarrow \frac{di_L}{dt} = -\frac{R.r_c}{(R+r_c)L} i_L - \frac{R}{(R+r_c)L} v_c - \frac{R.r_c}{(R+r_c)L} I_Z$$

Rearrange the related equations

$$\frac{di_L}{dt} = -\frac{R.r_c}{(R+r_c)L} i_L - \frac{R}{(R+r_c)L} v_c - \frac{R.r_c}{(R+r_c)L} I_Z$$

$$\frac{dv_c}{dt} = \frac{R.r_c}{C(R+r_c)} i_L - \frac{1}{C(R+r_c)} v_c + \frac{R}{C(R+r_c)} I_Z$$

$$V = \frac{R.r_c}{(R+r_c)} i_L - \frac{R}{(R+r_c)} v_c + \frac{R.r_c}{(R+r_c)} I_Z$$

Rewrite above equation in matrix form:

$$\begin{cases} \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-R.r_c}{L(R+r_c)} & \frac{-R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & \frac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & \frac{-R.r_c}{L(R+r_c)} \\ 0 & \frac{R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \\ V = \begin{bmatrix} \frac{R.r_C}{R+r_C} & \frac{R}{R+r_C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & \frac{R.r_C}{R+r_C} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \end{cases} \quad (A.10)$$

A.2 Buck converter transfer functions

The average equation of (A.5) and (A.10) was given in (3.26). It is recalled again here:

$$\begin{cases} \begin{bmatrix} \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} \dfrac{-R.r_c}{L(R+r_c)} & \dfrac{-R}{L(R+r_c)} \\ \dfrac{R}{C(R+r_c)} & \dfrac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \dfrac{d}{L} & \dfrac{-R.r_c}{L(R+r_c)} \\ 0 & \dfrac{R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \\ V = \begin{bmatrix} \dfrac{R.r_c}{R+r_c} & \dfrac{R}{R+r_c} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & \dfrac{R.r_c}{R+r_c} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \end{cases} \tag{A.11}$$

The linearised equation of (A.11) was given in (3.27). It is repeated:

$$\begin{cases} \begin{bmatrix} \dot{\hat{i}}_L \\ \dot{\hat{v}}_c \end{bmatrix} = \begin{bmatrix} \dfrac{-R.r_c}{L(R+r_c)} & \dfrac{-R}{L(R+r_c)} \\ \dfrac{R}{C(R+r_c)} & \dfrac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_c \end{bmatrix} + \begin{bmatrix} \dfrac{D}{L} & \dfrac{-R.r_c}{L(R+r_c)} & \dfrac{V_{in}}{L} \\ 0 & \dfrac{R}{C(R+r_c)} & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_z \\ \hat{d} \end{bmatrix} \\ \hat{v} = \begin{bmatrix} \dfrac{R.r_c}{R+r_c} & \dfrac{R}{R+r_c} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_c \end{bmatrix} + \begin{bmatrix} 0 & \dfrac{R.r_c}{R+r_c} & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_z \\ \hat{d} \end{bmatrix} \end{cases} \tag{A.12}$$

Express (A.12) in general state-space format

$$\begin{cases} \dot{\hat{x}} = A\hat{x} + \begin{bmatrix} B_{u1} & B_{u2} & B_d \end{bmatrix} \begin{bmatrix} \hat{u}_1 \\ \hat{u}_2 \\ \hat{d} \end{bmatrix} \\ \hat{y} = C\hat{x} + \begin{bmatrix} E_{u1} & E_{u2} & E_d \end{bmatrix} \begin{bmatrix} \hat{u}_1 \\ \hat{u}_2 \\ \hat{d} \end{bmatrix} \end{cases} \tag{A.13}$$

From (A.12), various transfer functions can be derived. In this work, only two transfer functions $G_{dv}(s)$ and $G_{di}(s)$ are needed for the control design.

Duty ratio to output transfer function $G_{dv}(s)$ can be found from (3.15)

$$G_{dv}(s) = C[sI-A]^{-1}B_d + E_d$$

$$G_{dv}(s)=\begin{bmatrix}\frac{R.r_C}{R+r_C} & \frac{R}{R+r_C}\end{bmatrix}\left[\begin{bmatrix}s & 0\\ 0 & s\end{bmatrix}-\begin{bmatrix}\frac{-R.r_C}{L(R+r_C)} & \frac{-R}{L(R+r_C)}\\ \frac{R}{C(R+r_C)} & \frac{-1}{C(R+r_C)}\end{bmatrix}\right]^{-1}\begin{bmatrix}\frac{V_{in}}{L}\\ 0\end{bmatrix}$$

Let

$$A_s=\left[\begin{bmatrix}s & 0\\ 0 & s\end{bmatrix}-\begin{bmatrix}\frac{-R.r_C}{L(R+r_C)} & \frac{-R}{L(R+r_C)}\\ \frac{R}{C(R+r_C)} & \frac{-1}{C(R+r_C)}\end{bmatrix}\right]=\begin{bmatrix}s+\frac{R.r_c}{L(R+r_c)} & \frac{R}{L(R+r_c)}\\ \frac{-R}{C(R+r_c)} & s+\frac{1}{C(R+r_c)}\end{bmatrix}$$

$$\Rightarrow A_s^{-1}=\frac{1}{\det(A_s)}\begin{bmatrix}s+\frac{1}{C(R+r_C)} & \frac{-R}{L(R+r_C)}\\ \frac{R}{C(R+r_C)} & s+\frac{R.r_C}{L(R+r_C)}\end{bmatrix}$$

$$\det(A_s)=s^2+s\left(\frac{1}{CR}+\frac{r_c}{L}\right)+\frac{1}{LC}$$

$$G_{dv}(s)=\begin{bmatrix}r_c & 1\end{bmatrix}\frac{1}{\det(A_s)}\begin{bmatrix}s+\frac{1}{C(R+r_c)} & \frac{-R}{L(R+r_c)}\\ \frac{R}{C(R+r_c)} & s+\frac{R.r_c}{L(R+r_c)}\end{bmatrix}\begin{bmatrix}\frac{V_{in}}{L}\\ 0\end{bmatrix}$$

$$G_{dv}(s)=\frac{V_{in}}{LC}\frac{1+sr_CC}{s^2+s\left(\frac{1}{RC}+\frac{r_C}{L}\right)+\frac{1}{LC}}$$

Duty ratio to inductor current transfer function $G_{di}(s)$ can be found from (3.15)

$$G_{di}(s)=C_i[sI-A]^{-1}B_d$$

$$G_{di}(s)=\begin{bmatrix}1 & 0\end{bmatrix}\frac{1}{\det(A_s)}\begin{bmatrix}s+\frac{1}{C(R+r_c)} & \frac{-R}{L(R+r_c)}\\ \frac{R}{C(R+r_c)} & s+\frac{R.r_c}{L(R+r_c)}\end{bmatrix}\begin{bmatrix}\frac{V_{in}}{L}\\ 0\end{bmatrix}$$

$$G_{di}(s)=\frac{V_{in}}{LCR}\frac{1+s(R+r_c)C}{s^2\left(1+\frac{r_C}{R}\right)+s\left(\frac{1}{RC}+\frac{r_c}{L}\right)+\frac{1}{LC}}$$

Appendix B

The solution for $G_{c1}(s)$ and $G_{c2}(s)$

The know parameters are k_2, w_{cp1}, w_{cp2}, w_{cp3}, a_0, a_1, a_2 and a_3. We want to find w_β, w_γ, k_1 *and* w_α.

$$\begin{cases} \dfrac{k_1}{k_2} w_\alpha w_{cp1} w_{cp3} = a_0 & (1) \\ \dfrac{k_2 w_\gamma w_\beta w_{cp2} + k_1[w_{cp1} w_{cp3} + w_\alpha(w_{cp1} + w_{cp3})]}{k_2} = a_1 & (2) \\ \dfrac{k_2[(w_\gamma + w_\beta)w_{cp2} + w_\gamma w_\beta] + k_1(w_\alpha + w_{cp1} + w_{cp2})}{k_2} = a_2 & (3) \\ \dfrac{k_2(w_\gamma + w_\beta + w_{cp2}) + k_1}{k_2} = a_3 & (4) \end{cases}$$

Equation (1) can be written

$$k_1 w_\alpha = a_0 k_2 / (w_{cp1} w_{cp3})$$

Equation (4) can be written

$$k_1 = k_2 a_3 - k_2 w_{cp2} - k_2 (w_\beta + w_\gamma)$$

or

$$k_1 = \lambda_3 - k_2 (w_\beta + w_\gamma)$$

where $\lambda_3 = k_2 a_3 - k_2 w_{cp2}$

Substituting $k_1 w_\alpha$ and k_1 into (2) and (3) and rearranging the equation:

$$\begin{cases} k_2 w_{cp2} w_\beta w_\gamma - w_{cp1} w_{cp3}(w_\beta + w_\gamma) = \lambda_1 - w_{cp1} w_{cp3} \lambda_3 \\ k_2 w_\beta w_\gamma + k_2(w_{cp2} - w_{cp1} - w_{cp3})(w_\beta + w_\gamma) = \lambda_2 - (w_{cp1} + w_{cp3})\lambda_3 \end{cases}$$

where $\lambda_1 = k_2 a_1 - a_0 k_2 (w_{cp1} + w_{cp3}) / w_{cp1} w_{cp3}$

$\lambda_2 = k_2 a_2 - a_0 k_2 / w_{cp1} w_{cp3}$

By arranging in matrix form:

$$\begin{bmatrix} k_2 w_{cp2} & -w_{cp1} w_{cp3} \\ k_2 & k_2(w_{cp2} - w_{cp1} - w_{cp3}) \end{bmatrix} \begin{bmatrix} w_\beta w_\gamma \\ w_\beta + w_\gamma \end{bmatrix} = \begin{bmatrix} \lambda_1 - w_{cp1} w_{cp3} \lambda_3 \\ \lambda_2 - (w_{cp1} + w_{cp3})\lambda_3 \end{bmatrix}$$

Solving above equations, we can obtain $w_\beta w_\gamma$ and $(w_\beta + w_\gamma)$. Each unknown parameters w_β and w_γ can be found by solving the equation below

$$x^2 - (w_\beta + w_\gamma)x + w_\beta w_\gamma = 0$$

which gives the solutions:

$$x_1 = w_\beta$$

$$x_2 = w_\gamma$$

Substitution of w_β and w_γ into related equations, therefore, k_1 and w_α can be written as:

$$k_1 = \lambda_3 - k_2(w_\beta + w_\gamma)$$

$$w_\alpha = a_0 k_2 / (w_{cp1} w_{cp3}) k_1$$

Appendix C

The solution for $G_{c1}(s)$ and $G_{c2}(s)$ by MATLAB

```
%%The Solution of Gc1(s) and Gc2(s) %%
%% The Location of Zero and Pole
wz1=390; wz2=6.0e4; wz3=1.8e5; wz4=1.8e5;
wp1=4.3e3; wp2=2.5e5; wp3=3.5e5;

% The controller Gc3(s) is:
Ze=[-wz1 –wz2 –wz3 –wz4];
Po=[0  -wp1 –wp2 –wp3];
Ze1=poly(Ze);
Po1=poly(Po);
Gc3=tf(Ze1,Po1);

%Define the parameters
 p1=-Po(:,2); p2=-Po(:,3); p3=-Po(:,4); k=6.8;
 a0=Ze1(:,5); a1=Ze1(:,4); a2=Ze1(:,3); a3=Ze1(:,2);
gama1=a1*k-((a0*k*(wp1+p3))/p1/p3);
gama2=a2*k-((a0*k)/p1/p3);
gama3=a3*k-(p2*k);

% Define a square matrices
a11=k*p2;
a12=-p1*p3;
a21=k;
a22=k*p2-k*(p1+p3);

b11=gama1-(p1*p3*gama3);
b21=gama2-((p1+p3)*gama3);
```

```
Ag=[a11 a12; a21 a22];
Bg=[b11;b21];

Xz=inv(Ag)*Bg;
epol=[1 -Xz(2,:) Xz(1,:)];

% %Solution for Gc1(s) and Gc2(s)
BetaNGama=roots(epol);
k1=a3*k-k*(p2+Xz(2,:));
alpha=a0*k/(p1*p3*k1);
```

Appendix D

Transfer functions $H_{co}(s)$ and $H_{cl}(s)$

D.1 Transfer function $H_{co}(s)$

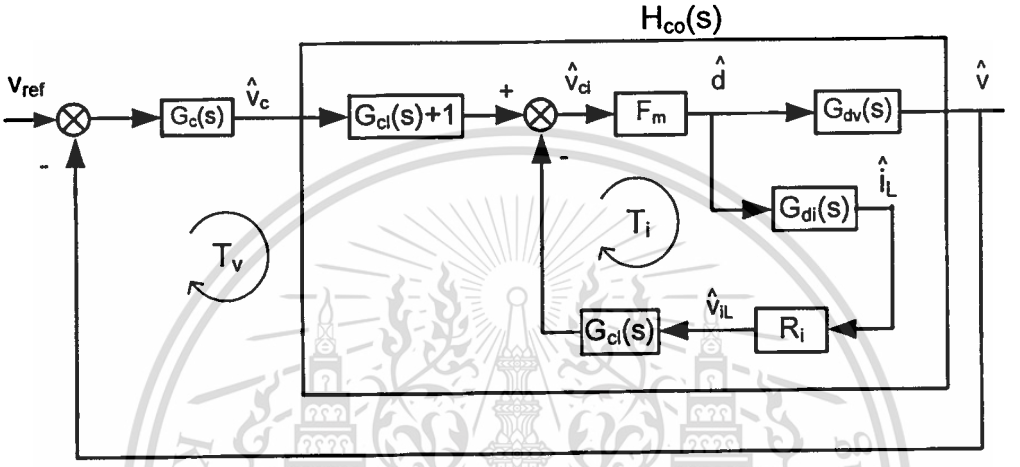


Fig D.1 Small-signal model of buck converter with ACMC

From the figure, $H_{co}(s)$ can be defined

$$H_{co}(s) = [G_{cl}(s) + 1] G_{dv}(s).T_i^{'}$$

where

$$T_i^{'} = \frac{F_m}{1 + F_m R_i G_{di}(s) G_{cl}(s)}$$

Recall the related transfer functions

$$G_{di}(s) = \frac{N_{di}(s)}{D_{di}(s)} = \frac{V_{in}}{LCR} \frac{1 + s(R + r_c)C}{s^2 + s\left(\frac{1}{RC} + \frac{r_c}{L}\right) + \frac{1}{LC}}$$

$$G_{dv}(s) = \frac{N_{dv}(s)}{D_{dv}(s)} = \frac{V_{in}}{LC} \frac{1 + sr_C C}{s^2 + s\left(\frac{1}{RC} + \frac{r_C}{L}\right) + \frac{1}{LC}}$$

$$G_{cl}(s) = \frac{N_{cl}(s)}{D_{cl}(s)} = \frac{w_{cl}}{s}\frac{1+\frac{s}{w_{clz}}}{1+\frac{s}{w_{clp}}}$$

$$\Rightarrow T_i^{'} = \frac{N_i^{'}(s)}{D_i^{'}(s)} = \frac{F_m}{1+F_m R_i \frac{N_{di}(s)}{D_{di}(s)}\frac{N_{cl}(s)}{D_{cl}(s)}}$$

$$= \frac{F_m D_{di}(s) D_{cl}(s)}{D_{di}(s)D_{cl}(s) + F_m R_i N_{di}(s) N_{cl}(s)}$$

By assuming $R >> r_c$

$$D_{di}(s)D_{cl}(s) = LCR\left[s^2 + s\left(\frac{1}{RC}+\frac{r_c}{L}\right)+\frac{1}{LC}\right]\left[s(1+\frac{s}{w_{clp}})\right]$$

$$= \frac{LCR}{w_{clp}}\left[s^4 + \left(w_{clp}+\frac{1}{RC}+\frac{r_c}{L}\right)s^3 + \left(w_{clp}\left(\frac{1}{RC}+\frac{r_c}{L}\right)+\frac{1}{LC}\right)s^2 + \frac{w_{clp}}{LC}s\right]$$

$$F_m R_i N_{di}(s) N_{cl}(s) = F_m R_i V_{in}(1+sRC)w_{cl}\left(1+\frac{s}{w_{clz}}\right)$$

$$= \frac{F_m R_i V_{in} w_{cl}}{w_{clz}}(1+sRC)(s+w_{clz})$$

$$= \frac{F_m R_i V_{in} w_{cl}}{w_{clz}}\left[s^2 RC + s\left(1+RCw_{clz}\right)+w_{clz}\right]$$

Let

$$\beta = \frac{LCR}{w_{clp}}$$

$$\alpha = \frac{F_m R_i V_{in} w_{cl}}{w_{clz}}$$

The denominator $D_i^{'}(s)$ of $T_i^{'}$ can be written as

$$\Rightarrow D_i^{'}(s) = D_{di}(s)D_{cl}(s) + F_m R_i N_{di}(s) N_{cl}(s)$$

$$= \beta\left[s^4 + \left(w_{clp}+\frac{1}{RC}+\frac{r_c}{L}\right)s^3 + \left(w_{clp}(\frac{1}{RC}+\frac{r_c}{L})+\frac{1}{LC}\right)s^2 + \frac{w_{clp}}{LC}s\right]$$

$$+ \alpha\left[s^2 RC + s\left(1+RCw_{clz}\right)+w_{clz}\right]$$

$$D_i'(s)=\beta\left[\begin{array}{l}s^4+\left(w_{clp}+\frac{1}{RC}+\frac{r_c}{L}\right)s^3+\left(w_{clp}\left(\frac{1}{RC}+\frac{r_c}{L}\right)+\frac{1}{LC}+\frac{\alpha RC}{\beta}\right)s^2\\+\left(\frac{w_{clp}}{LC}+\frac{\alpha\left(1+RCw_{clz}\right)}{\beta}\right)s+\frac{\alpha w_{clz}}{\beta}\end{array}\right]$$

$$\Rightarrow T_i'=\frac{N_i'(s)}{D_i'(s)}=\frac{F_m D_{di}(s)D_{cl}(s)}{\beta\left[\begin{array}{l}s^4+\left(w_{clp}+\frac{1}{RC}+\frac{r_c}{L}\right)s^3+\left(w_{clp}\left(\frac{1}{RC}+\frac{r_c}{L}\right)+\frac{1}{LC}+\frac{\alpha RC}{\beta}\right)s^2\\+\left(\frac{w_{clp}}{LC}+\frac{\alpha\left(1+RCw_{clz}\right)}{\beta}\right)s+\frac{\alpha w_{clz}}{\beta}\end{array}\right]}$$

$$G_{cl}(s)+1=\frac{N_{cl}(s)}{D_{cl}(s)}+1=\frac{N_{cl}(s)+D_{cl}(s)}{D_{cl}(s)}$$

$$=\frac{1}{w_{clp}}\frac{s^2+\left(w_{clp}+\frac{w_{cl}w_{clp}}{w_{clz}}\right)s+w_{cl}w_{clp}}{s\left(1+\frac{s}{w_{clp}}\right)}$$

Therefore,

$$H_{co}(s)=\left[G_{Cl}(s)+1\right]G_{dv}(s)T_i'=\left(\frac{N_{cl}(s)+D_{cl}(s)}{D_{cl}(s)}\right)\frac{N_{dv}(s)}{D_{dv}(s)}\frac{N_i'(s)}{D_i'(s)}$$

$$H_{co}(s)=\frac{1}{w_{clp}}\frac{s^2+\left(w_{clp}+\frac{w_{cl}w_{clp}}{w_{clz}}\right)s+w_{cl}w_{clp}}{D_{cl}(s)}\frac{N_{dv}(s)}{D_{dv}(s)}$$

$$\frac{F_m D_{di}(s)D_{cl}(s)}{\beta\left[\begin{array}{l}s^4+\left(w_{clp}+\frac{1}{RC}+\frac{r_c}{L}\right)s^3+\left(w_{clp}\left(\frac{1}{RC}+\frac{r_c}{L}\right)+\frac{1}{LC}+\frac{\alpha RC}{\beta}\right)s^2\\+\left(\frac{w_{clp}}{LC}+\frac{\alpha\left(1+RCw_{clz}\right)}{\beta}\right)s+\frac{\alpha w_{clz}}{\beta}\end{array}\right]}$$

or

$$H_{co}(s)=\frac{1}{w_{clp}}\frac{F_m V_{in}R\left(1+sr_cC\right)\left[s^2+\left(w_{clp}+\frac{w_{cl}w_{clp}}{w_{clz}}\right)s+w_{cl}w_{clp}\right]}{\beta\left[\begin{array}{l}s^4+\left(w_{clp}+\frac{1}{RC}+\frac{r_c}{L}\right)s^3+\left(w_{clp}\left(\frac{1}{RC}+\frac{r_c}{L}\right)+\frac{1}{LC}+\frac{\alpha RC}{\beta}\right)s^2\\+\left(\frac{w_{clp}}{LC}+\frac{\alpha\left(1+RCw_{clz}\right)}{\beta}\right)s+\frac{\alpha w_{clz}}{\beta}\end{array}\right]}$$

Finally, $H_{co}(s)$ can be written as:

$$H_{co}(s)=\frac{F_m V_{in} R}{\beta w_{clp}} \frac{\left[\begin{array}{l} r_c C s^3+\left(1+r_C C\left(w_{clp}+\frac{w_{cl} w_{clp}}{w_{clz}}\right)\right) s^2 \\ +\left(\left(w_{clp}+\frac{w_{cl} w_{clp}}{w_{clz}}\right)+r_c C w_{cl} w_{clp}\right) s+w_{cl} w_{clp} \end{array}\right]}{\left[\begin{array}{l} s^4+\left(w_{clp}+\frac{1}{RC}+\frac{r_C}{L}\right) s^3+\left(w_{clp}\left(\frac{1}{RC}+\frac{r_C}{L}\right)+\frac{1}{LC}+\frac{\alpha RC}{\beta}\right) s^2 \\ +\left(\frac{w_{clp}}{LC}+\frac{\alpha\left(1+RC w_{clz}\right)}{\beta}\right) s+\frac{\alpha w_{clz}}{\beta} \end{array}\right]}$$

or

$$H_{co}(s)=H_c \frac{b_3 s^3+b_2 s^2+b_1 s+b_0}{s^4+a_3 s^3+a_2 s^2+a_1 s+a_0}$$

where

$$H_c=\frac{F_m V_{in}}{LC}$$

$$b_3=r_c C$$

$$b_2=1+r_c C\left(w_{clp}+\frac{w_{cl} w_{clp}}{w_{clz}}\right)$$

$$b_1=\left(w_{clp}+\frac{w_{cl} w_{clp}}{w_{clz}}\right)+r_c C w_{cl} w_{clp}$$

$$b_0=w_{cl} w_{clp}$$

$$\alpha=\frac{F_m R_1 V_{in} w_{cl}}{w_{clz}}$$

$$\beta=\frac{LCR}{w_{clp}}$$

$$a_3=w_{clp}+\frac{1}{RC}+\frac{r_c}{L}$$

$$a_2=w_{clp}\left(\frac{1}{RC}+\frac{r_c}{L}\right)+\frac{1}{LC}+\frac{\alpha RC}{\beta}$$

$$a_1=\frac{w_{clp}}{LC}+\frac{\alpha\left(1+w_{clz} RC\right)}{\beta}$$

$$a_0=\frac{\alpha w_{clz}}{\beta}$$

D.2 Transfer function $H_{cl}(s)$:

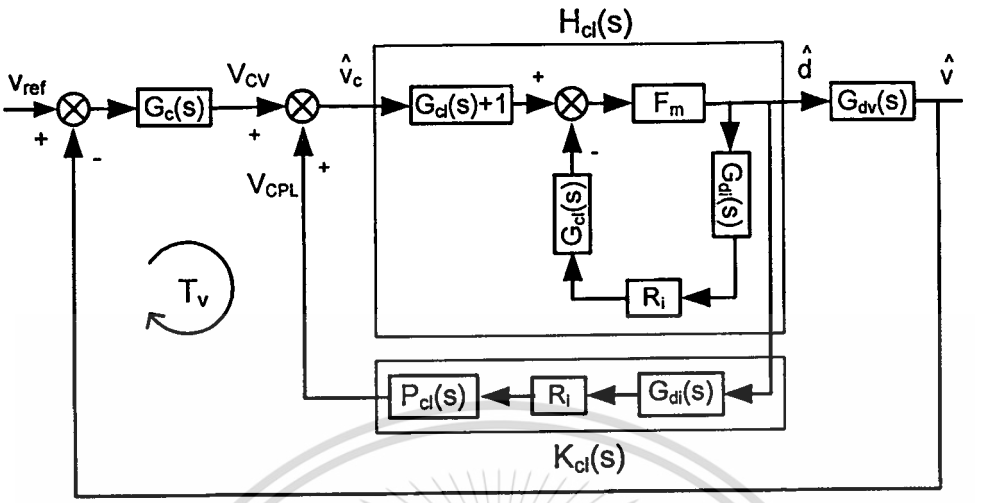


Fig. D.2 Small-signal model of buck converter with CFACMC

From the small signal diagram shows in Fig D.2, $H_{cl}(s)$ can be written:

$$H_{cl}(s) = (G_{cl}(s)+1)T_i'$$
$$= (G_{cl}(s)+1)\frac{F_m}{1+F_m R_i G_{cl}(s) G_{di}(s)}$$

By using the expression of $G_{cl}(s)$ and T_i' in section D.1 $H_{cl}(s)$ can expressed as

$$H_{cl}(s) = \frac{N_{cl}(s)+D_{cl}(s)}{D_{cl}(s)}\frac{N_i'(s)}{D_i'(s)}$$
$$= \frac{1}{w_{clp}}\frac{s^2+\left(w_{clp}+\frac{w_{cl}w_{clp}}{w_{clz}}\right)s+w_{cl}w_{clp}}{s\left(1+\frac{s}{w_{clp}}\right)}$$
$$\frac{F_m D_{di}(s) D_{cl}(s)}{\beta\left[s^4+\left(w_{clp}+\frac{1}{RC}+\frac{r_c}{L}\right)s^3+\left(w_{clp}\left(\frac{1}{RC}+\frac{r_c}{L}\right)+\frac{1}{LC}+\frac{\alpha RC}{\beta}\right)s^2\right.}$$
$$\left.+\left(\frac{w_{clp}}{LC}+\frac{\alpha(1+RCw_{clz})}{\beta}\right)s+\frac{\alpha w_{clz}}{\beta}\right]$$

$$H_{cl}(s) = \frac{F_m LCR}{\beta w_{clp}} \frac{\left[s^2 + \left(w_{clp} + \frac{w_{cl}w_{clp}}{w_{clz}}\right)s + w_{cl}w_{clp}\right]\left[s^2 + s\left(\frac{1}{RC} + \frac{r_c}{L}\right) + \frac{1}{LC}\right]}{\left[s^4 + \left(w_{clp} + \frac{1}{RC} + \frac{r_c}{L}\right)s^3 + \left(w_{clp}\left(\frac{1}{RC} + \frac{r_c}{L}\right) + \frac{1}{LC} + \frac{\alpha RC}{\beta}\right)s^2 + \left(\frac{w_{clp}}{LC} + \frac{\alpha\left(1 + RCw_{clz}\right)}{\beta}\right)s + \frac{\alpha w_{clz}}{\beta}\right]}$$

Hence,

$$H_{cl}(s) = H_{ck} \frac{\left[s^2 + s\left(w_{clp} + \frac{w_{cl}w_{clp}}{w_{clz}}\right) + w_{cl}w_{clp}\right]\left[s^2 + s\left(\frac{1}{RC} + \frac{r_c}{L}\right) + \frac{1}{LC}\right]}{s^4 + a_{H3}s^3 + a_{H2}s^2 + a_{H1}s + a_{H0}}$$

where

$$H_{ck} = F_m$$

$$\alpha = \frac{F_m R_1 V_{in} w_{cl}}{w_{clz}}$$

$$\beta = \frac{LCR}{w_{clp}}$$

$$a_{H3} = w_{clp} + \frac{1}{RC} + \frac{r_c}{L}$$

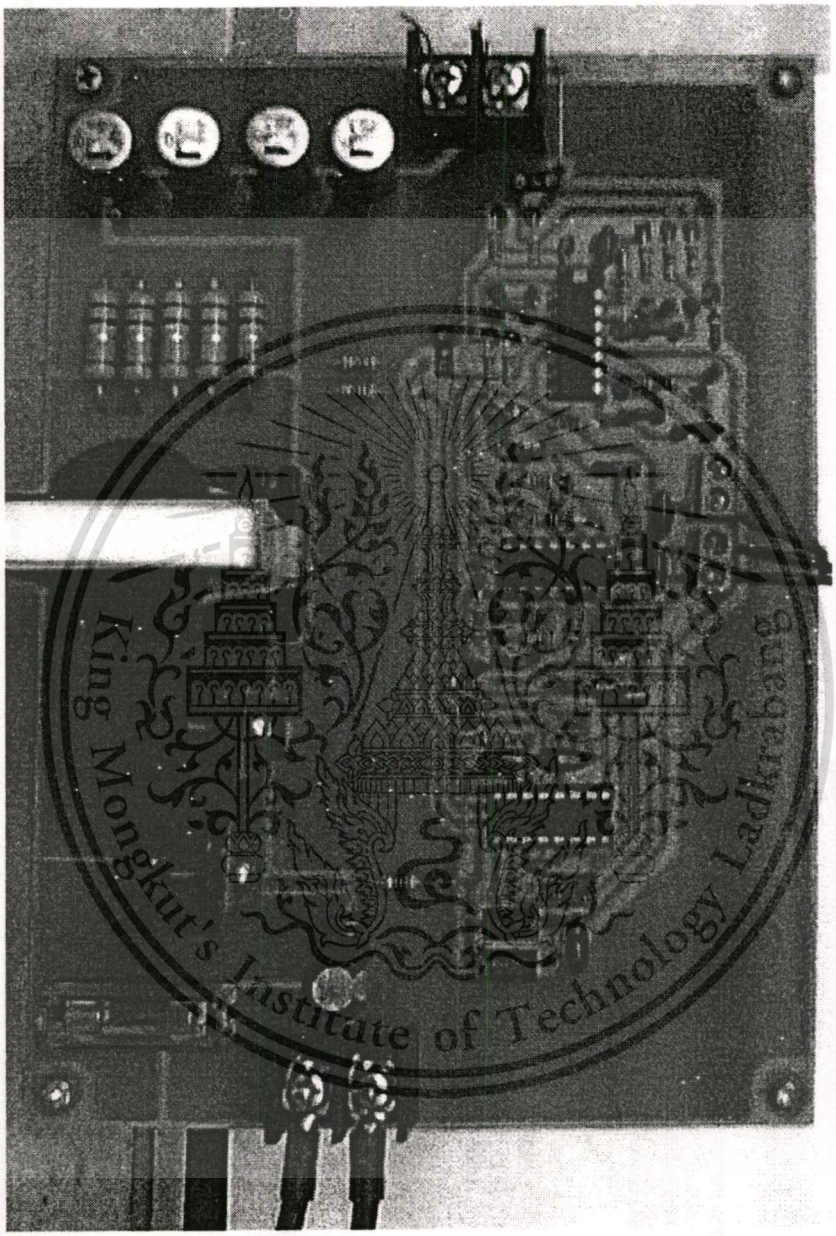
$$a_{H2} = w_{clp}\left(\frac{1}{RC} + \frac{r_c}{L}\right) + \frac{1}{LC} + \frac{\alpha RC}{\beta}$$

$$a_{H1} = \frac{w_{clp}}{LC} + \frac{\alpha\left(1 + w_{clz}RC\right)}{\beta}$$

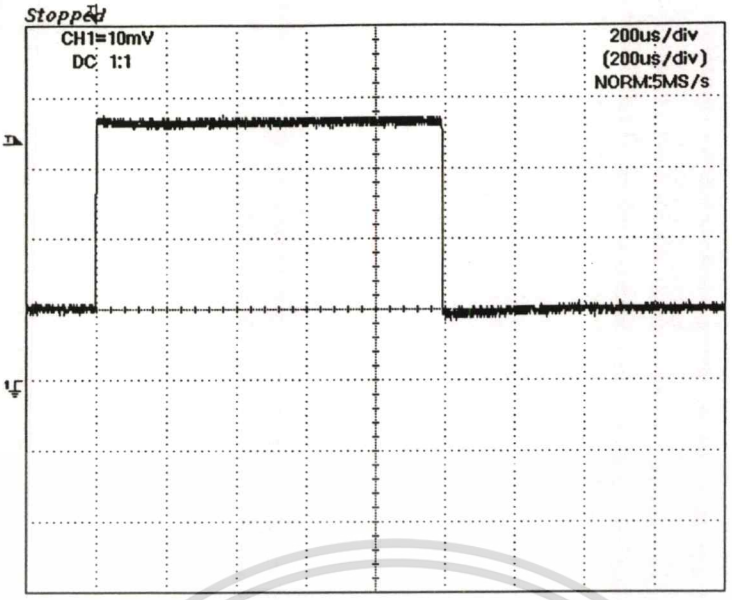
$$a_{H0} = \frac{\alpha w_{clz}}{\beta}$$

Appendix E

Photo of Prototype Circuit



Prototype circuit of buck converter with 3 modes controller



Waveform of a step load current used in the experiment

Appendix F

List of publication

[1] P. Chrin, H. Hirata and C. Bunlaksananusorn , "Averaged Modeling and Simulation of DC-DC Converters using Simulink", ITC-CSCC2006, pp 157-160, July 2006.

[2] P. Chrin and C. Bunlaksananusorn , "Large-Signal Average Modeling and Simulation of DC-DC Converters with SIMULINK", PCC '07, pp 27-32, April 2007.

AVERAGED MODELLING AND SIMULATION OF DC-DC CONVERTERS USING SIMULINK

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ABSTRACT

This paper presents averaged modelling and simulation of DC-DC converters using SIMULINK. The modelling is illustrated with a buck converter, where nonlinear averaged models of its power and control stages are developed. The closed loop model formed by feedback connection of the power and control stages can predict, with good accuracy, regulation characteristics of the converter under large-signal condition. This claim is supported by experimental results.

Keywords: DC-DC converters, Modelling, Simulation

1. INTRODUCTION

Modelling and simulation play a crucial role in the design process of DC-DC converters. They allow the converter performance to be evaluated before the prototype circuit is built. Hence, design flaws, if occurred, can be detected and corrected at the early stages in the design process, leading to the cost saving. Modelling and simulation of DC-DC converters have recently been a topic of intense research [1]. Of particular interest is the averaged modelling and simulation, the field which is interested in the averaged behaviour of the converters, ignoring the detailed switching ripple. The averaged simulation yields a much faster computer run time than the detailed simulation; thus it is often used to evaluate overall dynamic performance of the converters. In the past, the averaged simulation is mostly performed by SPICE [2]. The drawback of using SPICE is that the model to be simulated must be translated into an equivalent circuit, which can be very abstract and difficult if the model is a complicated equation. Recently, Forsyth et. al. [3] use SIMULINK to model and simulate a DC-DC converter as it can handle the mathematical equation better than SPICE. However, the authors use linearised models for the converter's control circuits and this has raised the question of validity of the model in predicting the converter performance under large-signal condition.

This paper extends the work in [3] by using the nonlinear model for the control circuits, thus making it suitable for simulation under the large-signal condition. The paper is organised as follows. In section 2, the nonlinear averaged model of the buck conveter's power and control stages are described. The closed loop SIMULINK models are presented in section 3, along with the results. Finally, a conclusion is given in section 4.

2. MODELLING OF DC-DC CONVERTERS

2.1 Power Stage

A buck converter's power stage is shown in Fig. 1. The power MOSFET is operated as an electronic switch and turned on/off by a constant-frequency Pulse-Width-Modulated (PWM) signal from the control circuit. In the figure, r_c is the Equivalent Series Resistance (ESR) of the capacitor, R is the standing load, and the current source, I_z, represents the additional load drawn from the converter. In Continuous Conduction Mode (CCM) where the inductor current flows continuously over one switching period, the converter exhibits two circuit states as shown in Fig. 2. During the MOSFET turn-on interval (Fig. 2(a)) the inductor is charged and its current increases linearly. During the MOSFET turn-off interval (Fig. 2(b)), the inductor is discharged and its current decreases linearly. The relationship between input voltage V_{in} and output voltage V is given by

$$V = dV_{in} \quad (1)$$

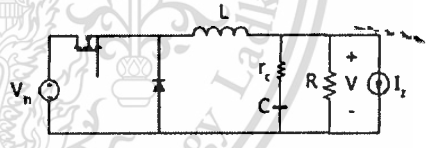

Fig.1: Buck Converter

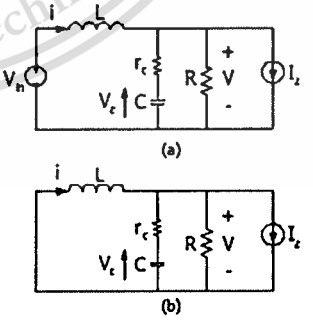

Fig.2: Buck Converter when (a) MOSFET turns on (b) MOSFET turns off

where d is a duty ratio of the MOSFET, which has a value between zero and one. Hence, the output voltage of the buck converter is always lower than the input voltage.

From Fig. 2., state-space equations for each circuit configuration can be written as given by (2) and (3).

$$\begin{bmatrix} \dot{i} \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} \frac{-Rr_c}{L(R+r_c)} & \frac{-R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & \frac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{Rr_c}{L(R+r_c)} \\ 0 & \frac{-R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} \dot{i} \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} \frac{-Rr_c}{L(R+r_c)} & \frac{-R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & \frac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & \frac{Rr_c}{L(R+r_c)} \\ 0 & \frac{-R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \quad (3)$$

The inductor current, i, and capacitor voltage, v_c, are state variables. The input voltage, V_{in}, and load current, I_z, are the system's input, while the system's output is the output voltage, V. The averaged state-space equation of the buck converter is obtained by weight average of (2) and (3) by the duty ratio and expressed in a general form by [4]

$$\dot{x} = Ax + Bu \quad (4)$$

where $x = \begin{bmatrix} i \\ v_c \end{bmatrix}$ is a state vector, $u = \begin{bmatrix} V_{in} \\ I_z \end{bmatrix}$ is an input vector, $A = dA_{on} + (1-d)A_{off}$, and $B = dB_{on} + (1-d)B_{off}$. A_{on}, B_{on} and A_{off}, B_{off} are the A and B matrices of (2) and (3) respectively. Thus, the averaged state-space model of the buck converter is given by

$$\begin{bmatrix} \dot{i} \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} \frac{-Rr_c}{L(R+r_c)} & \frac{-R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & \frac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{d}{L} & \frac{Rr_c}{L(R+r_c)} \\ 0 & \frac{-R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \quad (5)$$

Note that (5) is a nonlinear equation because it exists the product dV_{in}, where both are independent variables.

2.2 Control Stage

2.2.1 Voltage-Mode Control

The buck converter with voltage-mode control is shown in Fig. 3. The output voltage, V, of the converter is fed back and compared with the reference voltage, V_{ref}. The difference between the two voltages, namely the error voltage, is passed to the controller, H(s). The controller generates the control voltage, V_c, which is then compared with the sawtooth voltage to produce a PWM signal, d, to switch the MOSFET. The ratio of d and V_c, which defines the PWM modulator gain, is given by [3]

$$\frac{d}{V_c} = \frac{1}{V_p} \quad (6)$$

where V_p is the amplitude of the sawtooth voltage.

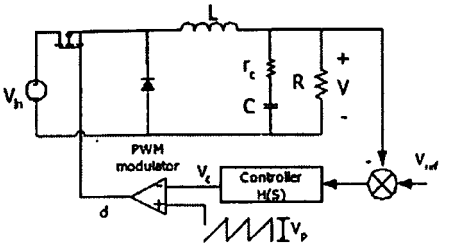

Fig.3: Buck Converter with Voltage-Mode Control

There are several types of controller that can be used with the buck converter. In this work, the controller depicted in Fig. 4, which has two poles and two zeros, is chosen to compensate the dominant second-order characteristics due to L and C of the buck converter. The controller's transfer function is expressed as

$$H(s) = \frac{V_c}{V} = K\frac{(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} \quad (7)$$

where $K = R_3/(R_1+R_2)$, $\omega_{z1} = 1/R_4C_2$, $\omega_{z2} = 1/R_2C_1$, $\omega_{p1} = 1/(R_3+R_4)C_2$, and $\omega_{p2} = (R_1+R_2)/R_1R_2C_2$.

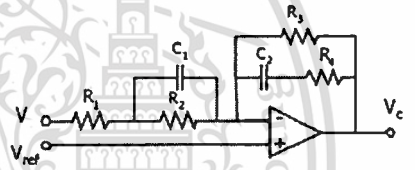

Fig.4: Controller for Voltage-Mode Control

2.2.2 Current-Mode Control

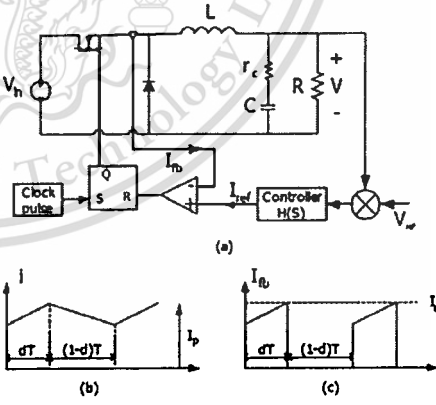

Fig.5: Buck Converter with Current-Mode Control

The buck converter with current-mode control is shown in Fig. 5. Its operation is as follows. At the beginning of a switching cycle, the clock signal sets the flip-flop (Q=1),

turning on the MOSFET. The MOSFET's current, which is equal to the inductor current during this interval, increases linearly. This current is sensed and compared with the control signal I_{ref} generated by the controller. When the sensed current, I_{fb}, is slightly greater than I_{ref}, The comparator's output goes high and resets the flip-flop (Q=0), thereby turning off the MOSFET. The MOSFET will be turned on again by the next clock signal and the same mechanism repeated.

By considering the inductor current waveform under steady-state condition in Fig. 5(b), the averaged inductor current, I, is determined to be

$$I = I_p - \frac{(V_{in} - V)dT}{2L} \quad (8)$$

where I_p is a peak inductor current and T is a switching period. The current-mode control waveform in Fig. 5(c) gives:

$$I_{fb} = R_s I_p = I_{ref} \quad (9)$$

where R_s is the current feedback gain. Substituting (9) into (8) and solving for d gives

$$d = \frac{2L}{(V_{in} - V)T}\left(\frac{I_{ref}}{R_s} - I\right) \quad (10)$$

In current-mode control, the inductor current is controlled and therefore is no longer an independent variable. Because of this, the buck converter with current-mode control exhibits the characteristics of a first-order system, i.e. its dynamic is dominated by C. As a result, the controller H(s) used in Fig. 5(a) is simpler than that used in voltage-mode control. The PI controller shown in Fig. 6 is, hence, chosen for this purpose. The integral action will help enhance output voltage regulation, while the proportional gain can be optimise to give the desirable response time. The transfer function of the PI controller is given by

$$H(s) = \frac{V_c}{V} = \frac{K(s + \omega_z)}{s} \quad (11)$$

where $K = R_2/R_1$, $\omega_z = 1/R_2C_1$

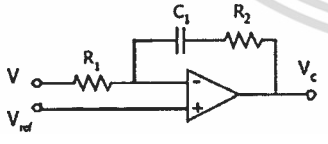

Fig.6: Controller for Current-Mode Control

3. SIMULINK MODELS AND RESULTS

A SIMULINK model of the buck converter with voltage-mode control is shown in Fig. 7. The power stage's averaged equation in (5) is inputted using the standard

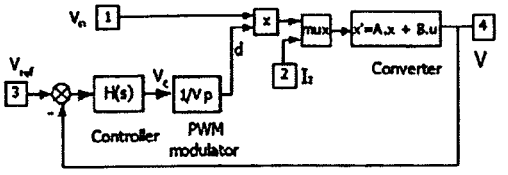

Fig.7: SIMULINK Model of Voltage-Mode Control

Table 1: Converter Parameters

Parameters	Values
V_{in}	24V
V	5V
R	5Ω
L	55μH
C	200μF
r_c	0.095Ω

state-space format in SIMULINK, with parameters of the converter listed in Table 1. The switching frequency is fixed at 100kHz (T=10μs). The PWM modulator in (6) is represented by the gain block $1/V_p$, where V_p = 1.8V. The multiplier block is used to form the product dV_{in}. The multiplexer (mux) block combines dV_{in} and I_z to be the input vector of the system. The controller, H(s), in (7) has been designed to ensure system stability and good transient response. The design yields C_1=C_2=0.22uF, R_1=120Ω, R_2=R_3=560Ω, and R_3=500kΩ. Thus, the controller inputted to SIMULINK for voltage-mode control is

$$H(s) = 735.3\frac{(1+1.23\times10^{-4}s)(1+1.23\times10^{-4}s)}{(1+0.11s)(1+2.17\times10^{-5}s)}. \quad (12)$$

The output voltage response of the model in Fig. 7, subjected to a step load current of 3A (i.e. I_z suddenly increases from 0 to 3A), is simulated and the result given in Fig. 9(a). The settling time and maximum voltage drop are about 150μs and 0.28V respectively. This simulated result corresponds well with the experimental result in Fig. 9(b), which is recorded from the prototype converter subjected to the same loading condition.

A SIMULINK model of the buck converter with current-mode control is shown in Fig. 8. Basic math operators and gain blocks are arranged to generate d according to (10). The demultiplexer (demux) block is used to separate the inductor current from the output voltage in the output vector, so that both variables can be fed back independently. The converter has the same circuit parameters as listed in Table 1 and the current feed back gain R_s is 1.71Ω. The PI controller in (11) is again designed to ensure system stabilty and good transient response. The design yields C_1=270pF, R_1=4.7kΩ and R_2=100kΩ. Thus, the controller inputted to SIMULINK for current-mode control is

$$H(s) = \frac{21.27(s + 37.04\times10^3)}{s}. \quad (13)$$

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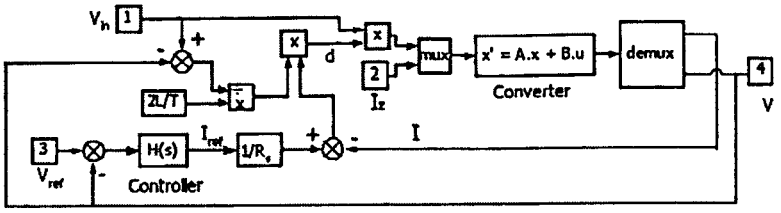
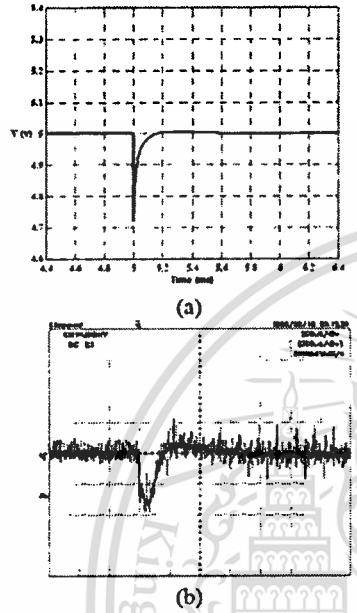


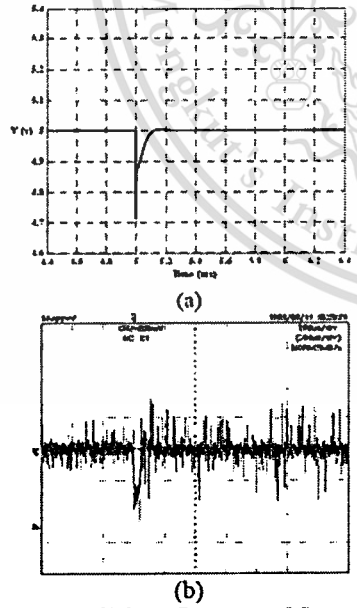
Fig.8: SIMULINK Model of Current-Mode Control



(a)

(b)

Fig.9: Output Voltage Response of Voltage-Mode Control (a) Simulated Result (b) Experimental Result



(a)

(b)

Fig.10: Output Voltage Response of Current-Mode Control (a) Simulated Result (b) Experimental Result

The simulated output voltage response of the model in Fig. 8, subjected to a step load current of 3A, is given in Fig. 10(a). From the response, the settling time of about 100μs and maximum voltage drop of 0.28V can be observed. This simulated result generally with the experimental result shown in Fig. 10(b), which is recorded from the prototype converter subjected to the same loading condition.

4. CONCLUSION

The averaged nonlinear models of a buck converter with voltage-mode control and current-mode control have been implemented in SIMULINK. The models can predict the dynamic of the converter under large-signal transient, with good accuracy, as witnessed by good agreement between simulated and experimental results. The results also show that current-mode control performance is superior to that of voltage-mode control, though it uses a simpler controller. The presented technique can be extended to other types of DC-DC converters, with only modification to the power stage model.

5. REFERENCES

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Large-Signal Average Modeling and Simulation of DC-DC Converters with SIMULINK

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***Abstract*—In this paper, modeling and simulation of DC-DC converters under SIMULINK environment is presented. The modeling is performed with a buck converter, employing three different control schemes: voltage-mode control, current-mode control, and average current-mode control. The resulted models are a nonlinear average model that can be used to simulate the converter performance under large-signal condition. Experiment on the prototype circuits subjected to a load current disturbance yields the results which are in reasonable agreement with their simulated counterparts, confirming the validity of the developed models.**

***Index Terms*— DC-DC converters, Modeling, Simulation.**

I. Introduction

Modern electronic equipment and systems are made up of high-density high-speed circuitry, which requires a low voltage and high current to function. For the proper operation of this type of loads, a power supply must be able to provide a constant voltage over a wide current range and possess excellent regulation characteristics in both steady and transient states. Modeling and simulation have played an important role in the design of modern DC-DC converters. They allow the converter performance to be evaluated before the actual circuit is built. Hence, design flaws, if any, can be detected and corrected at the early stages in the design process, leading to the increased productivity and cost saving.

Modeling and simulation of DC-DC converters have been a topic of intense research in the past decades [1]. In general, the converters can be modeled for switched simulation or average simulation. In the switched simulation, switching action of the converters is simulated and the results are waveforms with switching ripples resemble to those found in actual converters. On the other hands, the average simulation simulates only the average behaviour of the converters and therefore the results are the smooth continuous waveforms that represent an average value of the interested quantities. It is well known that the averaged simulation yields a much faster computer run time than the switched simulation. Hence, the averaged simulation is often used in the evaluation of overall dynamic performance of the converters. In the past, the average simulation is mostly performed by SPICE [2]. The drawback of using SPICE is that the model to be simulated must be translated into an equivalent circuit which can become difficult if the model is described by complicated equations. Although the newer versions of SPICE program provide commands to support mathematical based models, their capability is still somewhat limited. Recently, the paper [3] shows that SIMULINK [4] can be an effective tool to model and simulate DC-DC converters. However, the authors use a linearised model for the converter circuits and this has raised the question of validity of the model in predicting the converter performance under a large-signal condition.

To address such the drawback, this paper presents large-signal average modeling and simulation of DC-DC converters with SIMULINK. It extends the work in [3] by using a nonlinear model for both power and control stages of the converter, thus making the resulted models suitable for simulation under large-signal condition.

II. Modeling of DC-DC Converters

Nonlinear average models of a buck converter and its three output voltage control schemes are developed as follows

A. Buck Power Stage

A buck converter is shown in Fig. 1. In Continuous Conduction Mode (CCM) where the inductor current flows continuously over one switching period, the converter exhibits two circuit states. The first state is when the MOSFET is turned on (Fig. 2(a)). The second state is when the MOSFET is turned off (Fig. 2(b)). State-space equations for each circuit configuration can be expressed by

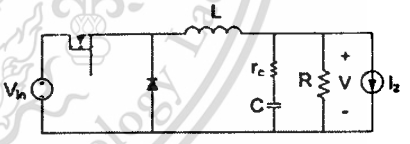

Fig. 1. Buck converter.

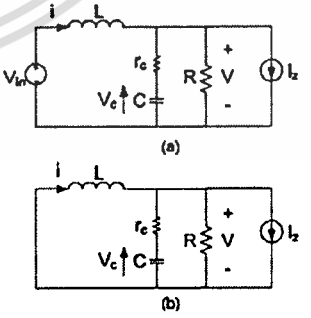

Fig. 2. Buck converter when MOSFET: (a) turns on and (b) turns off.

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$$\begin{bmatrix} \dot{i} \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} \frac{-Rr_c}{L(R+r_c)} & \frac{-R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & \frac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{Rr_c}{L(R+r_c)} \\ 0 & \frac{-R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} \dot{i} \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} \frac{-Rr_c}{L(R+r_c)} & \frac{-R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & \frac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & \frac{Rr_c}{L(R+r_c)} \\ 0 & \frac{-R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix} \quad (2)$$

where i and v_c are the inductor current and capacitor voltage respectively. The current source, I_z, models a load current disturbance and r_c is an Equivalent Series Resistance (ESR) of the output capacitor. The average state-space equations of the buck converter are obtained by weight average of (1) and (2) in accordance with [5] and is given by

$$\begin{bmatrix} \dot{i} \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} \frac{-Rr_c}{L(R+r_c)} & \frac{-R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & \frac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{d}{L} & \frac{Rr_c}{L(R+r_c)} \\ 0 & \frac{-R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_z \end{bmatrix}. \quad (3)$$

Note that (3) is a nonlinear equation because it contains the product dV_{in}, where d and V_{in} are independent variables.

B. Voltage-Mode Control (VMC)

A VMC scheme is shown in Fig. 3. The output voltage, V, of the converter is fed back and compared with the reference voltage, V_{ref}. The difference between the two voltages, namely the error voltage, is processed by the controller, H(s). The controller generates the control voltage, V_c, which is then compared with the sawtooth voltage to produce a PWM signal, d, to switch the MOSFET. The ratio of d and V_c, which defines the PWM modulator gain, is given by [3]

$$\frac{d}{V_c} = \frac{1}{V_p} \quad (4)$$

where V_p is the amplitude of the sawtooth voltage.

A controller depicted in Fig. 4 is chosen to compensate the dominant second-order characteristics of the buck converter. The controller consists of two poles (ω_{p1}, ω_{p2}) and two zeros (ω_{z1}, ω_{z2}) as expressed by the transfer function

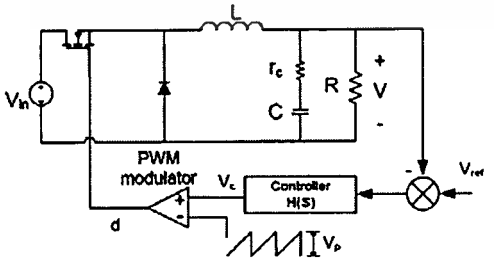

Fig. 3. Buck converter with VMC.

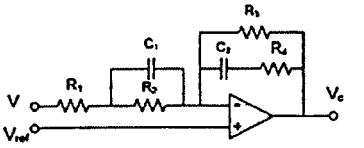

Fig. 4. Two-pole two-zero controller.

$$H(s) = \frac{V_c}{V} = K \frac{(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} \quad (5)$$

where $K = R_3/(R_1+R_2)$, $\omega_{z1} = 1/R_4C_2$, $\omega_{z2} = 1/R_2C_1$, $\omega_{p1} = 1/(R_3+R_4)C_2$, and $\omega_{p2} = (R_1+R_2)/R_1R_2C_2$. In the controller design, the first pole, ω_{p1}, is usually placed at low frequency to boost a DC gain of the system, the second pole, ω_{p2}, placed to cancel the zero due to the ESR of the converter's output capacitor, and the two zeros, ω_{z1} and ω_{z2}, placed to cancel the double poles of the converter's L-C filter.

C. Current-Mode Control (CMC)

A CMC scheme is shown in Fig. 5. At the beginning of a switching cycle, the clock signal sets the flip-flop (Q=1), turning on the MOSFET switch. The switch current, which is equal to the inductor current during this interval, increases linearly. This current is sensed as I_{fb} and compared with the control signal I_{ref} from the controller. When I_{fb}, is slightly greater than I_{ref}, the output of the comparator goes high and resets the flip-flop (Q=0), thereby turning off the MOSFET. The MOSFET will be turned on again by the next clock signal and the same process repeated.

By considering the inductor current waveform under steady-state condition in Fig. 5(b), the average inductor current, I, can be determined as

$$I = I_p - \frac{(V_{in} - V)dT}{2L} \quad (6)$$

where I_p is a peak inductor current and T is a switching period. The switch current waveform in Fig. 5(c) establishes the relationship between I_p and I_{ref} that:

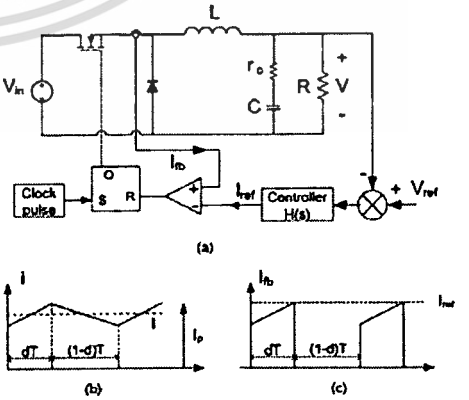

Fig. 5. (a) Buck converter with CMC; (b) Inductor current waveform; (c) Switch current waveform.

$$I_{fb} = R_s I_p = I_{ref} \quad (7)$$

where R_s is a current sensing gain. Substitution of (7) into (6) yields

$$d = \frac{2L}{(V_{in} - V)T}\left(\frac{I_{ref}}{R_s} - I\right). \quad (8)$$

In CMC, the inductor current is controlled and therefore is no longer an independent variable. Because of this, the current-mode controlled buck converter exhibits the characteristics of a first-order system, i.e. its dynamic is dominated by the converter's output capacitor. A Proportional-Integral (PI) controller shown in Fig. 6 is selected for the CMC buck converter in Fig. 5. It has one pole at origin, which represents an integrator, and one zero (ω_z). The PI controller's transfer function is given by

$$H(s) = \frac{V_c}{V} = \frac{K(s + \omega_z)}{s} \quad (9)$$

where $K = R_2/R_1$, $\omega_z = 1/R_2C_1$. The pole at the origin increases a DC gain of the system. In effect, this integrator helps improve output voltage regulation of the converter. The zero, ω_z, can be placed to result in the desired bandwidth and therefore the desired response time.

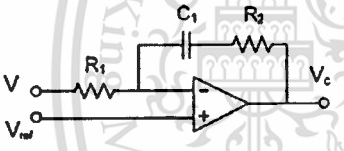

Fig. 6. Proportional-Integral (PI) controller.

D. Average Current-Mode Control (ACMC)

An ACMC scheme is shown in Fig. 7. The voltage controller, H(s), operates in a similar manner to the controller of the VMC, yielding the control signal V_c. The inductor current is sensed by the resistor R_s and multiplied by a gain A_c to give the sensed current signal, $V_s = iA_cR_s$. The difference between V_s and V_c is processed by the current controller. The resulting signal, V_{ci}, is then compared with the sawtooth voltage to produce a PWM signal, d, to switch the MOSFET.

When the output voltage, V, deviates from V_{ref}, the control signal, V_c, and the duty ratio, d, will change.

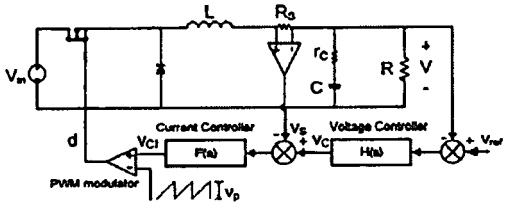

Fig. 7. Buck converter with ACMC.

The change in d results in the adjustment of the average inductor current and output voltage. At a new steady-state condition, the average inductor current will be at the value sufficient to maintain the constant output voltage. Hence, in ACMC the average current is controlled to regulate the output voltage. From Fig. 7, the duty ratio is expressed as

$$d = \frac{1}{V_p}\left[F(s)\left\{H(s)(V_{ref} - V) - V_s\right\}\right]. \quad (10)$$

A two-pole one-zero compensation circuit shown in Fig. 8 is selected for both the voltage and current controllers of the ACMC. Its transfer function is given by

$$H(s) = K\frac{\left(1 + \frac{s}{\omega_{z1}}\right)}{s\left(1 + \frac{s}{\omega_{p2}}\right)} \quad (11)$$

where $K = 1/R_1(C_1+C_2)$, $\omega_{z1} = 1/R_2C_2$, and $\omega_{p2} = (C_1+C_2)/R_2C_1C_2$. The ACMC consists of a current and voltage loops. The integrator is essential particularly for the current loop, since the average inductor current (V_s) must closely track its reference value (V_c). The zero, ω_{z1}, is placed to give the desired bandwidth in the respective loops. The current loop is a fast acting loop and must have a higher bandwidth than the voltage loop. In both loops, the second pole, ω_{p2}, is usually placed to yield the loop-gain attenuation at high frequency to suppress switching noises.

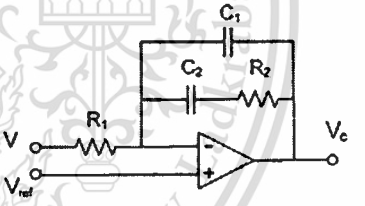

Fig. 8. Two-pole one-zero controller.

III. Simulink Models and Results

In this section, SIMULINK models of a buck converter employing VMC, CMC and ACMC are developed. To check their validity in large-signal simulation, the models are simulated and the results compared with the experimental results from the prototype converters. Table I lists circuit parameters of the prototype buck converters, which are also used in the simulation. The VMC and CMC prototypes have the same power circuit parameters and operate at the same input and output voltages, i.e. V_{in}=24V and V=5V. Their control is implemented by the IC UC3825 [6], which can be configured to work in either VMC or CMC. The ACMC prototype has been designed to operate at V_{in}=5V and V=2V. It uses the IC UC3886 [7] to implement control functions. Due to the different operating voltages, the circuit parameters of the ACMC prototype differ from its VMC and CMC counterparts.

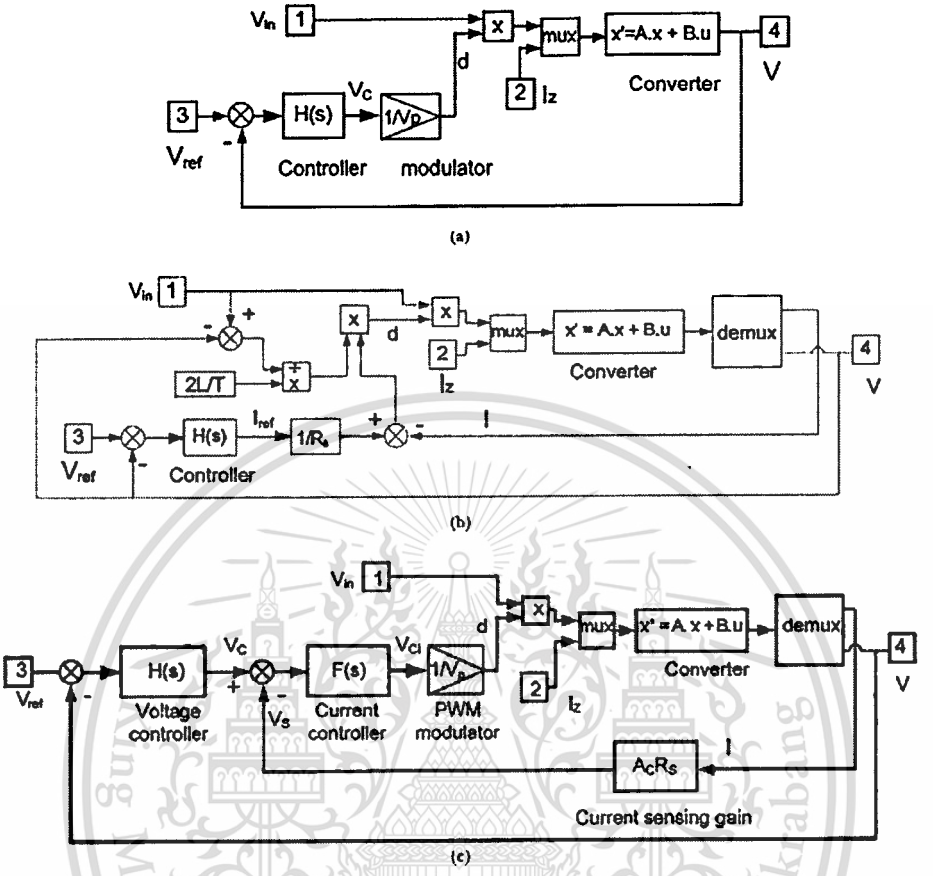

Fig. 9 SIMULINK models of a buck converter with: (a) VMC, (b) CMC, and (c) ACMC.

TABLE I
CIRCUIT PARAMETERS OF PROTOTYPE BUCK CONVERTER

Parameters	VMC and CMC	ACMC
V_{in}	24V	5V
V	5V	2V
R	5Ω	2 Ω
L	55μH	45μH
C	200μF	1200μF
r_c	0.095Ω	0.025Ω
T = 1/f	10μs	10μs

A. SIMULINK Model of VMC Buck Converter

A SIMULINK model of the buck converter with VMC is shown in Fig. 9(a). The state-space average equations in (3) are entered to SIMULINK through its standard state-space format. The PWM modulator gain in (4) is represented by the gain block $1/V_p$, where V_p=1.8V for the IC UC3825. The multiplier block is used to form the product dV_{in}. The multiplexer (mux) block combines dV_{in} and I_z to be the input vector of the system. The controller, H(s), in (5) has been appropriately designed to ensure system stability and good transient response. The design yields the following component values: C_1=C_2=0.22uF, R_1=120Ω, R_2=R_4=560Ω, and R_3=500kΩ. Substitution of these component values into (5) gives the controller transfer function,

$$H(s) = 735.3\frac{(1+1.23x10^{-4}s)(1+1.23x10^{-4}s)}{(1+0.11s)(1+2.17x10^{-5}s)}. \qquad (12)$$

Equation (12) is entered to SIMULINK through the standard transfer function format.

The output voltage response of the VMC model in Fig. 9(a) subjected to a step load current of 3A (i.e. I_z suddenly increases from 0 to 3A) is simulated, with the result given in Fig. 10(a). The settling time and maximum voltage drop are about 150μs and 0.28V respectively. This simulated result agrees reasonably well with the experimental result in Fig. 10(b), which was recorded from the prototype VMC buck converter under the same operating condition.

B. SIMULINK Model of CMC Buck Converter

A SIMULINK model of the buck converter with CMC is shown in Fig. 9(b). Basic mathematical operators and gain blocks are put together to create the duty ratio equation as described by (8). The demultiplexer (demux) block is used to separate the inductor current from the

output voltage in the output vector, so that both variables can be fed back independently. As in VMC, the power circuit is modeled by the average state-space equation in (3), using the circuit parameters listed in Table I. The current feed back gain, R_s, is 1.71Ω. The PI controller in (9) is designed to ensure system stability and good transient response. The design yields C_1=270pF, R_1=4.7kΩ and R_2=100kΩ. Substitution of these component values into (9) gives the controller transfer function,

$$H(s)=\frac{21.27(s+37.04x10^3)}{s}. \quad (13)$$

The simulated output voltage response of the CMC model in Fig. 9(b) subjected to a step load current of 3A is given in Fig. 11(a). From the response, the settling time of about 100μs and maximum voltage drop of 0.28V can be observed. This simulated result corresponds with the experimental result shown in Fig. 11(b).

C. SIMULINK Model of ACMC Buck Converter

A SIMULINK model of the buck converter with ACMC is shown in Fig. 9(c). The inductor current and output voltage in the output vector are separated by the demux block and used for current and voltage feedback respectively. The way these two feedback loops are connected apparently represents the duty ratio equation in (9). The current sensing gain (A_cR_s) is 0.075 and V_p=2.8V for the IC UC3886. The current controller has been designed to give the current loop bandwidth of 10kHz, resulting in R_1 = 560Ω, R_2 = 10kΩ, C_1 = 500pF, and C_2 = 22nF, and the voltage controller the voltage loop bandwidth of 5kHz, resulting in R_1 = 3.9kΩ, R_2 = 10kΩ, C_1 = 500pF, and C_2 = 22nF. Therefore, transfer functions of the current and voltage controllers used in the simulation are

$$F(s)=\frac{7.94x10^4(1+2.23x10^{-4}s)}{s(1+4.89x10^{-6}s)}, \quad (14)$$

$$H(s)=\frac{1.14x10^4(1+2.12x10^{-4}s)}{s(1+4.89x10^{-6}s)}. \quad (15)$$

The simulated output voltage response of the ACMC model in Fig. 9(c) subjected to a step load current of 3A is given in Fig. 12(a). The response exhibits the settling time of 800μs and maximum voltage drop of 70mV. This simulated result closely resembles its experimental counterpart in Fig. 12(b).

IV. Conclusions

In this paper, the large-signal average models of a buck converter with VMC, CMC, and ACMC have been presented. Though the controllers used are linear (equations (12) to (15)), the models in Fig. 9 nevertheless are nonlinear because they constitute the nonlinear power stage (equation (3)) and control laws (equations (8), (10)). As seen in Figs. 10 to 12, these average models can predict with good accuracy the dynamic performance of the converter under the step-load disturbance, validating their effectiveness in large-signal simulation. When suitably applied, the developed models may be used to facilitate the design of modern DC-DC converter modules.

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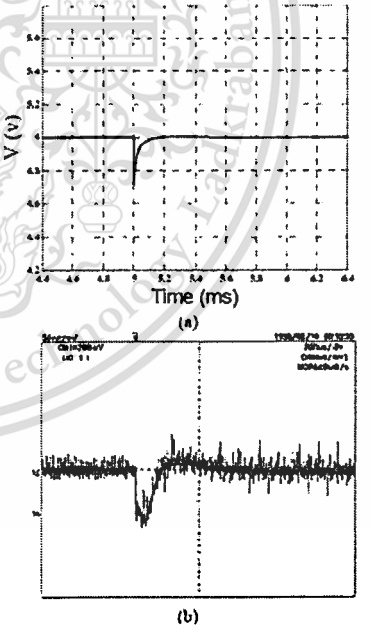

Fig. 10. Output voltage response of VMC buck converter due to a step load change of 3A: (a) simulated; (b) experimental.

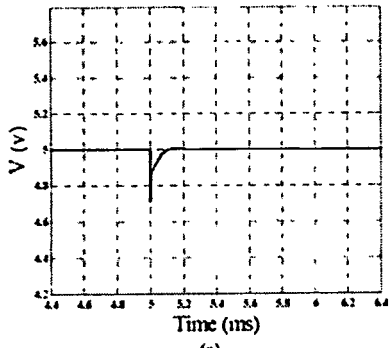

Fig. 11. Output voltage response of CMC buck couverter due to a step load change of 3A: (a) simulated: (b) experimental.

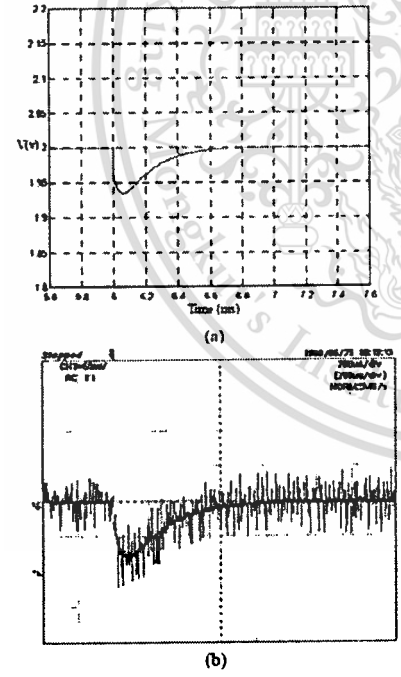

Fig. 12. Output voltage response of ACMC buck converter due to a step load change of 3A: (a) simulated: (b) experimental.