ON THE DESIGN AND IMPLEMENTATION OF INTEGRABLE CURRENT-MODE ANALOG SIGNAL PROCESSING CIRCUITS

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หัวข้อวิทยานิพนธ์	**การออกแบบและสร้างวงจรประมวลผลสัญญาณที่ทำงานในแบบสัญญาณกระแสแบบอนาลอกโดยหลักการวงจรรวม**
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บทคัดย่อ

วิทยานิพนธ์นี้เสนอการออกแบบและสร้างวงจรประมวลผลสัญญาณที่มีการทำงานของวงจรเป็นแบบสัญญาณกระแสแบบอนาลอกโดยใช้หลักการวงจรรวม โดยวงจรที่จะนำเสนอมีด้วยกัน 4 วงจรดังนี้

วงจรแรกคือ โครงข่ายแบบผ่านทุกความถี่ที่สามารถปรับค่าโพลความถี่ได้โดยวิธีทางอิเล็กทรอนิกส์ที่ทำงานในแบบสัญญาณกระแสโดยใช้ตัวเก็บประจุแบบต่อลงดิน วงจรประกอบด้วยวงจรสายพานกระแสที่ควบคุมด้วยกระแสสองวงจรและตัวเก็บประจุต่อลงดินหนึ่งตัว โครงข่ายที่นำเสนอมีสองแบบคือแบบเฟสนำหน้าและแบบเฟสล้าหลังโดยโครงข่ายทั้งสองมีการทำงานในโหมดกระแสและมีความต้านทานทางด้านเอ้าพุทสูงดังนั้นจึงทำให้สามารถนำมาใช้เป็นวงจรย่อยในระบบการประมวลผลสัญญาณที่ทำงานในโหมดกระแสได้เป็นอย่างดี ผลการจำลองการทำงานได้ใช้โปรแกรม PSPICE มาช่วยตรวจสอบการทำงานของวงจรร่วมกับทฤษฎี

วงจรที่สองคือ วงจรเรียงกระแสแบบเต็มคลื่นทำงานที่ความถี่สูงและมีความเที่ยงตรงสูงโดยใช้วงจรออปเปอเรชันแนลทรานส์คอนดักแตนซ์แอมปลิไฟล์แบบฟูลลี่ดิฟเฟอเรนเชียลอินพุทและเอ้าพุท โครงสร้างของวงจรประกอบด้วยวงจรแปลงแรงดันเป็นกระแส วงจรเรียงกระแสที่มีความเที่ยงตรงสูงและวงจรแปลงกระแสเป็นแรงดัน สัญญาณแรงดันอินพุทจะถูกแปลงเป็นสองสัญญาณกระแสที่มีความแตกต่างกันด้วยวงจรออปเปอเรชันแนลทรานส์คอนดักแตนซ์แอมปลิไฟล์แบบฟูลลี่ดิฟเฟอเรนเชียลอินพุทและเอ้าพุท สัญญาณกระแสจะถูกเรียงกระแสด้วยไดโอดที่สร้างจากมอสทรานซิสเตอร์และจะถูกแปลงเป็นแรงดันเอ้าพุทด้วยตัวต้านทานที่สร้างจากมอสทรานซิสเตอร์ วงจรที่นำเสนอจะถูกออกแบบด้วยซีมอสทั้งหมดจึงเหมาะสำหรับนำมาสร้างเป็นวงจรรวม การจำลองการทำงานได้แสดงถึงสมรรถนะของวงจรโดยสามารถเรียงกระแสได้ความถี่สูงถึง 200MHz และที่ Zero Crossing มีค่าแรงดัน 196μV

วงจรที่สามคือ วงจรคูณสัญญาณกระแสทำงานที่แรงดันต่ำ วงจรที่นำเสนอสร้างขึ้นจากวงจรสะท้อนกระแสอย่างง่ายซึ่งนำไปสู่ทำให้วงจรสามารถทำงานที่แรงดันต่ำได้ หลักการสร้างวงจรจะใช้วงจรกำลังสองและวงจรคัดลอกกระแส วงจรที่นำเสนอใช้ขนาดค่าความกว้างและความยาวของมอสทรานซิสเตอร์เท่ากันและไม่ใช้ตัวต้านทานจึงทำให้ง่ายต่อการนำไปสร้างเป็นวงจรรวม การจำลองการทำงานได้ใช้โปรแกรม PSPICE มาช่วยตรวจสอบคุณสมบัติของวงจร โดยได้ใช้โมเดลซีมอส 0.5μm ของ MIETEC ที่แหล่งจ่ายแรงดัน 1.5โวลท์ ผลการจำลองการทำงานแสดงช่วงปฏิบัติงานของอินพุทเท่ากับ ±10μA และมีช่วงความถี่ปฏิบัติงานสูงถึง 200MHz ผลการทดลองสามารถยืนยันการทำงานของวงจรที่นำเสนอ

วงจรสุดท้ายคือ วงจรคูณสัญญาณแบบหลายหน้าที่ทำงานในคลาส AB โดยวงจรที่นำเสนอสร้างขึ้นจากวงจรทรานส์ลิเนียร์แบบลูปคู่และวงจรสะท้อนกระแส วงจรที่นำเสนอมีคุณสมบัติที่โดดเด่นคือ มีอินพุทเป็นแบบอินพุทเดี่ยว วงจรทำงานในคลาส AB ทำให้ลดการใช้พลังงาน วงจรสามารถคูณสัญญาณแบบหลายหน้าที่ หมายความว่า วงจรสามารถคูณสัญญาณระหว่างกระแสกับกระแส คูณสัญญาณระหว่างแรงดันกับแรงดัน และสามารถคูณสัญญาณระหว่างกระแสกับสัญญาณแรงดันได้ในวงจรเดียวโดยไม่ต้องเปลี่ยนโครงสร้างของวงจร และวงจรมีเสถียรภาพทางอุณหภูมิดีมาก เมื่อกำหนดกระแสในสภาวะสงบของวงจรไว้ที่ 10μA ผลการจำลองการทำงานของวงจรด้วยโปรแกรม PSPICE แสดงค่าช่วงปฏิบัติงานของอินพุทเท่ากับ ±20μA ที่ -3dB วัดช่วงความถี่ปฏิบัติงานได้ 19MHz การใช้กำลังงานสูงสุด 0.46mW เมื่อกำหนดแหล่งจ่าย ±1.5โวลท์ และเสถียรภาพของวงจรทางด้านอุณหภูมิดีมาก การทำงานของวงจรคูณสัญญาณแบบหลายหน้าที่ที่นำเสนอสามารถยืนยันได้จากผลการทดลองเมื่อวงจรที่นำเสนอสร้างด้วยทรานซิสเตอร์ซีมอสเบอร์ MC14007

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ABSTRACT

This thesis presents four approaches for designing and implementing of integrable current-mode analog signal processing circuits. Four approaches to proposing in this thesis are described below:

First, a technique to realizing the two current-mode all-pass networks using two current-controlled conveyors (CCCIIs) and a grounded capacitor are presented. The current-mode all-pass network can be electronic tunability. This approach proposes both phase lead and phase lag all-pass networks. The circuit operates in current-mode with high output impedance; hence, it can be directly employed as a subsystem of monolithic circuit without additional matching circuits. PSPICE simulation results are carried out in order to verify the theory.

Second, a high frequency, high precision full-wave rectifier using a fully differential input and output operational transconductance amplifier (FDIO-OTA), which is very suitable for CMOS technology implementation is presented. The system comprises a voltage-to-current converter, precision full-wave rectifier and a current-to-voltage converter. A voltage input signal is converted into two symmetrical current signals by using a FDIO-OTA. Two current signals will be rectified by using MOS diodes and convert into output voltage by using a grounded MOS resistor. The circuit exhibits a very precise rectifier and very high operating frequency. The simulation results demonstrate the performance of the proposed circuit.

Third, a compact low-voltage current-mode four-quadrant CMOS multiplier circuit is proposed. The core of the circuit is the simple CMOS current mirrors, which leads to operate from low-voltage power supply. The realization method is based on the use of the square-difference technique. This current multiplier uses the dimension of all CMOS transistors are equal, without passive component and current source,

easily structure which is also very suitable for IC implementation. Simulated multiplier performance with a 0.5μm CMOS model using a 1.5V supply voltage demonstrate the input current range of this multiplier circuit is ±10μA and bandwidth of about 200MHz. The experimental results of proposed circuit confirm theoretical analysis are carried out.

Finally, a versatile class-AB CMOS four-quadrant analog multiplier circuit is presented. Three dual translinear loops and current mirrors are the basic building blocks in this realization scheme. The proposed multiplier is carried in current-mode, thus the circuit gives wide input range and wide-bandwidth response for a low consumption. The major advantages over the other analog multiplier are; this circuit has single ended inputs; the analog multiplier based on dual translinear loops operating in class-AB mode which make them interesting for low-voltage and low-power applications; and its output can be the product of two signal currents, the product of two signal voltages, or the product of a signal current and a signal voltage. The simulation results of proposed analog multiplier demonstrate a input current range is ±20μA, a -3dB bandwidth of about 19MHz, a maximum power consumption of about 0.46mW, and temperature compensated when two supply voltage of -1.5V and +1.5V and a quiescent current of 10μA in a 0.5μm CMOS model are obtained. Operation of proposed analog multiplier was also confirmed through an experiment using CMOS transistor array.

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CONTENTS

Pages

Thai abstract.....I

English abstract.....III

Acknowledgments.....V

Contents.....VI

Figure contents.....IX

Table contents.....XII

Chapter 1 Introduction.....1

1.1. Background.....1

1.2. Purposes of the study.....2

1.3. Thesis organization.....3

1.4. References.....4

Chapter 2 Device modeling.....5

2.1. Bipolar junction transistor.....5

2.1.1. BJT structure and operation.....5

2.1.2. BJT small signal modeling.....8

2.2. Metal oxide semiconductor.....11

2.2.1. MOS structure and operation.....11

2.2.2. BJT small signal modeling.....13

2.3. References.....15

Chapter 3 Capacitor-grounded current-mode all-pass networks using MO-CCCIIs.....16

3.1. Introduction.....16

3.2. Multi-output second generation current-controlled conveyor.....17

3.3. Proposed current-mode all-pass networks.....19

3.4. Performance analysis.....20

3.4.1. Tracking error effects.....21

3.4.2. High frequency limitation.....21

3.4.3. Sensitivity study.....22

CONTENTS

Pages

3.5. Simulation results.....23

3.6. Quadrature oscillator with all-pass network.....28

3.7. Conclusions.....32

3.8. References.....33

Chapter 4 High frequency and high precision CMOS full-wave rectifier.....35

4.1. Introduction.....35

4.2. Fully differential input and output operational transconductance amplifier.....38

4.3. Proposed full-wave rectifier circuit.....39

4.4. High frequency considered.....43

4.5. Simulation results.....44

4.6. Temperature considered.....48

4.7. Conclusions.....54

4.8. References.....54

Chapter 5 Low-voltage CMOS current multiplier.....56

5.1. Introduction.....56

5.2. Circuit descriptions.....57

5.4. Performance analysis.....63

5.4.1. Second-order effect.....63

5.4.1.1. Channel-length modulation.....64

5.4.1.2. Mobility degradation.....64

5.4.2. Mismatches analysis.....65

5.4.3. Frequency response analysis.....66

5.3. Results.....67

5.3.1. Simulation results.....67

5.3.2. Experimental results.....69

5.5. Conclusions.....72

5.6. References.....72

CONTENTS

Pages

Chapter 6 Versatile class-AB analog multiplier.....74

6.1. Introduction.....74

6.2. Circuit descriptions.....75

6.2.1. Class-AB CMOS squaring circuit.....75

6.2.2. Proposed versatile class-AB analog multiplier.....79

6.3. Performance analysis.....82

6.3.1. Mismatch and second-order effects.....82

6.3.2. Input range and input/output resistance.....84

6.3.3. Frequency response.....88

6.4. Simulation and experimental results.....90

6.4.1. Simulation results.....90

6.4.2. Experimental results.....95

6.5. Conclusions.....97

6.6. References.....98

Chapter 7 Conclusions and future researches.....101

7.1. Introduction.....101

7.2. Recommended future work.....101

Publications of the author.....103

About the author.....104

FIGURE OF CONTENTS

Figure **Pages**

2.1 (a) The layout, (b) the cross-sectional view, (c) the symbol of an NPN BJT, (d) the symbol of an PNP BJT.....5

2.2 A large-signal model for a BJT in the active region.....6

2.3 The small signal model of an active BJT.....9

2.4 (a) The layout and cross-section views of an NMOS transistor, (b) symbol of NMOS, (c) symbol of PMOS.....11

2.5 The small-signal model for a MOS transistor in active region.....13

2.6 The low-frequency, small-signal model.....13

3.1 MO-CCCII symbols.....17

3.2 The bipolar implementation.....18

3.3 The current all-pass network using two CCCIIs with a grounded capacitor: (a) phase shifts from +180° to 0, (b) phase shifts from 0 to -180°.....19

3.4 Equivalent circuit of CCCII.....22

3.5 Magnitude and phase characteristics of I_2/I_1 versus frequency using capacitor C_1=12nF and bias current I_{o2}=100μA of figure3.3(a).....23

3.6 Magnitude and phase characteristics of I_4/I_3 versus frequency using .....capacitor C_1=12nF and bias current I_{o4}=100μA of figure 3.3(b).....24

3.7 Time domain waveforms of the input and +90 degree-shifted output currents of figure 3.3(a).....24

3.8 Time domain waveforms of the input and -90 degree-shifted output currents of figure 3.3(b).....25

3.9 Current-tuning of corner frequency with bias current for C_1=12nF of figure 3.3(a).....25

3.10 Current-tuning of corner frequency with bias current for C_2=12nF of figure 3.3(b).....26

3.11 Current-tuning of corner frequency with bias current for C_1=12nF of figure 3.3(a).....26

3.12 Variation of THD with input current signal for I_{o2}=100μA of figure 3.3(a).....27

FIGURE CONTENTS

Figure **Pages**

3.13 Current-mode quadrature oscillator using current-mode all-pass network of figure 3.3(a) and lossless integrator.....28

3.14 Simulated output wave form of the current-mode quadrature oscillator.....29

3.15 Plots of oscillation frequencies versus bias current.....30

3.16 Plots of amplitudes of I_{out1} versus bias current.....30

3.17 Amplitude matching of the quadrature signals versus frequency.....31

3.18 Phase matching of the quadrature signals versus frequency.....31

4.1 Single ended OTA based half-wave rectifier.....37

4.2 (a) CMOS FDIO-OTA structure, (b) Symbol.....37

4.3 FDIO-OTA-based full-wave rectifier.....38

4.4 MOS diode: (a) Cross-section of MOS diode, (b) Symbol.....39

4.5 Complete circuits of proposed high frequency and high precision full-wave rectifier.....39

4.6 Cross-section of two diode-connected PMOS transistor:
(a) drain-gate-connected and bulk-source-connected,
(b) drain-source-connected and gate attached to ground.....41

4.7 Circuit model of non-ideal: (a) FDIO-OTA, (b) MOS diode.....43

4.8 Circuit model of non-ideal proposed full-wave rectifier.....44

4.9 Simulated results for DC transfer characteristic.....45

4.10 Simulated results for DC transfer characteristic at zero crossing regions.....45

4.11 Operation of the proposed full-wave rectifier at a frequency 1MHz.....46

4.12 Operation of the proposed full-wave rectifier at a frequency 50MHz.....46

4.13 Operation of the proposed full-wave rectifier at a frequency 100MHz.....47

4.14 Operation of the proposed full-wave rectifier at a frequency 200MHz.....47

4.15 Operation of the proposed full-wave rectifier of a frequency 1MHz at different temperature when CMOS diodes are replaced with Schottky diode: (a) full-wave output, (b) zero crossing region.....49

4.16 Operation of the proposed full-wave rectifier of a frequency 1MHz at different temperature when used CMOS diode: (a) full-wave output, (b) zero crossing region.....50

FIGURE CONTENTS

Figure **Pages**

4.17 Temperature compensated by using current biasing technique proposed by Hayatleh *et al.*[16].....51

4.18 Operation of the proposed full-wave rectifier of a frequency 100MHz at different temperature with temperature compensated: (a) full-wave output, (b) zero crossing regions.....52

4.19 Operation of the proposed full-wave rectifier of a frequency 100MHz at different temperature without temperature compensated: (a) full-wave output, (b) zero crossing regions.....53

4.20 Simulated for high-frequency response.....53

5.1 The squarer circuit.....60

5.2 The squarer and copy current circuit.....60

5.3 Proposed low-voltage current multiplier.....61

5.4 The circuit for cancel the constant current.....62

5.5 Simulated DC transfer characteristic.....67

5.6 Response characteristics: (a) frequency response, (b) phase response.....68

5.7 The simulated total harmonic distortion.....69

5.8 Block diagrams used for experimentation.....70

5.9 Measured frequency doublers with a 10kHz tringular wave inputs.....70

5.10 Measured output waveform of a 18kHz sinusoid and a 1kHz triangular wave.....71

6.1 Basic building blocks.....76

6.2 Squaring and copy current into a single circuit.....76

6.3 Proposed versatile class-AB analog multiplier 77

6.4 Linear MOS transistor.....81

6.5 (a) Class AB converter, (b) negative current converter, (c) positive current mirror.....88

6.6 Simulated DC transfer characteristics for two inputs are currents.....91

6.7 Simulated DC transfer characteristics for two input are voltages.....91

6.8 Simulated DC transfer characteristics for input are voltage and current.....92

6.9 Frequency and phase response characteristics for inputs are voltages.....92

FIGURE CONTENTS

Figure **Pages**

6.10 Frequency and phase response characteristics for inputs are currents.....93

6.11 Total harmonic distortions versus input current.....93

6.12 Total harmonic distortions versus input voltage.....94

6.13 Simulated DC transfer characteristic for I_Y=10μA
and temperature=50°C, 75°C and 100°C.....94

6.14 Measured frequency doubler with a 10kHz sine wave inputs.
Lower trace: 400mV_{P-P} sine signal of 10kHz (200mV/div),
Upper trace: output waveform (200mV/div), horizontal scale is 25μs/div.....96

6.15 Measured output waveform of a 50kHz sinusoid and a 3kHz triangular
wave. Lower trace: 400mV_{P-P} sinusoidal signal of 3kHz (500mV/div),
Upper trace: output waveform (500mV/div), Horizontal scale is 100μs/div.....96

6.16 Measured output spectrum of analog multiplier, for the case in which
a 400mV_{P-P} sine signal of 50kHz and a 400mV DC voltage are applied
with V_X and V_Y, respectively [horizontal scale is 100μs/div; vertical
scale is 10dBm].....97

TABLE CONTENTS

Table **Pages**

2.1 BJT parameters used in this thesis.....8

2.2 The parameter of 0.5μm CMOS used in this thesis.....12

5.1 Simulated result parameters of proposed CMOS current multiplier.....71

6.1 Functions for versatile analog multiplier.....82

6.2 MOS transistor sizes.....90

6.3 Simulated performance of proposed versatile analog multiplier.....98

CHAPTER 1
INTRODUCTION

In this chapter, the author present a brief historical overview of the motivation of voltage-mode and current-mode, the author discuss the advantage of current-mode circuit when it compared with voltage-mode circuit, next the author focus to the goad of this research and, finally, the detail of thesis is described.

1.1. Background

Since the introduction of integrated circuits, the operational amplifier has served as the basic building block in analogue circuit design. Since then, new integrated analogue circuit applications have emerged and the performance requirement for analogue circuit has changed. Voltage-mode operational amplifier circuits have limited bandwidth at high closed-loop gain due to the constant gain-bandwidth product. Furthermore, the limited slew-rate of the operational amplifier affects the large-signal, high frequency operation. When wide bandwidth, low power consumption and low voltage operation are needed simultaneously, the voltage-mode operational amplifier easily becomes too complex and has characteristics that are not needed, for example DC-accuracy. On other hand, circuit techniques used in radio frequency applications are usually too simple to reach the required accuracy. Therefore, there is growing need for new, low voltage analogue circuit technique.

At present current-mode circuits have been receiving significant attention because of their inherent wide bandwidths, greater linearity, wider dynamic range, simple circuitry and low power consumption [1]-[2]. For supposing mentioned above can be expanded as follow; when signals are widely distributed as voltages, the parasitic capacitances are charged and discharged with the full voltage swing, which limits speed but increases the power consumption of voltage-mode circuit. Current-mode circuit cannot avoid nodes with high voltage swing, either but these are usually local nodes with less parasitic capacitance. Therefore, it is possible to reach higher speed, wide bandwidth and low power consumption with current-mode techniques.

When the signal is conveyed as a current, the voltages in MOS transistor circuits are proportional to the square-root of signal (let saturation region operation is

assumed for the device). Similarly, in bipolar transistor circuits the voltages are proportional to the logarithm of the signal. Therefore, a compression of voltage signal swing and a reduction of supply voltage are possible. This reduction of supply voltage not affects the input signal swing when its input signal is current form; whereas if the circuit is voltage-mode, reduction of supply voltages is mean that reducing input signal swing. Thus, certain current-mode circuits, the circuits are utilized to reduce the supply voltage.

Current-mode techniques are characterized by signals as typically processed in the current domain. Current-mode circuits have some recognized advantages: firstly, they do not require a high voltage gain, so high performance amplifiers are not needed. Then, they do not need high precision passive components, so they can be designed almost entirely with transistors. This makes the current-mode circuits compatible with typical digital processes. Finally, they show high performance in terms of speed, bandwidth and accuracy. Therefore, at present, the current-mode circuits become primary importance in the design of modern integrated circuits, which are widely utilized in portable-system applications [3].

In the past, several circuits of the realization of current-mode signal processing uses CMOS technology [4]-[7] and bipolar technology through current conveyors [8]-[11] have been published. It maintains an inherent advantage of its excellent operation at high frequency, high accuracy and the ease manipulating current as a variable [1].

1.2. Purposes of the study

The purposes of this research are presented the design and implementation of integrable current-mode analog signal processing circuits. The analog circuits such as all-pass networks, a full-wave rectifier and analog multipliers are proposed. A more general objective of this research is the development of a design methodology of integrable current-mode analog signal processing. Some of the key results of this research are listed here:

(1) A simplified design technique has been developed for the design of current-mode all-pass networks. The circuit design uses two second-generation current controlled conveyors (CCCIIs) and a grounded capacitor. The proposed circuits operated in current-mode and high

output impedance. Thus, its can be directly employed as a subsystem of monolithic circuit. The use of a grounded capacitor and without resistor makes the proposed circuit ideal for integrated circuit implementation. PSPICE simulation results are incorporated to verify the theory.

(2) Designed a high frequency and high precision full-wave rectifier with a fully differential input and output operational transconductance amplifier (FDIO-OTA), MOS diodes and MOS resistor. The methodology used current-mode realization in order to achieve the high frequency and high precision of full-wave rectifier. The simulation results demonstrate the performance of the proposed circuit.

(3) Designed and implemented two four-quadrant analog multiplier circuits. The first circuit is presented a low-voltage and low-power current multiplier. The core of the circuit is the simple CMOS current mirrors, which leads to operated from low-voltage power supply. The second circuit presented a versatile class-AB analog multiplier. The major advantages of this approach are; its has single ended inputs; since its input is dual translinear loop operate in class-AB mode which make this multiplier configuration interesting for the low-power applications; current multiplying, voltage multiplying, or current and voltage multiplying can be obtained. The simulation and experimental results of proposed circuit confirm theoretical analysis is carried out.

1.3. Thesis organization

In chapter 2, the basic structure and principle of the bipolar junction transistors (BJTs) and metal oxide semiconductor (MOS) transistors are described. Current-mode all-pass networks using CCCIIs and a grounded capacitor are presented in chapter 3 including a discussion of circuit performance and simulation results. Chapter 4 describes the high frequency and high precision full-wave rectifier circuit. Two four-quadrant analog multiplier circuits are focused in chapter 5 and chapter 6. Finally, chapter 7 contains concluding remarks and recommendations for the future work.

1.4. References

1.4. References

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CHAPTER 2
DEVICE MODELING

This chapter serves as an introduction to a brief structure and operation of bipolar junction transistors (BJTs) and metal oxide semiconductor (MOS) transistors. The large-signal and small-signal models for intregrated-circuit devices are also analyze. Finally, PSPICE parameters for the bipolar process of ATT&T ALA400-CBICR and 0.5μm CMOS process obtained through MIETEC which used in this thesis are included in this chapter.

2.1. Bipolar junction transistor

2.1.1. BJT large-signal modeling

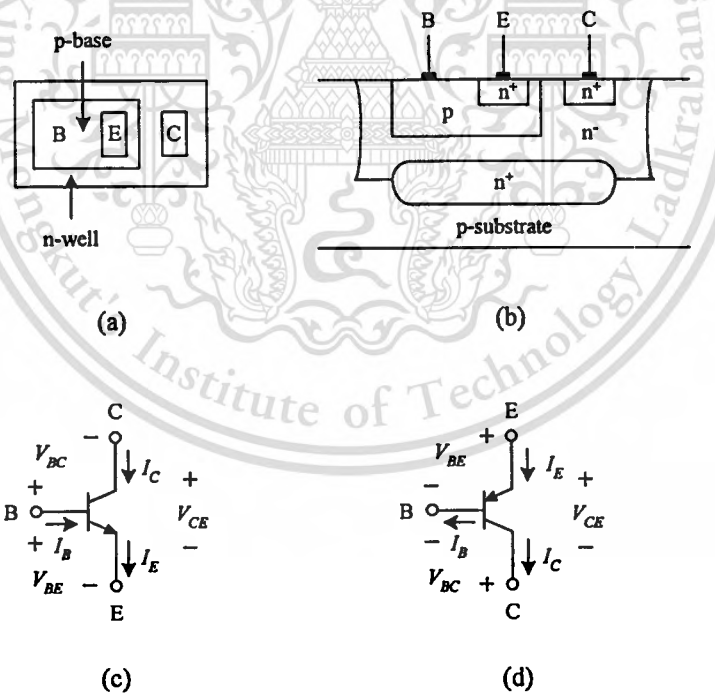

Figure 2.1 (a) The layout, (b) the cross-sectional view, (c) the symbol of an NPN BJT, (d) the symbol of an PNP BJT.

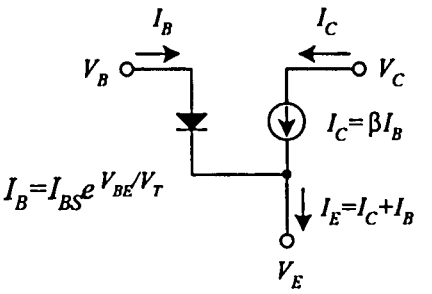

Figure 2.2 A large-signal model for a BJT in the active region.

A cross-sectional view of an NPN BJT with geometrical layout and the corresponding symbols for NPN and PNP is shown in figure 2.1. The expensive operation of the BJT can be explored in [1].

In this thesis, only active region will be discussed. The active region is a conducting BJT that has V_{CE} greater than $V_{CE\text{-}sat}$. Such a collector-emitter voltage is required to ensure that none of the holes from the base go to the collector. The collector current can be given [1]

$$I_C = I_{CS}e^{V_{BE}/V_T} \tag{2.1}$$

where I_{CS} is the scale current. Figure 2.2 shown a large-signal model of a BJT operating in the active region. When I_B is the base current, I_C is the collector current, I_E is the emitter current, V_{BE} is the base-emitter voltage, V_T is the thermal voltage, V_B is the base voltage, V_C is the collector voltage, V_E is the emitter voltage, β is the forward current gain, I_{BS} is the constant that is often referred to as the saturation current of the junction.

Since $I_B=I_C/\beta$ [1], the base current I_B can be expressed as

$$I_B = \frac{I_{CS}}{\beta}e^{V_{BE}/V_T} = I_{BS}e^{V_{BE}/V_T} \tag{2.2}$$

which is multiplying constant of $I_{CS}/\beta=I_{BS}$. Typical values of β are between 50 and 200.

Since $I_E=I_B+I_C$, it can be given as

$$I_E = I_{CS}\left(\frac{\beta+1}{\beta}\right)e^{V_{BE}/V_T} = I_{ES}e^{V_{BE}/V_T} \tag{2.3}$$

or equivalently

$$I_C = \alpha I_E \tag{2.4}$$

when I_{CS} and I_{ES} are the scale currents. The α has been defined as

$$\alpha = \frac{\beta}{\beta+1} \tag{2.5}$$

and for large values of β, it can be approximated as

$$\alpha \cong 1-\frac{1}{\beta} \cong 1. \tag{2.6}$$

If the effect of V_{CE} on I_C is included in the model, the current-controlled source, βI_B, should be replaced by a current source given by

$$I_C = \beta I_B\left(1+\frac{V_{CE}}{V_A}\right) \tag{2.7}$$

where V_A is the Early-voltage constant and V_{CE} is the collector-emitter voltage. This additional modeling of the finite output impedance is normally not done in large-signal analysis without the use of a computer due to its complexity.

For the parameters of BJT required in chapter 3 can be listed below [2]:

Table 2.1 BJT parameters used in this thesis.

NPN TRANSISTOR

NR100N-1X NPN TRANSISTOR

.MODEL NX1 NPN RB=524.6 IRB=0 RBM=25 RC=50 RE=1 IS=121E-18

EG=1.206 XTI=2 XTB=1.538 BF=137.5 IKF=6.974E-3 NF=1 VAF=159.4

ISE=36E-16 NE=1.713 BR=0.7258 IKR=2.198E-3 NR=1 VAR=10.73 ISC=0 NC=2

TF=0.425E-9 TR=0.425E-8 CJE=0.214E-12 VJE=0.5 MJE=0.28 CJC=0.983E-13

VJC=0.5 MJC=0.3 XCJC=0.034 CJS=0.913E-12 VJS=0.64 MJS=0.4 FC=0.5

PNP TRANSISTOR

PR100N-1X PNP TRANSISTOR

.MODEL PX1 NPN RB=327 IRB=0 RBM=24.55 RC=50 RE=3 IS=73.5E-18

EG=1.206 XTI=1.7 XTB=1.866 BF=110.0 IKF=2.359E-3 NF=1 VAF=51.8

ISE=25.1E-16 NE=1.650 BR=0.4745 IKR=6.478E-3 NR=1 VAR=9.96 ISC=0 NC=2

TF=0.610E-9 TR=0.610E-8 CJE=0.180E-12 VJE=0.5 MJE=0.28 CJC=0.164E-12

VJC=0.8 MJC=0.4 XCJC=0.037 CJS=1.03E-12 VJS=0.55 MJS=0.35 FC=0.5

2.1.2. BJT small signal modeling

The most commonly used small-signal model for a BJT is the hybrid-π model. The hybrid-π model of BJT in the active region is shown in figure 2.3. The transconductance g_m is perhaps the most important parameter of the small-signal model. The transconductance is the ratio of the small-signal collector current, i_C, to the small-signal base-emitter voltage V_{BE}. Thus, it can be expressed as

$$g_m = \frac{i_C}{V_{BE}} = \frac{\partial I_C}{\partial V_{BE}} \tag{2.8}$$

Recall that in the active region

$$I_C = I_{CS} e^{V_{BE}/V_T} \tag{2.9}$$

Then

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_{CS}}{V_T} e^{V_{BE}/V_T} \tag{2.10}$$

Using (2.9), again it can be obtained

$$g_m = \frac{I_C}{V_T} \tag{2.11}$$

where V_T is give by

$$V_T = \frac{kT}{q} \tag{2.12}$$

where k being Boltzmant's constant approximately 1.38×10^{-23} JK^{-1} and q being the charge of an electron equal 1.602×10^{-19}C. The V_T is approximately 26mV at temperature of T equal 300°K. Thus, the transconductance is proportional to the bias current of a BJT. In integrated circuit design, it is important that the transconductance remains temperature independent, so the bias currents are usually made proportional to absolute temperature (since V_T is proportional to absolute temperature).

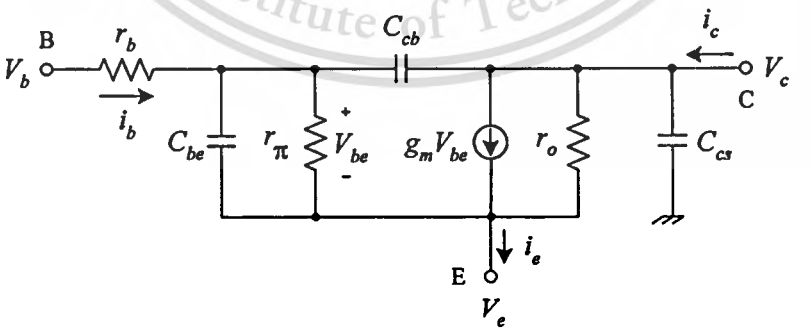

Figure 2.3 The small signal model of an active BJT.

The resistor π in figure 2.3 can be given [1]

$$r_\pi = \frac{\partial V_{BE}}{\partial I_B} \tag{2.13}$$

or

$$r_\pi = \frac{V_T}{I_B} \tag{2.14}$$

The finite base-emitter impedance r_π, which proportional to I_B is the advantage to chapter 3 for realizing the electronic tunable circuit.

The small-signal resistance r_O models the dependence of the collector current on the collector-emitter voltage. It can be given by [1]

$$r_O = \frac{V_A}{I_C} \tag{2.15}$$

where V_A called the Early voltage. Typical values of V_A for the integrated-circuit transistor are in the range 50V to 100V [1]. The resistor r_b models the resistance of the semiconductor material between the base contact and the effective base region due to the moderately lightly doped base P material. This resistor, although small can be important in limiting the speed of very-high-frequency low-gain BJT circuit and it a major source of noise.

The high frequency operation of a BJT is limited by the capacitances of the small signal model. The first capacitor is C_{be}, which is the sum of the depletion capacitance of the base-emitter junction and the diffusion capacitance. The second capacitor is C_{cb}, which is the depletion capacitance of the collector-base junction. The other capacitor is a large capacitor C_{cs}, which is the capacitance of the collector to substrate junction. Since this area is quite large. The C_{cs} is the depletion capacitance that results from this area, which much larger that either C_{cb} or C_{be}.

2.2. Metal oxide semiconductor

2.2.1. MOS large-signal modeling

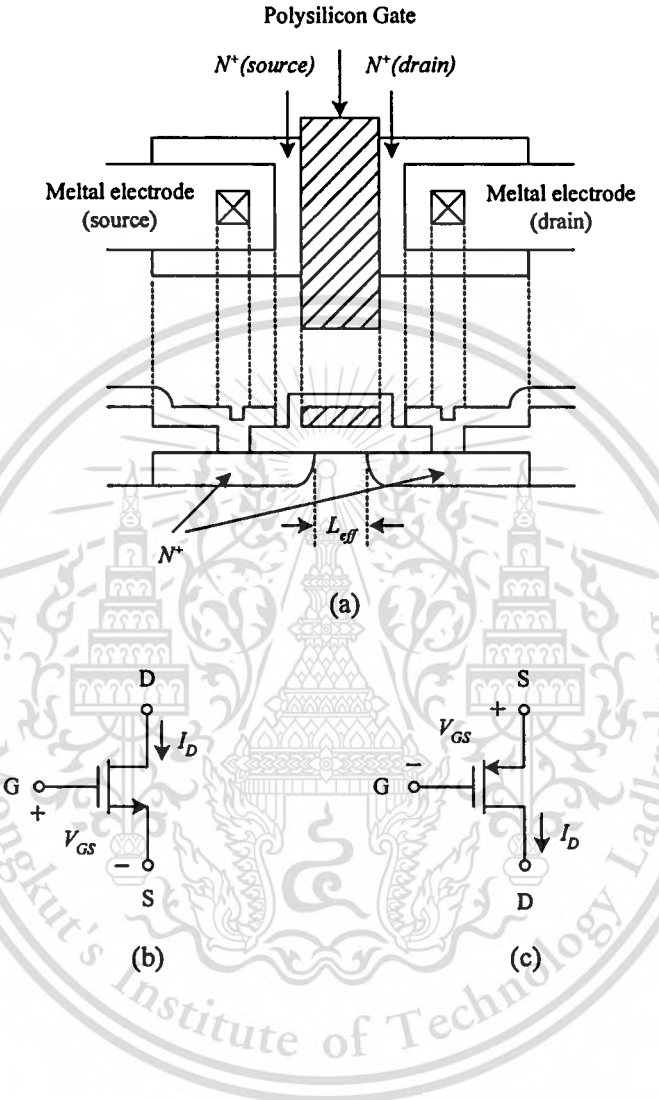

Figure 2.4 (a) Layout and cross-section views of an NMOS transistor, (b) symbol of NMOS and (c) symbol of PMOS.

The basic operation of MOS transistor was presented in [3]. Therefore, this thesis will refer only important equations which used to design and analysis the proposed circuits. Figure 2.4 shows the layout and cross-section views of an NMOS transistor and symbols of NMOS and PMOS used in this thesis. The MOS transistor uses the gate-source voltage (V_{GS}) controlling the drain-source current (I_D). The importance drain current equation of MOS transistor can be given by two equations [5]:

$$I_D = \mu_O C_{OX}\left(\frac{W}{L}\right)\left((V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right) \tag{2.16}$$

for operating in the triode region: $V_{DS}<V_{GS}-V_{TH}$, and

$$I_D = \frac{\mu_O C_{OX}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})^2 \tag{2.17}$$

for operating in saturation region: $V_{DS}>V_{GS}-V_{TH}$, and ignores the second-order effects such as the finite output impedance of the resistor.

For large-small signal model, the meaning of parameters is listed as follows: μ_O = mobility of carrier, C_{OX} = gate capacitance per unit area, W = channel width of the MOS transistor, L = channel length of the MOS transistor, I_D = drain current, V_{GS} = gate-source voltage, V_{DS} = drain-source voltage, V_{TH} = threshold voltage. The parameters of CMOS used in this thesis can be listed in Table 2.2.

Table 2.2 The parameter of 0.5μm CMOS used in this thesis.

MODEL NMOS LEVEL=3 UO=460.5 TOX=1.0E-8 TPG=1 VTO=+0.62
JS=1.08E-6 XJ=0.15U RS=417 RSH=2.73 LD=0.04U VMAX=130E3
NSUB=1.71E17 PB=0.761 ETA=0.00 THETA=0.129 PHI=0.905 GAMMA=0.69
KAPPA=0.10 CJ=76.4E-5 MJ=0.357 CJSW=5.68E-10 MJSW=0.302
CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=3.07E-28 AF=1
WD=+0.11U DELTA=+0.42 NFS=1.2E11 DELL=0U LIS=2 ISTMP=10 TT=0.1E-9

MODEL PMOS LEVEL=3 UO=100 TOX=1.0E-8 TPG=1 VTO=-0.58
JS=0.38E-6 XJ=0.10U RS=886 RSH=1.81 LD=0.03U VMAX=113E3
NSUB=2.08E17 PB=0.911 ETA=00 THETA=0.120 PHI=0.905 GAMMA=0.76
KAPPA=2 CJ=85E-5 MJ=0.429 CJSW=4.67E-10 MJSW=0.631
CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=1.08E-29 AF=1
WD=+0.14U DELTA=0.81 NFS=0.52E11 DELL=0U LIS=2 ISTMP=10 TT=0.1E-9

2.2.2. MOS small signal modeling

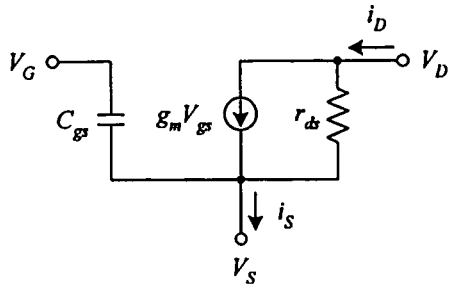

Figure 2.5 The small-signal model for a MOS transistor in active region.

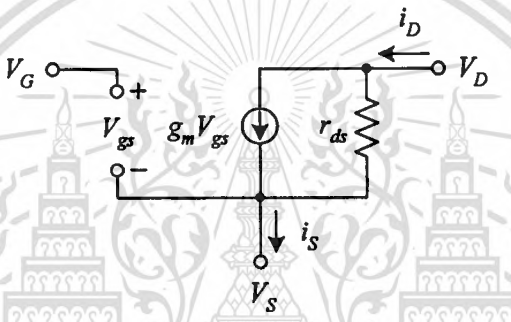

Figure 2.6 The low-frequency, small-signal model.

The most commonly used small-signal model for a MOS transistor operating in the active region is shown in figure 2.5. In this model, it assumes that bulk-source connected. It first consider the DC parameters in which all the parameters are ignored (i.e., replaced by open circuits). This leads to the low-frequency, small-signal model as shown in figure 2.6. The voltage-controlled current source $g_m V_{GS}$ is the most important of the model, with the transistor transconductance g_m defined as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{2.18}$$

Substituting (2.17) in (2.18) to apply the derivative, results the g_m is given by [1]

$$g_m = \sqrt{2\mu_o C_{ox} \frac{W}{L} I_D} \tag{2.19}$$

The r_{ds} is the output resistance of MOS transistor which can calculate the change in the drain-source voltage ΔV_{DS} arising from changes in the drain current ΔI_D. Thus, by using (2.17), r_{ds} can be given by

$$r_{ds} = \frac{\Delta V_{DS}}{\Delta I_D} \cong \frac{1}{\lambda I_D} \tag{2.20}$$

where

$$\lambda = \frac{k_{ds}}{2L\sqrt{V_{DS} - V_{GS} + V_{TH} + \Phi_o}} \tag{2.21}$$

and

$$k_{ds} = \sqrt{\frac{2K_{ds}\varepsilon_o}{qN_A}} \tag{2.22}$$

λ is called channel-length modulation and causes the drain current to increase when the drain-source voltage is increased. Typical values of λ are in the range $0.05V^{-1}$ to $0.005V^{-1}$ [1].

Finally, when MOS transistor enter to saturation region, the gate-source capacitance, C_{gs}, can be expressed by [4]

$$C_{gs} \cong \frac{2}{3} WLC_{OX} \tag{2.23}$$

This capacitance is primarily due to the change in channel charge as a result of a change in V_{GS}. It is the largest capacitor that important in limiting the high frequency of MOS circuits.

2.4. References

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CHAPTER 3

CAPACITOR-GROUNDED CURRENT-MODE ALL-PASS NETWORKS USING MO-CCCIIs

The purpose of this chapter is to present two new networks for realizing first-order current-mode all-pass networks using multi-output second generation current-controlled conveyors (MO-CCCIIs) and a grounded capacitor. The corner frequency can be controlled electronically by adjusting the bias current of the CCCII. Two proposed circuits operate in current-mode and high output impedance. Thus, its can be directly employed as a subsystem of monolithic circuit. The use of a grounded capacitor and without resistor makes the proposed circuit ideal for integrated circuit implementation. PSPICE simulation results are incorporated to verify the theory.

3.1. Introduction

All-pass filters, having constant frequency independent gain, with electronic-controlled phase shifts, are widely useful in many applications, for example, they can be employed as the frequency determining elements in electronic-controlled oscillator, or they can be directly employed as phase modulators in communication systems. Many all-pass filter realizations using active elements are available in the literatures [1]-[9]. These circuits use active elements such as op-amp [1], second-generation current conveyor (CCII) [2]-[5], four-terminal floating nullor (FTFN) [6], current-differencing buffer (CDBA) [7], third-generation current conveyor (CCIII) [8], operational transresistance amplifier (OTRA) [9] and passive RC elements are proposed. Hence they are not easily electronic adjustable.

At present current-mode circuits are becoming popular, since they have many advantages compared with their voltage-mode such as wider dynamic range, inherent wide bandwidth, simple circuitry and low power consumption [9]-[10]. Recently, several circuits for the realization current-mode all-pass filter using difference active components have been reported [2], [6]-[9], [12]-[13]. Among these topologies, one [2], [6] and [9] require an element-matching condition even through it uses a minimum number of active components, another [7] employs three active components

and require output impedance matching device, and the others [8], [12], [13] require floating capacitor.

By using the second-generation current controlled conveyor (CCCII), current conveyor applications can be extended to the domain of electronically adjustable function [10]-[11]. In the past, first-order all-pass filter electronically adjustable transfer functions employing CCCII have been reported [5], [12]-[13]. Some of circuit enjoyed using minimum active elements [12]-[13]. However, all of these circuits require the floating capacitor; hence it not ideality for IC implementation.

In this chapter, two simple first-order current-mode all-pass networks using two multi-output second-generation current controlled conveyors (MO-CCCIIs) and one grounded capacitor are presented. The circuits also operate in current-mode and high output impedance; hence it can be directly employed in many monolithic circuits without extra conversion stages. The proposed current-mode all-pass sections require no external resistor, without matching constrains and are electronically adjustable by controlling the bias current of conveyor. The use of grounded capacitor is beneficial to IC implementation [14], [15].

3.2. Multi-output second generation current-controlled conveyor

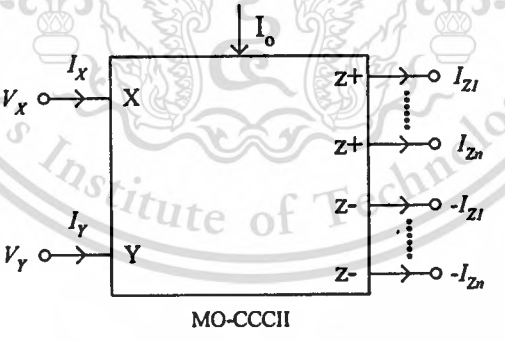

Figure 3.1 MO-CCCII symbols.

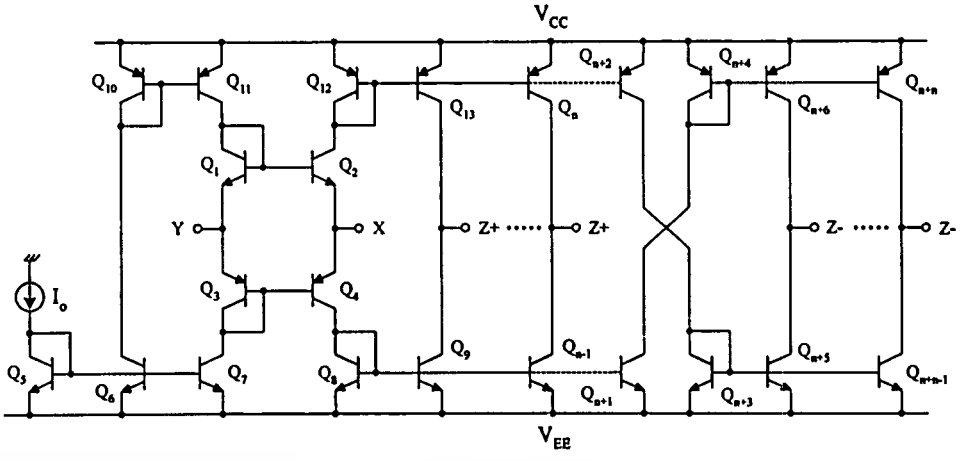

Figure 3.2 The bipolar implementation.

The symbol of a MO-CCCII shown in figure 3.1 is characterized by the following relationship:

$$\left.\begin{aligned} V_X &= V_Y + I_X R_X \\ I_Y &= 0 \\ I_Z &= \pm I_X \end{aligned}\right\} \tag{3.1}$$

The input impedances for the ideal CCCII are infinite at terminal Y and R_X at terminal X, respectively. The terminal Z, that is equivalent to a current generator, possesses infinite output impedance. Electronic adjustability of the CCCII is attributed to the dependent of the parasitic resistance on the bias current of the current conveyor at terminal X.

Positive and negative-type MO-CCCII into a single circuit can easily be implemented using bipolar transistor. Schematic implemented with bipolar transistor is shown in figure 3.2 [16]. The parasitic X-terminal resistance, R_X can be expressed as

$$R_X = \frac{kT/q}{2I_o} = \frac{V_T}{2I_o} \tag{3.2}$$

where V_T is the thermal voltage = 26mV at T = 300°K and I_o is the bias current of the conveyor. R_X can be controlled by varying the bias current I_o.

The plus-type single output CCCII is obtained by removing transistors Q15 to Q28, minus-type single output CCCII is obtained by removing transistors Q13 to Q18 and Q25 to Q28 and plus-type multi-output CCCII is obtained by removing transistors Q19 to Q28.

3.3. Proposed current-mode all-pass networks

The proposed first-order current-mode all-pass network with two CCCIIs and a grounded capacitor is shown in figure 3.3. Note that the use of grounded capacitor is particularly attractive for integrated circuit implementation [14], [15]. The input current of the circuit is connected to the port X of the plus-type MO-CCCII, which makes its input impedance can be obtained through the bias currents I_{o1} and I_{o3}, whereas, output current signal taken out through port z of CCCIIs; hence its high output impedance.

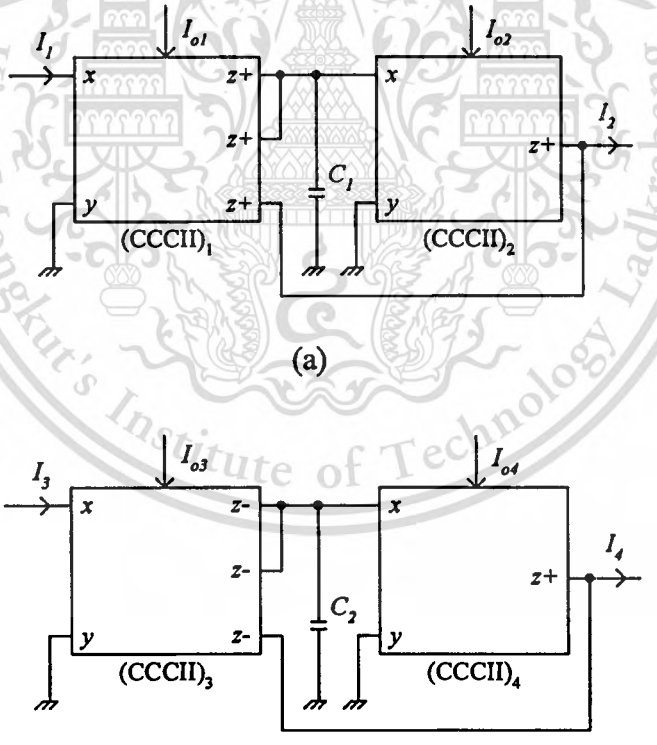

Figure 3.3 The current all-pass network using two CCCIIs with a grounded capacitor: (a) phase shifts from +180° to 0, (b) phase shifts from 0 to -180°.

The current transfer functions of the circuit in figures 3.3(a) and 3.3(b) are given as follows:

$$\frac{I_2}{I_1} = \frac{sC_1R_{X2} - 1}{sC_1R_{X2} + 1} \tag{3.3}$$

$$\frac{I_4}{I_3} = \frac{1 - sC_2R_{X4}}{1 + sC_2R_{X4}} \tag{3.4}$$

Equations (3.3) and (3.4) show the network of figures 3.3(a) and (b) realize two first-order current-mode all-pass networks and yield phase shifts from +180° to 0 and from -180° to 0, respectively, without constant loss in a current-mode all-pass characteristic. The corner frequency of the circuit in figure 3.3(a) (ω_{O1}) and 3.3(b) (ω_{O2}) are found as, respectively:

$$\omega_{O1} = \frac{1}{C_1R_{X2}} = \frac{2I_{o2}}{V_TC_1} \tag{3.5}$$

$$\omega_{O2} = \frac{1}{C_2R_{X4}} = \frac{2I_{o4}}{V_TC_2} \tag{3.6}$$

From equations (3.5) and (3.6), it is obvious that the pole frequency of two all-pass networks can be controlled with adjusting bias currents I_{o2} and I_{o4}. Therefore the electronically tunable can be obtained.

3.4. Performance analysis

The ideal circuit previous realization based on assumption the characteristics of CCCIIs are perfectly transferred. However, in a practical realization, several non-idealities that contribute to error form the ideal performance are present. The major factors to be considered are current tracking errors of the CCCIIs, non-ideal effect when the all-pass networks operating in high and sensitivity.

3.4.1. Tracking error effect

Taking into account the non-idealities of CCCIIs, equation (3.1) can be modified as

$$\left.\begin{aligned} V_X &= \alpha V_Y + I_X R_X \\ I_Y &= 0 \\ I_Z &= \pm\beta I_X \end{aligned}\right\} \tag{3.7}$$

where

$$\left.\begin{aligned} \alpha &= (1-\varepsilon_V) \\ \beta &= (1-\varepsilon_i) \end{aligned}\right\} \tag{3.8}$$

Here $\varepsilon_V(|\varepsilon_V|\ll 1)$ and $\varepsilon_i(|\varepsilon_i|\ll 1)$ represent the voltage and current transfer errors, respectively. The non-ideal current transfer function of figures 3.3(a) and 3.3(b) can be rewritten as

$$\frac{I_2}{I_1} = \frac{\alpha(sC_1R_{X2} + 1 - 2\alpha)}{sC_1R_{X2} + 1} \tag{3.9}$$

$$\frac{I_4}{I_3} = \frac{\alpha(2\alpha - 1 - sC_2R_{X4})}{1 + sC_2R_{X4}} \tag{3.10}$$

From equations (3.9) and (3.10), indicate that the current tracking error effect will be dominant in the gain and no effect on corner frequency of all-pass network. However, practically, the current transfer ratio (α) of CCCII are unity; thus equations (3.9) and (3.10) are reduced to the ideal current transfer function of equations (3.3) and (3.4), respectively.

3.4.2. High frequency limitation

The equivalent circuit of CCCII operating in high frequency is shown in figure 3.4. The non-ideal operation of the CCCII [18] results in parasitic elements at each port, represented as R_X in series with L_X, R_Y in parallel with C_Y, R_Z in parallel with C_Z, for ports x, y, and z, respectively.

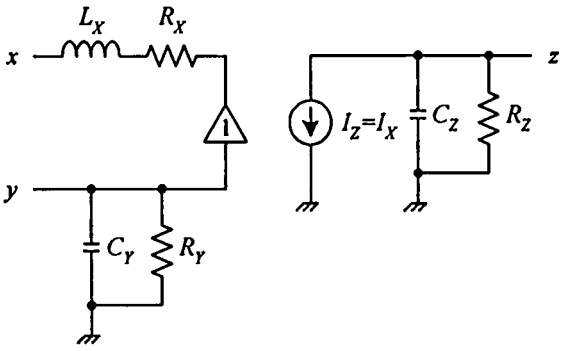

Figure 3.4 Equivalent circuit of CCCII.

The proposed current-mode all-pass networks are analyzed by taking into account the non-idealities of CCCIIs. Taking these effects into consideration, the non-ideal current transfer function for the circuit of figures 3.3(a) and 3.3(b) can be expressed as

$$\frac{I_2}{I_1} = \frac{R_{Z1} - \left(1 + sR_{Z1}\left(C_1 + C_{Z1}\right)\left(R_{X2} + sL_{X2}\right)\right)}{R_{Z1} + \left(1 + sR_{Z1}\left(C_1 + C_{Z1}\right)\left(R_{X2} + sL_{X2}\right)\right)} \tag{3.11}$$

$$\frac{I_4}{I_3} = \frac{\left(sR_{Z3}\left(C_2 + C_{Z3}\right)\left(R_{X4} + sL_{X3}\right) + 1\right) - R_{Z3}}{\left(sR_{Z3}\left(C_2 + C_{Z3}\right)\left(R_{X4} + sL_{X3}\right) + 1\right) + R_{Z3}} \tag{3.12}$$

At high frequencies, an inductance L_X appears in series with R_X and C_Z appears in parallel with R_Z. For a practical CCCII, R_{X2}, $R_{X4} \ll R_Z$, $C_Z \ll C_1$, C_2 up to hundreds of MHz. Thus, non-ideal errors will not affect on gain and corner frequency of proposed circuits, but the value of inductance L_X of equations (3.11) and (3.12) will effect on the corner frequency of the all-pass characteristics.

3.4.3. Sensitivity study

The incremental sensitivity of all-pass network of figure 3.3 is analysed. Suppose the bias currents are $I_{o2}=I_{o4}=I_o$ and $C_1=C_2=C$, the active and passive ω_O sensitivities of the proposed all-pass network can be expressed as

$$S_{I_o}^{\omega_o} = -S_C^{\omega_o} = -S_{V_T}^{\omega_o} = 1 \tag{3.13}$$

It is evident from (3.13) that incremental sensitivities for the pole ω_o of the all-pass network are within 1 in magnitude. Thus, the circuit enjoys the attractive sensitivity performance.

3.5. Simulation results

To verify the proposed circuit, PSPICE simulation is used. The CCCII is simulated using the schematic implementation shown in figure 3.2 with a DC supply voltage ±2.5V. The BJT model parameters of the NR100N and PR100N transistors given in Table 2.1 are used in the simulation [17].

Figures 3.5 and 3.6 shows the magnitude and phase of current transfer function versus frequency obtained from the simulation using, as an example, capacitors C_1=C_2 =12nF, I_{o2}=I_{o4}=100μA. It can be seen from figure 3.5 that, for the phase shift at +90°, the corresponding corner frequency is 100kHz and at -90°, the corresponding corner frequency is 100kHz, which can be shown in figure 3.6. In figures 3.5 and 3.6, the deviation of the gain-magnitude is 0.1 and 0.3, respectively, and the phase-error is 0.7° and 1.5°, respectively, when compared with theory.

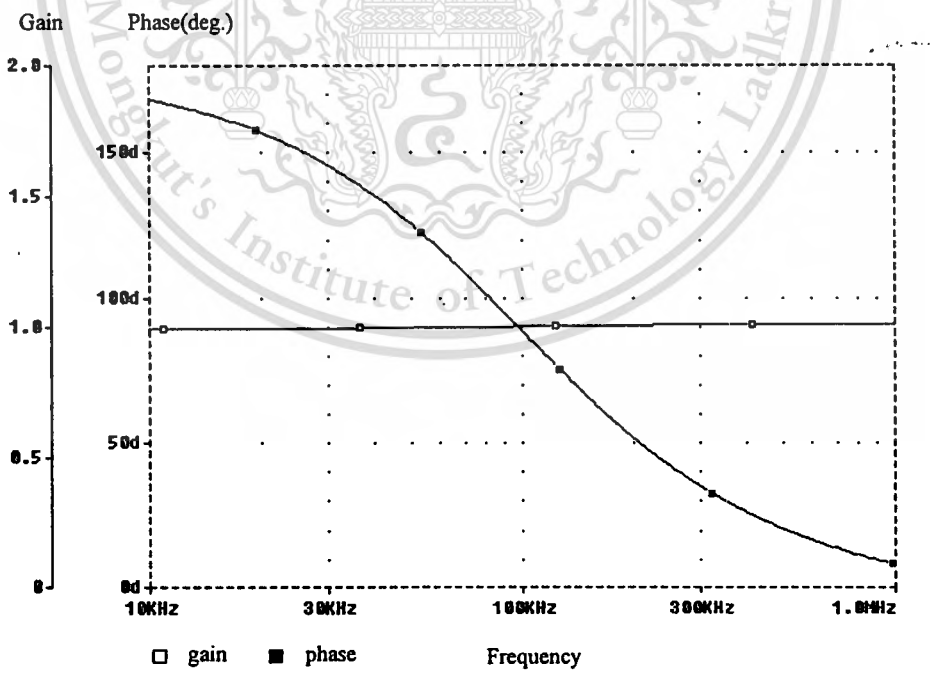

Figure 3.5 Magnitude and phase characteristics of I_2/I_1 versus frequency using the capacitor C_1=12nF and bias current I_{o2}=100μA of figure 3.3(a).

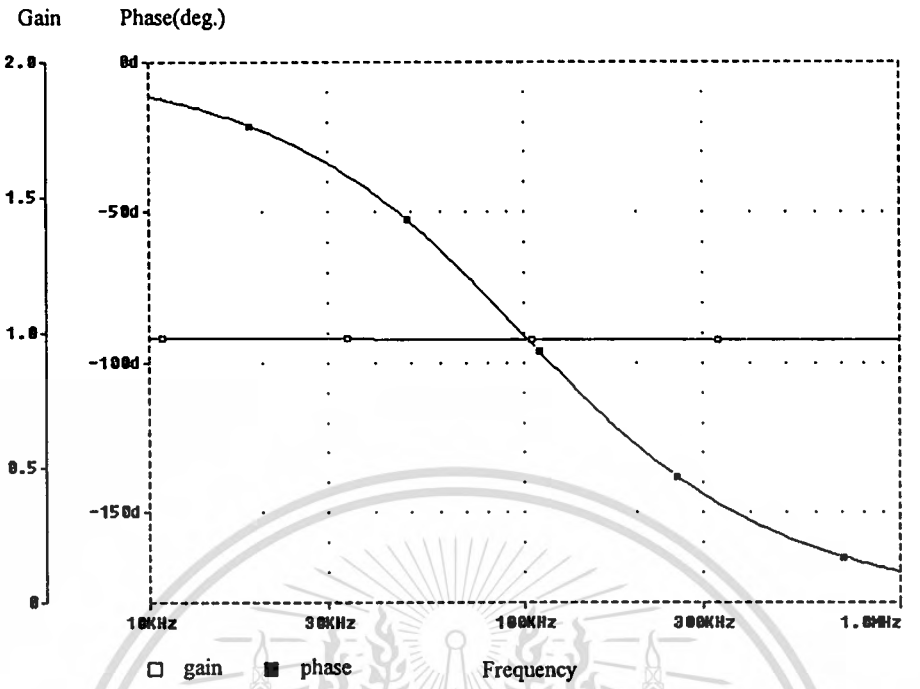

Figure 3.6 Magnitude and phase characteristics of I_4/I_3 versus frequency using the capacitor C_2=12nF and bias current I_{o4}=100μA of figure 3.3(b).

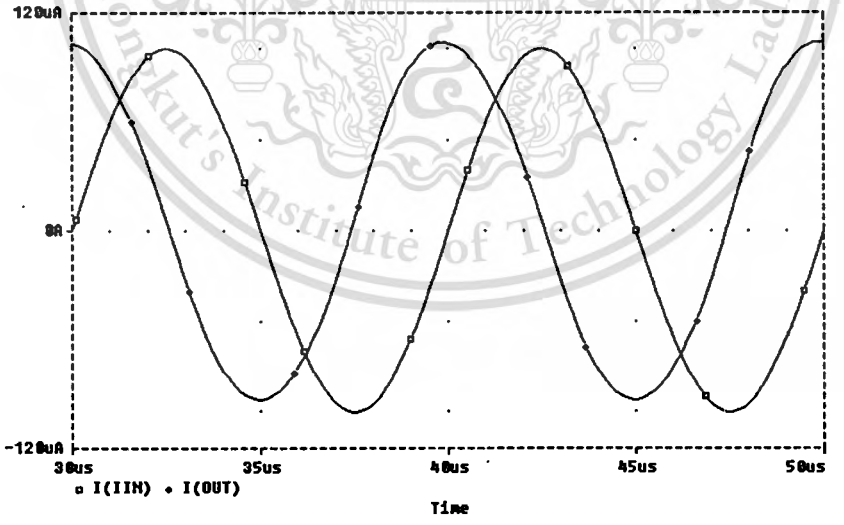

Figure 3.7 Time domain waveforms of the input and +90 degree-shifted output currents of figure 3.3(a).

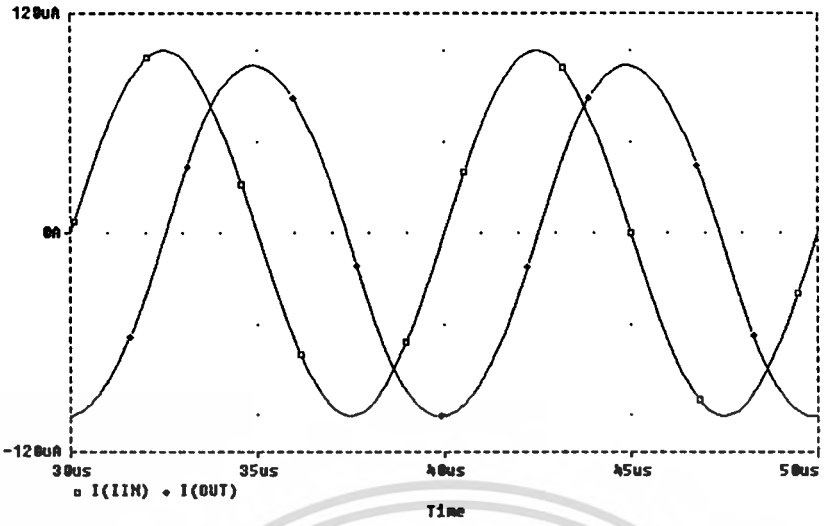

Figure 3.8 Time domain waveforms of the input and -90 degree-shifted output currents of figure 3.3(b).

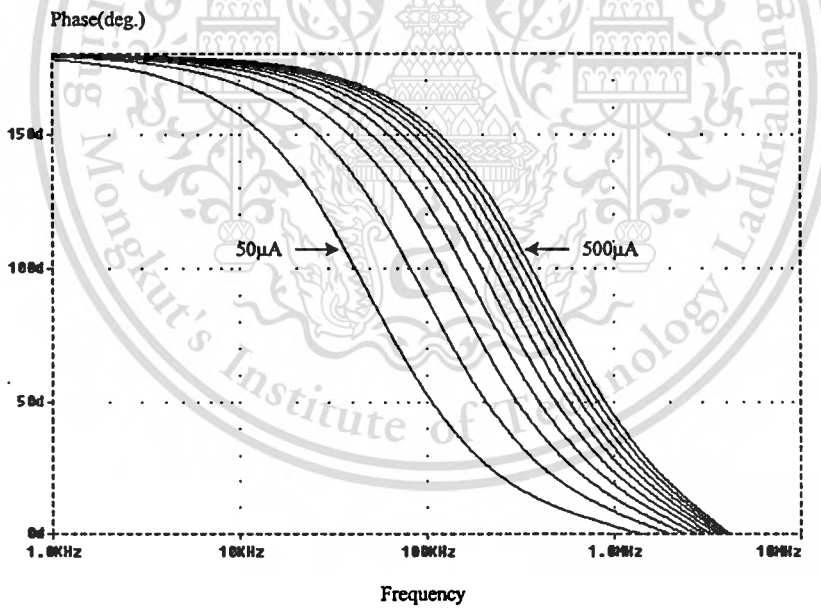

Figure 3.9 Current-tuning of corner frequency with bias current from 50µA to 500µA with the step 50µA for C_1=12nF of figure 3.3(a).

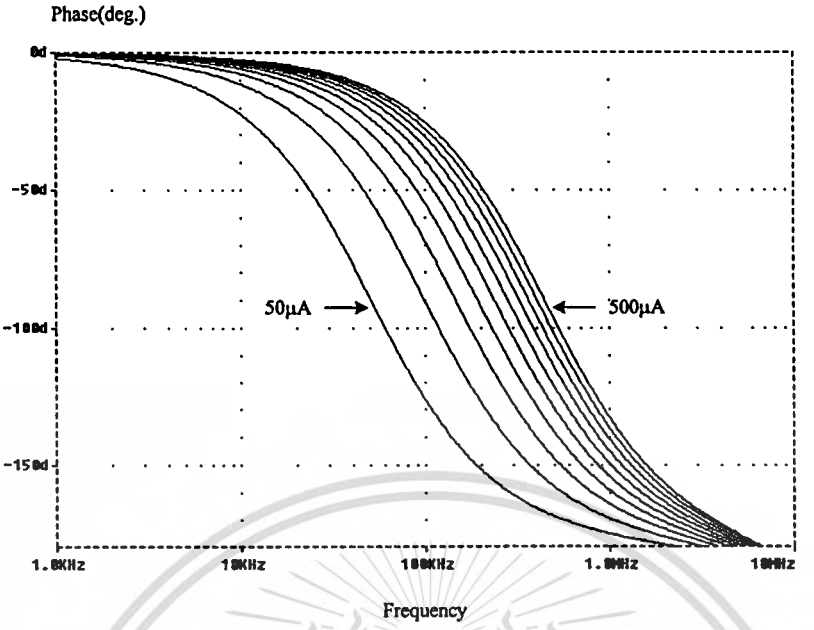

Figure 3.10 Current-tuning of corner frequency with bias current from 50μA to 500μA with the step 50μA for C_2=12nF of figure 3.3(b).

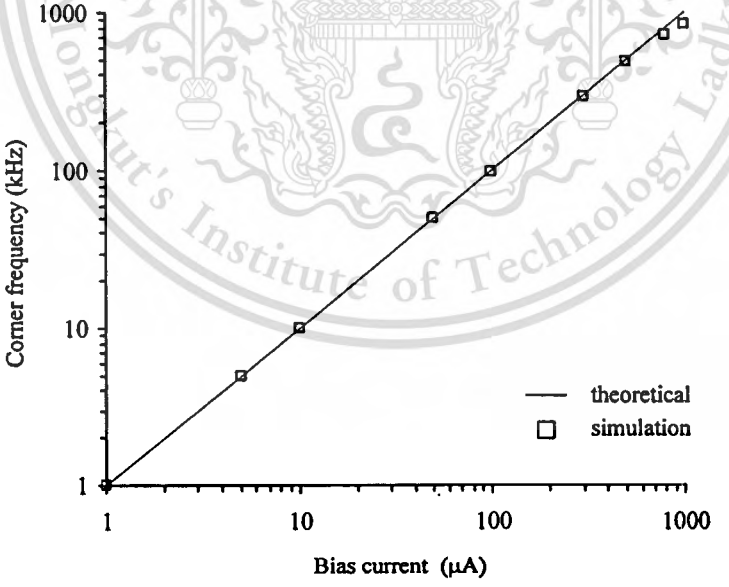

Figure 3.11 Current-tuning of corner frequency with bias current for C_1=12nF of figure 3.3(a).

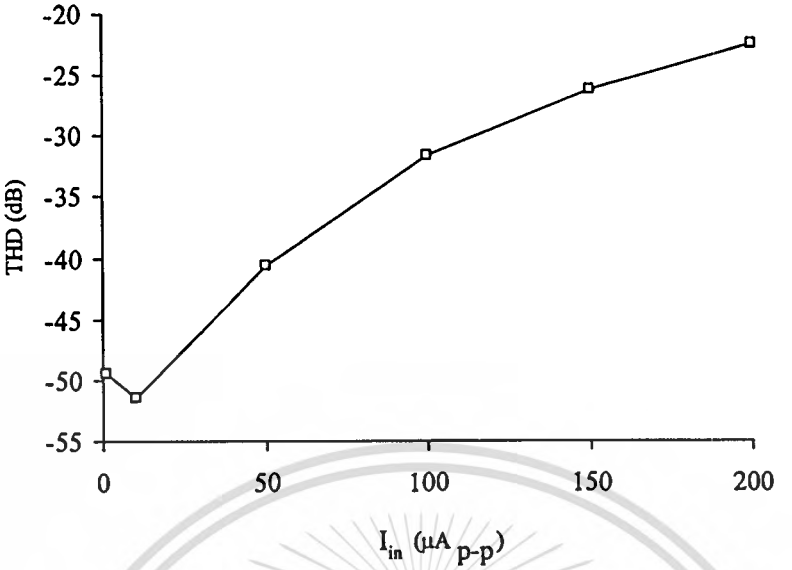

Figure 3.12 Variation of THD with input current signal for I_{o2}=100μA of figure 3.3(a).

Time domain waveforms of the input and output currents are shown in figures 3.7 and 3.8 for the above designed values, showing a +90 and a -90 degree, respectively, phase-shift in the output to a sinusoidal input of 100kHz.

Figures 3.9 and 3.10 are shown the electronic tuning aspect of the current-mode all-pass network where the phase response for varying bias current is given. It can be noted that for the design of a 90° and a -90° phase shifter, the frequency is varied from 5kH to 500kH for variation of I_{o2} and I_{o4}, respectively, from 50μA to 500μA with the step of 50μA.

The proposed circuit of figures 3.3(a) and 3.3(b) are realized the same basic idea. Therefore, to conform with theory again, only the corner frequency versus bias current of figure 3.3(a) is potted which shown in figure 3.11. The proposed circuit in figure 3.3(a) is also simulated for the study of total harmonic distortion (THD) at the output. Figure 3.12 shows the dependence of THD on the input current signal level by applying a sinusoidal input of 10kHz with C_1 =12nF and I_{o2}=100μA. The THD is found lower that -40dB for amplitude of 50μA.

3.6. Quadrature oscillator with all-pass network

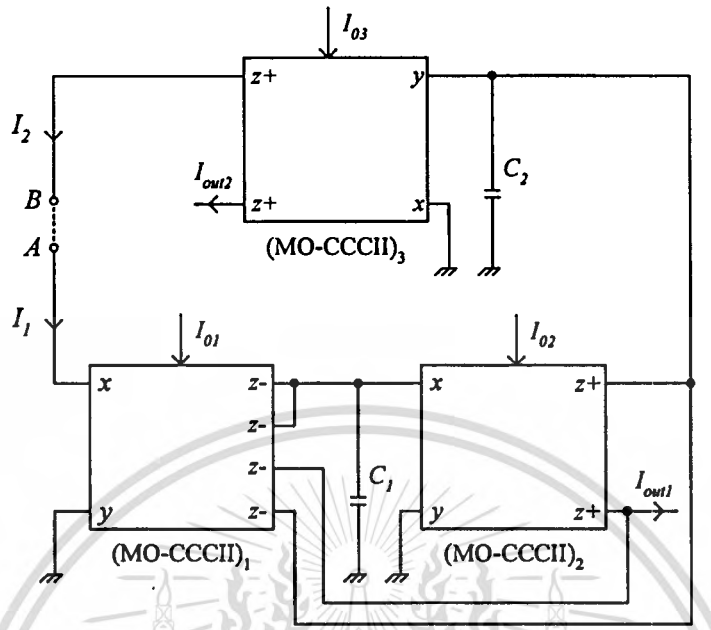

Figure 3.13 Current-mode quadrature oscillator using current-mode all-pass network of figure 3.3(a) and lossless integrator.

As an application the proposed circuit is used to construct a current-mode quardrature oscillator circuit as shows in figure 3.13 with lossless integrator in closed loop. The MO-CCC$_3$ along with C_2 forms the lossless integrator. By cascading with a current-mode all-pass network and a current-mode lossless integrator, the current transfer function of current-mode quadrature oscillator circuit can be written as

$$\frac{B}{A}=\frac{I_2}{I_1}=\frac{s-1/C_1R_{X2}}{s+1/C_1R_{X2}}\frac{1/C_2R_{X3}}{s} \tag{3.14}$$

For sinusoidal oscillation, the loop (LG) should be equal to 1 (B/A=1), for s=jω, therefore B must be feedback connected to A. The condition of oscillation can be obtained as

$$\frac{1/R_{X3}}{1/R_{X2}}=\frac{C_2}{C_1} \tag{3.15}$$

and

$$\omega_o = \left(1/C_1C_2R_{X2}R_{X3}\right)^{1/2} \tag{3.16}$$

If select C_1=C_2=C and R_{X2}=R_{X3}=R_X, the frequency of oscillation is given by

$$\omega_o = 1/R_xC \tag{3.17}$$

From (3.17), since R_X=$V_T/2I_o$, it is shows that the frequency of oscillation linearly proportional to the bias current I_o. Two current outputs are obtained as I_{out1} and I_{out2}. Because of I_{out1} and I_{out2} are obtained across the lossless integrator formed by C_2 and MO-CCCII$_3$; hence it ensure that the phase difference, ϕ, between I_{out1} and I_{out2} is $\phi = 90^\circ$ [18]. The proposed circuit enjoys the high output impedance, the electronic tunability, that is, the ω_O can be controlled using the bias current of the MO-CCCIIs. The use of all grounded capacitor is particularly attractive for IC implementation [14]-[15].

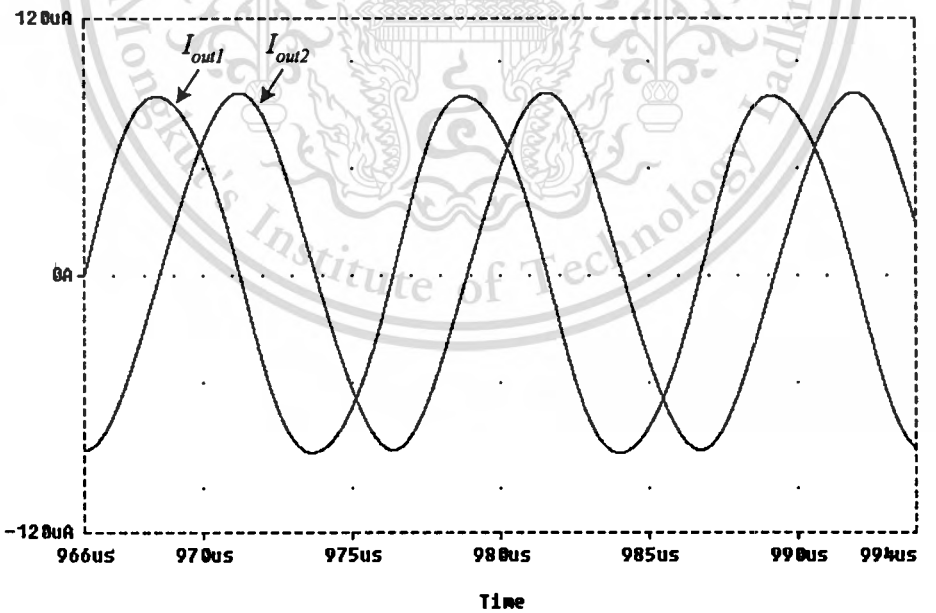

Figure 3.14 Simulated output waveforms of the current-mode quadrature oscillator.

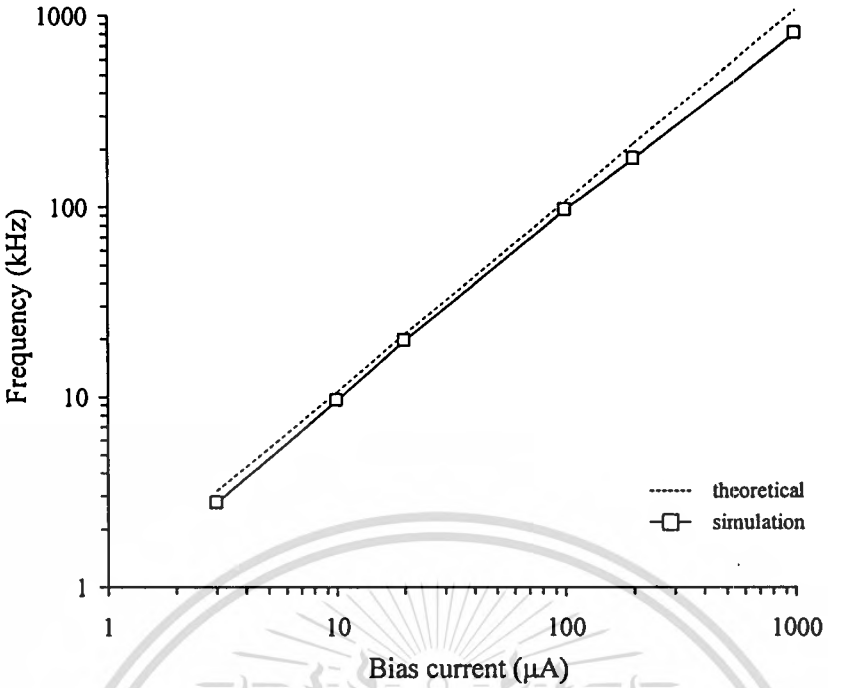

Figure 3.15 Plots of oscillation frequencies versus bias current.

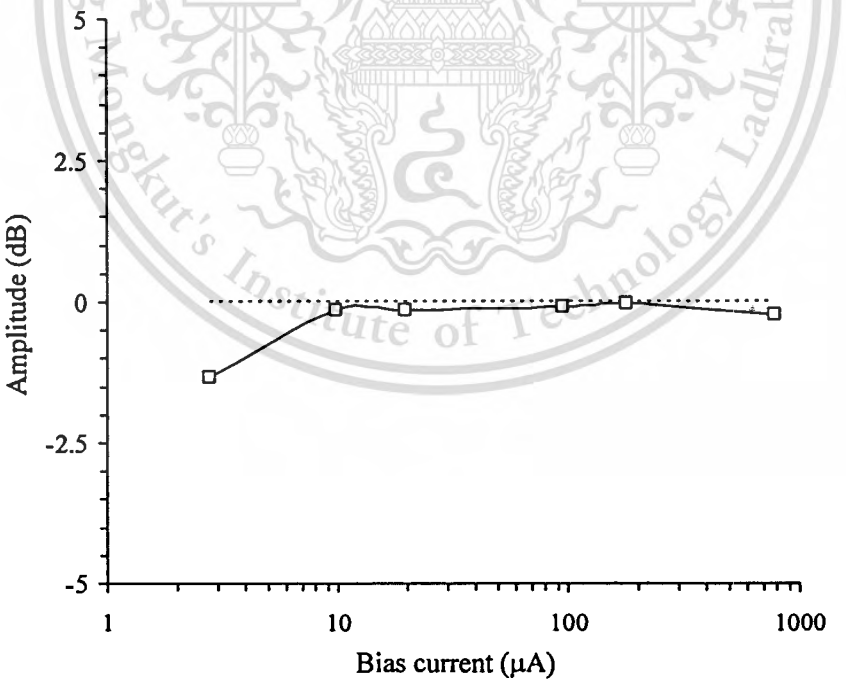

Figure 3.16 Plots of amplitudes of I_{out1} versus bias current.

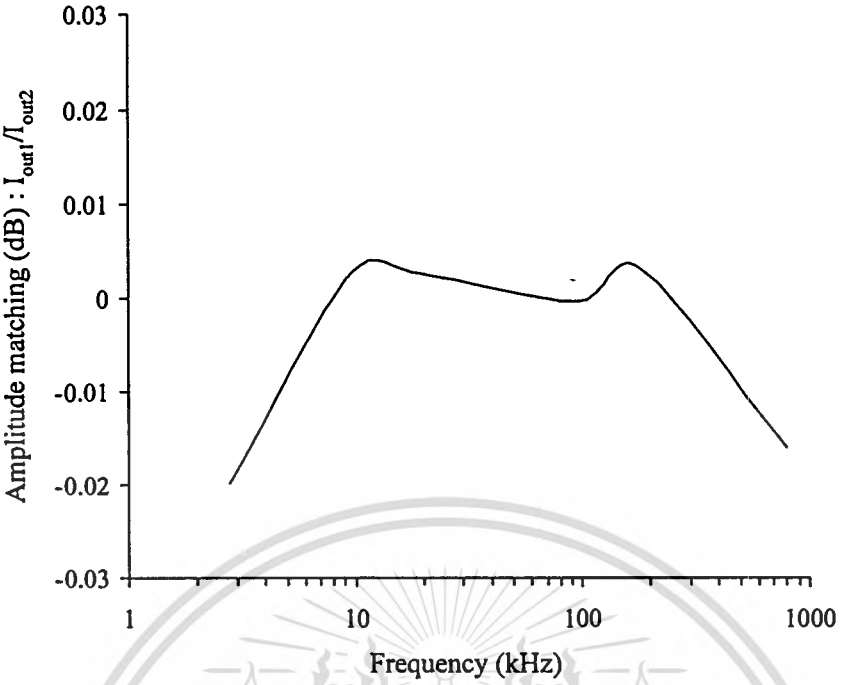

Figure 3.17 Amplitude matching of the quadrature signals versus frequency.

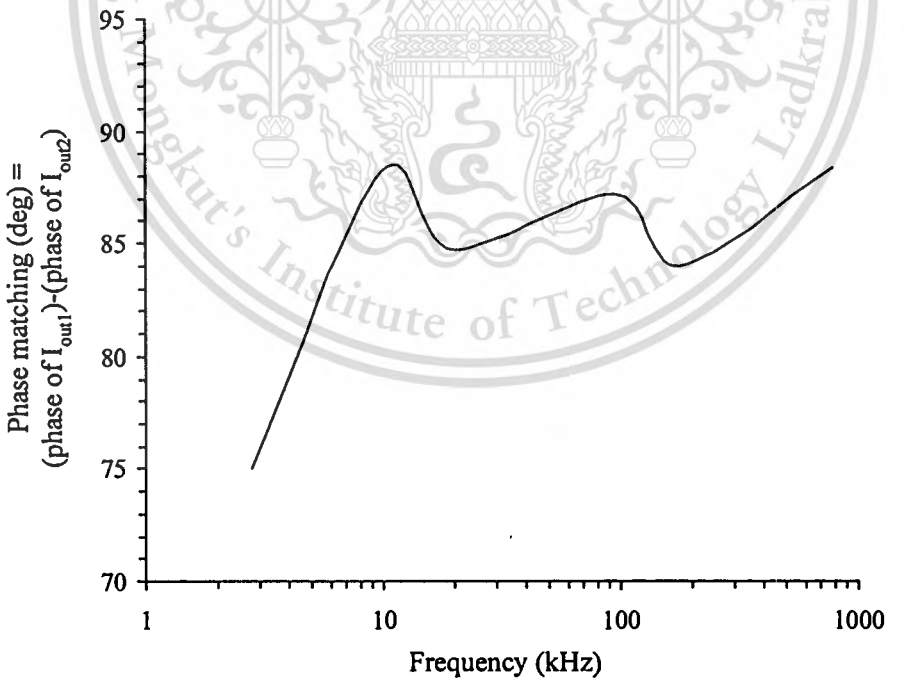

Figure 3.18 Phase matching of the quadrature signals versus frequency.

Again, the performance of the circuit show in figure 3.13 has been simulated through PSPICE. The BJT model parameters of the NR100N and NP100N transistors given in Table 2.1 are used in the simulation [17]. Figure 3.14 shows the simulated output wave form I_{out1} and I_{out2} of the circuit in figure 3.13 with C_1=12nF, C_2=11nF, $I_{o2}=I_{o3}$=100μA where C_1 was designed to be larger than C_2 to ensure the oscillator will start. The oscillation frequency is simulated to be 96kHz. Figure 3.15 illustrates comparisons of the plots of oscillation frequencies versus bias currents for cases of theory analysis and PSPICE analysis. The comparisons of the plots of amplitudes versus bias current for cases of theory analysis and PSPICE analysis are shown in figure 3.16. It can be seen that the circuit exhibits a large tuning range. The simulation results agree quite well with the theoretical analysis. Figures 3.17 and 3.18 depict the amplitude matching in term of the ratio I_{out1}/I_{out2} and the phase matching in term of the difference (phase of I_{out1})-(phase of I_{out2}), respectively, of the quadrature signals versus frequencies.

3.7. Conclusion

This work has proposed two approaches of realization of current-mode all-pass network. All proposed circuits employ two CCCIIs and one grounded capacitor. The circuits exhibit the following properties:

(i) use of a grounded capacitor without requiring any passive components, which is an attractive for intregration;

(ii) its offer a simple circuitry and does not require any parameter matching condition;

(iii) provides electronic control of corner frequency over a wide range through the bias current of CCCII;

(iv) low passive and active parameters sensitivity.

As an application, a current-mode quadrature oscillator circuit is realized. The MO-CCCII based circuits are verified using simulation. The quadrature oscillator exhibits advantages follow the pattern of current-mode circuit. The results are confirmed by PSPICE with the device parameters for AT&T CBIC-R process as listed in Table 2.1.

3.8. References

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CHAPTER 4
HIGH FREQUENCY AND HIGH PRECISION CMOS FULL-WAVE RECTIFIER

This chapter describes a high frequency and high precision full-wave rectifier using a fully differential input and output operational transconductance amplifier (FDIO-OTA), which is very suitable for CMOS technology implementation. The system comprises a voltage to current converter, precision full-wave rectifier and a current to voltage converter. An input voltage signal is converted into two symmetrical current signals by using a FDIO-OTA. Two current signals will be rectified by using MOS diodes and convert into output voltage by using grounded MOS resistor. The circuit exhibits a very precise rectifier and very high operating frequency. The simulation results demonstrate the performance of the proposed circuit.

4.1. Introduction

The full-wave rectifier is a circuit that is an extension of the half-wave rectifier which is an important circuit building block used in nonlinear analogue signal processing systems such as telecommunication, instrumentation, measurement and control. The low-level signals and the precision rectifiers are very important. The main problem of the operation of diode-only rectifier is limited by the threshold voltage (approximately 0.7V for silicon diode). The precision rectifiers based on operational amplifier (op-amp), diodes and resistors are presented [1]-[4]. The exhibit of these proposed is an output distort in the crossover region, called "corner distortion". The corner distortion is an error during the zero crossing of the input signal since the op-amp and diodes have to recover during non-conduction/conduction transition with a finite small signal *dv/dt* (slew rate). The use of the high slew-rate op-amps does not solve this problem because it is a small signal transient problem [5]. The gain-bandwidth is a parameter of op-amp that limits the high frequency performance of this scheme. Moreover, since these structures use the op-amp and the resistors; these circuits are not suitable for IC fabrication.

The precision full-wave rectifier consisting of current conveyors, diodes and resistors has also been proposed that enjoys attractive feature of high frequency performance and the low zero crossing distortion by using current-mode technique [5]-[7]. However, these circuits require the two current conveyors as well as characteristics. Mismatching of current conveyors will affect the output waveform of full-wave format, namely, the amplitude of the first polarity signal may not be the equalized amplitude of the second polarity signal. In addition, the circuit proposed in Toumazou *et al.* [5], Khan *et al.* [6] requires a floating resistor which is not ideal for IC implementation. The realization of full-wave rectifier based on CMOS class-AB configuration was proposed by Ramirez-Angulo [8], Surakampontorn and Riewruja [9]. This proposed approach requires the signal current to be greater than four times the bias current to avoid the square-law error of MOS transistors. Another approach is based on the use of one current conveyor and bipolar transistors operating in class B [10], this circuit is realization that enjoys the high precision rectifier. However, the two grounded resistors are used and the high frequency performance is limited in this scheme.

Linear operational transconductance amplifier (OTA) is a voltage to current converter circuit which is a fundamental building block of analogue circuit and systems. It is used as the main active element such as continuous-time active filter, analog multiplier, voltage controlled-resistance etc. The OTA provides a highly linear electronic tunability and a wide frequency range. Moreover, OTA-based circuits require no resistor, and therefore, are suitable for monolithic implementation. The precision rectifier based on using an OTA and diodes is presented by Sanchez-Sinencio *et al.* [11] as shown in figure 4.1; this circuit is the half-wave rectifier. The single ended OTA can provide only half-wave rectifier.

This paper presents the design of a high frequency and high precision CMOS full-wave rectifier circuit. This circuit is possibly realized by using FDIO-OTA as shown in figure 4.2. The use of multi-outputs OTA will reduce the number of elements and will miniaturize the circuit. The circuit consists of FDIO-OTA, MOS diodes and MOS resistor. The proposed precision MOS diode realization of the full-wave rectifier is drain-source-connected gate and is attached to ground. The resistor is implemented by MOS transistors. Therefore, all components can be designed based on CMOS technology without passive component. This proposed rectifier yields the following advantages.

(i) The proposed full-wave rectifier does not have the external resistors, therefore it is more suitable for IC fabrication than previously proposed [5]-[6].

(ii) The proposed full-wave rectifier rectifies the high frequency up to 200MHz when simulated through PSPICE program with 0.5μm CMOS model obtained through MIETEC, whereas previous full-wave rectifier can operate at 100MHz frequency.

(iii) The proposed full-wave rectifier provides the high precision voltage rectifying.

(iv) At temperature lower than 60°C, the proposed full-wave rectifier has good temperature stability without compensation technique.

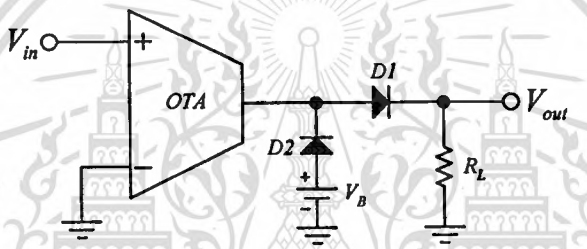


Figure 4.1 Single ended OTA-based half-wave rectifier.

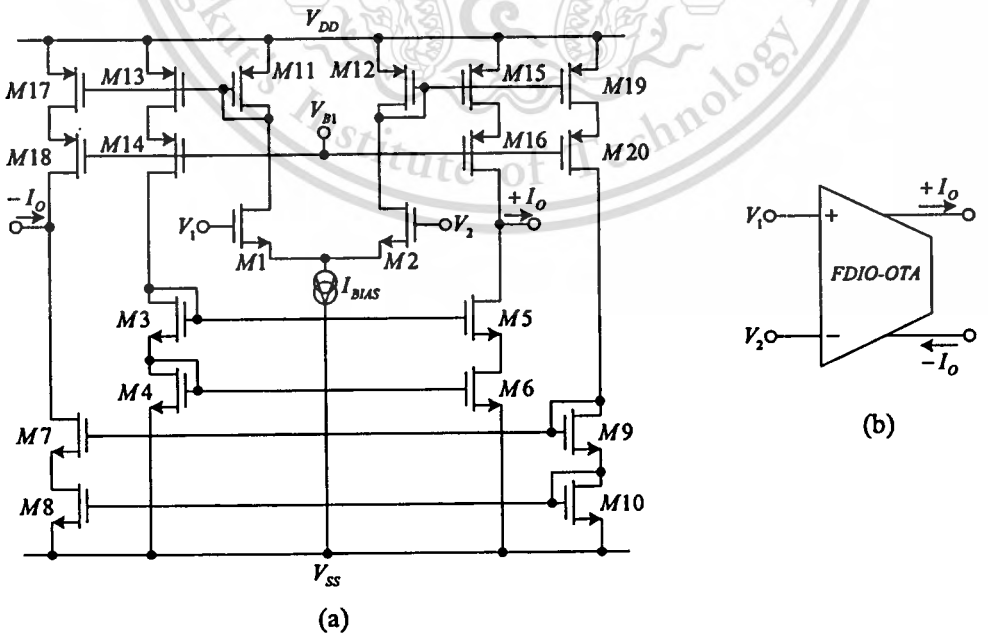


Figure 4.2 (a) CMOS FDIO-OTA structure, (b) Symbol.

4.2. Fully differential input and output operational transconductance amplifier

The OTA has input as voltage, output as current. The simple structure of the well-know OTA is a single ended OTA, having used only four transistors and a current source. Figure 4.2 shows the FDIO-OTA. It is a really symmetric architecture, which has inherently common-mode feedback. Assuming all the MOS transistors in the circuit operate in their saturation regions, the output current of the FDIO-OTA yields

$$I_O = \pm g_m(+V_1 - V_2) \tag{4.1}$$

where

g_m = transconductance

I_O = output current

V_1, V_2 = input voltages

$$g_m = \sqrt{(\mu C_{OX} W / L)(I_{BIAS})} \tag{4.2}$$

where

μ = mobility of carrier;

C_{OX} = gate capacitance per unit area;

W, L = channel width and channel length of the MOS transistor, respectively;

I_{BIAS} = bias current.

where the plus and minus signs of the output current represent $+I_O$ and $-I_O$. The circuit symbol of FDOI-OTA is shown in figure 4.2(b). In following simulation process, this circuit is used to emulate the proposed full-wave rectifier.

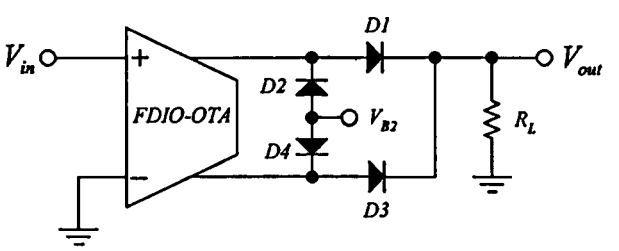


Figure 4.3 FDIO-OTA-based full-wave rectifier.

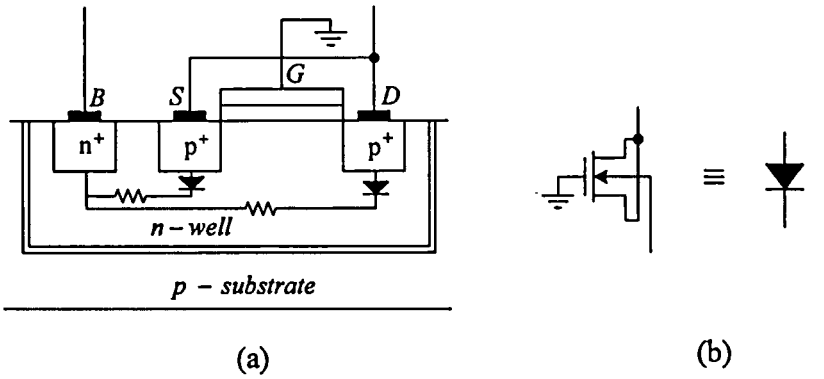


Figure 4.4 MOS diode: (a) cross-section of MOS diode, (b) symbol.

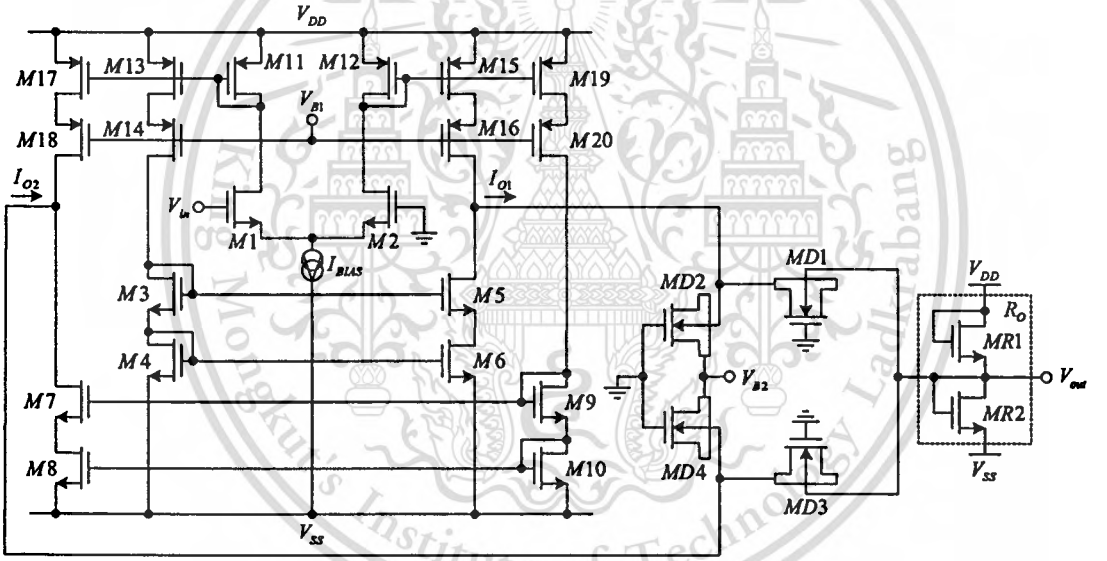


Figure 4.5 Complete circuits of proposed high frequency and high precision full-wave rectifier.

4.3. Proposed full-wave rectifier circuit

This proposed full-wave rectifier is extended from the half-wave rectifier as shown in figure 4.1. The proposed full-wave rectifier is shown in figure 4.3, it actually performs the current domain. In the scheme of figure 4.3, the circuit consists of a FDIO-OTA to change the voltage into current (V-I converter), the four diodes rectify the current and a resistor changes the rectified current into the output voltage

(I-V converter). By using the MOS diode as shown in figure 3.4, the scheme of the full-wave rectifier in figure 4.3 can be realized by all MOS transistors as shown in figure 4.5. The relativity of the positive and negative polarity input voltage and output current can be expressed as

$$V_{in} > 0 : I_{O1} = +g_m V_{in} \tag{4.3.1}$$

$$V_{in} < 0 : I_{O2} = -g_m V_{in} \tag{4.3.2}$$

The operation of the proposed circuit is as follows. In case of the positive polarity input voltage that makes MD1 as well as MD4 turned on, and MD2 and MD3 as well as turned off. The output current I_{O1} will flow through MD1 and MOS grounded resistor (MR1 and MR2), resulting in positive polarity voltage at V_{out}, whereas the output current I_{O2} is bypassed to ground via MD4. The negative polarity input voltage that makes MD2 including MD3 to be turned on, and MD1 including with MD4 to be turned off. The output current I_{O2} will flow through MD3 and MOS resistor, this current creates the positive voltage at V_{out}. The current output I_{O1} is connected to ground by MD2. Using (4.1) and $R_O=1/g_m$, the relation between the input and the output voltage of the proposed rectifier can be obtained as:

$$V_{in} > 0 : V_{out} = +V_{in} \tag{4.4.1}$$

$$V_{in} < 0 : V_{out} = -V_{in} \tag{4.4.2}$$

The MOS diodes, MD1 to MD4, can be implemented by drain-source-connected and gate attached to ground [12]. It is possible to use a MOS transistor connected as a diode as shown in figure 4.4. Assume the MOS process version of p-substrate is used in figure 4.4(a), therefore, MOS diode is suitable for implementing in n-well. The bulk and drain-source-connected can represent the anode and cathode, respectively. For this technique, the MOS diode yields the following advantages.

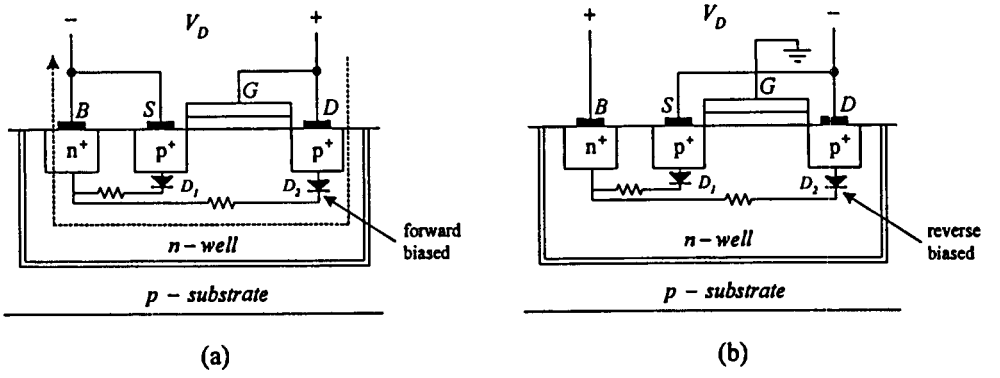


Figure 4.6 Cross-section of two diode-connected PMOS transistor: (a) drain-gate-connected and bulk-source-connected, (b) drain-source-connected and gate attached to ground.

(i) In the part, it well-known that the MOS diode can be implemented by drain-gate-connected and bulk-source-connected [1]. Assume an PMOS transistor is connected in such a way, the MOS diode can be shown in figure 4.6(a), whereas this thesis uses the MOS diode as shown in figure 4.6(b). The bulk of the PMOS transistor from n-well CMOS process and source-drain-connected are represent the anode and cathode, respectively. The MOS diode in figure 4.6(b) will not turn on when the voltage across it is negative. The explanation of the operation is as follows. In case of $V_{sg}=V_D$ is negative, the drain and source terminals interchange and it see that new gate-source terminals are shorted [1]. The junction diode D_1, which is established between n-well and p^+-diffusion of the drain region is forward biased so that a current flows from node D, through diode D_2, to node B. As can be expected, this current increases exponentially with the magnitude of $-V_D$. By contrast, there is no current flowing though either D_1 or D_2, if the bulk is became the anode and source-drain-connected is became the cathode, as shown in figure 4.6(b).

(ii) The threshold voltage of a MOS transistor as function of the bulk-source voltage V_{BS} is given by

$$V_{TH} = V_{THO} + \gamma\left(\sqrt{|2\phi_F - V_{BS}|} - \sqrt{|2\phi_F|}\right) \tag{4.5}$$

where

V_{THO} zero bias threshold voltage;

γ bulk effect factor;

ϕ_F Fermi potential.

For PMOS transistors, $2\phi_F \approx -0.7V$, $\gamma \approx -0.5V^{1/2}$, and $V_{THO} \approx -0.58V$, typically, and a bulk bias V_{BS} is normally > 0V, which numerically increases the threshold voltage. However, by biasing VBS < 0V, it can actually decrease the threshold voltage [16], [17]. From figure 4.20(b), when an MOS diode is received the forward bias, VBS < 0; hence the threshold voltage of MOS diode can be decreased since they have a threshold voltage of approximately 0.4 (typically ≈ 0.58V).

(iii) The MOS diode in figure 4.6(b) yields better temperature stability than the MOS diode in figure 4.6(a).

MOS resistor using two MOS transistor is shown in figure 4.5 by Wang [13]. The operation of MOS resistor is as follows. Assume MR1 and MR2 have the same characteristics remaining in the saturation region. The resistance value of MOS resistor can be expressed as

$$R = \frac{1}{2K(V_{DD} - V_{TH})} \tag{4.6}$$

where

$K = \mu_O C_{OX}(W/L)$,

V_{TH} = threshold voltage,

V_{DD} = supply voltage.

The V_{B2} is a constant DC voltage source for reducing the distortion due to the small signal *dv/dt* limitation [5]. The voltage source $V_{B2}=V_{TH,MD2}+V_{TH,MD4}$, which is a value approximately equal to the sum of the threshold voltage of MOS diodes MD2 and MD4.

4.4. High frequency considered

Ideally, when applying the high frequency at the input of full-wave rectifier, full-wave pattern must appear at the output node and the output positive polarity must be as same as the input positive polarity. The next output positive polarity must be the same as the input negative polarity. However, in practice, delay and distortion are present. The major factor to be considered is parasitic capacitance. The circuit model of a non-ideal OTA operating in saturation region is shown in figure 4.7(a), where C_{in} is the input capacitance, C_O is the output capacitance and G_O is the output conductance. The circuit model of a non-ideal MOS diode is shown in figure 4.7(b), where C_{BS} is the bulk-source capacitance and C_{GS} is the gate-source capacitance. When non-ideal OTA and MOS diode are included in the rectifier, the proposed circuit in figure 4.3 can be redrawn as figure 4.8 and the high-frequency transfer function of the circuit is

$$\frac{v_{out}}{v_{in}} = \frac{s^2 C_{BS1} C_T G_O G_m + s C_{BS1}}{1 + s(C_{BS1}R_L + C_{RO}R_L + C_{BS1}) + s^2(C_{BS1}^2 R_L - C_{BS}^2 + C_{BS1}C_{RO}R_L) + s^3 C_{BS1}^2 C_{RO} R_L} \quad (4.7)$$

where $C_T = C_O + C_{BS2} + C_{GS1}$. C_{RO} is the output capacitance of MOS resistor.

For high-frequency response, the major high-frequency limitation of the proposed circuit results from the C_{BS} of the MOS diode. The output capacitance of the OTA (C_O) is affected by decreasing the precision.

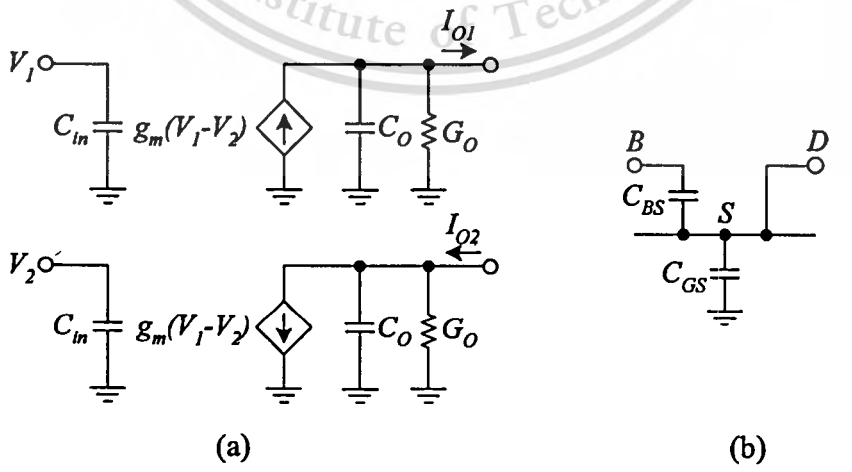


Figure 4.7 Circuit model of non-ideal: (a) FDIO-OTA, (b) MOS diode.

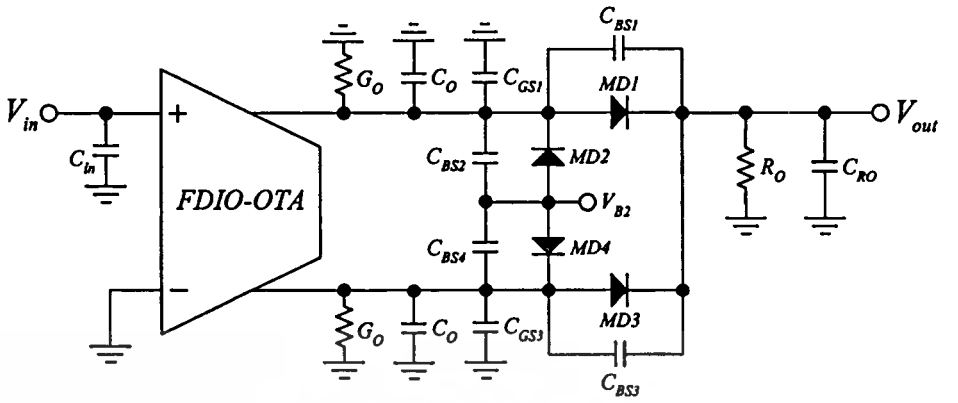


Figure 4.8 Circuit model of non-ideal proposed full-wave rectifier.

4.5. Simulation results

In order to confirm the validity of the proposed rectifier, PSPICE simulation was carried out. The parameters used in simulation are 0.5μm CMOS model obtained through MIETEC as listed in Table 2.1. The W/L parameters of MOS transistors are 25μm/1μm for M1 to M10, 40μm/1μm for M11 to M20, 3.2μm/1μm for MR1 to MR2, 0.6μm/0.5μm for MD1 to MD4 and I_{BIAS}=500μm. The supplied voltages used are V_{DD}=-V_{SS}=5V, V_{B1}=2V and V_{B2}=0.8V. The DC transfer characteristics of the proposed full-wave rectifier are shown in figure 4.9, which shows the operating voltage ranging from –500mV to 500mV of the input voltage. The zero crossing region of the DC transfer characteristic is shown in figure 4.10. In this figure, corner distortion is found as 196μV.

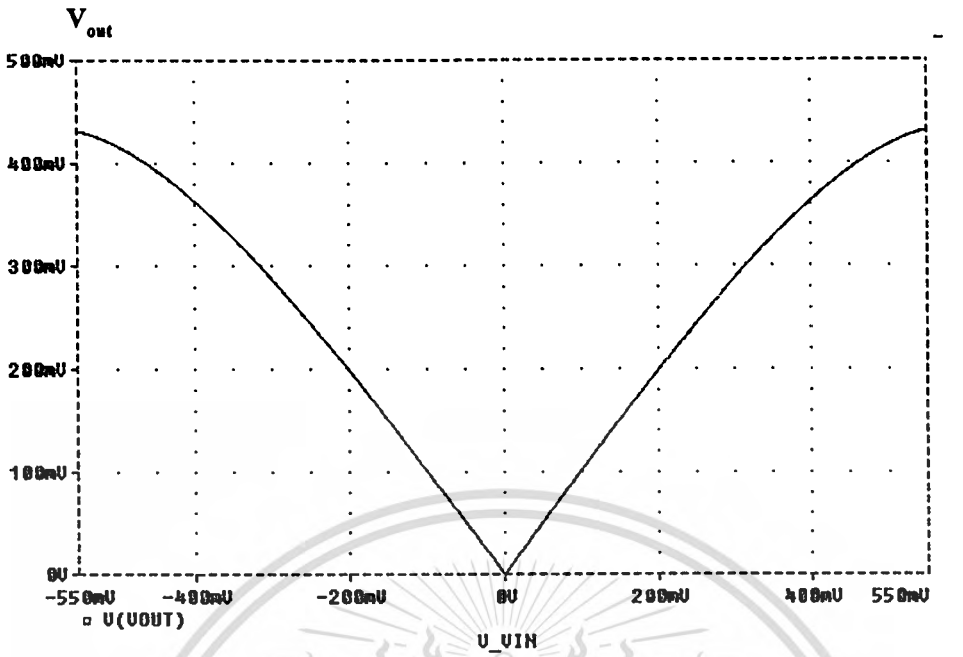


Figure 4.9 Simulated results for DC transfer characteristic.

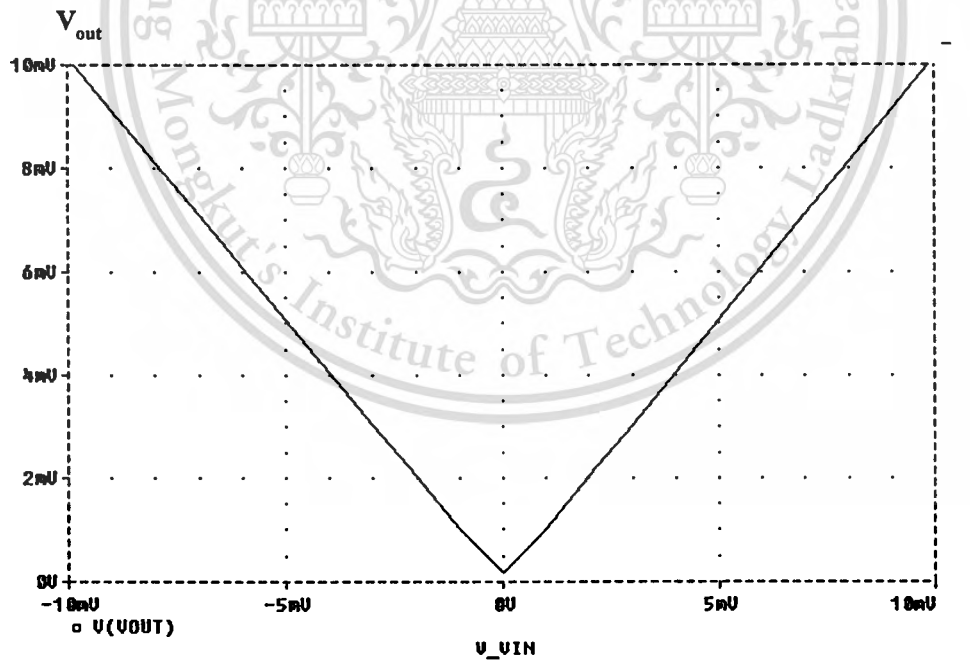


Figure 4.10 Simulated results for DC transfer characteristic at zero crossing regions.

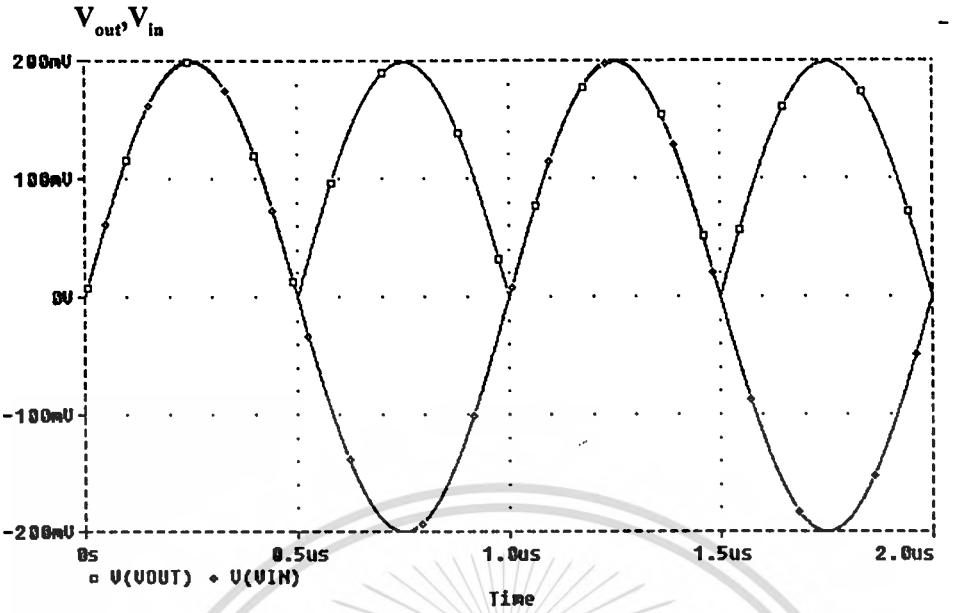


Figure 4.11 Operation of the proposed full-wave rectifier at a frequency 1MHz.

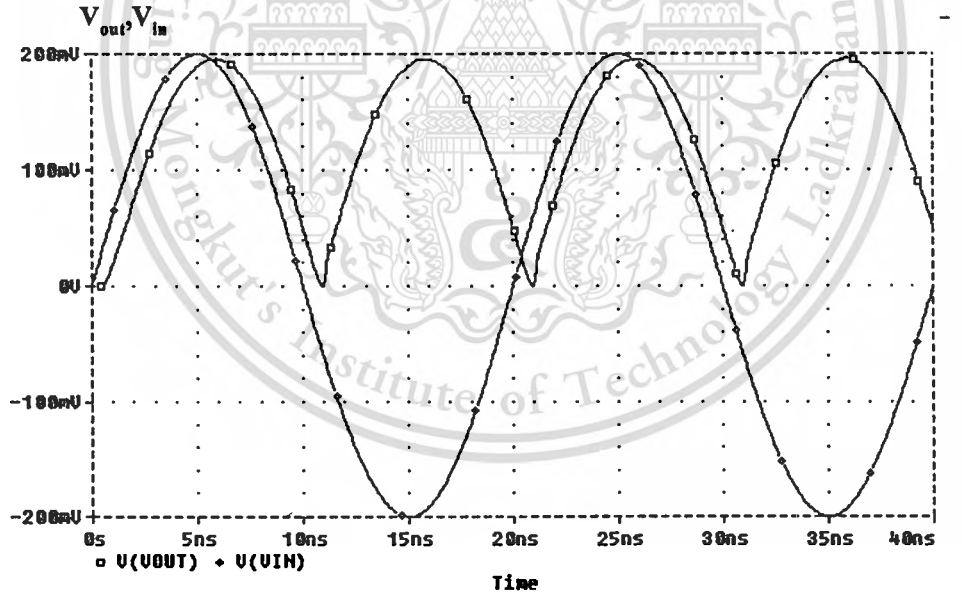


Figure 4.12 Operation of the proposed full-wave rectifier at a frequency 50MHz.

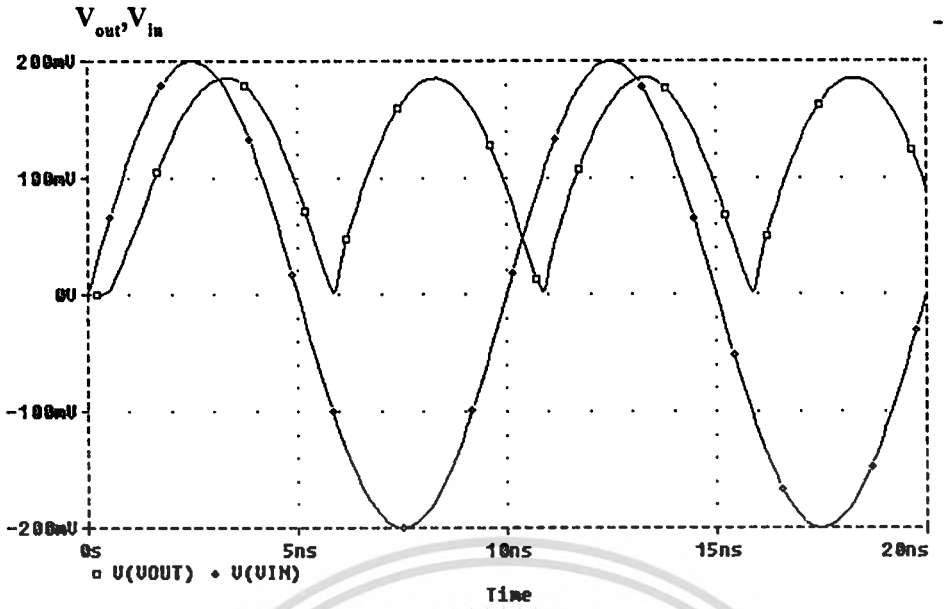


Figure 4.13 Operation of the proposed full-wave rectifier at a frequency 100MHz.

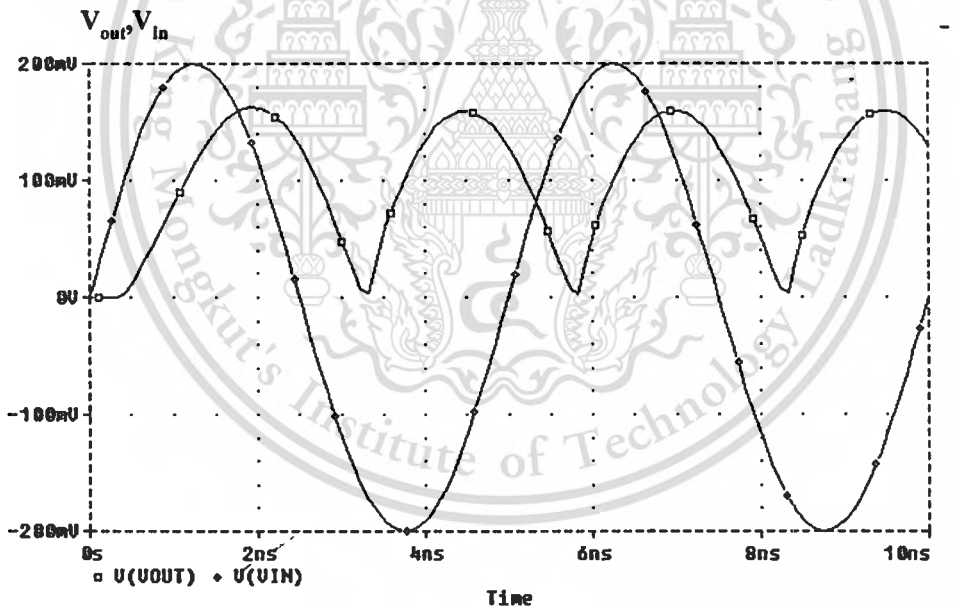


Figure 4.14 Operation of the proposed full-wave rectifier at a frequency 200MHz.

Applying the $200mV_{peak}$ sine wave at the input of the proposed full-wave rectifier, the input and output signals at frequency of 1MHz, 50MHz, 100MHz, and 200MHz are shown in figures 4.11 to 4.14, respectively. The amplitude errors between the input and output signals in figures 4.13 and 4.14 resulted from the

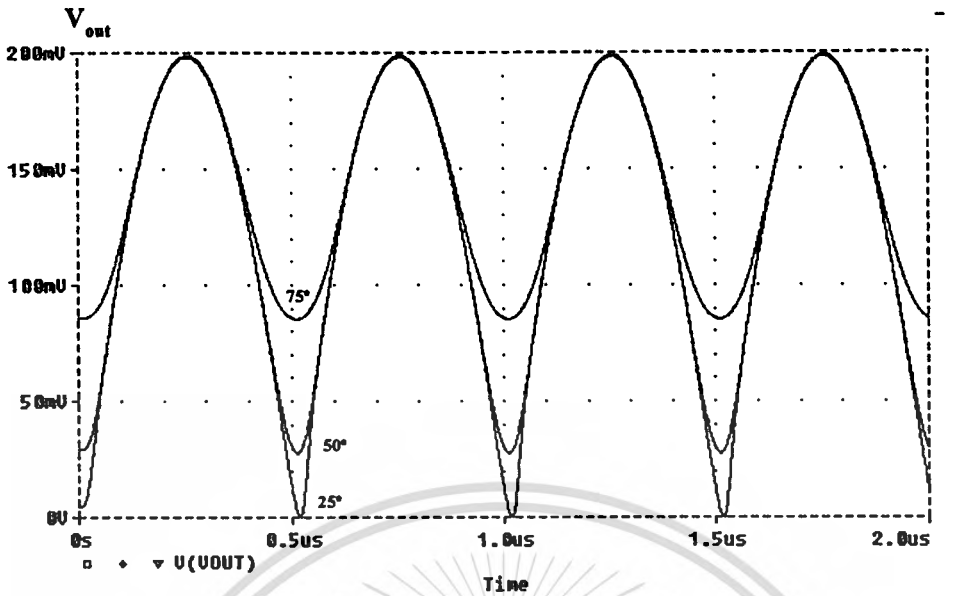
decreased gain of the proposed rectifier for the operation at high frequency. This problem can easily be compensated by increasing the value of R_O through decreasing the W/L ratio of MR1 and MR2.

4.6 Temperature considered

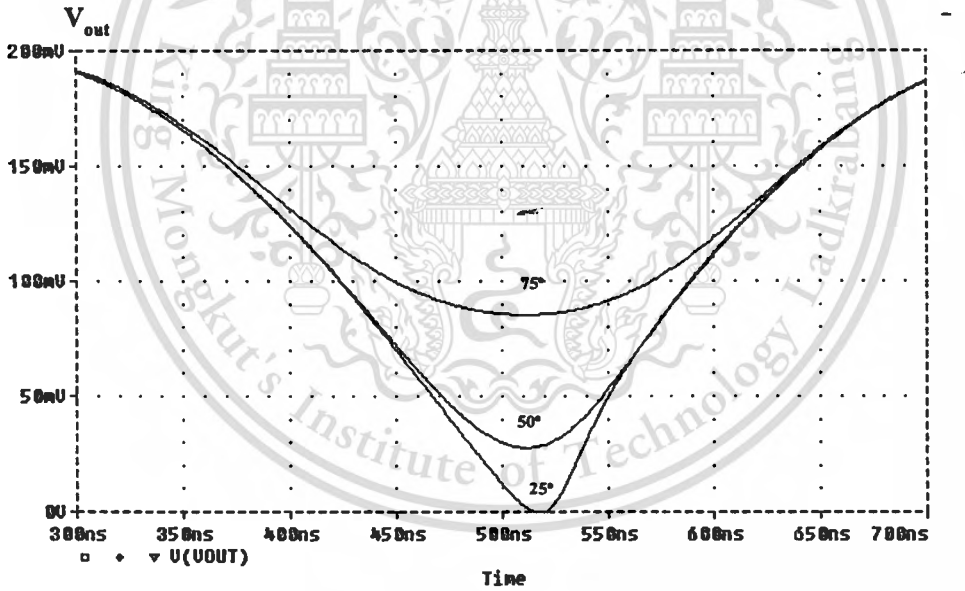
The precision full-wave rectifiers with the addition of a DC voltage source (V_B) proposed by Toumazou *et al.* [5], with bias the rectifying diodes to a quiescent point close to their ON stage. Unfortunately, this biased voltage rectifier design exhibits a poor temperature characteristic, with the additional drawback that any excess of bias voltage V_B will directly add to the DC offset voltage at the output node. This section demonstrates that the MOS diode have less temperature sensitivity than the Schocttky diode [5].

At the frequency of 1MHz, this repost simulates the temperature performance of the proposed full-wave rectifier as shown in figure 4.5 by changing temperatures from 25°C to 75°C. Figure 4.15 shows the output waveform of the proposed rectifier at temperatures of 25°C, 50°C and 75°C when the MOS diodes MD1 to MD4 of figure 4.5 is replaced with Schottky diodes. Again, figure 4.16 shows the output waveform of the proposed rectifier at temperatures of 25°C, 50°C and 75°C when the circuit of figure 4.5 is MOS diodes. In figure 4.16, the zero crossing are 166μV, 1.6mV and 11.6mV at 25°C, 50°C and 75°C, respectively, whereas, in figure 4.15 the zero crossing are 100μV, 28mV, and 85mV at 25°C, 50°C, and 75°C, respectively. The temperature-dependent parameter of the MOS diode is V_{TH} and μ [14], whereas the temperature-dependent parameter of the Schottky diode is V_T [15]. It is evaluated that V_T of Schottky diodes have the temperature more sensitive than V_{TH} and μ of MOS diodes; or namely, the Schottky diode has a temperature more sensitive than the MOS diode.

A solution to improve the poor temperature characteristic has been proposed in [15] with the use of a "DC current-biased" diode circuit, as shown in figure 4.17. The good temperature stability can be achieved. However, it is a cause of the precision decreasing at the high frequency. To demonstrate this point, this report again presents the simulation of the proposed full-wave rectifier at the frequency of 100MHz with the temperature compensated by replacing the voltage source V_{B2} with DC current source [15] as shown in figure 4.17.

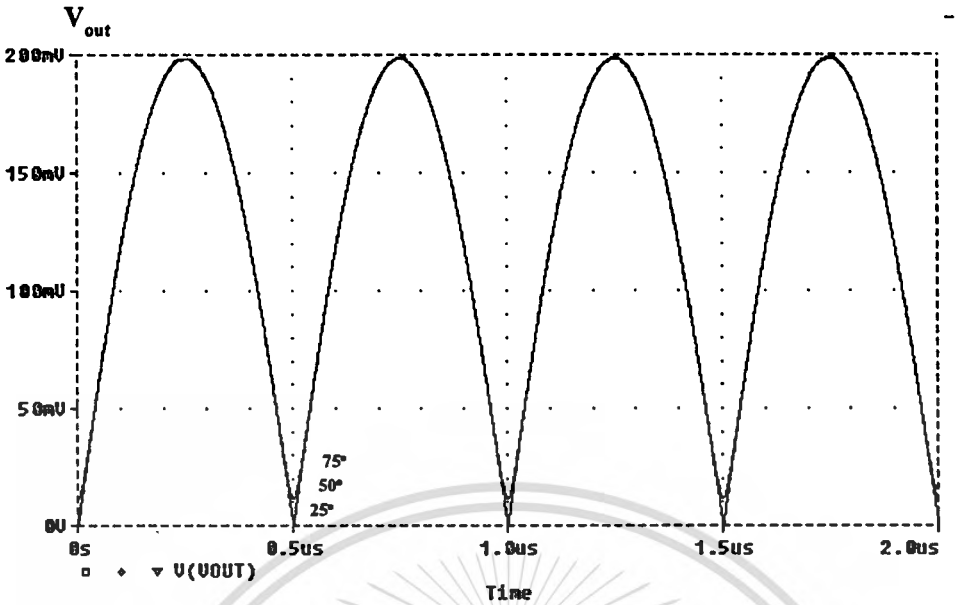


(a)

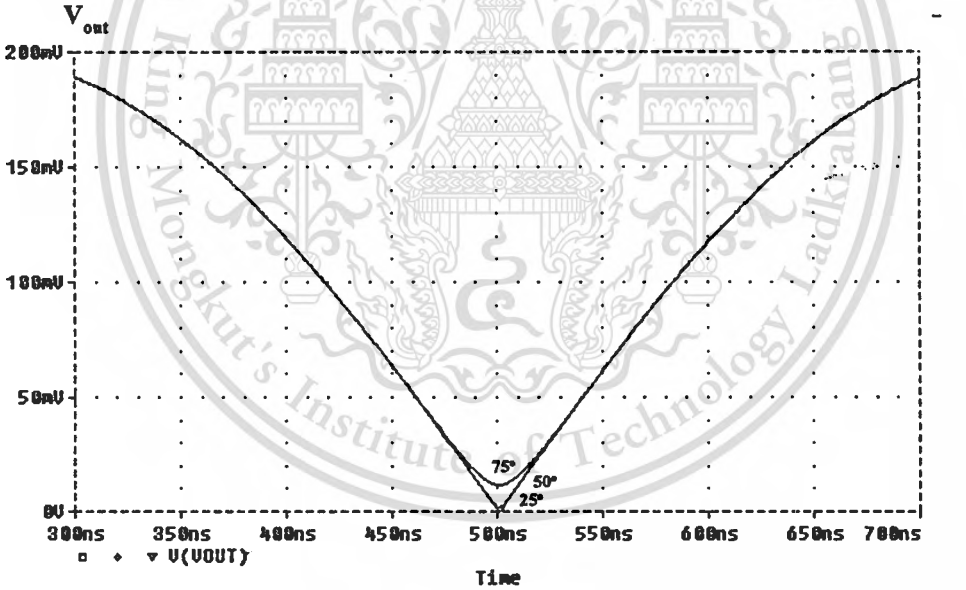


(b)

Figure 4.15 Operation of the proposed full-wave rectifier of a frequency 1MHz at different temperatures when CMOS diodes are replaced with Schottky diode: (a) full-wave output, (b) zero crossing regions.



(a)

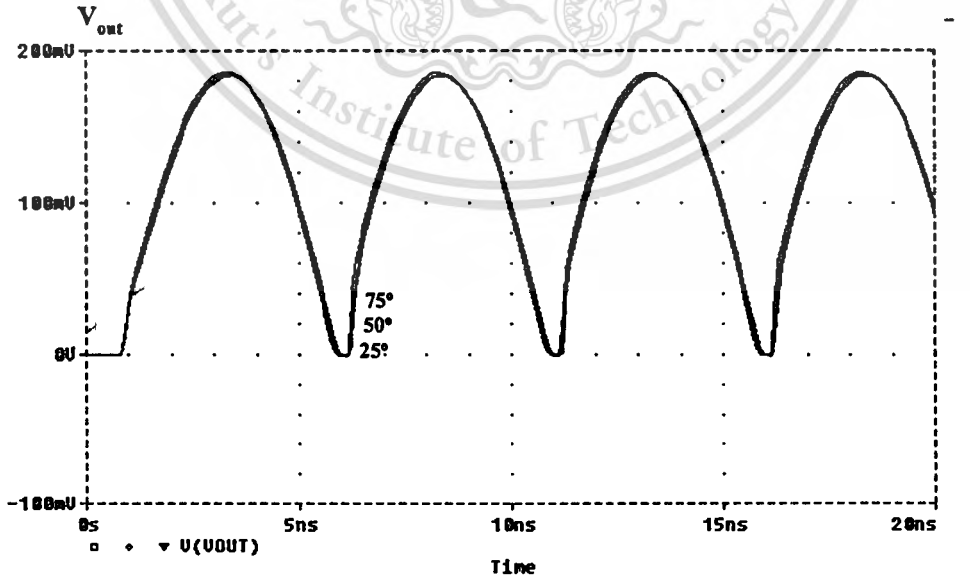


(b)

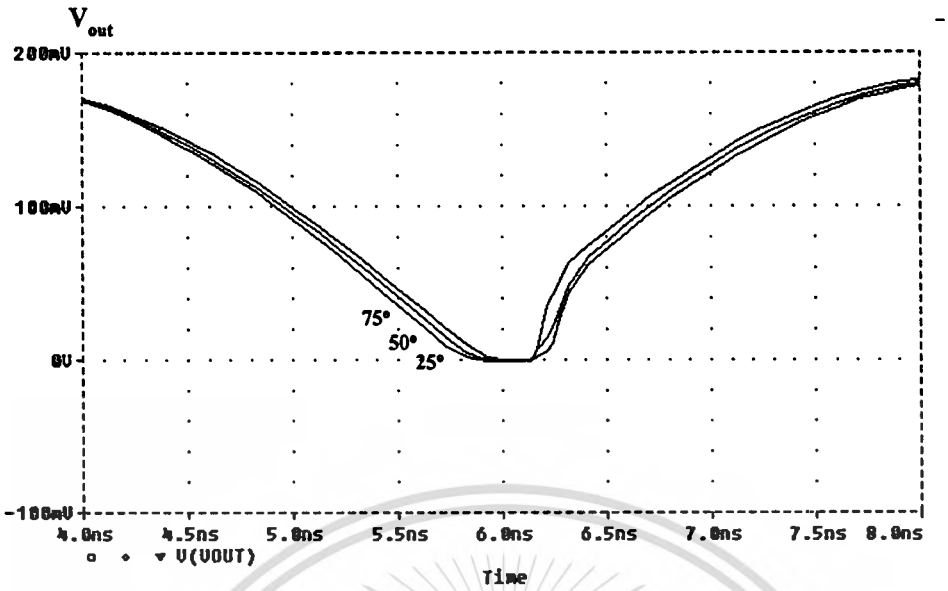
Figure 4.16 Operation of the proposed full-wave rectifier of a frequency 1MHz at different temperature when used CMOS diode: (a) full-wave output, (b) zero crossing regions.

Figure 4.18 shows the output waveform of the proposed full-wave rectifier at temperature of 25°C, 50°C and 75°C when the circuit of figure 4.5 is compensated with DC current source. Figure 4.19 shows the output waveform at temperature of 25°C, 50°C and 75°C, for the case that V_{B2} is 0.8V. It is clear that the temperature compensated with the DC current source is a good technique. However, it is a cause of decreasing precision at high frequency. If compare the results of figure 4.18 with figure 4.19, it was obvious that the results of the proposed rectifier without temperature compensation as shown in figure 4.19 has a better shape than the proposed rectifier with temperature compensation as shown in figure 4.18. The high-frequency response of the full-wave rectifier circuit is shown in figure 4.20. The cutoff frequency as simulated is about 250MHz.

Figure 4.17 Temperature compensated by using current biasing technique proposed by Hayatleh *et al.* [15].

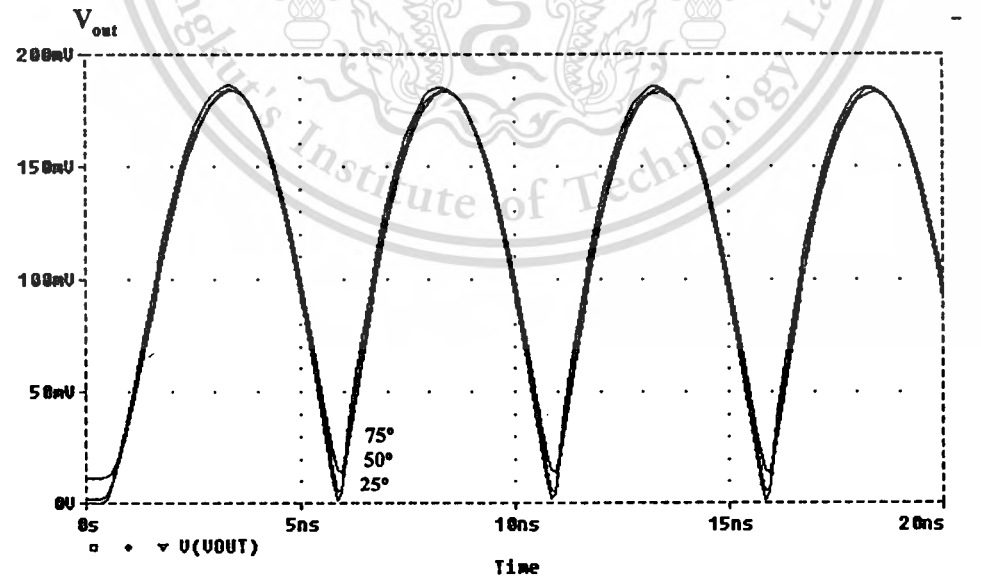


(a)

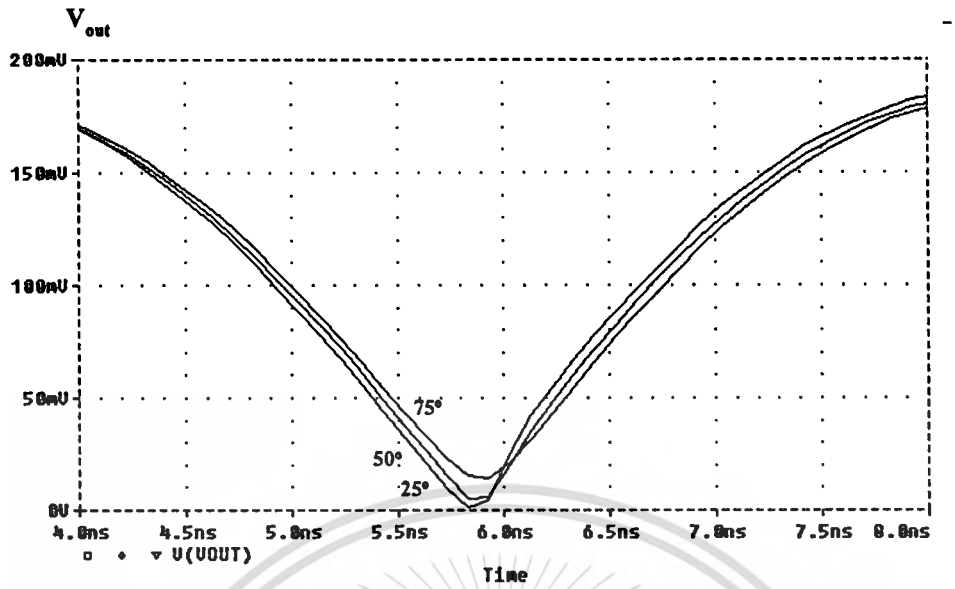


(b)

Figure 4.18 Operation of the proposed full-wave rectifier of a frequency 100MHz at different temperatures with temperature compensated: (a) full-wave output, (b) zero crossing regions.



(a)



(b)

Figure 4.19 Operation of the proposed full-wave rectifier of a frequency 100MHz at different temperatures without temperature compensated: (a) full-wave output, (b) zero crossing regions.

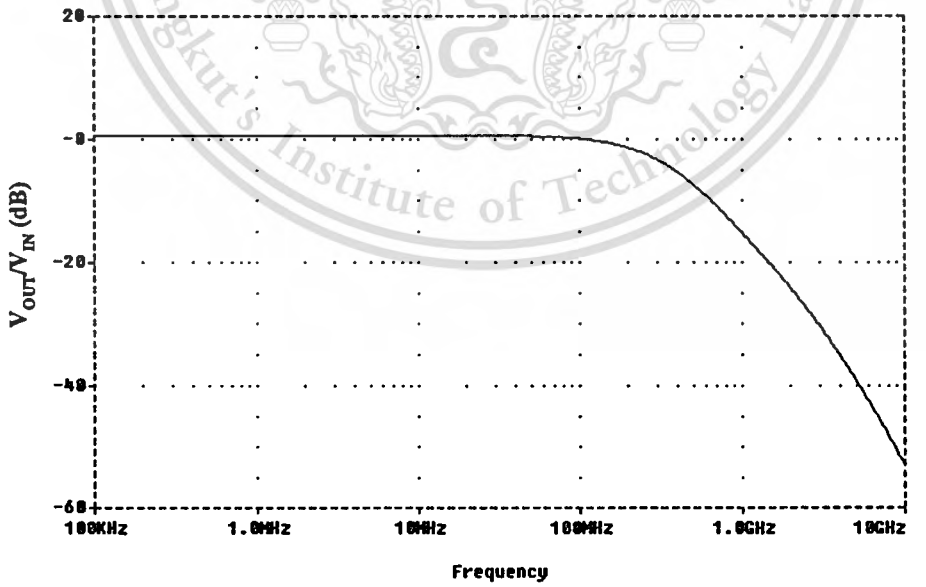


Figure 4.20 Simulated for high-frequency response.

4.7. Conclusion

This work proposes the design of a high frequency and high precision CMOS full-wave rectifier that operates in the current domain. The proposed rectifier is based on FDIO-OTA. However, with the different circuit structure, the proposed rectifier yields features superior to that of the previously reported full-wave rectifier in view of the voltage employed, the high precision, the number of devices, the operating frequency, the temperature stability, and suitability for IC fabrication. The proposed rectifier uses a ±5V supply voltage and produces an input operating ranging from -500mV to 500mV. In addition, its operating frequency is up to 200MHz (simulation result with 0.5μm CMOS model obtained through MIETEC). The simulated frequency response of the proposed circuit is shown in figure 4.19. It is should be noted that the bandwidth about 250MHz is observed. The proposed full-wave rectifier uses the MOS transistor to convert the output current to output voltage which is suitable for a high impedance load. The features of the proposed full-wave rectifier are as follows: (i) it can rectify the small input signal; (ii) it operates at high frequency range; (iii) it is more suitable structure for IC fabrication because of the absence of external resistors.

4.8. References

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CHAPTER 5
LOW-VOLTAGE CMOS CURRENT MULTIPLIER

A compact low-voltage four-quadrant CMOS current multiplier circuit is presented. The core of the circuit is the simple CMOS current mirrors, which leads to operate from low-voltage power supply. The realization method using the quarter-square technique based on the use of the squarer and copy current configurations. This proposed circuit uses the dimension of all CMOS transistors are equal, without the passive component and current source, easily structure which also very suitable for IC implementation. Simulated multiplier performance with a 0.5μm CMOS model using a 1.5V supply voltage demonstrate the input current range of this multiplier circuit is ±10μA and bandwidth of about 200MHz. The experimental results of proposed circuit confirm theoretical analysis are carried out.

5.1. Introduction

The analog multiplier is one of the important building blocks in VLSI communication systems, which can be applied to frequency mixers, variable gain amplifiers, adaptive filters, phase-locked loops and many other signal processing circuits. Other applications such as neural network systems require multiplier cells to be modular with low power consumption. Low-voltage and low-power analog CMOS design solutions are necessary for high performance mixed-signal integrated circuits. Several techniques of implementing CMOS analog multiplier circuits suitable for low-voltage, low-power applications have been reposted. They are the technique based on MOS transistors operating in either the weak inversion region [1]-[5] or strong inversion region [6]-[11], the use of floating-gate MOS transistors technique [12]-[14]. The multiplier based on the MOS transistor operating in the weak inversion region limits the high-frequency response and very sensitive to device mismatches. The floating-gate MOS transistor based multiplier enjoys the use of minimum numbers of active devices However, it is required the special processing and calibration steps associated.

At present, because of the main frequency of wider bandwidth, greater linearity and simple circuitry compared with their voltage-mode counter part, current-mode

circuits have been received growing interest in analog signal processing circuits. Many circuits of current-mode CMOS multiplier circuits have been presented in the literature [5]-[8].

This repost proposes a simple and compact low-voltage four-quadrant current multiplier circuit that employs the simple current mirrors with avoid a stack configuration, minimum aspect ratio of MOS transistor and without passive component. The circuit is operated in current-mode. The current-mode operation of the circuit gives low-voltage and low-power and good frequency response. To simulate the proposed circuit by using PSPICE and the experiment can be carried out. This circuit is suitable for low-voltage current-mode IC application.

5.2. Circuit descriptions

Four-quadrant multiplier can be implemented based on different techniques. One previous principles of operation is based on well-known identity [5]-[7]:

$$(X+Y)^2-(X-Y)^2=4XY \tag{5.1}$$

Equation (5.1) is called the quarter square. The disadvantages of this technique are that there are a lot of number of used devices and the required differential input signal. Thus, the square-difference technique [8], [11] has been proposed to improve the equation form, its equation can be written as

$$(X+Y)^2-X^2-Y^2=2XY \tag{5.2}$$

The advantages are that the numbers of used devices decrease and single ended input signal are required. This repost also employs the latter technique. The proposed circuit composes of a squarer circuit and two squarer and copy current circuits as shown in figure 5.1 and figure 5.2, respectively. Two circuits are based on simple current mirrors, so the voltage power supply can be given as follow as $V_{DD}>V_{THN}+|V_{THP}|$ for operating in strong inversion. In figure 5.1, assume all MOS transistors are operated in saturation region with source-body-connected. The drain current of transistors M5 and M1 can be expressed as

$$I_{D5} = \frac{K_P}{2}\left(V_{GS5} - |V_{THP}|\right)^2 \tag{5.3.1}$$

$$I_{D1} = \frac{K_N}{2}\left(V_{GS1} - V_{THN}\right)^2 \tag{5.3.2}$$

where K_P and K_N are the transconductance parameters, V_{THP}, V_{THN} are the threshold voltages and V_{GS5}, V_{GS1} are the gate-to-source voltage of MOS transistors M5 and M1, respectively. Let $V_{GS1}=V_{in}$, then

$$I_{D5} = \frac{K_P}{2}\left(V_{DD} - V_{in} - |V_{THP}|\right)^2 \tag{5.4.1}$$

$$I_{D1} = \frac{K_N}{2}\left(V_{in} - |V_{THP}|\right)^2 \tag{5.4.2}$$

M1-M2 and M5-M6 are current mirrors with connected in back-to-back. The positive direction is selected to be outwards, so it can be written as

$$I_{D1} = I_{D5} - I_{in} \tag{5.5}$$

Substitute (5.4.1) and (5.4.2) into (5.5), it obtain

$$\frac{K_N}{2}\left(V_{in} - V_{THN}\right)^2 = \frac{K_P}{2}\left(V_{DD} - V_{in} - |V_{THP}|\right)^2 - I_{in} \tag{5.6}$$

Let $K_P=\mu_P C_{OX}(W/L)=K_N=\mu_N C_{OX}(W/L)=K$, the relationship of I_{in} and V_{in} is

$$V_{in} = \frac{V_{DD} - |V_{THP}| + V_{THN}}{2} - \frac{I_{in}}{K\left(V_{DD} - |V_{THP}| - V_{THN}\right)} \tag{5.7}$$

Substitute (5.7) into (5.4.1) and (5.4.2), yields

$$I_{D1} = \frac{K}{2}\left(\frac{V_{DD} - |V_{THP}| - V_{THN}}{2} - \frac{I_{in}}{K\left(V_{DD} - |V_{THP}| - V_{THN}\right)}\right)^2 \tag{5.8}$$

$$I_{D5} = \frac{K}{2}\left(\frac{V_{DD} - |V_{THP}| - V_{THN}}{2} + \frac{I_{in}}{K\left(V_{DD} - |V_{THP}| - V_{THN}\right)}\right)^2 \quad (5.9)$$

In figure 5.1, when $I_{in}>0$, it is fed through M1 and then is mirrored to the drain current of M2 as I_{D2}, whereas $I_{in}<0$ it is fed through M5 and then is mirrored to the drain current of M6 as I_{D6}, this I_{D6} is again mirrored to the drain current of M3 as I_{D3}. Assume MOS transistors M1 to M6 are well matched. Thus, $I_{D2}=I_{D1}$ and $I_{D3}=I_{D5}$, the output current of squarer circuit is

$$I_{oq} = I_{D2} + I_{D3} \quad (5.10.1)$$

Substitute (5.8) and (5.9) into (5.10.1), then

$$I_{oq} = \frac{I_{in}^2}{K\left(V_{DD} - |V_{THP}| - V_{THN}\right)^2} + \frac{K\left(V_{DD} - |V_{THP}| - V_{THN}\right)^2}{4} \quad (5.10.2)$$

The figure 5.1 can be modified to be figure 5.2, this is a circuit both square and copy current signals into a single circuit. The output current of the copy current circuit is

$$I_{oc} = -I_{in} \quad (5.11)$$

The proposed four-quadrant current multiplier circuit is shown in figure 5.3. It is consists of two squarer and copy circuits and a squarer circuit. First squarer and copy current circuit creates $(I_X)^2$ and I_X signal, second squarer and copy current circuit creates $(I_X)^2$ and I_Y signal. The current I_X and I_Y are summed, and then are sent to the squarer circuit. Thus, the output current of the squarer circuit is; $(I_X+I_Y)^2$. The multiplication can be achieved by subtracting between $(I_X)^2+(I_Y)^2$ and $(I_X+I_Y)^2$, therefore the output current of the current multiplier circuit in figure 5.3 can be expressed as

$$I_{out} = \frac{-2I_X I_Y}{K\left(V_{DD} - |V_{TP}| - V_{TN}\right)^2} + \frac{K\left(V_{DD} - |V_{TP}| - V_{TN}\right)^2}{4} \quad (5.12)$$

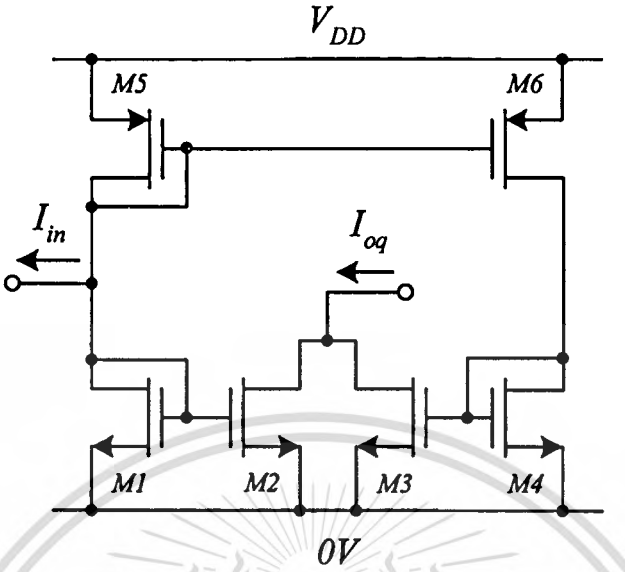

Figure 5.1 The squarer circuit.

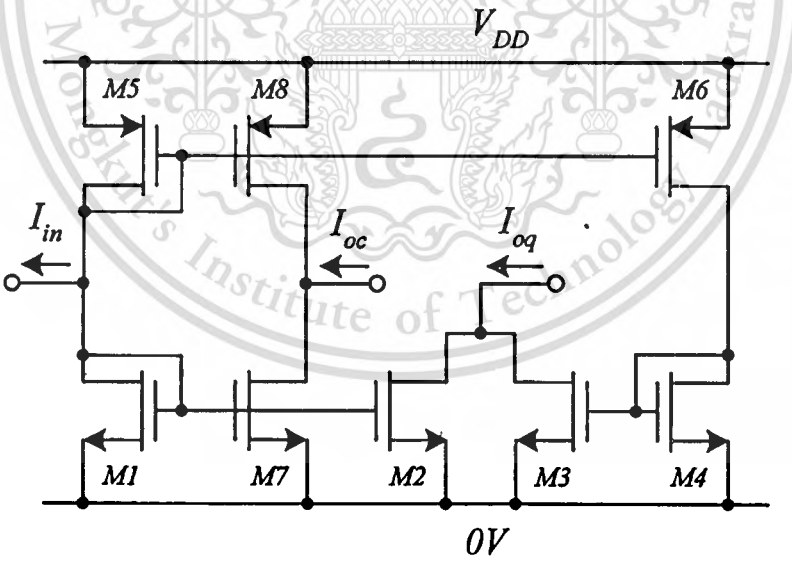

Figure 5.2 The squarer and copy current circuit.

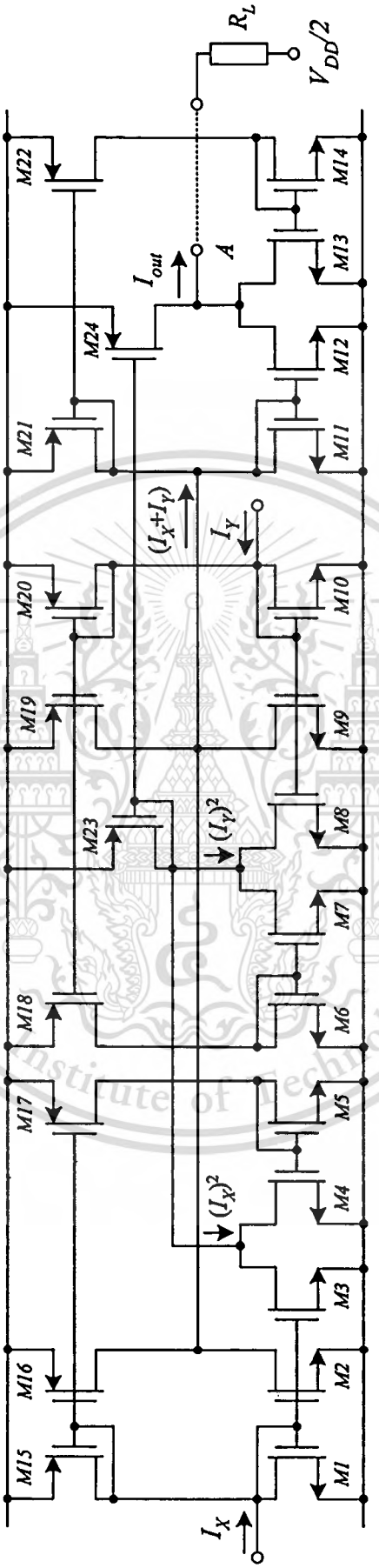

Figure 5.3 Proposed low-voltage current multiplier.

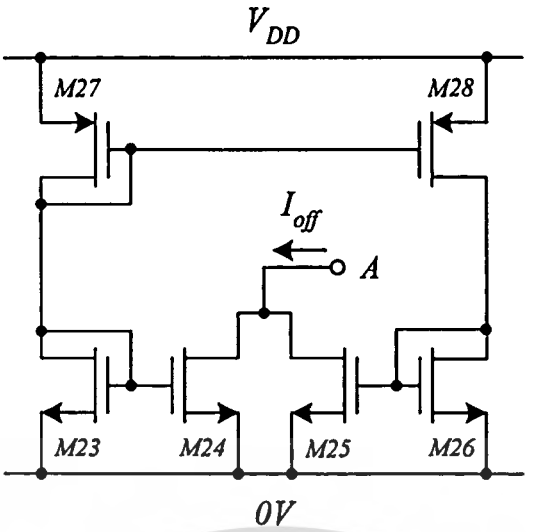

Figure 5.4 The circuit used for canceling the constant current.

Equation (5.12), it note that I_{out} is a product of I_X and I_Y with summed of constant current term; $(K(V_{DD}-|V_{THP}|-V_{THN})^2)/4$. Undesired term can be cancelled with output offset current by connecting between node A and 0V. Figure 5.4 is the circuit used for canceling the constant current. From equation (5.10.2), let $I_{in}=0$, the output offset current (I_{offset}) can be written as

$$I_{offset} = \frac{K(V_{DD} - |V_{THP}| - V_{THN})^2}{4} \tag{5.13}$$

Thus, (5.12) becomes,

$$I_{out} = \frac{-2I_X I_Y}{K(V_{DD} - |V_{THP}| - V_{THN})^2} \tag{5.14}$$

The input currents of proposed current multiplier are separated into two current components. When $I_{in}>0$, it will feed through the NMOS current mirror, whereas $I_{in}<0$, it will feed through the PMOS current mirror. To evaluate this current, the circuit in figure 5.2 is considered again. If the drain conductance coefficients and absolute value of the threshold voltage of M1 and M5 are equal, the current component I_{D1} and I_{D5} are given follows

$$I_{D1} = \left(\frac{4I_q - I_{in}}{4\sqrt{I_q}} \right)^2 \tag{5.15}$$

$$I_{D5} = \left(\frac{4I_q + I_{in}}{4\sqrt{I_q}} \right)^2 \tag{5.16}$$

where I_{D1} and I_{D5} are the drain currents of M1 and M5, respectively, $-4I_q \le I_{in} \le 4I_q$. For $I_{in} < -4I_q$, $I_{D1}=I_{in}$ and $I_{D5}=0$. For $I_{in} > 4I_q$, $I_{D5}=I_{in}$ and $I_{D1}=0$. Therefore, the relationship $I_{in}=I_{D1}+I_{D5}$ is always wanted. The above mentioned condition is the linear input current (I_{in}) to the linear input voltage (V_{in}), its characteristic given by $I_{in}=4(KI_qV_{in})^{1/2}$. This is obtain for the input current ranges of $-4I_q \le I_{in} \le 4I_q$, where K is the drain conductance coefficient of M1 and M5 and I_q is the quiescent current ($I_{in}=0$).

5.4. Performance analysis

Our previous circuit performance analysis has been based on the assumptions that the transistors have characteristics are perfectly square-law characteristic. However, in a practical realization, several non-idealities that contribute to error from non-ideal performance are present. The major factors to be considered are the second-order effect of transistor, mismatches analysis and high-frequency limitation.

5.4.1. Second-order effect

The previous description of the current multiplier neglected the second-order effect such as the body effect, channel-length modulation, mobility degradation. In practically, these second-order effects will degrade the circuit performance. The body effect can be reduced by source-bulk-connected. The channel length modulation effect can be improved by using the long channel length devices, but that is a cause of increasing parasitic capacitance, which is limit the bandwidth of the circuit.

In this section, there are two major effects will be discussed. The channel-length modulation and mobility reduction will be analyzed.

5.4.1.1. Channel-length modulation

For MOS transistor operates in saturation region, the first-order approximation square-law characteristic including the channel-length modulation (λ) can be written as [15]-[16]

$$I_D = \frac{K}{2}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{5.17.1}$$

when $V_{DS}=V_{GS}-V_{TH}$. Substitution V_{DS} term into (5.17.1), we have [11]

$$I_D = \frac{K}{2}(V_{GS} - V_{TH})^2 + \frac{\lambda K}{2}(V_{GS} - V_{TH})^3 \tag{5.17.2}$$

Equation (5.17.2) represents the drain current included the channel-length modulation. The first term is a quadratic term. The last term is a third-order term that will cause of first and third harmonic distortion. By substituting (5.17.2) into (5.10.2), the output current of squarer circuit can be rewritten as

$$I_{oq} = \frac{I_{in}^2}{KA^2} + \frac{KA^2}{4} - \frac{3\lambda I_{in}^2}{2KA} - \frac{\lambda KA^3}{8} \tag{5.18}$$

where $A=V_{DD}-|V_{THP}|-V_{THN}$. According to (5.18) and (5.12), it can be

$$I_{out} = \frac{-2I_X I_Y}{KA^2} + \frac{KA^2}{4} + \frac{3\lambda I_X I_Y}{KA} - \frac{\lambda KA^3}{8} \tag{5.19}$$

From equation (5.19) indicates that the channel-length modulation will be dominant in the first and third harmonics distortion.

5.4.1.2. Mobility degradation

The drain current of MOS transistor including the mobility degradation can be modeled as [15]-[16]

$$I_D = \frac{K(V_{GS} - V_{TH})^2}{1 + \theta(V_{GS} - V_{TH})} \tag{5.20}$$

where θ is the mobility degradation parameter which has a value of about 0.1~ $0.001V^{-1}$. By using Taylor series, (5.20) can be written as

$$I_D = K(V_{GS} - V_{TH})^2\left(1 - \theta(V_{GS} - V_{TH}) + \theta^2(V_{GS} - V_{TH})^2 .....\right) \tag{5.21}$$

For a calculation, the first order of θ was used only whereas the high-order terms of θ were neglected. By substituting (5.21) into (5.8) and (5.9), (5.10.2) can rewritten as

$$I_{oq} = \frac{I_{in}^2}{KA^2} + \frac{KA^2}{4} - \frac{3\theta I_{in}^2}{2AK} - \frac{\theta KA^3}{8} \tag{5.22}$$

Thus, (5.12) can be rewritten as

$$I_{out} = \frac{-2I_X I_Y}{KA^2} + \frac{KA^2}{4} + \frac{3\theta I_X I_Y}{AK} - \frac{\theta KA^3}{8} \tag{5.23}$$

Equation (5.23) indicates the mobility degradation effect will be dominant in the first-order harmonic distortion.

5.4.2. Mismatches analysis

From (5.14), the mismatch contributes to error from the ideal output current of the multiplier are the transconductance parameter mismatch. In previous, the transfer function assume K_N and K_P are equaled, it is harder to ensure that K_N=K_P. Assume the transconductance parameter mismatch of NMOS against the PMOS transistor is defined as $\Delta K = K_N - K_P$. It can be given the transconductance parameters of NMOS and PMOS transistors are $K+\Delta K/2$ and $K-\Delta K/2$, respectively. Substituting $K+\Delta K/2$ and $K-\Delta K/2$ into (5.8) and (5.9), respectively, the output current I_{oq} can be rewritten as

$$I_{oq} = \frac{I_{in}^2}{K\left(V_{DD} - |V_{THP}| - V_{THN}\right)^2} + \frac{K\left(V_{DD} - |V_{THP}| - V_{THN}\right)^2}{4} - \frac{\Delta K}{K}\frac{I_{in}}{2} \qquad (5.24)$$

Again, according (5.24), (5.10.2) included the transconductance parameter mismatch can be rewritten as

$$I_{out} = \frac{-2I_X I_Y}{K\left(V_{DD} - |V_{THP}| - V_{THN}\right)^2} - \frac{K\left(V_{DD} - |V_{THP}| - V_{THN}\right)^2}{4} + \frac{\Delta K}{K}\frac{I_X}{2} + \frac{\Delta K}{K}\frac{I_Y}{2} \qquad (5.25)$$

Equation (5.25) implies that the mismatch causes a change of slope and an offset in the DC characteristics.

5.4.3. Frequency response analysis

The frequency response of the circuit can be observed by using small-signal equivalent analysis. If MOS transistor operates in saturation region, the gate-source capacitance C_{gs} is a large capacitance, whereas other capacitances are neglected. For high frequency response, the major high-frequency limitation of the proposed current multiplier results from the bandwidth of three current mirrors, which is one positive current mirror and two negative current mirrors. If consider only input I_X, one positive current mirror is M1-M2, and two negative current mirrors are M15-M16 and M23-M24. The three dominant poles P_1(M1-M2), P_2(M15-M16) and P_3(M23-M24) of three current mirrors are given by

$$P_1 = \frac{g_{m1}}{2\pi(C_{gs1} + C_{gs2})} \qquad (5.26)$$

$$P_2 = \frac{g_{m15}}{2\pi(C_{gs15} + C_{gs16})} \qquad (5.27)$$

$$P_3 = \frac{g_{m23}}{2\pi(C_{gs24} + C_{gs24})} \qquad (5.28)$$

where C_{gsi} is the gate-to-source capacitance and g_{mi} is the transconductance of the MOS transistor Mi. For example, if the small signal parameters C_{gs} and g_m obtained from the simulation are $g_{m1} = g_{m2} = 4.78\times10^{-5}AV^{-1}$, $g_{m15} = g_{m16} = 4.56\times10^{-5}AV^{-1}$, g_{m23}

$= g_{m24} = 8.8\times10^{-5}AV^{-1}$, $C_{gs1} = C_{gs2} = 4.24\times10^{-15}F$, $C_{gs15} = C_{gs16} = 1.73\times10^{-14}F$ and $C_{gs23} = C_{gs24} = 1.73\times10^{-14}F$. The high-frequency of poles P_1, P_2 and P_3 will be located at approximately 897MHz, 209MHz and 404MHz, respectively. It can be evaluated that the major high-frequency limitation of the proposed current multiplier results from the bandwidth of the negative current mirrors.

5.3. Results

5.3.1. Simulation results

The following simulation results are obtained using PSPICE with level 3 model of 0.5μm CMOS parameter obtained through MIETEC as listed in Table 2.2. The aspect ratios of transistors are 2μm/1μm for M1 to M14 and 8.7μm/1μm for M15 to M24. The simulation conditions are single power supply voltage 1.5V, R_L = 1kΩ. Figure 5.5 shows the DC transfer curves of the multiplier circuit. The output current swing between -5μA and 5μA, while the input current has a linear differential input range up to ±10μA are demonstrated. Figure 5.6 shows the frequency responses and phase characteristic of proposed current multiplier in figure 5.3, where a bandwidth of about 200MHz was observed. Figure 5.7 shows the total harmonic distortion (THD) on 5kHz, 50kHz and 5MHz are plotted.

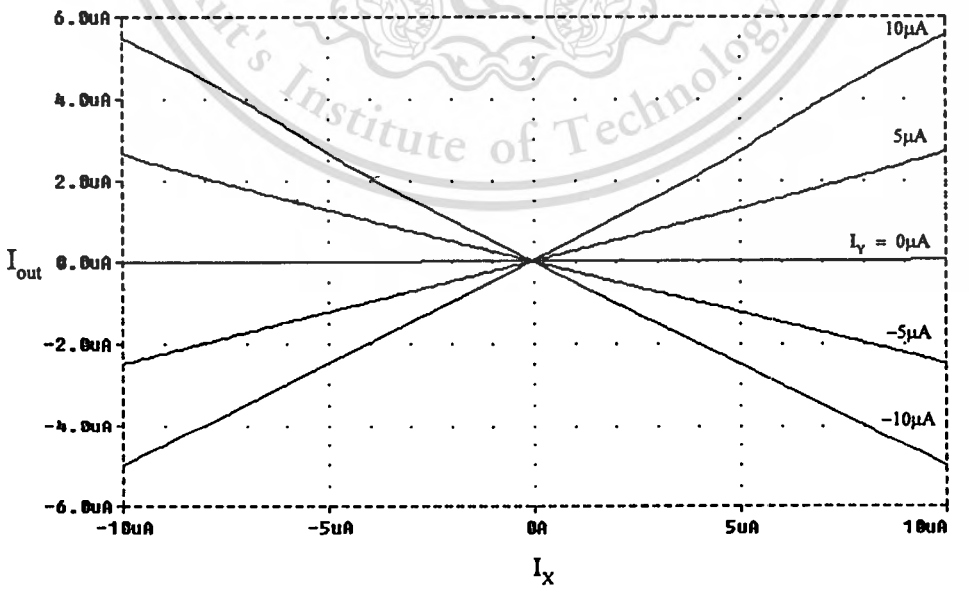

Figure 5.5 Simulated DC transfer characteristic.

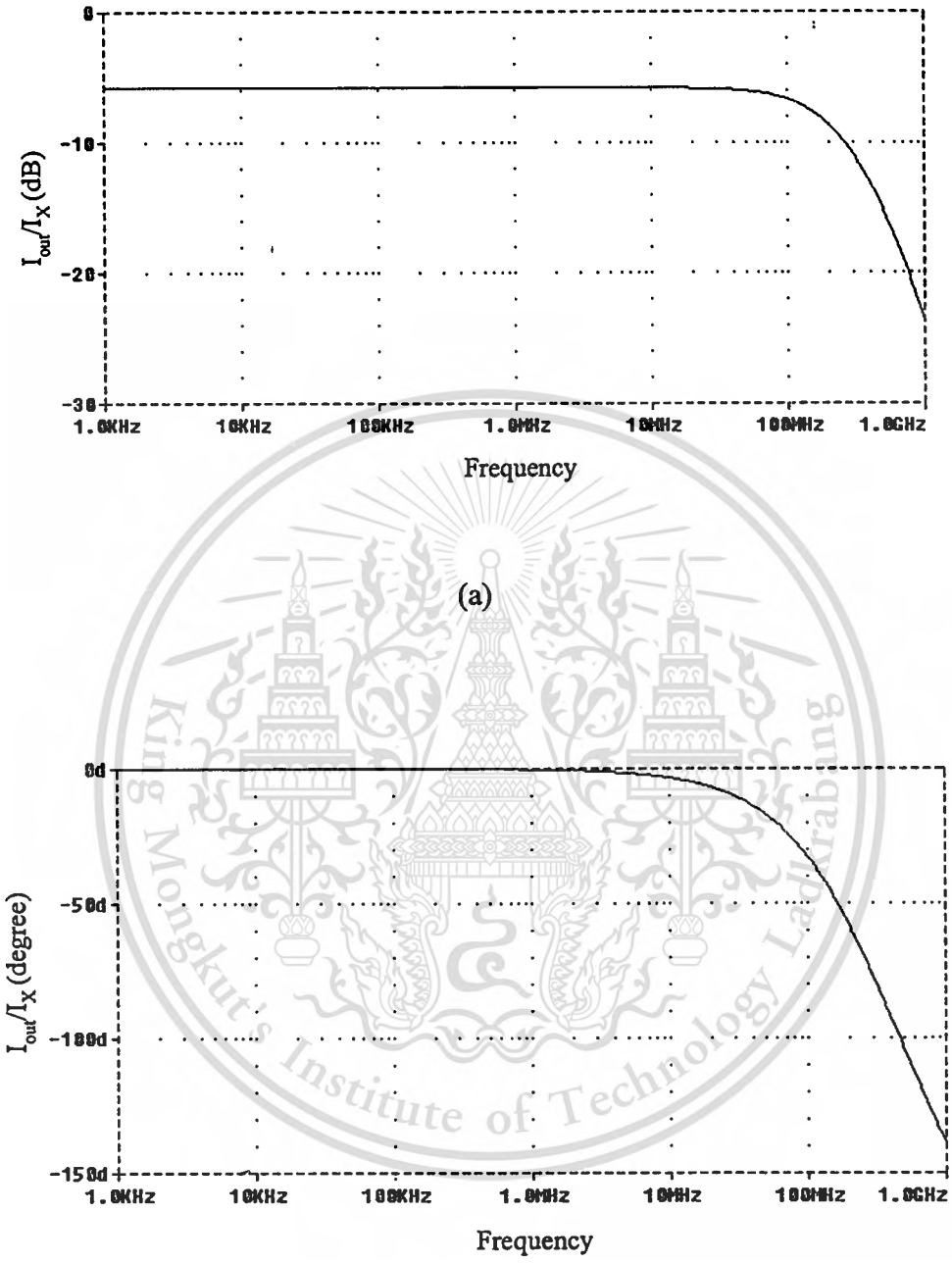

Figure 5.6 Response characteristics: (a) frequency response, (b) phase response.

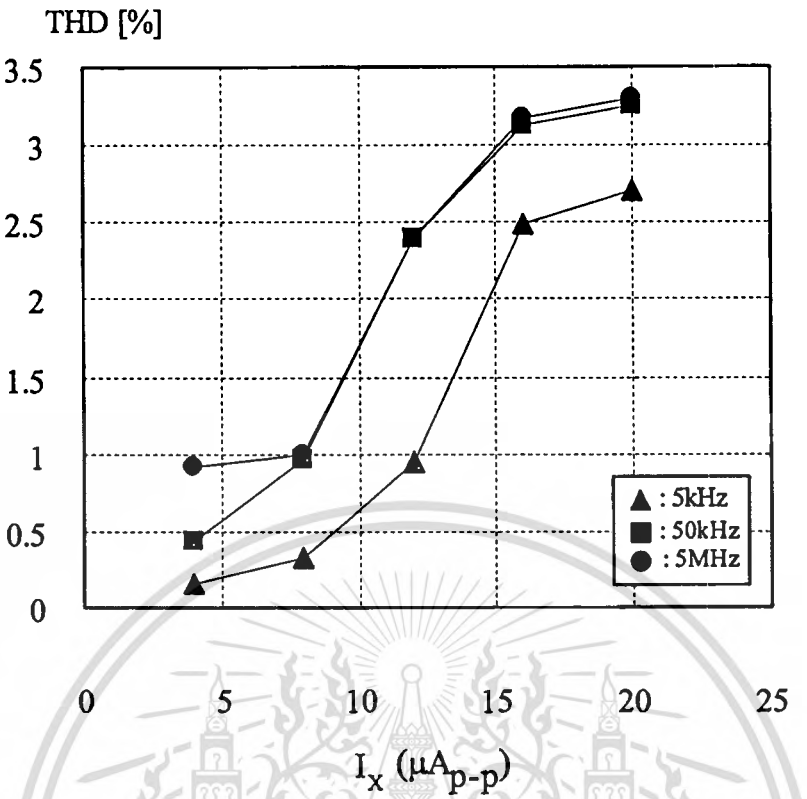

Figure 5.7 Simulated total harmonic distortion.

5.3.2. Experimental results

The circuit of figure 5.3 is prototyped in the form of complementary MOS transistor pair (MC14007). In this experiment, $V_{DD} = -V_{SS} = 1.8V$ and $R_L = 10k\Omega$ where used for the multiplier. A voltage to current converter (V-I converter) is added in front of the multiplier in order to be input signals as shown in figure 5.8. If assume $V_X = V_Y = V_{in}$, $R_X = R_Y = R_{in}$, and $I_X = I_Y = I_{out}$, the output current of CCIIs can be written as

$$I_{out} = \frac{V_{in}}{R_{in}} \tag{4.29}$$

Let $R_{in} = 3k\Omega$ and $V_{in} = 2V_{P-P}$, the output current I_{out} is approximately equal to $66.6\mu A_{P-P}$.

Figure 5.9 shows the performance of the multiplier as frequency doublers, when the input signals are two in-phase 10kHz triangular wave $2V_{P-P}$ from function

generator (lower trace, 1V/div). The output is a triangular wave of twice the input signal frequency (upper trace 50mV/div). Figure 5.10 shows the multiplier being used for AM modulation with inputs of $2V_{P-P}$ for a 1kHz triangular wave (lower trace, 2V/div) and $2V_{P-P}$ for a 18kHz sinusoidal from function generators. Measured output (upper trace) is 200mV/div. Horizontal scale is 250μs/div.

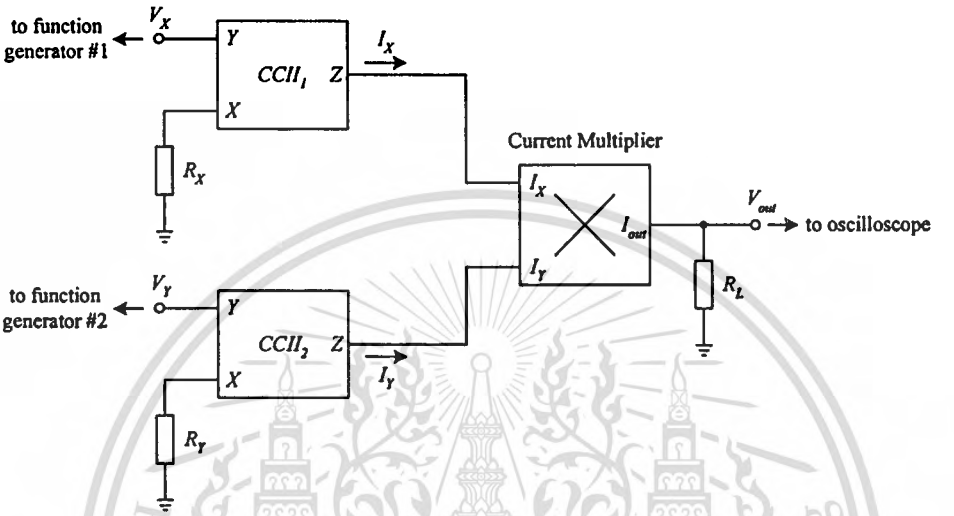

Figure 5.8 Block diagrams used for experimentation.

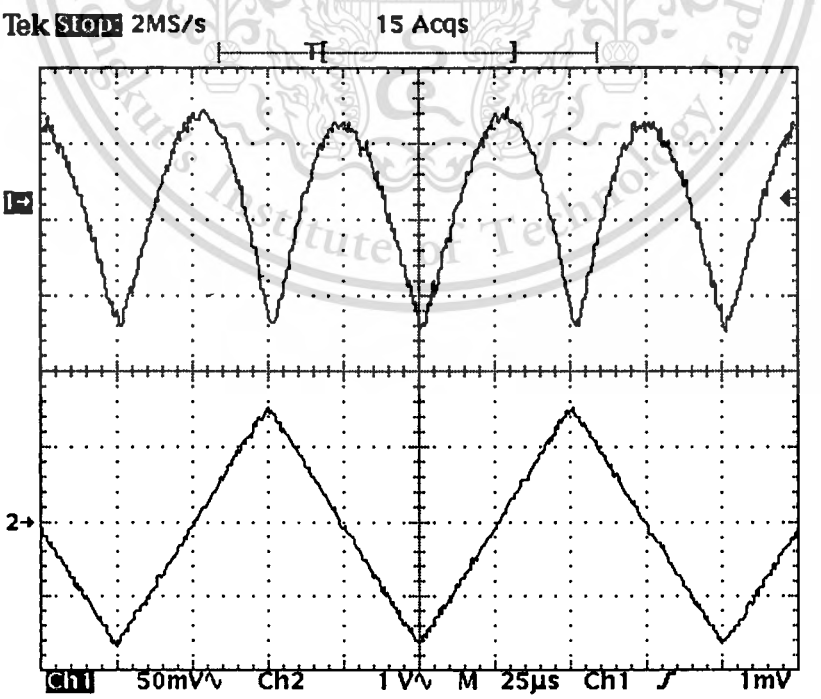

Figure 5.9 Measured frequency doublers with a 10kHz triangular wave inputs.

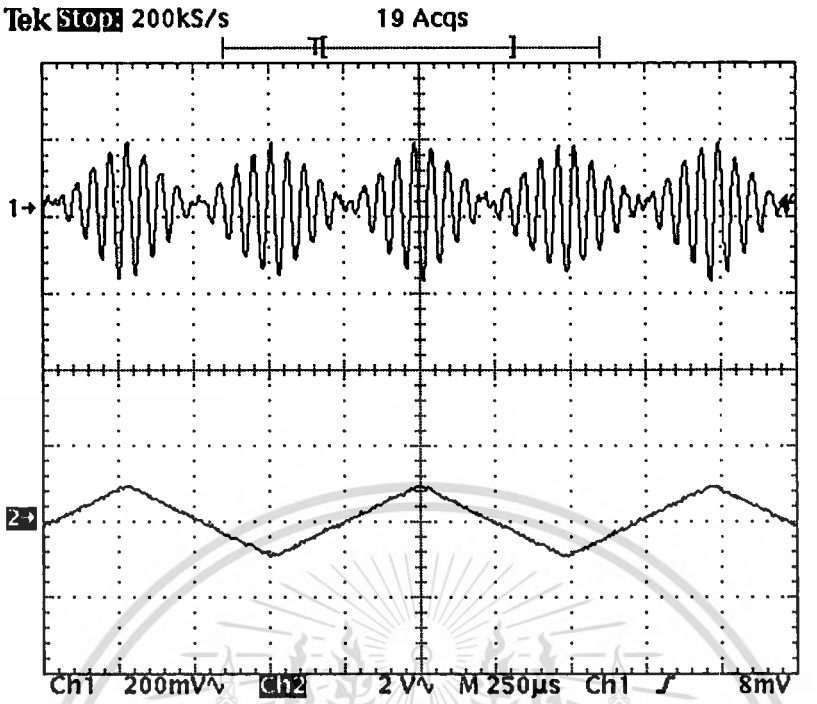

Figure 5.10 Measured output waveform of a 18kHz sinusoid and a 1kHz triangular wave.

Table 5.1 Simulated result parameters of proposed CMOS current multiplier.

Parameter	Value
Technology	0.5µm CMOS
Supply voltage	1.5V
Input current range : I_X : I_Y Output current range	±10µA ±10µA 10µA
THD@5kHz:12μA_{P-P}	0.94%
Bandwidth (-3dB)	207MHz
Offset current	-53nA
Power consumption	110µW

5.5. Conclusions

The low-voltage four-quadrant current multiplier is proposed. The design is based on the square-difference technique. This proposed circuit has distinguished in used low-voltage power supply which is very low power consumption, no passive element, less transistor dimension and simple circuitry. The structure based on simple current mirror that offer it suitable for IC implementation. The simulation and experimental results have been shown to confirm the operation of the proposed multiplier circuit. All simulation parameters of proposed circuit are shown in Table 5.1.

5.6. References

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CHAPTER 6
VERSATILE CLASS-AB ANALOG MULTIPLIER

In this chapter, the author presents a versatile class-AB CMOS four-quadrant analog multiplier circuit. Three dual translinear loops and current mirrors are the basic building blocks in this realization scheme. The proposed multiplier is carried in current-mode, thus the circuit gives wide input range and wide-bandwidth response for a low consumption. The major advantages over the other analog multiplier are; this circuit has single ended inputs; the analog multiplier based on dual translinear loops operating in class-AB mode which make them interesting for low-voltage and low-power applications; and its output can be the product of two signal currents, the product of two signal voltages, or the product of a signal current and a signal voltage. The simulation results of proposed analog multiplier demonstrate a input current range is ±20μA, a -3dB bandwidth of about 19MHz, a maximum power consumption of about 0.46mW, and temperature compensated when two supply voltage of -1.5V and +1.5V and a quiescent current of 10μA in a 0.5μm CMOS model are obtained. Operation of proposed analog multiplier was also confirmed through an experiment using CMOS transistor array.

6.1. Introduction

Analog multiplier circuits are important nonlinear analog signal processing function finding application of a wide variety in adaptive filtering, modulation, frequency translation, automatic gain control, neural network, etc. At present, the power consumption is a key parameter in the designing of high performance mixed signal integrated circuits. The CMOS technology is widely recognized as the most desirable technology for ICs implementation [1]. Low power consumption analog CMOS design solutions are necessary for high performance mixed-signal integrated circuits. In the past, some CMOS multiplier circuits have been developed [2]-[6]. However, they are not suitable for applying to low power consumption applications. Several techniques of reducing power consumption have been reported. They are the use of floating-gate MOS transistors technique [7]-[9], based on bulk driven MOS transistors technique [10]-[11], technique based on MOS transistors operating in

subthreshold mode [11]-[13], and technique based on employs MOS transistors operating in class-AB mode [14]-[15]. However, these analog multiplier circuits have been developed with the output can be product of either two voltage signals or two current signals.

In this section, the author presents a versatile analog multiplier circuit based on dual translinear loops. By using dual translinear loop, the inputs of proposed analog multiplier circuit can be voltages and/or currents; hence it properly combine a voltage multiplier, a current multiplier, a current and voltage multiplier into a circuit (it can be called the versatile analog multiplier circuit [16]-[17]). Class-AB technique is chosen for reducing the power consumption. This technique yields the advantages.

(i) The special processing and calibration steps associated with floating gate devices are avoided.

(ii) The input transistor pair gain reduction and input impedance reduction associated with a bulk driven avoided.

(iii) The high frequency response reduction associated with device operate in subthreshold mode are avoided.

(iv) Used of standard digital CMOS topology.

The proposed analog multiplier exhibits wide bandwidth, high temperature stability and high speed. This design has single ended inputs which no requires additional hardware and consequently more silicon area. Thus, it can be applied in a large system. PSPICE simulation and experimental results will be confirmed to demonstrate the performance of the proposed circuit.

6.2. Circuit descriptions

6.2.1. Class-AB CMOS squaring circuit

An MOS version of a dual translinear loop for realizing the proposed versatile analog multiplier is shown in figure 6.1. MOS transistors M1 to M4 form a dual translinear loop and MOS transistors M5 and M6 form a current mirror. Generally, the drain current of an MOS transistor operated in saturation region by neglecting second order effect such as mobility reduction and channel-length modulation can be expressed as [1]

$$I_D = K(V_{GS} - V_{TH})^2 \tag{6.1.1}$$

or $$V_{GS} = V_{TH} + \sqrt{\frac{I_D}{K}} \quad (6.1.2)$$

where $K=0.5\mu_O C_{OX}(W/L)$ is the transconductance parameter, μ_O is the electron mobility, C_{OX} is the gate oxide capacitance per unit area, W/L is the transistor aspect ratio, V_{GS} is the gate-to-source voltage and V_{TH} is the threshold voltage of the MOS transistor.

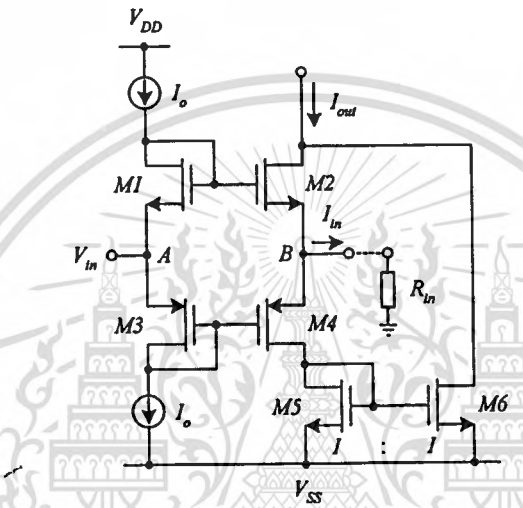

Figure 6.1 Basic building blocks.

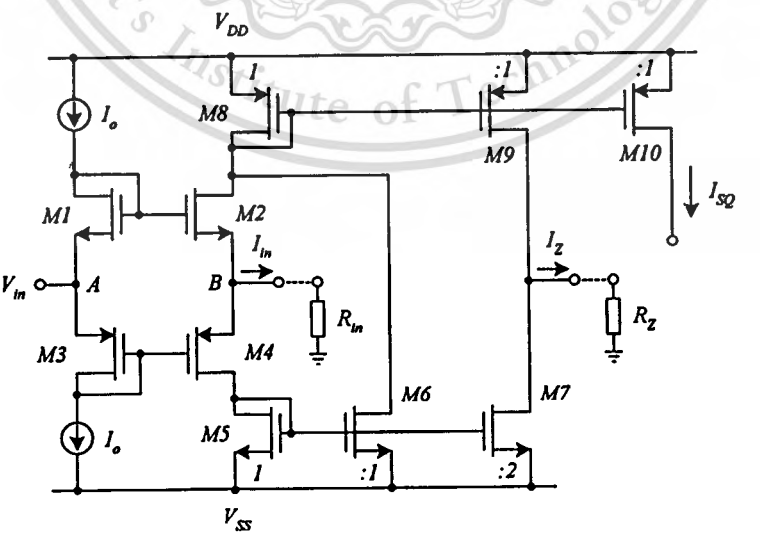

Figure 6.2 Squaring and copy current into a single circuit.

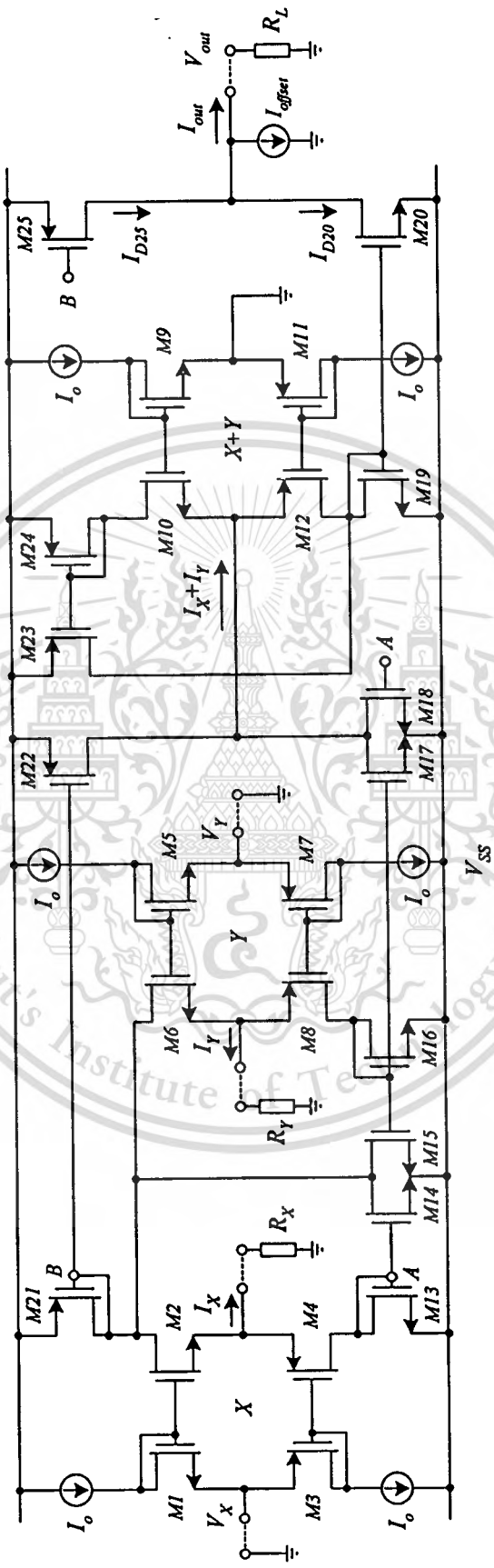

Figure 6.3 Proposed versatile class-AB analog multiplier.

Consider MOS transistors M1 to M4, summing the gate-source voltages around the loop can be given [20]

$$V_{GS1} + V_{GS3} = V_{GS2} + V_{GS4} \tag{6.2}$$

Assuming MOS transistors M1 to M4 form a dual translinear loop in figure 6.1 are biased in the saturation region, all MOS transistors are well matched, and the same values of the transconductance parameters, that is K_N=K_P, then using (6.1) and (6.2), the relationship of the currents I_{D2} and I_O, I_{D2} and I_{D4} in the loop can described as

$$2\sqrt{I_O} = \sqrt{I_{D2}} + \sqrt{I_{D4}} \tag{6.3}$$

The drain currents I_{D1} and I_{D3} are equal to the current source I_O. From class-AB principle [14]-[15], the currents I_{D2} and I_{D4} can be expressed as

$$I_{D2} = I_O - \frac{I_{in}}{2} + \frac{I_{in}^2}{16I_O} \tag{6.4}$$

and

$$I_{D4} = I_O + \frac{I_{in}}{2} + \frac{I_{in}^2}{16I_O} \tag{6.5}$$

The V_{in} is the input voltage at port Y, I_{in} is the input current at port X and R_X is the conversion resistance. Assume a current mirror, M5-M6, has a perfect unity current gain. The output current I_{out} of figure 5.1 can be written as

$$I_{out} = 2I_O + \frac{I_{in}^2}{8I_O} \tag{6.6}$$

From (6.6), this result is the current squarer of input signal, a basic building block of the class-AB CMOS analog multiplier. It should be noted that, when the input is a voltage. The signal will be applied at port Y. Since the dual translinear loop is also working as a voltage-to-current converter where V_{in}=V_X=V_Y [20] and R_{in} is the conversion resistance, the output current I_{out} of this case can be given by

$$I_{out} = 2I_O + \frac{V_{in}^2}{8R_{in}^2 I_O} \tag{6.7}$$

From equations (6.6) and (6.7), it can be noted that the input signal can be a voltage or a current. The circuit in figure 6.1 can be modified to combine a squarer and a copier into a single circuit while maintaining the class-AB mode, which is shown in figure 6.2. Assuming a current mirror, M8-M10, is well matched, thus it can be given as

$$I_{SQ} = 2I_O + \frac{I_{in}^2}{8I_O} \tag{6.8}$$

By setting the aspect ratio (W/L) of M5 twice of M7, I_Z can be expressed as

$$I_Z = I_{in} \tag{6.9}$$

The circuit shown in figure 6.2 is a circuit used for key building block of the propose class-AB analog multiplier.

6.2.2. Proposed versatile class-AB analog multiplier

The basic principle of the proposed multiplier is based on the square-difference identity: $(X+Y)^2-X^2-Y^2 = 2XY$. By using this equation, the proposed analog multiplier circuit can be shown in figure 6.3. It consists of the class-AB squaring circuits in figures 6.1 and 6.2. Three dual translinear loops and current mirrors were used. First loop, M1 to M4, is provided a squarer function: X^2, second loop, M5 to M8, is provided a squarer function: Y^2 and third loop, M9 to M12, is provided a squarer function: $(X+Y)^2$.

Assuming current mirrors, M21-M22, M25 and M19-M20 has a perfect unity current gain, thus

$$I_{D20} = 2I_O + \frac{(I_X + I_Y)^2}{8I_O} \tag{6.10}$$

and

$$I_{D25} = 4I_O + \frac{I_X^2 + I_Y^2}{8I_O} \tag{6.11}$$

From Kirchhoff's current law, it can be given

$$I_{out} = I_{D20} - I_{D25} + I_{off} \tag{6.12}$$

Substituting (6.10) and (6.11) into (6.12), results the output current of figure 6.3 can be expressed as

$$I_{out} = \frac{I_X I_Y}{4I_O} - 2I_O + I_{off} \tag{6.13}$$

Let $I_{off} = 2I_O$, the current I_{out} can be rewritten as

$$I_{out} = \frac{I_X I_Y}{4I_O} \tag{6.14}$$

This means that proposed analog multiplier operate as the multiplier as required. From equation (6.14), the analog multiplier circuit is a current multiplier when V_X and V_Y are attached to ground. Using (6.7) and let R_X=R_Y=R_L, the inputs I_X and I_Y are connected to grounded resistors, R_X and R_Y, respectively, the proposed analog multiplier circuit is become a voltage multiplier. The product of two inputs can be expressed as

$$V_{out} = \frac{V_X V_Y}{4I_O} \tag{6.15}$$

If V_X is attached to ground, I_Y is connected to grounded resistor or V_X is attached to ground, I_X is connected to grounded resistor. The current and voltage multiplier can be expressed as

$$V_{out} = \frac{I_X V_Y}{4I_O} \tag{6.16}$$

and $$V_{out} = \frac{V_X I_Y}{4I_O} \tag{6.17}$$

From the various outputs of the multiplier, the proposed multiplier can be called the versatile analog multiplier as same in [16]-[17]. It should be noted from the equations (6.14)-(6.17) that, since no term of transconductance parameter and threshold voltage of MOS transistor that cause of temperature effect are included in I_{out} and V_{out}. This means that I_{out} and V_{out} less sensitive to temperature.

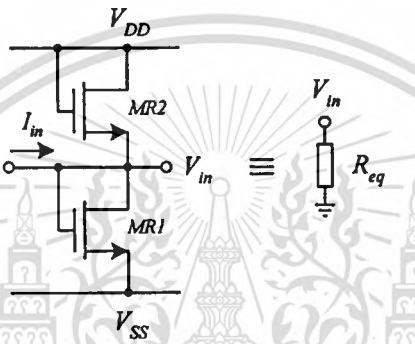

Figure 6.4 Linear MOS transistor.

For case the inputs are voltages, an analog multiplier is required to grounded resistors for V-I conversion. The MOS implementation of resistor used to instead their resistors, R_X and R_Y, can be obtained using only two MOS transistors. The MOS resistor is shown in figure 6.4 by Wang [21]. Assuming MOS transistors MR1 and MR2 are well matched, operated in saturation region, and the same of characteristics; $K = \mu_O C_{OX} W/L$, $V_{DD} = -V_{SS}$, the resistance values can be given as

$$R_{eq} = \frac{1}{4K(V_{DD} - V_{THN})} \tag{6.18}$$

It can be seen from equations (6.14) to (6.17) that the input signals of proposed analog multiplier can be voltages and/or currents. The multi-functions of the product are listed in Table 6.1. Finally, this proposed circuit is suitable for IC implementation when the resistors can be instead by MOS resistors.

Table 6.1 Functions for versatile analog multiplier.

Function	Condition
$I_{out} = \frac{I_X I_Y}{2I_O}$	V_X is attached to ground, V_Y is attached to ground,
$V_{out} = \frac{V_X V_Y}{2I_O}$	I_X is connected to R_X, I_Y is connected to R_Y
$V_{out} = \frac{I_X V_Y}{2I_O}$	V_X is attached to ground, I_Y is connected to R_Y
$V_{out} = \frac{V_X I_Y}{2I_O}$	I_X is connected to R_X, V_Y is attached to ground

6.3. Performance analysis

In this section, the characteristics of analog multiplier of figure 6.3 will be analyzed. The input range, input and output impedances, mismatched and second-order effects and frequency responses will be discussed.

6.3.1. Mismatch and second-order effects

The transconductance mismatch and second-order effect are discussed in this report. If the mismatch is defined as $K_N = K$ and $K_P = K+\Delta K$, then equation (6.3) become

$$\sqrt{\frac{I_O}{K}} + \sqrt{\frac{I_O}{K+\Delta K}} = \sqrt{\frac{I_{D2}}{K}} + \sqrt{\frac{I_{D4}}{K+\Delta K}} \tag{6.19}$$

Using the approximation $(1+I_{in})^{-1/2} \approx 1-(1/2)I_{in}$, if $I_{in} \ll 1$, ignoring terms containing Δ^2, assume $4(1-\Delta)I_{in} \gg (\Delta/2)I_{in}$, the equations (6.4) and (6.5) can be rewritten as

$$I_{D2} \approx I_O - (1/2 - 1/\Delta)\frac{I_{in}}{2} + (1 - 4/\Delta)\frac{I_{in}^2}{16I_O} \tag{6.20}$$

and

$$I_{D4} \approx I_O + (1/2 - 1/\Delta)\frac{I_{in}}{2} + (1 - 4/\Delta)\frac{I_{in}^2}{16I_O} \tag{6.21}$$

According (6.20) and (6.21), the output current I_{out} of the proposed multiplier can be rewritten as

$$I_{out} \approx 2I_O + \frac{I_{in}^2}{8I_O} + \frac{I_{in}}{\Delta} - \frac{I_{in}^2}{4I_O\Delta} \tag{6.22}$$

Again, according (6.22), (6.20) and (6.21) can be rewritten as

$$I_{D20} \approx 2I_O + \frac{(I_X + I_Y)^2}{8I_O} + \frac{I_X + I_Y}{\Delta} - \frac{(I_X + I_Y)^2}{\Delta 4I_O} \tag{6.23}$$

and

$$I_{D25} \approx 4I_O + \frac{I_X^2 + I_Y^2}{8I_O} + \frac{I_X + I_Y}{\Delta} - \frac{I_X^2 + I_Y^2}{\Delta 4I_O} \tag{6.24}$$

Using (6.23) and (6.24), the output current I_{out} of figure 6.3 can be rewritten as

$$I_{out} \approx \frac{I_X I_Y}{4I_O} - \frac{I_X I_Y}{\Delta 4I_O} \tag{6.25}$$

and

$$V_{out} \approx \frac{V_X V_Y}{4I_O} - \frac{V_X V_Y}{\Delta 4I_O} \tag{6.26}$$

From (6.25) and (6.26) imply that the transconductance mismatch causes a change slope in the DC characteristics.

The second order effects such as body effect, mobility reduction, and channel-length modulation is discussed next. The second source of nonlinear is mobility degradation. The mobility variation is reduced by maximizing the gate-source voltage of the class-AB MOS transistors. Channel length modulation is another source of nonlinear. To reduce this effect, it is necessary to stabilize the drain-source voltage of the class-AB transistors by some effect, such as using a sufficiently large channel length throughout the circuit or cascading this also improves the current mirroring accuracy. The body effect can be reduced by connecting with source and bulk of MOS transistor.

6.3.2. Input range and input/output resistance

The input voltage range of the proposed multiplier is restricted by dual translinear loops, M1-M4 and M5-M8, and MOS transistors M13, M16, M21, operating in the saturation region. If assume that the V_{DS} of each MOS transistors are high enough to satisfy the saturation condition. From the principle of class-AB, the MOS transistors M2 and M4 alternately operate (M2-off, M4-on or M2-on, M4-off). Assume MOS transistor M2 actives, by using Kirchhoff's voltage law, it can be given as

$$V_{DD} = V_{SG21} + V_{GS2} - V_{TH2} + V_{RX} \tag{6.27}$$

$$V_{in} = V_{SG1} + V_{GS2} + V_{RX} \tag{6.28}$$

Using equation (6.1.2), (6.27) and (6.28) become

$$V_{DD} = V_{SG21} + \sqrt{\frac{I_{D2}}{K_2}} + V_{RX} \tag{6.29}$$

$$V_{in} = V_{SG1} + \sqrt{\frac{I_{D2}}{K_2}} + V_{TH2} + V_{RX} \tag{6.30}$$

The relation of V_{in} and V_{DD} can be given by subtracting with (6.29) and (6.30), it leads to

$$V_{DD} = -\sqrt{\frac{I_{D21}}{K_{21}}} - V_{TH21} + V_{in} + \sqrt{\frac{I_{D1}}{K_1}} \tag{6.31}$$

Using (6.6) and let $|I_{in}| = 4I_O$, $I_{D1} = I_O$, the maximum voltage input range V_X can be written as

$$V_{X(MAX)} \le V_{DD} + 2\sqrt{\frac{I_O}{K_{21}}} - \sqrt{\frac{I_O}{K_1}} + V_{TH21} \tag{6.32}$$

Again, assume MOS transistor M4 actives, using Kirchhoff's voltage law, it can be expressed as

$$V_{SS} = V_{SG13} + V_{GS4} - V_{TH4} + V_{RX} \tag{6.33}$$

$$V_{in} = -V_{SG3} + V_{GS4} + V_{RX}\,. \tag{6.34}$$

Using (6.1.2), (6.33) and (6.34) become

$$V_{SS} = V_{SG13} + \sqrt{\frac{I_{D4}}{K_4}} + V_{RX} \tag{6.35}$$

$$V_{in} = -V_{SG3} + \sqrt{\frac{I_{D4}}{K_4}} + V_{TH4} + V_{RX}\,. \tag{6.36}$$

Subtracting with (6.29) and (6.30), the relation of V_{in} and V_{DD} can be given as

$$V_{SS} = -\sqrt{\frac{I_{D13}}{K_{13}}} - V_{TH13} + V_{in} + \sqrt{\frac{I_{D3}}{K_3}} \tag{6.37}$$

Using (6.6) and let $|I_{in}| = 4I_O$, $I_{D3} = I_O$, the minimum voltage input range V_X can be written as

$$V_{X(MIN)} \le V_{SS} + 2\sqrt{\frac{I_O}{K_{13}}} - \sqrt{\frac{I_O}{K_1}} + V_{TH13} \tag{6.38}$$

From (6.32) and (6.38), the voltage input range V_X of proposed multiplier as shown in figure 6.3 can be given as

$$V_{SS} + 2\sqrt{\frac{I_O}{K_{13}}} - \sqrt{\frac{I_O}{K_1}} + V_{TH13} \le V_X \le V_{DD} + 2\sqrt{\frac{I_O}{K_{21}}} - \sqrt{\frac{I_O}{K_1}} + V_{TH21}\,. \tag{6.39}$$

By using the maner follow above, the input voltage range of the input V_Y can be expressed as

$$V_{SS}+2\sqrt{\frac{I_O}{K_{16}}}-\sqrt{\frac{I_O}{K_6}}+V_{TH16}\le V_Y\le V_{DD}+2\sqrt{\frac{I_O}{K_{21}}}-\sqrt{\frac{I_O}{K_5}}+V_{TH21} \qquad (6.40)$$

where K_i and V_{THi} are the tranconductance parameter and the threshold voltage, respectively, of MOS transistors Mi.

Whereas, the values of input current ranges I_X and I_Y are restricted by the saturation condition of an MOS transistor of the dual translinear loops (M1 toM8). Therefore, the input current ranges of figure 6.3 should be given by [18]

$$|I_X|=|I_Y|\le 2I_O. \qquad (6.41)$$

The analog multiplier in figure 6.3 can find their input and output impedance by taking it into the small-small circuit. Consider MOS transistors M1, M3, and I_O, the input impedance at port V_X can be given as

$$r_{VX}=(r_{IO}+1/g_{m1})//(r_{IO}+1/g_{m3}) \qquad (6.42)$$

whereas the input impedance at port V_Y is resticted by MOS transistors M5, M7, and I_O, it can be expressed as

$$r_{VX}=(r_{IO}+1/g_{m5})//(r_{IO}+1/g_{m7}) \qquad (6.43)$$

where r_{IO} is the inner resistance of current sources I_O and g_{mi} is the transconductance parameter of MOS transistor Mi. If let $r_{IO}\ll 1/g_{m1}$, $1/g_{m3}$, $1/g_{m5}$ and $1/g_{m7}$, the input impedance at ports V_X and V_Y can be expressed as

$$r_{VX}=r_{VY}\cong r_{IO}/2 \qquad (6.44)$$

Consider MOS transistors M2, M4, M13, M14 and M21 and taking it into the small-small circuit, the input impedance at port I_X can be given as

$$r_{IX} = \frac{1}{(g_{m2} + g_{m4}) + (g_{m4} g_{m14} g_{ds2} / g_{m21} g_{m13})} \tag{6.45}$$

Again, the input impedance at port I_Y is resticted by MOS transistors M6, M8, M15, M16 and M21, it can be written as

$$r_{IY} = \frac{1}{(g_{m6} + g_{m8}) + (g_{m8} g_{m15} g_{ds6} / g_{m21} g_{m15})} \tag{6.46}$$

when g_{ds2} and g_{ds6} are the drain-source resistance of MOS transistors M2 and M6, respectively. Assume that $g_{ds} \ll g_m$, the input impedances at ports I_X and I_Y can be approximated as, respectively,

$$r_{IX} = 1/(g_{m2} + g_{m4}) \tag{6.47}$$

$$r_{IY} = 1/(g_{m6} + g_{m8}) \tag{6.48}$$

The output impedance r_{out} can be calculated from M20, M25, it can be expressed as

$$r_{out} = r_{ds20} r_{ds25} / (r_{ds20} + r_{ds25}) \tag{6.49}$$

Typically, the inner resistance of the current sources is very high. Thus as indicated by (6.44), the input resistances V_X and V_Y of proposed multiplier in figure 6.3 is very high. Example, the MOS transistor with V_{THN} = 0.62V, V_{THP} = -0.58V and $\mu_O C_{OX}$ = $53 \times 10^{-7} AV^{-2}$. Let $V_{DD} = -V_{SS}$ = 1.5V and I_O = 10μA, then the input ranges V_X, V_Y, I_X and I_Y of proposed multiplier is approximately equal to |20μA| and |400mV|, respectively.

6.3.3. Frequency responses

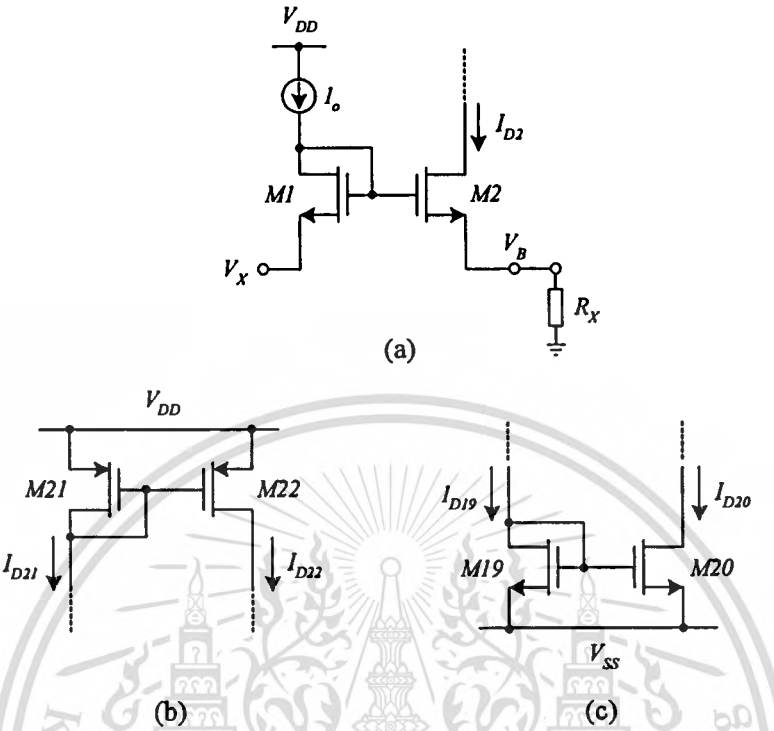

Figure 6.5 (a) Class AB converter; (b) negative current mirror; (c) positive current mirror.

From the proposed analog multiplier of figure 6.3, if consider only the input V_X. The major high-frequency limitation of the proposed current multiplier results from the bandwidth of three sections which is shown in figure 6.5. The first potential high frequency limitation is due to the capacitances and the conversion impedance R_X as shown in figure 6.5(a). The second high-frequency limitation is due to the bandwidth of negative current mirrors as shown in figure 6.5(b). The third high-frequency limitation is due to the bandwidth of positive current mirrors as shown in figure 6.5(c). Using the small-signal model of figure 2.5, the relationship voltage of the voltages V_X and V_B as shown in figure 6.5(a) can be written as

$$\frac{V_B}{V_X} = \frac{\left(s+\frac{g_{m1}}{C_{gs1}}\right)\left(s+\frac{g_{m2}}{C_{gs2}}\right)}{s^2+s\left(\frac{g_{m1}}{C_{gs1}}+\frac{g_{m2}}{C_{gs2}}+\frac{1}{R_X}\right)+\frac{g_{m1}\left(g_{m2}+\frac{1}{R_X}\right)}{C_{gs1}C_{gs2}}} \tag{6.50}$$

when $g_m \gg g_{ds}$. If let $g_{m2}R_X \gg 1$, the converter poles (P_1) will be independent on R_X and can be approximately expressed by

$$P_1 = \frac{1}{2\pi}\sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}}. \tag{6.51}$$

The negative current mirror and the positive current mirror pole as shown in figures 6.5(a) and 6.5(c), respectively, can be written as, respectively,

$$\frac{I_{D22}}{I_{D21}} = \frac{\frac{g_{m22}}{C_{gs21}+C_{gs22}}}{s+\frac{g_{m21}}{C_{gs21}+C_{gs22}}} \tag{6.52}$$

$$\frac{I_{D20}}{I_{D19}} = \frac{\frac{g_{m20}}{C_{gs19}+C_{gs20}}}{s+\frac{g_{m19}}{C_{gs19}+C_{gs20}}}. \tag{6.53}$$

The negative current mirror pole (P_2) and the positive current mirror pole (P_3) as shown in figures 6.5(a) and 6.5(c), respectively, are given by

$$P_2 = \frac{g_{m21}}{2\pi(C_{gs21}+C_{gs22})} \tag{6.54}$$

$$P_3 = \frac{g_{m19}}{2\pi(C_{gs19}+C_{gs20})} \tag{6.55}$$

where C_{gsi} is the gate-to-source capacitance and g_{mi} is the transconductance of the MOS transistor Mi. For example, if the small signal parameters C_{gs} and g_m obtained

from the simulation are $g_{m1} = g_{m2} = 1.13\times10^{-4}AV^{-1}$, $g_{m19} = g_{m20} = 1.58\times10^{-4}AV^{-1}$, $g_{m21} = g_{m22} = 2.23\times10^{-4}AV^{-1}$, $C_{gs1} = C_{gs2} = 1.8\times10^{-13}F$, $C_{gs19} = C_{gs20} = 1.8\times10^{-13}F$, $C_{gs21} = C_{gs22} = 8.44\times10^{-13}F$. The high-frequency of pole P_1, P_2 and P_3 will be located at approximately 99.9MHz, 21MHz and 69.8MHz, respectively. It can be evaluated that the major high-frequency limitation of the proposed versatile multiplier results from the bandwidth of the negative current mirrors.

6.4. Simulation and experimental results

6.4.1. Simulation results

The performance of proposed analog multiplier circuit shown in figure 6.3 are simulated using PSPICE with level 3 model of 0.5μm CMOS parameter of MIETEC as shown in Table 2.2. The MOS transistor aspect ratio in Table 6.2 is used. The supplied voltages used are V_{DD}=-V_{SS}=1.5V and the bias current I_O=10μA. R_L=R_X=R_Y are replaced with MOS resistor as shown in figure 6.4.

Table 6.2 MOS transistor sizes.

Transistor	W/L (μm/μm)
M1,M2,M5,M6,M9,M10,M13,M14, M15 M16,M19,M20	20/4
M3,M4,M7,M8,M11,M12,M22,M23,M24,M25	93/4
M17,M18	40/4
MR1,MR2	2/2

Figure 6.6 shows the DC transfer characteristics of the proposed analog multiplier when inputs are currents. The output current swings approximately between -10μA to +10μA for the input current range of ±20μA, while the V_X and V_Y are attached to ground. Figure 6.7 shows the DC transfer characteristics of multiplier under condition by varying V_X from -300mV to 300mV against varying V_Y from -300mV to 300mV at 100mV per step, while the input I_X and I_Y are connected to MOS resistors (≈10kΩ). The input and output swing can be increased by large input and output resistors. Figure 6.8 shows the DC transfer characteristics in the case of versatile multiplier. Here, the input current I_X is varied from -20μA to +20μA and the input voltage V_Y is

varied from -300mV to +300mV, whereas the input voltage V_X is attached to ground and the input current I_Y is connected to MOS resistor. From PSPICE simulations, the linearity error was 1.2%.

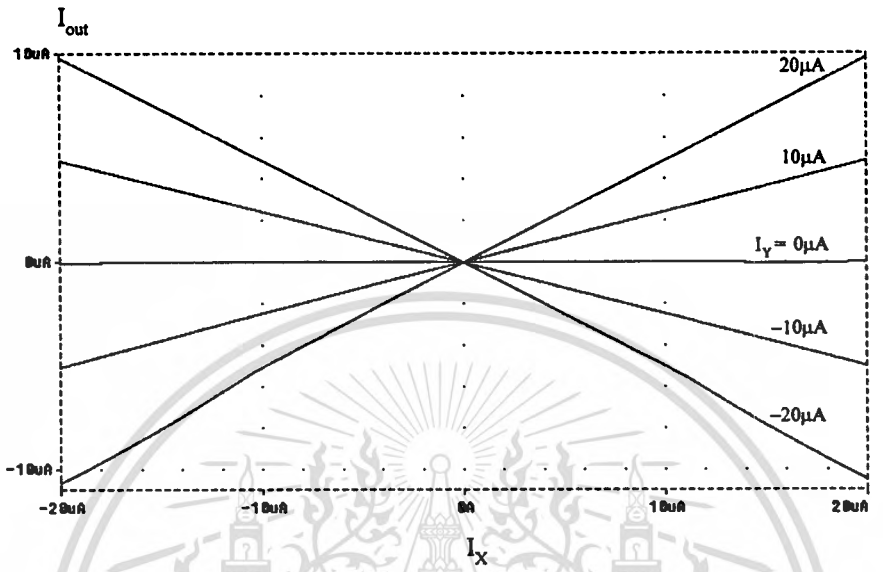

Figure 6.6 Simulated DC transfer characteristics for two inputs are currents.

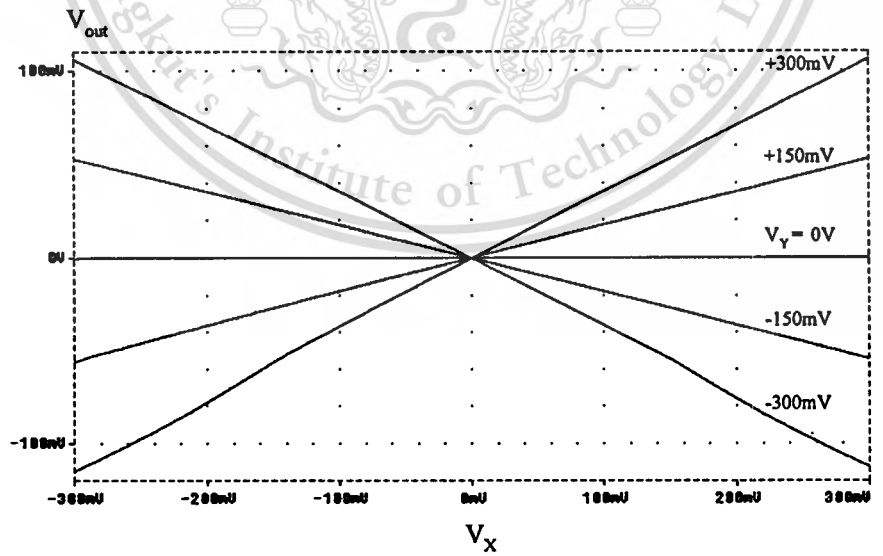

Figure 6.7 Simulated DC transfer characteristics for two inputs are voltages.

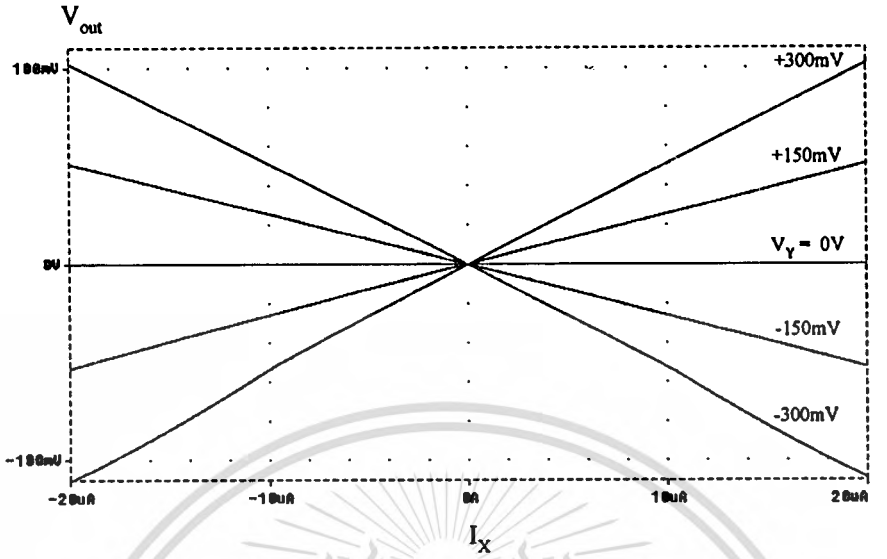

Figure 6.8 Simulated DC transfer characteristics for inputs are voltage and current.

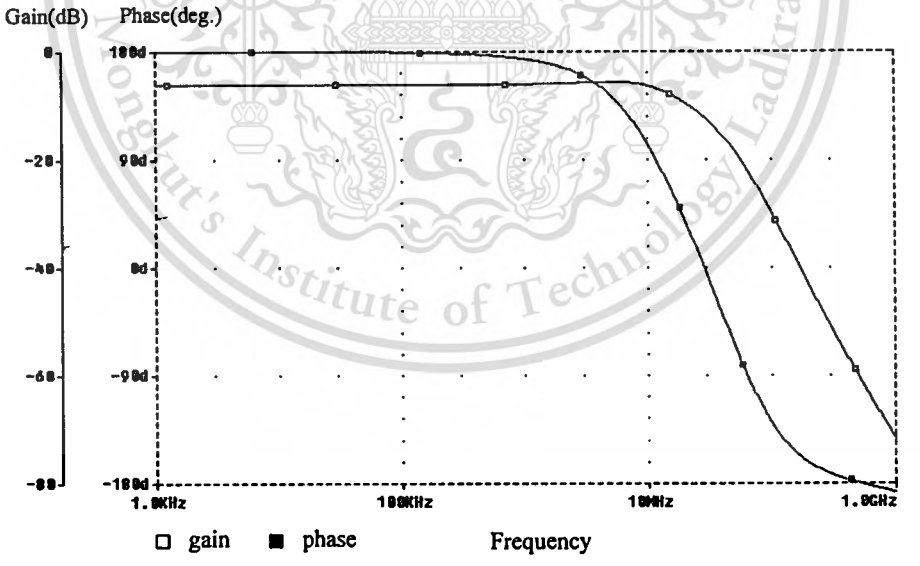

Figure 6.9 Frequency and phase response characteristic for inputs are voltages.

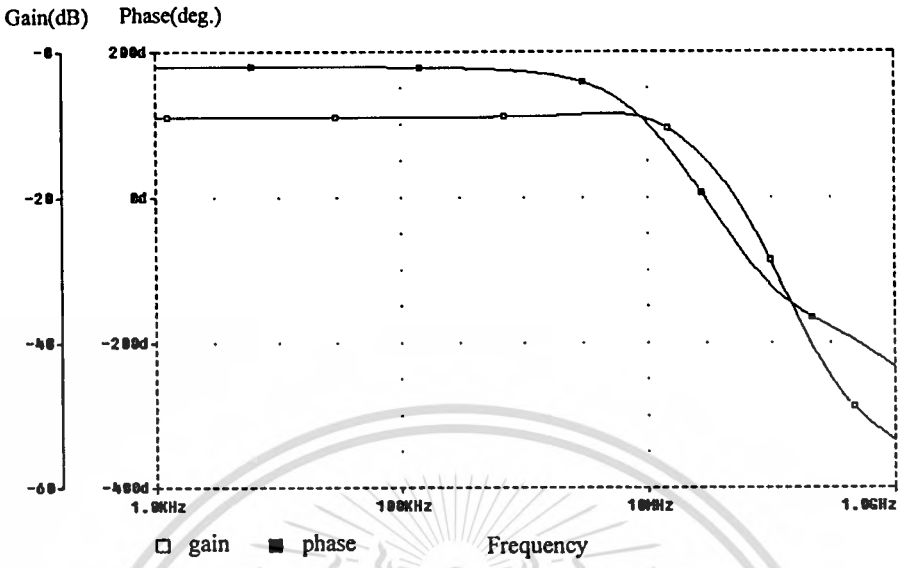

Figure 6.10 Frequency and phase response characteristic for inputs are currents.

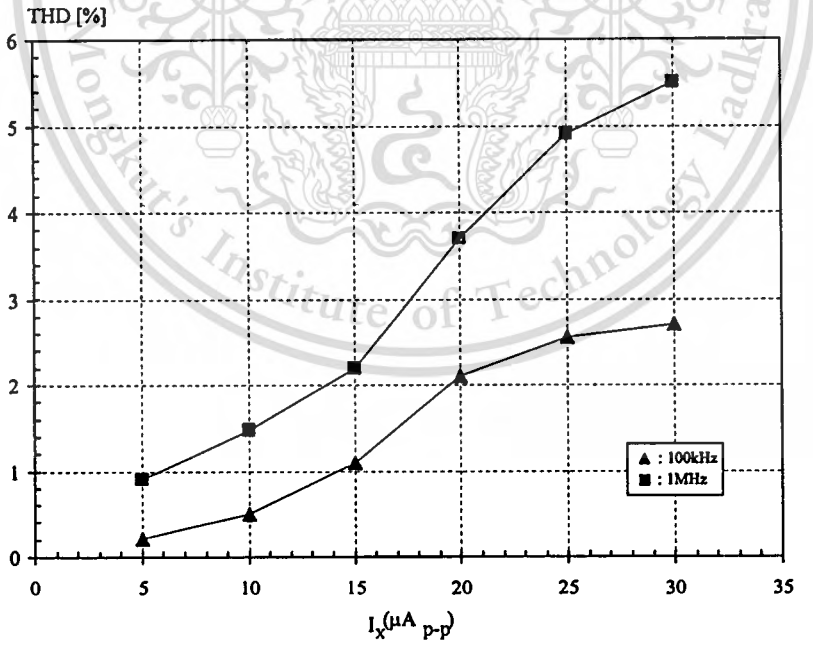

Figure 6.11 Total harmonic distortions versus input current.

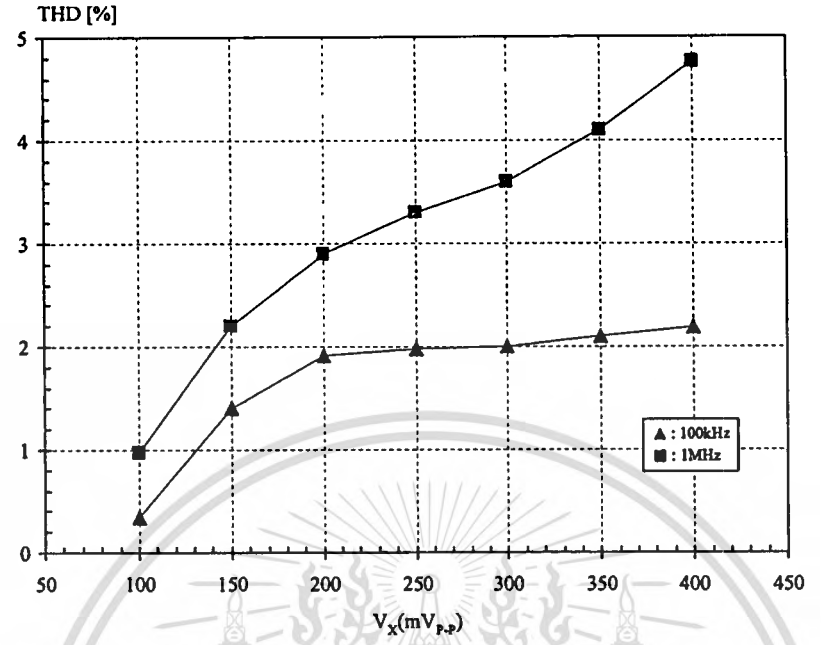

Figure 6.12 Total harmonic distortions versus input voltage.

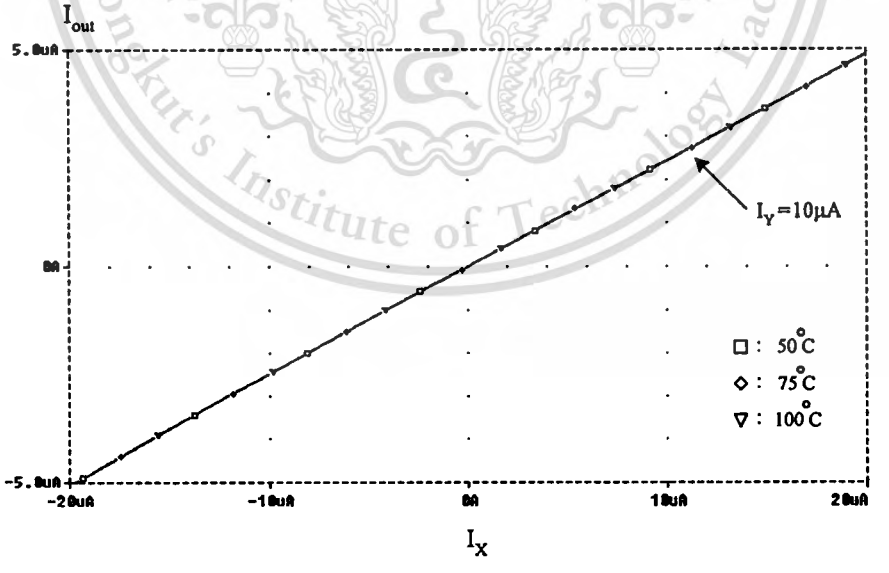

Figure 6.13 Simulated DC transfer characteristics for the temperature=50°C, 75°C and 100°C.

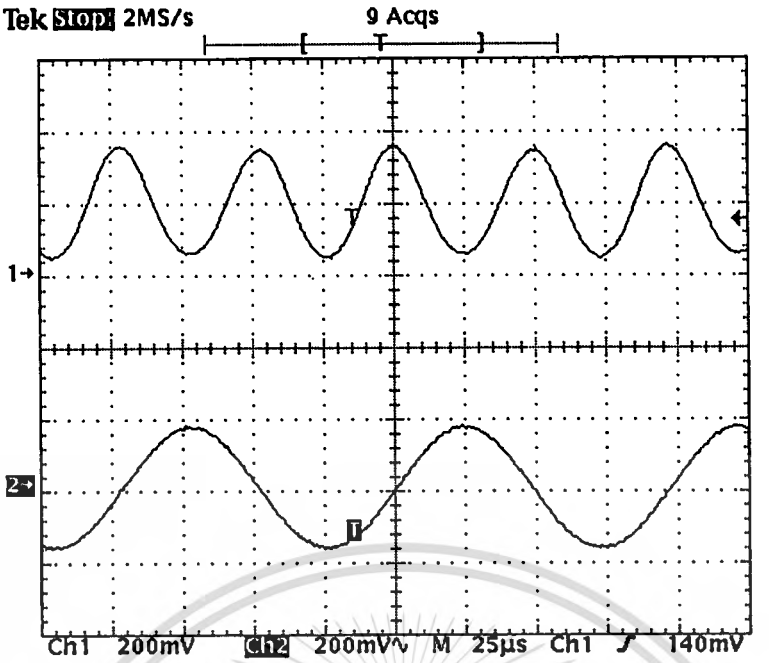

Figure 6.14 Measured frequency doubler with a 10kHz sine wave inputs. Lower trace: 400mV$_{P-P}$ sine signal of 10kHz (200mV/div), Upper trace: output waveform (200mV/div), horizontal scale is 25µs/div.

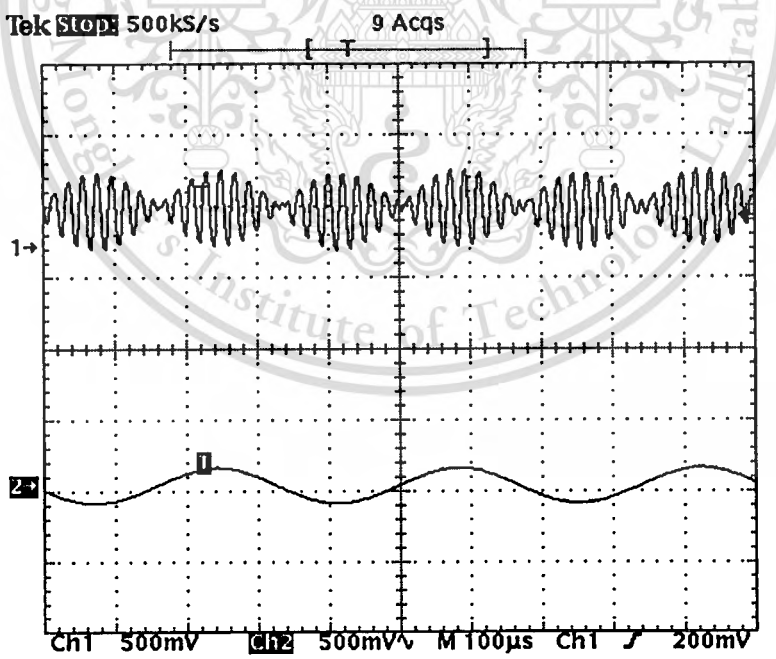

Figure 6.15 Measured output waveform of a 50kHz sinusoid and a 3kHz sinusoid. Lower trace: a 400mV$_{P-P}$ sine signal of 3kHz (500mV/div), Upper trace: output waveform (500mV/div), Horizontal scale is 100µs/div.

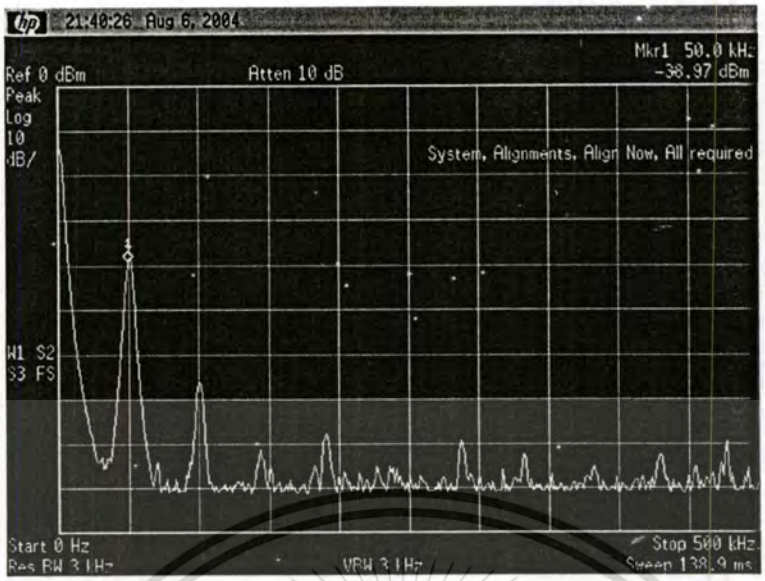

Figure 6.16 Measured output spectrum of analog multiplier, for the case in which a 400mV$_{P-P}$ sine signal of 50kHz and a 400mV DC voltage are applied with V_X and V_Y, respectively [horizontal scale is 100μs/div; vertical scale is 10dBm].

6.5. Conclusions

The class-AB versatile analog multiplier was presented in this chapter. The proposed circuit based on dual translinear loops operating in class-AB. The class-AB dual translinear loop used saturated complementary transistors and exploits the square-law behavior of MOS transistor. The particularities of this technique are high signal swing, high dynamic range, high bandwidth, and low consumption. The advantages of the proposed analog multiplier circuit are; (i) the multiplier has multi-functions, (ii) single ended input, (iii) high temperature stability. The proposed analog multiplier can be used in an analog VLSI cell for low power and high speed application, such as IF variable gain amplifier and adaptive filters. The experimental results have been shown to confirm the operation. The PSPICE simulation results of proposed analog multiplier are summarized in Table 6.3.

Table 6.3 Simulated performance of proposed versatile analog multiplier.

Parameter	Value
Technology	0.5μm CMOS
Supply voltage	±1.5V
Bias current	10μA
Input voltage range @ R_X=R_Y=10kΩ	±300mV
Output voltage range @ R_L=10kΩ	300mV
Input current range	±20μA
Output current range	20μA
Bandwidth (-3dB)	19MHz
Nonlinear error for I_X @I_Y=20μA	1.2%
Nonlinear error for V_X @V_Y=300mV	1.2%
THD for @I_X=20μA_{P-P},100kHz; I_Y=20μA_{DC}	2%
THD for @V_X=300mA_{P-P},100kHz;V_Y=300mA_{DC}	1.9%
Power consumption (Max.)	0.46mW

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CHAPTER 7
CONCLUSIONS AND FUTURE RESEARCHES

7.1. Conclusions

This chapter summarized purposes of research contribution and results, and provides some recommendations for future work. There were two general thrusts of this research. i) Issues of design of analog signal processing circuits in current-mode operation were explored with particular emphasis on designing of current-mode all-pass filter, rectifier and analog multipliers. ii) Techniques for reducing the power consumption and for designing the analog signal processing circuits suitable for IC implementation were investigated. Current-mode circuits have some recognized advantages: firstly, they do not require a high voltage gain, so high performance amplifiers are not needed. Then, they do not need high precision passive components, so they can be designed almost entirely with transistors. This makes the current-mode circuits compatible with typical digital processes. Finally, they show high performance in terms of speed, bandwidth and accuracy. The use of grounded capacitor, without external resistor and all solid-state structure will allow these proposed circuits ideality for IC implementation.

Four analog signal processing circuits developed in this thesis have been published in international conferences and international journals. These researches are published in IEEE TENCON 2004, The ECTI Annual Conference (ECTI-CON 2005), IJSP (International Journal of Signal Processing), and IJE (International Journal of Electronics).

7.2. Recommended future work

In this thesis, design and implementation of integable current-mode analog signal processing in CMOS and bipolar technologies are developed. If this works were to be continued, the ways to develop these works are follows:

(1) The all-pass networks served primarily as the design of concept that the circuits could meet the grounded capacitor and electronically tunable. The next step would be to directly employ as a subsystem of monolithic

circuit without extra conversion stages. The use of a grounded capacitor and without resistor makes the proposed circuit ideal for integrated circuit implementation. However, the all-pass networks in this design require two CCCIIs; hence the reducing of CCCII while maintain the performances such as use a grounded capacitor, high output impedance and electronically tunable not change is ideal for the future work.

(2) The features of the proposed full-wave rectifier are in view of the operating frequency and precision, the suitability for IC implementation. For the operating frequency up to 200MHz, however, this operating frequency obtained from only simulation, when the proposed full-wave rectifier is built as IC, this operating frequency may be lessen by the effect of parasitic capacitance in IC. The used of minimum sizes of W/L of MOS transistor will be supported.

(3) A versatile analog multiplier is proposed. The major advantages of this proposed multiplier are; this design has single ended inputs; current multiplying, voltage multiplying, or current and voltage multiplying can be obtaineted. In case input is voltage, the proposed versatile analog multiplier requires the resistors R_X and R_Y to convert the voltage to the current and R_L to convert the current to the voltage. The lineation of MOS resistors will effect to linear of the voltage multiplying, thus the linear resistor is required.

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