ON THE DESIGN OF CMOS TRUE RMS-TO-DC CONVERTER AND LINEAR ELECTRONICALLY TUNABLE OTA

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หัวข้อวิทยานิพนธ์	วงจรแปลงสัญญาณ RMS เป็นสัญญาณไฟฟ้ากระแสตรง และวงจรโอทีเอที่สามารถปรับค่าได้ทางอิเล็กทรอนิกส์แบบเป็นเชิงเส้น ที่ออกแบบบนพื้นฐานของเทคโนโลยีซีมอส
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บทคัดย่อ

วิทยานิพนธ์ฉบับนี้ เป็นการนำเสนอเทคนิคการออกแบบวงจรรวมทางด้านอนาลอก บนพื้นฐานของเทคโนโลยีซีมอส โดยอาศัยคุณสมบัติกฎยกกำลังสองของมอสทรานซิสเตอร์ที่ทำงานในช่วงอิ่มตัวและอาศัยวงจรสะท้อนกระแสเป็นโครงสร้างหลัก ซึ่งเป็นการนำเสนอเทคนิคการออกแบบวงจร 2 วงจร วงจรแรกที่นำเสนอ คือวงจรแปลงสัญญาณ RMS เป็นสัญญาณไฟฟ้ากระแสตรงแบบโหมดกระแสที่มีช่วงแบนด์วิทกว้าง ออกแบบโดยใช้วิธีคำนวณค่าโดยนัย (implicit computation method) โครงสร้างของวงจรประกอบด้วยวงจรยกกำลังสองแบบซีมอส วงจรสะท้อนกระแส และวงจรกรองแบบต่ำผ่าน เนื่องจากกระแสดีซีไบอัสของวงจรได้จากค่ากระแส I_{RMS} ที่เกิดจากคุณสมบัติการป้อนกลับของวงจร จึงทำให้วงจรมีกำลังสูญเสียต่ำ (low-power consumption) และคุณสมบัติการปฏิบัติงานเชิงความถี่ของวงจรขณะที่กระแสอินพุทเท่ากับ 1.5mA มีค่าเท่ากับ 100MHz วงจรที่สองที่นำเสนอ คือวงจรโอทีเอแบบซีมอสที่สามารถปรับค่าได้ทางอิเล็กทรอนิกส์แบบเป็นเชิงเส้น วงจรนี้สามารถปรับค่าอัตราขยายทรานส์คอนดัคแตนซ์โดยวิธีทางอิเล็กทรอนิกส์ได้อย่างเป็นเชิงเส้นด้วยกระแสดีซีไบอัส การออกแบบอาศัยหลักการหักล้างฟังก์ชันที่ไม่เป็นเชิงเส้นของวงจรซีมอสโอทีเอแบบพื้นฐานด้วยการยกกำลังสองเทอมที่ไม่เป็นเชิงเส้นของวงจรซีมอสโอทีเอแบบพื้นฐาน ด้วยคุณสมบัติของวงจรโอทีเอแบบซีมอสที่เหมือนกัน คุณสมบัติของวงจรสามารถปรับค่าอัตราขยายทรานส์คอนดัคแตนซ์แบบเป็นเชิงเส้นได้ด้วยวิธีทางอิเล็กทรอนิกส์ ด้วยกระแสดีซีไบอัสที่ให้แก่วงจรได้ในช่วง 3 เดเคด (decade) โดยมีค่าความผิดพลาดประมาณ 0.68% และมีค่าพิสัยแรงดันอินพุตที่ค่าความไม่เป็นเชิงเส้นน้อยกว่า 1 % แบบเชิงเส้น เท่ากับ $\pm$ 1 โวลต์ วงจรมีช่วงความถี่ปฏิบัติงานประมาณ 120MHz และเพื่อเป็นการยืนยันประสิทธิภาพของวงจรจึงได้นำเสนอตัวอย่างการนำวงจร EOTA ไปประยุกต์ใช้งานเป็นวงจรคูณสัญญาณกระแส วงจรขยายสัญญาณกระแสที่สามารถปรับค่าได้ด้วยแรงดันควบคุม และวงจรขยายสัญญาณกระแสที่สามารถปรับค่าได้

ด้วยกระแสควบคุม เป็นต้น โดยคุณสมบัติของวงจรที่ได้ออกแบบในวิทยานิพนธ์นี้ศึกษาโดยใช้โปรแกรม PSPICE ผลการทดลองจากการต่อวงจรจริง และผลจากการทดสอบคุณสมบัติของไอซี เพื่อเป็นการยืนยันถึงสมรรถนะการทำงานและคุณสมบัติของวงจรที่ได้ออกแบบขึ้น

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ABSTRACT

This thesis presents the designs of two new analog integrated circuit building blocks based on CMOS technology. The themes of this work are designed by using current mirrors to be the main structure of the circuits and by using the square law characteristic where all MOS transistors are operated in saturation regions. Firstly, a simple integrable circuit technique for the realization of a wide bandwidth current-mode CMOS true RMS-to-DC converter is presented. The realization scheme is based on the implicit computation method. The circuit structure is composed of a squaring circuit, current mirrors and a first-order low-pass filter. The conversion circuit consumes very low power, due to the bias current of the circuit is provided by the root-mean-square current I_{RMS} from the feedback function. The high frequency response of the proposed true RMS-to-DC converter is 100MHz for I_{in}=1.5mA. Secondly, an electronically and linearly tunable CMOS OTA call as EOTA is presented. Where its transconductance gain can be electronically and linearly tuned by the DC bias current. The circuit is constructed from a balanced CMOS OTAs and achieves its linearity by squaring the nonlinear transconductance of the balanced CMOS OTA. This proposed EOTA can be linearly tuned by the bias current for 3 decades. The achieved characteristics of the transconductance gain (g_m) is dependent upon the bias current I_B over the range of 1μA to 1mA (three decades) with the conversion error from simulation result of about 0.68%. The EOTA can linearly convert the input voltage into the output signal current with nonlinearity of less than 1% for the input voltage (V_{in}) in the ranges of -1V to 1V. The frequency response of the EOTA was also studied, where the -3dB bandwidth of about 120 MHz is achieved. The usefulness of the proposed EOTA is demonstrated through application examples, such as a current multiplier, a linearly voltage-controlled current

amplifier and a linearly current-controlled CMOS current amplifier. The performances of the proposed circuits are studied through PSPICE simulation results and experimental results.

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Khanittha Kaewdang

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CHAPTER 1

Introduction

1.1 Introduction

At present, CMOS technologies rapidly captures the digital market, the low cost of fabrication and the possibility of placing both analog and digital circuits on the same chip so as to improve the overall performance and/or to reduce the cost of packaging made CMOS technology attractive. The growing importance of CMOS technology in integrated circuit design has initialed a new wave of design efforts i.e. CMOS gates dissipated power only during switching and required very few devices, two attributes in sharp contrast to their bipolar or GaAs counterparts. Moreover the dimensions of MOS devices could be scaled down more easily than those of other types of transistors and the implementation of analog functions in CMOS technology has become important for the complete integration of system or subsystems in a single VLSI chip.

Therefore, in this thesis, the designs of two new analog integrated circuit building blocks based on CMOS technology are proposed. The themes of this work are designed by using current mirrors as the main structure of the circuits and using the square law characteristic where all MOS transistors are operated in saturation regions. Firstly, a simple integrable circuit technique for the realization of A Wide Bandwidth Current-Mode CMOS True RMS-to-DC Converter is proposed. Secondly, an Electronically and Linearly Tunable CMOS OTA (EOTA) will be presented.

For the first circuit building block, the proposed true RMS-to-DC converter will be discussed. Since one of the important parameters in the measurement of electrical signal is the root mean square value of a signal, which gives the average energy content. The energy content is important in noise measurements, power measurements, and measurements of output signals of sensors. The rms value can be used to describe a variety of signals, such as a dc signal, and also a heavily fluctuating non-periodic signal. Although for periodic signals the rms value can be calculated from the average value, a true rms converter should be suitable for signals of arbitrary shape. A true rms-to-dc converter is an important instrument which is useful in the fields of instrumentation, communication and display systems [1]. In the past, many true rms-to-dc converters that based on a bipolar integrated circuit technology are available [2]-[4]. Their conversion schemes are mostly performed through the use of full-wave rectifiers and

multiplier/divider circuits that employing a log-antilog principle. Due to the bandwidth and the slew-rate of the full-wave rectifiers, the useful frequency ranges of these converters are limited to less than 5 MHz. New design techniques based on bipolar dynamic translinear circuits have been proposed to implement true rms-to-dc converters [5], [6]. Unfortunately, only circuit descriptions are outlined, but the characteristics of the rms-to-dc conversion circuits have not been reported. In addition, their circuits are operated in only one quadrant and also required full-wave rectifiers. Recently, a new design technique for rms-to-dc converter that realizes around a dual translinear-base squarer circuit, where the input current can be a two-quadrant current, is proposed [7]. The circuit exhibits a wide bandwidth because the full-wave rectifier is not required by this conversion scheme. However, the implementation scheme is rather complicate and suitable for implementing only in bipolar technology.

For the second circuit building block, this thesis presents the electronically and linearly tuneable CMOS transconductor. This is because the linear transconductors or voltage-to-current converter circuits are fundamental building blocks of analog circuits and systems. They are found useful in interface circuits, instrumentation amplifiers, continuous-time-filters and oscillators. Furthermore, when the transconductance gain of the transconductor can be electronically varied, they can also be applied in automatic gain control circuits and in analog multipliers. In the last two decades, it is well accepted that a linear transconductor, which is constructed from a bi-polar differential pair and current mirrors, called as an operational transconductance amplifier (OTA), is one of the essential active building blocks in the design of analog circuits [8]-[10]. This is due to the fact that the OTA is a low-cost device that has only a single high-impedance node and its transconductance gain g_m can be linearly controlled over more than four decades by means of an external bias current. Moreover, the implementation of analog circuits in such a way that employs only OTA as standard cells will not only be easily constructed from readily commercial available IC, but also significantly simplifies the design. In CMOS technology, several linearly tunable transconductors based on the use of MOS transistors operating in saturation region have been proposed in the literatures [11]-[14]. Most of them are functioning in voltage controlled mode. The method of source-follower of the reference [11] is operated in square law characteristic with constant source-bulk voltages, where the control voltage is applied to the gate. Whereas for the cross coupled connection methods [12]-[14], the transconductance control voltages are applied through voltage level shifters. However, their controllable voltage ranges are rather limited and only narrow linearly tunable transconductance ranges are available. In some applications, such as,

an analog multiplier circuit, a frequency divider/multiplier circuit and an arbitrary power-law circuit, current controlled transcondcutors that this trasconductance gain can be linearly controllable by a DC bias current are preferable [15]-[17]. In the past, a current controlled CMOS transconductor was presented in [18]. But the linearly tunable transconductance range is narrow due to the MOS transistors are working in the weak-inversion region.

1.2 Purpose and objective of the study

In this thesis, the design techniques and implementation methods of the two circuit building blocks in the integrable circuit form based on CMOS technology are presented. The theme of this work are to design by using current mirrors as main structure of the circuits and using the square law characteristic, where all MOS transistors are operated in saturation regions. There are a true RMS-to-DC converter and a linear electronically tunable CMOS OTA (EOTA). Proposed circuits yield the following advantages:

(i) The proposed true RMS-to-DC converter that designed by the use of implicit computation to calculate the RMS value of an input signal, is suitable for all input waveforms. The conversion circuit is simple, suitable for implementing in monolithic integrated form. The circuit exhibits a wide bandwidth because the full-wave rectifier is not required by the proposed realization scheme. Moreover the circuit consumes very low power, due to the bias current of the circuit is provided by the root-mean-square current I_{RMS}.

(ii) The proposed linear electronically tunable CMOS OTA (EOTA) realization method is achieved by squaring the transconductance gain of the balanced CMOS OTA. Therefore the EOTA transconductance gain can be linearly tuned by an external bias current for three decades. The linear input-voltage range of about 1Vp with less than 1% nonlinearity is obtained. The usefulness of the proposed EOTA is demonstrated through application examples, such as a current multiplier, a linearly voltage-controlled current amplifier and a linearly current-controlled CMOS current amplifier.

1.3 Theory or idea used in the research

(i) All of the proposed circuits in this thesis are designed based on the MOS transistor square law characteristic and current mirrors as the main structure of the circuits.

(ii) The implicit computation method is used for the realization of root-mean-square function. The advantage of this technique is that the RMS circuit is not requiring the square-root circuit. The circuit structure is composed of a squaring circuit, current mirrors and a first-order low-pass filter. The circuit is simple that suitable for fabricated in CMOS technology and the wide bandwidth characteristic is achieved.

(iii) The realization method of the proposed electronically and linearly tunable CMOS OTA (EOTA) is achieved by squaring the transconconductance gain of the CMOS OTA. For this technique the linear transconductance is computed by squaring the transconductance of a balanced CMOS OTA which the proposed circuit is require 3 balanced CMOS OTA for realize the linear tracnsconductance characteristic.

1.4 Dissertation Overview

In chapter 2 the active circuit elements which used for designing the circuit building blocks in this thesis are described in this chapter. The circuit descriptions of the CMOS current mirrors, the CMOS current squaring circuit and the CMOS OTAs are outlined.

Chapter 3 concerning with the design and implementation of CMOS based true RMS-to-DC converter. The circuit description and circuit performance, such as: input dynamic range, conversion errors, frequency response and DC and ripple errors, are described. The implementation of the proposed RMS-to-DC converter by both the discrete circuits by using CMOS CD4007 transistor parameters and the real chip by implementing on 0.5 microns CMOS Technology AMIS process are outlined. The performance of the true RMS-to-DC converter has been studied through simulation and experimental results. In addition, the summary of RMS-to-DC converter characteristics is also included.

In chapter 4 the proposed electronically and linearly tunable CMOS OTA (EOTA) is presented. The circuit description, circuit performances, such as: input dynamic range, conversion errors, frequency response, are described. Moreover a current multiplier circuit, a linearly voltage-

controlled current amplifier and a linearly current-controlled CMOS current amplifier, are illustrated in the application examples. The circuit performances are studied through PSPICE simulation results.

Finally, Chapter 5 concerning with the conclusions and discussions.

CHAPTER 2

Active circuit elements

In this chapter, the circuit elements which will be used as major active circuit elements in this thesis are described. The circuit descriptions of the CMOS current mirror, the CMOS current squarer circuit and the CMOS OTA are respectively outlined.

2.1 Current-mirror

2.1.1 Circuit Description

Current mirrors have come to be widely used in analog integrated circuits both as biasing elements and as active load devices for amplifier stages. The use of current mirrors in biasing can result in superior insensitivity of circuit performance to variations in power supply and temperature [19], [20].

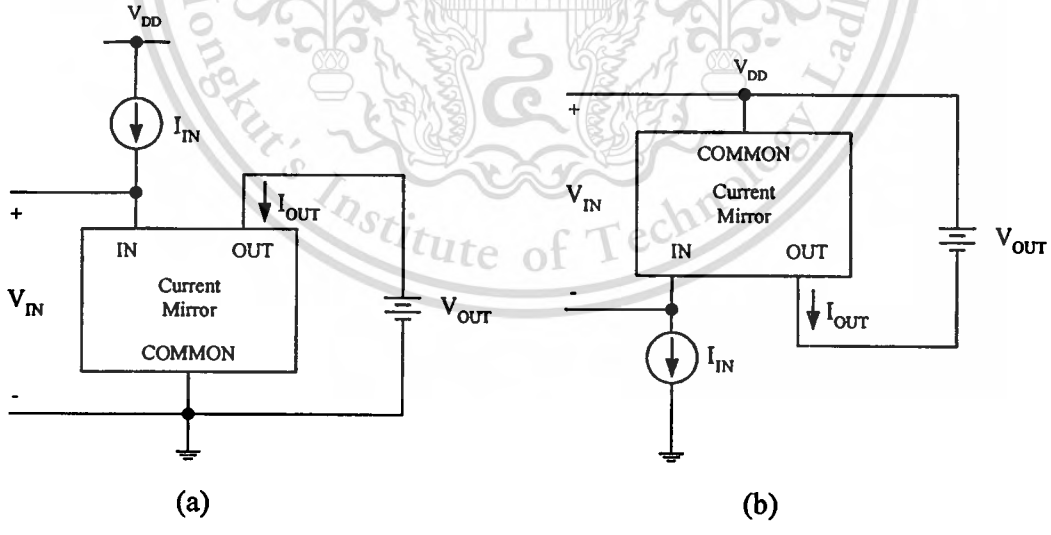


Fig. 2.1 Current-Mirror block diagram referenced to (a) ground and (b) the positive supply.

A current mirror is an element with at least three terminals, as shown in Fig. 2.1. The common terminal is connected to a power supply, and the input current source is connected to the input terminal. The output current is ideally equal to the input current multiplied by a desired current gain. If the gain is unity, the input current is simply reflected to the output, leading to the name current mirror. Under ideal conditions, the current-mirror gain is independent of input frequency, and the output current is independent of the voltage between the output and common terminal. Furthermore, the voltage between the input and common terminals is ideally zero because this condition allows the entire supply voltage to appear across the input current source, simplifying its transistor-level design. More than one input and/or output terminals are sometimes used.

For MOS transistor, a commonly used parameter for the characterization of channel length modulation (λ) is the reciprocal of the Early voltage (V_A), $\lambda = 1/V_A$. Thus we can include the effect of channel-length modulation in the *I-V* characteristics. If one assumes that the transistors operate in the saturation region $(V_{DS} > V_{GS} - V_T)$, the value of I_D in this region can be given by

$$I_D = \frac{\mu_n C_{ox} W}{2L}\left(V_{GS} - V_T\right)^2\left(1 + \lambda V_{DS}\right) \tag{2.1}$$

where the parameters are:

μ_n	surface mobility of the channel, $\left(cm^2/volt \cdot \sec\right)$
$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$	gate oxide capacitance density, $\left(F/cm^2\right)$
W	effective channel width, (m)
L	effective channel length, (m)
V_T	threshold voltage, (volt)
λ	channel length modulation parameter, ($volt^{-1}$)

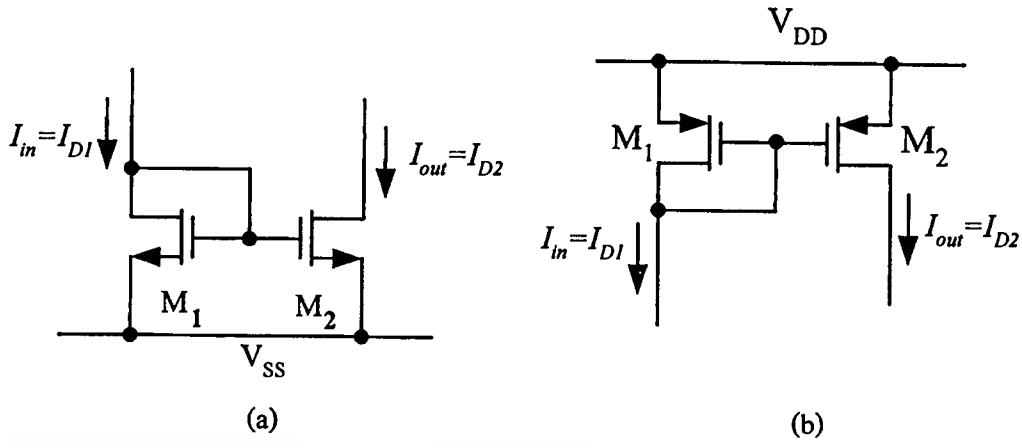


Fig. 2.2 Simple MOS current mirrors

(a) NMOS current mirror (b) PMOS current mirror

A simple realization of a CMOS current-mirror is presented in Fig. 2.2. From the circuit

$$V_{GS2} = V_{T2} + \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}(W/L)_2}} = V_{GS1} = V_{T1} + \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}(W/L)_1}} \quad (2.2)$$

If the transistors are identical, $(W/L)_2=(W/L)_1$, and therefore we get the relation of the currents

$$I_{out} = I_{D2} = I_{D1} \quad (2.3)$$

Eqn. (2.3) shows that the current that flows in the drain of M_1 is mirrored to the drain of M_2. Using Kirchhoff 's Curent Law, eqn. (2.3) yield.

$$I_{out} = I_{D2} = I_{in} \quad (2.4)$$

Thus for identical device operating in the saturation region with infinite output resistance, the gain of the current mirror is unity. This result holds when the gate currents are zero; that is, eqn. (2.4) is at least approximately correct for DC and low-frequency AC currents. As the input frequency increases, however, the gate currents of M_1 and M_2 increase because each transistor has a nonzero gate-source capacitance. In practice, the devices need not be identical. Then from eqns. (2.2) and (2.4),

$$I_{out} = \frac{(W/L)_2}{(W/L)_1}\left(\frac{V_{GS2}-V_{T2}}{V_{GS1}-V_{T1}}\right)^2 \cdot \frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}} \frac{\mu_{n2}C_{ox2}}{\mu_{n1}C_{ox1}} I_{D1}$$

$$= \frac{(W/L)_2}{(W/L)_1}\left(\frac{V_{GS2}-V_{T2}}{V_{GS1}-V_{T1}}\right)^2 \cdot \frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}} \frac{\mu_{n2}C_{ox2}}{\mu_{n1}C_{ox1}} I_{in} \qquad (2.5)$$

Then, if the effect of source and load impedances is first neglected, the current-mirror large signal equation shows current gain (A_i) proportional to the aspect ratios of transistors M_1 and M_2, with certain additional dependencies

$$A_i = \frac{I_{out}}{I_{in}} = \frac{(W/L)_2}{(W/L)_1}\left(\frac{V_{GS2}-V_{T2}}{V_{GS1}-V_{T1}}\right)^2 \cdot \frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}} \frac{\mu_{n2}C_{ox2}}{\mu_{n1}C_{ox1}} \qquad (2.6)$$

From this equation, we found that the process variation of the channel width W, channel length L, mobility μ_n, and oxide thickness t_{ox} can produce linear gain error.

If the effect of channel-length modulation can be neglected ($\lambda = 0$), assume the process parameters such as V_T, μ_n, C_{ox}, of MOS transistor are matched and $V_{DS2} \cong V_{DS1}$. The eqn. (2.5) can be rewritten as

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{D1} = \frac{(W/L)_2}{(W/L)_1} I_{in} \qquad (2.7)$$

and the current gain (A_i) in eqn. (2.6) can be rewritten as

$$A_i = \frac{I_{out}}{I_{in}} = \frac{(W/L)_2}{(W/L)_1} \qquad (2.8)$$

Eqn. (2.8) shows that the gain of the current mirror can be larger or smaller than unity because the transistor sizes can be ratioed. To ratio the transistor sizes, either the widths (W) or the lengths (L) can be made unequal in principle.

Due to finite input and output impedances have a significant effect on the current mirror gain accuracy. The small signal equivalent circuit of the current mirror will be used to analyze the input impedance , the output impedance and the current gain.

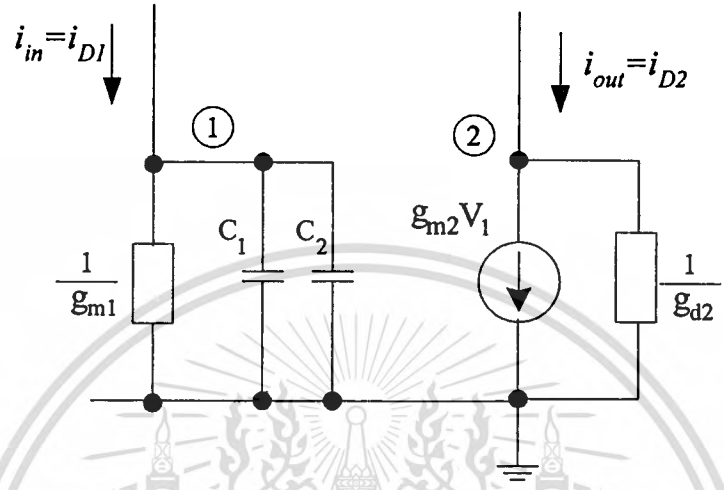


Fig. 2.3 Small signal equivalent circuit of NMOS current mirror in Fig. 2.2

From Fig. 2.3, the small-signal input impedance of the current mirror depends on the transconductance of the input transistor M_1

$$r_{in} \approx \frac{1}{g_{m1}} = \frac{1}{\sqrt{2\mu_{o1}C_{ox1}\frac{W_1}{L_1}I_{D1}}} \tag{2.9}$$

where g_{m1} is the transconductance of transistor M_1, and the small-signal output impedance depends on the drain-source conductance of the output transistor M_2, accordingly

$$r_{out} \approx \frac{1}{g_{d2}} = \frac{1}{\lambda I_{D2}} \tag{2.10}$$

where g_{d2} is the drain-source conductance of the transistor M_2.

The relation between the input current (I_{in}) and the output current (I_{out}) of the basic current mirror can be written as

$$I_{out} = \frac{g_{m2}}{g_{m1}} I_{in} \tag{2.11}$$

For the high frequency response of the simple current mirror, from Fig. 2.3 the transfer function of input current and output current ($i_{out}(s)/i_{in}(s)$) can be expressed in eqn. (2.12)

$$\frac{i_{out}(s)}{i_{in}(s)} = \frac{g_{m2}}{g_{m1}} \cdot \frac{1}{1 + \frac{s(C_1 + C_2)}{g_{m1}}} \tag{2.12}$$

where $C_i = C_{gsi} + C_{gdi}$

C_{gsi} is the gate-source capacitance of transistor M_i, (F)

C_{gdi} is the gate-drain capacitance of transistor M_i, (F)

The basic current mirror characteristics from eqns. (2.5) to (2.12) show that the current gain can be controlled by the channel width (W) and/or channel length (L) of the MOS transistor.

From eqn. (2.12) the cut-off frequency of the basic current mirror in Fig. 2.2 which depending on one pole can be expressed as eqn. (2.13)

$$f_{-3dB} \cong \frac{g_{m1}}{2\pi(C_1 + C_2)} \tag{2.13}$$

Eqn. (2.13) shows that the dominant pole of the basic current mirror is normally situated at quite high frequencies because of the low value of g_{m1}. Thus, the current mirror operates well up to high frequencies.

In modern sub-micron CMOS processes the g_m/g_{ds} ratio is less than 100 and consequently results in not a significant gain error. This gain error is usually reduced by increasing the output impedance using different cascode mirror topologies rather than the simple two transistor current-mirror. In this case, however, the drain-source voltages $V_{DS1} \neq V_{GS}$ gain error as expressed in eqn. 2.6 may result. Moreover, these drain voltages are signal dependent and thus the channel length modulation λ, which continuously increases as progressively shorter channel length devices are

introduced, can additionally produce significant amount of distortion. Therefore, topological improvements must be made in the current-mirror in order to maintain the drain-source voltages V_{DS1} and V_{DS2} as equal as possible. This is achieved by using the current-mirror topologies rather than the simple current-mirror or the cascode current-mirror that shows in Fig. 2.4. The additional current-mirror constructed of transistors M_3 and M_4 is added on top of the original current mirror in order to force the drain voltage V_{DS2} of the transistor M_2 equal to $V_{DS1} = V_{DS2} = V_{GS}$ [19]. Unfortunately, this reduces significantly the input and output voltage ranges and thus the minimum supply voltage of the circuit is quite high.

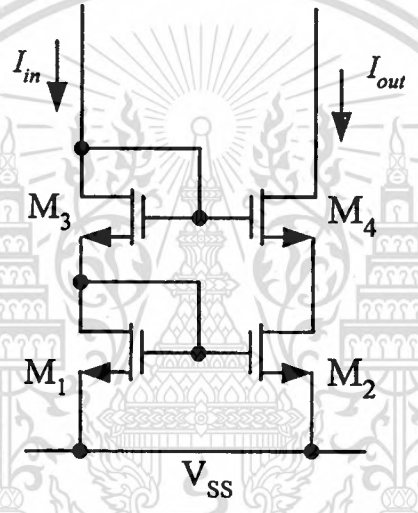


Fig. 2.4 A simple four transistor cascode current mirror.

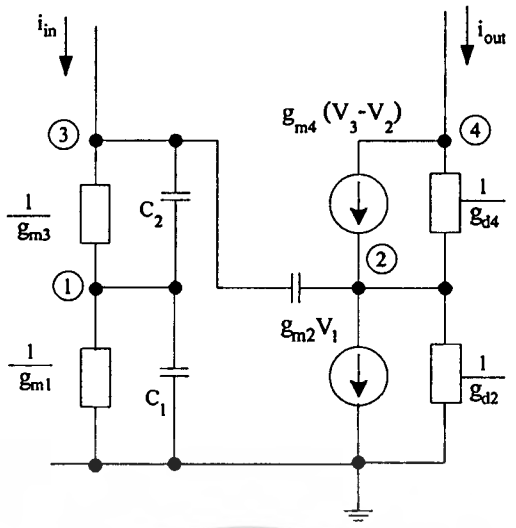


Fig. 2.5 Small signal equivalent circuit of cascode current mirror in Fig. 2.4

From the small signal equivalent circuit in Fig. 2.5, the relation between the input current (i_{in}) and the output current (i_{out}) of the cascode current mirror in Fig 2.3 can be written as

$$i_{out} = \frac{g_{m2}g_{m4}}{g_{m1}g_{m3}} i_{in} \tag{2.14}$$

The input impedance of the cascode current mirror can be written as

$$r_{in} = \frac{g_{m1} + g_{m3}}{g_{m1}g_{m3}} \tag{2.15}$$

and the output impedance can be written as

$$r_{out} = r_{d2} + r_{d4} + g_{m4}r_{d2}r_{d4} \cong g_{m4}r_{d2}r_{d4} \tag{2.16}$$

where r_{di} is the drain-source resistance of the MOS transistor M_i

The frequency response of the cascode current mirror in Fig. 2.5 can be expressed as

$$\frac{i_{out}(s)}{i_{in}(s)} = \frac{g_{m4}}{g_{m1}} \left[\frac{1}{\frac{C_1(C_2+C_3)}{g_{m1}g_{m2}} s^2 + \frac{\left((C_1+C_2)(g_{m1}+g_{m2})+C_{gs4}g_{m2}\right)}{g_{m1}g_{m2}} s+1} \right] \quad (2.17)$$

Eqn. (2.17) shows that the cascode current mirror has a complex pole. Therefore, its bandwidth of the cascode current mirror is less than the basic current mirror. However, the cascode current mirror has higher output resistance and less error in current i_{out}.

Table 2.1 Characteristics summary of the basic current mirror and cascode current mirror

Current mirror	Input resistance (r_{in})	Output resistance (r_{out})	Frequency response $i_{out}(s)/i_{in}(s)$
Basic Current mirror	$r_{in} = 1/g_{m1}$	$r_{out} = 1/g_{d2}$	$\frac{i_{out}(s)}{i_{in}(s)} = \frac{g_{m2}}{g_{m1}} \left(\frac{1}{1+\frac{S(C_1+C_2)}{g_{m1}}} \right)$
Cascode Current mirror	$r_{in} = \frac{g_{m1}+g_{m3}}{g_{m1}g_{m3}}$	$r_{out} = r_{d2} + r_{d4} + g_{m4}r_{d2}r_{d4}$ $\cong g_{m4}r_{d2}r_{d4}$	$\frac{i_{out}(s)}{i_{in}(s)} = \frac{g_{m4}}{g_{m1}} \left[\frac{1}{\frac{C_1(C_2+C_3)}{g_{m1}g_{m2}} s^2 + \frac{\left((C_1+C_2)(g_{m1}+g_{m2})+C_{gs4}g_{m2}\right)}{g_{m1}g_{m2}} s+1} \right]$

2.2 CMOS current squarer circuit

Squarer circuit is one of the useful basic circuit functions in the amplitude domain, the need for which arises quite often. They are essential to the extraction of the exact RMS value of a signal, and in power measurement in general.

Recently, the realization of squarer circuits have been proposed for various techniques [7], [21]-[30]. For [21]-[23], the circuits are designed by using the operational amplifier (op-amp) where the circuit designs with transistors that are operated in the saturation and the triode region. The output current is the function of their input voltage squared. On the other hand, the works in [24] - [30] are designed by using only MOS transistors. These circuits are function as a voltage-

mode squarer circuit. The circuits are designed by using square-law characteristic. All of MOS transistor are biased in the saturation region. Finally, the [7] is a current-mode squarer circuit.

Some example of the proposed squarer circuits will be outlined as follow.

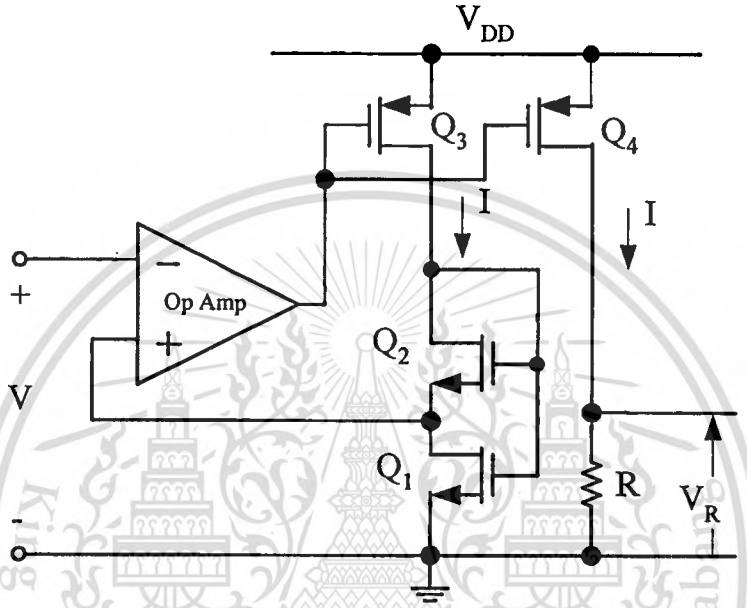


Fig. 2.6 Squarer circuit [21]

The squarer circuit that shown in Fig. 2.6 was proposed by *I.M. Filanovsky and H.P. Baltes* [21]. The circuit structure include an operational amplifier (op-amp) and nested transistor pair (Q_1 and Q_2) where transistor Q_1 operates in triode region. When the input voltage (V) is applied to the op-amp, the op-amp output voltage will force the transistor Q_3 and the current I, which will flow through the transistors Q_1 and Q_2 can be calculate as follow.

The transistor Q_2 will be pinch-off and transistor Q_1 will be forced into the triode region of operation. The gate-source voltage V_{GS2} of the transistor M_2 will be

$$V_{GS2} = V_{TN} + \sqrt{\frac{2I}{k_2}} \tag{2.18}$$

where V_{TN} is the threshold voltage of n-channel transistor and $K_2 = \mu_n C_{ox}(W/L)_2$ from the other side, due to the triode operation of Q_1, the current I will satisfy the equation

$$I = K_1(V_{GS1} - V_{TN})V - \frac{K_1 V^2}{2} \tag{2.19}$$

where $K_1 = \mu_n C_{ox}(W/L)_1$. Besides,

$$V_{GS1} = V + V_{GS2} \tag{2.20}$$

substituting (2.18) and (2.20) into (2.19), one can find that

$$I = K_1\left[\sqrt{(K_1/K_2)}\sqrt{(K_1/K_2)+1} + (K_1/K_2) + 1/2\right]V^2 \tag{2.21}$$

Transistors Q_3 and Q_4 are used to copy the current I to the output of the squaring circuit. Eqn. (2.21) shows that this circuit can operate as squarer function. The output current is proportional to the square of the input voltage. Due to this technique requires the operational amplifier, the circuit performance depends on the performance of the operational amplifier. Such as, the bandwidth is limited, since the cut-off frequency of the open-loop gain of the op-amp is typically in the range of 10-100Hz.

Fig. 2.7 shows the voltage-mode squarer circuit that proposed by *O.A. Seriki and R.W. Newcomb* [28]. The circuit is designed by the used of CMOS transistors. The circuit is function as voltage-mode squarer circuit.

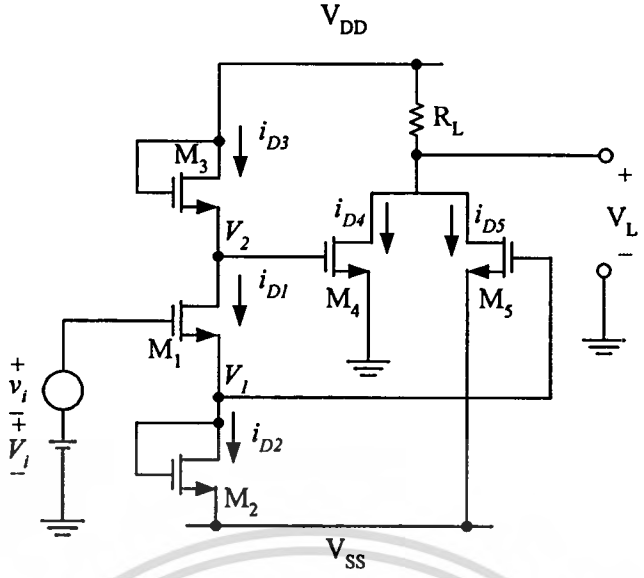


Fig. 2.7 Squarer circuit proposed by O.A. Seriki and R.W. Newcomb [2.8]

This circuit is a two-stage arrangement. The first stage which consisting of equal transistors M_1, M_2 and M_3 (NMOS) is a linear amplifier, where the output voltages V_1 and V_2 are measured with respect to ground, having their signal components the negative of each other. In the second stage, which is the squaring function, the current i_L that flowing through R_L is the sum of the drain currents i_{D4} and i_{D5} of the two equal transistors M_4 and M_5. These currents being squares of the inputs when the transistors are properly biased. For the circuit analysis, assuming the transistors are biased to operate in the square-law region, the drain current i_D of an n-channel MOS transistors is related to its gate-to-source voltage, V_{GS}, by

$$i_D = K(V_{GS} - V_T)^2 \tag{2.22}$$

Since the current i_{D1}, i_{D2} and i_{D3} flowing through the transistors are the same, the gate-to-source voltage V_{GS1}, V_{GS2} and V_{GS3} are equal. Since $V_{GS1}+V_{GS2}=2V_{GS2}=2V_{GS3}=V_1+V_{SS}+v_1$, Kirchhoff's voltage law shows that the voltages v_1 and v_2 are given by

$$v_1 = V_{DD} - V_{GS3} = V_{DD} - \frac{1}{2}(V_1 + V_{SS}) - \frac{1}{2}v_i \tag{2.23}$$

$$v_2 = V_{GS2} - V_{SS} = \frac{1}{2}(V_1 - V_{SS}) + \frac{1}{2}v_i \tag{2.24}$$

Hence, a signal v_i fed into the input of the first stage divided equally, but with opposite signs, between v_1 and v_2 to form the signal components of the voltages which control the gates of transistors M_4 and M_5 of the second stage.

The current i_L flowing through the resistor R_L is the sum of the drain current i_{D4} and i_{D5}. The total out put voltage, v_L, is given by

$$v_L = V_{oo} - KR_L(a_2 - a_1)v_i - \frac{1}{2}KR_L v_i^2 \qquad (2.25)$$

where V_{oo} is the dc bias component , $V_{oo} = V_{DD} - KR_L(a_1^2 + a_2^2)$, $a_1 = V_{DD} - \frac{1}{2}V_{SS} - \frac{1}{2}V_i - V_T$ and $a_2 = \frac{1}{2}V_{SS} + \frac{1}{2}V_i - V_T$.

From eqn. (2.25), since this second term is not desired in the output of a squaring circuit, it contributes to the amount of distortion or error introduced by the circuit. The last term is an undistorted reproduction of the square of the input signal and this is the desired output signal. The second term can be reduced or eliminated completely by satisfying the condition a_2 - a_1= 0. We can found that this circuit can function as voltage squaring circuit.

The circuit is shown in Fig. 2.8 that has been proposed in [7], is the current mode squarer circuit. This work is the one of the method that realized by using the square law characteristic of MOS transistor where all transistors are biased in saturation region. The circuit structure is simple and provides good accuracy over a wide range of input currents. Therefore, in this thesis, the current squarer circuit as shown in Fig. 2.8 has been used for designing the proposed true rms to dc converter. The circuit structure composes of two current mirrors and the output current is the function of the square input current and DC bias current. This current squarer circuit description will be outlined in this section.

2.2.1 Circuit Description

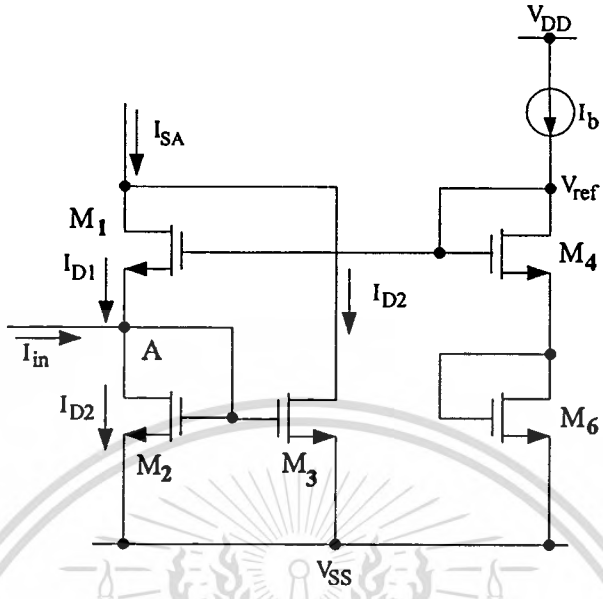


Fig. 2.8 CMOS current squarer circuit

The operation of the CMOS current squarer circuit of the Fig. 2.8 is based on the square law characteristic of MOS transistors biased in the saturation region [31], [32]. Transistors M_1 through M_3 function as a current squarer, where M_4 and M_6 and the current source I_b formed as the current-controlled bias circuit. The input signal current I_{in} is injected into point A. From the squarer circuit in Fig. 2.8, consider the transistor M_1, M_3, M_4 and M_6, we will obtain

$$V_{GS4} + V_{GS6} = V_{GS1} + V_{GS3} \tag{2.26}$$

Assume all MOS transistors are biased in the saturation region, the square-law behavior for the current –voltage relationship of the MOS transistor in saturation is assumed as

$$I_D = K\left(V_{GS} - V_T\right)^2 \tag{2.27}$$

where V_{GS} can be expressed as

$$V_{GS} = \sqrt{\frac{I_D}{K}} + V_T \tag{2.28}$$

from eqns. (2.26) and (2.28), set $V_{T1} = V_{T2} = V_{T4} = V_{T6} = V_T$ and $K_1 = K_2 = K_4 = K_6 = K$ and from circuit analysis $I_{D4} = I_{D6} = I_b$, therefore

$$2\sqrt{I_b} = \sqrt{I_{D1}} + \sqrt{I_{D3}} \tag{2.29}$$

squaring the eqn. (2.29) given

$$4I_b = I_{D1} + 2\sqrt{I_{D1}I_{D2}} + I_{D2} \tag{2.30}$$

From routine circuit analysis, the relation between I_{D1}, I_{D2} and I_{in} can be expressed as

$$I_{D1} = I_{D2} - I_{in} \tag{2.31}$$

or

$$I_{D2} = I_{D1} + I_{in} \tag{2.32}$$

From eqns. (2.30) and (2.31), we will obtain

$$2\sqrt{I_{D2}^2 - I_{in}I_{D2}} = 4I_b + I_{in} - 2I_{D2} \tag{2.33}$$

By squaring eqn. (2.33), the drain current of transistor M_2, (I_{D2}) can be written as

$$I_{D2} = \frac{16I_b^2 + 8I_bI_{in} + I_{in}^2}{16I_b} \tag{2.34}$$

Eqn. (2.34) can be rewritten as

$$I_{D2} = \frac{(4I_b + I_{in})^2}{16I_b} \qquad , |I_{in}| \le 4I_b \tag{2.35}$$

From eqns. (2.29) and (2.34), the drain current of transistor M_1, (I_{D1}) can be written as

$$I_{D1} = \frac{16I_b^2 - 8I_bI_{in} + I_{in}^2}{16I_b} \tag{2.36}$$

or

$$I_{D1} = \frac{(4I_b - I_{in})^2}{16I_b} \quad , |I_{in}| \le 4I_b \tag{2.37}$$

The unity gain positive current mirror CM_1, formed by M_2 and M_3, reflects the current I_{D2} in order to add with the current I_{D1}. Then, from eqns. (2.35) and (2.36), the summation of the currents I_{D1} and I_{D2} or $I_{SA} = I_{D1}+I_{D2}$ becomes

$$I_{SA} = I_{D1} + I_{D2} \tag{2.38}$$

Replace I_{D1} and I_{D2} in eqn. (2.32) with I_{D1} and I_{D2} from eqns. (2.34) and (2.36) respectively , I_{SA} can be rewritten as

$$I_{SA} = 2I_b + \frac{I_{in}^2}{8I_b} \tag{2.39}$$

We can see that I_{SA} consists of the signal current which is the squaring of the input signal I_{in} and the DC current $2I_b$. If the DC current $2I_b$ can be compensated, the circuit will be functioned as a squarer/divider circuit, which can be used as a basic cell to realize rms-to-dc converter by the implicit computation method in this thesis.

2. 3 A balanced CMOS OTA

An operational transconductance amplifier (OTA), also called a transconductance element or a transconductance, is a device that converts voltage inputs to current outputs (or a voltage controlled current source) such that $i_{out} = g_m V_{in}$. The transconductance gain g_m can usually be varied over a wide range by adjusting an external DC bias current I_B.

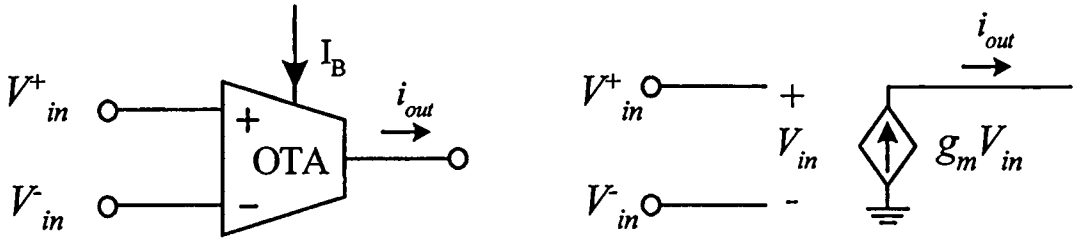


Fig. 2.9 Ideal model of the operational transconductance amplifier (OTA)

In Fig. 2.9, the small-signal model for an ideal OTA is seen to be a differential input voltage-controlled current source (VCCS), with infinite input and infinite output impedances. An OTA is a voltage controlled current source, more specially the term "operational" comes from the fact that it takes the difference of two voltages as the input for the current conversion. The ideal transfer characteristic is therefore

$$i_{out} = g_m \left(v_{in}^+ - v_{in}^- \right) \tag{2.40}$$

or, by taking the pre-computed difference as the input,

$$i_{out} = g_m v_{in} \tag{2.41}$$

with the ideally constant transconductance g_m as the proportional factor between the two. In practice the transconductance is also a function of the input differential voltage, as we will later see.

In the literature, many design techniques have been proposed for realizing the operational transconductance amplifier. For CMOS-based OTA, a well-known practical linearization technique for transconductors is source degeneration [33]-[35] and by using cross-coupled differential pairs operating in saturation, e.g. [36]-[40]. Some of these realizations are not intended for low-power usage, others have problems with the body effect and/or channel length-modulation. In addition an interesting approach of a low-power linear OTA working in the non-saturation region has been proposed in [41]. However a double supply voltage and matching of a

p-type and n-type OTA is needed. As a matter of principle the transconductances for positive and negative input voltages do not match exactly.

In this thesis, a balanced CMOS OTA has been used for realizes the transconductor which can be electronically and linearly tuned. The circuit structure is composed of a *V/I* converter (or differential amplifier) and three current mirrors. The circuit description will be described. Firstly a simple CMOS OTA will be introduced.

In Fig. 2.10 a simple CMOS OTA is shown, the simple CMOS OTA consists of a self-bias MOS transistor differential stage with active load. Transistors M_1 and M_2 form a matched transistor pair. Transistors M_3 and M_4 have equal W/L, as well. All current levels are determined by current source I_B, half of which flows through M_1 and M_3, with the other half flow through M_2 and M_4.

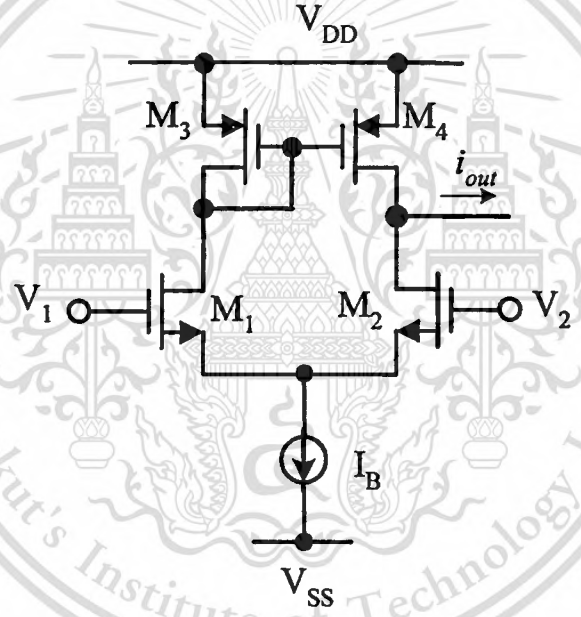


Fig. 2.10 A simple CMOS OTA

At low frequency, the transconductance of the OTA is given by $G_m=g_{m1}=g_{m2}$. It is also given by

$$G_m = \sqrt{2I_B K} \tag{2.42}$$

in which $K=\mu_n C_{ox} W/2L$ is the transconductacne parameter for MOS transistor in saturation. Also note that the current I_B in eqn.(2.42) is the total current, which is twice the current through one transistor.

For the structure of this simple CMOS OTA, their input stage consists of a differential pair loaded by a current mirror. This load is thus very asymmetrical due to only M_3 is connected as a diode that causes V_{DS3} fixed, whereas V_{DS4} is varied up to load. Therefore, the DC current which flows through M_1, M_3, and the other one flowing through M_2, M_4 are unbalance. From this result, the symmetrical CMOS OTA or balanced CMOS OTA is preferred for the circuit design in thesis, which provides the same load to both input devices.

Simple balanced CMOS OTA

The circuit schematic of the balanced CMOS OTA with symmetrical input stage is given in Fig. 2.11. The differential pair is formed by the input transistors M_1 and M_2. They drive their output currents in two transistors, M_3 and M_5, which are connected as diodes. They are the inputs of two current mirrors with current multiplication factor (current mirror ratio). The output current of transistor M_4 is then mirrored once more in current mirror M_7, M_8, with the unity gain current mirror, as indicated. In addition, for the balanced OTA structure, current mirrors constructed of transistor M_3-M_4 and M_5-M_6 will force the drain voltage V_{DS1} of transistor M_1 equal to V_{DS2} of transistor M_2.

2.3.1 Circuit Descriptions of a balanced CMOS OTA

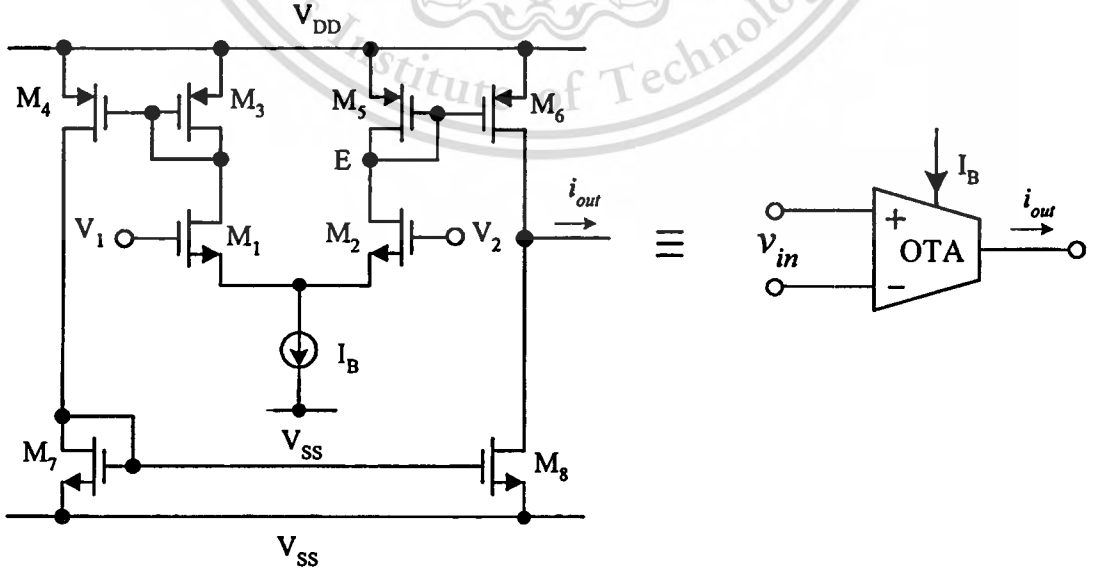


Fig. 2.11 Schematic diagram of a balanced CMOS OTA

For the purpose of the following analysis, we will assume that all MOS devices operate in the saturation region. This means that the transistor drain current I_D is characterized by a square-law model as

$$I_D = \begin{cases} K(V_{GS} - V_T)^2 & , \ for \ V_{GS} > V_T \\ 0 & , \ for \ V_{GS} \le V_T \end{cases} \quad (2.43)$$

where the transconductance parameter $K = \mu_n C_{ox} W/2L$, μ_n is the mobility of the carrier, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length, and V_{GS} and V_T are the gate-to-source and threshold voltages, respectively.

If we let V_{in} is the differential input voltage ($V_{in}=V_1-V_2$), i_{out} is the output current and I_B is the bias current. Let us assume that M_1 and M_2 are perfectly matched and the current mirrors have unity current gain. By using eqn. (2.43), the differential output current of the circuit in Fig. 2.11 can be given by [42]

$$\begin{aligned} i_{out} &= i_2 - i_1 \\ &= \sqrt{2I_B K} \cdot V_{in} \cdot \sqrt{1 - \frac{KV_{in}^2}{2I_B}}, \quad for -\sqrt{\frac{I_B}{K}} \le V_{in} \le \sqrt{\frac{I_B}{K}} \end{aligned} \quad (2.44)$$

The transconductance gain (g_m) of the MOS coupled pair can be derived by taking the derivative of (2.44) with respect to V_{in}, yielding

$$g_m = \left.\frac{di_{out}}{dV_{in}}\right|_{V_{in}=0} = \sqrt{2I_B K}, \quad for -\sqrt{\frac{I_B}{K}} \le V_{in} \le \sqrt{\frac{I_B}{K}} \quad (2.45)$$

From the eqn. (2.44), the current i_{out} can rewritten as

$$i_{out} = g_m V_{in} = \sqrt{2I_B K} \cdot V_{in} \quad (2.46)$$

Eqn. (2.45) shows that the transconductance gain (g_m) of the OTA can be varied by the bias current I_B, but in the form of square root function. In addition, in order to operate in the low distortion range, the input voltage V_{in} should be in the range of [20]

$$V_{in} \leq \left| \sqrt{I_B / K} \right| \tag{2.47}$$

Moreover, Fig. 2.12 is a multiple current output or fully differential OTA . As shown in dashed-line the multiple current outputs OTA can be implemented by current replicas using current mirrors formed by transistors M_9-M_{12}. However, the method that uses two OTAs in parallel input terminals to produce multiple outputs can also be used [43].

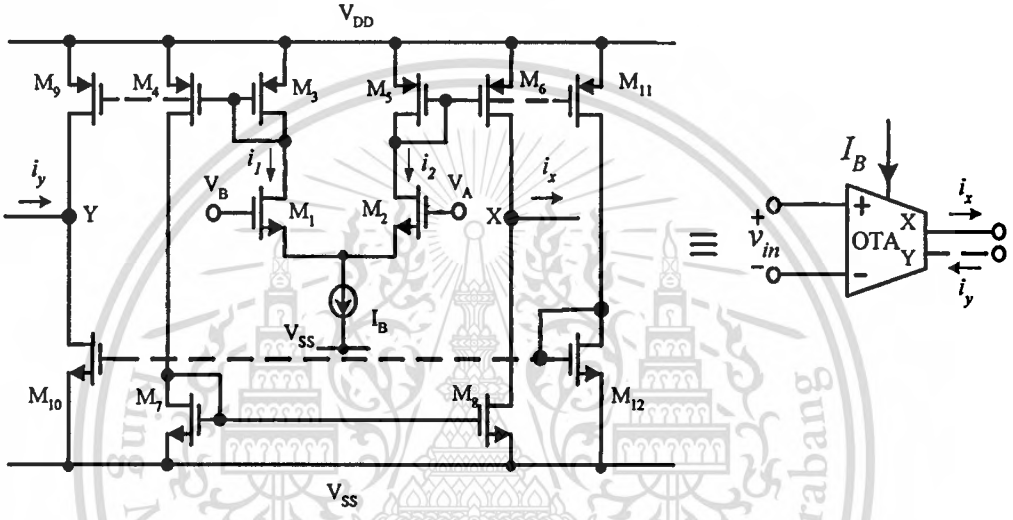


Fig. 2.12 Schematic diagram of the fully differential CMOS OTA

Where v_{in} is the differential input voltage (v_{in}=V_A-V_B), I_x is the output current and I_B is the bias current. The differential output current of the circuit of Fig. 2.12 can be given by

$$i_x = i_2 - i_1 = \sqrt{2I_B K} \cdot v_{in} \cdot \sqrt{1 - \frac{K v_{in}^2}{2I_B}}, \quad for - \sqrt{\frac{I_B}{K}} \leq v_{in} \leq \sqrt{\frac{I_B}{K}} \tag{2.48}$$

The transconductance gain (g_m) of the fully differential OTA can be derived by taking the derivative of (2.48) with respect to v_{in}, yielding

$$g_m = \left. \frac{di_x}{dv_{in}} \right|_{v_{in}=0} = \sqrt{2I_B K} \tag{2.49}$$

Thus we can obtain the following equation for a small signal;

$$i_x = g_m v_{in} = \sqrt{2I_B K} \cdot v_{in} \tag{2.50}$$

Eqn. (2.49) shows that the transconductance gain (g_m) of the OTA can be varied by the bias current I_B, but in the form of a square root function. It should be noted that the transconductance gain (g_m) of the balance CMOS OTA shown in Fig. 2.11 will provide low harmonic distortion if the input voltage is limited in the range of

$$g_m = \sqrt{2I_B K}, \quad for -\sqrt{\frac{I_B}{K}} \le v_{in} \le \sqrt{\frac{I_B}{K}} \tag{2.51}$$

The effect from the non-ideality can be studied through the use of the OTA small signal model that shown in the Fig. 2.13,

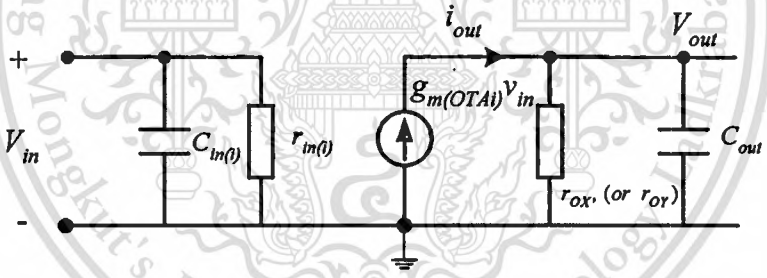


Fig. 2.13 Small signal model of a balanced CMOS OTA

where $r_{in(i)}$ is the input resistance of OTAi, r_{OX} or r_{OY} is the different output resistance at port X or port Y, $C_{in(i)}$ is the input capacitance of OTAi and $C_{out(i)}$ is the output capacitance of OTAi [20],[25],[26]. The differential output resistance r_{OX} is approximately equal to the output resistance of the current mirror M_5-M_6 in parallel with the output resistance of the current mirror M_7-M_8 or r_{OX} approximate $1/(g_{d6}+g_{d8})$ and , similarly, r_{OY} approximate $1/(g_{d9}+g_{d10})$

CHAPTER 3

CMOS Based True RMS-to-DC Converter

3.1. Introduction

The Root-Mean-Square (RMS) value of arbitrary signal is one of important parameters in electronics measurements, especially for digital multimeters (DMM's). The RMS value is the parameter for measuring the size of signal. As the name suggests; this parameter consists of the square root of the average value of the square of the signal. Moreover, the RMS value is such an important measurement for the following reason: It is the most common way of describing the size of an AC signal. The RMS value is a measure of the energy content in the signal since the RMS value of an AC voltage or signal is defined as being equivalent to that DC voltage or current which has a similar heating effect of the AC signal when applied to an identical resistor. In addition it is useful in some statistical operations; for example with any stationary, zero mean random signal, the RMS value is equal to the standard deviation of the signal.

A true RMS-to-DC converter is a device which converts a signal (DC, AC, AC+DC) for all waveforms to its equivalent DC heating value which proportional to the square root of the average of the input waveform squared. It is an important instrument that used for measuring the average energy content in an electrical signal. This device found useful in the fields of instrumentation, communication and display systems [1]. Automatic gain control and digital multimeters are examples of these applications.

To realize this RMS converter, we have two alternative methods; a comparing and a computing methods.

The comparing method, which is based on a thermal principle or the thermal RMS-to-DC converter [44],[45]. This method is achieved by converting an unknown voltage or current into heat from a known value of resistance. The squaring of the input signal is realized by measuring the temperature of a resistor, which is heated by the Joule heat of the electrical current. The dissipated energy is proportional to the square of the input signal. Integration can be achieved by using the thermal time constant of the circuit or by an extra electronic integration circuit. Most of the thermal converters use a feedback system, which compares the temperature of a dc-driven resistor with the temperature of the resistor driven by the input signal. The temperature can be

measured using a bipolar transistor [46] or a thermopile [47], which can be realized by using extra bulk micromachining steps. The thermal conversion is the simplest method in theory, but however, it is the most difficult and expensive to implement.

The computing method is based on analog signal processing or digital signal processing. Although the analog processing method using translinear property of bipolar circuitry has led to elegant solution [4],[6],[48], however, these converters are difficult to implement in standard CMOS processes. We can determine the RMS value of a wave form electronically with multiplier circuits by using either of the two techniques. One technique is knows as direct computation [Analog Device commercial IC AD737, AD736] which directly computes the square, the mean and square root of the analog value. Using this direct approach, a squarer, a low pass filter, and a square rooter are required according to the definition, resulting in a true rms-to-dc converter applicable to measuring an arbitrary waveform. This direct approach has a limited dynamic range because the stages following the squarer must try to deal with a signal that varies enormously in amplitude. The other one technique is indirect or implicit computation [commercial IC AD536A, AD637, MX636], [7],[49]-[51]. This approached uses feedback to perform the square root function implicitly or indirectly. Therefore the scheme requires only a squarer and a low pass filter to measuring an arbitrary waveform. Some advantages of implicit rms computation over other methods are fewer components, greater dynamic range, and generally lower cost.

Several methods to obtain true RMS-to-DC converters amenable to silicon implementation have been proposed [52]. However, in most cases, these converters are implemented by means of BJT transistors [6]. Thus, these techniques are difficult to translate to standard CMOS processes. An attempt to fill this gap is to employ an analog-to-digital converter and to perform digital processing [53],[54] that designed based on $\Delta\Sigma$ computational technique, but the extra circuitry needed leads to a considerable increment of chip area. In [55] another proposal employing continuous time analog processing and standard CMOS process are presented. In such an implementation, the dynamic MOS translinear principle are employed [4],[6]. The RMS to DC converter design based on CMOS technology has been also proposed [56]. The circuit design based on pseudo RMS-to-DC converter concept since it does not give, in the general case, an output proportional to the square root of the average of the input waveform squared.

In this thesis, through the use of a MOS transistor square law characteristic, a design technique for the realization of a true RMS-to-DC converter is proposed. The circuit is suitable

for all input wave forms. The conversion circuit performs the implicit computation scheme, by feedback the root-mean square current to be the circuit bias current. A full-wave rectifier is not required by the proposed realization scheme. The conversion circuit is simple, suitable for implementing in monolithic integrated form, and can be readily integrated as part of a larger system. The performance of the conversion circuit is studied from PSPICE simulation results and experimental results.

3.2 Exiting RMS-to-DC converters

Many true RMS-to-DC converters have been proposed [2]-[4], [57], most of them are design based on a bipolar integrated circuit technology. Their conversion schemes are mostly performed through the use of full-wave rectifiers and multiplier/divider circuits that employing a log-antilog principle. Due to the bandwidth and the slew-rate of the full-wave rectifiers, the useful frequency ranges of these converters are limited to less than 5 MHz. Commercial monolithic IC's for the RMS-to-DC converter are available. The popular examples from Analog Devices are the AD536/536AJ, AD636J, AD336J, AD737J, AD736 and AD737, from National Semiconductor is LH0097 and from Burr-Brown is 4340/4341. Most of these IC's are similarly built up from two main part: namely, a full-wave rectifier circuit and a multiplier/divider circuit employing a log-antilog principle. However, the bandwidth of the full-wave rectifiers and the high frequency performance of the IC's is also limited by their full-wave rectifier part.

New design techniques based on bipolar dynamic translinear circuits have been proposed to implement true RMS-to-DC converters [4],[6],[48]. Unfortunately, only circuit descriptions are outlined, but the characteristics of the RMS-to-DC conversion circuits have not been reported. In addition, their circuits are operated in only one quadrant and also required full-wave rectifiers. Recently, a new design technique for RMS-to-DC converter that realizes around a dual translinear-base squarer circuit, where the input current can be a two-quadrant current, is proposed [7]. The circuit exhibits a wide bandwidth because the full-wave rectifier is not required by this conversion scheme. However, the implementation scheme is rather complicate and suitable for implementing only in bipolar technology.

3.3 The proposed CMOS based true RMS-to-DC converter

In this section, through the use of a MOS transistor square law characteristic, a realization of a wide bandwidth current-mode CMOS true rms-to-dc converter is proposed. The conversion circuit performs the implicit computation scheme, by feedback the root-mean square current to be the circuit bias current. The square root function is obtained, while a square root circuit is not required by the proposed realization scheme. The circuit structure is simple since it requires only a squarer and a low-pass filter. The conversion circuit consumes very low power, due to the bias current of the circuit is provided by the root-mean-square current I_{RMS}.

Usually, for the RMS-to-DC converter through the implicit computation method, the circuit implements the root-mean-square function by performing two non-linear processes: squaring and square rooting. However, in this implementation, the squaring is the core of the circuit and the square rooting function is achieved through feedback. The proposed RMS-to-DC converter can be represented by the block diagram as shown in Fig. 3.1. It composes of the squarer/divider block, I_{in}^2 / I_b, in combination with the current mirrors CM_4 and CM_5 and the low-pass filter LPF (CM_3 and C_{AV}).

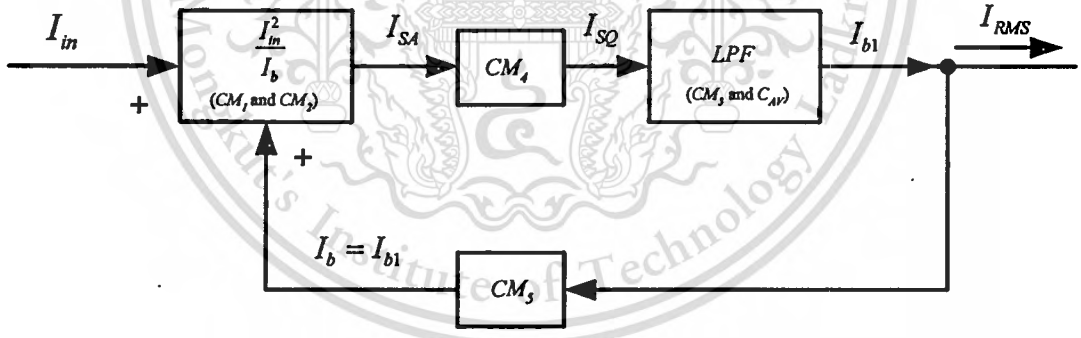


Fig. 3.1 Block diagram representation of the proposed true RMS-to-DC converter.

Noting that the conversion is performed through the feedback system, the instability will occur when the loop gain magnitude of the circuit exceeds one. However the loop gain magnitude of the proposed true RMS-to-DC converter is always less than one since the gain magnitude of CM_4 and CM_5 are unity and the gain magnitude of the LPF is always below one ($\omega >> 1/\tau$) for keeping the LPF work as ideal integrator. Therefore, the proposed RMS-to-DC converter is always stable.

3.3.1 Circuit descriptions of the true RMS-to-DC converter

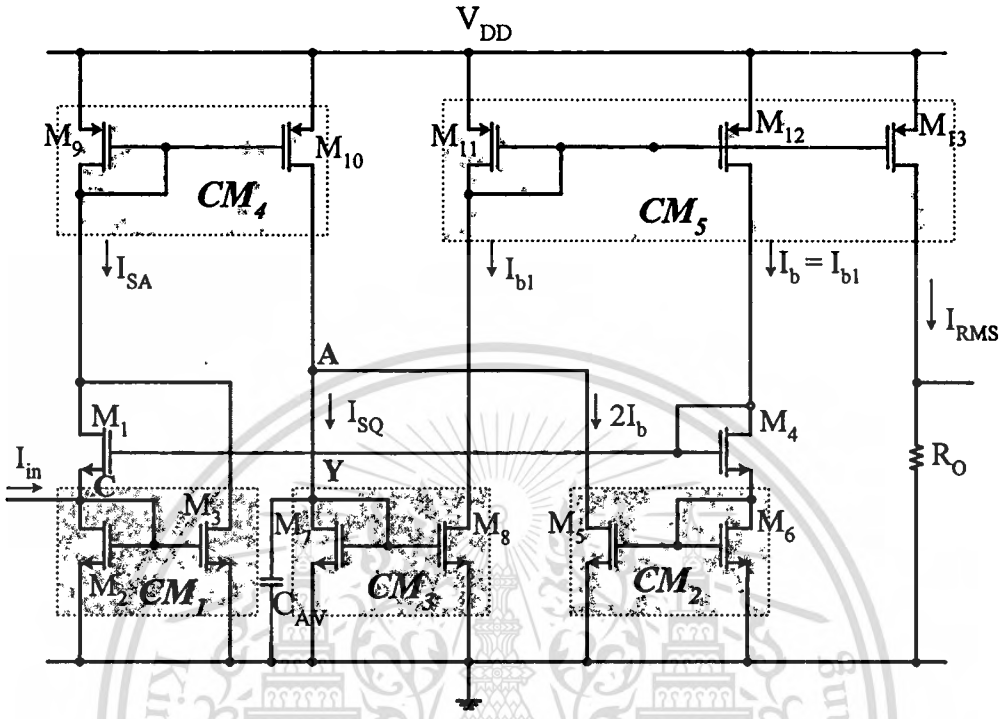


Fig. 3.2 The proposed true RMS-to-DC converter.

From Fig. 3.1 the schematic diagram of the proposed true RMS-to-DC converter can be represented as Fig. 3.2. In this figure, transistor M_1 to M_6 are formed as the current squaring circuit in combination with four current mirrors, CM_2 through CM_5, where the input signal current I_{in} is injected into point *C*. From routine circuit analysis, the summation of the currents I_{D1} and I_{D2} or $I_{SA} = I_{D1} + I_{D2}$ can be given by [analyzed in section 2.2.1]

$$I_{SA} = \frac{I_{in}^2}{8I_b} + 2I_b \qquad (3.1)$$

We can see that I_{SA} is the squaring of the input signal I_{in} plus the DC current $2I_b$. If the DC current $2I_b$ can be compensated, the circuit will be functioned as a squarer/divider circuit. Therefore in this proposed true RMS - to -DC converter is constructed such that the drain current of the

transistor M_5 of the current mirror CM_2 sources the current $2I_b$ from I_{SA}. Then from the eqn.(3.1), the current I_{SQ} can be expressed as

$$I_{SQ} = \frac{I_{in}^2}{8I_b} \tag{3.2}$$

In the figure, the current I_{SQ} passes through the averaging circuit or the first-order current mode low-pass filter (LPF) or the integrator circuit, which is consisting of the current mirror CM_3 (M_7 and M_8) and the grounded capacitor C_{AV} parallel connected to the mirror input [58]. The output current of the filter I_{bI} can be written as

$$I_{bI} \cong \frac{1}{8I_b\tau}\int I_{in}^2 dt \quad , \quad s\tau >> 1 \tag{3.3}$$

where $\tau = C_{AV}/g_{m7}$ is the time constant of the filter and g_{m7} is the transconductance of the transistor M_7. Due to the unity gain current mirrors CM_3 (M_7 and M_8) and CM_5 (M_{11} and M_{12}), the bias current I_b is derived by the current I_{bI} such that

$$I_b = I_{bI} \tag{3.4}$$

At the output, since we set the transistor channel widths of the current mirror CM_5 as $W_{13} = \sqrt{8}\, W_{11}$, it means the output current

$$I_{RMS} = \sqrt{8} I_b \tag{3.5}$$

From eqn. (3.3), since $I_b = I_{bI}$, by solving for I_b, we can write

$$I_b = \frac{1}{\sqrt{8}}\sqrt{\frac{1}{\tau}\int I_{in}^2 dt} \tag{3.6}$$

Then from eqns. (3.5) and (3.6), the current I_{RMS} can be given as

$$I_{RMS} = \sqrt{\frac{1}{\tau}\int I_{in}^2 dt} \tag{3.7}$$

We can see that the output current I_{RMS} is in the form of the root-mean-square value. It should be noted from the eqns. (3.2)-(3.7) that the square root function is achieved by the feedback of the current I_{b1} to be the bias current I_b of the circuit.

In order that the proposed RMS-to-DC converter gives a good performance for the required frequency range, the value of the capacitor C_{AV} must be chosen such that [55]

$$C_{AV} >> g_{m7(MAX)} / 4\pi f_{(MIN)} \tag{3.8}$$

where $f_{(MIN)}$ is the lower end of the frequency range of interest and

$$g_{m7(MAX)} = \sqrt{2K_p I_{SQ} W_7 / L_7} \tag{3.9}$$

W_7 is the channel width and L_7 is the channel length of the transistor M_7. From eqn. (3.2), the $g_{m7(MAX)}$ can be expressed as

$$g_{m7(MAX)} = \sqrt{2K_p I_M^2 W_7 / 8 I_b L_7} \tag{3.10}$$

where I_M is the peak amplitude of the input signal I_{in} and I_b is the circuit bias current. For example, for $K_P = 25.035\text{x}10^{-6}\ A/V^2$ and $W_7/L_7 = 20$, then $g_{m7(MAX)}$ can be given by

$$g_{m7(MAX)} = 0.0316\sqrt{\left(I_M^2 / 8 I_b\right)} \tag{3.11}$$

In this case, C_{AV} must be chosen such that

$$C_{AV} >> (8.891\times10^{-4}) I_M / \sqrt{I_b} f_{(MIN)} \tag{3.12}$$

It should be noted from (3.12) that the value of C_{AV} chosen is much depend on the ripple error that can be tolerate at the output. As a rule of thumb, the value of C_{AV} should exceed the right-hand term of eqn. (3.12) by the inverse of the fractional ripple error. For instance, for a 1 percent ripple

error, C_{AV} should be about 1/0.01 or 100 times as large as the right-hand term. For example, if a sinusoidal input signal with I_M = 1 mA, $f_{(MIN)}$ = 100 Hz, and the ripple error of 5 percent, then the averaging capacitance of C_{AV} = 10μF must be chosen.

The settling time, or time for the RMS converter to settle to within a given percent of the charge in RMS level, is set by the averaging time constant ($\tau = RC$). In this thesis, the settling time of the proposed RMS-to-DC converter is varies with the time constant of the first order low-pass filter, RC time constant ($\tau = C_{AV} / g_{m7}$), where g_{m7} is the function of I_{in} as expressed in eqn. (3.11). Due to the averaging capacitor connected across in the input part of the NMOS current mirror that form as the first order low-pass filter, the averaging time constant will increase as the input signal is reduced and vice versa. In addition, the settling time also varies with input signal levels, increasing as the input signal is reduced, and decreasing as the input is increased as shown in the simulation results section.

3.3.2 Circuit Performance

The ideal circuit performance that has been discussed in section 3.3.1 so far is based on the assumptions that the current mirrors have unity gain, transistors are perfectly matched, and each transistor is operated in its saturated regions and obeys a square law model. However, in practical realization, the finite values of transistor g_m and g_d and the transistor mismatched will contribute to deviate from the ideal performance. In the following, the transistor equivalent circuit and a small signal analysis will be used to study the performances of the conversion circuit of Fig.3.2.

3.3.2.1 Operating range

As we have been pointed out that the proposed true RMS-to-dc converter is based on the square law characteristic of MOS transistors biased in the saturation region. The square-law behavior for the current–voltage relationship of the MOS transistor in saturation is assumed as

$$I_D = \begin{cases} K(V_{GS} - V_T)^2 & , \ for \ V_{GS} > V_T \\ 0 & , \ for \ V_{GS} \le V_T \end{cases} \qquad (3.13)$$

where the transconductance parameter $K = \mu_n C_{ox} W/2L$, μ_n is the mobility of the carrier, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length, and V_{GS} and V_T are the gate-to-source and the threshold voltages, respectively.

Because of the input signal of the proposed true RMS-to-DC converter in Fig. 3.2 is a current signal. In order to remain a proper operation, the input current is restricted to the range

$$|I_{in}| < K(V_1 - 2V_T)^2 \tag{3.14}$$

$$V_1 = V_{DD} - V_{DS12(sat)} \tag{3.15}$$

Replace V_1 from (3.15) in (3.14), eqn. (3.14) can be rewritten as

$$|I_{in}| < K(V_{DD} - V_{DS12(sat)} - 2V_T)^2 \tag{3.16}$$

or, if biased with the relation of the DC bias current (I_b) which is fed back by the RMS current from the output. We will obtain

$$|I_{in}| < 4I_b \tag{3.17}$$

Eqns. (3.16) and (3.17) can be shown that the limitation of the input current is depend on the supply voltage and the dc bias current which should not over $4I_b$.

Due to the I_{RMS} is feedback to be the bias current I_b, or $I_b = I_{RMS}/\sqrt{8}$, of the circuit. Therefore, through I_b, the I_{RMS} should be large enough to bias all the transistors in their saturation regions. Table 3.1 shows the output currents in RMS values (I_{RMS}) and the DC bias currents (I_b) of the current signal input (I_{in}) for 3 difference input waveforms. There are square waveform, sine waveform and triangular waveform, respectively, where the I_{RMS} is equal to the root mean square value of the input signal, $I_{RMS} = \sqrt{\frac{1}{\tau}\int I_{in}^2 dt}$, and I_b is equal to the average of the input signal $I_b = I_{b1} = \frac{1}{8I_b\tau}\int I_{in}^2 dt$, or $I_b = I_{RMS}/\sqrt{8}$. In addition, this table shows the saturation condition of transistors when I_b is in the term of I_{in} for its input waveform.

Table 3.1 The relation between the bias current (I_b) and the input current (I_{in})

Input waveform	I_{in}	I_{RMS}	$I_b = I_{RMS}/\sqrt{8}$	**Saturation condition*** $I_{in} \le 4I_b$	**Note**
Square	$I_{in(peak)}$	$I_{in(peak)}$	$\frac{1}{\sqrt{8}} \cdot I_{in(peak)}$	$I_{in(peak)} \le 1.414 I_{in(peak)}$ $(I_{in} < 4I_b)$	Under the saturation condition
Sine	$I_{in(peak)}$	$\frac{1}{\sqrt{2}} \cdot I_{in(peak)}$	$\frac{1}{4} \cdot I_{in(peak)}$	$I_{in(peak)} \le I_{in(peak)}$ $(I_{in} = 4I_b)$	Under the saturation condition
Triangular	$I_{in(peak)}$	$\frac{1}{\sqrt{3}} \cdot I_{in(peak)}$	$\frac{1}{\sqrt{24}} \cdot I_{in(peak)}$	$I_{in(peak)} \le 0.82 I_{in(peak)}$ $(I_{in} > 4I_b)$	Out of the saturation condition

*The circuit is somewhat limited by the saturation condition $I_{in} \le 4I_b$

Note:

- *Under the saturation condition* is defined as MOS transistors are biased in the saturation region.

- *Out of the saturation condition* is defined as MOS transistors can not biased in the saturation region.

From table 3.1 we found that the bias current (I_b) and the signal input current (I_{in}) of the sine wave and square wave are under the saturation condition, $I_{in} \le 4I_b$, except in the case of the input signal is triangular wave. From this results, we found that the accuracy of square wave input signal and sine wave input signal will be better than the triangular wave input signal.

3.3.2.2 Conversion Errors

From the block diagram in Fig. 3.1, the accuracy of the RMS-to-DC conversion depends on the imperfection of the squaring and the current mirrors circuits. From the eqns. (3.2)-(3.7), we can notice that the implicit computation is achieved by the feedback of the current I_{RMS} to the I_{in}^2 / I_b block by setting $I_b = I_{RMS}/\sqrt{8}$, where I_b is the transistor bias current. Then the accuracy

of the RMS-to-DC conversion depends on the imperfection of the squaring and the current mirrors circuits. In addition, due to the output current (I_{RMS}) should designed by $I_{RMS}=\sqrt{8}\,I_b$ by setting channel width of transistor M_{13} is $W_{13}=\sqrt{8}\,W_{11}$, however, in practice the value of $\sqrt{8}$ can not exactly setting, therefore we approximately given $W_{13}=2.83W_{11}$. From this result the output current will have some error from the approximation of $\sqrt{8}\cong 2.83$ about 0.056%.

The operating range of the squaring part can be studied through a the large signal analysis, by considering the MOS transistors operating in saturation. Since the output current of the squaring circuit (I_{SA}) is the sum of the drain current of transistors M_1 and M_3 , $I_{D1}+I_{D3}$, where I_{D3} is mirrored from the current mirror CM_1, and if the gain of the current mirror CM_1 is unity, I_{D3} can be expressed in the function of I_{D2} as

$$I_{D3}=\frac{(W/L)_3}{(W/L)_2}\left(\frac{V_{GS3}-V_{T3}}{V_{GS2}-V_{T2}}\right)^2\cdot\frac{1+\lambda V_{DS3}}{1+\lambda V_{DS2}}\cdot\frac{\mu_{n3}C_{ox3}}{\mu_{n2}C_{ox2}}I_{D2} \quad (3.19)$$

From this equation, we found that the mismatched of the channel width W, channel length L, mobility μ_n, and oxide thickness t_{ox} of the current mirror can produce the gain error. Also, the effect from channel length modulation and mismatched of the threshold voltage. This gain error of the current mirror will effect to the accuracy of the output current of the squaring circuit. This error can be reduced by using large values of transistor length L_3, but especially by enforcing equal V_{DS} value of transistors M_2 and M_3.

If the effect of channel-length modulation can be neglected ($\lambda=0$), assume the process parameters such as V_T, μ_n, C_{ox}, of MOS transistor are matched and $V_{DS2}\cong V_{DS1}$. By copying of I_{D2} via transistor M_3 and adding it to current I_{D1} , the sum current $I_{D1}+I_{D3}$ is available as output current I_{SA} of squaring part [Appendix A]

$$I_{SA}=\frac{1}{2}\frac{\mu_nC_{ox}W}{2L}(V_1-2V_T)^2+\frac{I_{in}^2}{2\frac{\mu_nC_{ox}W}{2L}(V_1-2V_T)^2} \quad (3.20)$$

In order to remain a proper operation from Appendix A.11, the input current is restrict to the range $|I_{in}|<K(V_1-2V_T)^2$.

The eqn (3.20) describes a current squaring function. Using the bias circuit, formed by transistors M_4 and M_6 , to combination with the current squaring circuit in Fig. A1 which shown in Fig. 2.8, a simpler expression is obtained

$$I_{SA} = 2I_b + \frac{I_{in}^2}{8I_b} \tag{3.21}$$

Biasing with a current has the additional advantage of making the transfer function (in first-order approximation) independent of process parameters and operating temperature.

The conversion of the input signal current i_{in} to the current i_{SA} from the squaring part can be approximately expressed as [Appendix B]

$$\alpha = \frac{i_{SA}}{i_{in}} = \frac{1}{1 + \dfrac{g_{d1}(g_{m2} + g_{m3})}{g_{m1}g_{m3} + g_{m2}g_{m3} - g_{m1}^2 - g_{m1}g_{m2} - g_{m1}g_{d1} - g_{m2}g_{d1}}} \tag{3.22}$$

where g_{di} and g_{mi} denote the drain conductance and the conductance of the transistor M_i, respectively. The input current I_{in} will accurately convert to i_{SA} if $\alpha \approx 1$. The percentage conversion error of the squaring circuit can be written as

$$\frac{\delta\alpha}{\alpha} = \frac{g_{d1}(g_{m2} + g_{m3})}{g_{m1}g_{m3} + g_{m2}g_{m3} - g_{m1}^2 - g_{m1}g_{m2} - g_{m1}g_{d1} - g_{m2}g_{d1}} \times 100\% \tag{3.23}$$

For example, if $g_{m1} = 4.80 \times 10^{-4}$ AV^{-1}, $g_{m2} = 4.44 \times 10^{-4}$ AV^{-1}, $g_{m3} = 5.39 \times 10^{-4}$ AV^{-1} and $g_{d1} = 3.26 \times 10^{-6}$ AV^{-1}, the resulting conversion error is equal to 0.322%. It should be noted from eqn. (3.23) that the conversion error depends on drain conductance (g_d) of the transistors, where $g_d \approx \lambda I_D$ and λ is the channel length modulation parameter. We can further reduce this error by decreasing the transistor drain current I_D. In addition, if long channel transistors are used, we can neglect channel length modulation effect [59]

The current reflection errors ε_{pos} and ε_{neg} associated with the positive and negative current mirrors, respectively, can be approximately given by [60]

$$\varepsilon_{pos} = \left(\frac{I_{out}}{I_{in}}\right)_{CMpos} - 1 = \left(\frac{L_7 W_8}{W_7 L_8}\right)_{NMOS} \cdot \left(\frac{1+\lambda V_{DS8}}{1+\lambda V_{DS7}}\right)_{NMOS} - 1 \quad (3.24a)$$

$$\varepsilon_{neg} = \left(\frac{I_{out}}{I_{in}}\right)_{CMneg} - 1 = \left(\frac{L_9 W_{10}}{W_9 L_{10}}\right)_{PMOS} \cdot \left(\frac{1+\lambda V_{DS10}}{1+\lambda V_{DS9}}\right)_{PMOS} - 1 \quad (3.24b)$$

where V_{DS} is drain-source voltage. For example, let $W_7 = W_8 = W_9 = W_{10} = 100\,\mu$m, $L_7 = L_8 = L_9 = L_{10} = 5\,\mu$m, $\lambda = 0.01$ volts^{-1}, $V_{DS7} = 2.72$ volts, $V_{DS8} = 4.94$ volts, $V_{DS9} = -2.76$ volts, and $V_{DS10} = -4.99$ volts, these errors (ε_{pos} and ε_{neg}) is approximately less than 2.17 %. Notice from the eqns. (3.24a) and (3.24b) that the accuracy of the current mirror also depends on the channel length modulation. In order to reduce the influence of the channel length modulation, cascode current mirrors should be used.

3.3.2.3 Frequency response

The frequency response of an RMS-to-DC converter provides a measure of how well the circuit can measure the RMS of sine wave input signals of varying frequencies. This frequency response is different from that used when describing filters or amplifiers which are essentially linear devices. The RMS-to-DC converter is a non-linear device with an AC input and a DC output and so has a frequency response which is defined as the percent error on the output against the frequency of the input sine wave. This frequency range is much greater than $1/\tau$ where τ is the time constant of the smoothing circuit being used. As the frequency of the input signal is reduced, the smoothing filter is not able to average effectively and a greater ripple content appears on the output together with a DC output error.

So, for low input frequencies, about 10Hz, a compromise needs to be made between having a large time constant for smoothing which provides a slow response time with good accuracy or having a small time constant which provides a faster response time but poorer accuracy. The high frequency response is limited by the finite bandwidth of the circuit structure, which for this proposed true RMS-to-DC converter circuit, it is limited by the current mirror, CM_5. Many commercial ICs that employ by using op amp to construct the full wave rectifier, therefore, the high frequency response is dependent on the finite bandwidth and slew rate of the input full wave rectifier of the circuit.

To verify the high frequency response, from the block diagram of Fig. 3.2, the transfer function of the proposed RMS-to-DC converter circuit can be approximately given by

$$\frac{I_{RMS}(s)}{I_{in}(s)} = \frac{I_{SA}(s)}{I_{in}(s)} \cdot \frac{I_{SQ}(s)}{I_{SA}(s)} \cdot \frac{I_{b1}(s)}{I_{SQ}(s)} \cdot \frac{I_{RMS}(s)}{I_{b1}(s)} \tag{3.25}$$

By a small signal analysis of the Fig.3.2, the transfer function of the circuit can be approximated as [Appendix C]

$$\frac{I_{RMS}(s)}{I_{in}(s)} = \frac{(g_{m3}-g_{m1})/(g_{m1}+g_{m2})}{\left(1+s\frac{C_1+C_2+C_3}{g_{m1}+g_{m2}}\right)} \cdot \frac{g_{m10}/g_{m9}}{\left(1+s\frac{C_9+C_{10}}{g_{m9}}\right)} \cdot \frac{g_{m8}/g_{m7}}{\left(1+s\frac{C_7+C_8}{g_{m7}}\right)} \cdot \frac{g_{m13}/g_{m11}}{\left(1+s\frac{C_{11}+C_{12}+C_{13}}{g_{m11}}\right)} \tag{3.26}$$

Let p_1 denotes the pole of the squaring circuit, p_2 is the pole of the current mirror CM4, p_3 is the pole of the lowpass filter, and p_4 is the pole of the current mirror CM5. Then from eqn. (3.26), the poles p_1, p_2, p_3 and p_4 can be respectively expressed as

$$p_1 = -\frac{g_{m1}+g_{m2}}{C_1+C_2+C_3} \tag{3.27}$$

$$p_2 = -\frac{g_{m9}}{C_9+C_{10}} \tag{3.28}$$

$$p_3 = -\frac{g_{m7}}{C_7+C_8} \tag{3.29}$$

$$p_4 = -\frac{g_{m11}}{C_{11}+C_{12}+C_{13}} \tag{3.30}$$

If I_{in} = 1mA, g_{m1} = 4.80×10^{-4} AV^{-1}, g_{m2} = 4.44×10^{-4} AV^{-1}, g_{m9} = 3.31×10^{-4} AV^{-1}, g_{m7} = 4.27×10^{-4} AV^{-1}, g_{m11} = 3.31×10^{-4} AV^{-1}, $C_1=C_2=C_3=C_7=C_8=1.21\times10^{-13}$F, $C_9=C_{10}=C_{11}=C_{12}=1.15\times10^{-13}$F, and $C_{13}=3.26\times10^{-13}$F, where $C_i = Cgs_i$ and Cgs_i is the gate-to-source capacitance of transistor M_i. Then the cut-off frequencies of the poles p_1, p_2, p_3 and p_4 are approximately located at 405MHz, 229MHz, 281MHz and 95MHz, respectively. We can see that the high frequency limitation is due

to the pole p_4 that associated with the PMOS current mirror (CM5). Then the cut-off frequency of the RMS-to-DC converter can be given by

$$f_{-3dB} = \frac{(g_{m11})}{2\pi(C_{11}+C_{12}+C_{13})} \tag{3.31}$$

It should be noted that g_{m1}, g_{m2}, g_{m7}, g_{m9} and g_{m11} are varied in direct proportion to the input current I_{in}, since $g_m = \sqrt{2K_p(W/L)I_D}$ and $I_D = I_{RMS}/\sqrt{8} \cong 0.707 I_{in(peak)}$. Therefore, the cut-off frequency of the RMS-to-DC converter can be increased if I_{in} increase, and vice versa. For example, using the same data above, for I_{in}= $1mA_{(peak)}$ the cut-off frequency of the RMS-to-DC converter circuit is about 95MHz and for I_{in}=$500\mu A_{(peak)}$ the cut-off frequency of the RMS-to-DC converter circuit is about 66MHz.

3.3.2.4 DC and ripple errors

In practice, apart from the current I_{RMS}, there are also a low-frequency ripple and a dc error that presented at the output port of the circuit, which depend on the value of the capacitor C_{AV} and the frequency of the input current I_{in}. These errors can be computed by expressing the relationship of the currents I_{RMS} and I_{in} in the form of transfer function, where the current I_{in} is an input sine wave of the form $I_{in} = \sqrt{2} I_{RMS} \cos(\omega t)$. Using a simple trigonometric and Taylor series approximation and by assuming that the frequency of input current is greater than the inverse of the averaging time constant τ (or $f > 1/\tau$), the output ripple e_{ripple} and the dc error e_{odc} can be expressed in term I_{RMS} of as [65] , [66] ,[Appendix D]

$$e_{ripple} = \frac{I_{RMS}\cos 2\omega t}{2\sqrt{1+4\omega^2\tau^2}} \tag{3.32}$$

and

$$e_{odc} = \frac{I_{RMS}}{16(1+4\omega^2\tau^2)} \tag{3.33}$$

where only the ripple that due to the second-harmonic term is expressed. The ripple error in the output can be reduced in many applications with a simple low-pass filter. Eqns. (3.32) and (3.33)

showing that the ripple error e_{ripple} and dc error e_{odc} decrease with increasing AC input frequency.

Clearly, the ripple and DC error can be reduced by increasing the time constant of the LPF, however this will slow down the response of the circuit.

3.4 Simulation and Experimental results

The performance of the proposed true RMS-to-DC converter has been studied through simulation and experimental results. The simulation has been carried out by employing PSPICE analogue simulation program, using the CMOS CD4007 transistor parameters that were extracted by the use of the method in [61], [62]. The transistor dimensions are listed in the Table 3.2.

Table 3.2 The aspect ratios of the transistors in Fig.3.2.

Transistor	W(μm)	L(μm)
M1,M2,M3,M4,M6,M7,M8	100	5
M9,M10,M11,M12	100	5
M5	200	5
M13	283	5

For the input current (I_{in}) equal to zero, all MOS transistors are cut-off and I_{out} is also zero. This statement can be confirmed through simulation result, where in the case of V_{dd}= 5V the circuit has the supply current (I_{supply}) of about 100pA, which is near to zero. Fig. 3.3 shows the operation of the true RMS-to-DC converter of Fig.3.2 for sine wave input with $I_{in(peak)}$=100μA and f=1kHz. Where the current $I_{D(M9)}$ is the output current from the squaring circuit, $I_{D(M11)}$ is the output current from the integrator (LPF) and $I_{D(M13)}$ is the I_{RMS}. When an input signal is applied from time 0s to 5ms, the circuit is conducted only in the half cycle, where we can see that the $I_{D(M9)}$ is the form of rectified waveform. After that due to the feedback loop and the averaging circuit (or LPF), time 5ms to 10ms, gradually developed and supply to be the bias current I_{b1} (or $I_{D(M11)}$) of the circuit. For the steady state the squaring circuit can properly operate as a squarer

function. Therefore the circuit can function as Root-Mean-Square. Since the dc bias current of the true RMS-to-DC converter is zero and conducts only when the input signal is present, this circuit is operated as a Class B circuit.

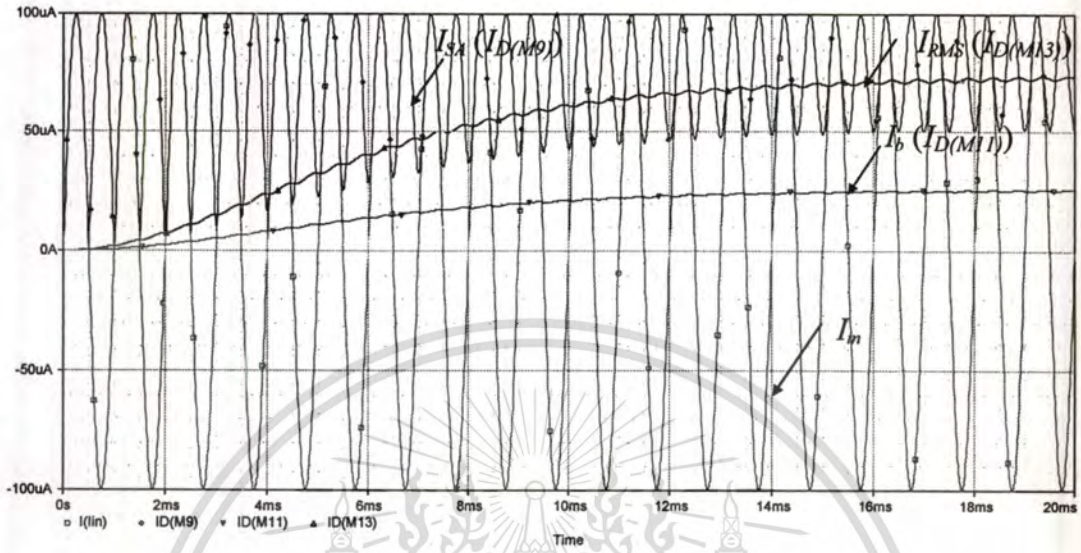


Fig. 3.3 The operation of the proposed true RMS-to-DC converter

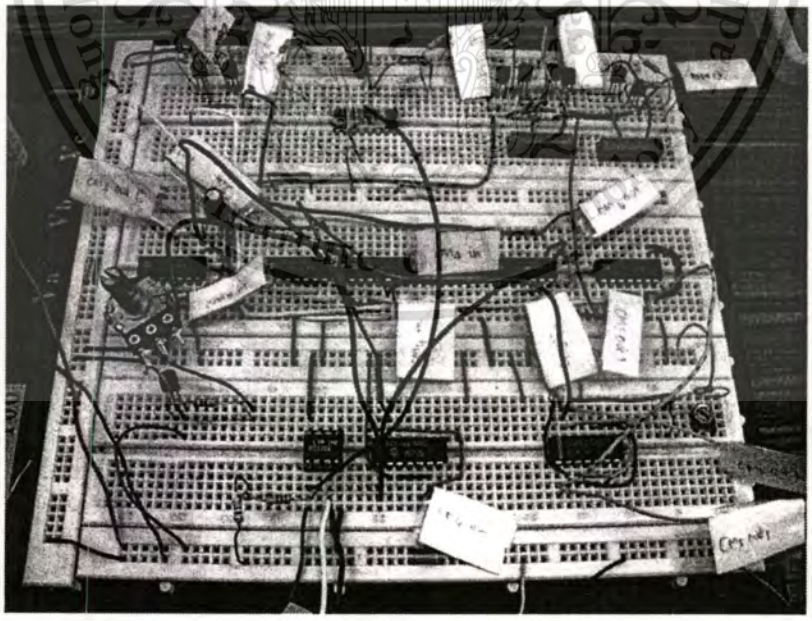


Fig. 3.4 The experiment of the RMS-to-DC converter on a prototype board

In order to test the performance of the circuit, the true rms-to-dc converter of the Fig.3.2 was also constructed on prototype board as shown in Fig. 3.4. All MOS device used was in the form of complementary MOS pair (CD4007). The transistors that required close matching, especially M_1, M_2 and M_3 and the current mirrors were contained in the same array package. The supply voltage was set to V_{dd} =15V. The capacitor C_{AV} is 10 μF for f_{MIN} = 100Hz. Due to the proposed RMS-to-DC converter operates in current mode, a commercially available current conveyor CCII01 [63] was used to convert the input voltage V_{in} into the input current signal I_{in}. The resistor R_{in}=1kΩ is connected at ports X and the input voltage was applied to the port Y of the CCII. For example, by setting the input signal current of I_{in} = $1mA_{(peak)}$, the input voltage equal to 1V is applied to port Y of the CCII. To measure the value of the I_{RMS}, a resistor of 1kΩ was connected at the output of the RMS-to-DC converter and the voltage across the resistor R_o is measured instead.

The experimental results in Fig. 3.5(a), 3.5(b) and 3.5(c) show the I_{RMS} for the input signals in the form of sinusoidal, triangular and square wave waveforms, respectively, with the peak amplitude of 1mA and with the frequency of 1 kHz. With the error of less than 10μA, the I_{RMS} signal with the amplitudes close to 0.7mA, 0.5mA, and 1mA, respectively, were achieved. These results demonstrated that the circuit can convert the AC signals into the corresponding DC signals with accurate rms values. To demonstrate that the circuit can operate in a wide frequency range, Fig.3.6(a), 3.6(b) and 3.6(c) show the measured I_{RMS} for the cases of the sinusoidal input signal with the frequencies of f = 500Hz, 5kHz and 5MHz, respectively, and with the peak amplitude of 1mA. The results show that the I_{RMS} signals with the amplitude of about 0.7mA are achieved. The dc errors from the simulation results are about 11%, 0.2% and 0.1%, respectively. We found that this results were agree with the dc error predicted from eqn.(3.33), where the dc error decrease with increasing AC input frequency ($\omega >> 1/\tau$).

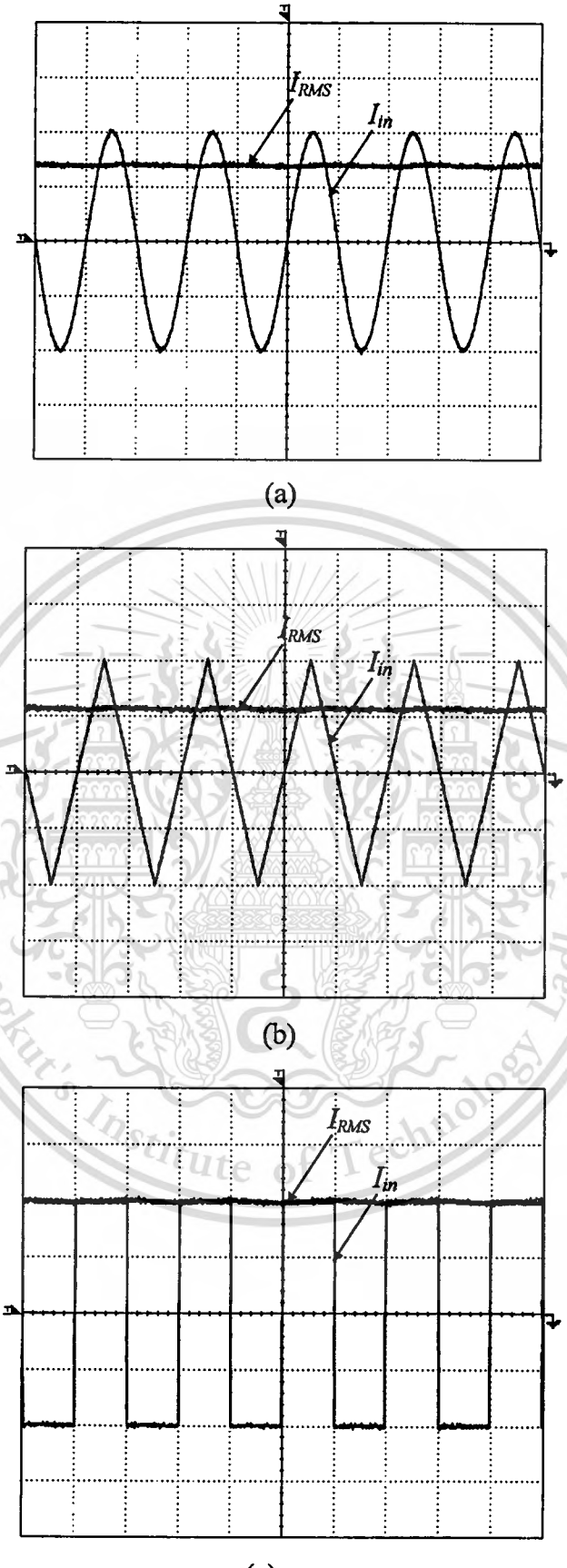
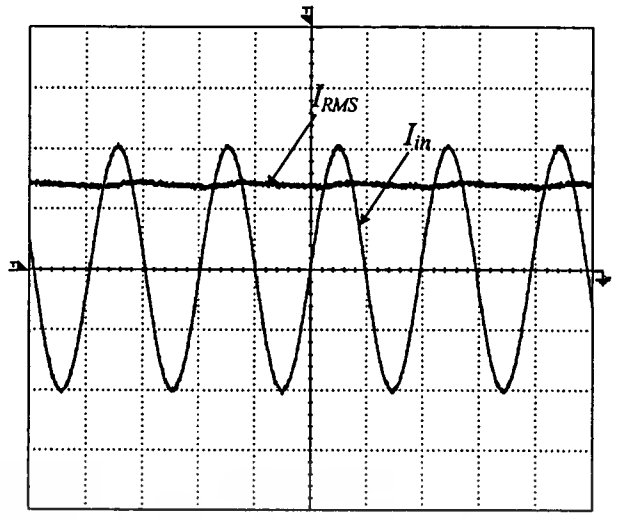
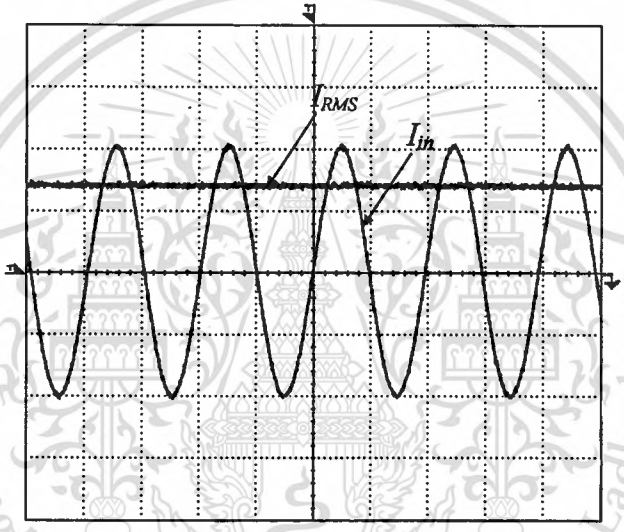


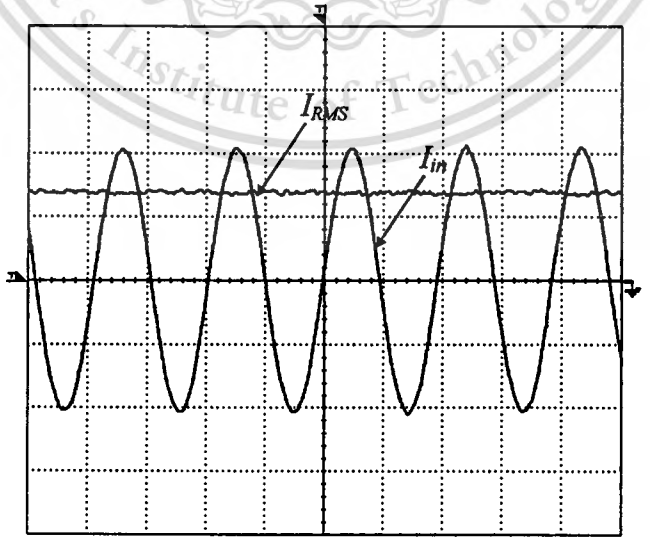
Fig. 3.5 Experimental results for the input signals: (a) sinusoidal; (b) triangular; and (c) square wave. (Vertical scale: 0.5V/div. Horizontal scale: 0.5ms/div)



(a)



(b)



(c)

Fig. 3.6 Experimental results of I_{RMS} with I_{in}=1mA for:

(a) f = 500Hz ; (Vertical scale: 0.5V/div. Horizontal scale: 1ms/div)

(b) f = 5kHz ; (Vertical scale: 0.5V/div. Horizontal scale: 100μs/div) and

(c) f = 5MHz ; (Vertical scale: 0.5V/div. Horizontal scale: 100ns/div).

From the Fig.3.6(a), 3.6(b) and 3.6(c), we can notice that the output ripple for the input signal at low frequencies, i.e. f = 500Hz, is higher than the case of the input signals with higher frequency. This is due to that, in this case, the capacitor C_{AV} is selected for f_{MIN} = 100Hz. We will further study this effect through the simulation result owing to that the ripple cannot accurately be measured from the experimental results. Usually, the % ripple is calculated by

$$\% \text{ ripple} = (I_{ripple(p\text{-}p)}/I_{DC}) \times 100\% \tag{3.34}$$

where $I_{ripple(p\text{-}p)}$ is the peak to peak amplitude of the output current and I_{DC} is the DC component of the output current. From the simulation results at f = 500 Hz, 5 kHz and 5 MHz, the output signals have percent ripple errors of about 1.1% , 0.13% and 0.0001%, respectively. On the other hand, according to eqn.(3.8), since the averaging capacitor is selected 20 times grater than the predicted value (C_{AV}=10μF) and for I_M = 1mA, the calculated output percent ripple is about 1% at f = 500Hz. It agree with the simulation results above. Fig. 3.7 shows the simulated results of the I_{RMS} for 3 difference values of the capacitor C_{AV}, i.e. 1μF, 5μF and 10μF, when the input is a sinusoidal waveform with the peak amplitude of 1 mA and the frequency f = 1 kHz. The results show that the circuit will provide the I_{RMS} with lower ripple if a larger capacitor is used. But, however, it will result in a longer settling time.

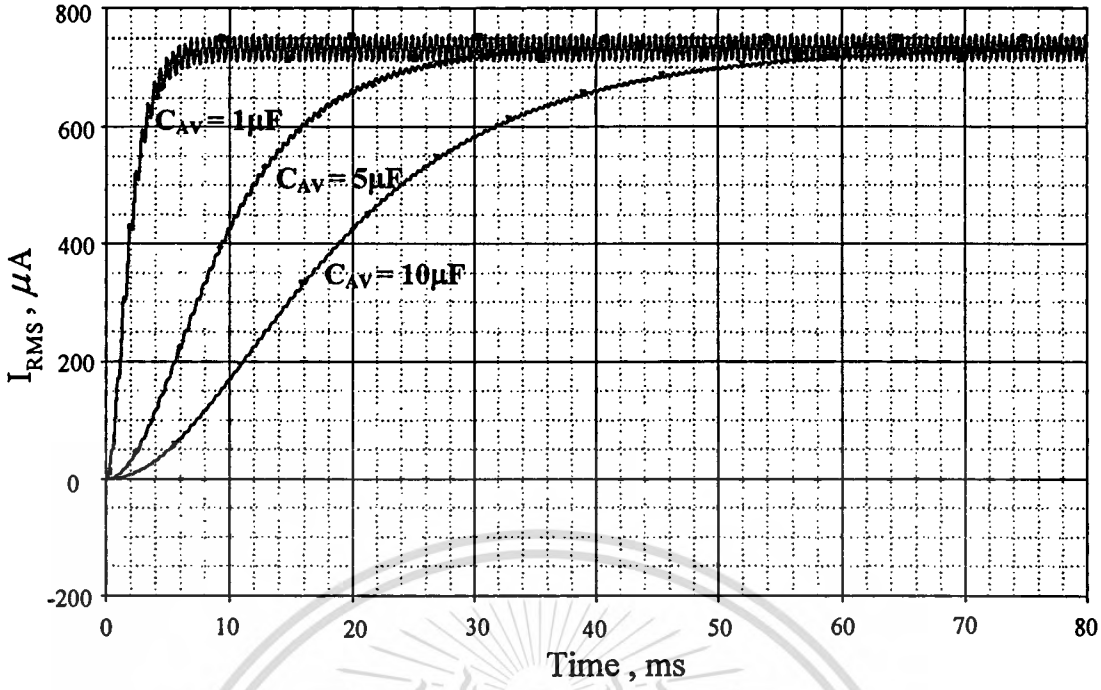


Fig. 3.7 The I_{RMS} that simulated for 3 different values of the capacitor C_{AV}.

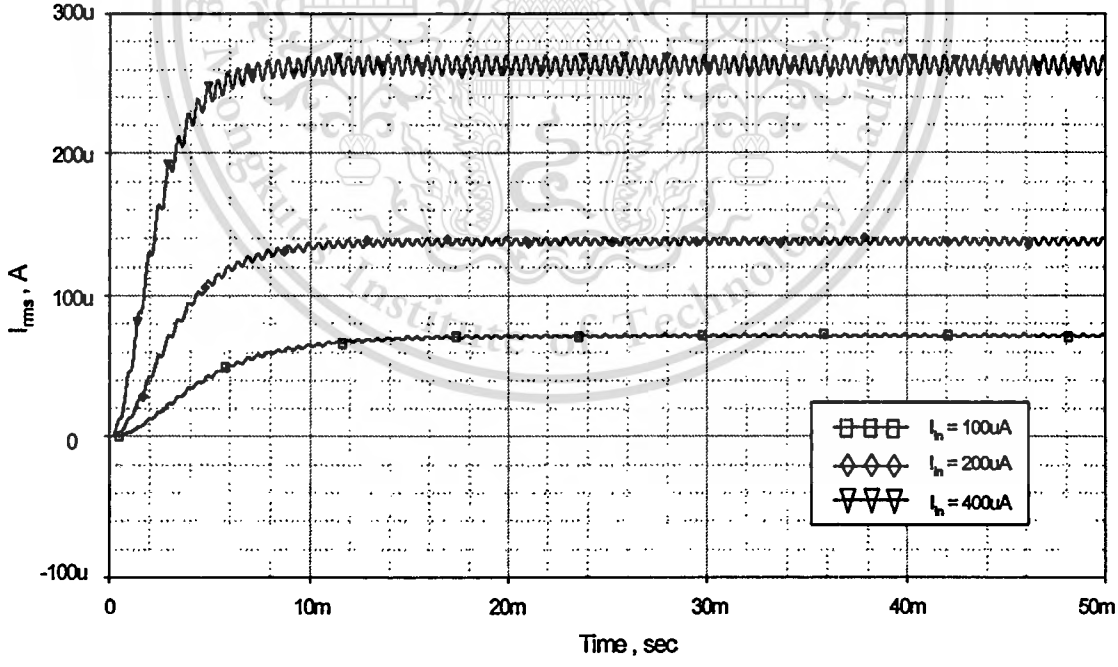


Fig. 3.8 Settling time versus input current (I_{in}).

Fig. 3.8 show the simulated results of the proposed RMS-to-DC converter settling time versus the signal input current I_{in} . The results were simulated for the case of I_{in}=400μA, 200μA and 100μA

where the capacitor C_{AV} = 0.5μF and the frequency f = 1 kHz, respectively. The settling time is about 6.22ms, 7.76ms and 11ms, respectively with less than 5% of reading error. This simulation results demonstrated that, the settling time is depending by the averaging time constant ($\tau = C_{AV}/g_{m7}$). The settling time varies with input signal levels, increasing as the input signal is reduced, and decreasing as the input is increased.

The experimental results that demonstrate the linearity of the RMS-to-DC converter are shown in Fig.3.9. The transfer characteristics are the plots of the I_{RMS} against the input signal current I_{in} with the peak amplitude varied from 300μA to 1.5mA, for the sine, triangular and square waveforms. The signal frequencies are 1kHz and C_{AV}=10μF. We found that the maximum conversion nonlinearity of about 2% was achieved. It should be noted that the lower limit of the circuit is due to the fact that the I_{RMS} is feedback to be the bias current I_b of the circuit. Therefore, through I_b, the I_{RMS} should be large enough to bias all the transistors in their saturation regions.

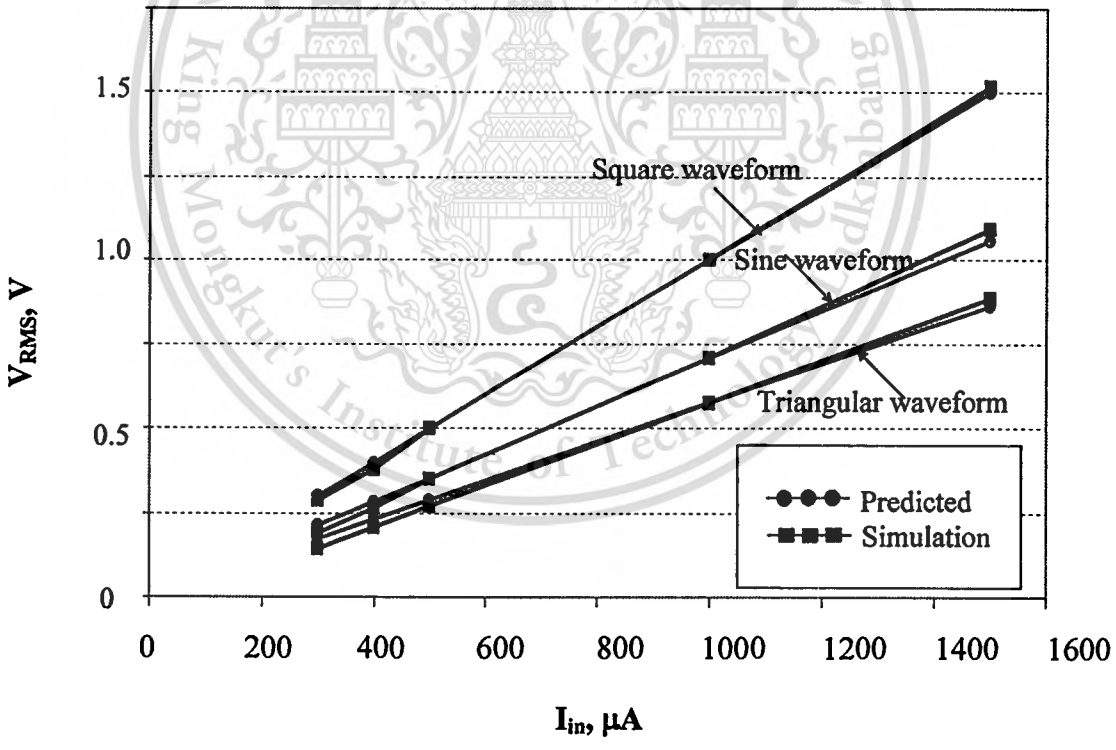


Fig. 3.9 DC transfer characteristic curves of the rms-to-dc converter circuit.

The relation of I_{RMS} between I_b and I_{in} can be shows from these results. For example, the input signals is sinusoidal, triangular and square waveforms, respectively, for $I_{in(peak)}$ = 1mA, f = 1 kHz. In the case of input waveform is sinusoidal with amplitude

Sinusoidal : I_b = 0.25mA , I_{RMS} = 0.714 mA Error = 0.01% of reading

Triangular : I_b = 0.2mA , I_{RMS} = 0.612 mA Error = 0.06% of reading

Square : I_b = 0.35mA , I_{RMS} = 1.05 mA Error = 0.05% of reading.

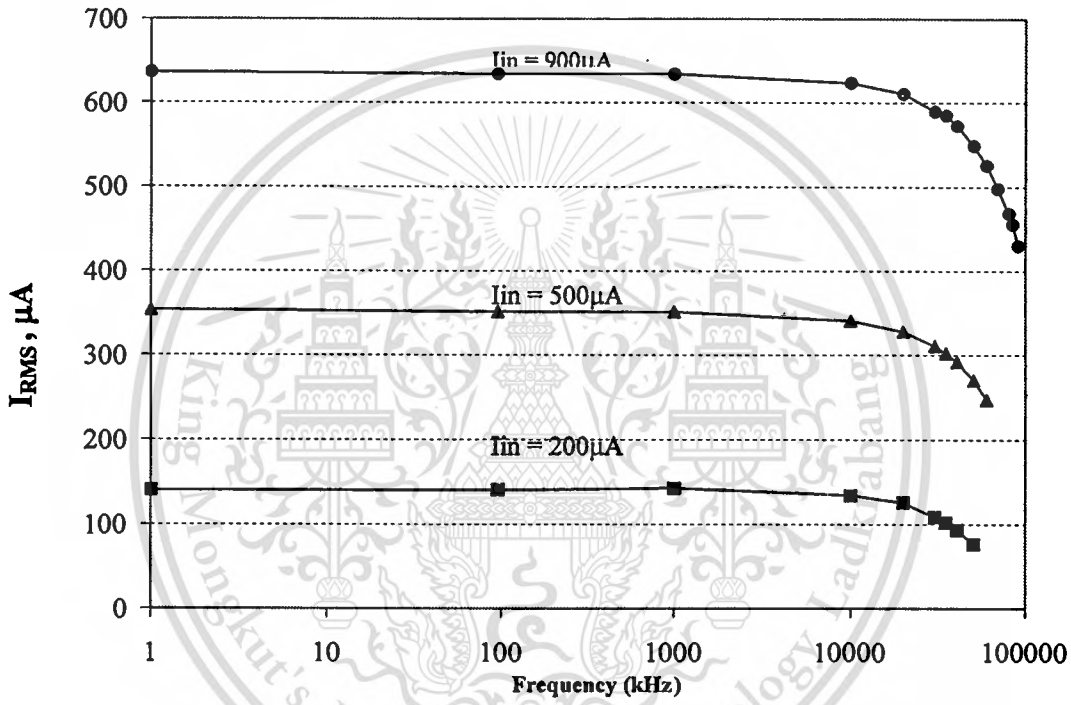


Fig. 3.10 High-frequency responses due to the variation of I_{in}.

Due to the stray capacitances in the bread boarding circuit, the high frequency response capability was not measured directly. The high frequency performance was studied through PSPICE simulation. Fig. 3.10 shows the frequency response for difference values of the input current (I_{in}). The input signals are sine waves with the amplitude of 20%, 50% and 90% of the full-scale current (I_{in} = 1mA$_{(peak)}$). The results show the bandwidth of about 35 MHz, 60 MHz and 85MHz, respectively. The results are agreed with the predicted value from the eqn. (3.31), where the bandwidth drops off as the input current signal is reduced. The simulation results for the –3dB

bandwidth with the peak input current ranging from I_{in} = 100μA to 1000μA were summarized in the Table 3.3. The simulated power dissipation for I_{in} = 1mA is about 6.04nW, which is very low.

Table 3.3 Performance of the RMS-to-DC converter design based on CMOS complementary CD4007.

Parameters	Simulated results
Supply voltage (rated)	5V to 15V
Input current range (MAX)	1.5mA
Power Dissipation	6.04nW (at I_{in}=0)
Gain error	2% Max. nonlinearity, 100 μA to 1.5mA input
Peak amplitude value	-3 dB bandwidth
I_{in} = 100 μA	25 MHz
I_{in} = 200 μA	40 MHz
I_{in} = 500 μA	60 MHz
I_{in} = 900 μA	85 MHz
I_{in} = 1000 μA	90 MHz
I_{in} = 1500 μA	100 MHz

Generally, crest factor is the ratio of the peak value relative to the RMS value. So far the characteristics of the circuit have been studied for the common waveforms as sine and triangle waveforms, which have relatively low crest factor ($\leq$2). The simulation results for the input signal with difference crest factors are shown in Fig 3.11. The rectangular pulse train with pulse width of 1ms was used for this test, since it is the worst-case waveform for RMS measurement. The duty cycle and peak amplitude were adjusted to produce a crest factors from 1 to 5, while maintaining a constant $1mA_{(peak)}$ input current [64]. We found that the proposed RMS-to-DC converter performs very well with crest factors of 3 or less. As shown in the Fig.3.11, for the case of crest factor equal to 3, the conversion error is less than 5%. However, for the higher crest factor, such as 4, the conversion error is more than 8%. This is due to that the waveforms with higher crest factor, the RMS value is decreased. Consequently, the bias current of the RMS-to-DC converter circuit is also reduced and will effect to

the accuracy of the circuit. To provide good accuracy at high crest factor, the input current should be increased. For example, with the crest factor = 4, the conversion error was reduced to 6% if we set the input current (I_{in}) equal to 2mA.

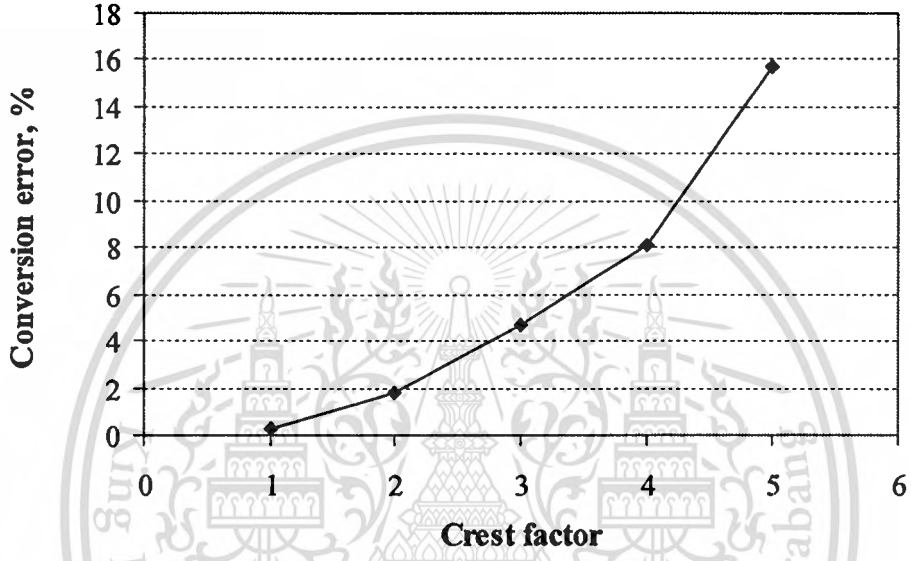
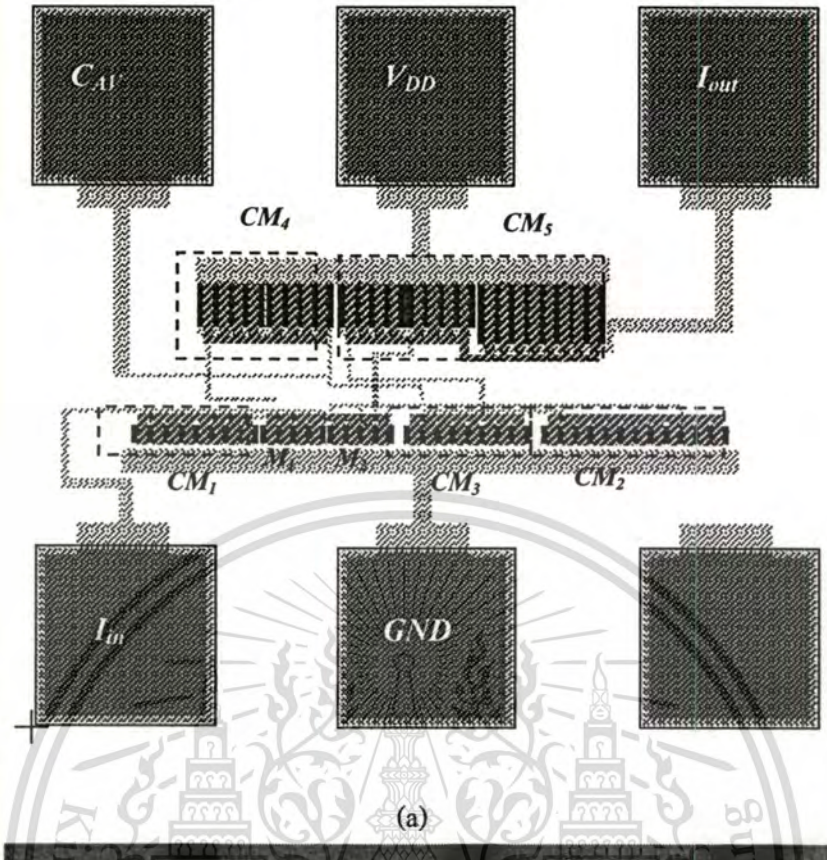


Fig. 3.11 Simulation results for the additional error versus crest factor.

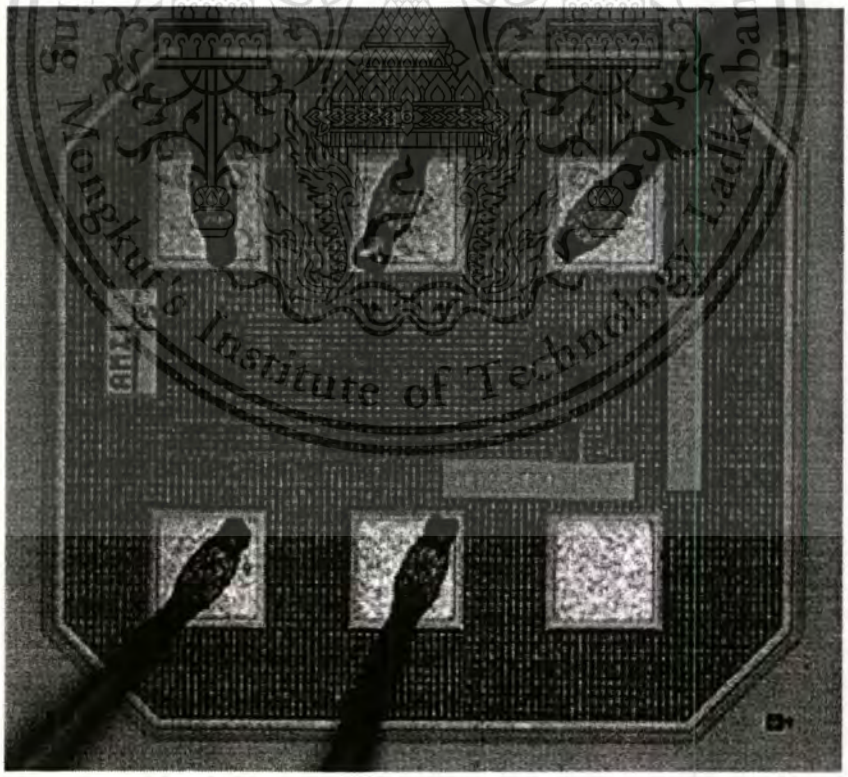
3.5 The implementation of the proposed RMS-to-DC converter and its experimentations.

The true RMS-to-DC converter that proposed in this thesis can be realize for real chip. The conversion circuit is simple, suitable for implementing in monolithic integrated form, and can be readily integrated as part of a larger system.

Fig. 3.12 shows the layout and microphotograph, fabricated in a 0.5 microns CMOS Technology AMIS process with $V_{th} \cong 0.7V$, of the proposed true RMS-to-DC converter. The total chip area occupied was 484x442 micron^2 excluding the bonding pads.



(a)



(b)

Fig. 3.12 The True RMS-to-DC Converter: (a) The layout and (b) Microphotograph.

The performance of the integrated true RMS-to-DC converter has been studied through simulation and experimental results. The simulation has been carried out by employing spectre in CADENCE simulation program and using the transistor parameters of the 0.5 microns CMOS Technology AMIS process. The transistor dimensions of the circuit in Fig. 3.2 are in micron, where the dimension of the transistors M_5 is W=80μm and L=5μm, M_{13} is W=283μm and L=5μm, M_1-M_4, M_6 are W=40μm and L=5μm and M_9-M_{12} are W=100μm and L=5μm. The power supply voltage were set to V_{DD}= 5V.

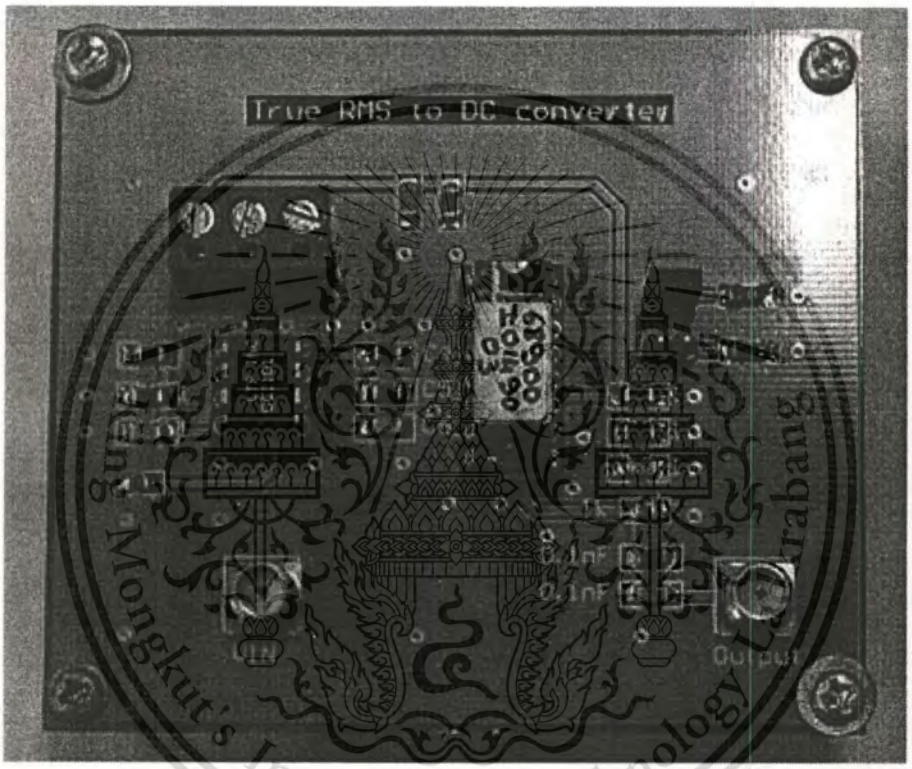
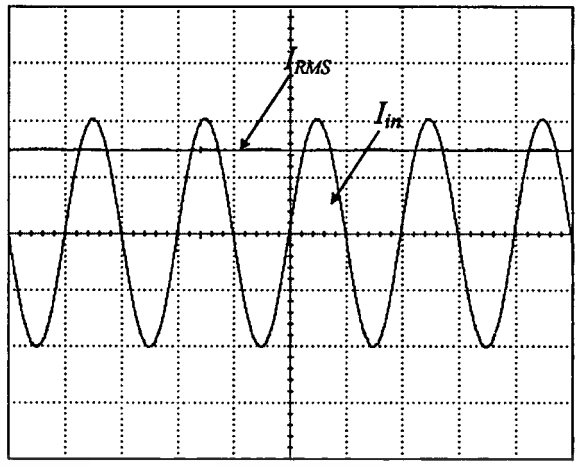
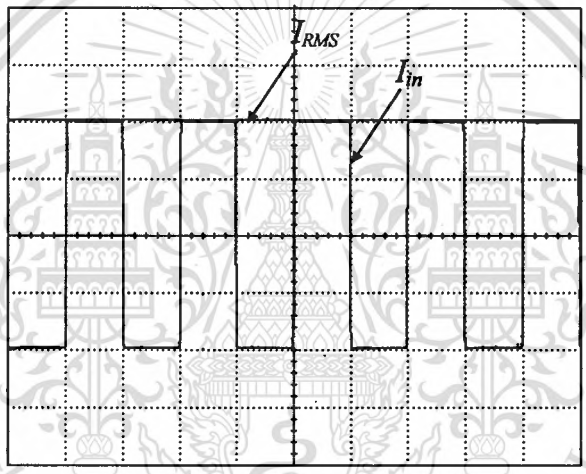


Fig. 3.13 True RMS-to-DC converter measurement setup

Employing the chip of the Fig.3.12, the measurement setup is shown in Fig. 3.13. The external capacitor C_{AV} is 10μF. Due to the proposed RMS-to-DC converter operates in current mode, a commercially available current conveyor CCII01 was used to convert the input voltage V_{in} into the input current signal I_{in}. The resistor R_{in}=1kΩ is connected at ports X and the input voltage was applied to the port Y of the CCII. For example, by setting the input signal current of I_{in} = $1mA_{(peak)}$, the input voltage equal to 1V is applied to port Y of the CCII. To measure the value of the I_{RMS}, a resistor of 1kΩ was connected at the output of the RMS-to-DC converter and the voltage across the resistor R_o is measured instead.



(a)



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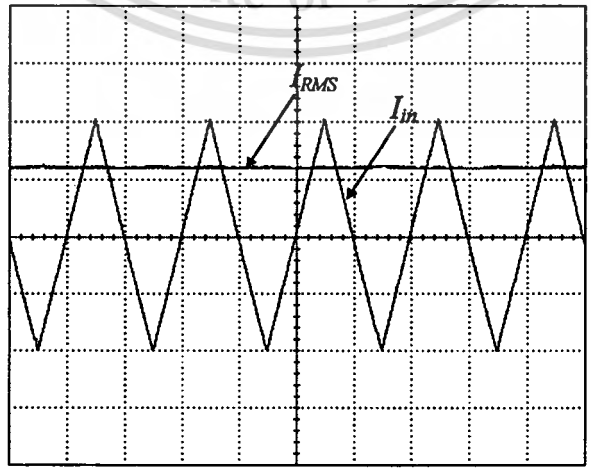

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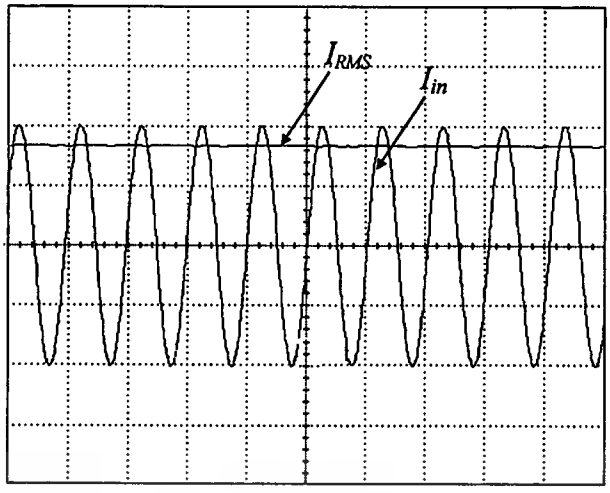

(d)

Fig. 3.14 Experimental results for the input signals: (a) sinusoidal; (b) triangular; (c) square wave; (Vertical scale: 0.5V/div. Horizontal scale: 5us/div) and (d) sinusoidal. (Vertical scale: 0.5V/div. Horizontal scale: 200ns/div)

The experimental results in Fig. 3.14(a), 3.14(b) and 3.14(c) show the I_{RMS} for the input signal of sinusoidal, triangular and square waveforms, respectively, with the peak amplitude of 1mA and with the frequency of 100 kHz. The I_{RMS} signal with the amplitude close to 0.7mA, 0.5mA, and 1mA, respectively, with the error of less than 10μA, were achieved. These results demonstrated that the circuit can be accurately converted the AC signals into the RMS values. To demonstrate that the circuit can operate in a wide frequency range, Fig. 3.14(d) shows the measured I_{RMS} for the cases of the sinusoidal input signal with the frequencies of f = 5MHz, and with the peak amplitude of 1mA. The results show that the I_{RMS} signals with the amplitude of about 0.7mA are achieved. The dc error from the simulation results is about 12%. From the simulation results at f = 100 Hz, 100kHz and 5 MHz, the output signal have percent ripple error of about 3% , 1.35% and 0.0001%, respectively.

The high frequency performance was studied through cadence simulation. The simulation results for the –3dB bandwidth with the peak input current ranging from I_{in} = 100μA to 1.5mA were summarized in the Table 3.4.

Table 3.4 Performance of the RMS-to-DC converter design based on 0.5μm CMOS AMIS technology .

Parameters	Simulated Results
Supply voltage (rated)	1.5V-5V
Input current range $_{(MAX)}$	1.5mA
Power Dissipated	0.1mW
Gain error	2% Max. nonlinearity, 100μA to 1.5mA input
Peak amplitude value	-3 dB bandwidth
I_{in} = 100 μA	20 MHz
I_{in} = 200 μA	40 MHz
I_{in} = 500 μA	60 MHz
I_{in} = 900 μA	85 MHz
I_{in} = 1000 μA	90 MHz
I_{in} = 1500 μA	100 MHz

Table 3.5 Summary of RMS-to-DC converter characteristics

Characteristics	**CMOS complementary CD4007**	**0.5μm CMOS AMIS Technology**
Supply voltage	Min : 5V Max : 15V	Min : 1.5V Max : 5V
I_{in}	Min : 100μA Max : 1.5mA	Min : 100μA Max : 1.5mA
Conversion accuracy		
Total error	100μA-1mA Max. ± 3% of reading	100μA-1mA Max. ± 3% of reading
Nonlinearity	2% at 1mA 1MHz	2% at 1mA 1MHz
Error VS Crest factor		
CF = 3	4.7%	4%
CF = 5	16.7%	13%
Input Characteristics		
Signal range	5V supply 1 mA I_{RMS}	5V supply 1 mA I_{RMS}
Peak transient	1 mA_{P-P}	1 mA_{P-P}

Characteristics	CMOS complementary CD4007	0.5µm CMOS AMIS Technology
Input offset current	1.5 pA	8 pA
Frequency Response		
BW for 5% additional error		
	Frequency (Hz)	Frequency (Hz)
I_{in} = 100µA	25MHz	20MHz
I_{in} = 200µA	40MHz	40MHz
I_{in} = 500µA	60MHz	60MHz
I_{in} = 900µA	85MHz	85MHz
I_{in} = 1mA	90MHz	90MHz
I_{in} = 1.5mA	100MHz	100MHz
Out put characteristics		
Offset current	10pA	50pA

Table 3.5 shows the summary characteristics of the proposed true rms to dc converter of CMOS complementary CD4007 and 0.5µm CMOS AMIS technology. There are the conversion accuracy, the error VS crest factor, the input characteristics, the frequency response and the output characteristics. This results quite agree with the prediction.

The performance of some commercial RMS-to-DC converter circuits and the proposed RMS-to-DC converter in this thesis are listed in Table 3.6.

Table 3.6 The performance of commercial RMS-to-DC converters and the proposed RMS to DC converter.

	AD536AJ	**AD637J**	**AD736J**	**AD735**	**SMM-21110**	***Proposed RMS***
Voltages						
Supplies (rated)	±15 V	±15 V	±5 V	±5 V	±15 V	1.5V to5 V
Input range(max)	$7V_{RMS}$	$7V_{RMS}$	$1V_{RMS}$	$1V_{RMS}$	$3mA_{pk-pk}$	100μA-1.5mA
Accuracy						
Gain error	0.5%	0.5%	0.5%	0.5%	±0.5 dB	2%
Offset error	5mV	1mV	0.5mV	0.4mV	5nA	10pA-0.1nA
Crest factor error	CF=3 0.1% CF=7 1.0%	CF=3 0.1% CF=10 1.0%	CF=3 0.7% CF=5 2.5%	CF=3 0.7% CF=5 2.5%	CF=5 0.5dB CF=8 1.0dB	CF=3 4% CF=5 13%
Dynamic						
3 dB bandwidth						
V_{in} = 10mV	90 kHz	80 kHz	55 kHz	5.5 kHz	50 kHz (I_{in}=1μA)	25 MHz (I_{in}=100μA)
V_{in} = 10mV	450 kHz	600 kHz	170 kHz	170 kHz	300 kHz (I_{in}=10μA)	60 MHz (I_{in}=500μA)
V_{in} = 1V	2.3 MHz	5 MHz			1.5 MHz (I_{in}=1mA)	90 MHz (I_{in}=1mA)
Comments*						
	(1)	(2)	(3)	(4)	(5)	(6)

Comments * :

(1) Monolithic device. Gain and offset errors easily trimmed. The AD636 is a very similar device, but designed for signals below 200mV.

(2) Wider bandwidth RMS-to-DC converter.

(3) Low power monolithic RMS-to-DC converter. Similar device is the AD737.

(4) Low power monolithic RMS-to-DC converter. Without output buffer. Contains power down circuitry. Similar device AD736.

(5) Current input to current output device. Requires several external resistors for voltage operation.

(6) Current input to current output device. Wide bandwidth and low power true RMS-to-DC converter.

This table shows that the proposed RMS-to-DC converter has some advantages over other methods. The circuit operates for single supply at low voltage, wide input swing, wide bandwidth.

Table 3.7 The performance of the other RMS-to-DC converters and the proposed RMS to DC converter

RMS-to-DC	[6]	[7]	[56]	propose RMS
Technology	Bipolar	Bipolar	MOS model 5	0.5μm AMIS
V_{supply}	2V-4V	± 15V	± 1.5V	1.5V-5V
Input Signal	V_{in}= 4V (max)	V_{in}=13.4V(max), I_{in}= 10μA-1mA	I_{in}= 40μA(max)	I_{in}=100μA-1.5mA
Bandwidth	5MHz	150MHz	>100kHz	90MHz
Accuracy	NA	0.2% at 1mA	1% at 40μA	2% at 1mA
Crest factor error	CF=10 1%	CF=3 0.25% CF=10 3%	NA	CF =3 4% CF=5 13%
Input waveform	All waveform	All waveform	sinusoidal	All waveform
RMS-to-DC	True RMS-to-DC	True RMS-to-DC	Pseudo RMS	True RMS-to-DC

This table shows that the proposed RMS-to-DC converter has some advantages over other methods. The circuit operates for single supply at low voltage, wide dynamic range and wide bandwidth.

3.6 Discussion and Conclusion

In this chapter, a simple CMOS true RMS-to-DC converter circuit has been developed that based on the use of the characteristic of a CMOS squaring circuit, where all the transistors are biased in the saturation region. The realization scheme is based on the implicit computation method and is suitable for implemented in standard CMOS process. The circuit is suitable for all

input waveforms. Moreover the wide bandwidth characteristic is obtained since the circuit structure is simple and requires a few components.

The characteristics of the proposed RMS-to-DC converter are studied by the implementation of CMOS complementary pairs CD4007 on a bread-board discrete circuit. The transient response, DC transfer characteristic and the error versus crest factor are tested by the experimentation. Due to the stray capacitances in the bread boarding circuit, the high frequency response capability was not measured directly, PSPICE simulation is used for study the high frequency performance. In addition, to confirm that this proposed circuit is suitable for implementing in monolithic integrated form. This circuit is also studied based on 0.5 microns CMOS technology AMIS process by PSPICE simulation results and it has been fabricated. The chip performances are tested by the measurement setup, there are agreed with the simulation and the implementation by CMOS complementary CD4007. The RMS-to-DC converter performances from the simulation, the experimental of discrete circuit and the experimental of real chip are included in this chapter. The simulation and experimental results are agreed with the prediction.

CHAPTER 4

Electronically and Linearly Tunable CMOS OTA

4.1 Introduction

Linear transconductors or voltage-to-current converter circuits are fundamental building blocks of analog circuits and systems. They are found useful in interface circuits, instrumentation amplifiers, continuous-time-filters and oscillators. In addition, when the transconductance gain of the transconductor can be electronically varied, they can also be applied in automatic gain control circuits and in analog multipliers. In the last two decades, it is well accepted that a linear transconductor, which is constructed from a bi-polar differential pair and current mirrors, called as an operational transconductance amplifier (OTA), is one of the essential active building blocks in the design of analog circuits [67]-[69]. This is due to the fact that the OTA is a low-cost device that has only a single high-impedance node and its transconductance gain g_m can be linearly controlled over more than four decades by means of an external bias current. Moreover, the implementation of analog circuits in such a way that employs only OTA as standard cells will not only be easily constructed from readily commercial available IC, but also significantly simplified the design.

The main objective of this chapter is, therefore, to present a circuit design technique for the synthesis of a linear electronically tunable CMOS OTA, called as an EOTA. Since, the realization method is achieved by squaring the transconconductance gain of the CMOS OTA, the transconductance gain of the EOTA is directly depend on the DC bias current. To provide a maximum output voltage swing and wide linearly tunable transconductance range, a balanced CMOS OTA or voltage to current transducer will be employed as basic active circuit elements to realize the EOTA, whereas the completed EOTA requires 3 balanced CMOS OTAs. Since it is generally assume that all MOS transistors are operating in the saturation region, hence the individual functions of the circuits are derived from the approximate square-law characteristic of MOS transistors in saturation. In addition, it is well accepted that the design and implementation of electronically tunable analog circuits using bipolar-based OTA as active circuit elements are well established and well tabulated. Then, having access to such a linear electronically tunable CMOS OTA, it would enable us to realize CMOS analog circuits with their property can be electronically tuned by simply replace a bipolar OTA with an EOTA. This kind of advantage will be

demonstrated through application examples. For the first example, the proposed EOTA is employed to implement a current multiplier circuit, that using only active elements and without the requirement of external passive elements and the current amplifier, a linearly voltage-controlled current amplifier and a linearly current-controlled CMOS current amplifier, are illustrated in the second application example. The circuit performances are studied through PSPICE simulation results.

4.2 The available electronically tunable CMOS OTA

In CMOS technology, several linearly tunable transconductors based on the use of MOS transistors operating in saturation region have been proposed in the literatures [70]-[73]. Most of them are functioning in voltage controlled mode. The method of source-follower of the reference [70] is operated in square law characteristic with constant source-bulk voltages, where the control voltage is applied to the gate. Whereas for the cross coupled connection methods [71]-[73], the transconductance control voltages are applied through voltage level shifters. However, their controllable voltage ranges are rather limited and only narrow linearly tunable transconductance ranges are available. In some applications, such as, an analog multiplier circuit, a frequency divider/multiplier circuit and an arbitrary power-law circuit, current controlled transcondcutors that this trasconductance gain can be linearly controllable by a DC bias current are preferable [74]-[76]. In the past, a current controlled CMOS transconductor was presented in [77]. But the linearly tunable transconductance range is narrow due to the MOS transistors are working in the weak-inversion region.

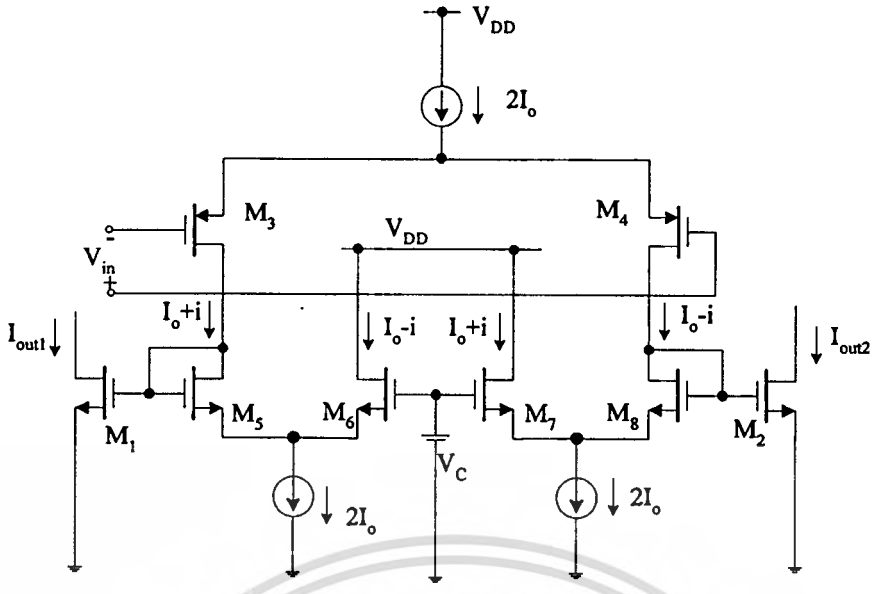

Fig. 4.1 A linear transconductor circuit [70]

In Fig. 4.1, the linear CMOS trasconductor circuit which proposed by *S.-C. Huang and M. Ismail* [70] has a transconductance linearly variable by a gate voltage (V_C). From this proposed circuit, the circuit is based on the square-law behavior of MOS transistors are biased in saturation regions

$$I_d = K\left(V_{GS} - V_{TH}\right)^2 \qquad (4.1)$$

Transistors M_1 and M_2 are the square-law transistors that perform the actual transconductor function. Transistor M_3-M_8 constitute three differential matched pairs with equal tail current $2I_o$. This pairs are connected in such a way that M_5-M_6 and M_7-M_8 carry the same currents as M_3-M_4. As a result of this, voltage V_{in} is copied to the transconductor transistors M_1 and M_2. This is shown as follows: presume that M_3 and M_4 are characterized by K_3 and V_{th3}, M_5-M_8 by K_5 and V_{th5}. Using equation (4.1) and referring to Fig. 4.1, the following relation may be written

$$V_{in} = \left(\sqrt{I_o + i} - \sqrt{I_o - i}\right) \Big/ \sqrt{K_3} \qquad (4.2)$$

$$V_{GS5} - V_{GS6} = V_{GS7} - V_{GS8} = \left(\sqrt{I_o + i} - \sqrt{I_o - i}\right) \Big/ \sqrt{K_3}$$

$$= \sqrt{K_3 / K_5}\, V_{in} \qquad (4.3)$$

From eqn. (4.3) that two proportional copies of V_{in} arise across the lower differential pairs. These voltages are added to and subtracted from transconductance control voltage V_C. Using eqn. (4.1) and presuming that M_1 and M_2 are charzcterised by K_1 and V_{TH1}, the output currents I_{out1} and I_{out2} can be calculated:

$$I_{out1} = K_1\left(V_C + \sqrt{K_3/K_5}V_{in} - V_{TH1}\right)^2 \tag{4.4}$$

$$I_{out2} = K_1\left(V_C - \sqrt{K_3/K_5}V_{in} - V_{TH1}\right)^2 \tag{4.5}$$

the differential output current (I_{out1}-I_{out2}) is in the function of the control voltage V_C as expressed in eqn. (4.6)

$$I_{out1} - I_{out2} = 4K_1(V_C - V_{TH1})\sqrt{K_3/K_5}V_{in} \tag{4.6}$$

eqn. (4.6) describes the transfer function of a linear transconductor. Its transconductance value is linearly variable by voltage V_C.

However the controllable range of this circuit is narrow due to V_C must be bias the MOS transistors keep operate in saturation region.

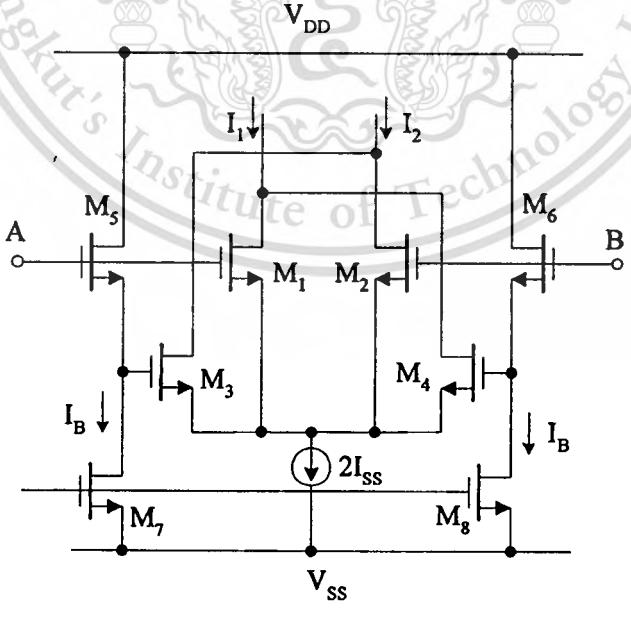

Fig. 4.2 Linear Transconductor circuit based on cross-coupled technique [72]

Fig. 4.2 shows the linear CMOS trasconductor circuit which was proposed by *Z. Wang and W. Gugenbuhl* [72] . The linear transfer characteristic is obtained by two cross-coupled differential transistor pairs operating in saturation pairwise at unequal bias, offering offset-free operation with both differential or single-ended input and differential output. From the figure, the MOS transistors M_1-M_4 and M_5-M_8 have the same dimensions operating in saturation regions. Therefore the control voltage V_B , which is applied to the gates of M_7 and M_8, is identical to the gate-source voltage of M_5 and M_6 and acts as a voltage shift from the inputs to the gate of M_3 and M_4. Applying the square law characteristics, the differential output current of this circuit can be expressed as

$$I_o = I_1 - I_2 = 2KV_B(V_P - V_N) \tag{4.7}$$

where V_P and V_N are the gate source voltage of M_1 and M_2.

Since the differential input voltage V_{in}=V_P-V_N eqn. (4.7) , yields

$$I_o = I_1 - I_2 = 2KV_BV_{in} \tag{4.8}$$

The transconductance is G=$2KV_B$, which is linearly controllable by the voltage V_B. However, its controllable voltage range is rather limited and only narrow linearly tunable transconductance range.

4.3 An Electronically and Linearly Tunable CMOS OTA (EOTA)

In this section, the realization method of an electronically and linearly tunable CMOS OTA is proposed. The proposed EOTA is achieved by squaring the transconductance gain of the balanced CMOS OTA. The EOTA transconductance gain can be linearly tuned by an external bias current for wide range (3 decades).

4.3.1 Circuit description the EOTA

For the purpose of the following analysis, we will assume that all MOS devices operate in the saturation region. It means that the transistor drain current I_D is characterized by a square-law model as

$$I_D = \begin{cases} K(V_{GS} - V_T)^2 & , \ for \ V_{GS} > V_T \\ 0 & , \ for \ V_{GS} \le V_T \end{cases} \tag{4.9}$$

where the transconductance parameter $K = \mu_n C_{ox} W/2L$, μ_n is the mobility of the carrier, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length, and V_{GS} and V_T are the gate-to-source and threshold voltages, respectively.

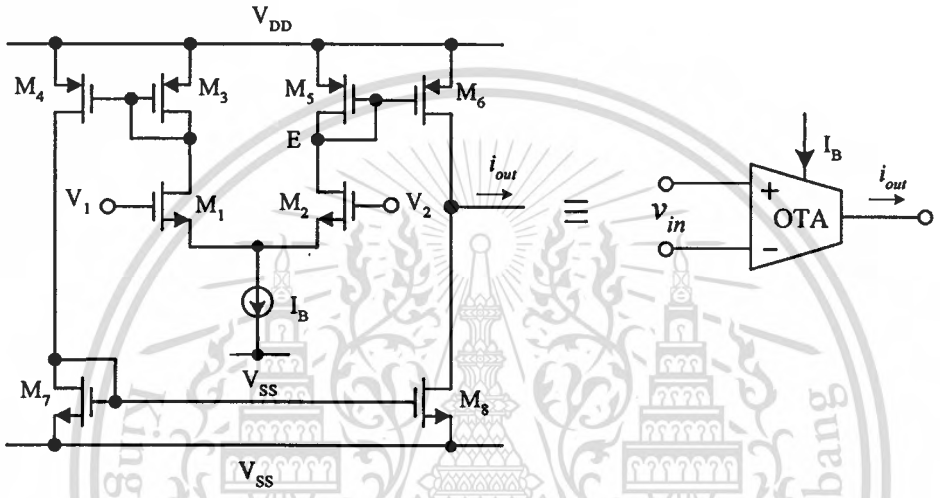

Fig. 2.11 Schematic diagram of a balanced CMOS OTA

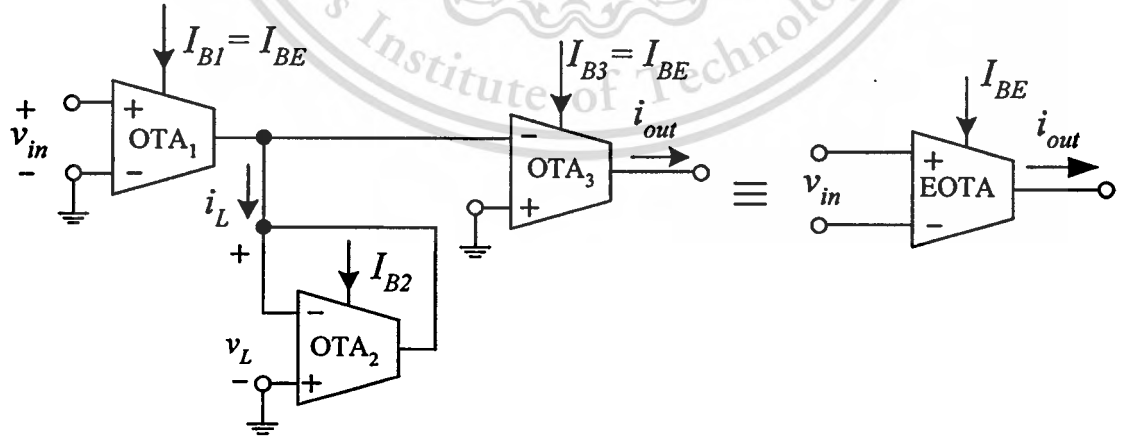

Fig. 4.3 The proposed electronically and linearly tunable CMOS OTA

Through the use of three balanced single-output CMOS OTAs, a CMOS-based electronically and linearly tunable OTA, called as an EOTA, can be realized by the circuit diagram shown in Fig. 4.3. The OTA_1 converts a differential input signal voltage $v_{in} = v_1 - v_2$ into a signal current i_L to flow into an active resistor R_L, formed by the OTA_2, where $R_L = 1/g_{m(OTA2)}$ and $g_{m(OTA2)}$ represents the transconductance gain of the OTA_2. Since the current signal $i_L = g_{m(OTA1)}V_{in}$, the voltage drop across the active resistor (OTA_2) becomes

$$v_L = i_L Z_L = g_{m(OTA1)} v_{in} \cdot \frac{1}{g_{m(OTA2)}} \tag{4.10}$$

The OTA_3 will convert the voltage v_L, with the transconductance gain of $g_{m(OTA3)}$, into the output current i_{out} as

$$i_{out} = g_{m(OTA3)} v_L \tag{4.11}$$

From eqns. (4.10) and (4.11), the current i_{out} can be rewritten as

$$i_{out} = \frac{g_{m(OTA1)} g_{m(OTA3)}}{g_{m(OTA2)}} v_{in} \tag{4.12}$$

Since $g_{m(OTA1)} = \sqrt{2I_{B1}K_1}$, $g_{m(OTA2)} = \sqrt{2I_{B2}K_2}$ and $g_{m(OTA3)} = \sqrt{2I_{B3}K_3}$, if we set $I_{B1}=I_{B3}=I_{BE}$, then from eqn. (4.12) we obtain

$$i_{out} = \frac{2I_{BE}\sqrt{K_1 K_3}}{\sqrt{2I_{B2}K_2}} V_{in} = g_{mT} v_{in} \tag{4.13}$$

where g_{mT} represents the transconductance gain of the proposed EOTA and can be expressed as

$$g_{mT} = 2I_{BE}K_T \tag{4.14}$$

and $K_T = \sqrt{K_1 K_3 / 2I_{B2}K_2}$, which can usually be kept to be constant. The eqn. (4.14) clearly indicted that the transconductance gain of the proposed EOTA can be electronically and linearly tuned by the bias current I_{BE}. This linear relationship is in the form that similar to the

transconductance gain of the bipolar based OTA that found useful in many applications [78]. Since the balanced CMOS OTA is formed by MOS coupled pair and current mirrors, therefore, the proposed EOTA is very suitable for fabricating in CMOS integrated form.

4.3.2 Circuit Performances

4.3.2.1 Operating range

It is well accepted that the prediction of the eqn. (4.14) will be valid only for a small value of V_{in}. From the eqn. (2.44), since OTA_1 and OTA_3 are formed by MOS coupled pairs, to maintain in the linear range and low total harmonic distortion, the voltages V_{in} and V_L should respectively be restricted to the ranges of [79]

$$|V_L|_{MAX} = 0.4/\sqrt{2K} \cdot Z_L \text{ and } |V_{in}|_{MAX} = 0.4\sqrt{I_{BB}/K} \qquad (4.15)$$

where it should be noted from the eqn. (4.15) that the maximum usable voltage range is limited by $\left| V_L \right|_{MAX}$ if $g_{m(OTA1)}/g_{m(OTA2)} > 1$ and it is limited by $\left| V_{in} \right|_{MAX}$ if $g_{m(OTA1)}/g_{m(OTA2)} < 1$. For example, for I_{BE} = 1mA and I_{B2} = 700μA, the maximum usable range is determined by $\left| V_L \right|_{MAX}$ and $\left| V_L \right|_{MAX}$ is about 0.94 volts, for $K = \mu_n C_{ox} W/2L = 1.27 \times 10^{-4}$ A/V^2, $\mu_n C_{ox} = 5.08 \times 10^{-5}$ V and $W/2L = 2.5$.

4.3.2.2 Conversion Errors

4.3.2.2.1 Error analysis

The transconductance gain error that results from in the inaccuracy of the EOTA can be determined from a large signal analysis. Consider the balanced CMOS OTA, the transconductance gain G_m of the eqn. (2.45) can be written as

$$G_m = \frac{i_{out}}{V_{in}} = \sqrt{2I_B K} \cdot \sqrt{1 - \frac{KV_{in}^2}{2I_B}}, for -\sqrt{\frac{I_B}{K}} \le V_{in} \le \sqrt{\frac{I_B}{K}} \qquad (4.16)$$

If we set the transconductance error of the balanced CMOS OTA of the Fig. 4.3 as $E=\frac{KV_{in}^2}{2I_{BB}}$, then eqn. (4.16) can be rewritten as

$$G_m = \frac{i_{out}}{V_{in}} = \sqrt{2I_B K}\cdot\sqrt{1-E} \tag{4.17}$$

We found that the G_m will equal to the g_m of eqn. (2.46) in the condition that $KV_{in}^2/2I_B \ll 1$. This can be achieved by keeping the input voltage signal V_{in} small or set the DC bias current I_B to a large value.

By applying the G_m of the eqn. (4.17) to the circuit of Fig. 4.3, we obtain the transconductance gain of the proposed EOTA for large signal as

$$G_{mT} = 2I_{BE}K_T\left(1+\frac{\sqrt{1-E_1}\sqrt{1-E_3}-\sqrt{1-E_2}}{\sqrt{1-E_2}}\right) \tag{4.18}$$

where the errors $E_1=\frac{K_1V_{in1}^2}{2I_{B1}}$, $E_2=\frac{K_2V_{in2}^2}{2I_{B2}}$ and $E_3=\frac{K_3V_{in3}^2}{2I_{B3}}$ are the transconductance errors due to the OTA_1, OTA_2 and OTA_3 respectively. Given that E_T is the transconductance error of the EOTA from the linear transconductance gain, we can write

$$E_T = \frac{\sqrt{1-E_1}\sqrt{1-E_3}-\sqrt{1-E_2}}{\sqrt{1-E_2}} \tag{4.19}$$

Thus, we have the percent of the conversion error as

$$\%E_T = \frac{\sqrt{1-E_1}\sqrt{1-E_3}-\sqrt{1-E_2}}{\sqrt{1-E_2}}\times 100\% \tag{4.20}$$

For example, if V_{in1} = 0.5V, V_{in2}= V_{in3}= 0.751V, I_{B1}= I_{B3}= I_{BE} = 1mA, I_{B2}= 700μA and K_1= K_2= K_3= 1.27×10^{-4}, the resulting transconductance error ($\%E_T$) is equal to 0.54%

4.3.2.3 High frequency response

Due to the proposed electronically and linearly tunable CMOS OTA as shown in Fig. 4.3 is composed of three balanced CMOS OTAs, the high frequency response of this circuit can be verified by treated as the balanced CMOS OTAs that are connected in cascade. Using of the Fig. 2.11, the transconductance gain $g_{m(OTA)}$ of the CMOS OTA is now model as a single dominant pole as [80][84]

$$g_{m(OTA)} = g_{m2} \Big/ \left[1+\left(sC_p/g_{m5}\right)\right] \tag{4.21}$$

where g_{m2} and g_{m5} denote the transconductance of the transistor M_2 and M_5 of the OTA, respectively. From the Fig. 2.11, we denote C_p as the capacitance that associated with the node E of the current mirror M_5-M_6 and $C_p = C_{gs2}+C_{gd2}+C_{gs5}+C_{gd5}+C_{gs6}$ where C_{gs} represents the gate-source capacitance of the transistor and C_{gd} represent the gate-drain capacitance of the transistor.

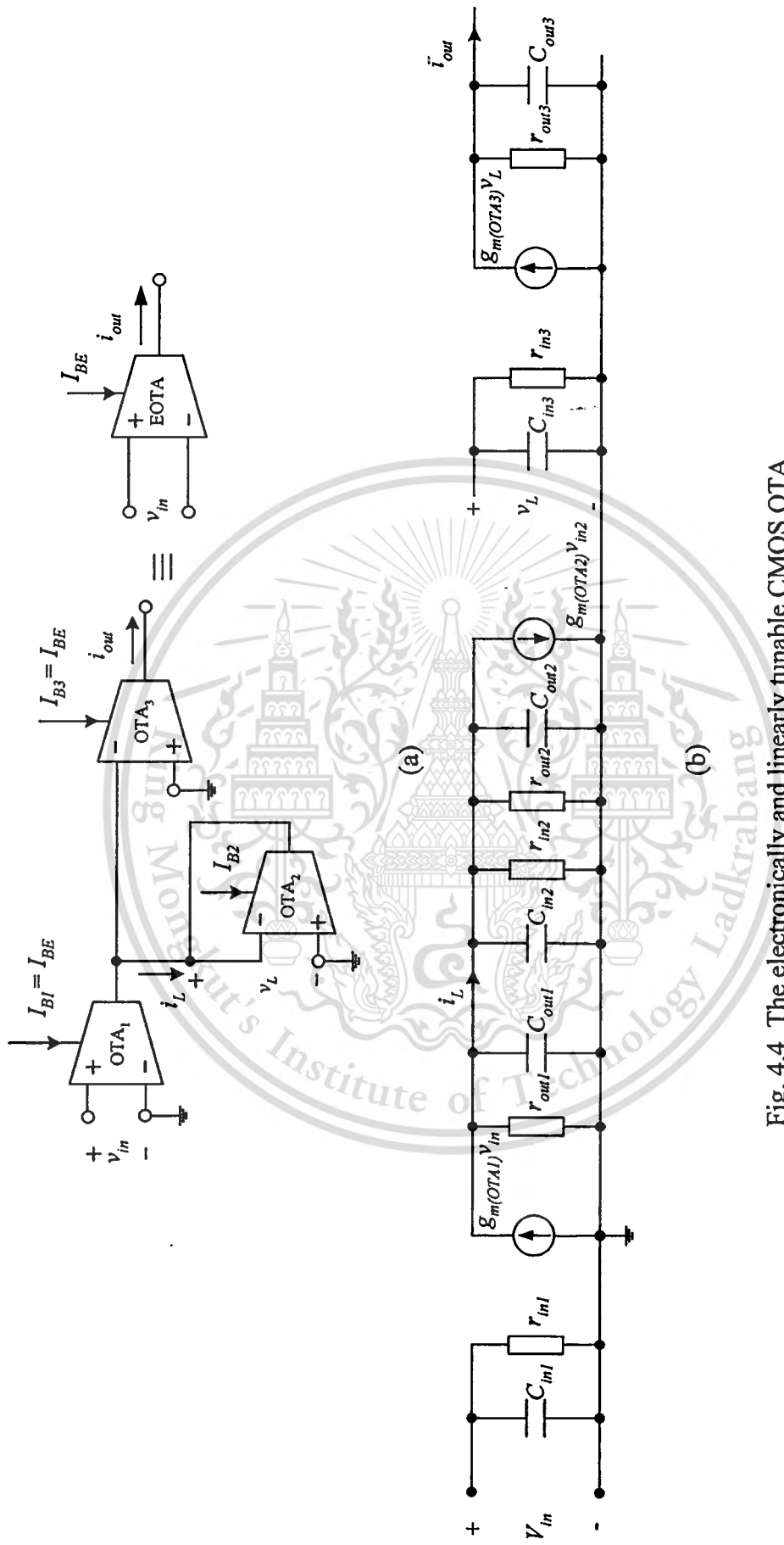

Fig. 4.4 The electronically and linearly tunable CMOS OTA

(a) building block diagram
(b) small signal equivalent circuit

From the Fig. 4.4, the active resistor R_L which is formed by OTA_2 can be expressed as

$$R_L = \frac{1}{g_{m(OTA2)} + g_{in(2)} + g_{out(2)} + s(C_{in(2)} + C_{out(2)})} \quad (4.22)$$

Where $g_{m(OTA2)}$ is transconductance gain of the OTA_2

$g_{in(2)} = 1/r_{in(2)}$ where $r_{in(2)}$ is the input resistance of OTA_2

$g_{out(2)} = 1/r_{out(2)}$ where $r_{out(2)}$ is the output resistance of OTA_2

$C_{in(2)}$ is the input capacitance of the OTA_2

$C_{out(2)}$ is the output capacitance of the OTA_2

If $g_{m(OTA2)} >> g_{in(2)}$, $g_{out(2)}$ and $C_{p(2)} >> C_{out(2)}$ and $C_{in(2)} = C_{gs1}+C_{gs2}$, therefore eqn.(4.22) can be approximately expressed as

$$R_L = \frac{1}{g_{m(OTA2)} + sC_{in(2)}} \quad (4.23)$$

Through circuit analysis using eqn.(4.23), the transfer function of the EOTA can be expressed as

$$\frac{i_{out}(s)}{V_{in}(s)} = \frac{g_{m(OTA1)}g_{m(OTA3)}}{g_{m(OTA2)}} \frac{(s+z_2)}{(s+p_1)(s+p_3)(s+p_{L1})(s+p_{L2})} \quad (4.24)$$

Then from eqn. (4.24), the zero and poles z_2, p_1, p_3, p_{L1} and p_{L2} can be respectively expressed as

$$p_1 = \frac{g_{m5(1)}}{2\pi C_{p(1)}},\ p_3 = \frac{g_{m5(3)}}{2\pi C_{p(3)}},\ z_2 = \frac{g_{m5(2)}}{2\pi C_{p(2)}},\ p_{L1}, p_{L2} = \frac{-\frac{C_{in(2)}}{g_{m2(2)}} \pm \sqrt{\left(\frac{C_{in(2)}}{g_{m2(2)}}\right)^2 - 4\frac{g_{m5(2)}C_{in(2)}C_{p(2)}}{g_{m2(2)}}}}{2\frac{g_{m5(2)}C_{in(2)}C_{p(2)}}{g_{m2(2)}}} \quad (4.25)$$

Note that the poles due to the active resistor R_L, p_{L1} and p_{L2}, are always real poles since $\left(C_{in(2)}/g_{m2(2)}\right)^2 > -4\left(g_{m5(2)}C_{in(2)}C_{p(2)}\right)/g_{m2(2)}$, where $g_{m(OTA1)} = g_{m2(1)}$, $g_{m(OTA2)} = g_{m2(2)}$ and $g_{m(OTA3)} = g_{m2(3)}$. The $g_{mi(1)}$, $g_{mi(2)}$ and $g_{mi(3)}$ represent the transconductance of transistor M_i of OTA_1, OTA_2 and OTA_3 respectively, for $i = 1, 2, 3,...$ and $C_{p(1)}$, $C_{p(2)}$, and $C_{p(3)}$ represent the total capacitances at nodes E

of the OTA_1, OTA_2 and OTA_3, respectively. For example, the following data have been used; V_{in} = 0.1V, I_{BE} = 100μA and I_{B2} = 40μA, $g_{m(OTA1)} = g_{m2(1)} = 1.66\times10^{-4}AV^{-1}$, $g_{m(OTA2)} = g_{m2(2)} = 9.44\times10^{-5}AV^{-1}$, $g_{m(OTA3)} = g_{m2(3)} = 1.56\times10^{-4}\ AV^{-1}$, $g_{m5(1)} = 1.96\times10^{-4}\ AV^{-1}$, $g_{m5(2)} = 1.18\times10^{-4}AV^{-1}$, $g_{m5(3)} = 1.96\times10^{-4}\ AV^{-1}$, $C_{gs1} = C_{gs2}$ = 0.268 pF, $C_{gs5} = C_{gs6}$ = 0.54 pF and $C_{gd2} = C_{gd5}$ = 0pF (at saturation region C_{gd}=0). $C_{in(2)} = C_{gs1(2)}+C_{gs2(2)}$ = 0.536pF.

The poles and zero frequencies are located as p_1 = 23 MHz, p_3 = 23 MHz , p_{L1} = 88 MHz, $p_{L2}= 1.26\times10^{6}$ MHz and z_2 = 14 MHz. We found that the high frequency limitation is due to the zero (z_2) that associated with the OTA_2. Since these poles and zero locations depend on the DC bias current of the OTAs which can be expressed in eqn.(4.25), therefore the circuit can be operated in a wider bandwidth by increasing the dc bias currents (higher resistance value) of the circuit. For example, in the case of, V_{in} = 0.1V, I_{BE} = 1mA and I_{B2} = 400μA, the high frequency limitation is located at 38MHz.

4.3.3 Application examples

4.3.3.1 Current Multiplier

In this section, we will propose the use of the EOTA to realize a current-mode multiplier, which use only active circuit elements and not require external passive circuit elements. The proposed current-mode multiplier circuit is shown in Fig. 4.2 which this structure has been proposed by the author in [81]. It should be noted from the eqn. (4.14) that if the EOTA is operated in the linear range, the transconductance is $g_{mT} = 2I_{BE}K_T$, which g_{mT} can be tuned by the DC bias current I_{BE}.

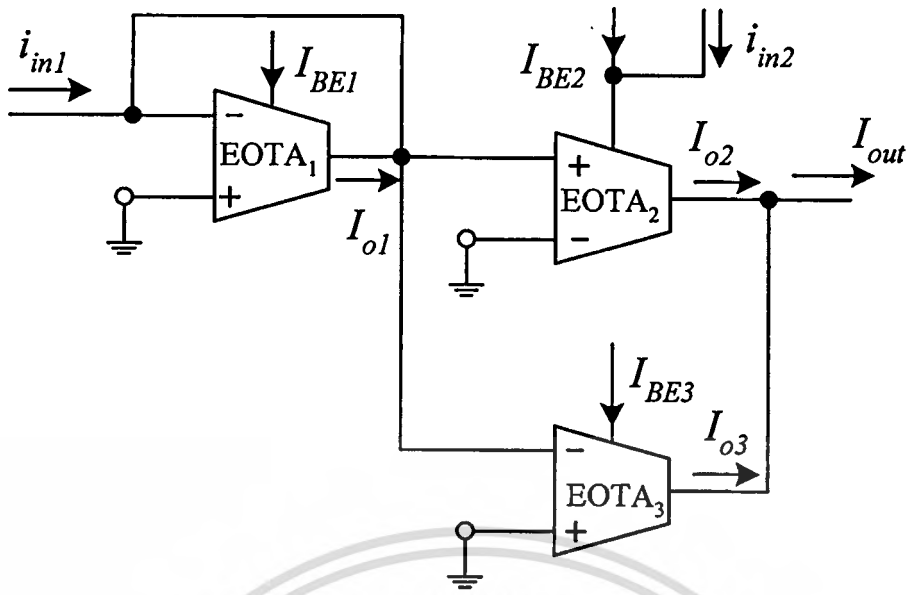

Fig. 4.5 The current-mode multiplier circuit using the proposed EOTA.

From the Fig. 4.5, the input signal current i_{in1} is injected into the EOTA$_1$, which is connected as a current controlled grounded resistor. The voltage across the EOTA$_1$ is then used as the input voltage for the EOTA$_2$ and EOTA$_3$. The input signal current i_{in2} is added with the bias current I_{BE2} of the EOTA$_2$. Let g_{mT1}, g_{mT2} and g_{mT3} be the transconductance gains of the EOTA$_1$, EOTA$_2$ and EOTA$_3$, respectively. Then from the eqn. (4.14) and from routine circuit analysis the output currents I_{o2} and I_{o3} of the EOTA$_2$ and EOTA$_3$, respectively, can be written as

$$I_{o2} = \frac{g_{mT2}}{g_{mT1}} i_{in1} = \frac{(I_{BE2} + i_{in2})}{I_{BE1}} i_{in1} \tag{4.26}$$

and

$$I_{o3} = -\frac{g_{mT3}}{g_{mT1}} i_{in1} = -\frac{I_{BE3}}{I_{BE1}} i_{in1} \tag{4.27}$$

where I_{BE1} , I_{BE2} and I_{BE3} represent the DC bias currents of the EOTA$_1$, EOTA$_2$ and EOTA$_3$, respectively, and the transconductance gains $g_{mT1} = 2I_{BE1}K_{T1}$, $g_{mT2} = 2(I_{BE2} + i_{in2})K_{T2}$ and $g_{mT3} = 2I_{BE3}K_{T3}$. Noting from the Fig. 2.11 and Fig. 4.5, that the DC bias current of the EOTA (I_{BE}) of the multiplier circuit can be achieved by setting the DC bias currents of the OTA$_1$ and the OTA$_3$ to $I_{B1} = I_{B3} = I_{BE}$. If we set $I_{BE2} = I_{BE3} = I_b$, the output current I_{out} of the circuit that is the summation of the currents I_{o2} and I_{o3} can be expressed as

$$I_{out} = I_{o2} + I_{o3} = \frac{i_{in1} i_{in2}}{I_{BE1}} \tag{4.28}$$

which is in the form of a current-mode multiplication function.

4.3.3.2 Current Amplifiers

In this section, the realization of the current amplifiers by using EOTA, which use only active circuit elements, are described.

4.3.3.2.1 Linearly voltage-controlled current amplifier

The proposed voltage-controlled tunable current amplifier is constructed as the circuit diagram in Fig. 4.6. Where the input signal current (i_{in}) is added to the DC bias current (I_{BE}). The control voltage (V_C) is supplied to the input of EOTA. From the routine circuit analysis of Fig. 4.3, the output current (i_{out}) can be expressed as

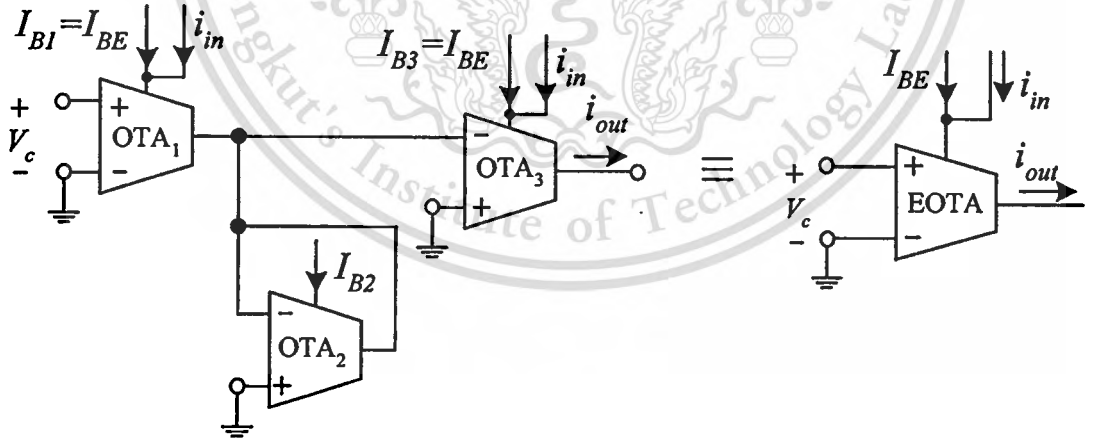

Fig. 4.6 A linearly voltage-controlled current amplifier

$$i_{out} = 2K_T V_C \left(i_{in} + I_{BE}\right) \tag{4.29}$$

$$i_{out} = \left(2K_T V_C\right) i_{in} + \left(2K_T V_C\right) I_{BE} \tag{4.30}$$

From the eqn. (4.30), we found that the output current consists of the AC signal and DC current ($2K_T V_C \cdot I_{BE}$). If we can compensate this DC current, the output current of the voltage controlled current amplifier can be rewritten as

$$i_{out} = \left(2K_T V_C\right) i_{in} = A_i i_{in} \tag{4.31}$$

Where A_i is the current gain of the proposed voltage controlled current amplifier and can expressed as

$$A_i = 2K_T V_C \tag{4.32}$$

and $K_T = \sqrt{K_1 K_3 / 2I_{B2} K_2}$. It shows that the output current can be linearly tuned by the DC voltage V_C.

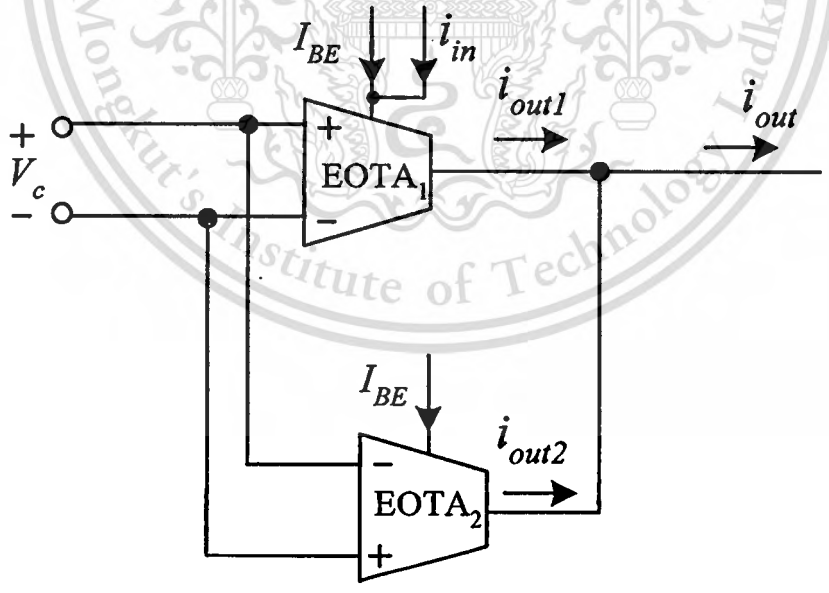

Fig. 4.7 Schematic diagram of the current amplifier with DC gain compensated

Fig. 4.7 shows the circuit building block to eliminate the DC current of Fig. 4.6 where i_{out1} and i_{out2} are given as,

$$i_{out1} = (2K_T V_C) i_{in} + (2K_T V_C) I_{BE} \tag{4.33}$$

and

$$i_{out2} = -(2K_T V_C) I_{BE} \tag{4.34}$$

The output current i_{out} of the circuit, that is the summation of the currents i_{out1} and i_{out2}, can be expressed as

$$i_{out} = i_{out1} + i_{out2} = (2K_T V_C) i_{in} \tag{4.35}$$

From eqn. (4.35) it is clearly seen that the circuit can operate as a current amplifier, the gain of which can be linearly tuned by the control voltage (V_C).

4.3.3.2.2 Linearly current-controlled CMOS current amplifier

A current amplifier design based by on EOTA that can electronically and linearly be tunable is proposed in Fig. 4.8 which is composed of one balanced single-output CMOS OTA and one EOTA.

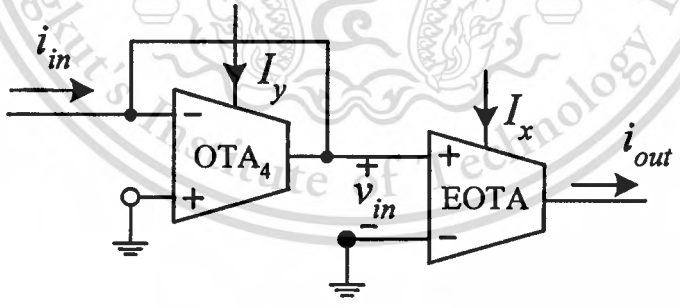

Fig. 4.8 A linearly current-controlled tunable current amplifier

The input current (i_{in}) is injected into the OTA_4, which is formed as an active resistor ($1/g_{m(OTA4)}$). The voltage drop across the active resistor (OTA_4) is then used as an input voltage (v_{in}) for EOTA and can be expressed as

$$v_{in} = \frac{i_{in}}{g_{m(OTA4)}} \tag{4.36}$$

The EOTA will convert the voltage v_{in} into the output current i_{out} as

$$i_{out} = g_{mT} v_{in} \tag{4.37}$$

From eqns. (4.36) and (4.37), the current i_{out} of the proposed current-controlled current amplifier can be written as

$$i_{out} = \frac{g_{mT}}{g_{m(OTA4)}} i_{in} \tag{4.38}$$

where $g_{mT} = g_{m(OTA1)} g_{m(OTA3)} / g_{m(OTA2)}$, $g_{m(OTA1)} = \sqrt{2 I_{B1} K_1}$, $g_{m(OTA2)} = \sqrt{2 I_{B2} K_2}$, $g_{m(OTA3)} = \sqrt{2 I_{B3} K_3}$ and $g_{m(OTA4)} = \sqrt{2 I_{B4} K_4}$. If we set $K_1 = K_2 = K_3 = K_4 = K$ and $I_{B4} = I_{B2} = I_y$, $I_{B1} = I_{B3} = I_{BE} = I_x$, then from eqn. (4.38) we obtain

$$i_{out} = \frac{g_{m(OTA1)} g_{m(OTA3)}}{g_{m(OTA2)} g_{m(OTA4)}} i_{in} \tag{4.39}$$

Since

$$i_{out} = \frac{I_x}{I_y} i_{in} = A_C i_{in} \tag{4.40}$$

where A_C is the current gain of the proposed current amplifier and can be expressed as

$$A_C = \frac{I_x}{I_y} \tag{4.41}$$

We can see that the output current can be tuned by the DC bias current I_x and I_y. If indicates that the gain is direct proportional to I_x and inverse proportional to I_y.

4.4 Simulation results

The performance of the proposed electronically and linearly tunable CMOS OTA was verified through the use of PSPICE simulation results. All the OTA was simulated by using CMOS transistor parameters of the SCN2 level 2 of MOSIS. The transistor dimensions of the circuit in Fig. 2.11 are in micron, where the dimensions of the transistors M_1 and M_2 are W=50μm and L=10μm, the dimensions of the transistor M_3-M_8 are W=100μm and L=10μm. The power supply voltage were set to $V_{DD} = -V_{SS} = 5V$.

To demonstrate that the circuit can linearly converted voltage signal into current signal, Fig. 4.9 shows the simulated transfer characteristic of the EOTA of the Fig. 4.3. The plots of the output current I_{out} versus the input voltage V_{in} show that, for the dc bias current (I_{BE}) in the cases of 1mA, 800μA and 400μA, the EOTA can linearly convert the input voltage into output signal current with nonlinearity of less than 1% for the input voltage (V_{in}) in the ranges of -1V to 1V, -0.86V to 0.86V and -0.66V to 0.66V, respectively. These results were agreed with the prediction value from the eqn. (4.14). The conversion error in the case of I_{BE}=1mA is plot in Fig. 4.10. For example, for the case of the DC bias current I_{BE} = 1mA and for V_{in} = 0.86V, I_{B2} = 700μA, the transconductance gain $g_{mT} = 5.398 \times 10^{-4}$ AV^{-1}, where the conversion error is about 0.6%. The frequency response of the EOTA was also studied, where the -3 dB bandwidth of about 120 MHz is achieved.

The relation between the transconductance and the bias current I_{BE} was measured by fixing V_{in} = 0.1V and varying I_{BE} from 10nA to 1mA. The results are plot in Fig. 4.11. From this, it can be seen that the transconductance is linearly dependent upon the bias current I_{BE} over the range of 1μA to 1mA (three decades). It found that the transconductace can be tune linearly by I_{BE}, where at I_{BE} =1mA the conversion error from simulation result is about 0.68%, where its conversion error of g_{mT} versus I_{BE} is plot in Fig. 4.12.

The lower limit of the circuit is due to condition in eqn. (2.44) that transistors must be operating in saturation region. In the cases of V_{in} = 0.1V, 0.2V and 0.5V, respectively, we found that the DC bias current I_{BE} must be more than 1μA, 5μA and 32μA, respectively.

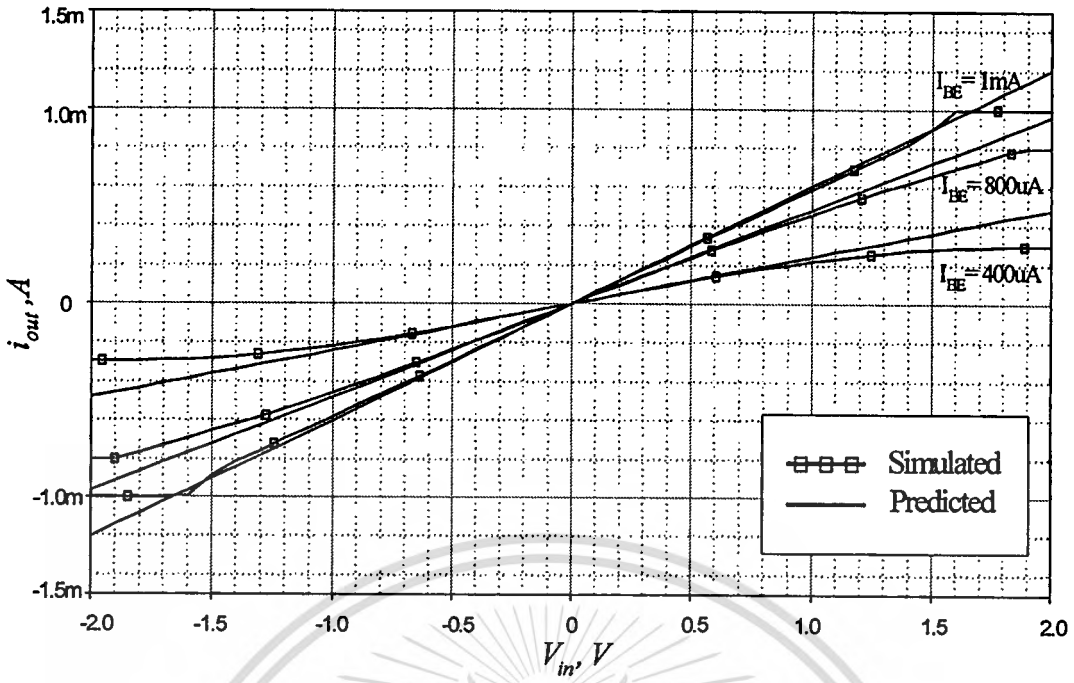

Fig. 4.9 DC transfer characteristics of the EOTA

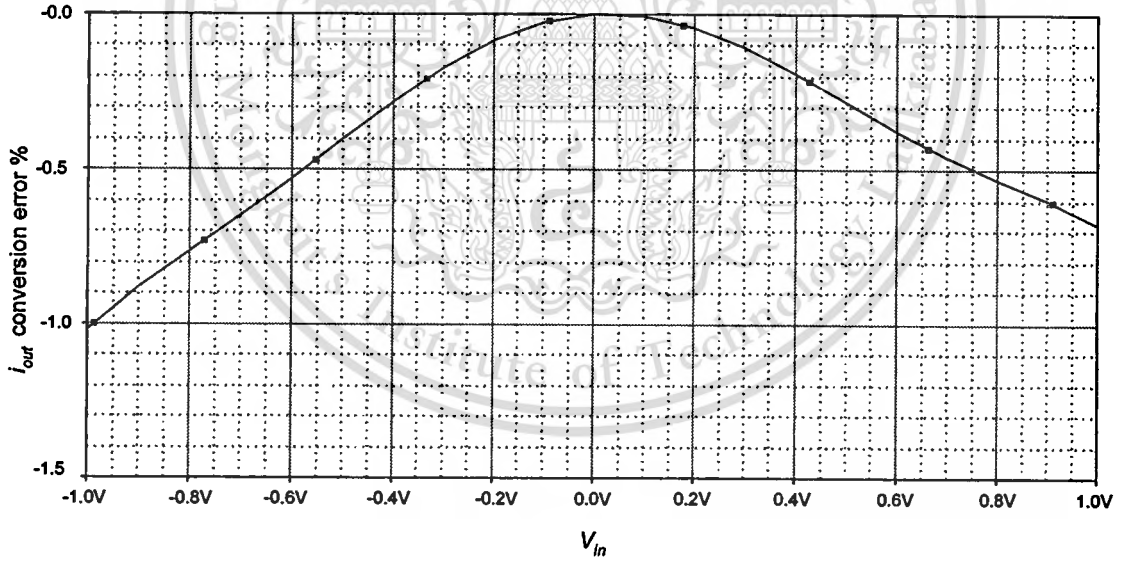

Fig. 4.10 Conversion error of i_{out} versus V_{in} of the EOTA

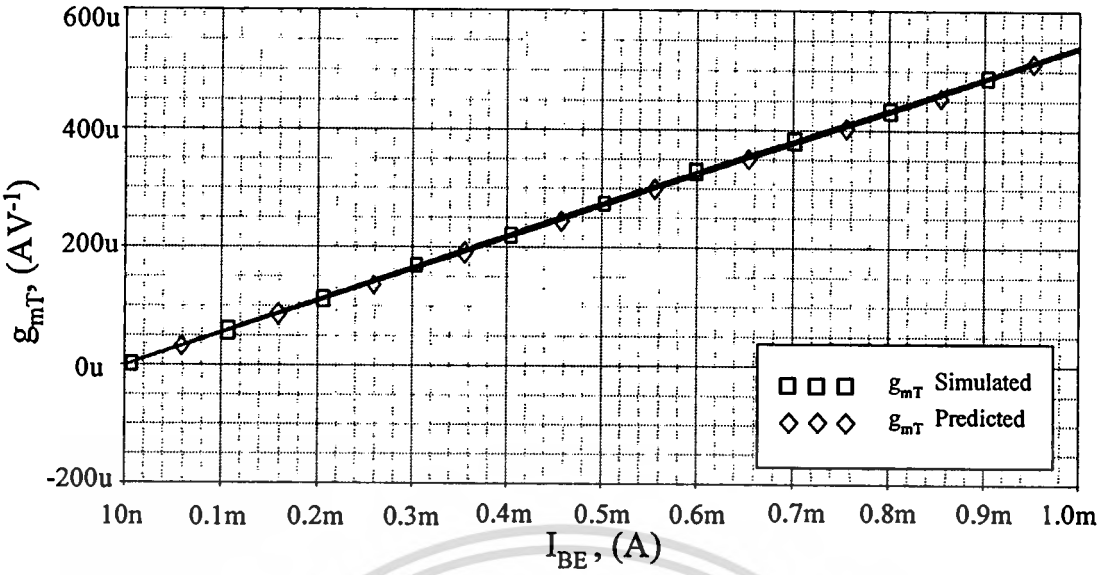

Fig. 4.11 Linear transconductance tunable range

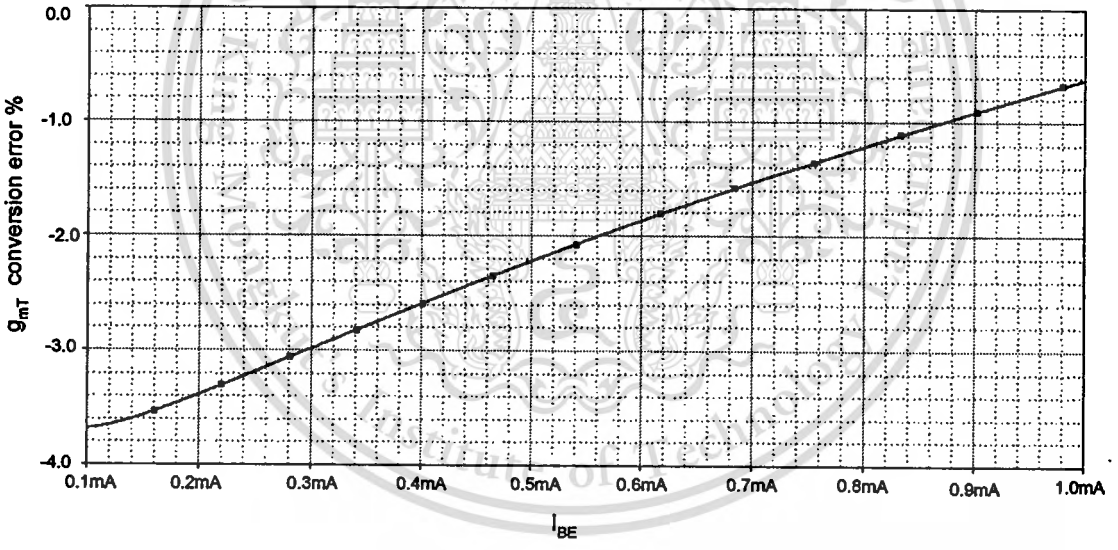

Fig. 4.12 Conversion error of g_{mT} versus I_{BE} of the EOTA

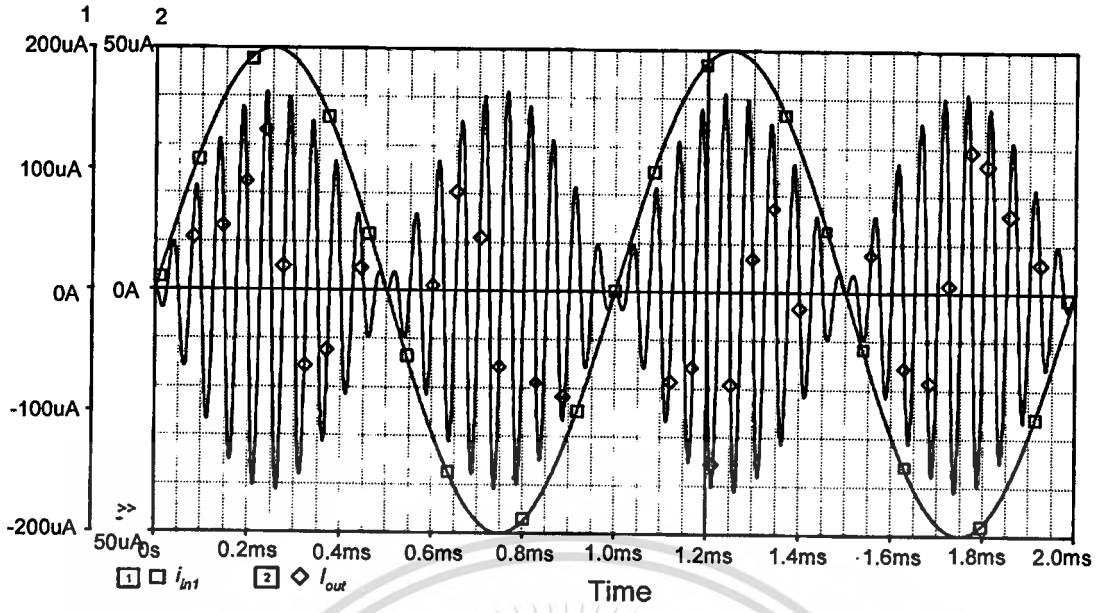

Fig. 4.13 Simulated transient response for the multiplier circuit

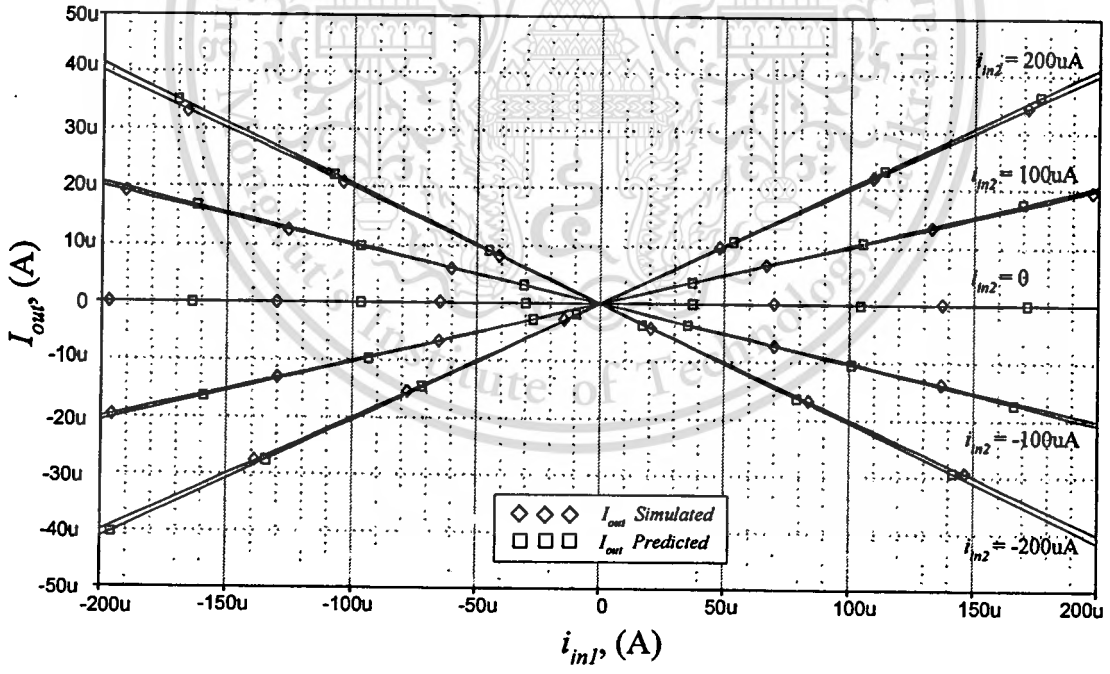

Fig. 4.14 Simulated DC transfer characteristic of the multiplier

Accordingly these limits were agreed very well with the prediction that the of CMOS transistors are operating in saturation region from eqn. (2.45). At the DC bias current I_{BE} = 1mA, in the case of V_{in} = 0.5V, I_{B2}= 880μA, the result shows that the transconductance gain g_{mT}= 5.398×10^{-4} AV^{-1} is achieved. The conversion error from the simulation result is about 0.5%, this results are agree with the conversion error predicted from eqn.(4.17).

To demonstrate that the circuit of Fig. 4.4 can be functioned as current multiplier, two sinusoidal current signals are applied. Fig. 4.13 shows the response for the case of $i_{in1} = 0.2\sin(2\pi1000t)$ mA, $i_{in2} = 0.2\sin(2\pi20000t)$ mA and I_{BE1} = 1mA. This result confirms that the circuit can accurately modulate two different input signal currents. The DC transfer characteristics of the multiplier circuit shown in Fig. 4.14 were observed by setting the bias currents I_{BE1}= I_{BE2}= I_{BE3}= 1mA, and the input current i_{in1} and i_{in2} are varied from -200μA to 200μA with 100μA per step. The transfer characteristic demonstrated that the simulated and calculated data are agreed very well over the input range of± 190μA with the error of less than 1%. The high frequency characteristic of the multiplier circuit is also studied. The simulated –3dB bandwidth for the case of the input i_{in1} to the output I_{out}, with i_{in1} = 0.5sin(2π10000t) mA, i_{in2}= 500μA and I_{BE1} = 1mA, is about 75 MHz and the simulated –3dB bandwidth of the circuit for the input i_{in2} to the output I_{out}, with i_{in2} = 0.5sin(2π10000t) mA, i_{in1}= 500μA and I_{BE1} = 1mA, is about 71 MHz.

For the linearly voltage-controlled current amplifier in Fig. 4.6, we set I_{BE}= 600μA and I_{B2}=1mA. Fig. 4.15 shows the current transfer characteristic of the proposed voltage controlled current amplifier. This figure shows the plot of the output current i_{out} against the input current i_{in} from -500μA to 500μA for different V_c values; V_c= 0.1V, 0.5V, 1V and 1.5V. The simulation and calculated data are agreed very well, where the conversion error of i_{out} versus i_{in} in the case of V_c =0.5V is plot in Fig. 4.16. For example at V_c = 0.5V, over the ± 500μA input range, error was less than 5%.

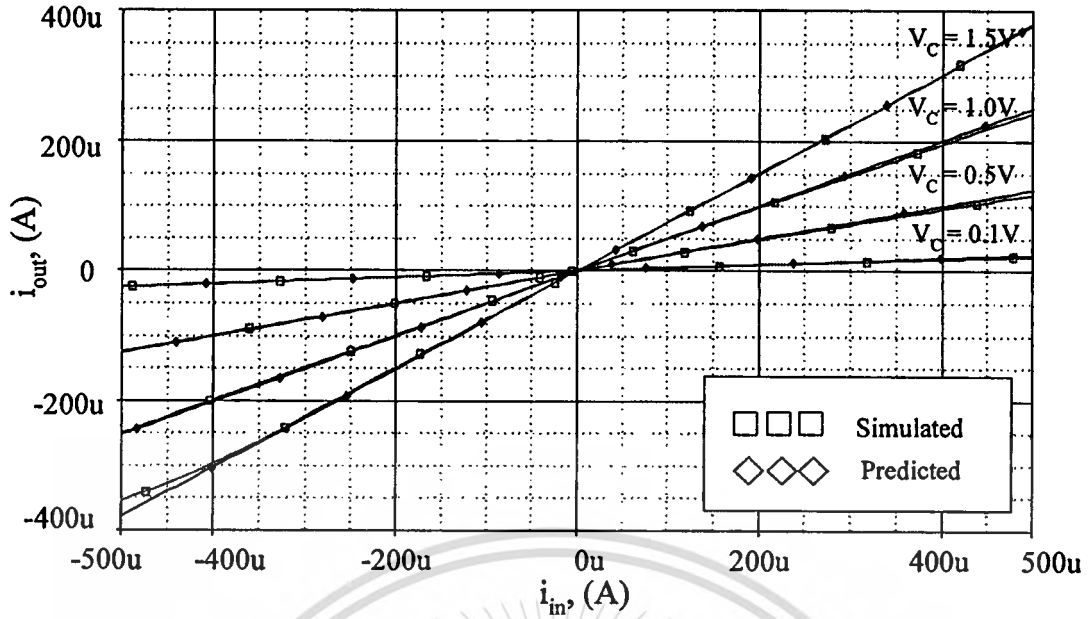

Fig. 4.15 The current transfer characteristic of the voltage controlled current amplifier

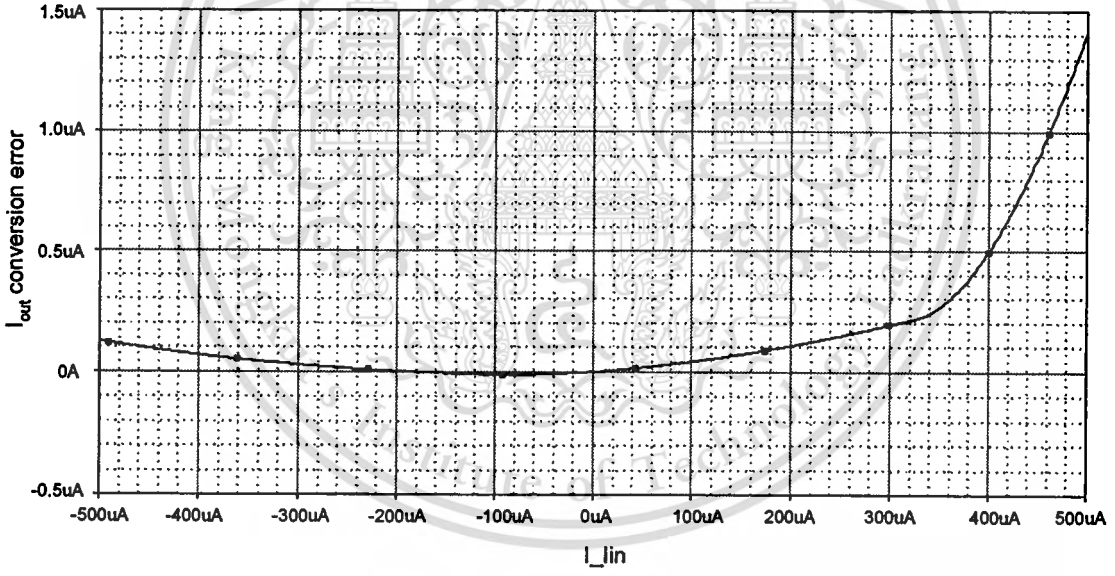

Fig. 4.16 Conversion error of i_{out} versus i_{in} of voltage controlled current amplifier

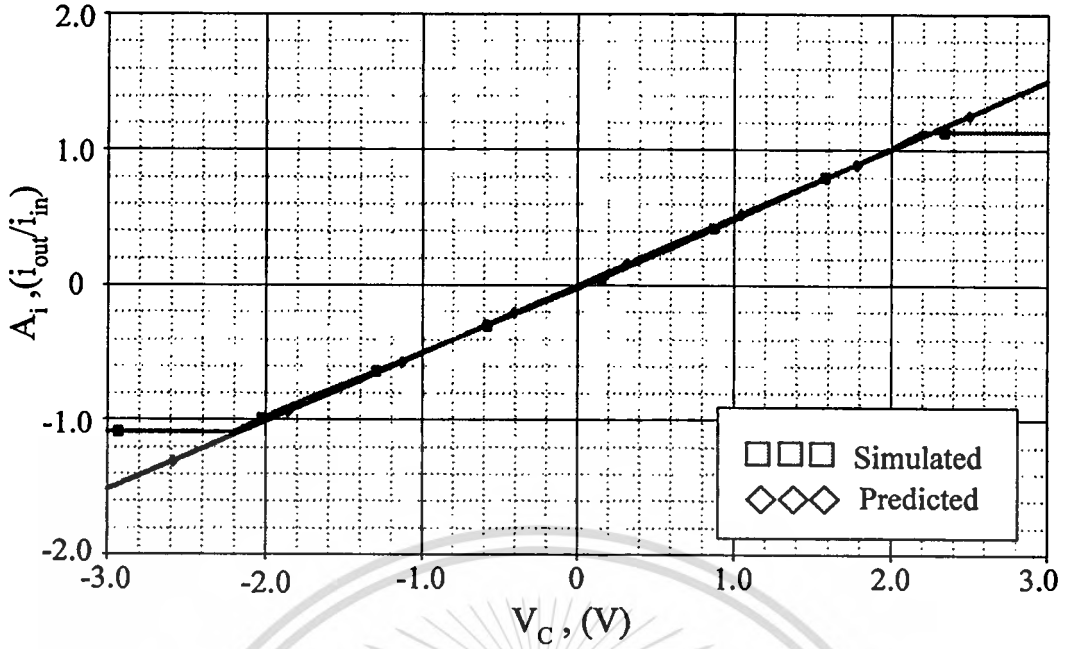

Fig. 4.17 The performance of gain controllability of the voltage controlled current amplifier

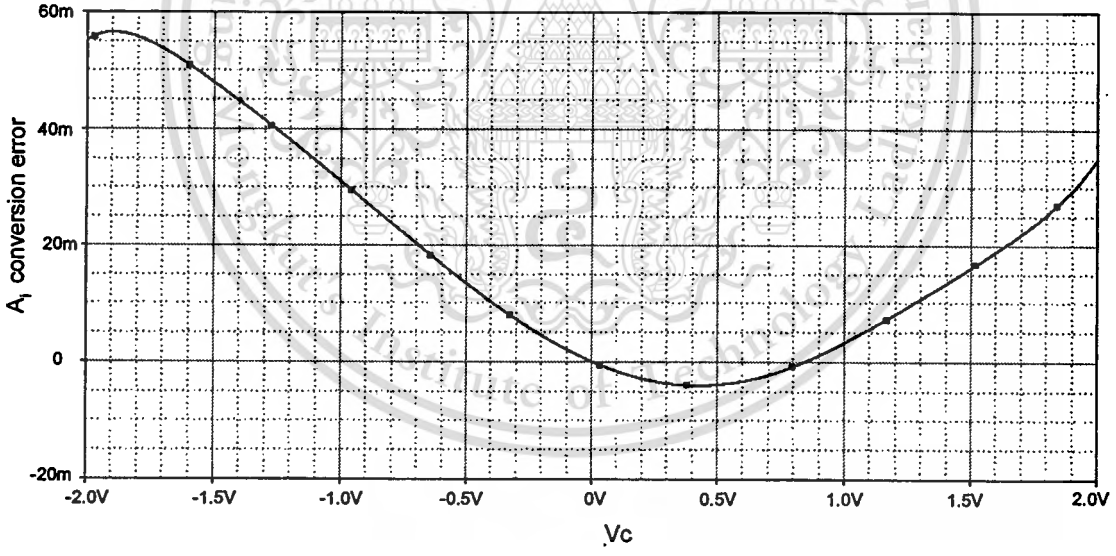

Fig. 4.18 Conversion error of A_i versus V_c of voltage controlled current amplifier

Fig. 4.17 represents the plots of the variation of current gain $A_i = i_{out}/i_{in}$ versus the control voltage V_c in the case of i_{in}=10μA. It is seen that both the results from simulation and calculation are in good agreement, where the conversion error of A_i is plot in Fig. 4.18. The nonlinearity is seen to be less than 5% for the control voltage (V_c) range from -2V to 2V, The control voltage range of the circuit depend on condition in eqn. (2.45) that transistor must be operating in saturation region.

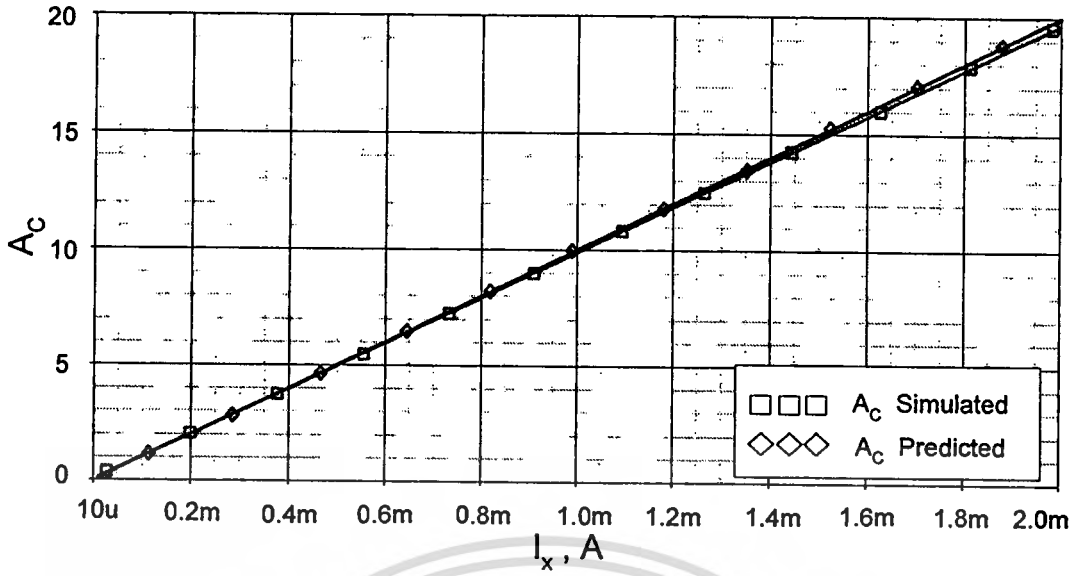

Fig. 4.19 The gain controllability of the linearly current-controlled current amplifier

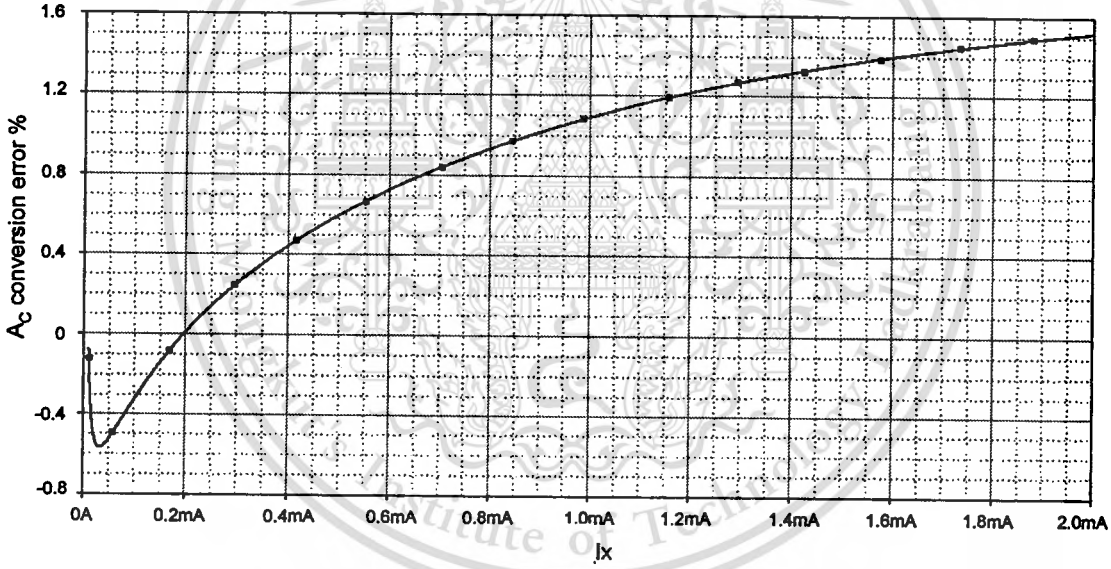

Fig. 4.20 Conversion error of A_c versus I_x of the linearly current-controlled current amplifier

The gain and the controllability of the proposed current-controlled current amplifier in Fig. 4.8 obtained by simulation and calculation are shown in Fig. 4.19, for I_x from 10μA to 2mA where I_y is kept be constant at 100μA. It is seen that both results are in good agreement, where the conversion error of A_c versus I_X is plot in Fig. 4.20. For example, at I_x = 2mA, the conversion error is less than 1.5%. We found that the current gain (A_C) can be electronically and linearly tuned from 0.1 to 20 (3 decade).

Table 4.1 The performance of the proposed linearly controllable transconductances and the propose EOTA

Transconductor	[4.16]	[4.17]	[4.18]	proposed EOTA
Technology	2μm MOSIS	0.8μm CMOS CXQ	5μm CMOS	2μm MOSIS
Controllable g_m	DC voltage	DC voltage	DC voltage	DC current
Controllable range	0.1-1V	1.2-1.4V	NA	10μA-1mA
Transconductance range	98-396μA/V	180-346μA/V	330μA/V	0.54-540μA/V
V_{supply}	5V	1.4V	± 5V	± 3V to ± 5V
V_{in}	-1.4 to 1.4V	± 1V	1.2V	± 1V (I_{BE}=1mA)
Bandwidth	50MHz	420MHz	20MHz	120MHz

This table shows that the proposed EOTA has some advantages over other proposed linearly controllable transconductances in [4.16], [4.17] and [4.18]. The EOTA has wider controllable range and wider transconductance range.

4.5 Conclusion

A design of electronically and linearly tunable CMOS OTA has been proposed. The EOTA circuit composed of three balanced CMOS OTAs which is suitable for implementing in CMOS integrated form. The achieve characteristics of the proposed circuit were similar as the bipolar OTA that the transconductance gain (g_m) can be linearly tuned by the DC bias current. Simulation results have been employed to demonstrate the performances of the proposed EOTA. Moreover to confirm that EOTA can be replacing the bipolar OTA, the current-mode multiplier circuit, and both of current-controlled and voltage controlled current amplifier current amplifier were used to display the performances of the proposed circuit.

CHAPTER 5

Conclusions

In this thesis, the simple integrable analog integrated circuit building blocks: a Simple Integrable CMOS True RMS-to-DC Converter and an electronically and linearly tunable CMOS OTA (EOTA) were designed. These design techniques are suitable for integrated in CMOS technology. The performances of the proposed circuits are verified through the PSPICE simulation and the experimentation.

5.1 Main achievements and contribution

A simple integrable CMOS true RMS-to-DC converter is presented in chapter 3. The implicit computation method was used in order to design the simple CMOS True RMS-to-DC Converter. This method can achieve great accuracy, wide bandwidth, high input swing, and low cost. The circuit can be operated from a single supply. The device draws less than 0.1mW for the supply voltage of 5 volts. The circuit has been developed based on the characteristic of a CMOS squaring circuit, where all the transistors are biased in the saturation region. This proposed true RMS-to-DC converter accept complex input waveforms containing AC and DC component. The characteristics of the proposed RMS-to-DC converter are studied through the use of discrete CMOS complementary pairs CD4007 that implemented on bread-board. The transient response, DC transfer characteristic and the error versus crest factor are experimentally tested. The high frequency response capability was not measured directly since the stray capacitances in the bread boarding circuit. Therefore, PSPICE simulation result is used to study the high frequency performance. The high frequency limitation of the proposed true RMS-to-DC converter is 100MHz for I_{in} =1.5mA. This result demonstrate that the frequency is limited by the finite bandwidth of the circuit structure which in this circuit is limited by the current mirror CM_5 [Appendix B].

In addition, to confirm that this proposed circuit is suitable for implementing in monolithic integrated form, the circuit is also layouted and fabricated based on 0.5 microns CMOS technology AMIS process. The chip performances are tested by the measurement setup. There chip performances are agree with the simulation results and the performances of the circuit

that implemented by CMOS complementary CD4007. The simulation and experimental results also agree with the theoretical prediction.

In chapter 4, an Electronically and Linearly Tunable CMOS OTA (EOTA) is presented. This circuit composes of three balanced CMOS OTAs. The realization technique is achieved by squaring the transconductance gain of the balanced CMOS OTA. This circuit is suitable for implementing in CMOS integrated form. The achieve characteristics of the transconductance gain (g_m) is dependent upon the bias current I_B over the range of 1μA to 1mA (three decades) with the conversion error from simulation result is about 0.68%. The EOTA can linearly convert the input voltage into output signal current with nonlinearity of less than 1% for the input voltage (V_{in}) in the ranges of -1V to 1V. The frequency response of the EOTA was also studied, where the -3dB bandwidth of about 120 MHz is achieved. However the circuit can be operated in a wider bandwidth by increasing the dc bias currents of the circuit.

The current-mode multiplier circuit, and both of current-controlled and voltage controlled current amplifier were used to display the performances and the advantage of the proposed EOTA. The current-mode multiplier circuit using the proposed EOTA can be function as a four-quadrant current multiplier which use only active circuit elements but not require external passive circuit elements. The simulation results can confirms that the circuit can accurately modulate two different input signal currents. The transfer characteristic demonstrated that the simulated and calculated data are agreed very well over the input range of ± 190μA with the error of less than 1%. The high frequency characteristic of the multiplier circuit is also studied. The simulated –3dB bandwidth of the current multiplier is about 71MHz. For the voltage-controlled current amplifier that designed based on the proposed EOTA, its current gain can be electronically and linearly tune by the control voltage V_C. The current gain can be tuned for the range of 0.1 to 1 times. In the case of the current-controlled current amplifier its current gain can be electronically and linearly tune for the range of 0.1 -20 times by the DC bias current.

In summary, the goal of this work is to design the new analog integrated circuit building blocks: A true RMS-to-DC converter and an electronically and linearly tunable OTA which suitable to implement in CMOS technology. Moreover some applications were used to demonstrate the design flexibility of the approaches. Although they have some disadvantages, however they can be improved on the future work.

5.2 Suggestions for future work

From this work, we can suggest for future work based on the experience and the knowledge acquired. We found that the performances of the proposed true RMS-to-DC converter and the EOTA that studied from the simulation and the experimental results still provide the error of about 10%. Due to the circuit structure of the proposed true RMS-to-DC converter and the proposed EOTA are composed of the basic current mirrors, the current mirror mismatch causes the DC off-set current which will effects to the accuracy of the circuits. For the proposed true RMS-to-DC converter that designed by feedback the output current (I_{RMS}) to be the DC bias current of the circuit, if the current mirrors have the DC off-set current the error of the output current will occur. For the proposed EOTA, the error of the circuit is also cause by the current mirror mismatch. From this result both circuit accuracy can be improve by using the topology that improve the current mirror, such as, the cascode current mirror.

Since the proposed circuits are designed based on square law characteristics that the MOS transistors are operated in saturation region, therefore to maintain the circuit that still operate in the linear range and low total harmonic distortion, the MOS transistors should be biased in saturation region.

For the proposed voltage-controlled current amplifier that designed and restricted by using the proposed EOTA, the gain current is not high due to the current gain, $A_i = 2K_T V_C$, which depend on the K_T where K_T is a small value. However, we can improve the current amplifier for higher gain by given the current gain ratio of the current mirrors of the balanced CMOS OTA much more than the unity. By the OTA schematic diagram in Fig.2.9, if we assume that the current mirrors M_3-M_4, M_5-M_6 and M_7-M_8 have current gain ratios equal to *1*: *n*, *1*: *n* and *n* : *n*, respectively. The current gain of the voltage–controlled current amplifier can be obtained by $A_i = 2nK_T V_C$. We can found that if we set *n* much more that unity, the current gain can be tuned for the wide range.

Moreover the proposed EOTA should be developed by designing a new transconductance cell for reducing the number of transistors that will be reduces the power consumption of both proposed circuits and that wider signal dynamic range may be possible at the low power supply voltage.

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APPENDIX A

Large signal analysis of the squaring circuit [32]

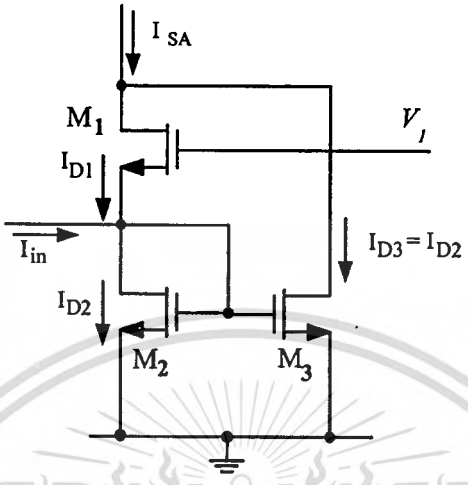


Fig. 1A The current squaring circuit

Consider two matched MOS transistors which include the effect of channel-length modulation (λ), operating in saturation and characterized to first order by

$$I_{D1} = \frac{\mu_n C_{ox} W}{2L}(V_{GS1} - V_{T1})^2 (1 + \lambda V_{DS1}) \tag{A.1}$$

$$I_{D2} = \frac{\mu_n C_{ox} W}{2L}(V_{GS2} - V_{T2})^2 (1 + \lambda V_{DS2}) \tag{A.2}$$

By copying of I_{D2} via transistor M_3 and adding it to current I_{D1}, the sum current $I_{D1} + I_{D3}$ is available as output current I_{SA} of squaring part

$$I_{SA} = I_{D1} + I_{D3} \tag{A.3}$$

From the unity gain current mirror CM_1, I_{D3} can be expressed in the function of I_{D2} as

$$I_{D3} = \frac{(W/L)_3}{(W/L)_2}\left(\frac{V_{GS3} - V_{T3}}{V_{GS2} - V_{T2}}\right)^2 \cdot \frac{1 + \lambda V_{DS3}}{1 + \lambda V_{DS2}} \cdot \frac{\mu_{n3} C_{ox3}}{\mu_{n2} C_{ox2}} I_{D2} \tag{A.4}$$

If the effect of channel-length modulation can be neglected ($\lambda = 0$), assume the process parameters such as V_T, μ_n, C_{ox}, of MOS transistor are matched and $V_{DS2} \cong V_{DS1}$. The eqns. (A.1) and (A.2) can be rewritten as

$$I_{D1} = \frac{\mu_n C_{ox} W}{2L}\left(V_{GS1} - V_{T1}\right)^2 \tag{A.5}$$

$$I_{D2} = \frac{\mu_n C_{ox} W}{2L}\left(V_{GS2} - V_{T2}\right)^2 \tag{A.6}$$

$$V_{GS1} = V_1 - V_{GS2} \tag{A.7}$$

where V_1 is bias voltage at transistor M_1 , and V_{GS1}, V_{GS2} are the gate-source voltage of transistor M_1 and M_2 respectively.

Using simple algebra we may write for the output current difference

$$I_{D2} - I_{D1} = \frac{\mu_n C_{ox} W}{2L}\left(V_1 - 2V_T\right)\left(V_{GS2} - V_{GS1}\right) \tag{A.8}$$

With (A.3), (A.5) - (A.7), the sum of the output currents may be written as

$$I_{D2} + I_{D1} = \frac{1}{2}\frac{\mu_n C_{ox} W}{2L}\left(V_1 - 2V_T\right)^2 + \frac{\left(I_{D1} - I_{D2}\right)^2}{2\frac{\mu_n C_{ox} W}{2L}\left(V_1 - 2V_T\right)^2} \tag{A.5}$$

By copying of I_{D2} via transistor M_3 and adding it to current I_{D1} , the sum current $I_{D1} + I_{D3}$ is available as output current I_{SA} of squaring part

$$I_{SA} = I_{D1} + I_{D3} = I_{D1} + I_{D2} \tag{A.6}$$

From Fig. A1, the common node of M_1 and M_2 is now considering as input. The input current can be written as

$$I_{in} = I_{D2} - I_{D1} \tag{A.7}$$

Substitution of (A.7) and (A.6) in (A.5) yields

$$I_{SA} = \frac{1}{2}\frac{\mu_n C_{ox} W}{2L}(V_1 - 2V_T)^2 + \frac{I_{in}^2}{2\frac{\mu_n C_{ox} W}{2L}(V_1 - 2V_T)^2} \tag{A.8}$$

which describes a current squaring function. Using the bias circuit, formed by transistors M_4 and M_6 , to combination with the current squaring in Fig. A1 which shown in Fig. 2.8, a simpler expression is obtained

$$I_{SA} = 2I_b + \frac{I_{in}^2}{8I_b} \tag{A.9}$$

Biasing with a current has the additional advantage of making the transfer function (in first-order approximation) independent of process parameters and operating temperature.

From the current controlled biasing circuit (M_4 and M_6). We found that the relation between the control current I_b and the voltage V_1 is given by [2.15]

$$I_b = \frac{1}{4}K(V_2 - 2V_T) \tag{A.10}$$

where $K = \frac{\mu_n C_{ox} W}{2L}$

From equation (A.8), in order to remain a proper operation, the input current is restricted to the range

$$|I_{in}| < K(V_2 - 2V_T)^2 \tag{A.11}$$

or, if biased with the biasing circuit

$$|I_{in}| < 4I_b \tag{A.12}$$

APPENDIX B

Conversion error of the squaring circuit

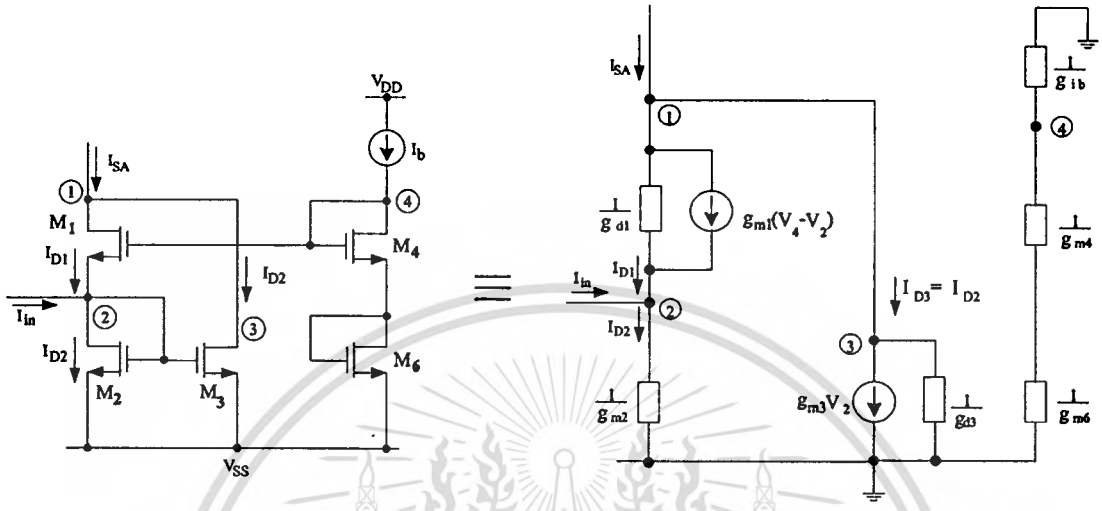


Fig. 1B Squaring circuit (a) Circuit diagram, (b) Small-signal equivalent circuit.

By using KCL analysis, transfer function of the input small signal current (i_{in}) and the output current (i_{SA}) of the squaring circuit in Fig. 1B can be expressed below.

From Fig. 1B(b) using KCL at node 2 , the equation is shown.

$$i_{in} + \left[g_{d1}\left(v_1 - v_2\right) + g_{m1}\left(v_4 - v_2\right) \right] = g_{m2} v_2 \qquad \text{(B.1)}$$

using KCL at node 1

$$i_{SA} = g_{d1}\left(v_1 - v_2\right) + g_{m1}\left(v_4 - v_2\right) + g_{m3} v_2 + g_{d3} v_3 \qquad \text{(B.2)}$$

If $g_m >> g_d$ from equations (B.1) and (B.2) the conversion of the input signal current I_{in} to the current I_{SA} from the squaring part can be approximately expressed as

$$\alpha = \frac{i_{SA}}{i_{in}} = \frac{1}{1 + \dfrac{g_{d1}(g_{m2} + g_{m3})}{g_{m1}g_{m3} + g_{m2}g_{m3} - g_{m1}^2 - g_{m1}g_{m2} - g_{m1}g_{d1} - g_{m2}g_{d1}}} \quad \text{(B.3)}$$

where g_{di} and g_{mi} denote the drain conductance and the conductance of the transistor M_i, respectively. The input current i_{in} will accurately convert to i_{SA} if $\alpha \approx 1$. The percentage conversion error of the squaring circuit can be written as

$$\frac{\delta\alpha}{\alpha} = \frac{g_{d1}(g_{m2} + g_{m3})}{g_{m1}g_{m3} + g_{m2}g_{m3} - g_{m1}^2 - g_{m1}g_{m2} - g_{m1}g_{d1} - g_{m2}g_{d1}} \times 100\% \quad \text{(B.4)}$$

APPENDIX C

Frequency response of true RMS to DC converter

Consider the frequency response of the true rms-to-dc converter. Because of the circuit is composed of the squaring circuit in combination with four current mirrors (CM_2 through CM_5). Thus we should pay attention on the frequency response of the squaring circuit and the current mirrors.

To verify the high frequency response, from the block diagram of Fig. 3.1, the transfer function of the proposed rms-to-dc converter circuit can be given by

$$\frac{i_{RMS}(s)}{i_{in}(s)} = \frac{i_{SA}(s)}{i_{in}(s)} \cdot \frac{i_{SQ}(s)}{i_{SA}(s)} \cdot \frac{i_{b1}(s)}{i_{SQ}(s)} \cdot \frac{i_{RMS}(s)}{i_{b1}(s)} \qquad \text{(C.1)}$$

The small signal equivalent circuit of the squaring circuit from and the positive current mirror CM4 and the negative current mirror CM3, can be represented in Fig. 1C (b), 2C (b) and 3C (b), respectively.

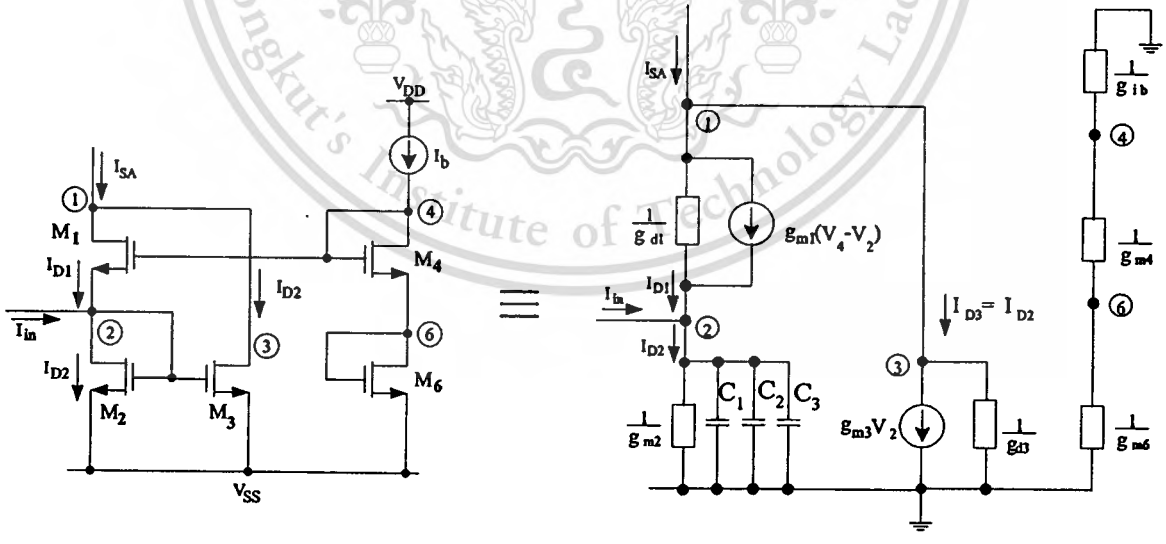


Fig. 1C Squaring circuit (a) Circuit diagram, (b) Small-signal equivalent circuit.

By using KCL analysis, transfer function of the input signal current (I_{in}) and the output current (I_{SA}) of the squaring circuit in Fig. 1C can be expressed below.

From Fig. 1C(b) using KCL at node 2 , the equation is shown.

$$i_{in}+\left[g_{d1}\left(v_1-v_2\right)+g_{m1}\left(v_4-v_2\right)\right]=\left[g_{m2}+s\left(C_1+C_2+C_3\right)\right]v_2 \quad \text{(C.2)}$$

using KCL at node 1

$$i_{SA}=g_{d1}\left(v_1-v_2\right)+g_{m1}\left(v_4-v_2\right)+g_{m3}v_2+g_{d3}v_3 \quad \text{(C.3)}$$

If $g_m >> g_d$ from equations (C.2) and (C.3) the transfer function $i_{SA}(s)/i_{in}(s)$ of the squaring circuit in Fig.1C can be approximately expressed as

$$\frac{i_{SA}(s)}{i_{in}(s)}=\frac{\dfrac{g_{m3}-g_{m1}}{\left(C_1+C_2+C_3\right)}}{\left(s+\dfrac{g_{m1}+g_{m2}}{\left(C_1+C_2+C_3\right)}\right)} \quad \text{(C.4)}$$

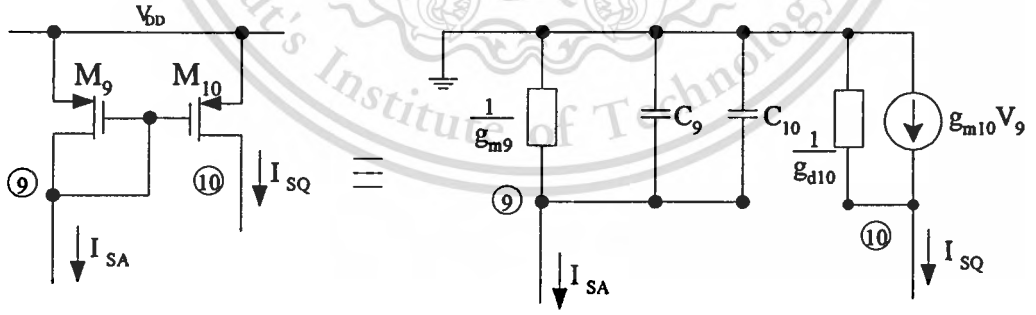


Fig. 2C Current mirror (CM4) (a) Circuit diagram, (b) Small-signal equivalent circuit.

From Fig. 2C , using KCL at node 9, the equation can be shown.

$$\left[g_{m9}+s\left(C_9+C_{10}\right)\right]v_9=-i_{SA} \quad \text{(C.5)}$$

using KCL at node 10,

$$-i_{SQ} = g_{m10}v_9 + g_{d10}v_{10} \tag{C.6}$$

If $g_m >> g_d$ from equations (C.5) and (C.6) the transfer function $i_{SQ}(s)/i_{SA}(s)$ of the current mirror (CM4) in Fig. 2C can be expressed as

$$\frac{i_{SQ}(s)}{i_{SA}(s)} = \frac{g_{m10}/g_{m9}}{\left(1 + s\dfrac{C_9 + C_{10}}{g_{m9}}\right)} \tag{C.7}$$

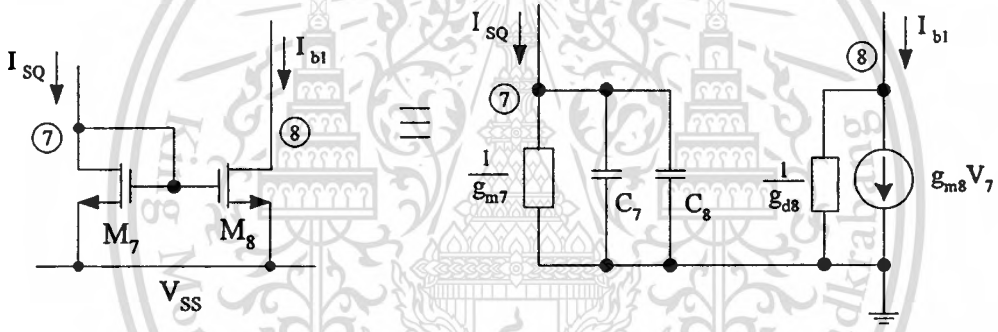


Fig. 3C Current mirror (CM3) (a) Circuit diagram, (b) Small-signal equivalent circuit.

From Fig. 3C, using KCL at node 7, the equation can be shown.

$$\left[g_{m7} + s(C_7 + C_8)\right]v_7 = i_{SQ} \tag{C.8}$$

using KCL at node 8,

$$i_{b1} = g_{m8}v_7 + g_{d8}v_8 \tag{C.9}$$

If $g_m >> g_d$ from equations (C.8) and (C.9) the transfer function $i_{b1}(s)/i_{SQ}(s)$ of the current mirror (CM3) in Fig. 3C can be expressed as

$$\frac{i_{b1}(s)}{i_{SQ}(s)} = \frac{g_{m8}/g_{m7}}{\left(1+s\dfrac{C_7+C_8}{g_{m7}}\right)} \qquad \text{(C.10)}$$

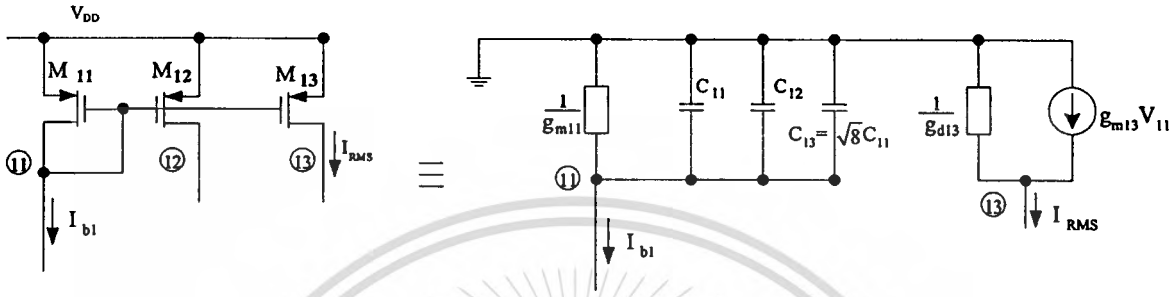


Fig. 4C Current mirror (CM_5) (a) Circuit diagram, (b) Small-signal equivalent circuit.

From Fig. 4C , using KCL at node 11, the equation can be shown.

$$\left[g_{m11}+s\left(C_{11}+C_{12}+C_{13}\right)\right]v_{11} = i_{b1} \qquad \text{(C.11)}$$

using KCL at node 13,

$$i_{RMS} = g_{m13}v_{11} + g_{d13}v_{13} \qquad \text{(C.12)}$$

If $g_m >> g_d$ from equations (C.11) and (C.12) the transfer function $i_{b1}(s)/i_{SQ}(s)$ of the current mirror (CM5) in Fig. 4C can be expressed as

$$\frac{i_{RMS}(s)}{i_{b1}(s)} = \frac{g_{m13}/g_{m11}}{\left(1+s\dfrac{C_{11}+C_{12}+C_{13}}{g_{m11}}\right)} \qquad \text{(C.13)}$$

By a small signal analysis of the proposed true RMS-to-DC converter, the transfer function of the circuit can be approximated as

$$\frac{i_{RMS}(s)}{i_{in}(s)} = \frac{(g_{m3}-g_{m1})/(g_{m1}+g_{m2})}{\left(1+s\dfrac{C_1+C_2+C_3}{g_{m1}+g_{m2}}\right)} \cdot \frac{g_{m10}/g_{m9}}{\left(1+s\dfrac{C_9+C_{10}}{g_{m9}}\right)} \cdot \frac{g_{m8}/g_{m7}}{\left(1+s\dfrac{C_7+C_8}{g_{m7}}\right)} \cdot \frac{g_{m13}/g_{m11}}{\left(1+s\dfrac{C_{11}+C_{12}+C_{13}}{g_{m11}}\right)} \quad \text{(C.14)}$$

Let p_1 denotes the pole of the squaring circuit, p_2 is the pole of the current mirror CM4, p_3 is the pole of the lowpass filter, and p_4 is the pole of the current mirror CM_5. Then from eqn. (C.14), the poles p_1, p_2, p_3 and p_4 can be respectively expressed as

$$p_1 = -\frac{g_{m1}+g_{m2}}{C_1+C_2+C_3} \quad \text{(C.15)}$$

$$p_2 = -\frac{g_{m9}}{C_9+C_{10}} \quad \text{(C.16)}$$

$$p_3 = -\frac{g_{m7}}{C_7+C_8} \quad \text{(C.17)}$$

$$p_4 = -\frac{g_{m11}}{C_{11}+C_{12}+C_{13}} \quad \text{(C.18)}$$

High frequency limitation is due to the pole p_4 that associated with the PMOS current mirror (CM_5). The cut-off frequency of the rms-to-dc converter can be given by

$$f_{-3dB} = \frac{(g_{m11})}{2\pi(C_{11}+C_{12}+C_{13})} \quad \text{(C.19)}$$

APPENDIX D

Error Analysis of the RMS value

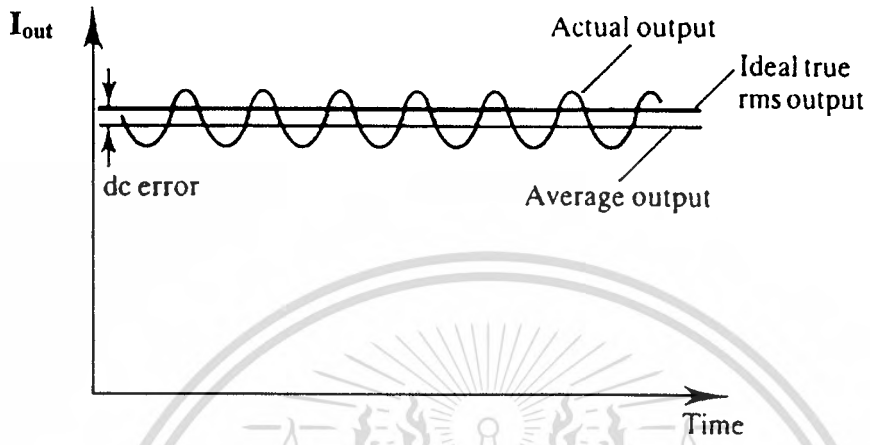


Fig. 1D Output waveform for sinusoidal input current

Since the RMS current value (I_{RMS}) is expressed as

$$I_{RMS} = \sqrt{\frac{1}{\tau}\int_0^{\tau} I_{in}^2 dt} \tag{D.1}$$

From equation C.1 the transfer function of the true RMS-to-DC converter can be written as

$$I_{out}^2(s) = \frac{I_{in}^2(s)}{(1+s\tau)} \tag{D.2}$$

where τ is equal to RC. Suppose that the input current is given by

$$I_{in} = \sqrt{2} I_{RMS} \cos(\omega t) \tag{D.3}$$

where I_{RMS} is the RMS value of the sinusoidal input signal of angular frequency ω. The output current as a function of the input frequency is

$$I_{out}(t) = \sqrt{I_{RMS}\left(1 + \frac{\cos(2\omega t)}{\sqrt{1+4\omega^2\tau^2}}\right)} \tag{D.4}$$

Using a simple trigonometric and Taylor series approximation and by assuming that the frequency of input current is greater than the inverse of the averaging time constant τ (or $f > 1/\tau$), I_{out}(t) of equation (D.4) can be given by

$$I_{out}(t) = I_{RMS}\left[1 - \frac{1}{16(1+4\omega^2\tau^2)} + \frac{I_{RMS}\cos(2\omega t)}{2\sqrt{1+4\omega^2\tau^2}}\right] \tag{D.5}$$

From this it is seen that there is both a dc error and an ac error in the output. The dc error e_{odc} can by expressed as

$$e_{odc} = \frac{I_{RMS}}{2\left[1+4\omega^2\tau^2\right]}, \quad \omega > \frac{1}{\tau} \tag{D.6}$$

and from equation (D.6) the ac error in the output current, the output ripple e_{ripple}, is essentially

$$e_{ripple} = \frac{I_{RMS}\cos 2\omega t}{2\left[1+4\omega^2\tau^2\right]^{1/2}}, \quad \omega > \frac{1}{\tau} \tag{D.7}$$

since the fourth-harmonic ripple term is much less than the second-harmonic term with $\omega > 1/\tau$. The ripple error in the output can be reduced in many applications with a simple low-pass filter, but an error in the output dc level e_{odc} will still exist.

PUBLICATIONS OF THE THESIS

Full Papers;

1) Khanittha Kaewdang, K. Kumwachara and W. Surakampontorn, "A Simple Wide-Band CMOS based True RMS-to-DC Converter," **International Journal of Electronics**, vol. 91, no. 7, July 2004, pp. 407-420.

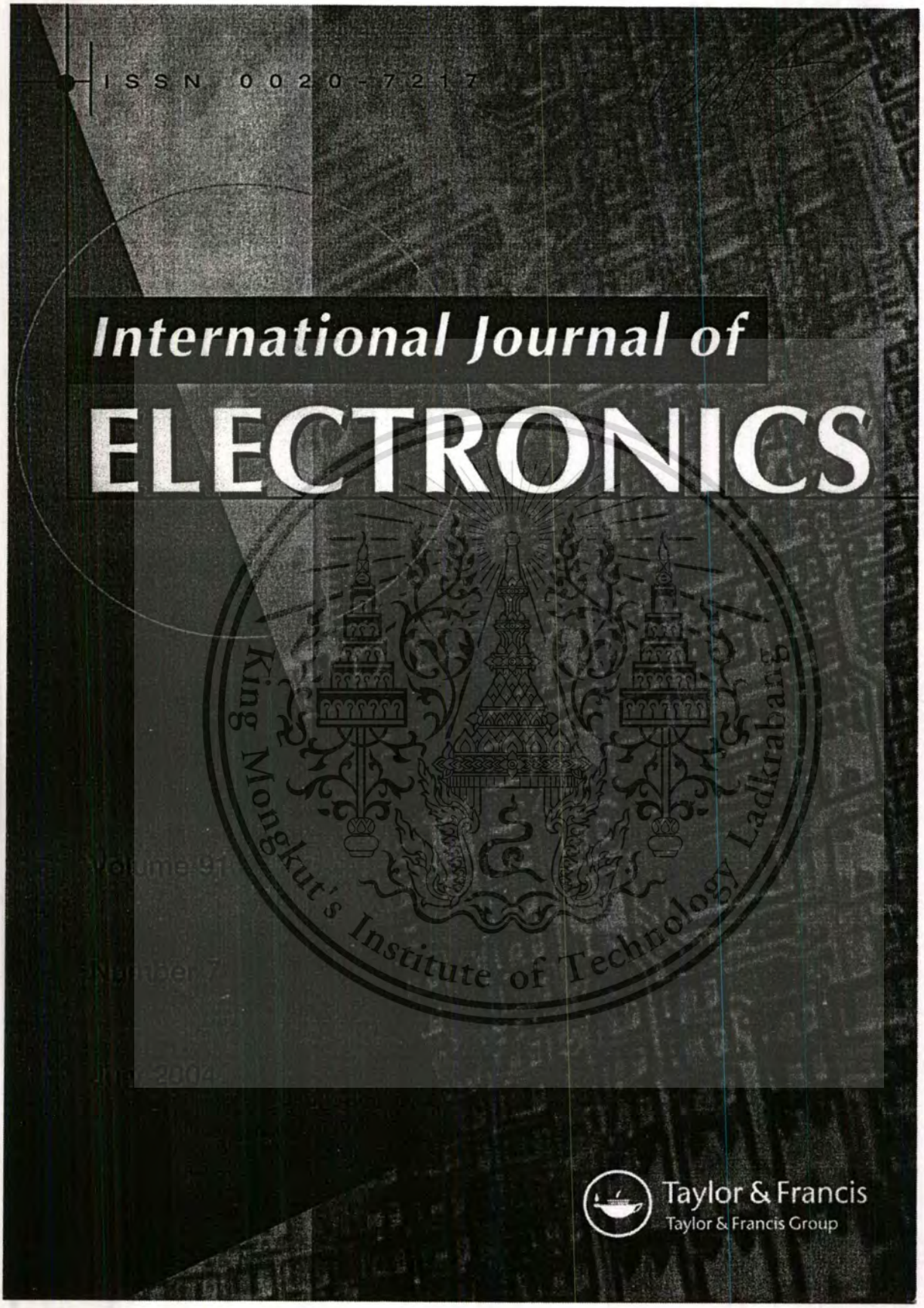
2) Khanittha Kaewdang and W. Surakampontorn, "On the realization of electronically current-tunable CMOS OTA," **International Journal of Electronics and Communications**, ARTICLE In Press, Corrected Proof, Available online 12 July 2006 (Accepted)

Conference papers;

1) Khanittha Kaewdang, Worapong Tangsrirat and Wanlop Surakampontorn, "An Electronically and Linearly Tunable CMOS OTA," **International Technical Conference on Circuits/Systems, Computers and Communications (ITC CSCC 2004)**, Sendai, Japan, 6-8 July 2004, pp. 6A3L-1-1 – 6A3L-1-4.

2) Khanittha Kaewdang, Wanlop Surakampontom and Nobuo Fujii, "A design of CMOS tunable current amplifiers," **IEEE International Symposium on Communications and Information Technology (ISCIT 2004)**, 2004, Sapporo, Japan, vol. 1, 26-29 Oct. 2004, pp.519 – 522.

3) Khanittha Kaewdang, Kiattisak Kumwachara and Wanlop Surakampontorn, "A realization of simple current-mode CMOS based true RMS-to-DC converter," **The 2004 IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS2004)**, 2004, Tainan, Taiwan, vol. 2, 6-9 Dec. 2004, pp.733 – 736.



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A simple wide-band CMOS based true rms-to-dc converter

KHANITTHA KAEWDANG†, KIATTISAK KUMWACHARA†
and WANLOP SURAKAMPONTORN†*

A simple integrable circuit technique for the realization of a wide bandwidth current-mode CMOS true rms-to-dc converter is proposed. The realization scheme is based on the implicit computation method that makes use of the characteristic of a CMOS squaring circuit, where the transistors are biased in their saturation regions. The conversion circuit consumes very low power due to the bias current of the circuit provided by the root-mean-square current I_{RMS}. The performance of the proposed circuit is studied through PSPICE simulation and experimental results.

1. Introduction

A true rms-to-dc converter is an important instrument that is used for measuring the average energy content in an electrical signal. This device found use in the fields of instrumentation, communication and display systems (Peyton and Walsh 1993). In the past, many true rms-to-dc converters based on bipolar integrated circuit technology were available (Seevinck *et al.* 1984, Wassenaar *et al.* 1988, Kalanko 1993). Their conversion schemes are mostly performed through the use of full-wave rectifiers and multiplier/divider circuits that employ a log–antilog principle. Due to the bandwidth and the slew-rate of the full-wave rectifiers, the useful frequency ranges of these converters are limited to less than 5 MHz. New design techniques based on bipolar dynamic translinear circuits have been proposed to implement true rms-to-dc converters (Mulder *et al.* 1996, 1997). Unfortunately, only circuit descriptions are outlined, but the characteristics of the rms-to-dc conversion circuits have not been reported. In addition, their circuits are operated in only one quadrant and also required full-wave rectifiers. Recently, a new design technique for a rms-to-dc converter that realizes around a dual translinear-base squarer circuit, where the input current can be a two-quadrant current, is proposed (Surakampontorn and Kumwachara 1999). The circuit exhibits a wide bandwidth because the full-wave rectifier is not required by this conversion scheme. However, the implementation scheme is rather complicated and only suitable for bipolar technology.

In this paper, through the use of a MOS transistor square law characteristic, a design technique for the realization of a true rms-to-dc converter is proposed. The conversion circuit performs the implicit computation scheme by feedback of the root-mean square current as the circuit bias current. A full-wave rectifier is not

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required by the proposed realization scheme. The conversion circuit is simple, suitable for implementing in monolithic integrated form, and can be readily integrated as part of a larger system. The performance of the conversion circuit is studied from PSPICE simulation and experimental results.

2. Circuit descriptions

2.1. *Squaring circuit*

Let us consider the schematic diagram shown in figure 1, where the operation of the circuit is based on the square law characteristic of MOS transistors biased in the strong inversion region (Bult and Wallenga 1987, Surakampontorn and Kumwachara 1999). Transistors M_1 through M_3 function as a current squarer, where M_4 and M_6 and the current source I_b are formed as the current-controlled bias circuit. The input signal current I_{in} is injected into point A. If I_{D1} and I_{D2} are the drain currents of transistors M_1 and M_2, respectively, the currents I_{D1} and I_{D2} can be respectively written as (Bult and Wallenga 1987, Landolt *et al.* 1992)

$$I_{D1} = \frac{(4I_b - I_{in})^2}{16I_b} \quad \text{for} \quad |I_{in}| \leq 4I_b \tag{1}$$

$$I_{D2} = \frac{(4I_b + I_{in})^2}{16I_b} \quad \text{for} \quad |I_{in}| \leq 4I_b. \tag{2}$$

The unity gain positive current mirror CM_1, formed by M_2 and M_3, reflects the current I_{D2} in order to add the current I_{D1}. Then, from (1) and (2), the summation of the currents I_{D1} and I_{D2} or $I_{SA} = I_{D1} + I_{D2}$ becomes

$$I_{SA} = \frac{I_{in}^2}{8I_b} + 2I_b. \tag{3}$$

We can see that I_{SA} consists of the signal current which is the squaring of the input signal I_{in} and the dc current $2I_b$. If the dc current $2I_b$ can be compensated, the circuit will function as a squarer/divider circuit, which can be used as a basic cell to realize the rms-to-dc converter by the implicit computation method (Lopez-Martin and Carlosena 2001).

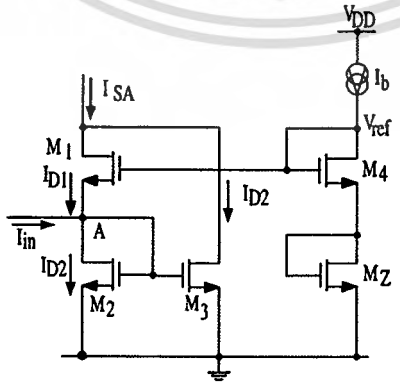

Figure 1. A CMOS current squaring circuit.

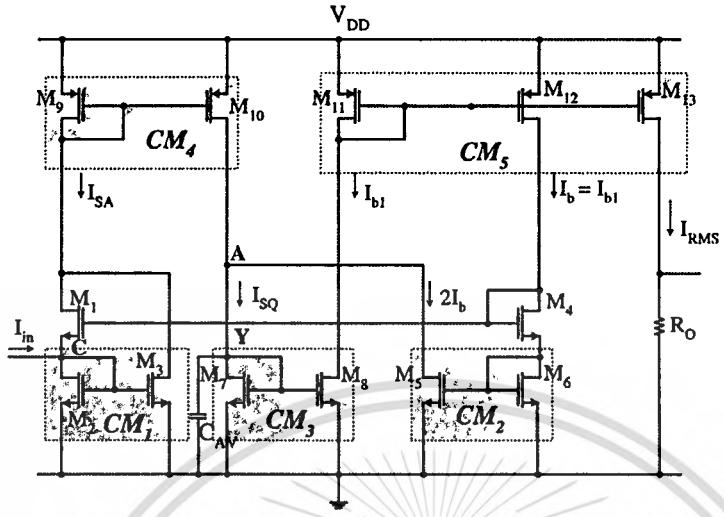

Figure 2. The proposed true rms-to-dc converter.

2.2. *The proposed true rms-to-dc converter*

Figure 2 shows the proposed true rms-to-dc converter, which is composed of the squaring circuit in figure 1 in combination with four current mirrors, CM_2 through CM_5. The circuit is constructed such that the drain current of the transistor M_5 of the current mirror CM_2 sources the current $2I_b$ from I_{SA}. Then from the (3) and figure 2, the current I_{SQ} can be expressed as

$$I_{SQ} = \frac{I_{in}^2}{8I_b}. \tag{4}$$

In the figure, the current I_{SQ} passes through the averaging circuit or the first-order current mode low-pass filter, which consist of the current mirror CM_3 (M_7 and M_8) and the grounded capacitor C_{AV} connected parallel to the mirror input (Pookaiyaudom *et al.* 1979). The output current of the filter I_{b1} can be written as

$$I_{b1} = \frac{1}{8I_b\tau}\int I_{in}^2\,dt \tag{5}$$

where $\tau = C_{AV}/g_{m7}$ is the time constant of the filter and g_{m7} is the transconductance of the transistor M_7. Due to the unity gain current mirrors CM_3 (M_7 and M_8) and CM_5 (M_{11} and M_{12}), the bias current I_b is derived by the current I_{b1} such that

$$I_b = I_{b1}. \tag{6}$$

At the output, since we set the transistor channel widths of the current mirror CM_5 as $W_{13} = \sqrt{8}W_{11}$, this means the output current

$$I_{RMS} = \sqrt{8}I_b. \tag{7}$$

From (5), since $I_b = I_{b1}$, by solving for I_b, we can write

$$I_b = \frac{1}{\sqrt{8}}\sqrt{\frac{1}{\tau}\int I_{in}^2\,dt}. \tag{8}$$

Then from (7) and (8), by solving for I_{RMS}, we get

$$I_{RMS} = \sqrt{\frac{1}{\tau}\int I_{in}^2 \, dt}. \tag{9}$$

We can see that the output current I_{RMS} is in the form of the root-mean-square value. It should be noted from (4)–(9) that the square root function is achieved by the feedback of the current I_{b1} to be the bias current I_b of the circuit.

In order that the proposed rms-to-dc converter gives a good performance in the required frequency range, the value of the capacitor C_{AV} must be chosen such that (Wang 1990 a)

$$C_{AV} \gg g_{m7(MAX)}/4\pi f_{(MIN)} \tag{10}$$

where $f_{(MIN)}$ is the lower end of the frequency range of interest and

$$g_{m7}(MAX) = \sqrt{2K_p I_{SQ} W_7/L_7} \tag{11}$$

where W_7 is the channel width and L_7 is the channel length of the transistor M_7. From (4), the $g_{m7(MAX)}$ can be expressed as

$$g_{m7}(MAX) = \sqrt{2K_p I_M^2 W_7/8I_b L_7} \tag{12}$$

where I_M is the peak amplitude of the input signal I_{in} and I_b is the circuit bias current. For example, for $K_P = 25.035 \times 10^{-6}$ A/V^{-2} and $W_7/L_7 = 20$, then $g_{m7(MAX)}$ can be given by

$$g_{m7(MAX)} = 0.0316\sqrt{(I_M^2/8I_b)}. \tag{13}$$

In this case, C_{AV} must be chosen such that

$$C_{AV} \gg (8.891 \times 10^{-4}) I_M/\sqrt{I_b} f_{(MIN)}. \tag{14}$$

It should be noted that the value of C_{AV} chosen is largely dependent on the ripple error that can be tolerated at the output. As a rule of thumb, the value of C_{AV} should exceed the right-hand term of (14) by the inverse of the fractional ripple error. For instance, for a 1% ripple error, C_{AV} should be about 1/0.01 or 100 times as large as the right-hand term. For example, if a sinusoidal input signal with $I_M = 1$ mA, $f_{(MIN)} = 100$ Hz, and the ripple error of 5%, then the averaging capacitance of $C_{AV} = 10\,\mu$F must be chosen.

2.3. *Circuit performance*

The ideal circuit performance has been discussed so far based on the assumptions that the current mirrors have unity gain, transistors are perfectly matched, and each transistor is operated in its saturated regions and obeys a square law model. However, in practical realization, the finite values of transistors g_m and g_d and transistor mismatch will contribute to deviation from the ideal performance. In the following, the transistor equivalent circuit and a small signal analysis will be used to study the performances of the conversion circuit of figure 2.

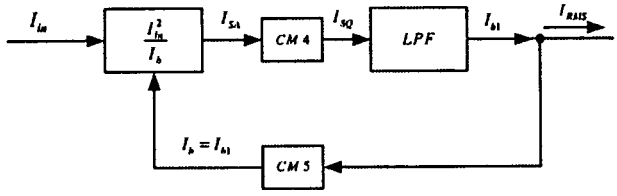

Figure 3. Block diagram representation of the true rms-to-dc converter.

2.3.1. Conversion Errors. Usually, for the rms-to-dc converter through the implicit computation method, the circuit implements the root-mean-square function by performing two non-linear processes: squaring and square rooting. However, in this implementation, the squaring is the core circuit and the square rooting function is achieved through feedback. The rms-to-dc converter of figure 2 can be represented by the block diagram as shown in figure 3. It is composed of the squarer/divider block, I_{in}^2/I_b, in combination with the current mirrors CM_4 and CM_5 and the lowpass filter (LPF). From (4)–(9), we can see that the implicit computation is achieved by the feedback of the current I_{RMS} to the I_{in}^2/I_b block by setting $I_b = I_{RMS}/\sqrt{8}$, where I_b is the transistor bias current. Then the accuracy of the rms-to-dc conversion will depend on the imperfection of the squaring and the current mirrors circuits.

The conversion of the input signal current I_{in} to the current I_{SA} from the squaring part can be approximately expressed as

$$\alpha = \frac{I_{SA}}{I_{in}} = \frac{1}{1 + [g_{d1}(g_{m2} + g_{m3})/(g_{m1}g_{m3} + g_{m2}g_{m3} - g_{m1}^2 - g_{m1}g_{m2} - g_{m1}g_{d1} - g_{m2}g_{d1})]} \tag{15}$$

where g_{di} and g_{mi} denote the drain conductance and the conductance of the transistor M_i, respectively. The input current I_{in} will accurately convert to I_{SA} if $\alpha \approx 1$. The percentage conversion error of the squaring circuit can be written as

$$\frac{\delta\alpha}{\alpha} = \frac{g_{d1}(g_{m2} + g_{m3})}{g_{m1}g_{m3} + g_{m2}g_{m3} - g_{m1}^2 - g_{m1}g_{m2} - g_{m1}g_{d1} - g_{m2}g_{d1}} \times 100\% \tag{16}$$

For example, if $g_{m1} = 4.80 \times 10^{-4}\,AV^{-1}$, $g_{m2} = 4.44 \times 10^{-4}\,AV^{-1}$, $g_{m3} = 5.39 \times 10^{-4}\,AV^{-1}$ and $g_{d1} = 3.26 \times 10^{-6}\,AV^{-1}$, the resulting conversion error is equal to 0.322%. It should be noted from (16) that the conversion error depends on drain conductance (g_d) of transistors, where $g_d \approx \lambda I_D$ and λ is the channel length modulation parameter. We can further reduce this error by decreasing the transistor drain current I_D. In addition, if long channel transistors are used, we can neglect the channel length modulation effect (Mehrvarz and Kwok 1996).

The current reflection errors ε_{pos} and ε_{neg} associated with the positive and negative current mirrors, respectively, can be approximately given by (Wang 1990 b)

$$\varepsilon_{pos} = \left(\frac{I_{out}}{I_{in}}\right)_{CMpos} - 1 = \left(\frac{L_7 W_8}{W_7 L_8}\right)_{NMOS} \left(\frac{1 + \lambda V_{DS8}}{1 + \lambda V_{DS7}}\right)_{NMOS} - 1 \tag{17a}$$

$$\varepsilon_{neg} = \left(\frac{I_{out}}{I_{in}}\right)_{CMneg} - 1 = \left(\frac{L_9 W_{10}}{W_9 L_{10}}\right)_{PMOS} \left(\frac{1 + \lambda V_{DS10}}{1 + \lambda V_{DS9}}\right)_{PMOS} - 1 \tag{17b}$$

where V_{DS} is drain-source voltage. For example, if $W_7 = W_8 = W_9 = W_{10} = 100\,\mu m$, $L_7 = L_8 = L_9 = L_{10} = 5\,\mu m$, $\lambda = 0.01\,V^{-1}$, $V_{DS7} = 2.72\,V$, $V_{DS8} = 4.94\,V$, $V_{DS9} = -2.76\,V$, and $V_{DS10} = -4.99\,V$, these errors (ε_{pos} and ε_{neg}) will be approximately less than 2.17%. Note from the (17*a*) and (17*b*) that the accuracy of the current mirror also depends on the channel length modulation. In order to reduce the influence of the channel length modulation, cascode current mirrors should be used.

2.3.2. Frequency response. To verify the high frequency response, from the block diagram of figure 3, the transfer function of the proposed rms-to-dc converter circuit can be given by

$$\frac{I_{RMS}(s)}{I_{in}(s)} = \frac{I_{SA}(s)}{I_{in}(s)} \cdot \frac{I_{SQ}(s)}{I_{SA}(s)} \cdot \frac{I_{b1}(s)}{I_{SQ}(s)} \cdot \frac{I_{RMS}(s)}{I_{b1}(s)}. \tag{18}$$

By a small signal analysis of figure 2, the transfer function of the circuit can be approximated as

$$\frac{I_{RMS}(s)}{I_{in}(s)} = \frac{(g_{m3} - g_{m1})/(g_{m1} + g_{m2})}{(1 + (s(C_1 + C_2 + C_3)/(g_{m1} + g_{m2})))} \frac{g_{m10}/g_{m9}}{(1 + (s(C_9 + C_{10})/g_{m9}))} \times \frac{g_{m8}/g_{m7}}{(1 + (s(C_7 + C_8)/g_{m7}))} \frac{g_{m13}/g_{m11}}{(1 + (s(C_{11} + C_{12} + C_{13})/g_{m11}))}. \tag{19}$$

Let p_1 denotes the pole of the squaring circuit, p_2 the pole of the current mirror CM_4, p_3 the pole of the lowpass filter, and p_4 the pole of the current mirror CM_5. Then from (19), the poles p_1, p_2, p_3 and p_4 can be respectively expressed as

$$p_1 = -\frac{g_{m1} + g_{m2}}{C_1 + C_2 + C_3} \tag{20}$$

$$p_2 = -\frac{g_{m9}}{C_9 + C_{10}} \tag{21}$$

$$p_3 = -\frac{g_{m7}}{C_7 + C_8} \tag{22}$$

$$p_4 = -\frac{g_{m11}}{C_{11} + C_{12} + C_{13}}. \tag{23}$$

If $I_{in} = 1\,mA$, $g_{m1} = 4.80 \times 10^{-4}\,AV^{-1}$, $g_{m2} = 4.44 \times 10^{-4}\,AV^{-1}$, $g_{m9} = 3.31 \times 10^{-4}\,AV^{-1}$, $g_{m7} = 4.27 \times 10^{-4}\,AV^{-1}$, $g_{m11} = 3.31 \times 10^{-4}\,AV^{-1}$, $C_1 = C_2 = C_3 = C_7 = C_8 = 1.21 \times 10^{-13}\,F$, $C_9 = C_{10} = C_{11} = C_{12} = 1.15 \times 10^{-13}\,F$, and $C_{13} = 3.26 \times 10^{-13}\,F$, where $C_i = Cgs_i$ and Cgs_i is the gate-to-source capacitance of transistor M_i. Then the cut-off frequencies of the poles p_1, p_2, p_3 and p_4 are approximately located at 405 MHz, 229 MHz, 281 MHz and 95 MHz, respectively. We can see that the high frequency limitation is due to the pole p_4 that associated with the PMOS current mirror (CM_5). The cut-off frequency of the rms-to-dc converter can be given by

$$f_{-3dB} = \frac{(g_{m11})}{2\pi(C_{11} + C_{12} + C_{13})}. \tag{24}$$

It should be noted that g_{m1}, g_{m2}, g_{m7}, g_{m9} and g_{m11} are varied in direct proportion to the input current I_{in}, since $g_m = \sqrt{2K_p(W/L)I_D}$ and $I_D = I_{RMS}/\sqrt{8} \cong 0.707 I_{in(peak)}$. Therefore, the cut-off frequency of the rms-to-dc converter is also increased if I_{in} increases, and vice versa. For example, using the same data above, for

$I_{in} = 1\,mA_{(peak)}$ the cut-off frequency of the rms-to-dc converter circuit is about 95 MHz and for $I_{in} = 500\,\mu A_{(peak)}$ the cut-off frequency of the rms-to-dc converter circuit is about 66 MHz.

2.3.3. DC and ripple errors. In practice, apart from the current I_{RMS}, there are also a low-frequency ripple and a dc error that presents at the output port of the circuit, which depend on the value of the capacitor C_{AV} and the frequency of the input current I_{in}. These errors can be computed by expressing the relationship of the currents I_{RMS} and I_{in} in the form of transfer function, where the current I_{in} is an input sine wave of the form $I_{in} = \sqrt{2} I_{RMS} \sin(\omega t)$. Using a simple trigonometric and Taylor series approximation and by assuming that the frequency of input current is greater than the inverse of the averaging time constant τ (or $f > 1/\tau$), the output ripple e_{ripple} and the dc error e_{odc} can be expressed in terms of I_{RMS} as (Wong and Ott 1976)

$$e_{ripple} = \frac{I_{RMS} \cos 2\omega t}{2\sqrt{1 + 4\omega^2 \tau^2}} \tag{25}$$

and

$$e_{odc} = \frac{I_{RMS}}{16(1 + 4\omega^2 \tau^2)} \tag{26}$$

where only the ripple that is due to the second-harmonic term is expressed. The ripple error in the output can be reduced in many applications with a simple low-pass filter. Equations (25) and (26) showing that the ripple error e_{ripple} and dc error e_{odc} decrease with increasing AC input frequency.

3. Simulation and experimental results

The performance of the circuit has been studied through simulation and experimental results. The simulation has been carried out by employing the PSPICE analogue simulation program, using the CMOS CD4007 transistor parameters that were extracted by the use of the method in Vladimirescu and Liu (1980) and Antogenetti and Massobrio (1988). The transistor parameters are listed in table 1 and the transistor dimensions are listed in table 2.

In order to test the performance of the circuit, the true rms-to-dc converter of the figure 2 was also constructed on a prototype board. All MOS devices used were in the form of complementary MOS pairs (CD4007). The transistors that required close matching, especially M_1, M_2 and M_3 and the current mirrors were contained in the same array package. The supply voltage was set to $V_{dd} = 15$ V. The capacitor C_{AV} is 10 μF for $f_{MIN} = 100$ Hz. Due to the proposed rms-to-dc converter operates in

model NM	NMOS (Level = 2 Vto = 1.5 Gamma = 1.4 Lambda = 0.01
+	Mj = 0.5 Rsh = 25 Uo = 580 Af = 1.2 Kf = 1E-26 Mjsw = 0.3 Cgbo = 200E-12
+	Cgso = 350E-12 Cgdo = 350E-12 Cj = 300E-6 Cjsw = 500E-12 Ld = 0.4u Tox = 80n)
model PM	PMOS (Level = 2 Vto = -1.2 Gamma = 0.4 Lambda = 0.01
+	Mj = 0.5 Rsh = 90 Uo = 230 Af = 1.2 Kf = 1E-26 Mjsw = 0.25 Cgbo = 200E-12
+	Cgso = 350E-12 Cgdo = 350E-12 Cj = 150E-6 Cjsw = 400E-12 Ld = 0.5u Tox = 80n)

Table 1. The model parameters of CMOS CD4007 used in the simulation.

Transistor	W (μm)	L (μm)
M_1, M_2, M_3, M_4, M_6, M_7, M_8	100	5
M_9, M_{10}, M_{11}, M_{12}	100	5
M_5	200	5
M_{13}	283	5

Table 2. The aspect ratios of the transistors in figure 2.

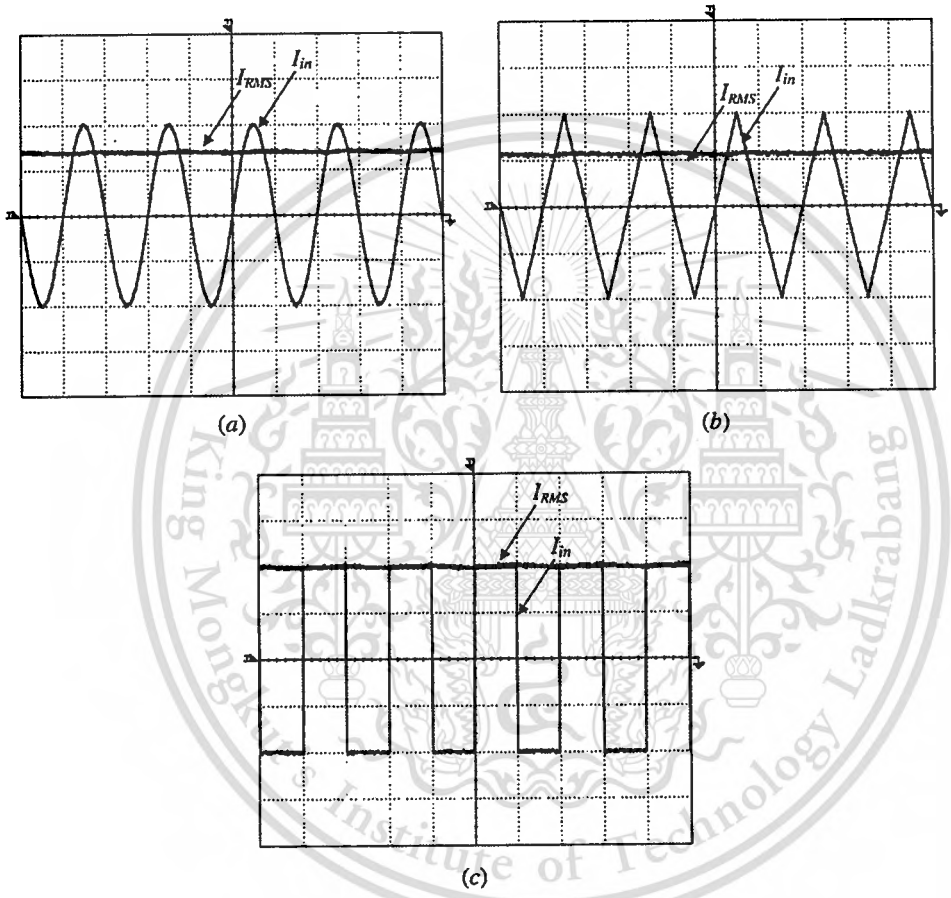

Figure 4. Experimental results for the input signals: (*a*) sinusoidal; (*b*) triangular; and (*c*) square wave (vertical scale: 0.5 V/div. horizontal scale: 0.5 ms/div).

current mode, a commercially available current conveyor CCII01 (LTP Electronics Limited 1994) was used to convert the input voltage V_{in} into the input current signal I_{in}. The resistor $R_{in} = 1\,k\Omega$ is connected at port X and the input voltage was applied to the port Y of the CCII. For example, by setting the input signal current of $I_{in} = 1\,mA_{(peak)}$, the input voltage equal to 1 V is applied to port Y of the CCII. To measure the value of the I_{RMS}, a resistor of 1 kΩ was connected at the output of the rms-to-dc converter and the voltage across the resistor R_o is measured instead.

The experimental results in figure 4 (*a*)–(*c*) show the I_{RMS} for the input signals in the form of sinusoidal, triangular and square wave waveforms, respectively, with the

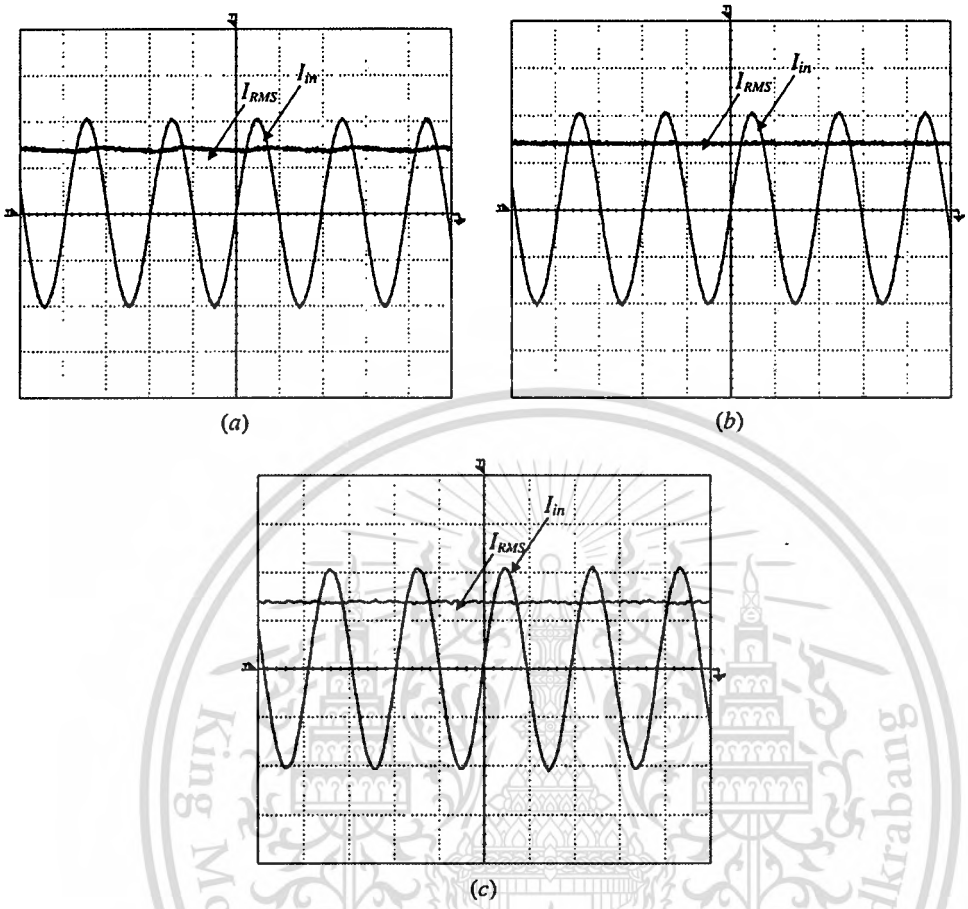

Figure 5. Experimental results of I_{RMS} with $I_{in}=1$ mA for: (*a*) $f=500$ Hz (vertical scale: 0.5 V/div, horizontal scale: 1 ms/div); (*b*) $f=5$ kHz (vertical scale: 0.5 V/div, horizontal scale: 100 μs/div); and (*c*) $f=5$ MHz (vertical scale: 0.5 V/div, horizontal scale: 100 ns/div).

peak amplitude of 1 mA and with the frequency of 1 kHz. With the error less than 10 μA, the I_{RMS} signal with the amplitudes close to 0.7 mA, 0.5 mA and 1 mA, respectively, were achieved. These results demonstrated that the circuit can convert the ac signals into the corresponding dc signals with accurate rms values. To demonstrate that the circuit can operate in a wide frequency range, figure 5 (*a*)–(*c*) show the measured I_{RMS} for the cases of the sinusoidal input signal with the frequencies of $f=500$ Hz, 5 kHz and 5 MHz, respectively, and with the peak amplitude of 1 mA. The results show that the I_{RMS} signals with the amplitude of about 0.7 mA are achieved. The dc errors from the simulation results are about 11%, 0.2% and 0.1%, respectively. We found that these results agree with the dc error predicted from (26), where the dc error decrease with increasing ac input frequency ($\omega \gg 1/\tau$).

From figure 5 (*a*)–(*c*), we notice that the output ripple for the input signal at low frequencies, i.e. $f=500$ Hz, is higher than the case of the input signals with higher frequency. This is due to that, in this case, the capacitor C_{AV} is selected for $f_{MIN}=100$ Hz. We will further study this effect through the simulation result because

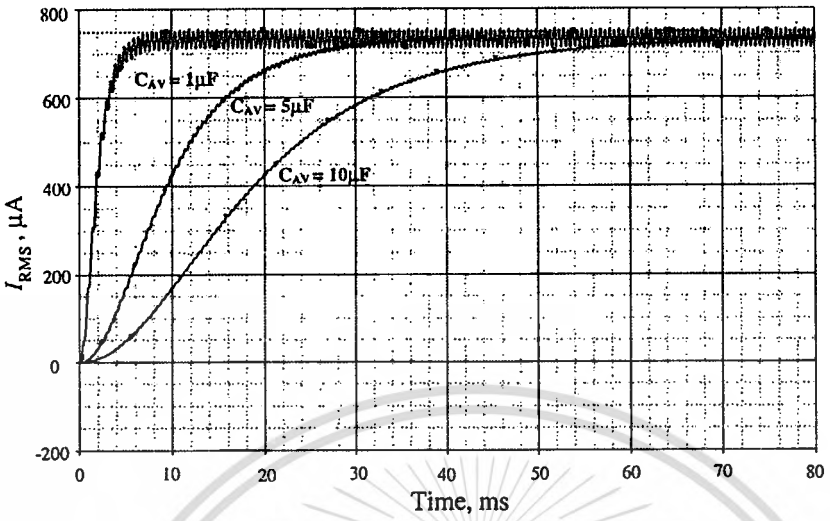

Figure 6. The I_{RMS} that simulated for 3 difference values of the capacitor C_{AV}.

the ripple cannot be measured accurately from the experimental results. Usually, the percent ripple is calculated by

$$\text{percent ripple} = (I_{\text{ripple (p-p)}}/I_{DC}) \times 100\% \tag{27}$$

where $I_{\text{ripple(p-p)}}$ is the peak to peak amplitude of the output current and I_{DC} is the dc component of the output current. From the simulation results at $f = 500$ Hz, 5 kHz and 5 MHz, the output signals have percent ripple errors of about 1.1%, 0.13% and 0.0001%, respectively. On the other hand, according to (10), since the averaging capacitor is selected 20 times greater than the predicted value ($C_{AV} = 10\,\mu$F) and for $I_M = 1$ mA, the calculated output percent ripple is about 1% at $f = 500$ Hz. This agrees with the simulation results above. Figure 6 shows the simulated results of the I_{RMS} for three difference values of the capacitor C_{AV}, i.e. 1 μF, 5 μF and 10 μF, when the input is a sinusoidal waveform with the peak amplitude of 1 mA and the frequency $f = 1$ kHz. The results show that the circuit will provide the I_{RMS} with lower ripple if a larger capacitor is used, but, however, it will result in a longer settling time.

The experimental results that demonstrate the linearity of the rms-to-dc converter are shown in figure 7. The transfer characteristics are the plots of the I_{RMS} against the input signal current I_{in} with the peak amplitude varied from 300 μA to 1.5 mA, for the sine, triangular and square waveforms. The signal frequencies are 1 kHz and $C_{AV} = 10\,\mu$F. We found that the maximum conversion non-linearity of about 2% was achieved. It should be noted that the lower limit of the circuit is due to the fact that the I_{RMS} is feedback to the bias current I_b of the circuit. Therefore, through I_b, the I_{RMS} should be large enough to bias all the transistors in their saturation regions.

Due to the stray capacitances in the bread boarding circuit, the high frequency response capability was not measured directly. The high frequency performance was studied through PSPICE simulation. Figure 8 shows the simulated frequency response for difference values of the input current (I_{in}). The input signals are sine waves with the amplitude of 20%, 50% and 90% of the full-scale current

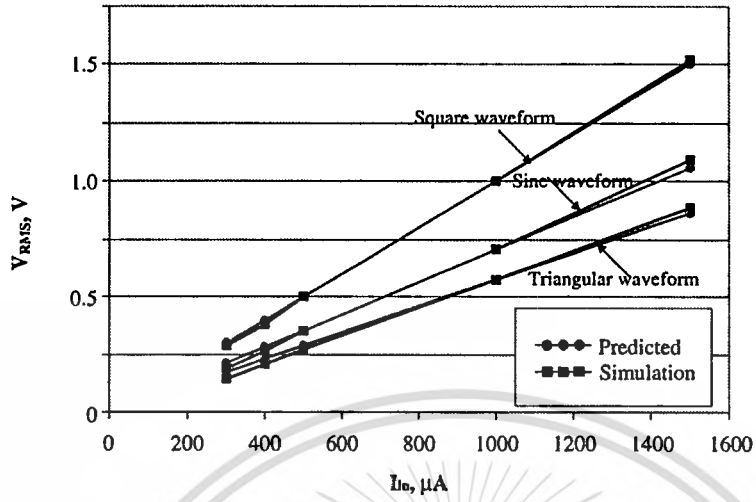

Figure 7. DC transfer curves of the rms-to-dc converter circuit.

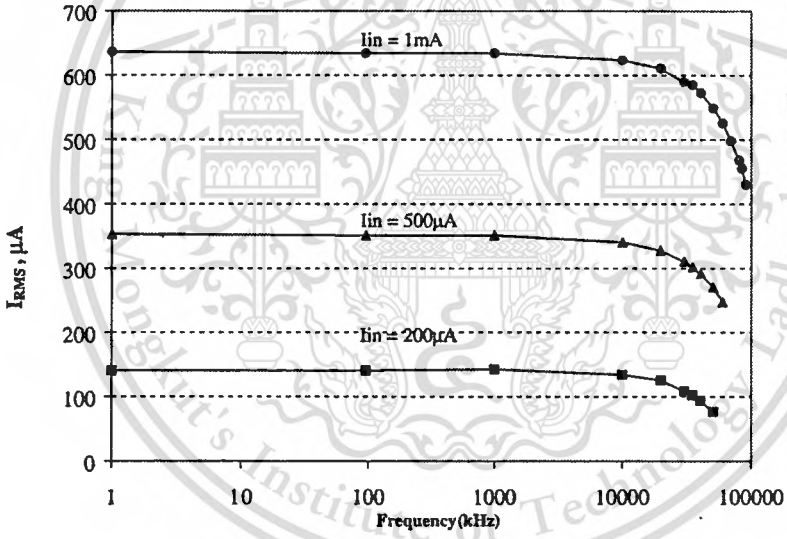

Figure 8. High-frequency responses due to the variation of I_{in}.

($I_{in} = 1\,\text{mA}_{(peak)}$). The results show the bandwidth of about 35 MHz, 60 MHz and 85 MHz, respectively. The results are agreed with the predicted value from (26), where the bandwidth drops off as the input current signal is reduced. The simulation results for the −3 dB bandwidth with the peak input current ranging from $I_{in} = 100\,\mu\text{A}$ to $1000\,\mu\text{A}$ were summarized in table 3. The simulated power dissipation for $I_{in} = 1\,\text{mA}$ is about 6.04 nW, which is very low.

Generally, crest factor is the ratio of the peak value relative to the rms value. So far the characteristics of the circuit have been studied for the common waveforms as sine and triangle waveforms, which have relatively low crest factor (≤2). The simulation results for the input signal with different crest factors are shown in figure 9. The rectangular pulse train with pulse width of 1 ms was used for this test, since it is the

Parameters	Simulated results
Supply voltage (rated)	5 V to 15 V
Input current range (MAX)	1.5 mA
Power dissipated	6.04 nW
Gain error	2% Max. nonlinearity 100 μA to 1.5 mA input
Peak amplitude value	−3 dB bandwidth
$I_{in} = 100\,\mu A$	25 MHz
$I_{in} = 200\,\mu A$	40 MHz
$I_{in} = 500\,\mu A$	60 MHz
$I_{in} = 900\,\mu A$	85 MHz
$I_{in} = 1000\,\mu A$	90 MHz
$I_{in} = 1500\,\mu A$	100 MHz

Table 3. Performance of the rms-to-dc converter.

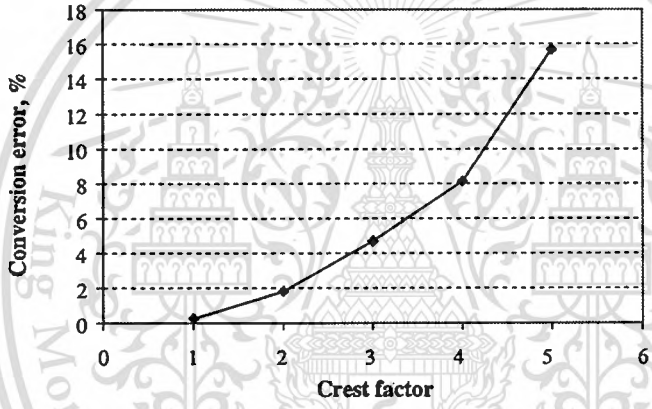

Figure 9. Simulation results for the additional error vs crest factor.

worst-case waveform for rms measurement. The duty cycle and peak amplitude were adjusted to produce crest factors from 1 to 5, while maintaining a constant $1\,mA_{(peak)}$ input current (Helms 1987). We found that the proposed rms-to-dc converter performs very well with crest factors of 3 or less. As shown in figure 9, for the case of crest factor equal to 3, the conversion error is less than 5%. However, for the higher crest factor, such as 4, the conversion error is more than 8%. This is due to the waveforms with the higher crest factor, such that the rms value is decreased. Consequently, the bias current of the rms-to-dc converter circuit is also reduced and will affect the accuracy of the circuit. To provide good accuracy at high crest factor, the input current should be increased. For example, with the crest factor of 4, the conversion error was reduced to 6% if we set the input current (I_{in}) equal to 2 mA.

4. Conclusion

We have developed a simple CMOS true rms-to-dc converter circuit that is based on the use of the characteristic of a CMOS squaring circuit, where all the transistors are biased in the saturation region. The realization scheme is based on the implicit

computation method and is suitable for implementation in standard CMOS process. The circuit is suitable for all input wave forms. The characteristics of the proposed are confirmed from the experimental results and PSPICE simulation results. The accuracy, linearity and frequency response were measured and summarized in table 3. Simulation results are also used to confirm the characteristics of the proposed circuits.

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On the realization of electronically current-tunable CMOS OTA

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Abstract

A CMOS operational transconductance amplifier (OTA) called as an EOTA, where its transconductance gain can be electronically and linearly tuned is proposed in this paper. The realization method is achieved by squaring the transconductance gain of the balanced CMOS OTA. The EOTA transconductance gain can be linearly tuned by an external bias current for three decades. The linear input-voltage range of about 1 Vp with less than 1% nonlinearity is obtained. The usefulness of the proposed EOTA is demonstrated through application example with a current multiplier. The performance of the proposed circuit is discussed and confirmed through PSPICE-simulation results.

Keywords: CMOS OTA; Electronically and linearly tuned; Current controlled

1. Introduction

Linear transconductors or voltage-to-current converter circuits are fundamental building blocks of analog circuits and systems. They are found useful in interface circuits, instrumentation amplifiers, continuous-time-filters and oscillators. In addition, when the transconductance gain of the transconductor can be electronically varied, they can also be applied in automatic gain control circuits and in analog multipliers. In the last two decades, it is well accepted that a linear transconductor, which is constructed from a bi-polar differential pair and current mirrors, called as an operational transconductance amplifier (OTA), is one of the essential active building blocks in the design of analog circuits [1–3]. This is due to the fact that the OTA is a low-cost device that has only a single high-impedance node and its transconductance gain g_m can be linearly controlled over more than four decades by means of an external bias current. Moreover, the implementation of analog circuits in such a way that employs only OTA as standard cells will not only be easily constructed from readily commercial available IC, but also significantly simplified the design.

In CMOS technology, several linearly tunable transconductors based on the use of MOS transistors operating in saturation region have been proposed in the literature [4–7]. Most of them are functioning in voltage-controlled mode. The method of source-follower of Ref. [4] is operated in square law characteristic with constant source-bulk voltages, where the control voltage is applied to the gate. Whereas for the cross-coupled connection methods [5–7], the transconductance control voltages are applied through voltage-level shifters. However, their controllable voltage ranges are rather limited and only narrow linearly tunable transconductance ranges are available. In some applications, such as, an analog multiplier circuit, a frequency divider/multiplier circuit and an arbitrary power-law circuit, current-controlled transconductors that this transconductance gain can be linearly controllable by a DC bias current are preferable [8–10]. In the past, a current-controlled CMOS transconductor was

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presented in Ref. [11]. But the linearly tunable transconductance range is narrow due to the MOS transistors are working in the weak-inversion region.

The main objective of this paper is, therefore, to present a circuit design technique for the synthesis of a linear electronically tunable CMOS OTA, called as an EOTA. Since, the realization method is achieved by squaring the transconductance gain of the CMOS OTA, the transconductance gain of the EOTA is directly depend on the DC bias current. To provide a maximum output voltage swing and wide linearly tunable transconductance range, a balanced CMOS OTA or voltage-to-current transducer will be employed as basic active circuit elements to realize the EOTA, whereas the completed EOTA requires three balanced CMOS OTA's. Since it is generally assumed that all MOS transistors are operating in the saturation region, the individual functions of the circuits are derived from the approximate square-law characteristic of MOS transistors in saturation. In addition, it is well accepted that the design and implementation of electronically tunable analog circuits using bipolar-based OTA as active circuit elements are well established and well tabulated. Then, having access to such a linear electronically tunable CMOS OTA, it would enable us to realize CMOS analog circuits with their property can be electronically tuned by simply replacing a bipolar OTA with an EOTA. This kind of advantage will be demonstrated through an application example. The proposed EOTA is employed to implement a current multiplier circuit, that using only active elements and without the requirement of external passive elements. The circuit performances are studied through PSPICE-simulation results.

2. Circuit description

For the purpose of the following analysis, we will assume that all MOS devices operate in the saturation region. This means that the transistor drain current I_D is characterized by a square-law model as

$$I_D = K(V_{GS} - V_T)^2 \quad \text{for } V_{GS} > V_T,$$
$$= 0 \quad \text{for } V_{GS} \leqslant V_T, \tag{1}$$

where the transconductance parameter $K = \mu C_{ox} W/2L$, μ is the mobility of the carrier, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length, and V_{GS} and V_T are the gate-to-source and the threshold voltages, respectively.

2.1. A balanced CMOS OTA

Fig. 1 shows a balanced single-output CMOS OTA, which is formed by MOS coupled pair and current mirrors, where V_{in} is the differential input voltage ($V_{in} = V_1 - V_2$), i_o is the output current and I_{BB} is the bias current. Let us assume that M_1 and M_2 are perfectly matched and the current mirrors

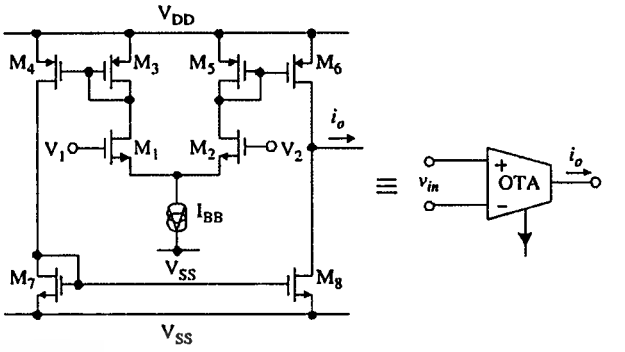

Fig. 1. Schematic diagram of a balanced CMOS OTA.

have unity current gain. By using Eq. (1), the differential output current of the circuit in Fig. 1 can be given by [12]

$$i_o = i_2 - i_1$$
$$= \sqrt{2I_{BB}K}\, V_{in} \sqrt{1 - \frac{KV_{in}^2}{2I_{BB}}} \quad \text{for}$$
$$-\sqrt{\frac{I_{BB}}{K}} \leqslant V_{in} \leqslant \sqrt{\frac{I_{BB}}{K}}. \tag{2}$$

The transconductance gain (g_m) of the fully differential OTA can be derived by taking the derivative of Eq. (2) with respect to V_{in}, yielding

$$g_m = \left.\frac{di_o}{dV_{in}}\right|_{V_{in}=0}$$
$$= \sqrt{2I_{BB}K} \quad \text{for}$$
$$-\sqrt{\frac{I_{BB}}{K}} \leqslant V_{in} \leqslant \sqrt{\frac{I_{BB}}{K}}. \tag{3}$$

From Eq. (2), the current i_o can written as

$$i_o = g_m V_{in} = \sqrt{2I_{BB}K}\, V_{in}. \tag{4}$$

Eq. (3) shows that the transconductance gain (g_m) of the OTA can be varied by the bias current I_{BB}, but in the form of square root function. In addition, in order to operate in the low distortion range, where all the transistors are operated in saturation, the input voltage V_{in} should be in the range of [13]

$$V_{in} \leqslant \left|\sqrt{I_{BB}/K}\right|. \tag{5}$$

2.2. The proposed electronically and linearly tunable CMOS OTA

Through the use of three balanced single-output CMOS OTAs, a CMOS-based electronically and linearly tunable OTA, called as an EOTA, can be realized by the circuit diagram shown in Fig. 2. The OTA_1 converts a differential input signal voltage $v_{in} = v_1 - v_2$ into a signal current i_L to

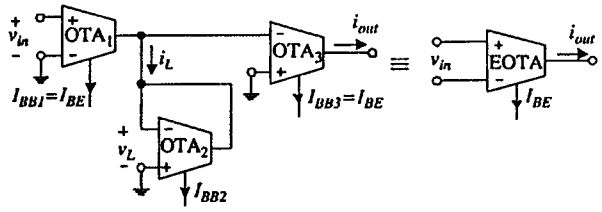

Fig. 2. The proposed EOTA.

flow into an active resistor R_L, formed by the OTA_2, where $Z_L = 1/g_{m2}$ and g_{m2} represents the transconductance gain of the OTA2. Since the current signal $i_L = g_{m1}v_{in}$, the voltage drop across the active resistor (OTA_2) becomes

$$v_L = i_L z_L = g_{m1} v_{in} \frac{1}{g_{m2}}. \tag{6}$$

The OTA_3 will convert the voltage v_L, with the transconductance gain of g_{m3}, into the output current i_{out} as

$$i_{out} = g_{m3} v_L = g_{m1} v_{in} \frac{1}{g_{m2}}. \tag{7}$$

From Eqs. (6) and (7), the current i_{out} can be rewritten as

$$i_{out} = \frac{g_{m1} g_{m3}}{g_{m2}} v_{in}. \tag{8}$$

Since $g_{m1} = \sqrt{2I_{BB1}K_1}$, $g_{m2} = \sqrt{2I_{BB2}K_2}$ and $g_{m3} = \sqrt{2I_{BB3}K_3}$, if we set $I_{BB1} = I_{BB3} = I_{BE}$, then from Eq. (8), we obtain

$$i_{out} = \frac{2I_{BE}\sqrt{K_1 K_3}}{\sqrt{2I_{BB2}K_2}} v_{in} = g_{mT} v_{in}, \tag{9}$$

where g_{mT} represents the transconductance gain of the proposed EOTA and can be expressed as

$$g_{mT} = 2I_{BE} K_T \tag{10}$$

and $K_T = \sqrt{K_1 K_3 / 2I_{BB2}K_2}$, which can usually be kept at constant. Eq. (10) clearly indicted that the transconductance gain of the proposed EOTA can be electronically and linearly tuned by the bias current I_{BE}. This linear relationship is in the form that similar to the transconductance gain of the bi-polar-based OTA that found useful in many applications [14]. Since the balanced CMOS OTA is formed by MOS coupled pair and current mirrors, therefore, the proposed EOTA is very suitable for fabricating in CMOS integrated form.

3. Performance of the EOTA

It is well accepted that the prediction of Eq. (10) will be valid only for a small value of V_{in}. From Eq. (5), since OTA_1 and OTA_3 are formed by MOS coupled pairs, to maintain in the linear range and low total harmonic distortion, the voltages V_{in} and V_L should, respectively, be restricted to the ranges of [13]

$$|V_L|_{MAX} = 0.4/\sqrt{2K}\, Z_L$$

and

$$|V_{in}|_{MAX} = 0.4\sqrt{I_{BB}/K}, \tag{11}$$

where it should be noted from Eq. (11) that the maximum usable voltage range is limited by $|V_L|_{MAX}$ if $g_{m1}/g_{m2} > 1$ and it is limited by $|V_{in}|_{MAX}$ if $g_{m1}/g_{m2} < 1$. For example, for $I_{BE} = 1$ mA and $I_{BB2} = 700\,\mu$A, the maximum usable range is determined by $|V_L|_{MAX}$ and $|V_L|_{MAX}$ is about 0.94 V, for $K = \mu_n C_{ox} W/2L = 1.27 \times 10^{-4}$ A/V^2, $\mu_n C_{ox} = 5.08 \times 10^{-5}$ V and $W/2L = 2.5$.

The transconductance gain error that results from in the inaccuracy of the EOTA can be determined from a large signal analysis. Consider the balanced CMOS OTA, the transconductance gain G_m of the Eq. (2) can be written as

$$G_m = \frac{i_{out}}{V_{in}} = \sqrt{2I_{BB}K}\sqrt{1 - \frac{KV_{in}^2}{2I_{BB}}} \quad \text{for} \quad -\sqrt{\frac{I_{BB}}{K}} \leqslant V_{in} \leqslant \sqrt{\frac{I_{BB}}{K}}. \tag{12}$$

If we set the transconductance error of the balanced CMOS OTA of Fig. 1 as $E = KV_{in}^2/2I_{BB}$, then Eq. (12) can be rewritten as

$$G_m = \frac{i_{out}}{V_{in}} = \sqrt{2I_{BB}K}\sqrt{1 - E}. \tag{13}$$

We found that the G_m will equal to the g_m of Eq. (3) in the condition that $KV_{in}^2/2I_{BB} \ll 1$. This can be achieved by keeping the input voltage signal V_{in} small or set the DC bias current I_{BB} to a large value.

By applying the G_m of Eq. (13) to the circuit of Fig. 2, we obtain the transconductance gain of the proposed EOTA for large signal as

$$G_{mT} = 2I_{BB}K_T\left(1 + \frac{\sqrt{1-E_1}\sqrt{1-E_3} - \sqrt{1-E_2}}{\sqrt{1-E_2}}\right), \tag{14}$$

where the errors $E_1 = K_1 V_{in1}^2/2I_{BB1}$, $E_2 = K_2 V_{in2}^2/2I_{BB2}$ and $E_3 = K_3 V_{in3}^2/2I_{BB3}$ are the transconductance errors due to the OTA_1, OTA_2 and OTA_3, respectively. Given that E_T is the transconductance error of the EOTA from the linear transconductance gain, we can write

$$E_T = \frac{\sqrt{1-E_1}\sqrt{1-E_3} - \sqrt{1-E_2}}{\sqrt{1-E_2}}. \tag{15}$$

Thus, we have the percent of the conversion error as

$$\%\, E_T = \frac{\sqrt{1-E_1}\sqrt{1-E_3} - \sqrt{1-E_2}}{\sqrt{1-E_2}} \times 100\%. \tag{16}$$

For example, if $V_{in1}=0.5$ V, $V_{in2}=V_{in3}=0.751$ V, $I_{BB1}=I_{BB3}=I_{BE}=1$ mA, $I_{BB2}=700\,\mu$A and $K_1=K_2=K_3=1.27\times10^{-4}$ A/V^2, the resulting transconductance error (% E_T) is equal to 0.54%.

4. A current multiplier circuit

In order to demonstrate the applications and the usefulness of the proposed EOTA, an application example will be outlined in this section. It outlines the use of the EOTA to realize the current-mode multiplier which employs only active circuit elements.

The current multiplier circuit is shown in Fig. 3. This application is adapted from the bipolar-based OTA-based circuits by replacing the bipolar-based OTA with the proposed EOTA [15]. From the figure, the input signal current i_{in1} is injected into the EOTA$_1$, which is connected as a current-controlled grounded resistor. The voltage across the EOTA$_1$ is then used as the input voltage for the EOTA$_2$ and EOTA$_3$. The input signal current i_{in2} is added with the bias current I_{B2} of the EOTA$_2$. Let g_{mT1}, g_{mT2} and g_{mT3} be the transconductance gains of the EOTA$_1$, EOTA$_2$ and EOTA$_3$, respectively. Then from Eq. (9) and from routine circuit analysis the output currents i_{o2} and i_{o3} of the EOTA$_2$ and EOTA$_3$, respectively, can be written as

$$i_{o2}=\frac{g_{mT2}}{g_{mT1}}i_{in1}=\frac{(I_{BE2}+i_{in2})}{I_{BE1}}i_{in1} \tag{17}$$

and

$$i_{o3}=-\frac{g_{mT3}}{g_{mT1}}i_{in1}=-\frac{I_{BE3}}{I_{BE1}}i_{in1}, \tag{18}$$

where I_{BE1}, I_{BE2} and I_{BE3} represent the DC bias current of the EOTA$_1$, EOTA$_2$ and EOTA$_3$, respectively, and the transconductance gains $g_{mT1}=2I_{BE1}K_{T1}$, $g_{mT2}=2(I_{BE2}+i_{in2})K_{T2}$ and $g_{mT3}=2I_{BE3}K_{T3}$. If we set $I_{BE2}=I_{BE3}=I_B$, the output current I_{out} of the circuit that is the summation of the currents i_{o2} and i_{o3} can be expressed as

$$I_{out}=i_{o2}+i_{o3}=\frac{i_{in1}i_{in2}}{I_{BE1}}, \tag{19}$$

which is in the form of a current multiplication function.

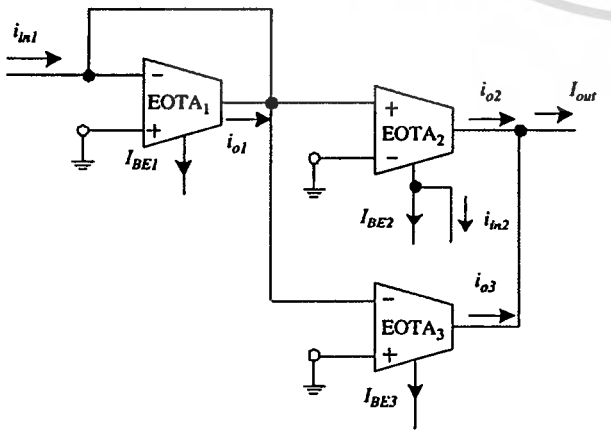

Fig. 3. The multiplier circuit using EOTA.

5. Simulation results

The performance of the proposed EOTA of Fig. 2 and its applications were verified through the use of PSPICE-simulation results. All the balanced CMOS OTA was simulated by using CMOS transistor parameters of the SCN2 level 2 of MOSIS [16]. The dimensions of transistors M_1 and M_2 are $W=50\,\mu$m and $L=10\,\mu$m, the dimensions of the transistor M_3-M_8 are $W=100\,\mu$m and $L=10\,\mu$m. The power supply voltage were set to $V_{DD}=-V_{SS}=\pm5$ V. Fig. 4 shows the simulated transfer characteristic of the EOTA of Fig. 2. The plots of the output current I_{out} versus the input voltage V_{in} show that, for the DC bias current (I_{BE}) in the cases of 1 mA, 800 μA and 400 μA, the EOTA can linearly convert the input voltage into output signal current with nonlinearity of less than 1% for the input voltage (V_{in}) in the ranges of −1 to 1 V, −0.86 to 0.86 V and −0.66 to 0.66 V, respectively. These results were agreed with the prediction value from Eq. (9). For example, for the case of the DC bias current $I_{BE}=1$ mA and for $V_{in}=0.86$ V, $I_{BB2}=700\,\mu$A, the transconductance gain $g_{mT}=5.398\times10^{-4}$ A/V, where the conversion error is about 0.5%. The frequency response of the EOTA was also studied, where the −3 dB bandwidth of about 120 MHz is achieved.

The plot of the relation between the transconductance gain g_{mT} and the bias current I_{BE} in Fig. 5 is measured by fixing $V_{in}=0.1$ V and varying I_{BE} from 10 nA to 1 mA. It shows that the transconductance gain g_{mT} can be linearly tuned by the bias current I_{BE} over the range of 1 μA–1 mA (three decades), where the simulated conversion error found to be about 0.68%. The similar relation of g_{mT} versus I_{BE} are also obtained for the cases of fixing $V_{in}=0.2$ V and $V_{in}=0.5$ V. But in these cases the linear tunable ranges should be started at the current I_{BE} that must more than 5 and 32 μA, respectively, since the entire MOS transistors must be operated in saturation region.

To demonstrate that the circuit of Fig. 3 can be functioned as current multiplier, two sinusoidal current signals are applied. Fig. 6 shows the response for the case of $i_{in1}=0.2\sin(2\pi1000t)$ mA, $i_{in2}=0.2\sin(2\pi20\,000t)$ mA and $I_{B1}=1$ mA. This result confirms that the circuit can accurately modulate two different input signal currents. The DC transfer characteristics of the multiplier circuit shown in Fig. 7 were observed by setting the bias currents $I_{B1}=I_{B2}=I_{B3}=1$ mA, and the input current i_{in1} and i_{in2} are varied from −200 μA to 200 μA with 100 μA per step. The transfer characteristic demonstrated that the simulated and calculated data are agreed very well over the input range of

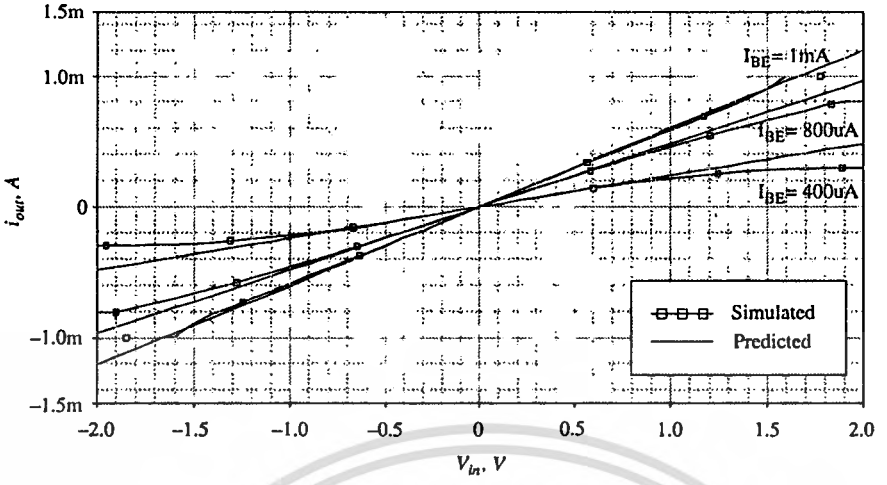

Fig. 4. DC transfer characteristics of the EOTA.

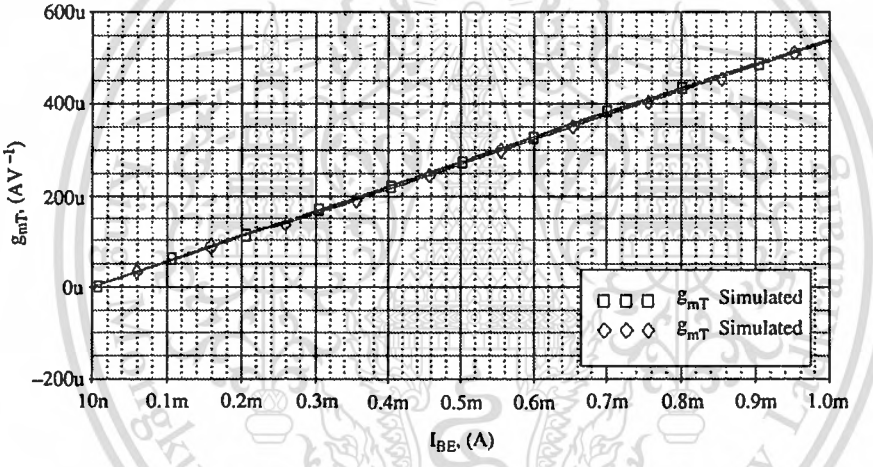

Fig. 5. Linear transconductance tunable range.

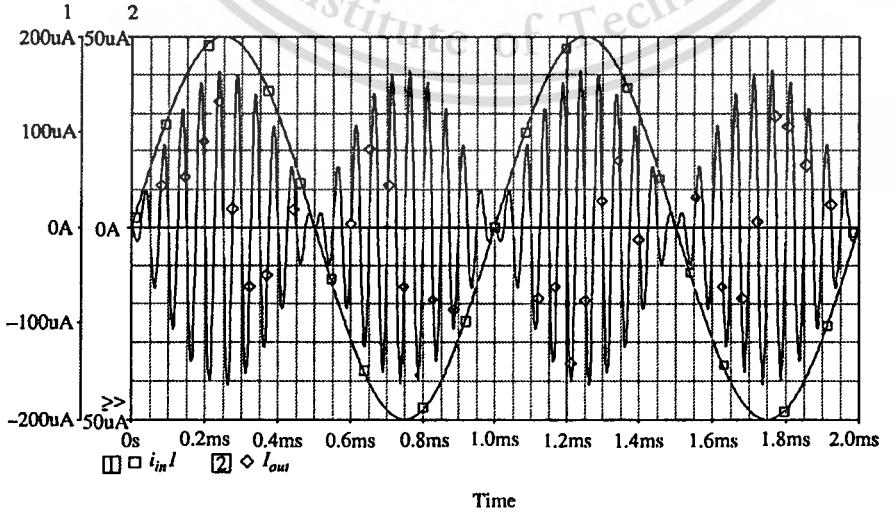

Fig. 6. Simulated transient response of the multiplier circuit.

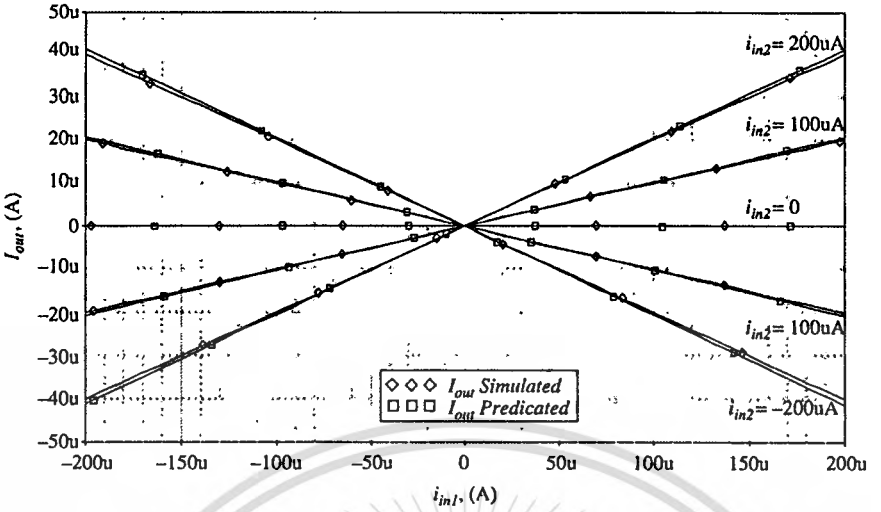

Fig. 7. Simulated DC transfer characteristic of the multiplier.

190 μA with the error of less than 1%. The high-frequency characteristic of the multiplier circuit is also studied. The simulated −3 dB bandwidth for the case of the input i_{in1} to the output I_{out}, with $i_{in1} = 0.5\sin(2\pi 10\,000t)$ mA, $i_{in2} =$ 500 μA and $I_{B1} = 1$ mA, is about 75 MHz and the simulated −3 dB bandwidth of the circuit for the input i_{in2} to the output I_{out}, with $i_{in2} = 0.5\sin(2\pi 10\,000t)$ mA, $i_{in1} = 500$ μA and $I_{B1} = 1$ mA, is about 71 MHz.

6. Conclusion

A design of the CMOS-based electronically and linearly current-tunable OTA has been proposed. The EOTA circuit composed of three balanced CMOS OTAs which is suitable for implementing in CMOS integrated form. The achieve characteristics of the proposed circuit were similar as the bipolar OTA that the transconductance gain (g_m) can be linearly tuned by the DC bias current. Simulation results have been employed to demonstrate the performances of the proposed EOTA. Moreover to confirm that EOTA can be replacing the bipolar OTA, the current-mode multiplier circuit is used to display the performances of the proposed circuit.

Acknowledgments

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A WIDE-BAND CURRENT-MODE OTA-BASED ANALOG MULTIPLIER-DIVIDER

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ABSTRACT

A current-mode analog multiplier-divider circuit that realized through the use of operational transconductance amplifiers (OTAs) is proposed in this paper. The proposed scheme is realized in such a way that employs only OTAs as active circuit elements and does not require external passive circuit elements. The circuit is simple and can be easily constructed from commercially available IC. The circuit is temperature compensated and the circuit bandwidth is approximately close to the bandwidth of pnp current mirrors or $f_{TP}/2$. The performance of the multiplier-divider circuit is discussed and confirmed by simulation results.

1. INTRODUCTION

Analog multipliers and dividers are important nonlinear building blocks that have found useful in wide range of applications,particularly,in the fields of control, instrumentation, measurement, signal processing and telecommunication. At present, because of the main featuring of wider bandwidth, greater linearity, wider dynamic range and simple circuitry compared with their voltage-mode counterparts, current-mode circuits have been received growing interest in analog signal processing. Many techniques to design current-mode analog multiplier-divider circuits have been presented in the literatures. For examples, the methods that are suitable for CMOS integrated technology [1-3], and the methods that are implemented through the use of active circuit elements such as, for examples, current feedback amplifiers (CFAs) [4] and second-generation current-controlled current-conveyors (CCCIIs) [5].

It is well accepted that an OTA is one of the essential active building blocks in the design of analog circuits such as, for example, active filters, active networks and oscillators [6,7]. This is due to the fact that an OTA is a low-cost device that has only a single high-impedance node and its transcondeuctance gain g_m can be linearly controlled over more than four decades by means of an external bias current. The implementation of analog circuits in such a way that employs only OTA as standard cells will not only be easily constructed from readily commercial available IC, but also significantly simplified the design. In addition, the OTA-based circuit that requires no external passive element would facilitate its integratability and programmability [8]. Although, in the past, circuit techniques that employ OTAs to implement analog multiplier have been presented [7,9]. However, they are voltage-mode circuits, only multiplication functions are realized, and the circuit bandwidths are only about 2 MHz. In this paper, a current-mode temperature compensated multiplier-divider circuit using only OTAs as active circuit elements has been presented. The realization scheme does not require external passive elements. PSPICE simulation results will be used to demonstrate the performance of the proposed realization scheme.

2. BASIC PRINCIPLE

In this work, a bipolar-based OTA will be employed as an active circuit element, where its schematic diagram is shown in the Fig.1. The commercially available OTAs of this type are such as LM13600 and CA3280. By assuming that the OTAs are operated in the linear range, the OTA transconductance gain is $gm = I_B/2V_T$, which can be tuned by the DC bias current (I_B).

The circuit diagram of the proposed current multiplier-divider circuit using OTAs is shows in Fig. 2. The input signal current i_{in1} is injected into the operational transconductance amplifier OTA1, which is connected as a current-controlled grounded resistor. The voltage across the OTA1 is then used as the input voltage for the OTA2 and OTA3. The input signal current i_{in2} is added with the bias current I_{B2} of the OTA2. Let g_{m1}, g_{m2} and g_{m3} be the transconductance gains of the OTA1, OTA2 and OTA3, respectively. Then, from routine circuit analysis, the output currents I_{O2} and I_{O3} of the OTA2 and OTA3, respectively, can be written as

$$I_{o2} = \frac{g_{m2}}{g_{m1}} i_{in1} = \frac{(I_{B2} + i_{in2})}{I_{B1}} i_{in1} \qquad (1)$$

and

$$I_{o3} = -\frac{g_{m3}}{g_{m1}} i_{in1} = -\frac{(I_{B3})}{I_{B1}} i_{in1} \qquad (2)$$

where $g_{m1} = I_{B1}/2V_T$, $g_{m2} = (I_{B2}+i_{in2})/2V_T$ and $g_{m3} = I_{B3}/2V_T$ and V_T is the usual thermal voltage. If we set the bias current such that $I_{B2} = I_{B3} = I_B$, the output current I_{out} of the circuit, that is the summation of the currents I_{O2} and I_{O3}, can be expressed as

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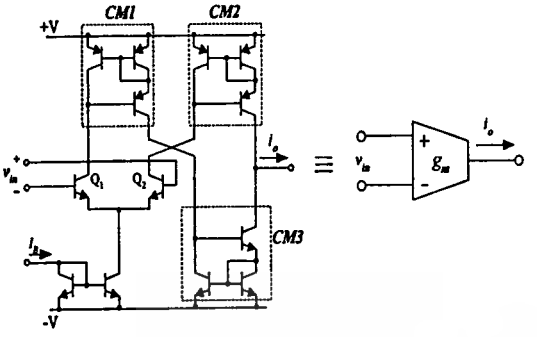

Figure 1. The schematic diagram of the OTA.

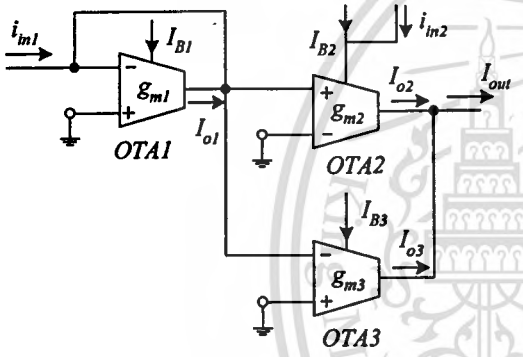

Figure 2. The proposed current-mode multiplier-divider cuicuit using OTAs.

$$I_{out} = I_{o2} + I_{o3} = \frac{i_{in1} i_{in2}}{I_{B1}} \qquad (3)$$

which is in the form of a current-mode analog multiplication-division function. The circuit is performed as a four-quadrant multiplier if i_{in1} and i_{in2} are the input current signals. On the other hand, the circuit is performed as a divider circuit if i_{in1} (or i_{in2}) and I_{B1} are the input signal currents. It should be noted from the eqns. (1)-(3) that, since the output current I_{out} is in the form of the ratio of OTAs transconductance gains, therefore, the thermal voltages V_T's of the OTAs are compensated. This means that the output current I_{out} is less sensitive to temperature.

3. CIRCUIT PERFORMANCE

The major factors that contribute to the error and non-linearity in the circuit can be identified as follows. The first factor is due to the offset current at the output port of the OTA1. From eqn. (3), if I_{os} is the offset current at the output port of the OTA1, the output current I_{out} can be rewritten as

$$I_{out} = \frac{(i_{in1} \pm I_{os}) i_{in2}}{I_{B1}} \qquad (4)$$

We can see that, apart from the multiplication-division result, this offset current produces a signal current that is proportional to the signal current i_{in2} to leak through the output. This effect can be reduced if $|i_{in1}| >> I_{os}$ and the bias current $I_{B1} >> I_{os}$. While the offset currents at the output ports of the OTA2 and OTA3 are not contribute to the multiplication error, but will produce a DC current at the output of the circuit.

The second factor that causes the non-linearity at the output of the circuit is due to the limited linear range of the input stages of the OTA2 and OTA3, where their input stages are conventional differential pairs. For linear operation, the input differential voltage of the bipolar-based OTA is restricted to be less than 26 mV. Therefore, to minimize this error, the voltage swing across the OTA1 should be kept to be less than 26 mV. On the other hand, it is means that the signal current i_{in1} should be limited to $|i_{in1}| < I_{B1}$.

For the high frequency response, consider the schematic diagram shown in the Fig.1. The OTA is comprised of three major building blocks, the common-base differential pairs (Q_1 and Q_2), the n-p-n current mirror (CM3) and the pnp current mirrors (CM1 and CM2). The bandwidth of the differential pair will be equal to f_{α}, which is approximately close to f_T of the n-p-n transistor or f_{TN}. For the current mirror, the bandwidth of Wilson's current mirror is approximately equal $f_T/2$. And, usually, the npn transistor f_{TN} is much higher than the lateral pnp transistor f_{TP}. Thus, the limitation to the high frequency performance of the proposed multiplier-divider circuit is mainly due to the bandwidth of the current mirrors CM2 and CM3, which is approximately equal to $f_{TP}/2$.

4. SIMULATION RESULTS

The performance of the proposed multiplier-divider circuit of Fig.2 was verified through the use of SPICE simulation results. All the OTA was simulated by using the bipolar transistor parameters of the 2N3904 and 2N3906 for the npn and pnp transistors, respectively, where β_N=416 and β_P=180. The transistors f_{TN} and f_{TP} were 400MHz and 300MHz, respectively. Since the DC offset current will distort the output signal, a DC current of about 5μA was injected at the output of the OTA1 to adjust the offset to be less than ±0.1μA. Noting that this offset can be reduced by using transistors with high value of beta, specially pnp transistors. The power supply voltages were set to V_{CC} = 10V and V_{EE} = -10V.

The multiplier function was tested by multiplying two sinusoidal signals. The results obtained are shown in Fig. 3 for i_{in1} = 0.5sin(2π1000t) mA, i_{in2} = 0.5sin(2π30000t) mA and I_{B1} = 1mA. Fig.4 shows the simulated DC transfer characteristics for the multiplier function, where the bias currents were set to $I_{B1} = I_{B2} = I_{B3}$=1mA.

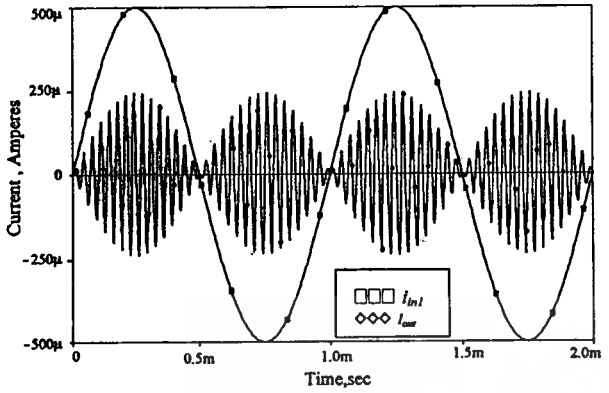

Figure 3. Simulated transient response for the multiplier function.

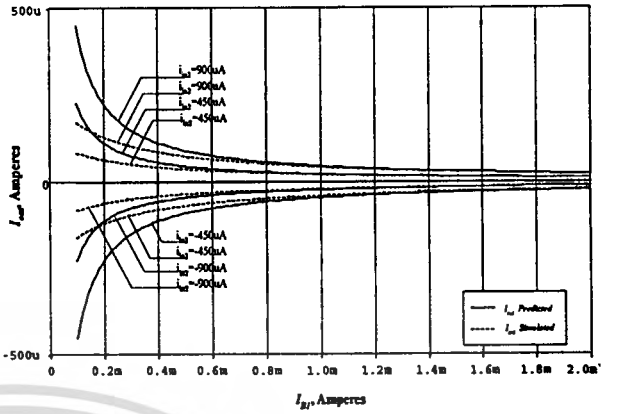

Figure 6. Simulated DC transfer characteristic of the divider.

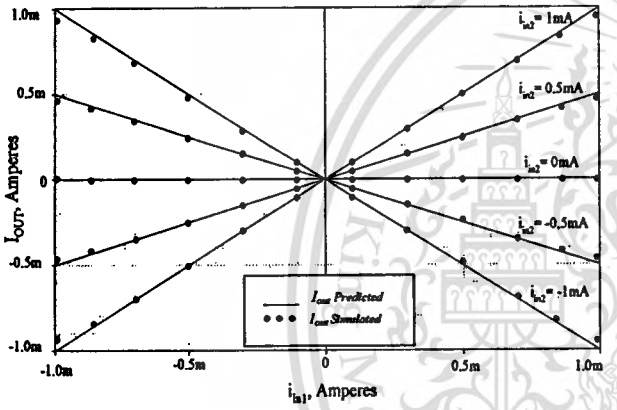

Figure 4. Simulated DC transfer characteristic of the multiplier.

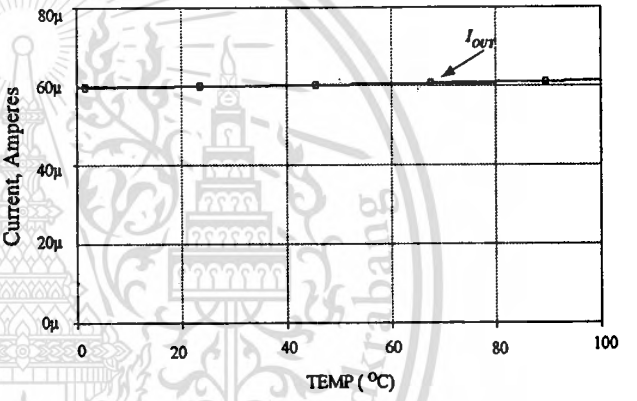

Figure 7. Simulated transient response of I_{out} versus Temperature.

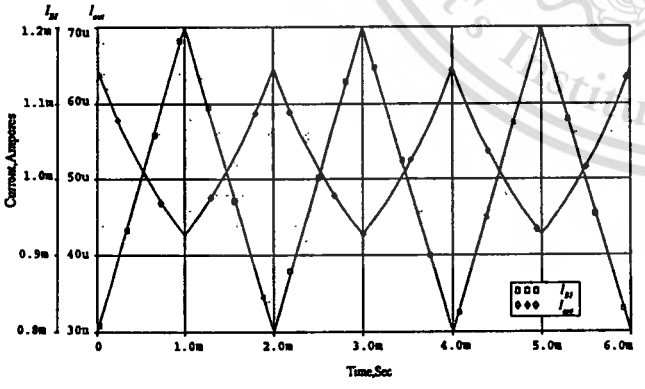

Figure 5. Simulated transient response for the divider function.

The figure shows the plot of the output current I_{out} against the input signal current i_{in1} from –1mA to 1mA and the input signal current i_{in2} from –1mA to 1mA with 0.5mA per step. The simulation and calculated data are agreed very well over the ±0.8mA input range with error of less than 0.1%. We can see large non-linearity for i_{in1} close 1mA this is due to that the voltage across the OTA1 is closed to the limited linear range. Fig.5 shows the simulated transient response of the circuit that is functioned as a divider. In this case, the output current I_{out} is an inverting function of a triangular wave signal, where i_{in1} and i_{in2} are DC currents, i.e. i_{in1} = 50μA, i_{in2} = 900μA, and I_{B1} is a 500Hz triangular wave with amplitude of 200μA and with DC component of equal to 1mA. To demonstrate the error, Fig.6 shows the comparison of the simulated and the calculated values of the output current I_{out}. The output current I_{out} is ploted against I_{B1} with i_{in2} taking values from –0.9mA to 0.9mA with 0.45mA steps. For i_{in2} is positive, we found that the relative error is decrease if i_{in2} is increase, for examples, for 1mA<I_{B1}<2mA, i_{in2} = 0.3, 0.6 and 0.5mA the error are 7.36, 6.17 and 5.0%, respectively. However for i_{in2} is negative, the relative error is high, such as the error is about 12 % for i_{in2} = -0.9mA, since the bias current of the OTA2 in this case is small (I_{B2}-$|i_{in2}|$). The linearity of the divider

function is depend on the value of the input current i_{in1} also, where i_{in1} should be kept in the linear range of the multiplier function.

For a load resistance R_L =100Ω, the simulated –3dB bandwidth of the circuit from the input i_{in1} to the output I_{out}, with i_{in1} = 0.1sin(2π10000t) mA, i_{in2} = 100μA and I_{B1} = 1mA, is about 155 MHz. The simulate –3dB bandwidth of the circuit from the input i_{in2} to the output I_{out}, with i_{in2} = 0.1sin(2π10000t) mA, i_{in1} = 100μA and I_{B1} = 1mA, is about 160 MHz. These responses indicate that the circuit bandwidth is close to the pnp transistor $f_{TP}/2$. However, since there exit a capacitance of about C_O = 7.5pF at the output terminal of the OTA, the pole due to R_L and C_O will limit the high frequency performance if the load resistance is too high. For example, if R_L = 1kΩ, the pole due to C_O is located at 21.2 MHz. The total harmonic distortion (THD) against input currents, for the case that the input signal i_{in2} is a dc current of 100μA and the input signal current i_{in1} = 0.25sin(2π10000t) mA, is about 0.22%. On the other hand, when the input signal current i_{in1} is dc current of 100μA and the signal current i_{in2} = 0.25sin(2π10000t) mA, the THD is about 0.25%. It should be noted that the THD for the case of i_{in1} to I_{out} is lower than the case of i_{in2} to I_{out}. This is due to that the harmonics distortion from of i_{in2} is straightforwardly appear at the I_{out}. But the harmonics distortion from OTA1 is firstly amplified by both the OTA2 and OTA3 and then the amplified harmonic are cancelled at the output terminal.

The dependency of the output current on temperature was studied and shown in Fig.7. The simulation results for the variation of the output current (I_{out}) due to the change of temperature are plotted for the operating temperature variations from 0 °C to 100 °C. We set the input signal currents i_{in1} and i_{in2} as dc currents, where I_{B1} = I_{B2} = I_{B3} = 1mA, i_{in1} = 1mA and i_{in2} = 60μA, which corresponds to I_{out} = 60μA at 27 °C. From the results, the output current varies from 59.62μA to 61.38μA, for the temperature 0 °C to 100 °C, respectively. The relative sensitivity of I_{out} with respect to temperature of the conventional OTA and the proposed circuit, which is given by $S_T^{I_{out}} = (\partial I_{out}/I_{out})/(\partial T/T)$, is approximately equal to 0.046 and 6.2×10^{-3}, respectively. This simulation results demonstrated that, by this realization, the temperature dependence of the transconductance gains g_{m1}, g_{m2} and g_{m3} of the bipolar OTAs can also be compensated.

5. CONCLUSIONS

In this paper, we have proposed a current-mode analog multiplier-divider circuit that realized through the use of OTAs. The circuit is simple and can be easily constructed from the commercially available OTA. The realization method does not require any external passive circuit element and also temperature compensated. The circuit bandwidth is close to the bandwidth of p-n-p current mirror or $f_{TP}/2$. Simulation results have been employed to demonstrate the performances of the multiplier-divider circuit. Noting that, although in this paper, the bipolar-based OTA has been used as the active circuit elements, however, the CMOS-based OTA which its transconductance gain g_m can be linearly tuned by the external DC bias current [10] can also be used.

6. ACKNOWLEDGEMENTS

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An Electronically and Linearly Tunable CMOS OTA

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Abstract: An electronically and linearly tunable CMOS OTA that constructed from a balanced CMOS OTAs is proposed in this paper. The circuit achieves its linearity by squaring the nonlinear transconductance of the balanced CMOS OTA. The proposed circuit can be linearly tune by the bias current for three decades. The obtained linear input-voltage range is $1V_p$ with less than 1% nonlinearity. The performance of the proposed circuit is discussed and confirmed through PSPICE simulation results.

1. Introduction

It is well accepted that linear transconductors or voltage-to-current converter circuits are fundamental building blocks of analog circuit and systems. They are used in interface circuits, instrumentation amplifiers, and continuous-time-filters. When the transconductance is electronically variable they can also be applied in automatic, gain control circuits, and analog multipliers. Several techniques to improve the linearity performance of both bipolar and MOS transconductors have been proposed in the literature. For examples, the methods that are design based on the square-law characteristic of MOS transistors biased in saturation [1]-[2] and the methods that compensate the transistor nonlinearity with other transistor of the same type such as cross-coupling of multiple differential pair [2] or [3] adaptive biasing [4]. However, for all these techniques the reported transconductor linearity are limit to 40-60 dB

Although, in the past, the transconductance gain of OTAs can be electronically tuned by DC bias current. However, they are only bipolar OTAs. The main objective of this paper is, therefore, to present a new circuit design technique for the synthesis of an electronically and linearly tunable OTA based on CMOS technology. This includes the circuit description of the voltage-to-current transducer or general CMOS OTA that is design based on a linearizing technique, and we then employ the general CMOS OTA to construct the electronically and linearly tunable CMOS OTA, called as EOTA. The completed EOTA requires 3 general OTA's. These circuits generally use MOS transistors operating in the saturation region, and hence the individual functions of the circuits are derived from the approximate square-law characteristic of MOS transistors in saturation. Despite the non-linearities of the differential pair architecture due to non-linear drain and source current of MOSFETs, its transconductance is dependent on the DC bias current I_B. Thus, tunability of the differential pair architecture can be implemented by having a variable I_B.

Having access to such an electronically and linearly tunable CMOS OTA would enable a direct replacement of the bipolar OTA. Such an approach would then obviate the need for classical application-specific, the current-mode multiplier is described and measured results are shown to demonstrate the design flexibility of the approach. The circuit performances are studied through PSPICE simulation results.

2. Circuit Descriptions

For the purpose of the following analysis, we will assume that all MOS devices operate in the saturation region. This means that the transistor drain current I_D is characterized by a square-law model as

$$I_D = \begin{cases} K(V_{GS} - V_T)^2 & , \ for \ V_{GS} > V_T \\ 0 & , \ for \ V_{GS} \le V_T \end{cases} \qquad (1)$$

where the transconductance parameter $K = \mu_n C_{ox} W/2L$, μ_n is the mobility of the carrier, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length, and V_{GS} and V_T are the gate-to-source and threshold voltages, respectively.

2.1. An balanced CMOS OTA

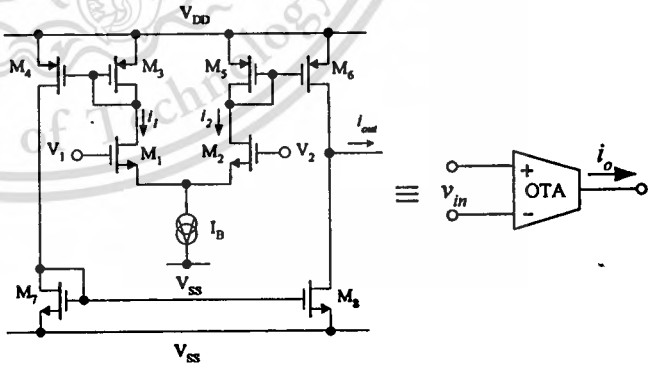

Figure 1. Schematic diagram of the balanced CMOS OTA

Figure 1 shows a balanced single-output CMOS OTA, which is formed by single-ended Voltage-to-Current Transducer (VCT) and current mirrors, where V_{in} is the differential input voltage ($V_{in}=V_1-V_2$), I_{out} is the output current and I_B is the bias current. Assuming M_1 and M_2 are perfectly matched and the current mirrors have a unity current gain. By using the square law of MOS transistor

operating in the saturation region, the differential output current in Figure 1 is given by [5]

$$i_{out} = i_1 - i_2$$

$$= \sqrt{2I_B K} \cdot V_{in} \cdot \sqrt{1 - \frac{KV_{in}^2}{2I_B}}, \quad for - \sqrt{\frac{I_B}{K}} \le V_{in} \le \sqrt{\frac{I_B}{K}} \quad (2)$$

The transconductance gain (gm) of the VCT can be derived by taking the derivative of (2) with respect to V_{in}, yielding

$$gm = \left. \frac{di_{out}}{dV_{in}} \right|_{V_{in}=0} = \sqrt{2I_B K} \quad (3)$$

We can written as

$$i_{out} = gmV_{in} = \sqrt{2I_B K} \cdot V_{in} \quad (4)$$

Equation (3) shows that the transconductance gain (gm) of the VCT can be varied by the bias current I_B.

2.2. An electronically and linearly tunable CMOS OTA

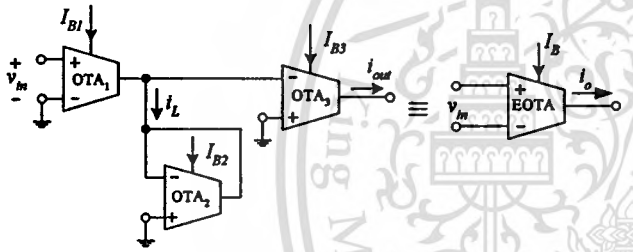

Figure 2. The proposed electronically and linearly tunable CMOS OTA

An electronically and linearly tunable CMOS OTA (EOTA) can be realized by the circuit diagram shown in figure 2, which is composed of three balanced single-output CMOS OTAs. The OTA$_1$ converts a differential input signal voltage $V_{in} = V_1 - V_2$ into a signal current i_L to flow into an active resistor Z_L, formed by the OTA$_2$, where $Z_L = 1/gm_2$ and gm$_2$ represents the transconductance gain of the OTA$_2$. Since the current signal $i_L = gm_1 V_{in}$, the voltage drop across the active resistor (OTA$_2$) becomes

$$V_L = i_L Z_L = gm_1 V_{in} \cdot \frac{1}{gm_2} \quad (5)$$

If gm$_3$ is the transconductance gain of the OTA$_3$, the OTA$_3$ will convert the voltage V_L into the output current i_{out} as

$$i_{out} = gm_3 V_L \quad (6)$$

From equations (5) and (6), the current i_{out} can be rewritten as

$$i_{out} = \frac{gm_1 gm_3}{gm_2} V_{in} \quad (7)$$

Since the transconductance gains $gm_1 = \sqrt{2I_{B1}K_1}$, $gm_2 = \sqrt{2I_{B2}K_2}$ and $gm_3 = \sqrt{2I_{B3}K_3}$, if we set I_{B1}=I_{B2}=I_B, then from equation (7) we obtain

$$i_{out} = \frac{2I_B\sqrt{K_1 K_3}}{\sqrt{2I_{B2}K_2}} V_{in} = gm_T V_{in} \quad (8)$$

where gm_T is the transconductance gain of the proposed EOTA and can be expressed as

$$gm_T = 2I_B K_T \quad (9)$$

and $K_T = \sqrt{K_1 K_3 / 2I_{B2} K_2}$, which can usually keep to constant. From the equation (9), we can clearly seen that the transconductance gain of the proposed EOTA can be electronically and linearly tuned by the bias current I_B.

2.3. Large signal analysis

The prediction of the equation 9 will valid only for a small value of V_{in}. For a large signal, the transconductance gain Gm from the equation (2) can be written as

$$Gm = \frac{i_{out}}{V_{in}} = \sqrt{2I_B K} \cdot \sqrt{1 - \frac{KV_{in}^2}{2I_B}}, for - \sqrt{\frac{I_B}{K}} \le V_{in} \le \sqrt{\frac{I_B}{K}} \quad (10)$$

If we set the error $E = \frac{KV_{in}^2}{2I_B}$, then equation (10) can be rewritten as

$$Gm = \frac{i_{out}}{V_{in}} = \sqrt{2I_B K} \cdot \sqrt{1 - E} \quad (11)$$

We found that the Gm will equal to the gm of equation (3) in the condition that $KV_{in}^2/2I_B << 1$. This can be achieved by keep the input voltage signal V_{in} small or set the DC bias current I_B to a large value.

As similar to the small signal analysis, we obtain the transconductance gain of the proposed EOTA in large signal (Gm) as

$$Gm_T = 2I_B K_T \left(1 + \frac{\sqrt{1-E_1}\sqrt{1-E_3} - \sqrt{1-E_2}}{\sqrt{1-E_2}} \right) \quad (12)$$

where the errors $E_1 = \frac{K_1 V_{in1}^2}{2I_{B1}}$, $E_2 = \frac{K_2 V_{in2}^2}{2I_{B2}}$ and $E_3 = \frac{K_3 V_{in3}^2}{2I_{B3}}$ are due to the OTA$_1$, OTA$_2$ and OTA$_3$

respectively. Given that E_T is the conversion error from the linear transconductance gain, where

$$E_T = \frac{\sqrt{1-E_1}\sqrt{1-E_3}-\sqrt{1-E_2}}{\sqrt{1-E_2}} \quad (13)$$

Thus, we have the percent of the conversion error as

$$\%E_T = \frac{\sqrt{1-E_1}\sqrt{1-E_3}-\sqrt{1-E_2}}{\sqrt{1-E_2}} \times 100\% \quad (14)$$

For example, if $V_{in1} = 0.5V$, $V_{in2} = V_{in3} = 0.751V$, $I_{B1} = I_{B3} = 1mA$, $I_{B2} = 880\,\mu A$ and $K_1 = K_2 = K_3 = 1.27\times10^{-4}$, the resulting conversion error ($\%E_T$) is equal to 0.54%

3. Application

In this section, we will propose the use of the EOTA to realize a current-mode multiplier, which use only active circuit elements but not require external passive circuit elements. The proposed current-mode multiplier circuit is shown in Figure 3 [6]. It should be noted from the equation (9) that if the EOTA is operated in the linear ranges, the transconductance is $gm_T = 2I_B K_T$, which gm_T can be tuned by the DC bias current I_B.

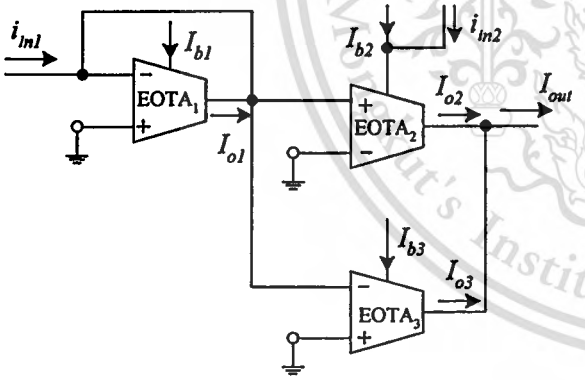

Figure 3. The current-mode multiplier circuit using the proposed EOTA.

From the Figure 3, the input signal current i_{in1} is injected into the EOTA$_1$, which is connected as a current controlled grounded resistor. The voltage across the EOTA$_1$ is then used as the input voltage for the EOTA$_2$ and EOTA$_3$. The input signal current i_{in2} is added with the bias current I_{B2} of the EOTA$_2$. Let gm_{T1}, gm_{T2} and gm_{T3} be the transconductance gains of the EOTA$_1$, EOTA$_2$ and EOTA$_3$, respectively. Then from the equation (9) and from routine circuit analysis the output currents I_{o2} and I_{o3} of the EOTA$_2$ and EOTA$_3$, respectively can be written as

$$I_{o2} = \frac{gm_{T2}}{gm_{T1}} i_{in1} = \frac{(I_{b2}+i_{in2})}{I_{b1}} i_{in1} \quad (15)$$

and

$$I_{o3} = -\frac{gm_{T3}}{gm_{T1}} i_{in1} = -\frac{I_{b3}}{I_{b1}} i_{in1} \quad (16)$$

where I_{b1}, I_{b2} and I_{b3} represent the DC bias current of the EOTA$_1$, EOTA$_2$ and EOTA$_3$, respectively, and the transconductance gains $gm_{T1} = 2I_{b1}K_{T1}$, $gm_{T2} = 2(I_{b2}+i_{in2})K_{T2}$ and $gm_{T3} = 2I_{b3}K_{T3}$. Noting from the Figure 2 and Figure 3, that the DC bias current of the EOTA (I_b) of the multiplier circuit can be achieved by setting the DC bias currents of the OTA$_1$ and the OTA$_2$ to $I_b = I_B = I_{B1} = I_{B3}$. If we set $I_{b2} = I_{b3} = I_b$, the output current I_{out} of the circuit that is the summation of the currents I_{o2} and I_{o3} can be expressed as

$$I_{out} = I_{o2} + I_{o3} = \frac{i_{in1} i_{in2}}{I_{b1}} \quad (17)$$

which is in the form of a current-mode multiplication function.

4. Simulation Results

The performance of the proposed electronically and linearly tunable CMOS OTA was verified through the use of PSPICE simulation results. All the VCT was simulated by using CMOS transistor parameters of the SCN2 level 2 of MOSIS [7]. The transistor dimensions of the circuit in Figure1 are in micron, where the dimensions of the transistors M1 and M2 are W=50μm and L=10μm, the dimensions of the transistor M3-M8 are W=100μm and L=10μm. The power supply voltage were set to $V_{DD} = -V_{SS} = \pm 5V$.

To demonstrate that the circuit can linearly converted voltage signal into current signal, Figure 4 shows the DC characteristic of the I_{out} versus V_{in} of the proposed circuit in Figure 3 for the cases of the dc bias current (I_B) of 1mA, 800μA and 400μA, respectively. The results show that the transconductance are almost constant and the nonlinearity are seen to be less than 1% for the input voltage (V_{in}) range from -1V to 1V, -0.86V to 0.86V and -0.66V to 0.66V respectively. These results were agreed with the predicted transconductance from equation (10).

The relation between the transconductance and the bias current I_B was measured by fixing $V_{in} = 0.1V$ and varying I_B from 10nA to 1mA. The results are plot in Figure 5. From this, it can be seen that the transconductance is linearly dependent upon the bias current I_B over the range of 1μA to 1mA (three decades). We found that the transconductace can be tune linearly by I_B, where at I_B=1mA the conversion error from simulation result is about 0.68%.

The lower limit of the circuit is due to condition in equation (2) that transistors must be operating in saturation region. In the cases of V_{in} = 0.1V, 0.2V and 0.5V, respectively, we found that the DC bias current I_B must be more than 1μA, 5μA and 32μA respectively.

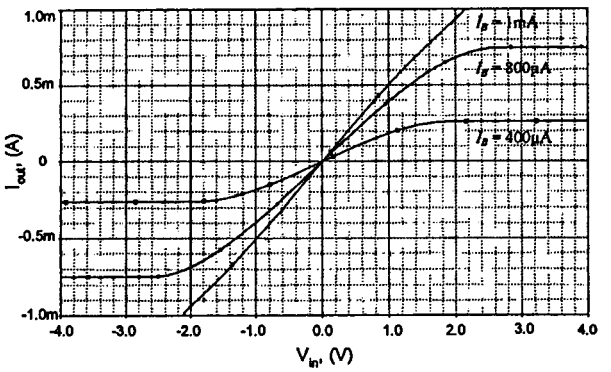

Figure 4. DC transfer characteristics of the proposed circuit

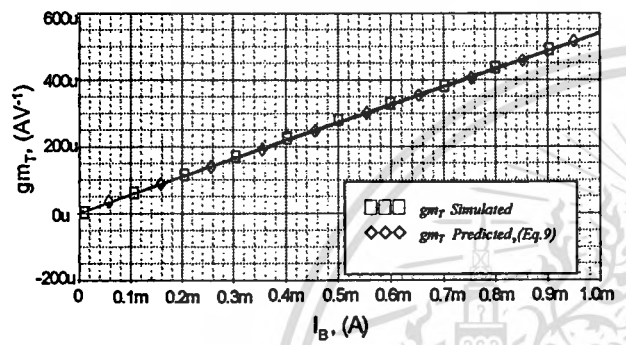

Figure 5. Linear range tunable transconductance characteristic

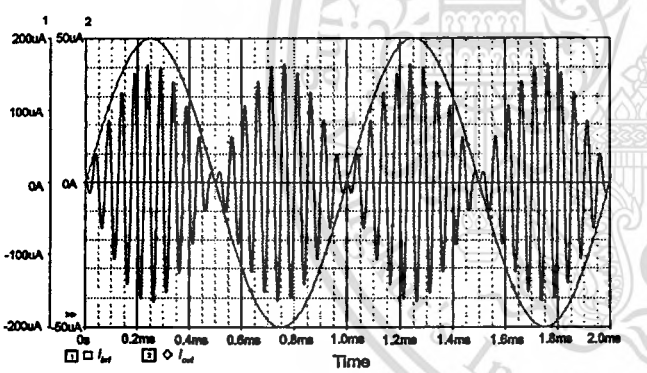

Figure 6. Simulated transient response for the multiplier circuit

Accordingly these limits were agreed very well with the prediction of CMOS are operating in saturation region from equation (2). At the DC bias current I_B = 1mA, in the case of *Vin* = 0.5V, I_{B2} = 880uA, the result shows that the transconductance gain $g_{mT} = 5.398 \times 10^{-4}$ AV^{-1} is achieved. The conversion error from the simulation result is about 0.5%, this results were agree with the conversion error predicted from eq.(14).

The multiplier circuit of Figure 3 was tested by multiplying two sinusoidal signals. The results obtained are shown in Figure 6 for $i_{in1} = 0.2\sin(2\pi 1000t)$ mA, $i_{in2} = 0.2\sin(2\pi 20000t)$ mA and I_{b1}= 1mA. The DC transfer characteristics of the multiplier circuit were also observed by setting the bias currents I_{b1}= I_{b2}= I_{b3}= 1mA, and the input current i_{in1} and i_{in1} are varied from -200μA to 200μA with 100μA per step. The results show that the simulated and calculated data are agreed very well over the ± 190μA input range with error of less than 1%.

5. Conclusions

A design of the electronically and linearly tunable CMOS OTA has been proposed. The conversion circuit composed of three general CMOS OTAs. The achieve characteristics of the proposed circuit were similar as the bipolar OTA that the transconductance gain (*Gm*) can be linearly tuned by the DC bias current. Simulation results have been employed to demonstrate the performances of the proposed EOTA. Moreover to confirm that EOTA can be replacing the bipolar OTA, the current-mode multiplier circuit was used to display the performances of the proposed circuit.

6. Acknowledgements

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A design of CMOS tunable current amplifiers

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ABSTRACT: Two CMOS tunable current amplifiers are proposed in this paper. They are voltage-controlled current gain and current-controlled current gain. Both circuits are designed based on CMOS OTA which amplifiers are linearly tunable. The circuits achieve their linearity by squaring the nonlinear transconductance of the balanced CMOS OTA. The proposed voltage-controlled current amplifier can be linearly tuned by DC voltage. The amplifier's nonlinearity is less than 1% for the voltage control (V_C) range from -2V to 2V. The current-controlled current amplifier can also have a linearly-tunable current gain by DC bias current over three decades (0.1-20) with an error less than 1.5%. The performances of the proposed circuit are discussed and confirmed through PSPICE simulation.

1. Introduction

Bipolar current amplifier is a useful circuit building block. Since it provides wide-band open-loop linear current gain, it can be used in open-loop amplifiers to achieve very high gain-bandwidth (GB) products [1]. Although, in the past, the current amplifier can be electronically tuned by DC bias current, they can be designed only in bipolar technology. Recently CMOS current gain cells with similar features have been proposed, however, with the gain is proportional to $\sqrt{K}$ or/and to $\sqrt{I_C}$ [2]- [4].

The main objective of this paper is, therefore, to present a new circuit design technique for the synthesis of CMOS tunable current amplifiers: a linear voltage-controlled current amplifier and a linear current-controlled current amplifier. This includes the circuit description of the voltage-to-current transducer or general CMOS OTA that is design based on a linearizing technique, which gives the CMOS-Based Electronically and Linearly Tunable OTA (EOTA) [5]. We then employ the general CMOS OTA and EOTA to construct the tunable current amplifiers. The gains of the voltage-controlled current amplifier and current-controlled current amplifier can be linearly tune by DC voltage (V_C) and DC bias current (I_B) respectively.

The measured results demonstrate the design flexibility of the approach. The circuit performances are studied through PSPICE simulation.

2. Circuit Descriptions

We will assume that all MOS devices operate in the saturation region. This means that the transistor drain current I_D is characterized by a square-law model as

$$I_D = \begin{cases} K(V_{GS} - V_T)^2 & , \text{ for } V_{GS} > V_T \\ 0 & , \text{ for } V_{GS} \le V_T \end{cases} \quad (1)$$

where the transconductance parameter $K = \mu_n C_{ox} W/2L$, μ_n is the mobility of the carrier, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length, and V_{GS} and V_T are the gate-to-source and threshold voltages,respectively.

2.1. A balanced CMOS OTA

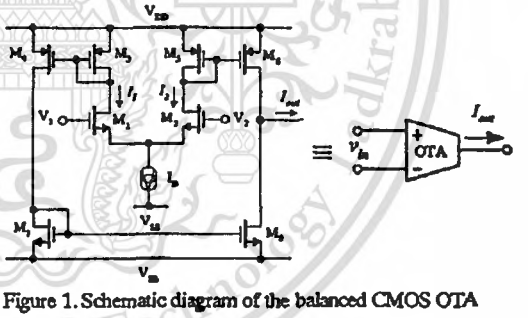

Figure 1. Schematic diagram of the balanced CMOS OTA

Figure 1 shows a balanced single-output CMOS OTA, which is formed by single-ended Voltage-to-Current Transducer (VCT) and current mirrors, where v_{in} is the differential input voltage ($v_{in}=v_1-v_2$), I_{out} is the output current and I_B is the bias current. Assuming that M_1 and M_2 are perfectly matched and the current mirrors have unity current gain and using the square law of MOS transistor operating in the saturation region, the differential output current of the circuit of Figure 1 can be given by [5]

$$I_{out} = I_2 - I_1$$

$$= \sqrt{2I_B K}\cdot v_{in}\cdot\sqrt{1-\frac{Kv_{in}^2}{2I_B}} \quad , \text{for } -\sqrt{\frac{I_B}{K}} \le v_{in} \le \sqrt{\frac{I_B}{K}} \quad (2)$$

The transconductance (g_m) of the VCT can be derived by taking the derivative of (2) with respect to v_{in} yielding

$$g_m = \left.\frac{dI_{out}}{dv_{in}}\right|_{v_{in}=0} = \sqrt{2I_B K} \qquad (3)$$

Thus we can obtain the following equation for a small signal;

$$i_{out} = g_m v_{in} = \sqrt{2I_B K}\cdot v_{in} \qquad (4)$$

Equation (3) shows that the transconductance gain (g_m) of the VCT can be varied by the bias current I_B, but in the form of square root function.

2.2. CMOS-Based Electronically and Linearly Tunable OTA (EOTA) [5]

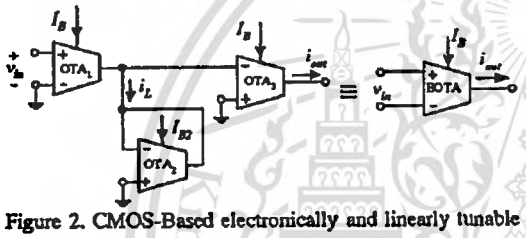

Figure 2. CMOS-Based electronically and linearly tunable OTA (EOTA)

A CMOS-Based electronically and linearly tunable OTA (EOTA) can be realized by the circuit diagram shown in figure 2, which is composed of three balanced single-output CMOS OTAs. The OTA_1 converts a differential input signal voltage $v_{in} = v_1 - v_2$ into a signal current i_L flowing into an active resistor Z_L formed by the OTA_2, where $Z_L = 1/g_{m2}$ and gm_2 represents the transconductance of the OTA_2. Since the current signal $i_L = g_{m1}v_{in}$, the voltage across the active resistor (OTA_2) becomes

$$v_L = i_L Z_L = g_{m1}v_{in}\cdot\frac{1}{g_{m2}} \qquad (5)$$

If g_{m3} is the transconductance of the OTA_3, the OTA_3 will convert the voltage v_L into the output current i_{out} as

$$i_{out} = g_{m3}v_L \qquad (6)$$

From equations (5) and (6), the current i_{out} can be rewritten as

$$i_{out} = \frac{g_{m1}g_{m3}}{g_{m2}}v_{in} \qquad (7)$$

Where the transconductances are given by $g_{m1} = \sqrt{2I_{B1}K_1}$, $g_{m2} = \sqrt{2I_{B2}K_2}$ and $g_{m3} = \sqrt{2I_{B3}K_3}$. If we set $I_{B1}=I_{B3}=I_B$, then from equation (7), we obtain

$$i_{out} = \frac{2I_B\sqrt{K_1K_3}}{\sqrt{2I_{B2}K_2}}v_{in} = g_{mT}v_{in} \qquad (8)$$

where g_{mT} is the transconductance gain of the proposed EOTA and can be expressed as

$$g_{mT} = 2I_B K_T \qquad (9)$$

and $K_T = \sqrt{K_1K_3/2I_{B2}K_2}$. The equation (9) clearly indicates that the transconductance of the EOTA can be electronically and linearly tuned by the bias current I_B, which is similar to the transconductance of the bi-polar based OTA.

3. CMOS Tunable Current Amplifiers

In this section, the realization of the current amplifiers by using EOTA, which use only active circuit elements, are described.

3.1 Linearly voltage-controlled current amplifier

The proposed voltage-controlled tunable current amplifier is constructed as the circuit diagram in figure 3, which consists of the EOTA in figure 2. Where the input signal current (i_{in}) is added to the DC bias current (I_B). The control voltage (V_C) is supplied to the input of EOTA. From the routine circuit analysis of figure 3, the output current (i_{out}) can be expressed as

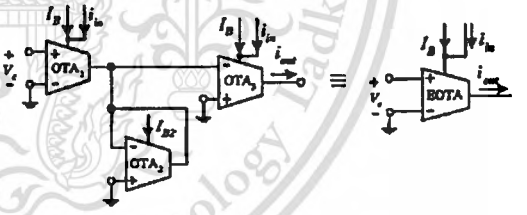

Figure 3. A linearly voltage-controlled Current Amplifier

$$i_{out} = 2K_T V_C\left(i_{in} + I_B\right) \qquad (10)$$

$$i_{out} = \left(2K_T V_C\right)i_{in} + \left(2K_T V_C\right)I_B \qquad (11)$$

From the equation (11), we found that the output current consists of the AC signal and DC current ($2K_TV_C\cdot I_B$). If we compensate this DC current, the output current of the voltage controlled current amplifier can be rewritten as

$$i_{out} = \left(2K_T V_C\right)i_{in} = A_i i_{in} \qquad (12)$$

Where A_i is the current gain of the proposed voltage controlled current amplifier and can expressed as

$$A_i = 2K_T V_C \qquad (13)$$

and $K_T = \sqrt{K_1 K_3 / 2I_{B2} K_2}$. We can see that the output current can be tuned linearly by the DC voltage V_C.

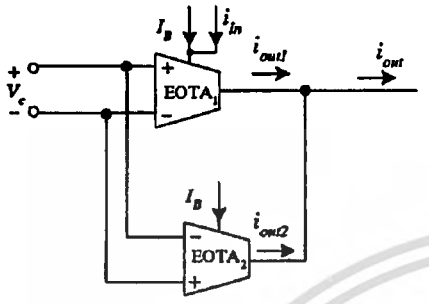

Figure 4. Schematic diagram of the current amplifier with DC gain compensated

Figure 4. shows the circuit building block to eliminate the DC current of figure 3. i_{out1} and i_{out2} are given as,

$$i_{out1} = (2K_T V_C) i_{in} + (2K_T V_C) I_B \quad (14)$$

and

$$i_{out2} = -(2K_T V_C) I_B \quad (15)$$

The output current i_{out} of the circuit, that is the summation of the currents i_{out1} and i_{out2}, can beexpressed as

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$$i_{out} = i_{out1} + i_{out2} = (2K_T V_C) i_{in} \quad (16)$$

From equation (16) it is clearly seen that the circuit can operate as a current amplifier, the gain of which can be linearly tuned by control voltage (V_C).

3.2 Linearly current-controlled CMOS current amplifier

A current amplifier design based on EOTA that can electronically and linearly be tunable is proposed in figure 5.

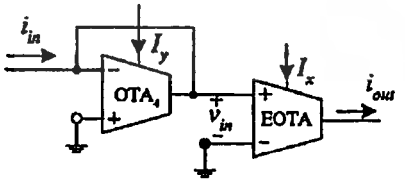

Figure 5. A linearly current-controlled tunable current amplifier

A linearly current-controlled current amplifier design based on EOTA is shown in figure 5, which is composed of one balanced single-output CMOS OTA and one EOTA. The input current (i_{in}) is injected into the OTA$_4$, which is aform as an active resistor ($1/g_{m4}$). The voltage drop across the active resistor (OTA$_4$) is then used as an input voltage (v_{in}) for EOTA and can be expressedas

$$v_{in} = \frac{i_{in}}{g_{m4}} \quad (17)$$

The EOTA will convert the voltage v_{in} into the output current i_{out} as

$$i_{out} = g_{mT} v_{in} \quad (18)$$

From equations (17) and (18), the current i_{out} of the propose current-controlled current amplifier canbe written as

$$i_{out} = \frac{g_{mT}}{g_{m4}} i_{in} \quad (19)$$

where $g_{mT} = g_{m1} g_{m3} / g_{m2}$, $g_{m1} = \sqrt{2I_{B1} K_1}$, $g_{m2} = \sqrt{2I_{B2} K_2}$, $g_{m3} = \sqrt{2I_{B3} K_3}$ and $g_{m4} = \sqrt{2I_{B4} K_4}$. If we set $K_1 = K_2 = K_3 = K_4 = K$ and $I_{B4} = I_{B2} = I_y$, $I_{B1} = I_{B3} = I_B = I_x$, then from equation (19) we obtain

$$i_{out} = \frac{g_{m1} g_{m3}}{g_{m2} g_{m4}} i_{in} \quad (20)$$

Since

$$i_{out} = \frac{I_x}{I_y} i_{in} = A_C i_{in} \quad (21)$$

where A_C is the current gain of the proposed current amplifier and can be expressed as

$$A_C = \frac{I_x}{I_y} \quad (22)$$

We can see that the output current can be tuned by the DC bias current I_x and I_y. This indicates the gain is proportional to I_x and I_y.

4. Simulation Results

The performance of the proposed current amplifiers were verified through the PSPICE simulation. All the balanced CMOS OTAs were simulated by using CMOS transistor parameters of the SCN2 level 2 of MOSIS. The dimensions of transistors M1 and M2 are W=50μm and L=10μm, the dimensions of the transistor M3-M8 are W=100μm and L=10μm. The power supply voltages were set to $V_{DD} = -V_{SS} = 5V$.

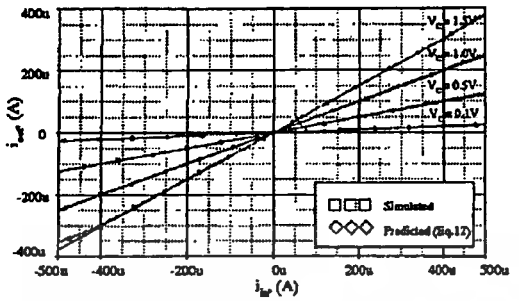

Figure 6. The current transfer characteristic of the voltage controlled current amplifier

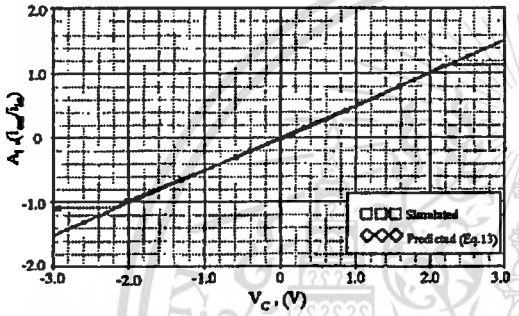

Figure 7. The performance of gain controllability of the voltage controlled current amplifier

For the linearly voltage-controlled current amplifier in figure 3, we set I_B= 600μA and I_{B2}=1mA. Figure 6 shows the current transfer characteristic of the proposed voltage controlled current amplifier. This figure shows the plot of the output current i_{out} against the input current i_{in} from -500μA to 500μA for different V_c values; V_c = 0.1V, 0.5V, 1V and 1.5V. The simulation and calculated data are agreed very well, for example at V_c = 0.5V, over the ±500μA input range, error was less than 1.5%.

Figure 7. represents plots of the variation of current gain $A_i = i_{out}/i_{in}$ versus the control voltage V_c in the case of i_{in}=10μA. It is seen that both results of simulation and calculation are in good agreement. The nonlinearity is seen to be less than 1% for the control voltage (V_c) range from -2V to 2V.

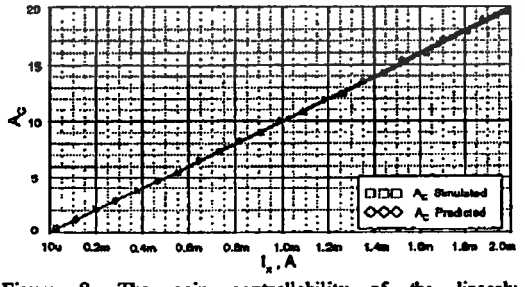

Figure 8. The gain controllability of the linearly current-controlled current amplifier

The gain and the controllability of the proposed current-controlled current amplifier in figure 5 obtained by simulation and calculation are shown in figure 8, for I_x from 10μA to 2mA where I_y is keep constant 100μA. It is seen that both results are in good agreement. At I_x = 2mA the conversion error is less than 1.5%. We found that the current gain (A_C) can be electronically and linearly tune from 0.1 to 20 (3 decade).

5. Conclusions

The CMOS tunable current amplifiers have been proposed in this paper. The achieved characteristics of the proposed current-controlled current amplifier are similar to the bipolar OTA as the current gain can be linearly tuned by DC bias current (I_B). In addition, the voltage-controlled current amplifier can also be linearly tuned by the DC voltage (V_C). The simulation results ensure our proposed technique and demonstrate the performances of the proposed circuit.

6. Acknowledgements

This work was funded by the Thailand Research Fund (TRF) under the Senior Research Scholar Program, grant number RTA4680003 and financial support from the Thailand Research Fund through the Royal Golden Jubilee Ph.D. Program (Grant No.PHD/0107/2546) Khanittha Kaewdang and Wanlop Surakampontorn acknowledge these supports.

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A REALIZATION OF SIMPLE CURRENT-MODE CMOS BASED TRUE RMS-TO-DC CONVERTER

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ABSTRACT

A simple circuit technique for the realization of an integrable current-mode CMOS true rms-to-dc converter is proposed. The realization scheme is based on the implicit computation method by makes use of the characteristic of a CMOS squaring circuit. Since the bias current of the circuit is provided by the I_{RMS}, the conversion circuit consumes very low power. The performance of the circuit is studied through spectre in Cadence simulation results and experimental results.

1. INTRODUCTION

A true rms-to-dc converter is an instrument that used for measuring the average energy content in an electrical signal. This device found useful in the fields of instrumentation, communication and display systems [1]. In the past, many true rms-to-dc converters that based on bi-polar integrated circuit technology are available [2]. Their conversion schemes are mostly performed through the use of a full-wave rectifier and a multiplier/divider circuit that employing a log-antilog principle. Due to the bandwidth and the slew-rate of the full-wave rectifiers, the useful frequency range of these converters is limited to less than 5 MHz. New design techniques based on bipolar dynamic translinear circuits have been proposed to implement true rms-to-dc converters [3]. Unfortunately, the characteristics of the rms-to-dc conversion circuits have not been reported but only circuit descriptions are outlined. In addition, their circuits are operated in only one quadrant and require full-wave rectifiers. Recently, a new design technique for rms-to-dc converter that design around a dual translinear-base squarer circuit is proposed [4], where the input current can be a two-quadrant current. Because the full-wave rectifier is not required by this conversion scheme, the circuit exhibits a wide bandwidth. However, the implementation scheme is rather complicate and suitable for bipolar technology. In this paper, through the use of a MOS transistor square law characteristic, a design technique for the realization of a true rms-to-dc converter is proposed. The conversion circuit performs the implicit computation scheme, by feedback the root-mean square current to be the circuit bias current. A full-wave rectifier is not required by the proposed realization scheme. The conversion circuit is simple, suitable for implementing in monolithic integrated form, and can be readily integrated as part of a larger system. The performance of the conversion circuit is studied through spectre in Cadence simulation results and through the experimental results from the fabricated 0.5 micron CMOS technology chip.

2. CIRCUIT DESCRIPTIONS

2.1 Squaring Circuit

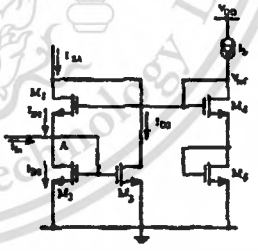

Figure 1. A CMOS current squaring circuit.

Let us assume that the operation of the circuit in Fig.1 is based on the square law characteristic of MOS transistors biased in the strong inversion region [4]. Transistors M_1 through M_3 function as a current squarer, where M_4 and M_5 and the current source I_b formed as the current-controlled bias circuit. The input signal current I_{in} is injected into point A. If I_{D1} and I_{D2} are the drain currents of M_1 and M_2, respectively, the currents I_{D1} and I_{D2} can be respectively written as

$$I_{D1} = \frac{(4I_b - I_{in})^2}{16I_b} \qquad \text{for } |I_{in}| \le 4I_b \qquad (1)$$

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$$I_{D2} = \frac{(4I_b + I_{in})^2}{16I_b} \qquad \text{for } |I_{in}| \le 4I_b \qquad (2)$$

The unity gain positive current mirror CM_1, formed by transistors M_2 and M_3, reflects the current I_{D2} in order to add with the current I_{D1}. Then, from eqns. (1) and (2), the summation of the currents I_{D1} and I_{D2} or $I_{S4} = I_{D1}+I_{D2}$ becomes

$$I_{S4} = \frac{I_{in}^2}{8I_b} + 2I_b \qquad (3)$$

We can see that I_{S4} consists of the signal current that is the squaring of the input signal I_{in} and the DC current $2I_b$. If the DC current $2I_b$ can be compensated, the circuit will be functioned as a squarer/divider circuit, which can be used as a basic cell to realize rms-to-dc converter by the implicit computation method.

2.2. The proposed true rms-to-dc converter

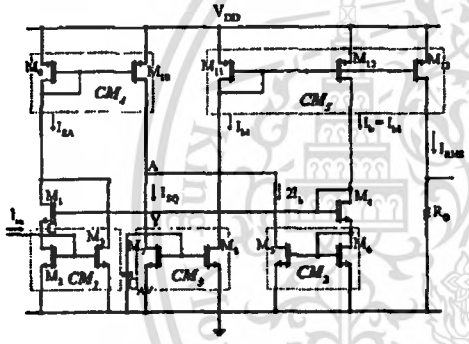


Figure 2. The proposed true rms-to-dc converter.

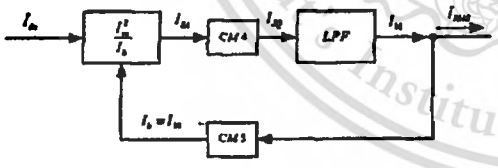


Figure 3. Block diagram representation of the true rms-to-dc converter.

Fig. 2 shows the proposed true rms-to-dc converter, which is composed of the squaring circuit in Fig.1 in combination with four current mirrors, CM_2 through CM_5. The circuit is constructed such that the drain current of the transistor M_5 of the current mirror CM_2 sources the current $2I_b$ from the current I_{S4}. Then from the eqn.(3) and the Fig.2, the current I_{SQ} can be expressed as

$$I_{SQ} = \frac{I_{in}^2}{8I_b} \qquad (4)$$

In the figure, the current I_{SQ} passes through the averaging circuit or the first-order current mode low-pass filter, which is consisting of the current mirror CM_3 (M_7 and M_8) and the grounded capacitor C_{AV} connected parallel to the mirror input. The output current of the filter I_{bl} can be written as

$$I_{bl} = \frac{1}{8I_b\tau}\int I_{in}^2 dt \qquad (5)$$

where $\tau = C_{AV}/g_{m7}$ is the time constant of the filter and g_{m7} is the transconductance of the transistor M_7. Due to the unity gain current mirrors CM_3 (M_7 and M_8) and CM_5 (M_{11} and M_{12}), the bias current I_b is derived by the current I_{bl} such that

$$I_b = I_{bl} \qquad (6)$$

At the output, since we set the transistor channel widths of the current mirror CM_5 as $W_{12} = \sqrt{8}\, W_{11}$, this means the output current

$$I_{RMS} = \sqrt{8} I_b \qquad (7)$$

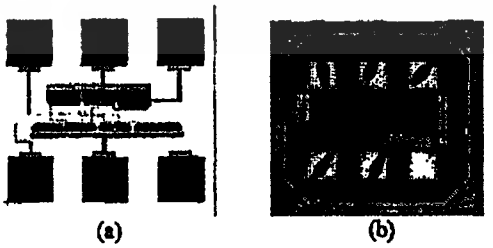
From eqn. (5) and since $I_b = I_{bl}$, then by solving for I_b, we can write

$$I_b = \frac{1}{\sqrt{8}}\sqrt{\frac{1}{\tau}\int I_{in}^2 dt} \qquad (8)$$

From eqns. (7) and (8), by solving for I_{RMS}, we get

$$I_{RMS} = \sqrt{\frac{1}{\tau}\int I_{in}^2 dt} \qquad (9)$$

The output current I_{RMS} is in the form of the root-mean-square value. It should be noted from the eqns. (4)-(9) that the square root function is achieved by the feedback of the current I_{bl} to be the bias current I_b of the circuit. Therefore, the conversion circuit of Fig. 2 can be represented by the block diagram as shown in Fig. 3. The layout and microphotograph, fabricated in a 0.5 microns CMOS Technology AMIS process with Vth≅ 0.7V, of the proposed true rms-to-dc converter are shown in Figure 4. The total chip area occupied, excluding the bonding pads, was 484x442 micron^2.



(a) (b)

Figure 4. The True RMS-to-DC Converter: (a) The layout and (b) Microphotograph.

In order that the proposed rms-to-dc converter gives a good performance in the required frequency range, the value of the capacitor C_{AV} must be chosen such that [5]

$$C_{AV} >> g_{m7(MAX)}/4\pi f_{(MIN)} \qquad (10)$$

where $f_{(MIN)}$ is the lower end of the frequency range of interest and

$$g_{m7(MAX)} = \sqrt{2K_p I_{SQ} W_7/L_7} \qquad (11)$$

W_7 is channel width and L_7 is channel length, of the transistor M_7. From eqn. (4) the $g_{m7(MAX)}$ can be express as

$$g_{m7(MAX)} = \sqrt{2K_p I_M^2 W_7/8I_b L_7} \qquad (12)$$

where I_M is the peak amplitude of the input signal I_{in} and I_b is the circuit bias current. For example, for $K_P = 7.19\times10^{-5}$ A/V^2 and $W_7/L_7 = 8$, then $g_{m7(MAX)}$ can be given by

$$g_{m7(MAX)} = 0.0339\sqrt{\left(I_M^2/8I_b\right)} \qquad (13)$$

In this case, C_{AV} must be chosen such that

$$C_{AV} >> (9.538\times10^{-4})I_M/\sqrt{I_b f_{(MIN)}} \qquad (14)$$

Noting that the value of C_{AV} chosen is much depending on the ripple error that can be tolerate at the output. As a rule of thumb, the value of C_{AV} should exceed the right-hand term of eqn. (14) by the inverse of the fractional ripple error. For instance, for a 1 percent ripple error, C_{AV} should be about 1/0.01 or 100 times as large as the right-hand term. For example, for a sinusoidal input signal with I_M = 1 mA, $f_{(MIN)}$ = 100 Hz ,and the ripple error of 5 percent, then the averaging capacitance of C_{AV} = 10μF must be chosen.

3. SIMULATON AND EXPERIMENTAL RESULTS

The performance of the circuit has been studied through simulation and experimental results. The simulation has been carried out by employing spectre in Cadence simulation program and using the transistor parameters of the 0.5 microns CMOS Technology AMIS process. The transistor dimensions of the circuit in Figure2 are in micron, where the dimension of the transistors M5 is W=80µm and L=5µm, M13 is W=283µm and L=5µm , M1-M4, M6 are W=40µm and L=5µm and M9-M12 are W=100µm and L=5µm . The power supply voltage were set to V_{DD}=5V.

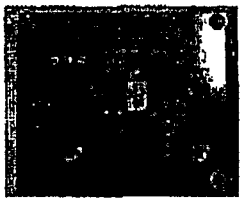


Figure 5 True rms-to-dc converter measurement setup

Employing the chip of the Fig.4, the measurement setup is shown in Figure 5. The external capacitor C_{AV} is 10 µF. Due to the proposed rms-to-dc converter operates in current mode, a commercially available current conveyor CCII01 was used to convert the input voltage V_{in} into the input current signal I_{in}. The resistor R_{in}=1kΩ is connected at ports X and the input voltage was applied to the port Y of the CCII. For example, by setting the input signal current of I_{in} = 1mA$_{(peak)}$, the input voltage equal to 1V is applied to port Y of the CCII. To measure the value of the I_{RMS}, a resistor of 1kΩ was connected at the output of the rms-to-dc converter and the voltage across the resistor R_o is measured instead.

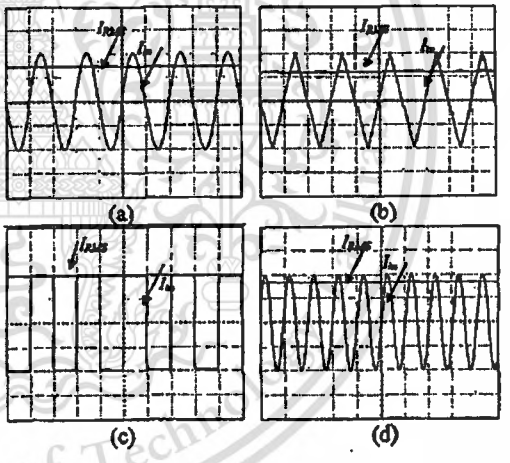


Figure 6 Experimental results for the input signals: (a) sinusoidal; (b) triangular; (c) square wave; (Vertical scale: 0.5V/div. Horizontal scale: 5us/div) and (d) sinusoidal. (Vertical scale: 0.5V/div. Horizontal scale: 200ns/div)

The experimental results in Fig. 6(a), 6(b) and 6(c) show the I_{RMS} for the input signal of sinusoidal, triangular and square waveforms, respectively, with the peak amplitude of 1mA and with the frequency of 100 kHz. The I_{RMS} signal with the amplitude close to 0.7mA, 0.5mA, and 1mA, respectively, with the error of less than 10µA, were achieved. These results demonstrated that the circuit can be accurately converted the AC signals into DC signals into the rms values. To demonstrate that the circuit can operate in a wide frequency range, Fig.6(d) shows the measured I_{RMS} for the cases of the sinusoidal

input signal with the frequencies of f = 5MHz, and with the peak amplitude of 1mA. The results show that the I_{RMS} signals with the amplitude of about 0.7mA are achieved. The dc error from the simulation results is about 12%.

We can notice that the ripple at low frequencies, i.e. f = 100Hz, is higher than the high frequency. This is due to that, in this case, the capacitor C_{AV} is selected for f_{MIN} = 100Hz. Owing to that the ripple can not accurately be measured from the experimental results, therefore, we will study through the simulation result, the % ripple is calculated by

$$\%\,\text{ripple} = (I_{ripple(p\text{-}p)}/I_{DC}) \times 100\% \qquad (27)$$

where $I_{ripple(p\text{-}p)}$ is the peak to peak amplitude of the output current and I_{DC} is the DC component of the output current. From the simulation results at f = 100 Hz, 100kHz and 5 MHz, the output signal have percent ripple error of about 3% , 1.35% and 0.0001%, respectively.

The high frequency performance was studied through cadence simulation. The simulation results for the –3dB bandwidth with the peak input current ranging from I_{in} = 100μA to 1500μA were summarized in the Table 3.

The experimental results to demonstrate the linearity of the rms-to-dc converter are shown in Fig.7. The transfer characteristic are the plot of the I_{RMS} against the input signal current I_{in} with the peak amplitude varied from 300μA to 1.5mA, for the sine, triangular and square waveforms. The signal frequencies are 1kHz and C_{AV}=10μF. We found that the maximum conversion nonlinearity of about 2% was achieved. The lower limit of the circuit is due to the fact that the I_{RMS} is feedback to be the bias I_b of the circuit. Therefore, through I_b, the I_{RMS} should be large enough to bias all the transistors in their saturation regions.

Table 3. Performance of the rms-to-dc converter.

Parameters	Simulated Results
Supply voltage (rated)	1.5-5V
Input current range (MAX)	1.5mA
Power Dissipated	0.1mW
Gain error	2% Max. nonlinearity, 100 μA to 1.5mA input
Peak amplitude value	-3 dB bandwidth
I_{in} = 100 μA	20 MHz
I_{in} = 200 μA	40 MHz
I_{in} = 500 μA	60 MHz
I_{in} = 900 μA	85 MHz
I_{in} = 1000 μA	90 MHz
I_{in} = 1500 μA	100 MHz

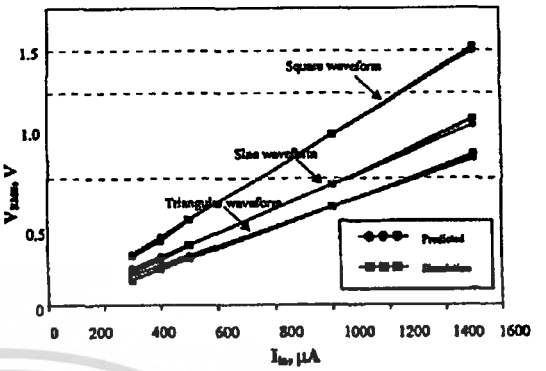


Figure 7. DC transfer curves of the rms-to-dc converter.

4. CONCLUSIONS

We have developed a simple CMOS true rms-to-dc converter circuit. The realization scheme is based on the implicit computation method and is suitable for implemented in standard CMOS process. The circuit is suitable for all input wave forms. The circuit has fabricated in a 0.5 microns CMOS Technology AMIS process with Vth ≅ 0.7V. The characteristics of the proposed are confirmed by the experimental results and the cadence simulation results.

5. ACKNOWLEDGEMENTS

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