DESIGNS OF HALF-WAVE AND FULL-WAVE RECTIFIERS USING CURRENT CONVEYORS

ADISAK MONPAPASSORN

King Mongkut's Institute of Technology Ladkrabang

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หัวข้อวิทยานิพนธ์ การออกแบบวงจรเร็คติฟายเออร์แบบครึ่งคลื่นและเต็มคลื่นโดยใช้วงจรสายพานกระแส

นักศึกษา นาย อดิศักดิ์ มนต์ประภัสสร

รหัสประจำตัว 41060002

ปริญญา วิศวกรรมศาสตรดุษฎีบัณฑิต

สาขาวิชา วิศวกรรมไฟฟ้า

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บทคัดย่อ

การสร้างวงจรเร็คติฟายเออร์แบบครึ่งคลื่นและเต็มคลื่นโดยใช้วงจรสายพานกระแสถูกนำเสนอในวิทยานิพนธ์ฉบับนี้ วงจรเร็คติฟายเออร์ที่นำเสนอประกอบด้วย วงจรเปลี่ยนแรงดันเป็นกระแส วงจรเร็คติฟายเออร์กระแส และวงจรเปลี่ยนกระแสเป็นแรงดัน สัญญาณอินพุตที่เป็นแรงดันถูกเปลี่ยนเป็นสัญญาณกระแสโดยวงจรเปลี่ยนแรงดันเป็นกระแส วงจรเร็คติฟายเออร์กระแสเร็คติฟายสัญญาณกระแสนี้ทำให้เกิดสัญญาณเอาต์พุตที่เป็นกระแสซึ่งถูกเปลี่ยนกลับเป็นสัญญาณเอาต์พุตที่เป็นแรงดันโดยวงจรเปลี่ยนกระแสเป็นแรงดัน ทฤษฎีของการทำงานถูกอธิบาย การทดลองโดยการสร้างจริงและการซิมมูเลชั่นถูกใช้ตรวจสอบการออกแบบทางทฤษฎี ผลการทดลองถูกเปรียบเทียบกับผลของวงจรเร็คติฟายเออร์ที่ใช้วงจรสายพานกระแสในเอกสารอ้างอิงที่ [2] และ [6-8]

สำหรับวงจรเร็คติฟายเออร์แบบเต็มคลื่นที่นำเสนอถูกสร้างโดยใช้วงจรสายพานกระแสใน IC เบอร์ AD844 ไบโพล่าร์ทรานซิสเตอร์เบอร์ 2N3904 และ 2N3906 ผลการทดลองแสดงถึงประสิทธิภาพทางด้านอุณหภูมิ กล่าวคือเมื่อเปลี่ยนอุณหภูมิทำงานจาก 27°C ถึง 70°C ค่าแรงดันเอาต์พุตต่ำสุดเปลี่ยนแปลงเพียง 76 μV สำหรับประสิทธิภาพด้านการเร็คติฟายแรงดันต่ำสุดเป็น 94 μV ซึ่งประสิทธิภาพทั้งสองนั้นดีกว่าของวงจรเร็คติฟายเออร์ที่ใช้วงจรสายพานกระแสในเอกสารอ้างอิงที่กล่าวมา

สำหรับวงจรเร็คติฟายเออร์แบบครึ่งคลื่นที่นำเสนอถูกเลียนแบบการทำงานโดยใช้เทคโนโลยีของ CMOS ขนาด 0.5 μm จาก MIETEC ผลการทดลองแสดงถึงประสิทธิภาพทางด้านอุณหภูมิ กล่าวคือเมื่อเปลี่ยนอุณหภูมิทำงานจาก 27°C ถึง 70°C ค่าแรงดันเอาต์พุตต่ำสุดเปลี่ยนแปลงเพียง 0 V สำหรับประสิทธิภาพด้านการเร็คติฟายแรงดันต่ำสุดเป็น 0 μV และประสิทธิภาพด้านความถี่ทำงาน วงจรสามารถทำงานได้ตั้งแต่ความถี่ 0 – 100 MHz ซึ่งประสิทธิภาพทั้งสามนั้นดีกว่าของวงจรเร็คติฟายเออร์ที่ใช้วงจรสายพานกระแสในเอกสารอ้างอิงที่กล่าวมา

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Thesis Title	Designs of Half-Wave and Full-Wave Rectifiers Using Current Conveyors
Student	Mr. Adisak Monpapassorn
Student ID.	41060002
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Thesis Advisor	Assoc.Prof.Dr.Kobchai Dejhan

ABSTRACT

The realizations of a half-wave rectifier and a full-wave rectifier using current conveyors are presented in this thesis. Each of the proposed rectifiers is composed of a voltage to current converter, a current mode full-wave rectifier, and a current to voltage converter. A voltage input signal is changed into a current signal by the voltage to current converter. The current rectifier rectifies this current signal resulting in a current output signal that is converted into a voltage output signal by the current to voltage converter. The theories of operations are described. The simulation and experiment results are used to verify the theoretical predictions. These results are compared with those of the current conveyor rectifiers in [2] and [6-8].

For the proposed full-wave rectifier, the current conveyor in AD844 IC, 2N3904 and 2N3906 bipolar transistors are used. Results show the temperature stability (shift in minimum output voltages between temperatures of 27°C and 70°C being 76 μV) and the minimum voltage rectification (94 μV) to be better than those of the above current conveyor rectifiers.

For the proposed half-wave rectifier, the 0.5 μm CMOS technology from MIETEC is applied. Results also show the temperature stability (shift in minimum output voltages between temperatures of 27°C and 70°C being 0 V), the minimum voltage rectification (0 V), and the operation frequency range (0 – 100 MHz) to be better than those of the above current conveyor rectifiers.

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Adisak Monpapassorn

King Mongkut's Institute of Technology Ladkrabang

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FIGURE CONTENTS

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FIGURE CONTENTS

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Chapter 1

Introduction

1.1 Source and introduction of the problem

Rectifiers are extensively used in wattmeters, AC voltmeters, RF demodulators, piecewise linear function generators, and various nonlinear analog signal processing circuits. The operation of diode-only rectifiers is limited by the threshold voltages of diodes, approximately 0.3 V for germanium diodes and 0.7 V for silicon diodes. Therefore diode-only rectifiers are used in only those applications in which the precision in the range of the threshold voltage is insignificant, such as RF demodulators and DC voltage supply rectifiers. For applications requiring high accuracy, the diode-only rectifiers cannot be used: MOS and bipolar integrated circuit rectifiers are used instead.

One advantage of the integrated circuit (IC) rectifiers designed using the simple devices such as opamps, current conveyors, transistors, diodes, and resistors as components, is that they can be built in many countries. The classical problem with conventional precision rectifiers based on diodes and opamps is that during the non-conduction/conduction transition of the diodes the opamps must recover with a finite small signal dV/dt resulting in significant distortion during the zero crossing of the input signal. The use of the high slew-rate opamps does not solve this fundamental drawback because it is a small signal transient problem [1]. Conventional rectifiers are thus limited to a frequency performance well below the gain-bandwidth product or f_T of the opamp [2]. This limitation is improved by designing the rectifiers by the use of the current rectifying techniques, which was reported by many researchers: Surakampontorn *et al.* [3], Ramirez-Angulo [4], Surakampontorn and Riewruja [5], Lidgey *et al.* [1], engineers of the LTP Electronics Ltd. [6], Toumazou *et al.* [2], Hayatleh *et al.* [7], Khan *et al.* [8]. Some of these reported rectifiers use the class AB amplifiers [3-5]. Although they have the advantage in view of the use of few devices, they also have the drawback. Namely, while $|I_{in}|$ is lower than $4I_B$, where I_{in} is an input current and I_B are two constant current sources used in the amplifier, an output current has an error being the square function of the input current. The use of rectifiers employing current conveyors and diodes can avoid this square function problem.

Recently, the rectifiers using current conveyors as a voltage to current converter have received wide attention. For example, LTP Electronics Ltd. [6] and Khan *et al.* [8] proposed the

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same current conveyor full-wave rectifiers as shown in figure 1.1(a). This full-wave rectifier is developed to reduce the distortion due to the small signal dV/dt limitation in the next time by Toumazou *et al.* [2] with the addition of a DC voltage source as shown in figure 1.1(b). Hayatleh *et al.* [7] further developed this full-wave rectifier to reduce the effect of temperature on the zero crossing performance by using a current source and a resistor in place of the voltage source, as shown in figure 1.1(c).

The problem of the current conveyor rectifiers in [6] and [8] is that they have low operation frequency. This problem is improved in the rectifiers, [2] and [7], but this improvement brings in the new problems: temperature stability and minimum voltage rectification. This thesis presents two current conveyor rectifiers, half-wave and full-wave rectifiers, which have no such problems.

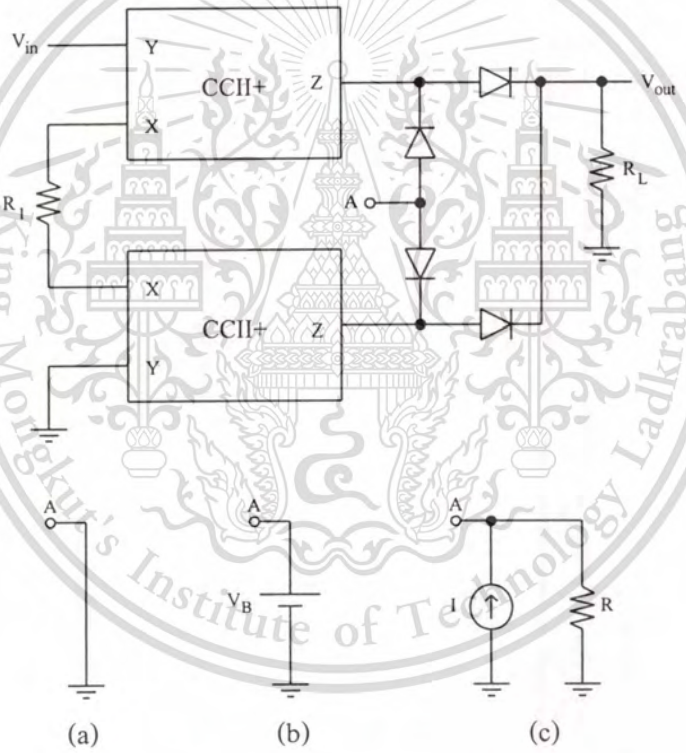

Figure 1.1 Current conveyor based precision full-wave rectifiers: (a) without biasing [6] and [8], (b) voltage biasing [2], and (c) current biasing [7].

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1.2 Purpose and objective of the study

In this thesis, the author presents the half-wave and full-wave rectifiers using current conveyor V-I converters, current rectifiers, and resistor I-V converters. Proposed rectifiers yield the following advantages:

- The proposed rectifiers using the number of solid-state devices are roughly equal to the current conveyor rectifiers from the LTP Electronics Ltd. [6], Khan *et al.* [8], Toumazou *et al.* [2] and Hayatleh *et al.* [7]. However, the proposed rectifiers use all grounded resistors. Whereas each of the previous current conveyor rectifiers uses both ungrounded and grounded resistors. In IC process, the grounded resistor can be created by using transistors to be lower than creating the ungrounded resistor. Therefore, the proposed rectifier is more suitable for IC fabrication than the previous current conveyor rectifiers.
- The proposed rectifiers can rectify the input voltage to be much lower than that previous current conveyor rectifiers can rectify.
- The proposed rectifiers provide better temperature stability than the previous current conveyor rectifiers.

1.3 Assumption of the study

- Designing voltage to current converters that use grounded resistors.
- Designing new current rectifiers.
- Designed current rectifiers have to provide good temperature stability.

1.4 Theory or idea used in the research

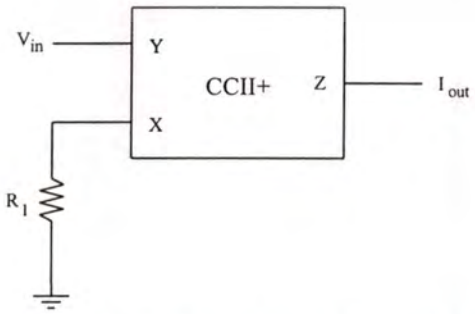

Figure 1.2 Voltage to current converter using one current conveyor and a resistor.

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- Note from the previous current conveyor rectifiers in figure 1.1 that a voltage to current converter consists of two current conveyors (CCII+s) and a left-ungrounded resistor. Really, the voltage to current converter can be created by using only one CCII+ and one grounded resistor as shown in figure 1.2, which this converter is used in the proposed rectifiers.
- Each of the previous current conveyor rectifiers of Toumazou *et al.* [2] and Hayatleh *et al.* [7] uses the biasing voltage at node A to improve the on/off transition problem of diodes in the current rectifier. This biasing voltage makes diodes turning-on all the time and makes the offset at an output. The proposed rectifiers use current rectifiers and biasing circuits that do not produce the offsets at outputs. Automatic precision biasing current compensating is used for the proposed full-wave rectifier, and the careful biasing voltage adjustment is used for the proposed half-wave rectifier.
- For the previous current conveyor rectifiers of Toumazou *et al.* [2] and Hayatleh *et al.* [7], the biasing voltage at node A has to be adjusted as 2 V_T approximately (V_T is a threshold voltage of the diode). Unfortunately, V_T depends upon the temperature. Namely when the temperature increases, it causes the offset voltage at the output. Inversely, when the temperature decreases, it causes diodes not to turn-on all the time. The proposed rectifiers use current rectifiers and biasing circuits that do not produce those temperature problems. The balance circuit structure with automatic compensation is used for the proposed full-wave rectifier, and the change of the biasing voltage to be up to the temperatures is used for the proposed half-wave rectifier.

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Chapter 2

Bipolar junction transistor and current mirror applications

2.1 Bipolar junction transistor

A bipolar junction transistor (BJT) is divided to two types: NPN and PNP, following the connection structure of semiconductors. A typical cross section of an NPN BJT is shown in figure 2.1 (a). Although this structure looks quite complicated, it corresponds approximately to the equivalent structure shown in figure 2.1 (b).

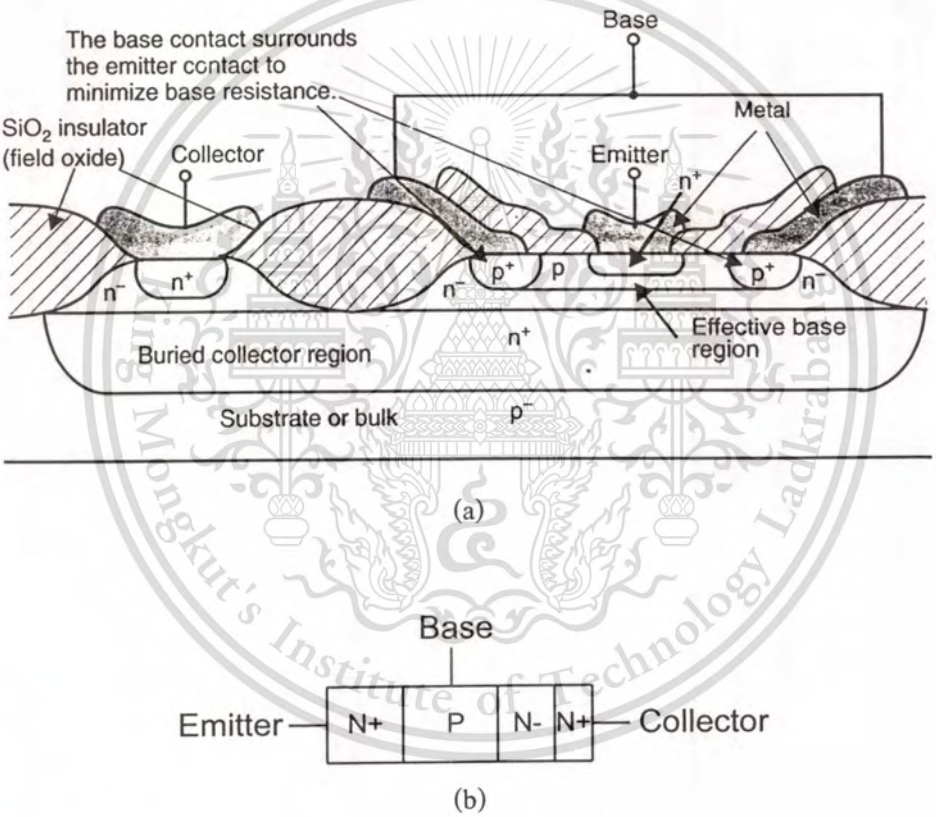

Figure 2.1 An NPN BJT: (a) a cross section and (b) a simplified structure.

Figure 2.2 shows the symbols of both NPN and PNP BJTs. The differences between them are the potentials of bias voltages and the directions of currents at the base, the collector and the emitter as shown in figure 2.2.

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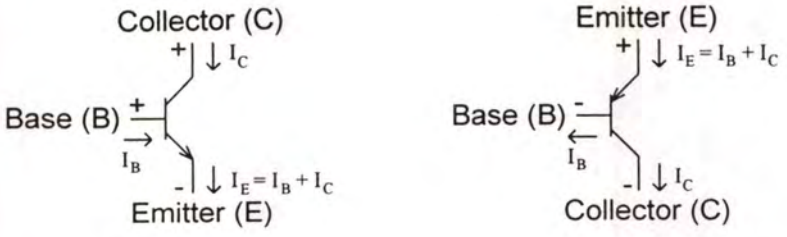

Figure 2.2 Symbols of (a) NPN BJT and (b) PNP BJT.

2.1.1 Basic operation

To understand the operation of BJTs, we consider here an NPN BJT with the emitter connected to ground, as shown in figure 2.3. If the bias voltage V_B is less than about 0.5 V, the BJT will be cut off, and no current will flow. We will see that when the base-emitter PN junction becomes forward biased, the current will start to flow from the base to the emitter, but, partly because the base width is small, a much larger proportional current will flow from the collector to the emitter. Thus, the NPN BJT can be considered as a current amplifier at low frequencies. In other words, if the BJT is not cut off and the collector-base junction is reverse biased, a small base current controls a much larger collector-emitter current.

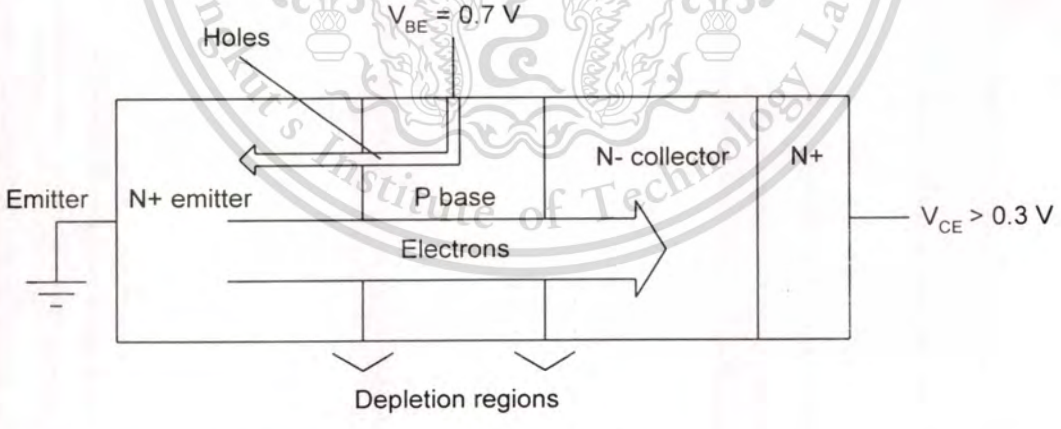

Figure 2.3 Various components of the currents of an NPN BJT.

A simplified overview of how an NPN BJT operates follows: when the base-emitter junction becomes forward biased, it starts to conduct, similar to any forward biased junction. The current consists of majority carriers from the base (in this case, holes) and majority carriers from the emitter (in this case, electrons) diffusing across the junction. Because the emitter is more heavily

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doped than the base, there are many more electrons injected from the emitter than there are holes injected from the base. Assuming the collector voltage is large enough so that the collector-base junction is the reverse biased, no holes from the base will go to the collector. However, the electrons that travel from the emitter to the base, where they are now minority carriers, diffuse away from the base-emitter junction because of the minority-carrier concentration gradient in the base region. Any of these minority electrons that get close to the collector-base junction will immediately be "whisked" across the junction due to the large positive voltage on the collector, which attracts the negatively charged electrons. In a properly designed BJT, the vertical base width W is small, and almost all of the electrons that diffuse from the emitter to the base reach the collector-base junction and are swept across the junction, thus contributing to current flow in the collector. The result is that the collector current very closely equals the electron current flowing from the emitter to the base. The much smaller base current very closely equals the current due to the holes that flow from the base to the emitter. The total emitter current is the sum of the electron collector current and the hole base current, but since the hole current is much smaller than the electron current, the emitter current is approximately equal to the collector current.

Since the collector current is approximately equal to the electron current flowing from the emitter to the base, and the amount of this electron current is determined by the base-emitter voltage, it can be shown that the collector current is exponentially related to the base-emitter voltage by the relationship

$$I_C = I_{CS} e^{V_{BE}/V_{TM}} \tag{2.1}$$

where V_{TM} is the thermal voltage. I_{CS} is the scale current. This scale current is proportional to the area of the base-emitter junction. The base current, determined by the hole current flowing from the base to the emitter, is also exponentially related to the base-emitter voltage V_{BE}, resulting in the ratio of the collector current to the base current being a constant that, to a first-order approximation, is independent of voltage and current. This ratio, typically denoted as β, is defined to be

$$\beta = \frac{I_C}{I_B} \tag{2.2}$$

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where I_C and I_B are the collector and base currents. Typical values of β are between 50 and 200

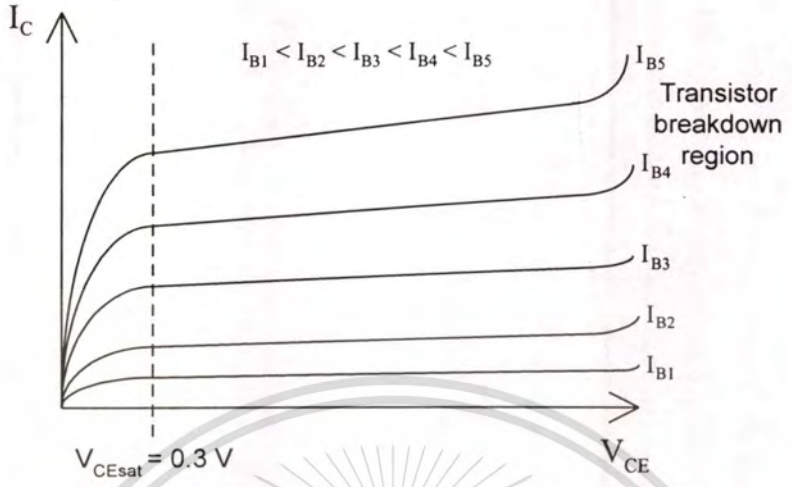

Figure 2.4 Typical plot of I_C versus V_{CE} for a BJT.

Note that equation (2.1) implies that the collector current is independent of the collector voltage. This independence ignores second-order effects, namely the decrease in effective base width W due to the increase in the width of the collector-base depletion region when the collector bias voltage is increased. To illustrate this point, a typical plot of the collector current I_C as a function of the collector to emitter voltage V_{CE} for different values of I_B, is shown in figure 2.4 for a practical transistor. The fact that the curves are not flat for $V_{CE} > V_{CE\text{-}sat}$ indicates the dependence of I_C on V_{CE}. Indeed, to a good approximation, the dependence is linear with a slope that intercepts the V_{CE} axis at $V_{CE} = V_A$ for all value of I_B. The intercept voltage value V_A is called the early voltage for BJT, with a typical value being from 50 V to 100 V. This dependency results in a finite output impedance and can be modeled by modifying equation 2.1 [10] to be

$$I_C \cong I_{CS} e^{V_{BE}/V_{TM}} \left(1 + \frac{V_{CE}}{V_A}\right) \tag{2.3}$$

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2.1.2 Small signal modeling

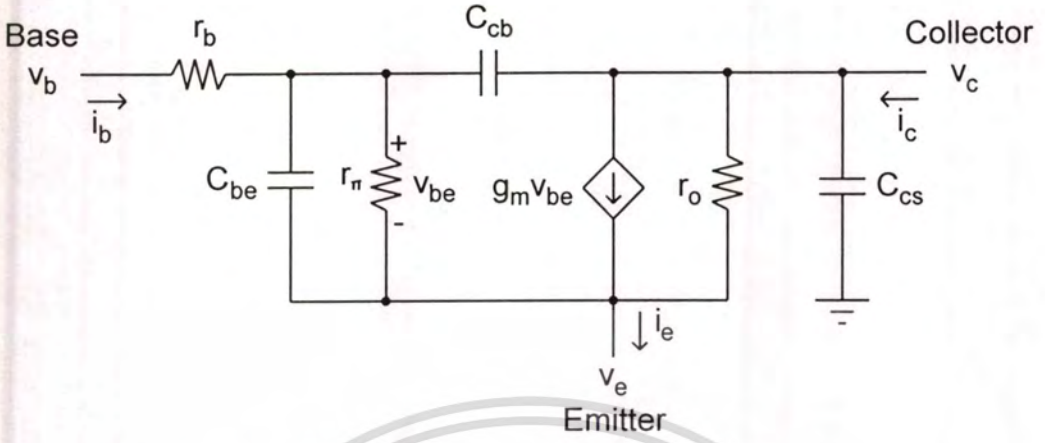

Figure 2.5 The small signal model of an active BJT.

The most commonly used small signal model is a hybrid-π model, which is shown in figure 2.5. The transistor transconductance g_m is perhaps the most important parameter of the small signal model. The transconductance is the ratio of the small signal collector current i_c to the small signal base-emitter voltage v_{be}. Thus, we have

$$g_m = \frac{i_c}{v_{be}} = \frac{\partial I_C}{\partial V_{BE}} \tag{2.4}$$

Recall that in the active region

$$I_C = I_{CS} e^{V_{BE}/V_{TM}} \tag{2.5}$$

Then

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_{CS}}{V_{TM}} e^{V_{BE}/V_{TM}} \tag{2.6}$$

Using (2.5) again, we obtain

$$g_m = \frac{I_C}{V_{TM}} \tag{2.7}$$

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where V_{TM} is given by

$$V_{TM} = \frac{KT}{q} \tag{2.8}$$

where K being Boltzmann's constant (1.38×10^{-23}) and q being the charge of an electron (1.602×10^{-19}C). This V_{TM} is approximately 26 mV at a room temperature of T = 300 °K. Thus, the transconductance is proportional to the bias current of a BJT. In integrated circuit design, it is important that the transconductance remains temperature independent, so the bias currents are usually made proportional to absolute temperature (since V_{TM} is proportional to absolute temperature).

The presence of the resistor r_π reflects the fact that the base current is nonzero. Then

$$r_\pi = \frac{\partial V_{BE}}{\partial I_B} \tag{2.9}$$

From (2.2),

$$I_B = \frac{I_C}{\beta} = \frac{I_{CS}}{\beta} e^{V_{BE}/V_{TM}} \tag{2.10}$$

we therefore have

$$\frac{1}{r_\pi} = \frac{\partial I_B}{\partial V_{BE}} = \frac{I_{CS}}{\beta V_{TM}} e^{V_{BE}/V_{TM}} \tag{2.11}$$

Using (2.10) again, we have

$$r_\pi = \frac{V_{TM}}{I_B} \tag{2.12}$$

or equivalently,

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$$r_\pi = \beta \frac{V_{TM}}{I_C} = \frac{\beta}{g_m} \tag{2.13}$$

Since

$$i_e = i_c + i_b \tag{2.14}$$

we also have

$$\begin{aligned} \frac{\partial I_E}{\partial V_{BE}} &= \frac{\partial I_C}{\partial V_{BE}} + \frac{\partial I_B}{\partial V_{BE}} \\ &= g_m + \frac{g_m}{\beta} \\ &= g_m \left(\frac{1+\beta}{\beta} \right) \\ &= \frac{g_m}{\alpha} \end{aligned} \tag{2.15}$$

Continuing, we have

$$\frac{1}{r_o} = \frac{\partial I_C}{\partial V_{CE}} \tag{2.16}$$

The small signal resistance r_o models the dependence of the collector current on the collector-emitter voltage. Repeating (2.3) here for convenience,

$$I_C = I_{CS} e^{V_{BE}/V_{TM}} \left(1 + \frac{V_{CE}}{V_A} \right) \tag{2.17}$$

we have

$$\frac{1}{r_o} = \frac{\partial I_C}{\partial V_{CE}} = \frac{I_{CS}}{V_A} e^{V_{BE}/V_{TM}} \tag{2.18}$$

Thus,

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$$r_o = \frac{V_A}{I_C} \tag{2.19}$$

which is inversely proportional to the collector current. As an aside, note that $g_m r_o = V_A/V_{TM}$ is a constant value independent of the transistor operating point. This constant is usually between 2,000 and 8,000 for an NPN BJT and is an upper limit on the attainable voltage gain for a single-transistor amplifier.

The resistor r_b models the resistance of the semiconductor material between the base contact and the effective base region due to the moderately lightly doped base P material. This resistor, although small (typically a few hundred ohms), can be important in limiting the speed of very high frequency low-gain BJT circuits and is a major source of noise.

The high frequency operation of a BJT is limited by the capacitances of the small signal model. The first capacitor is C_{be}, which is the sum of the depletion capacitance of the base-emitter junction and the diffusion capacitance. The second capacitor is C_{cb}, which is the depletion capacitance of the collector-base junction. The other capacitor is an another large capacitor C_{cs}, which is the capacitance of the collector to substrate junction. Since this area is quite large, C_{cs} is the depletion capacitance that results from this area, the capacitance will be much larger than either C_{cb} or C_{be}.

2.2 Current mirrors using BJTs [9]

2.2.1 Simple current mirror

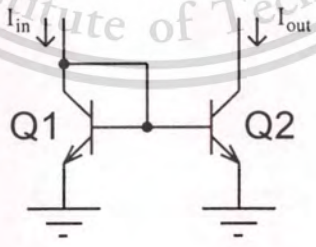

Figure 2.6 A simple bipolar current mirror.

A simple bipolar current mirror is shown in figure 2.6. This current mirror has an output current almost equal to its input current. In fact, its output current is slightly smaller than the input current, due to the finite base currents of the same characteristic Q1 and Q2. Taking these two base currents into account results in

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$$I_{out} = I_{in} - 2I_B \tag{2.20}$$

$$I_B = \frac{I_{out}}{\beta} \tag{2.21}$$

Substituting (2.20) by (2.21), we get

$$I_{out} = I_{in} - 2\frac{I_{out}}{\beta} \tag{2.22}$$

$$1 = \frac{I_{in}}{I_{out}} - \frac{2}{\beta} \tag{2.23}$$

$$I_{out} = \frac{1}{(1+2/\beta)} I_{in} \tag{2.24}$$

where β is the transistor current gain. For large β, this relation is approximately given by

$$I_{out} \cong (1-2/\beta) I_{in} \tag{2.25}$$

It is easy to find the output impedance of

$$r_{out} = r_{o2} \tag{2.26}$$

2.2.2 Wilson bipolar current mirror

To achieve higher output impedance, one can use a Wilson realization as shown in figure 2.7. All bipolar transistors are identical, making the currents:

$$I_{E2} = I_{C3} + 2I_B = (\beta + 2) I_B \tag{2.27}$$

$$I_{out} = I_{C2} = \frac{\beta}{\beta+1} I_{E2} = \frac{\beta(\beta+2)}{\beta+1} I_B \tag{2.28}$$

$$I_{B2} = \frac{1}{\beta+1} I_{E2} = \frac{\beta+2}{\beta+1} I_B \tag{2.29}$$

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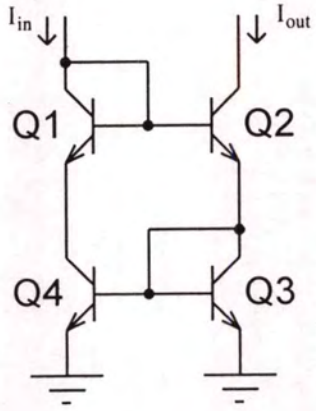

Figure 2.7 A high output impedance Wilson current mirror.

$$I_{in} = I_{C4} + I_{B2} = \beta I_B + \frac{\beta+2}{\beta+1} I_B \tag{2.30}$$

Using (2.28) and (2.30), the current gain can be written as

$$\frac{I_{out}}{I_{in}} = \frac{\frac{\beta(\beta+2)}{\beta+1} I_B}{\beta I_B + \frac{\beta+2}{\beta+1} I_B} = \frac{\frac{\beta(\beta+2)}{\beta+1}}{\frac{\beta(\beta+1)}{\beta+1} + \frac{\beta+2}{\beta+1}} = \frac{\beta(\beta+2)}{\beta(\beta+1)+(\beta+2)} \tag{2.31}$$

$$\frac{I_{out}}{I_{in}} = \frac{\beta^2+2\beta}{\beta^2+2\beta+2} = \frac{1}{1+\frac{2}{\beta^2+2\beta}} \approx \frac{1}{1+\frac{2}{\beta^2}} \approx 1 \tag{2.32}$$

This shows the operation precision of Wilson bipolar current mirror that is much better than the precision of the simple bipolar current mirror.

The output impedance of Wilson bipolar current mirror can be obtained by using the small signal equivalent circuits of the circuit in figure 2.7, as shown in figure 2.8. From (2.13), if all the transistors in Wilson current mirror have the large β. It leads to

$$r_\pi >> \frac{1}{g_m} \tag{2.33}$$

Considering r_{ex} of figure 2.8 (b) with (2.33)

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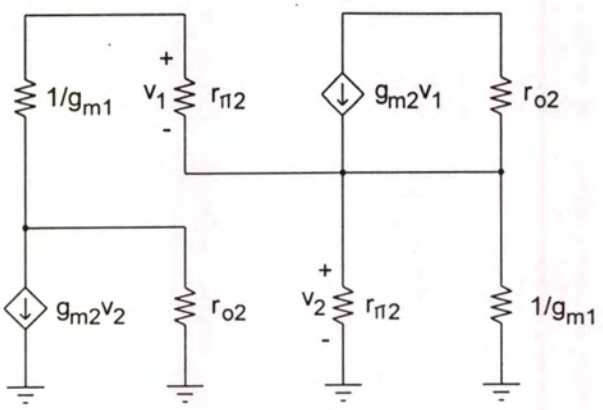
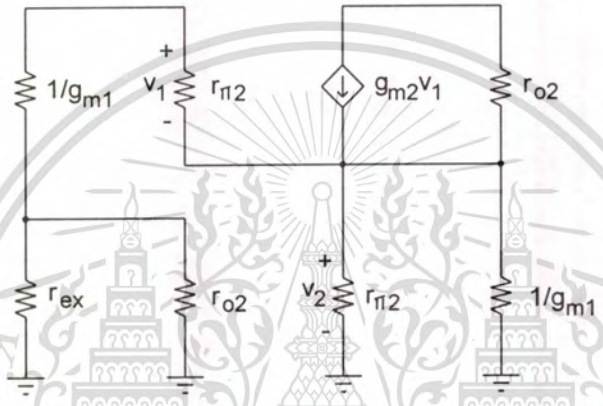


(a)



(b)

Figure 2.8 Small signal equivalent circuits of Wilson bipolar current mirror.

$$\frac{1}{r_{ex}} \approx g_{m2}\frac{\frac{1}{g_{m1}}}{r_{\pi 2}+\frac{2}{g_{m1}}} \approx \frac{g_{m2}}{\beta_2+2} \approx \frac{g_{m2}}{\beta_2} \approx \frac{1}{r_{\pi 2}} \tag{2.34}$$

this equation shows that

$$r_{ex} \approx r_{\pi 2} \tag{2.35}$$

Exploiting Ohm's law to find the output resistance

$$r_{out} = \frac{v_o}{i_o} \approx r_{o2}\left(1+\frac{\beta_2}{r_{\pi 2}+(r_{ex}\,//\,r_{o2})}(r_{ex}\,//\,r_{o2})\right) \tag{2.36}$$

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because of $r_{\pi 2} << r_{o2}$, equation (2.36) can be rewritten as

$$r_{out} \approx r_{o2}\left(1+\frac{\beta_2}{r_{\pi 2}+r_{\pi 2}}r_{\pi 2}\right) \approx \frac{\beta_2 r_{o2}}{2} \tag{2.37}$$

It is clear that this output impedance is much greater than the output impedance of the simple bipolar current mirror.

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Chapter 3

Current conveyors

3.1 Introduction

A current conveyor is normally a three terminal device which when arranged with other electronic elements in specific circuit configurations can perform many useful analog signal processing functions [12–14]. In many ways, the current conveyor simplifies circuit design in much the same manner as the conventional operational amplifier (opamp). This stems largely from the fact that the current conveyor offers an alternative way of abstracting complex circuit functions, thus aiding in the creation of new and useful implementations. This together with the fact that the actual terminal behavior of the current conveyor, like the opamp, approaches its ideal behavior quite closely. This, as most designers of opamp circuits know, implies that one can design current conveyor circuits that work at levels that are quite close to their predicted theoretical performance.

At the time of the introduction of the current conveyor (1968), it was not clear that what advantages the current conveyor offered over the conventional opamp. Moreover, the electronics industry was just beginning to focus its efforts on the creation and application of the first generation of monolithic opamps. Without clearly stated advantages, the electronics industry lacked the motivations to develop a monolithic current conveyor realization. After all, the opamp concept was entrenched in the minds of many analog circuit designers since the late 1940's and as far as IC manufacturers were concerned, an opamp market was already there to be tapped and expanded. It is only now that, analog designers are discovering that the current conveyor offers several advantages over the conventional opamp. Specifically, a current conveyor circuit can provide a higher voltage gain over a large signal bandwidth under small or large signal conditions than a corresponding opamp circuit, in effect a higher gain-bandwidth product [15]. In addition, current conveyors have been extremely successful in the development of an instrumentation amplifier, which does not depend critically on the matching of external components, instead depends only on the absolute value of a single component [16-18].

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3.2 First generation current conveyor [22]

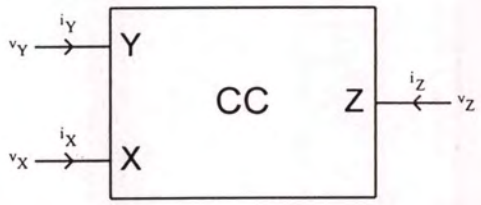

Figure 3.1 Black-box representation of the current conveyor.

The current conveyor (CCI), as initially introduced, is a 3-port device whose black-box representation can be shown as in figure 3.1. The operation of this device is such that if a voltage is applied to the input terminal Y, an equal potential will appear at the X input terminal. In a similar fashion, the input current I being feeding into the terminal X will result in an equal amount of current flowing into the Y terminal. As well, the current I will be conveyed to the output terminal Z such that the terminal Z becomes a current source, of value I, with high output impedance. Obviously, the potential of X, being set by that of Y, is independent of the current being fed into the X port. Similarly, the current through the input Y, being fixed by that of X, is independent of the voltage applied at Y. Thus the device exhibits a virtual short-circuit input characteristic at port X and a virtual open-circuit input characteristic at port Y.

The input-output characteristic of CCI can be described mathematically by the following hybrid equation

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \tag{3.1}$$

Note the + sign applies for the CCI in which both Z and X flow into the conveyor, denoted CCI+. The – sign apply for the opposite polarity case, denoted CCI-.

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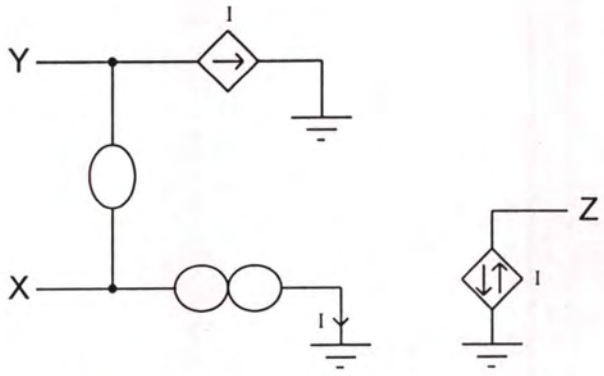

Figure 3.2 Nullator-norator representation of CCI. Downward arrow in the controlled source at Z is for a CCI+, the upward arrow for a CCI-.

To visualize the interaction of the port, voltages described by the above matrix equation the nullator-norator [19] representation (commonly referred to as a nullor) shown in figure 3.2 may be helpful. In this figure, a single ellipse is used to represent the nullator element and two intersecting ellipses to represent the norator element. The nullator element has constitutive equations V = 0 and I = 0 whereas the norator has an arbitrary voltage-current relationship. Clearly, the nullator element is used to represent the virtual short circuit apparent between the X and Y terminals. Also included in this equivalent circuit are two dependent current sources. These are used to convey the current at port X to ports Y and Z.

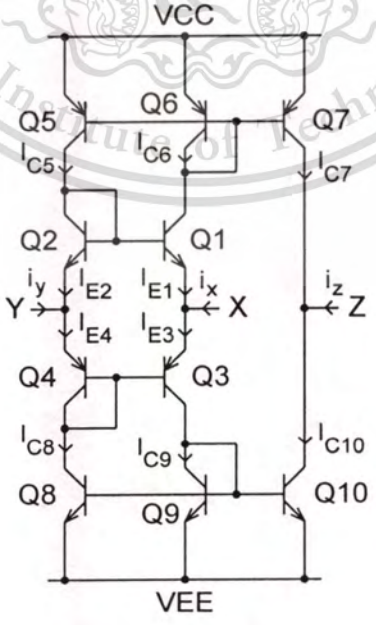

Figure 3.3 Bipolar implementation of CCI.

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A discrete implementation of the current conveyor is depicted in figure 3.3. Assuming that all transistors are matched and supply voltages $V_{CC} = -V_{EE}$ are used. Bipolar transistors Q5 to Q7 and Q8 to Q10 operate as current mirrors. Neglecting base currents I_B ($I_C = I_E$) because high β transistors are chosen. These yield

$$\left.\begin{aligned} I_{C5} = I_{E2} = I_{C6} = I_{E1} = I_{C7} \\ I_{E4} = I_{C8} = I_{E3} = I_{C9} = I_{C10} \end{aligned}\right\} \tag{3.2}$$

Considering three nodes of CCI: node X

$$I_{E1} + i_x = I_{E3} \tag{3.3}$$

node Y

$$I_{E2} + i_y = I_{E4} \tag{3.4}$$

and node Z

$$I_{C7} + i_z = I_{C10} \tag{3.5}$$

Exploiting (3.2), equations (3.3), (3.4) and (3.5) make

$$i_x = i_y = i_z \tag{3.6}$$

Equation (3.2) shows that Q1 and Q2 as well as Q3 and Q4 operate as current mirrors; therefore their emitter voltages have to be equal, that is

$$v_x = v_y \tag{3.7}$$

Both (3.6) and (3.7) are the same as (3.1), the circuit in figure 3.3 thus operates as CCI.

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3.3 Second generation current conveyor

To increase the versatility of the current conveyor, a second version (CCII) in which no current flows in terminal Y, was introduced [13]. This building block has since proven to be more useful than CCI. Utilizing the same block diagram representation of figure 3.1, CCII is described by

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \tag{3.8}$$

From (3.8), terminal Y exhibits an infinite input impedance. The voltage at X allows that applied to Y, thus X exhibits a zero input impedance. The current supplied to X is conveyed to the high impedance output terminal Z where it is supplied with either positive polarity (in CCII+) or negative polarity (in CCII-). In term of a nullor, the port behavior of the second-generation current conveyor (positive or negative) can be depicted as shown in figure 3.4(a). The similarity and difference between a CCI and CCII are clearly evident when one compares their equivalent circuits in figure 3.2 and figure 3.4(a). In the case of CCII-, the dependent current source is redundant; current flowing into terminal X must flow out of terminal Z. Hence, the equivalent circuit of CCII- can be represented with a single nullor element as shown in figure 3.4(b).

Figure 3.5 shows the bipolar implementation of a CCII+ and a CCII-. Two constant current sources I_B of CCII+ of figure 3.5(a) are equal and all the transistors of this figure are closely matched. Supply voltages, $V_{CC} = -V_{EE}$, are used. Using high β transistors, Currents I_B of all transistors are neglected. These yield

$$I_{E2} = I_{E4} = I_B \tag{3.9}$$

See node Y, we obtain

$$i_y + I_{E2} = I_{E4} \tag{3.10}$$

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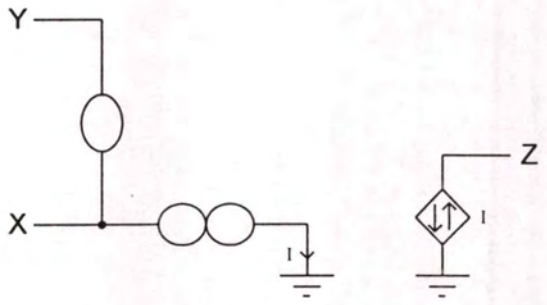
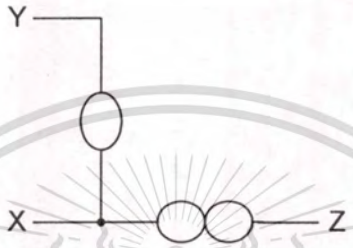


(a)



(b)

Figure 3.4 (a) Nullator-norator representation of a CCII. The downward arrow in the controlled source at Z is for a CCII+, the upward arrow for a CCII-. (b) A simplified representation of a CCII-.

From both (3.9) and (3.10), getting

$$i_y = 0 \tag{3.11}$$

Considering nodes X and Z with the above specifications of the circuit, dual transistors: Q5, Q6 and Q7, Q8 operates as current mirrors. We hence have

$$\left.\begin{aligned} I_{C5} &= I_{E1} = I_{C6} \\ I_{C7} &= I_{E3} = I_{C8} \end{aligned}\right\} \tag{3.12}$$

Current relation at node X is

$$I_{E1} + i_x = I_{E3} \tag{3.13}$$

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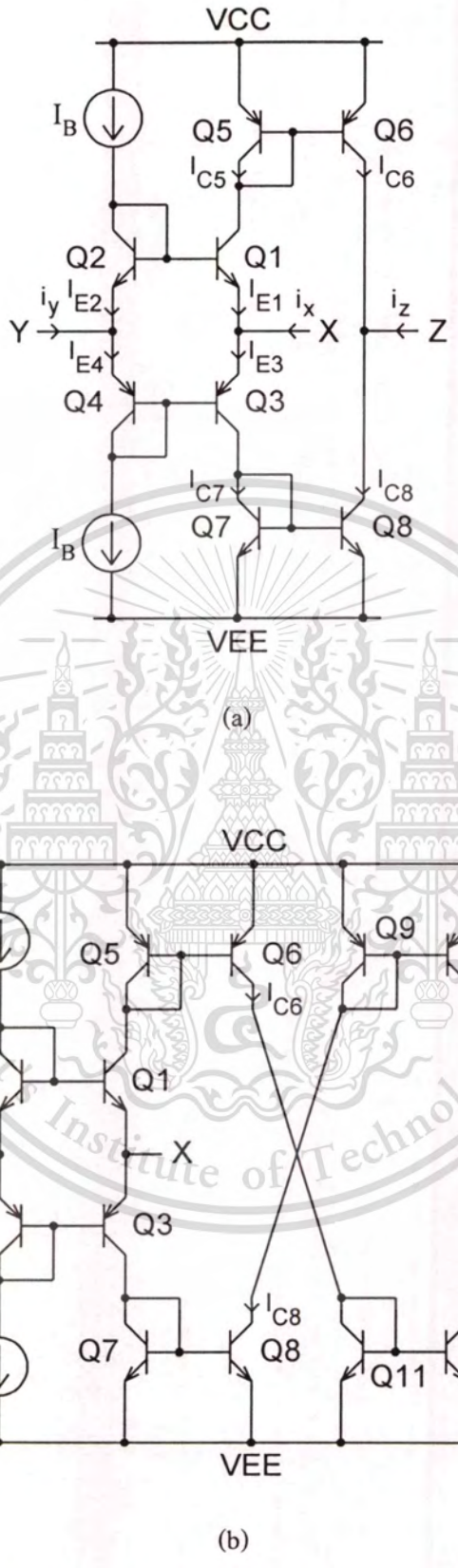

Figure 3.5 Examples of the circuits of (a) CCII+ and (b) CCII- using bipolar transistors.

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and current relation at node Z is

$$I_{C6} + i_z = I_{C8} \tag{3.14}$$

Applying (3.12) to (3.13) and (3.14) results in

$$i_z = i_x \tag{3.15}$$

At nodes X and Y, they are same balance (Q5 and Q7 seen as constant current sources), when node X without a load, yielding

$$v_x = v_y \tag{3.16}$$

this means that (Q1 and Q2) and (Q3 and Q4) are current mirrors, then

$$I_{E1} = I_{E2} = I_{E3} = I_{E4} \tag{3.17}$$

When node X connected to loads, equations (3.16) and (3.17) will be true where $I_B >> I_x$. From (3.11), (3.15) and (3.16), the circuit of figure 3.5(a) works as CCII+.

The operation of the CCII- of figure 3.5(b) like the operation of the above CCII+, only two current mirrors ((Q9 and Q10) and (Q11 and Q12)) are the added parts, to convert the direction of i_z. That is,

$$\left.\begin{aligned} I_{C8} &= I_{C10} \\ I_{C6} &= I_{C12} \end{aligned}\right\} \tag{3.18}$$

Consequently, at node Z

$$I_{C10} + i_z = I_{C12} \tag{3.19}$$

We can write the current relation by using (3.12), (3.13), (3.18) and (3.19) as

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$$i_z = -i_x \tag{3.20}$$

3.4 Commercial second generation current conveyor

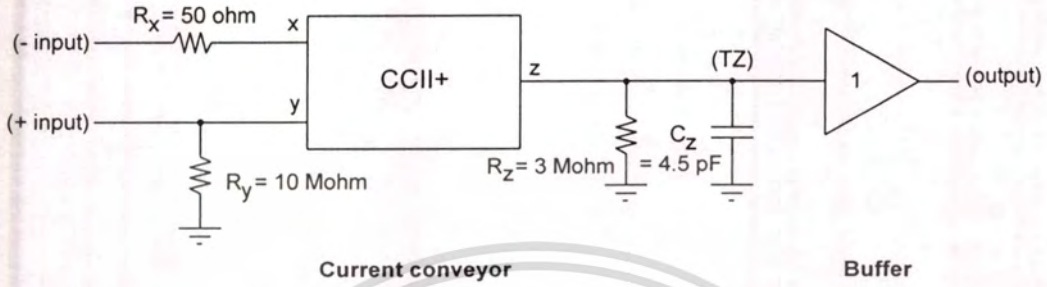

Figure 3.6 The model of the AD844 [20].

An integrated circuit that implements a current conveyor is now commercially available. Figure 3.6 shows an equivalent circuit for the AD844. The AD844 is modelled as an ideal second generation current conveyor having a gain of +1 (i.e. a CCII+), a unity gain buffer and some passive components which model the input and output impedances of the CCII+. More details of the AD844 from its data sheet are as follows. The AD844 can be operated from ±4.5 V to ±18 V power supplies. Its operation bandwidth is 60 MHz at gain of –1 and its maximum i_x and i_z are 5 mA.

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Chapter 4

Rectifiers

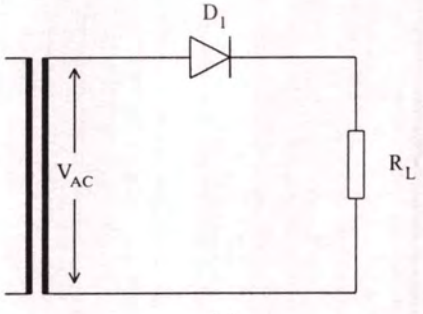
4.1 Introduction

Rectifiers are widely used in electrical and electronic applications. For example, the simple diode rectifiers using only diodes, both half-wave and full-wave rectifier types, are used in the DC power supply of the electrical and electronic circuits. A disadvantage of the simple diode rectifiers is that they cannot rectify the voltage to be lower than their threshold voltages (V_T), approximately 0.3 V for a germanium diode and 0.7 V for a silicon diode. This disadvantage causes that the simple diode rectifiers cannot be used in the small signal rectification of analog signal processing. To make the diode rectifying the voltage under the threshold voltage, we combine diodes with the active devices such as Operational Amplifier (opamp), Operational Transconductance Amplifier (OTA), and Current Conveyor (CCII+). Moreover, the MOSFET or BJT integrated circuit rectifier can rectify the voltage to be lower than the threshold voltage as well.

4.2 Simple diode rectifiers

4.2.1 A simple diode half-wave rectifier

A half-wave rectifier using only one diode is shown in figure 4.1(a). An AC input voltage (V_{AC}) is obtained from a secondary coil of a transformer. Figures 4.1(b) and 4.1(c) show an operation of this rectifier.



(a)

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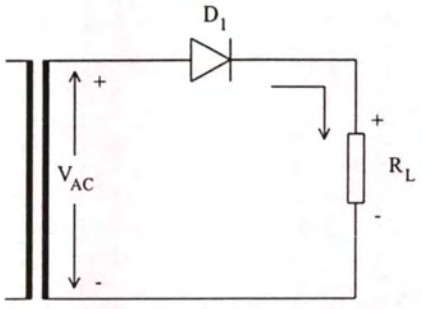
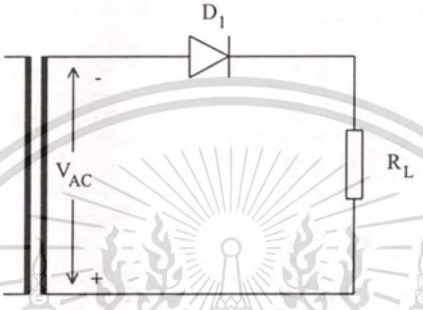


(b)



(c)

Figure 4.1 A simple diode half-wave rectifier and its operation.

Considering the AC potential condition of figure 4.1(b), in case the positive input voltage, a diode D_1 is forward biased. The voltage across the load R_L is therefore the input voltage. Figure 4.1(c) shows the condition of the negative input voltage. In this case, D_1 is the reverse biased diode, thus there is no the current flowing through D_1 and there is no the voltage across the load. The above operation can be expressed as

$$\left.\begin{aligned} V_{AC} > 0 ;\ V_{RL} = V_{AC} \\ V_{AC} < 0 ;\ V_{RL} = 0 \end{aligned}\right\} \tag{4.1}$$

The above operation is the case of an ideal diode (V_T = 0 V). For the true diode, equation (4.1) has to become

$$\left.\begin{aligned} V_{AC} > V_T ;\ V_{RL} = V_{AC} - V_T \\ V_{AC} < V_T ;\ V_{RL} = 0 \end{aligned}\right\} \tag{4.2}$$

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4.2.2 A simple diode full-wave rectifier using a center tapped transformer

Figure 4.2(a) shows a simple diode full-wave rectifier using a center tapped transformer. The rectifier uses only two diodes. The input voltage for this rectifier must be gotten from a secondary coil that is tapped at center. The operation of the rectifier is shown in figure 4.2(b) and 4.2(c).

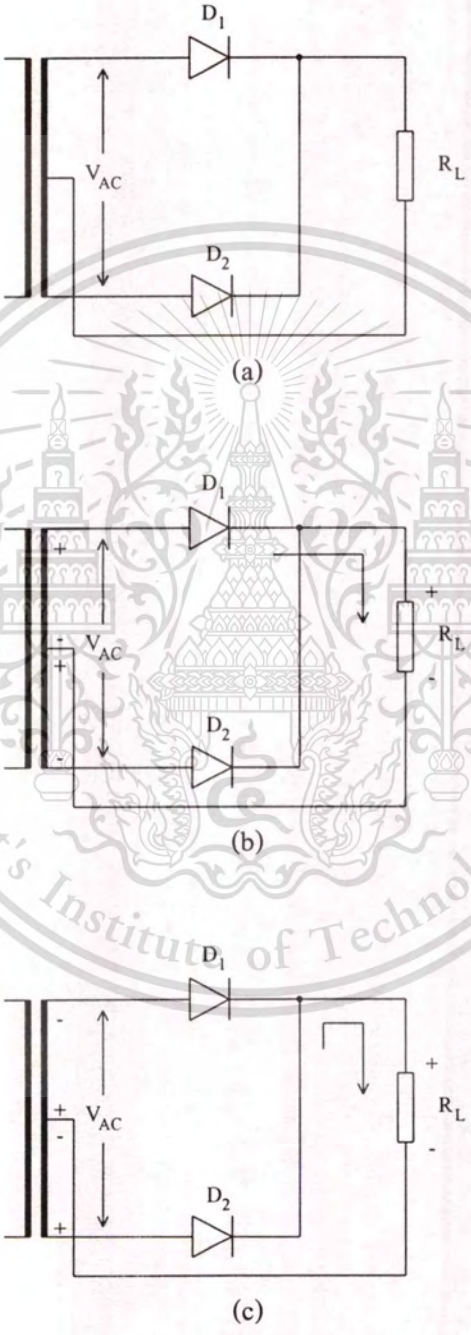

Figure 4.2 A simple diode full-wave rectifier using a center tapped transformer and its operation.

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When the input voltage is the positive voltage following to figure 4.2(b), D_1 is forward biased whereas D_2 is the reverse biased diode. The current will flow from the positive pole of the upper secondary coil through D_1 and R_L to a center tapped point of the secondary coil. This produces the positive voltage at R_L being equal to the voltage of the upper secondary coil. When the input voltage is the negative voltage as shown in figure 4.2(c), D_1 is the reverse biased diode whereas D_2 is the forward biased diode. The current will flow from the positive pole of the lower secondary coil through D_2 and R_L to the center tapped point. The voltage across R_L is hence the positive voltage of the lower secondary coil. The already mentioned operation can be written as

$$\left.\begin{aligned} V_{AC} > 0 ;\ V_{RL} &= \frac{V_{AC}}{2} \\ V_{AC} < 0 ;\ V_{RL} &= -\frac{V_{AC}}{2} \end{aligned}\right\} \tag{4.3}$$

where the operation of diodes is ideal. For the true diode, the equation is

$$\left.\begin{aligned} \frac{V_{AC}}{2} > V_T ;\ V_{RL} &= \frac{V_{AC}}{2} - V_T \\ -V_T < \frac{V_{AC}}{2} < V_T ;\ V_{RL} &= 0 \\ \frac{V_{AC}}{2} < V_T ;\ V_{RL} &= -\frac{V_{AC}}{2} - V_T \end{aligned}\right\} \tag{4.4}$$

4.2.3 A simple bridge diode full-wave rectifier

One drawback of a full-wave rectifier using a center-tapped transformer is the use of the center tapped secondary coil. A bridge full-wave rectifier needs no the center tapped transformer but it uses four diodes. Figure 4.3(a) shows the circuit of the bridge full-wave rectifier of which the operation is shown in figure 4.3(b) and figure 4.3(c). When the positive voltage is supplied to the bridge, see figure 4.3(b), diodes D_2 and D_3 are turned on while D_1 and D_4 are turned off. The current flows from the positive pole of the secondary coil through D_2, R_L and D_3 to the negative pole of the secondary coil resulting in the positive voltage appeared at R_L. In the opposite way, when the negative voltage is supplied to the bridge as figure 4.3(c), diodes D_1 and D_4 are turned on and D_2 and D_3 are turned off. The flow of the current from the positive pole of the secondary

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coil through D_4, R_L and D_1 to the negative pole of the secondary coil is occurred, causing the positive voltage across R_L. From the above, we get the ideal equation.

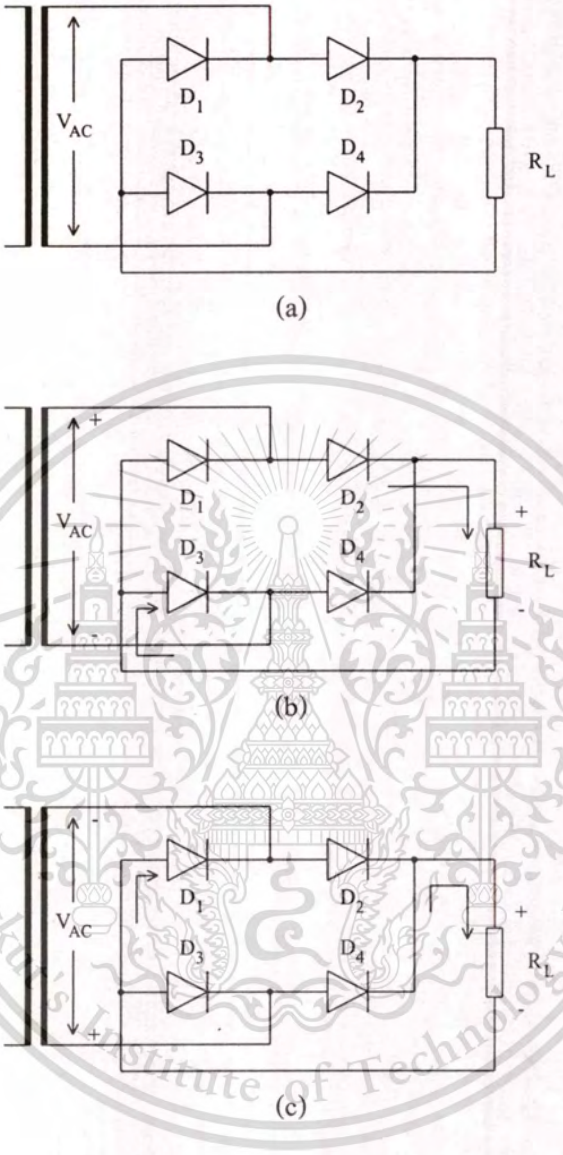

Figure 4.3 A simple bridge diode full-wave rectifier and its operation.

$$\left.\begin{aligned} V_{AC} > 0;\ V_{RL} = V_{AC} \\ V_{AC} < 0;\ V_{RL} = -V_{AC} \end{aligned}\right\} \tag{4.5}$$

Really, it should be

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$$\left.\begin{aligned} V_{AC} > 2V_T \;;\; V_{RL} &= V_{AC} - 2V_T \\ -2V_T < V_{AC} < 2V_T \;;\; V_{RL} &= 0 \\ V_{AC} < -2V_T \;;\; V_{RL} &= -V_{AC} - 2V_T \end{aligned}\right\} \quad (4.6)$$

It is apparent in equations: (4.2), (4.4) and (4.6) that a main problem of the use of simple diode rectifiers is that the voltage range of rectification is limited by the threshold voltage of diodes. We overcome this problem by adding an active device to diodes, as will be mentioned in the next sections.

4.3 Opamp rectifiers

4.3.1 An opamp half-wave rectifier

To solve the problem of the threshold voltage of simple diode rectifiers, opamps and diodes are together used. A half-wave rectifier using one opamp, two diodes and two resistors is represented in figure 4.4(a). With the highlight of the high open loop gain of the opamp, it can make the diodes conducting since the input voltage is very low voltage (much lower than the threshold voltage). Figure 4.4(b) and 4.4(c) display the operation of the opamp half-wave rectifier.

When the input voltage V_{in} of the circuit in figure 4.4(b) becomes the positive voltage, the output voltage of the opamp is the negative voltage (inverting amplifier configuration). This forces D_1 to conduct and D_2 to non-conduct. The output voltage of the opamp is roughly equal to the voltage at node A. Node A is a virtual ground node having approximately 0 V potential. Consequently, there is no the output voltage V_{out} in this case.

When the input voltage V_{in} becomes the negative voltage according to figure 4.4(c). The output voltage of the opamp is the positive voltage. In this case, D_2 conducts and D_1 non-conducts. The current will flow from the output of the opamp through D_2 and R_2 to node A. The output voltage V_{out} will be about the voltage that drops R_2, due to the virtual ground at node A. Ones can express the ideal operation as

$$\left.\begin{aligned} V_{in} > 0 \;;\; V_{out} &= 0 \\ V_{in} < 0 \;;\; V_{out} &= -V_{in}\frac{R_2}{R_1} \end{aligned}\right\} \quad (4.7)$$

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For the true operation, the resistance of the diode D_2 while conducting ($r_{d2(on)}$) must be taken. Thus, equation (4.7) has to become

$$\left.\begin{aligned} V_{in} > 0;\ V_{out} &= 0 \\ V_{in} < 0;\ V_{out} &= -V_{in}\frac{R_2 + r_{d2(on)}}{R_1} \end{aligned}\right\} \tag{4.8}$$

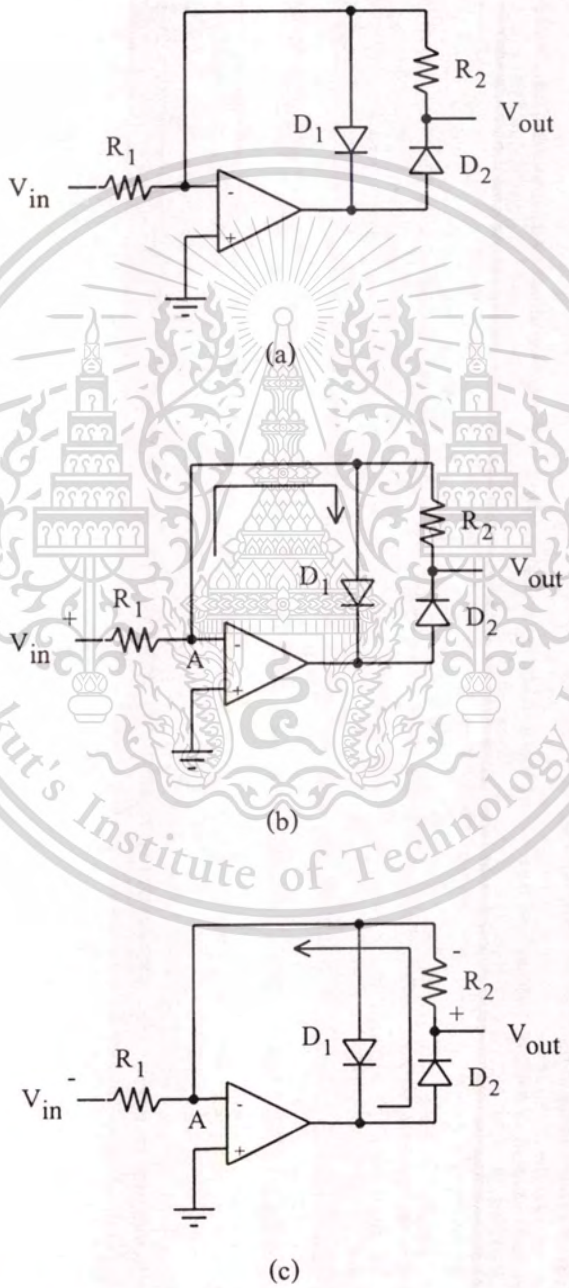

Figure 4.4 An opamp half-wave rectifier and its operation.

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4.3.2 An opamp full-wave rectifier

Figure 4.5(a) represents an opamp full-wave rectifier, which consists of two diodes, two opamps and five resistors. This circuit uses the high open loop gain of the opamp to compel the diode turning on since the very small input voltage, the same as an opamp half-wave rectifier. Figure 4.5(b) and figure 4.5(c) show the operation of the opamp full-wave rectifier. See figure 4.5 (b), it is the case of a positive input. Owing to an inverting circuit structure of the opamp 1, an output voltage of opamp 1 is the negative voltage. This makes D_2 to conduct and D_1 to non-conduct. The current will flow from node A (virtual ground) through R_2 and D_2 to the output of opamp 1 generating the voltage across R_2. The negative voltage at R_2 is the voltage at node B and is the input voltage of opamp 2, setting $R_2 = R_1$, the voltage at node B is

$$V_B = -\frac{R_2}{R_1}V_{in} = -V_{in} \tag{4.9}$$

If we consider $r_{d2(on)}$ hence V_B can be expressed as

$$V_B = -\frac{R_2 + r_{d2(on)}}{R_1}V_{in} \approx -V_{in} \tag{4.10}$$

Because R_2 is much greater than $r_{d2(on)}$.

The input positive voltage fed through R_4 is also the input voltage of opamp 2. Opamp 2 operates as an adder. The output voltage is

$$V_{out} = -\frac{R_5}{R_3}(-V_{in}) - \frac{R_5}{R_4}(V_{in}) \tag{4.11}$$

Choosing $R_1 = R_2 = R_4 = R_5$ and $R_3 = 0.5R_1$, the output voltage is the same as the input voltage,

$$V_{out} = V_{in} \tag{4.12}$$

Figure 4.5(c) is the case of the negative input voltage. The output of opamp 1 is therefore the positive voltage. This voltage drives D_1 to conduct and D_2 to non-conduct. Thus, the output voltage of opamp 1 is 0 V (node A is the virtual ground), there is no output voltage of opamp 1

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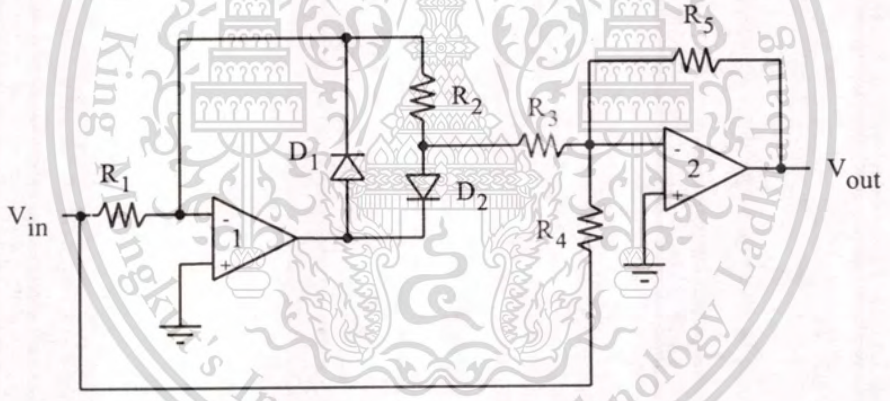
supplying to opamp 2 (V_B = 0 V). Only the input voltage supplies to opamp 2 through R_4. Setting $R_5 = R_4$, the output voltage is

$$V_{out} = -\frac{R_5}{R_4}(V_{in}) = -V_{in} \tag{4.13}$$

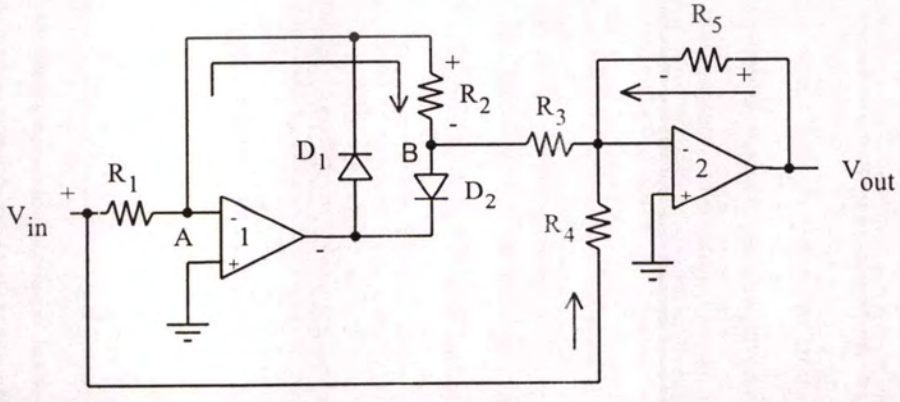
This is an inverting version of the input voltage, namely the positive voltage. The above operation equations are concluded as

$$\left.\begin{aligned} V_{in} > 0;\ V_{out} &= V_{in} \\ V_{in} < 0;\ V_{out} &= -V_{in} \end{aligned}\right\} \tag{4.14}$$

One sees that the output voltage is a positive full-wave voltage. If $r_{d2(on)}$ is considered following to (4.10), V_{out} when $V_{in} > 0$ will be higher than V_{in} a little.



(a)



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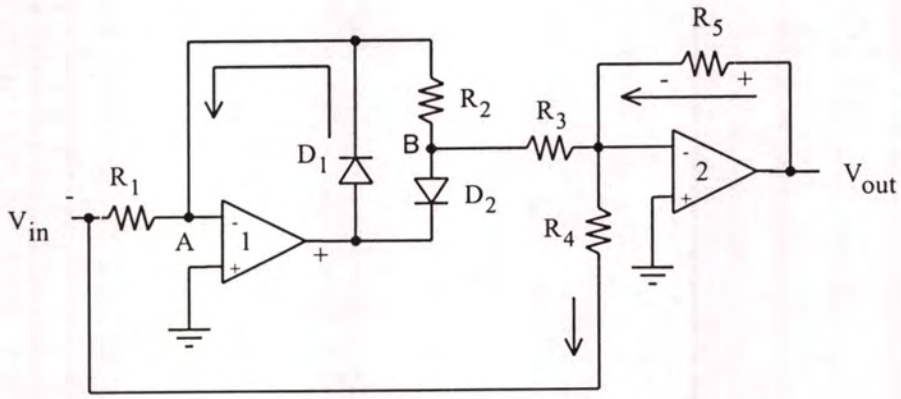

(c)

Figure 4.5 An opamp full-wave rectifier and its operation.

4.4 CCII rectifiers

A CCII rectifier is a rectifier that rectifies the signal in current form. Ones use the CCII in the voltage to current converter to change the input voltage into the current. The CCII used is the CCII+ of which the operation was already mentioned in chapter 3.

4.4.1 A CCII half-wave rectifier

Figure 4.6(a) shows a CCII half-wave rectifier using one CCII+, two diodes and two resistors. Due to the high impedance of node Y of the CCII, the rectifier has high input impedance. Because the voltage at node Y is followed to node X and the current at node X is conveyed to node Z, the output current of CCII+ in the circuit is

$$I_{out} = \frac{V_{in}}{R_1} \tag{4.15}$$

When an input voltage is the positive voltage following to figure 4.6(b), D_1 is turned on and D_2 is turned off. The output current of CCII+ will flow through D_1 and R_L making the positive voltage at R_L. As figure 4.6(c), the negative input voltage, D_1 is turned off and D_2 is turned on. The output current of CCII+ will be bypassed to ground by D_2, without the current and the voltage at R_L. That is

$$\left.\begin{aligned} V_{in} > 0;\ I_{out} &= \frac{V_{in}}{R_1} \\ V_{in} < 0;\ I_{out} &= 0 \end{aligned}\right\} \tag{4.16}$$

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The output current is converted to the output voltage by R_L, Thus if ones set $R_L = R_1$, getting

$$\left.\begin{aligned} V_{in} > 0;\ V_{out} &= I_{out} R_L = \frac{V_{in}}{R_1} R_L = V_{in} \\ V_{in} < 0;\ V_{out} &= 0 \end{aligned}\right\} \tag{4.17}$$

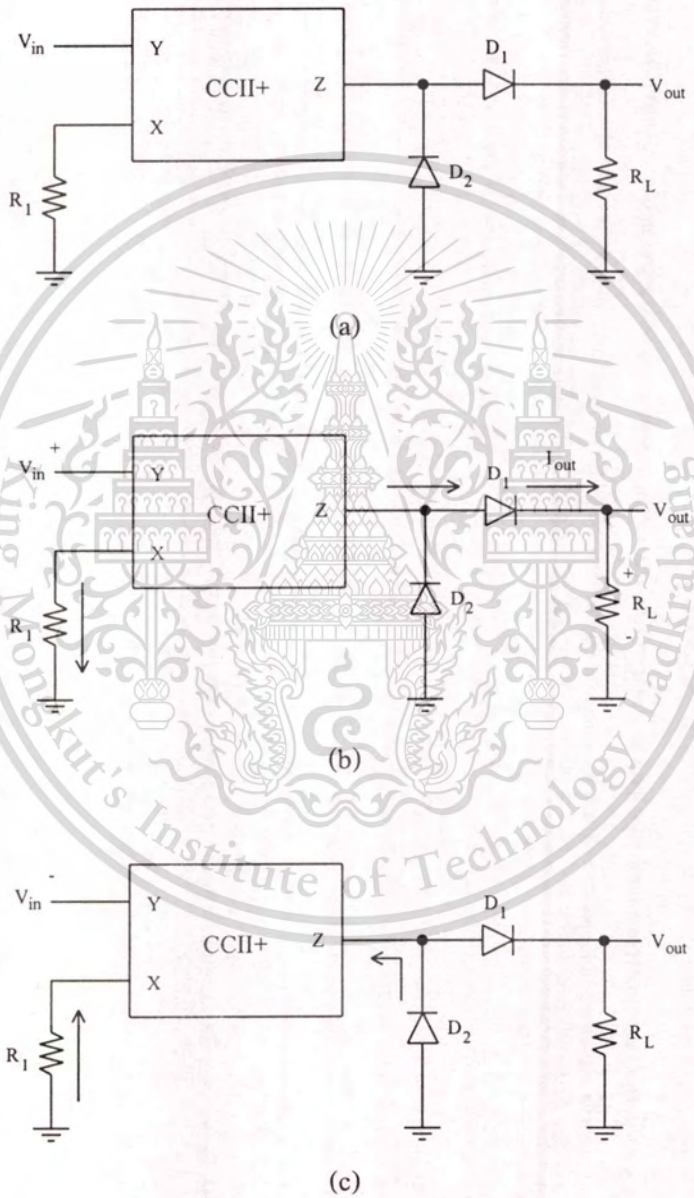

Figure 4.6 A CCII half-wave rectifier and its operation.

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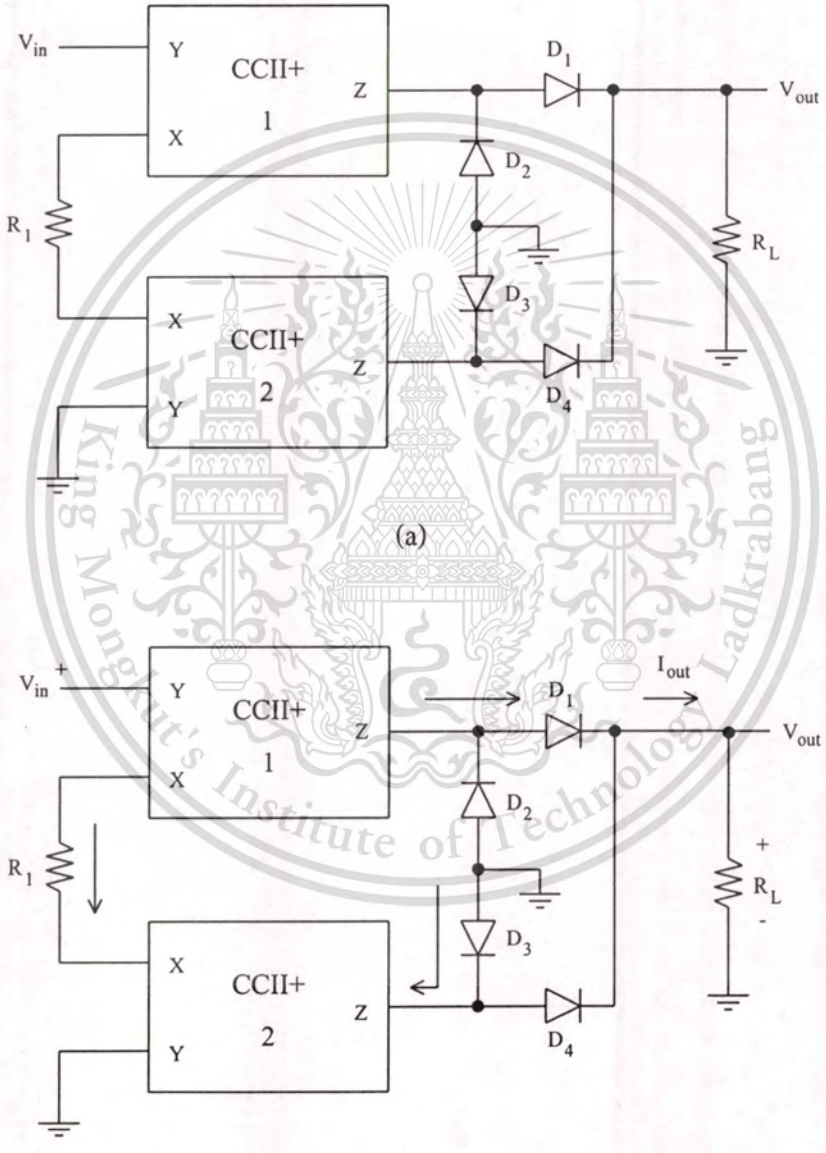
4.4.2 A CCII full-wave rectifier

Figure 4.7(a) displays a CCII full-wave rectifier that is composed of two CCII+ units, two resistors and four diodes, proposed in [6] and [8]. Note that an input voltage is fed to node Y of CCII+1, node Y of CCII+ 2 is grounded, R_1 is connected between node X of CCII+1 and that of CCII+2, the output current signal of CCII+1 is thus shifted the phase by 180 degrees from one of CCII+2.



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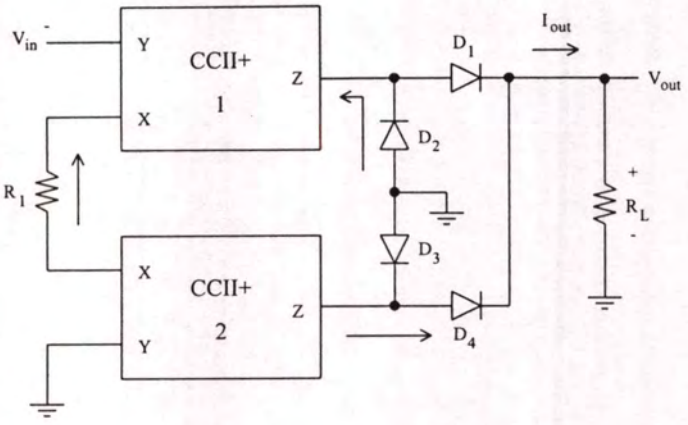

(c)

Figure 4.7 A CCII full-wave rectifier and its operation.

The operation of the CCII full-wave rectifier is shown in figure 4.7(b) and figure 4.7(c). Figure 4.7(b) is the case of the positive input voltage that makes D_1 as well as D_3 turned on, and D_2 as well as D_4 turned off. The output current of CCII+1 will flow through D_1 and R_L resulting in the positive voltage at R_L whereas the output current of CCII+2 is bypassed to ground by D_3.

The negative input voltage of figure 4.7(c) compels D_1 including D_3 to be turned off and D_2 including D_4 to be turned on. The current at R_L is the output current of CCII+2 flowing through D_4. This current creates the positive voltage dropping R_L. The output current of CCII+1 is connected to ground by D_2. Owing to R_1 at between nodes X of CCII+1 and CCII+2, the above operation can be expressed as

$$\left.\begin{aligned} V_{in} > 0;\ I_{out} &= \frac{V_{in}}{R_1} \\ V_{in} < 0;\ I_{out} &= -\frac{V_{in}}{R_1} \end{aligned}\right\} \tag{4.18}$$

The output current is converted to the output voltage by R_L; therefore, equation (4.18) can be rewritten as

$$\left.\begin{aligned} V_{in} > 0;\ V_{out} &= I_{out} R_L = \frac{V_{in}}{R_1} R_L = V_{in} \\ V_{in} < 0;\ V_{out} &= I_{out} R_L = -\frac{V_{in}}{R_1} R_L = -V_{in} \end{aligned}\right\} \tag{4.19}$$

by using $R_L = R_1$.

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4.4.3 Problem of the on/off transition of diodes and its improvement

Although rectifying a signal in the current mode can correct the problem of the threshold voltage, the problem of the on/off transition of diodes is still existed. The on/off transition problem of diodes results from the capacitance at P-N junctions of diodes. A small signal model of the forward biased diode is shown in figure 4.8

Figure 4.8(a) is the full small signal model of the forward biased diode [9]. It comprises an incremental resistance of the diode r_d, a diffusion capacitance C_d, and a depletion capacitance C_j. Generally, C_d is much larger than C_j, thus, ones get the simplified small signal model as figure 4.8 (b)

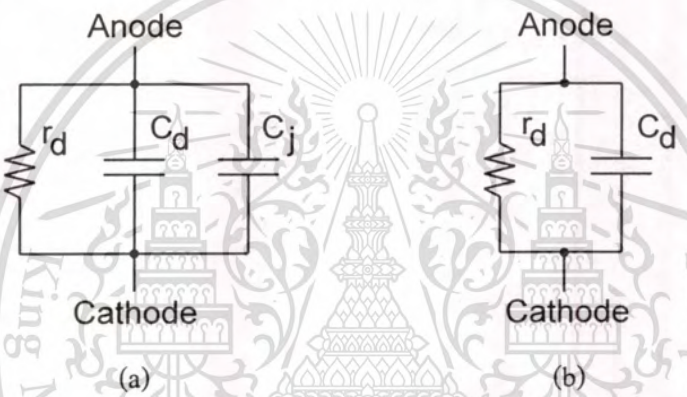

Figure 4.8 Small signal model of the forward biased diode (a) full model and (b) simplified model.

Figure 4.9 displays the small signal model of the reverse biased diode [9] that consists of only an average junction capacitance $C_{j\text{-}av}$ depending on the junction area. When we analyze the reverse biased diode including the forward biased one, the $C_{j\text{-}av}$ can be neglected because its capacitance is much smaller than the C_d of the forward biased diode.

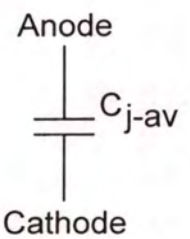

Figure 4.9 Small signal model of the reverse biased diode.

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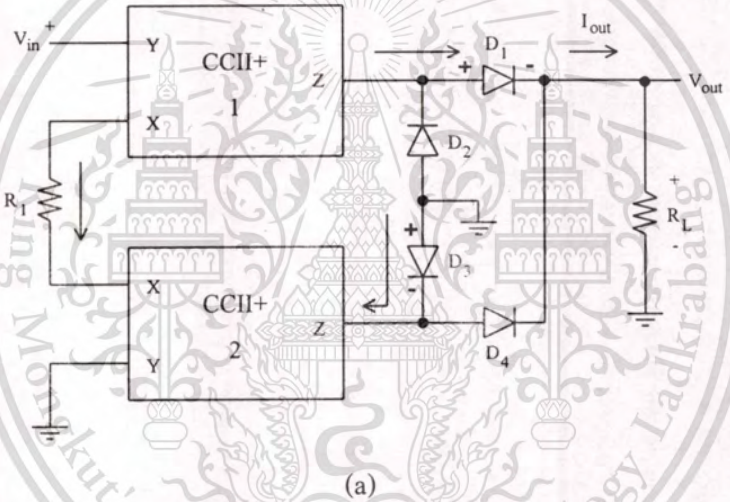
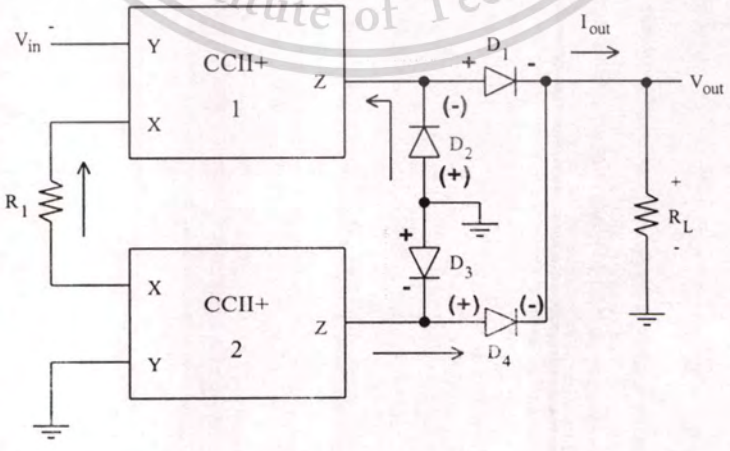
Reanalyzing the operation of the CCII full-wave rectifier with the small signal model capacitance and resistance, this operation is shown in figure 4.10. One uses the simplified small signal model of the forward biased diode in figure 4.8(b), and neglects the capacitance of the reverse biased diode since this capacitance is much smaller than the capacitance of the forward biased diode. Assuming that, at the first time, the small signal model capacitance of all diodes has no the electron charge. When the positive input voltage applied as shown figure 4.10(a), the currents flowing in the circuit charge C_d of D_1 and D_3. When the input voltage becomes the negative voltage as shown in figure 4.10(b). The currents flowing through D_2 and D_4 will not immediately occur because the currents have to first discharge C_d of D_1 and D_3 (discharge currents substituted by dotted line arrows). After the currents flow through D_2 and D_4, their C_d



(a)



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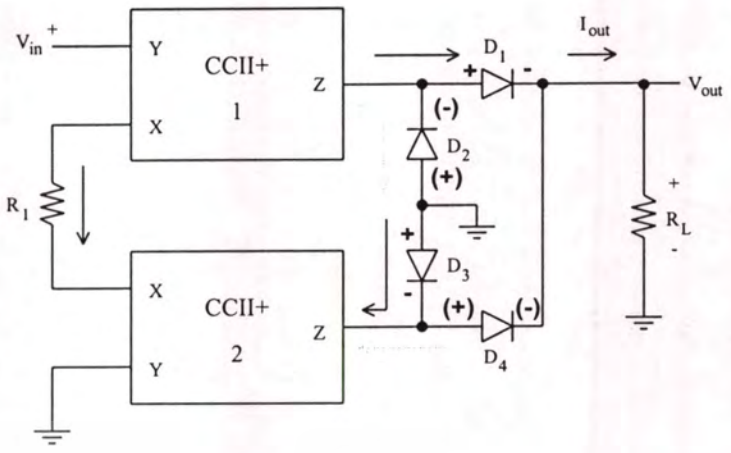

(c)

Figure 4.10 Operation of the CCII full-wave rectifier with the small signal model of the forward biased diode.

will be charged. In the same way, when the input voltage back becomes the positive voltage as shown in figure 4.10(c), the currents flowing through D_1 and D_3 will not also instantly occur because the currents must initially discharge C_d of D_2 and D_4. After the currents flow through D_1 and D_3, their C_d will be charged again. It is a loop. The result of the current that does not instantly flow through forward biased diodes when the input voltage changes from the positive to negative voltage or from the negative to positive voltage, that is missing of the output signal in the discharge times (t) as shown in figure 4.11.

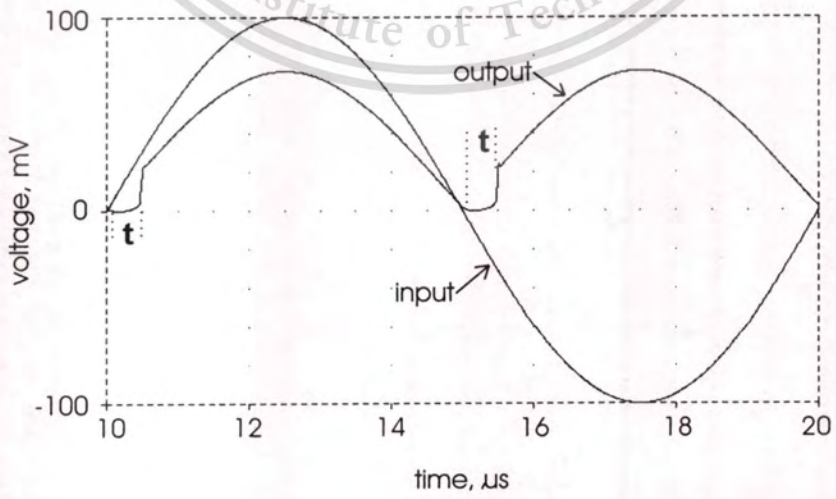

Figure 4.11 Missing of the output signal in discharge times.

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To solve the problem from the charge/discharge of the capacitance in diodes, All diodes have to be biased by the voltage in order to make them turning on all the time. The voltage biasing method was already shown in figure 1.1, one would show it again to be simple for readers in figure 4.12. Figure 4.12(a) shows the CCII rectifier without the diode biasing whereas figures 4.12(b) and 4.12(c) show the CCII rectifiers with the diode biasing. It is seen in figure 4.12(c) that it is the current biasing, really, that is the voltage biasing because the current I is converted to the voltage by the resistor R.

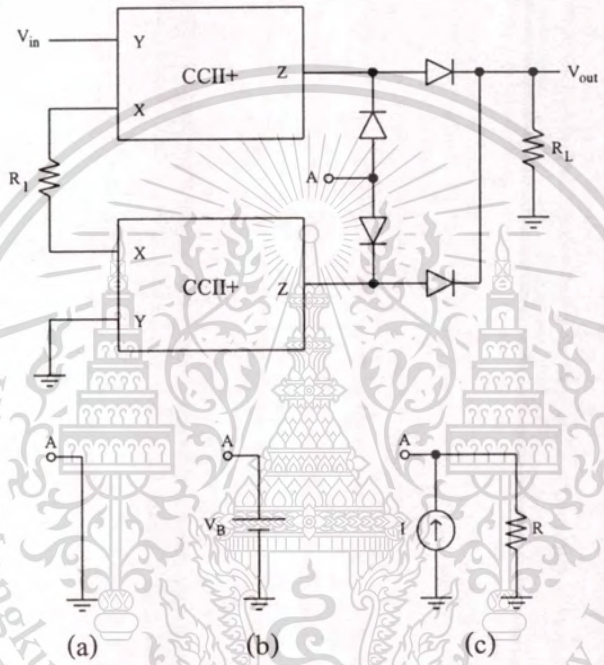

Figure 4.12 Current conveyor based precision full-wave rectifiers: (a) without biasing [6] and [8], (b) with biasing [2], and (c) with biasing [7].

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Chapter 5

Design of a full-wave rectifier using a current conveyor and current mirrors

5.1 Introduction

It is well known that a rectifier rectifying a signal in current form yields high operation frequency [2], [6]-[8]. A CCII full-wave rectifier is such rectifier that was already described in chapter 4. In this chapter, the author designs a new full-wave rectifier based on the CCII full-wave rectifiers [2], [6]-[8]. Namely the proposed full-wave rectifier uses a CCII voltage to current converter to change an input voltage to an input current, uses a current rectifier to rectify the input current, and uses a current to voltage converter to change the rectified current to the voltage. However, with the different circuit structure, the proposed rectifier yields the advantages.

- The proposed rectifier uses two grounded resistors while each of the above CCII full-wave rectifiers uses one grounded resistor and one ungrounded resistor. In IC fabrication, the realization of the grounded resistor is easier than the realization of the ungrounded resistor. Hence, the proposed rectifier is more suitable for IC fabrication than the above CCII full-wave rectifiers.
- The proposed rectifier yields better temperature stability than the above CCII full-wave rectifiers.
- The proposed rectifier can rectify lower minimum voltage than the above CCII full-wave rectifiers.

5.2 Proposed full-wave rectifier

A proposed full-wave rectifier is represented in figure 5.1. Its operation is as follows. From equation (3.8), an output current of the CCII+ (i_z) of the proposed rectifier can be written as

$$i_z = \frac{V_{in}}{R_1} \tag{5.1}$$

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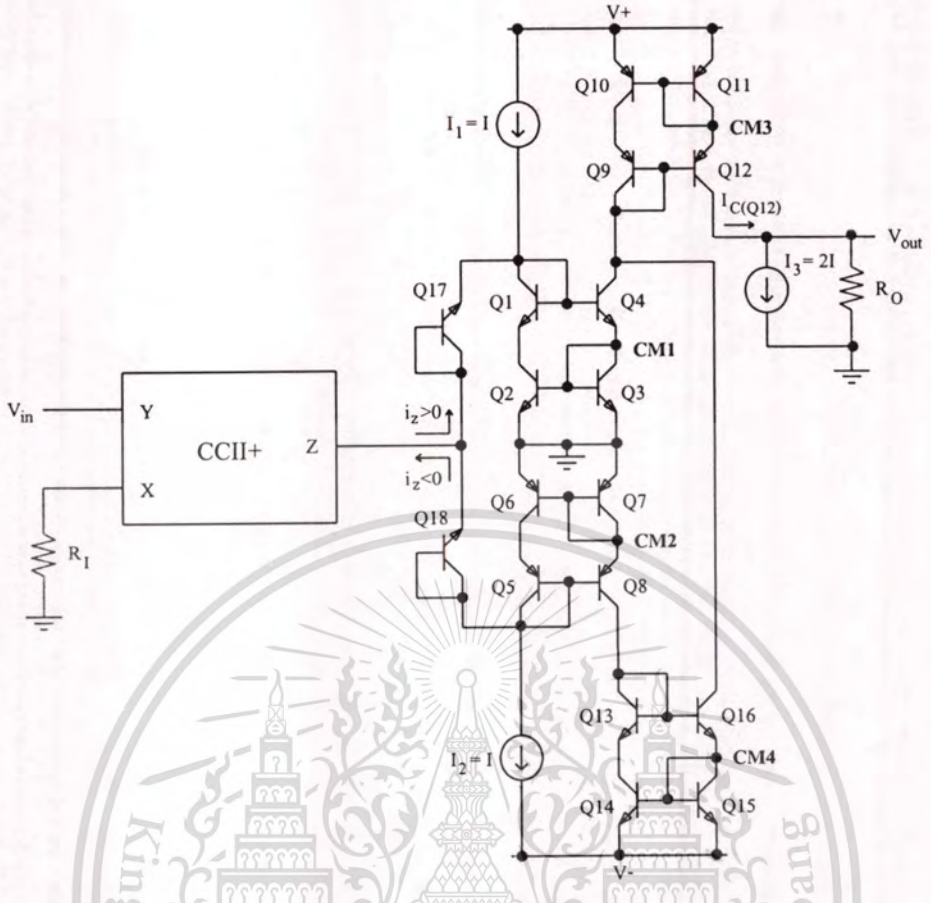

Figure 5.1 Proposed full-wave rectifier using one CCII and four current mirrors.

This current is fed into the input of a current mode full-wave rectifier. The current mode full-wave rectifier consists of four Wilson bipolar current mirrors (CM1 (Q1 to Q4), CM2 (Q5 to Q8), CM3 (Q9 to Q12), and CM4 (Q13 to Q16)); two transistor-diodes (Q17 and Q18); and three constant current sources (I_1, I_2, and I_3). The Q17 and Q18 operate as diodes to protect the short circuit between I_1 and I_2. The constant current sources, $I_1 = I_2 = I$, mean that the transistors in CM1 to CM4 are turned-on all the time, reducing the problem during the non-conduction/conduction transition of these transistors. Both I_1 and I_2 create an offset current (2I) through R_O. To eliminate this offset current at R_O, we exploit $I_3 = 2I$ at the output of the proposed rectifier.

The operation of the current mode full-wave rectifier is as follows: When $i_z > 0$, it is fed through Q17 and then is mirrored by CM1 to the collector of Q4 as $-i_z$, this $-i_z$ is again mirrored by CM3 to the collector of Q12 as $+i_z$. In addition, when $i_z < 0$, it is fed through Q18 and then is mirrored by CM2 to the collector of Q8 as $-i_z$, this $-i_z$ is second mirrored by CM4 to the collector of Q16 as $+i_z$, and this $+i_z$ is third mirrored by CM3 to the collector of Q12 as

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$-i_z$. From the operation of the current mode full-wave rectifier explained, the relations between the input current (i_z) and the output current at the collector of Q12 ($I_{C(Q12)}$) can be expressed as

$$\left.\begin{aligned} i_z > 0;\ I_{C(Q12)} &= +i_z + 2I \\ i_z < 0;\ I_{C(Q12)} &= -i_z + 2I \end{aligned}\right\} \tag{5.2}$$

The offset, $2I$, in equation (5.2) is compensated by using I_3. Thus we can write the relations between i_z and the output current (I_{R_O}) as

$$\left.\begin{aligned} i_z > 0;\ I_{R_O} &= +i_z \\ i_z < 0;\ I_{R_O} &= -i_z \end{aligned}\right\} \tag{5.3}$$

Using equation (5.1) and $R_O = R_I$, we get the relations between the input and the output voltages of the proposed rectifier as

$$\left.\begin{aligned} V_{in} > 0;\ V_{out} &= +V_{in} \\ V_{in} < 0;\ V_{out} &= -V_{in} \end{aligned}\right\} \tag{5.4}$$

It is evident that the proposed rectifier operates as the full-wave rectifier.

5.2.1 Error from the resistance at node X of the CCII

The resistance at node X of the CCII (see figure 3.6) is ideally 0 Ω. In fact, it is not 0 Ω for the practical current conveyer. Therefore equation (5.1) can be rewritten as

$$i_z = \frac{V_{in}}{R_I + R_x} \tag{5.5}$$

This leads to the operation the same as equation (5.4) where $R_L = R_I + R_x$.

5.2.2 Error from Wilson bipolar current mirrors

The error of Wilson bipolar current mirrors is one error of the proposed rectifier, i.e. the input and output currents of the Wilson bipolar current mirror [11] is given by

$$I_{out} = \frac{I_{in}}{1 + \left(2/\beta^2\right)} \tag{5.6}$$

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where β is the current gain of all the transistors in Wilson bipolar current mirrors. When Vin > 0, the output current of CCII+ is $i_z > 0$ that is mirrored by CM1 and CM3. Furthermore, when Vin < 0, the output current of CCII+ is $i_z < 0$ that is mirrored by CM2, CM4, and CM3. Hence, one can write the relations between the input and the output voltages with the error from Wilson bipolar current mirrors as

$$\left.\begin{aligned} V_{in} > 0;\ V_{out} &= \frac{+V_{in}}{\left(1+(2/\beta^2)\right)^2} \\ V_{in} < 0;\ V_{out} &= \frac{-V_{in}}{\left(1+(2/\beta^2)\right)^3} \end{aligned}\right\} \tag{5.7}$$

5.2.3 Input impedance

Because an input is only fed into node Y of the CCII, the input impedance is consequently the impedance at node Y of the CCII (see figure 3.6)

$$Z_{in} \cong R_y \tag{5.8}$$

5.2.4 Output impedance

The output impedance of the Wilson bipolar current mirror [11] in equation (2.37) is

$$r_{out} \cong \frac{\beta r_o}{2}$$

where r_o is the resistance between the collector and emitter of the transistor. For the proposed rectifier, all NPN transistors have the same β_{NPN} and all PNP transistors have the same β_{PNP}. The r_{oNPN} and r_{oPNP} are determined as the resistance between the collector and emitter of NPN and PNP transistors. The output impedance of the proposed rectifier is thus

$$Z_{out} \cong \frac{\beta_{PNP} r_{oPNP}}{2} // r_{o3} // R_O \tag{5.9}$$

where r_{o3} is the output resistance of I_3.

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5.2.5 Operation frequency

From the above operation of the proposed rectifier, to solve the on/off transition problem, the proposed rectifier uses I_1 to make the transistors in CM1 turning on all the time and also uses I_2 for the transistors in CM2. The use of I_1 and I_2 leads to the use of transistor-diodes, Q17 and Q18, to protect no flowing through CM1 and CM2 of I_1 and I_2. Additionally, the use of I_1 and I_2 results in the offset current 2I at the output, which is subtracted by using I_3. Although the on/off transition problem of CM1 and CM2 is cleared, the fewer on/off transition problem of Q17 and Q18 is a new problem.

Due to the proposed rectifier designed for the small signal rectification in analog signal processing, an operation frequency of the proposed rectifier is limited by the on/off transition problem of Q17 and Q18, resulting from the capacitance in the small-signal model of diodes as already mentioned in section 4.4.3. The proposed rectifier uses bipolar transistors in place of diodes, which the simplified small-signal model of the bipolar transistor [9] with the collector and the base jointly connected, operating as the diode, is shown in figure 5.2. This small-signal model is like the small-signal model of the diode in figure 4.8 (b), $C_{be} = C_d$ and $r_\pi // r_o = r_d$.

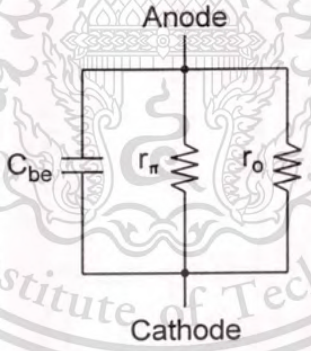

Figure 5.2 Simplified small-signal model of the bipolar transistor operating as the diode.

5.2.6. Operation voltage range

Because one uses the low value of R_1 to obtain the high value of i_z in order to reduce the error at the zero crossing of the output signal from the conduction/nonconduction transition problem of Q17 and Q18. The operation voltage range of the proposed rectifier thus depends upon the operation range of the CCII+ in the voltage to current converter that is limited by the maximum current $i_{z(max)}$ of CCII+.

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5.2.7 Temperature stability

Most effect of the temperature on the current conveyor rectifier is the minimum output voltage problem to be up to the temperature [7]. For the proposed rectifier, the minimum output voltage depends on three constant current sources I_1, I_2, and I_3 (see section 5.2) that are realized by Wilson bipolar current mirrors as shown in figure 5.3

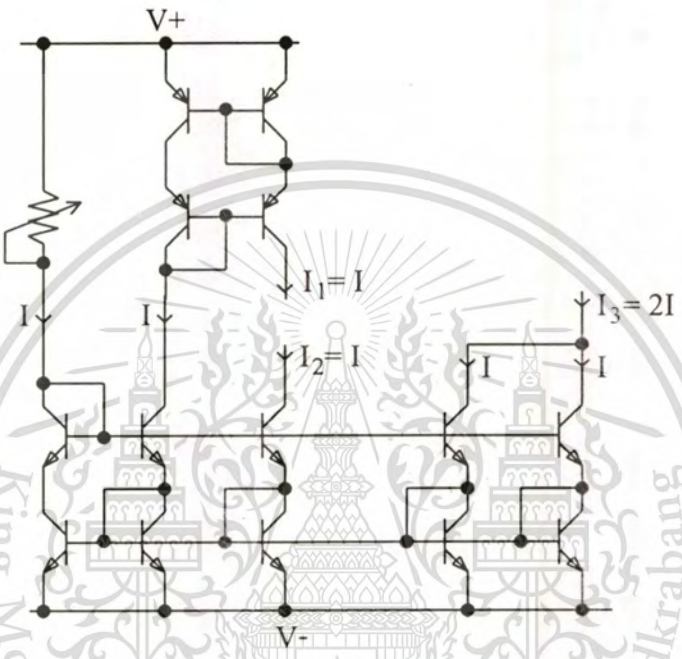

Figure 5.3 Constant current source circuit of the proposed rectifier.

Assuming all transistors are identical. When the temperature T changes to

$$T \Longrightarrow T + \Delta T \tag{5.10}$$

making the currents

$$I_1 \Longrightarrow I + \Delta I \tag{5.11}$$

and

$$I_2 \Longrightarrow I + \Delta I \tag{5.12}$$

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From the operation of the proposed rectifier explained previously, when the temperature changes, I_1 and I_2 produce the output offset current

$$I_{offset} = 2I + 2\Delta I \tag{5.13}$$

which is compensated by I_3, when the temperature changes, I_3 can be expressed as

$$I_3 = 2I + 2\Delta I \tag{5.14}$$

The minimum output voltage is

$$V_{out(\min)} = \left(I_{offset} - I_3\right)R_O \tag{5.15}$$

Equations (5.13) and (5.14) show that I_{offset} and I_3 are still equal therefore there is no changing the minimum output voltage (5.15) when the temperature changes. Practically, NPN and PNP transistors are not identical, only closely matched, this dose not makes I_{offset} and I_3 being quite equal. The minimum output voltage changes very small in this case.

5.3 Results

To verify the theoretical design, the proposed full-wave rectifier was simulated by using the PSPICE program. We use the current conveyor CCII+ in the current feedback opamp AD844 [20] and use the NPN and PNP transistors, 2N3904 and 2N3906 respectively. All these device models are obtained from the PSPICE library. The supply voltage used is $\pm$ 10 V(from data sheet of AD844, supply voltages between $\pm$ 4.5 V and $\pm$ 18 V can be chosen). The constant current sources employed are $I_1 = I_2 = 100$ μA and $I_3 = 200$ μA, these current sources were built by using only one current source that supplies the current through the unity and double gain current mirrors, see figure 5.3. The $R_I = R_O = 100$ Ω were chosen.

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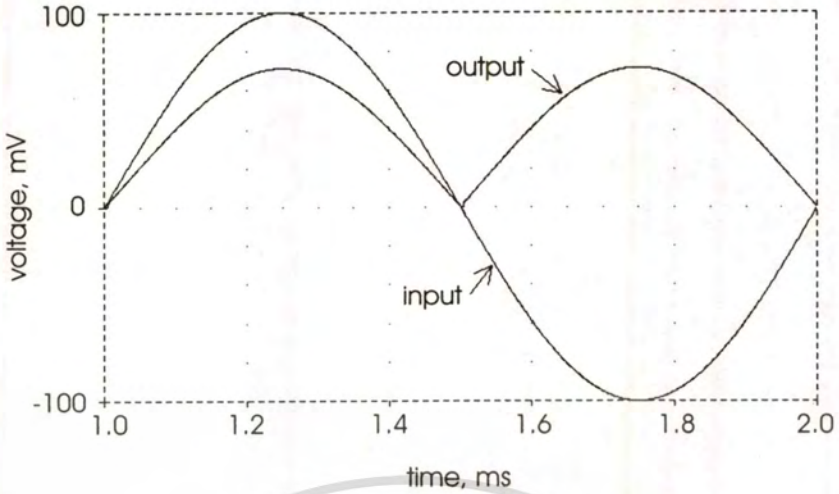
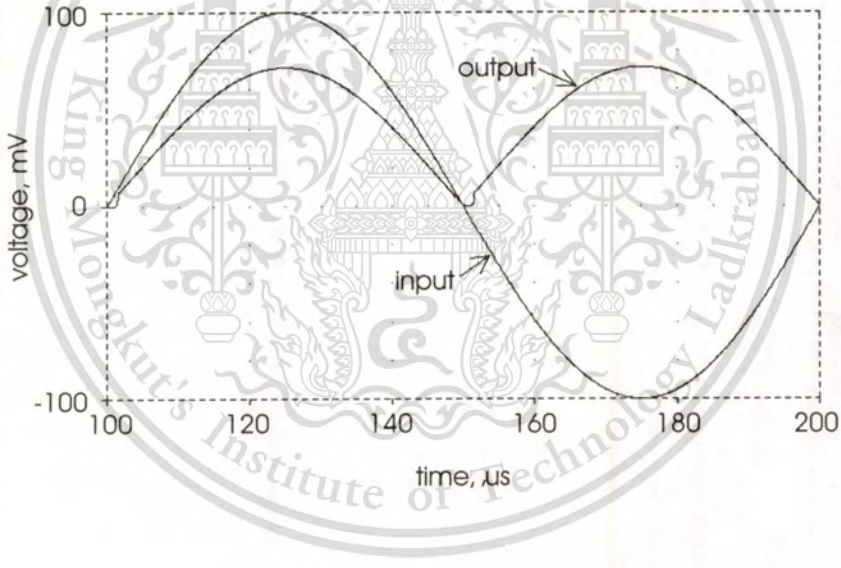


(a)



(b)

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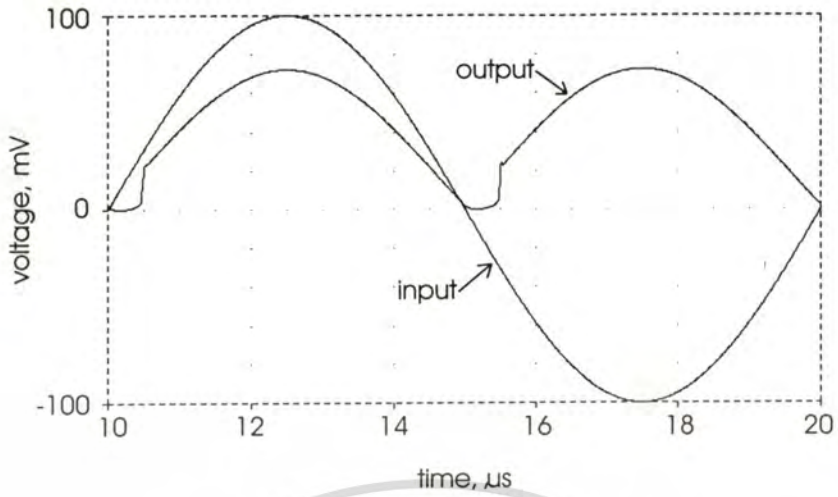

(c)

Figure 5.4 Simulated output and input signals at the frequencies of (a) 1 kHz, (b) 10 kHz and (c) 100 kHz.

Figure 5.4 shows the sine wave input signals (100 mV_{peak}) and output signals of the proposed full-wave rectifier at the frequencies of 1 kHz, 10 kHz and 100 kHz. The clear output wave form without missing of the signal was found at the frequency of 100 Hz. Comparing the proposed rectifier with rectifiers: [2] and [7] for the operation frequency, of course, because the on/off transition problem of Q17 and Q18 of the proposed rectifier is still existed, the operation frequency of the proposed rectifier will be lower. Note that from the output signals in figure 5.4, the limit of the operation frequency of the proposed rectifier is the error at zero-crossing due to the on/off transition problem of Q17 and Q18. This error affects the small signal more than the large signal, so the operation frequency for the large signal will higher than that for the small signal.

At the 100 kHz output signal in figure 5.4(c), the minimum rectified output voltage of 94 μV was observed. Whereas the minimum rectified output voltages for the rectifiers [2] and [7] are 16 mV and 8 mV, respectively, as reported by Hayatleh *et al.* [7]. Additionally, at this 100 kHz frequency, the magnified zero crossing ranges of the output signals at temperatures 27°C, 50°C, and 70°C are shown in figure 5.5. They show that the difference of the lowest output voltages between 27°C and 50°C is 40 μV and that between 50°C and 70°C is 36 μV. Whereas Hayatleh *et*

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al. [7] reported that the difference of the lowest output voltages of the rectifier [2] between 27°C and 50°C is 32 mV and that between 50°C and 70°C is 38 mV. Further, Hayatleh *et al.* [7] reported that the difference of the lowest output voltages of their rectifier between 27°C and 50°C is 8 mV and that between 50°C and 70°C is 12 mV. To be simple for readers, these minimum output voltages are concluded in table 5.1. All the above in this section shows the better performance in minimum voltage rectification and temperature stability of the proposed rectifier.

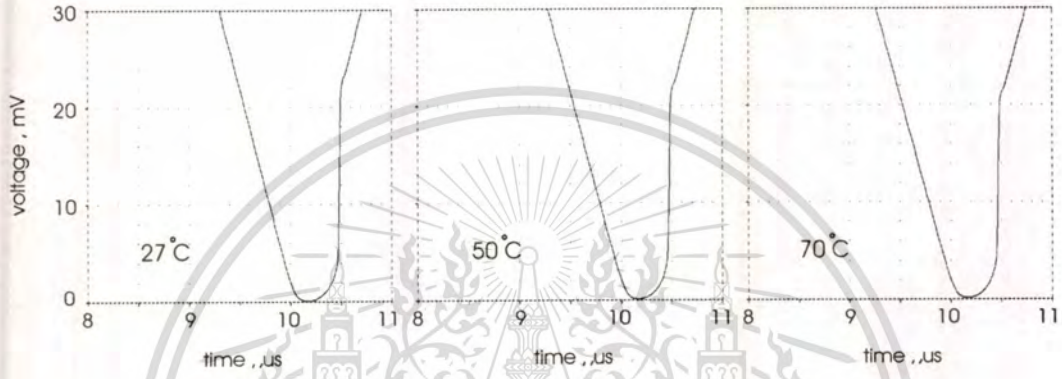

Figure 5.5 Temperature stability of the proposed rectifier.

The amplitude error of the output voltage signals in figure 5.4 results from three factors. The first factor is the non-ideal of the current conveyor, i.e. the input resistance at node X of the current conveyor in AD844 is 50 Ω [20], ideally, it must be 0 Ω. The second factor is the error of the Wilson bipolar current mirrors in the proposed rectifier. The other factor is the on/off transition problem of Q17 and Q18. These factors were already explained in section 5.2.

Rectifiers	Minimum output voltages at some temperatures				
	0°C	27°C	50°C	70°C	100°C
Proposed	50 μV	94 μV	134 μV	170 μV	225 μV
[2]	NA	16 mV	48 mV	86 mV	NA
[7]	NA	8 mV	16 mV	28 mV	NA

Table 5.1 Minimum output voltages of the proposed rectifier and of rectifiers in [2] and [7] at some temperatures.

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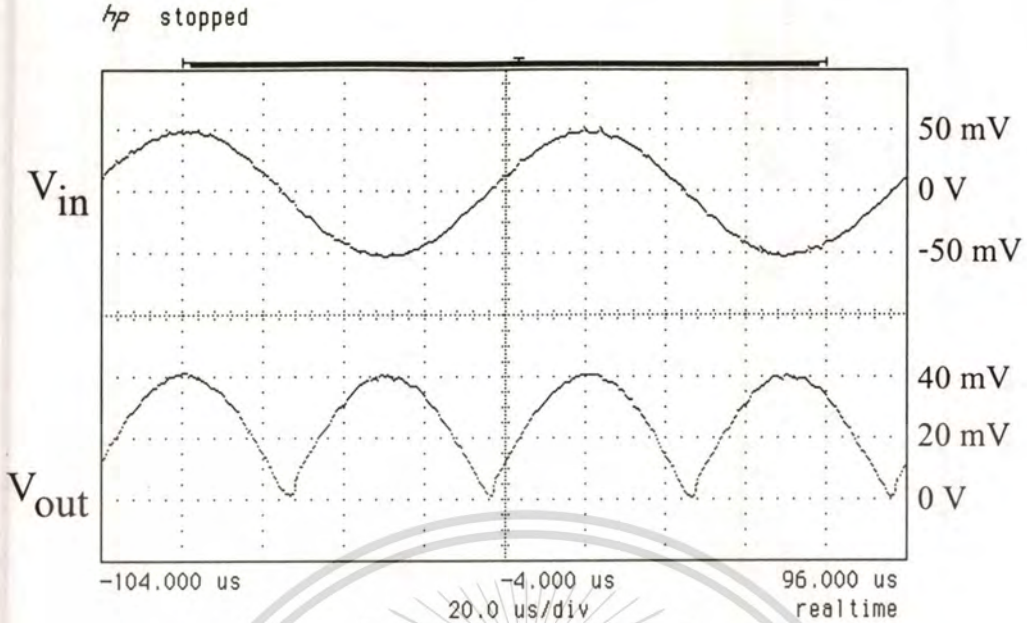
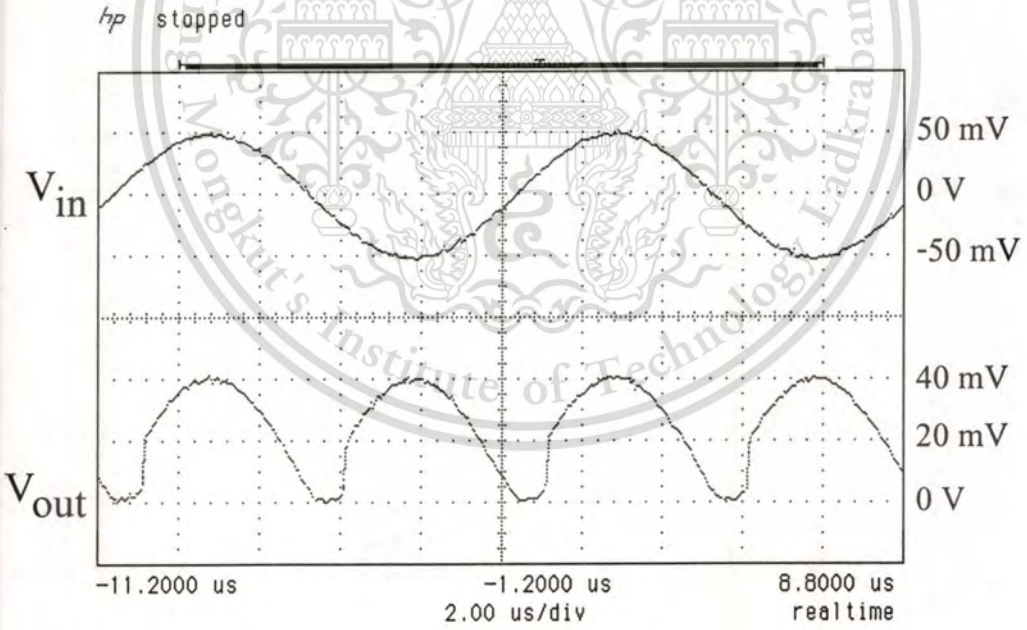


(a)



(b)

Figure 5.6 Input sine wave (50 mV_{peak}) and output waveforms of the proposed rectifier from experiment at the frequencies of (a) 10 kHz and (b) 100 kHz.

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The simulated rectifier was also constructed. Figure 5.6(a) shows the upper input waveform (50 mV/div) and the lower output waveform (20 mV/div) of the proposed rectifier at the frequency of 10 kHz, and figure 5.6(b) shows the waveforms at the frequency of 100 kHz. These experimental results correspond to simulation results.

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Chapter 6

Design of a CMOS dual output half-wave rectifier

6.1 Introduction

In section 5.1, we have known that rectifying a signal in the current form yields an operation frequency advantage. An approach is that an input voltage signal will be converted to a current signal. This current signal will be rectified and a resultant signal will be back converted to an output voltage signal. Chapter 5 has presented a full-wave rectifier that rectifies the signal in the current form with the bipolar transistor technology. In this chapter, the author presents a half-wave rectifier yielding both positive and negative half-wave outputs with the MOS transistor technology, which yields the advantages; compared with the current conveyor rectifiers [2], [6]-[8]; as follows.

- Each of the above current conveyor rectifiers uses a resistor and two current conveyors as devices in its V-I converter while the proposed rectifier uses the dual output all MOS V-I converter that is specially designed. Hence, the number of devices used in the proposed rectifier is much fewer. Further, the proposed rectifier is more suitable for integrated circuit fabrication than the above current conveyor rectifiers. (i.e. it needs no passive resistor).
- Each of the above current conveyor rectifiers employs a high supply voltage (needed by current conveyors) and has a low operating frequency (dependent on the operating frequencies of current conveyors). With the advantage of the specially designed V-I converter, the proposed rectifier employs only a $\pm$ 1.2 V supply voltage and provides an operating frequency up to 100 MHz (simulated result with 0.5 μm MOS model obtained through MIETEC)
- Each of the above current conveyor rectifiers uses the stable diode bias voltage to bias diodes in the rectifier in order to make the diodes turn on all the time. This voltage is equal to approximately $2V_T$, where V_T is the threshold voltage of the diodes. Furthermore, this voltage must be the minimum voltage to obtain the minimum offset voltage at output. Unfortunately, V_T depends upon the temperature: when the temperature increases, it causes an offset voltage at the output; inversely, when the temperature decreases, it causes diodes not to turn on all the time. The proposed

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rectifier uses the diode bias voltage at the series two diodes, $2V_T$. This voltage depends on the temperature of diodes being the same as the voltage $2V_T$ of the series two diodes in the bridge. Thus, the proposed rectifier has much better temperature stability than either of above current conveyor rectifiers.

6.2 MOS transistor

Presently, the most popular technology for realizing microcircuits makes use of MOS transistors. MOS circuits normally use two complementary types of transistors, n-channel and p-channel. While n-channel devices (NMOS) conduct with a positive gate voltage, p-channel devices (PMOS) conduct with a negative gate voltage. Moreover, electrons are used to conduct current in n-channel transistors, while holes are used in p-channel transistors. Microcircuits containing both n-channel and p-channel transistors are called CMOS circuits.

Figure 6.1 Symbols of (a) NMOS and (b) PMOS.

In circuit drawing, many symbols of MOS transistors have been used. Figure 6.1 shows the symbols used in the thesis. MOS transistors are actually four-terminal devices. These terminals are a gate (G), a drain (D), a source (S) and a bulk or substrate. But, in the symbols, only three terminals are shown because bulks are connected to the sources within MOS transistors. MOS transistors use the gate-source voltage (V_{GS}) controlling the drain-source current (I_D). The gate is physically separated from the channel by a thin insulator thus there is no the gate current. The drain current of MOS transistors [9] is given by two equations:

$$I_D = \mu C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{6.1}$$

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for operating in the triode region ($V_{GS} > V_t$, $V_{DS} < V_{eff}$), and

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_t)^2\left[1 + \lambda(V_{DS} - V_{eff})\right] \tag{6.2}$$

for operating in the active region ($V_{GS} > V_t$, $V_{DS} \geq V_{eff}$),

where μ is the mobility of carriers, C_{ox} is the gate capacitance per unit area, W is the gate width, L is the gate length, V_t is the MOS threshold voltage, V_{DS} is the drain-source voltage, V_{eff} is V_{GS} - V_t, and λ is the output impedance constant.

6.3 Current mirror, class AB amplifier, and current conveyor

Current mirrors using MOS transistors are divided into NMOS and PMOS types as shown in figure 6.2. The same characteristic NMOSs are used for the NMOS current mirror and the same characteristic PMOSs are used for the PMOS current mirror. Owing to gates connected to drains, and the same gate-source voltages of the pairs of NMOSs and PMOSs, all MOS transistors operate in the active region. Practically, λ is very low. Thus, the drain currents of two NMOSs are approximately equal and those of two PMOSs are approximately equal as well.

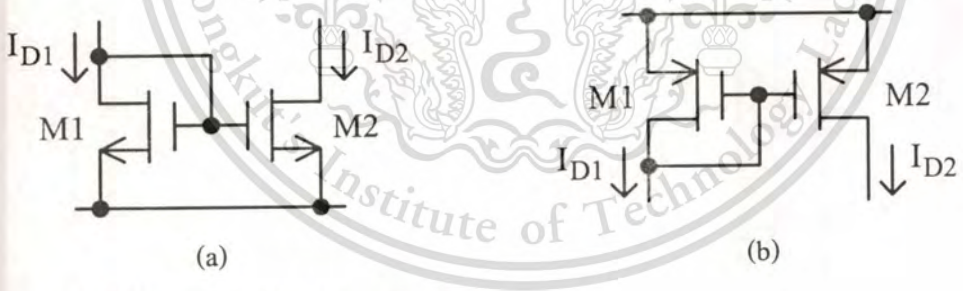

Figure 6.2 (a) NMOS and (b) PMOS current mirrors.

The other application of MOS transistors is to realize a class AB amplifier that consists of two NMOSs, two PMOSs and two constant current sources as shown in figure 6.3. All the MOS transistors in the amplifier are closely matched and all constant current sources are set as $I_1 = I_2 = I_B$. Because of a balance circuit structure of the class AB amplifier, while node X without a load, $I_1 = I_2 = I_{DN} = I_{DP}$, this means that M1 and M2 as well as M3 and M4 work as current mirrors, hence

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$$V_X = V_Y \tag{6.3}$$

When node X is connected to the load, the voltage at node X will be lower than the voltage at node Y. The shift in between input and output voltages depends on the resistance at node X, output impedance for operating of the amplifier as a buffer. This impedance will be low, good case, if $I_1 = I_2 = I$ being high is set.

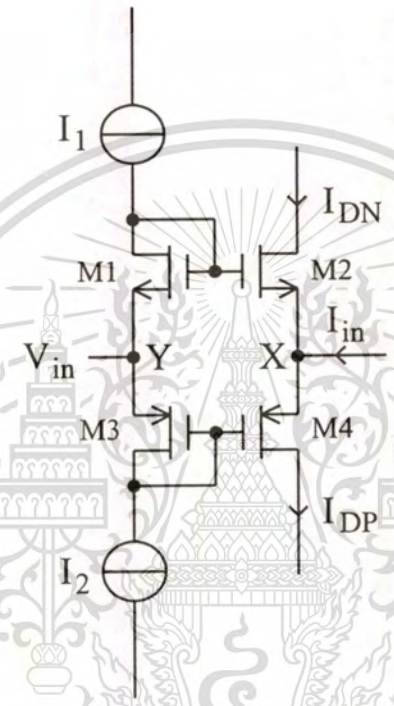

Figure 6.3 CMOS class AB amplifier.

The currents in the amplifier [23] are given by

$$I_{DN} = \frac{(4I_B - I_{in})^2}{16I_B} \text{ for } -4I_B \le I_{in} \le 4I_B \tag{6.4}$$

$$I_{DP} = \frac{(4I_B + I_{in})^2}{16I_B} \text{ for } -4I_B \le I_{in} \le 4I_B \tag{6.5}$$

$$I_{DN} = I_{in}; I_{DP} = 0 \quad \text{for } I_{in} < -4I_B \tag{6.6}$$

$$I_{DP} = I_{in}; I_{DN} = 0 \quad \text{for } I_{in} > 4I_B \tag{6.7}$$

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It is the fact from the amplifier at node X that I_{in} is equal to I_{DP} - I_{DN} both in case (6.4) including (6.5) and in case (6.6) as well as (6.7). Consequently, if we combine one class AB amplifier, two NMOS current mirrors, and two PMOS current mirrors as the circuit in figure 6.4, we will get a new circuit operating as a second generation current conveyor (CCII+) with two nodes Z.

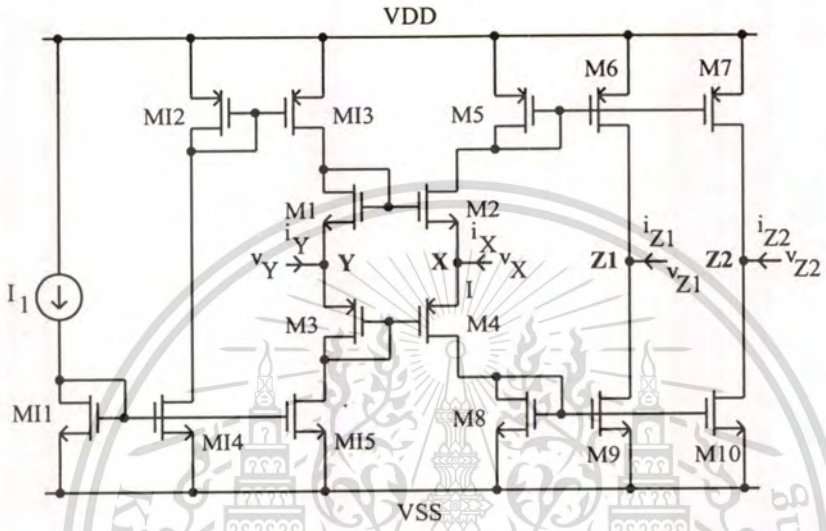

Figure 6.4 Second generation current conveyor using a class AB amplifier and current mirrors.

From section 3.3, three characteristics of the CCII+ are as follows. First, the current flowing into node Y is zero. From the CCII circuit in figure 6.4, $V_{DD} = -V_{SS}$, all MOS transistors are closely matched, I_1 is mirrored by MI1, MI4, MI2 and MI3 as the drain current of M_1, and is mirrored by MI1 and MI5 as the drain current of M3. Thus, the drain currents of M1 and M3 are equal. This makes that there is no the current flowing into node Y.

Second, the voltage at node X is equal to the voltage at node Y. Due to the same drain currents of M1 and M3 and the same characteristics of all MOS transistors, the voltage at node Y is followed to node X (6.3).

Other, the current flowing into node Z (i_Z) is equal to the current flowing into node X (i_X). Considering node X, i_X is the sum of the drain currents of M2 ((6.4) and (6.6)) and M4 ((6.5) and (6.7)). Both drain currents are mirrored by PMOS current mirror (M5 and M6) and by NMOS current mirror (M8 and M9) to node Z1, and are also mirrored by PMOS current mirror (M5 and M7) and by NMOS current mirror (M8 and M10) to node Z2. Therefore i_X, i_{Z1} and i_{Z2} are equal.

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6.4 MOS resistor

MOS resistor [24] using two NMOSs is shown in figure 6.5. Its operation is as follows. MOSs MA and MB having the same characteristics remain in the saturation region. An input current i is applied to the node between a source of MA and a drain of MB (node A). Neglecting a λ parameter (λ = 0), because it is very low value, the drain currents of MA and MB can be expressed as

Figure 6.5 MOS resistor using two NMOSs.

$$I_{D(MA)} = \frac{K}{2}(V_{DD} - V_A - V_t)^2 \tag{6.8}$$

$$I_{D(MB)} = \frac{K}{2}(V_A - V_{SS} - V_t)^2 \tag{6.9}$$

where $K = \mu C_{ox} W/L$.

Considering (6.8) and (6.9) as two square terms in the left-hand of

$$(a+b)^2 - (a-b)^2 = 4ab \tag{6.10}$$

Using KCL and the current constraint at node A, we get the result

$$V_A = \frac{I_{D(MB)} - I_{D(MA)}}{2KV_{DT}} = \frac{i}{2KV_{DT}} \tag{6.11}$$

where $V_{DT} = V_{DD} - V_t = -(V_{SS} + V_t)$, $V_{DD} = -V_{SS}$

This leads to

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$$R = \frac{1}{2KV_{DT}} \tag{6.12}$$

6.5 Proposed dual output half-wave rectifier

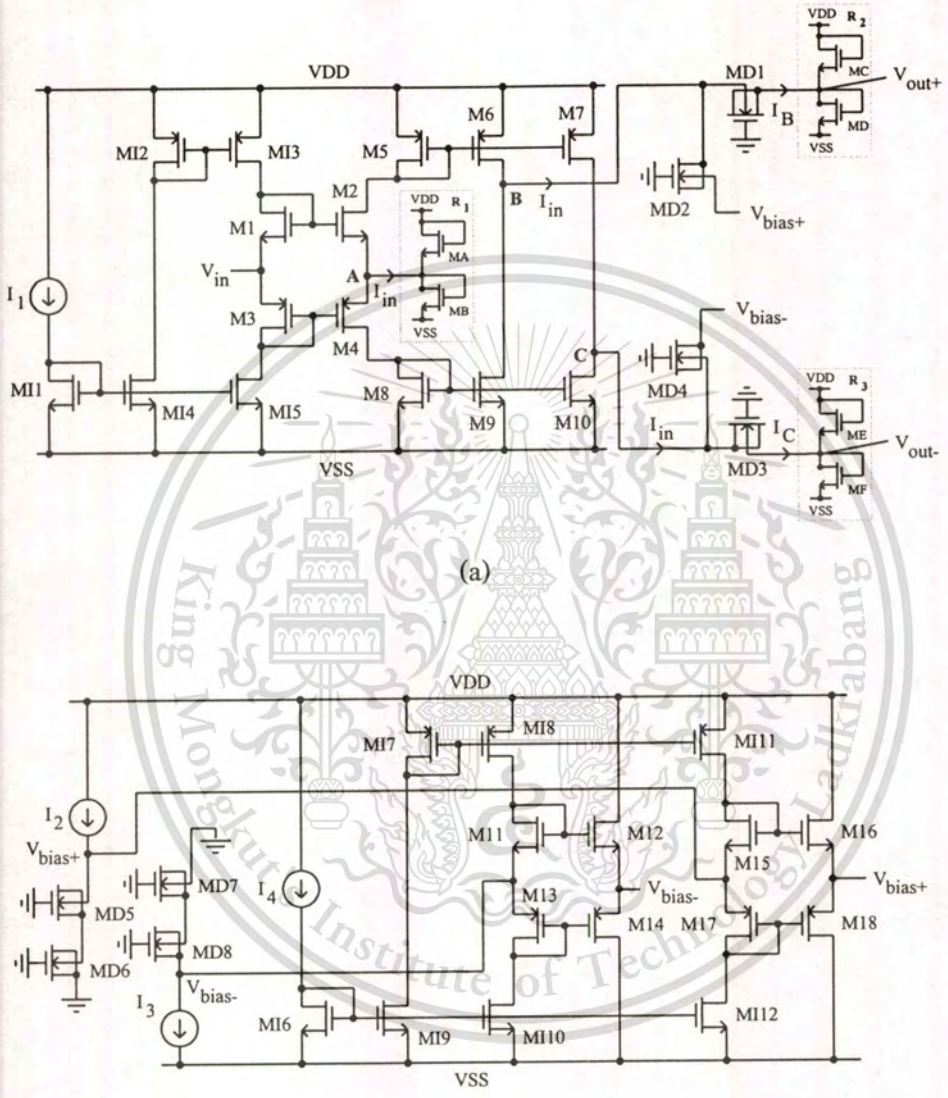

Figure 6.6 Proposed dual output half-wave rectifier: (a) rectifier; (b) bias voltage source; and (c) operation of MOS as diode.

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Figure 6.6(a) represents a proposed dual output half-wave rectifier. Note that, in the circuit, both CCII+ and MOS resistor explained above are used. An input voltage V_{in} is followed to node A (operation of CCII between nodes Y and X) producing an input current I_{in}. Exploiting (6.12), I_{in} is

$$I_{in} = V_{in}(2KV_{DT}) \tag{6.13}$$

The current I_{in} is mirrored by M5, M6, M8, and M9 to node B and is mirrored by M5, M7, M8, and M10 to node C (operation of the CCII between nodes X and Z). The current rectifiers are the positive and negative half-wave rectifiers. The MOS diodes, MD1 and MD2 (see figure. 6.6 (c)), form as the positive half-wave rectifier. Its operation is as follows. When I_{in} is positive, MD1 is turned on and MD2 turned off; for this reason, I_{in} is equal to I_B. Conversely, when I_{in} is negative, MD1 is turned off and MD2 turned on, resulting in I_{in} being bypassed into V_{bias+}; as a result, there is no I_B. The current I_B is converted to the voltage V_{out+} by the MOS resister R_2 (MC and MD). Setting $R_1 = R_2 = R_3$ with the use of the closely matched MA to MF, we can write the relation between V_{in} and V_{out+} as

$$\left.\begin{aligned} V_{in} > 0;\ V_{out+} &= V_{in} \\ V_{in} < 0;\ V_{out+} &= 0 \end{aligned}\right\} \tag{6.14}$$

The negative half-wave rectifier consists of MD3 and MD4, which operate as follows. When I_{in} is positive, MD3 is turned off and MD4 turned on, causing I_{in} to be bypassed into V_{bias-}; thus there is no I_C. Inversely, when I_{in} is negative, MD3 is turned on and MD4 turned off; therefore I_C is equal to I_{in}. This I_C is converted to the voltage V_{out-} by R_3 (ME and MF). The relation between V_{in} and V_{out-} can be expressed as

$$\left.\begin{aligned} V_{in} > 0;\ V_{out-} &= 0 \\ V_{in} < 0;\ V_{out-} &= V_{in} \end{aligned}\right\} \tag{6.15}$$

Figure 6.6(b) shows a bias voltage source. The bias voltages, V_{bias+} and V_{bias-}, are applied to make MOS diodes in the rectifiers (MD1 to MD4) turn on all the time to clad the output voltage excursions during the zero crossings for operation at high frequency. The current I_2 flowing

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through MD5 and MD6 generates V_{bias+}, and the current I_3 flowing through MD7 and MD8 produces V_{bias-}. Both V_{bias+} and V_{bias-} must be the minimum and maximum voltages, respectively, that can make MD1 to MD4 turn on all the time to get the minimum offset voltages at the outputs; that is carried out by adjusting I_2 for V_{bias+} and I_3 for V_{bias-}. To protect the effects of loads and outputs of the V-I converter on the bias voltages, the class AB voltage buffers, already mentioned above, are used. M11 to M14 are the buffer of V_{bias-}, the drain currents of M11 and M13 are made equal to I_4 by setting the same characteristics of MI6 to MI10. Similarly, M15 to M18 are the buffer of V_{bias+}; the drain currents of M15 and M17, and I_4 are made the same currents by using the same characteristics of MI6, MI7, MI9, MI11, and MI12.

At low frequencies, the input impedance [9] of the proposed half-wave rectifier is

$$r_{in} = \left(\frac{1}{g_{m1}} + r_{dsl3}\right) // \left(\frac{1}{g_{m3}} + r_{dsl5}\right) \tag{6.16}$$

where g_m is the transconductance of MOS and r_{ds} is the drain-source resistance of MOS.
In addition, the output impedance when V_{in} is positive; MD1 and MD4 are turned on, MD2 and MD3 turned off; we get

$$r_{out+} = R_2 // \left(r_{md(on)} + \left(r_{ds6} // r_{ds9}\right)\right) \tag{6.17}$$

$$r_{out-} = R_3 \tag{6.18}$$

In case V_{in} is negative; MD2 and MD3 are turned on, MD1 and MD4 turned off; we obtain

$$r_{out+} = R_2 \tag{6.19}$$

$$r_{out-} = R_3 // \left(r_{md(on)} + \left(r_{ds7} // r_{ds10}\right)\right) \tag{6.20}$$

where $r_{md(on)}$ is the resistance of MOS diodes to conduct.

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The operation voltage range of the proposed half-wave rectifier depends on the operation of M2 and M4. Namely, M2 and M4 have to operate in the active region the same as M1 and M3, leading to

$$\left.\begin{aligned} V_{in(\min)} &= V_{SS} + |V_{eff4}| + |V_{eff8}| + |V_{tp}| + |V_{tn}| \\ V_{in(\max)} &= V_{DD} - |V_{eff2}| - |V_{eff5}| - |V_{tn}| - |V_{tp}| \end{aligned}\right\} \quad (6.21)$$

It is evident in (6.21) that increasing supply voltage can expand the operation voltage range of the proposed half-wave rectifier.

6.6 Results

To verify the theoretical design, the proposed rectifier was simulated by using a PSPICE program with the 0.5 μm MOSFET model obtained through MIETEC as listed in table 6.1. The W/L parameters of MOSs and the constant current sources in the proposed rectifier are listed in Table 6.2. The supply voltage used is ± 1.2 V. The DC transfer characteristics of the proposed rectifier are shown in figure 6.7, which displays the operating voltage range from -300 mV to 300 mV of the input voltage. In this range, the power consumption of approximately 1.8 mW was observed. The magnified zero crossings of figure 6.7 are shown in figure 6.8. In this figure, the blunting regions are found as -3 mV ≤ V_{in} ≤ 2 mV for the positive half-wave output and -2 mV ≤ V_{in} ≤ 1 mV for the negative half-wave output.

```
.MODEL NM NMOS LEVEL=3
+UO=460.5 TOX=1.0E-8 TPG=1 VTO=0.62 JS=1.08E-6
+XJ=0.15U RS=417 RSH=2.73 LD=0.04U VMAX=130E3
+NSUB=1.71E17 PB=0.761 ETA=0.00 THETA=0.129 PHI=0.905
+GAMMA=0.69 KAPPA=0.10 CJ=76.4E-5 MJ=0.357 CJSW=5.68E-10
+MJSW=0.302 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10
+KF=3.07E-28 AF=1 WD=+0.11U DELTA=+0.42 NFS=1.2E11
+DELL=0U LIS=2 ISTMP=10 TT=0.1E-9
.MODEL PM PMOS LEVEL=3
+UO=100 TOX=1.0E-8 TPG=1 VTO=-0.58 JS=0.38E-6
+XJ=0.10U RS=886 RSH=1.81 LD=0.03U VMAX=113E3
+NSUB=2.08E17 PB=0.911 ETA=0.00 THETA=0.120 PHI=0.905
+GAMMA=0.76 KAPPA=2 CJ=85E-5 MJ=0.429 CJSW=4.67E-10
+MJSW=0.631 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10
+KF=1.08E-29 AF=1 WD=+0.14U DELTA=0.81 NFS=0.52E11
+DELL=0U LIS=2 ISTMP=10 TT=0.1E-9
```

Table 6.1 MOS model used in the simulation.

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MI1-MI12, M1-M5, M8	20 μm / 0.6 μm
M6, M9	26.7 μm / 0.6 μm
M7, M10	26.3 μm / 0.6 μm
MA-MF	2 μm / 2 μm
MD1-MD8	2 μm / 0.6 μm
M11-M18	100 μm / 0.6 μm
I_1	20 μA
I_2, I_3	250 μA
I_4	100 μA

Table 6.2 W/L parameters and constant current sources of the proposed rectifier.

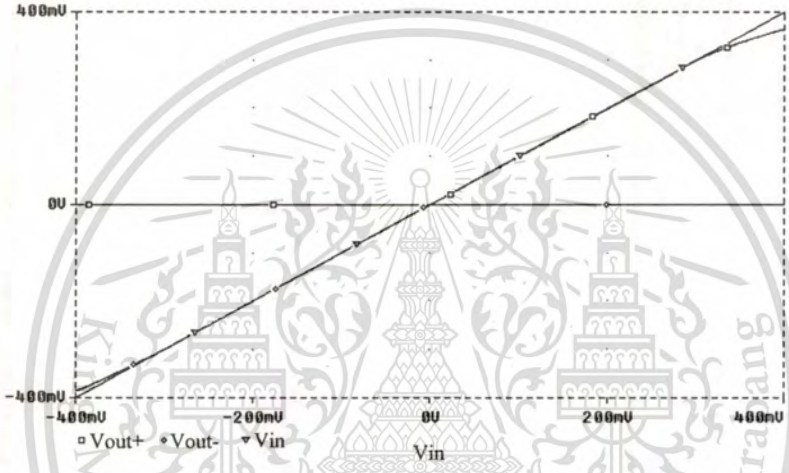

Figure 6.7 DC transfer characteristics of the proposed rectifier.

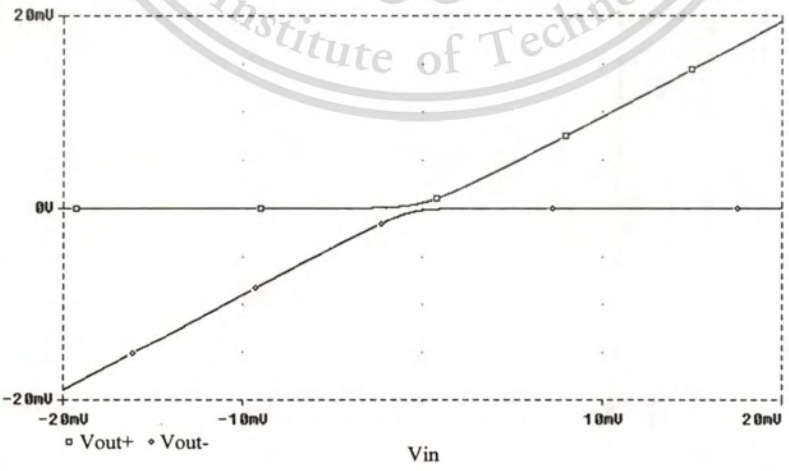

Figure 6.8 Magnified zero crossings of figure 6.7.

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Applying the 100 mV_{peak} sine wave at the input of the proposed rectifier, the input and output signals at frequencies of 1 MHz, 10 MHz, and 100 MHz are shown in figure 6.9, figure 6.10, and figure 6.11, respectively. The amplitude errors between the input and output signals in figure 6.11 result from the decrease of the gain of the proposed rectifier for the operation at high frequency. There are two methods of compensating this problem. The first method is to increase the value of R_2 and R_3 by decreasing the W/L ratios of MC to MF. The second method is to increase the gain of the current mirrors in the proposed rectifier by increasing the W/L ratios of M6, M7, M9, and M10.

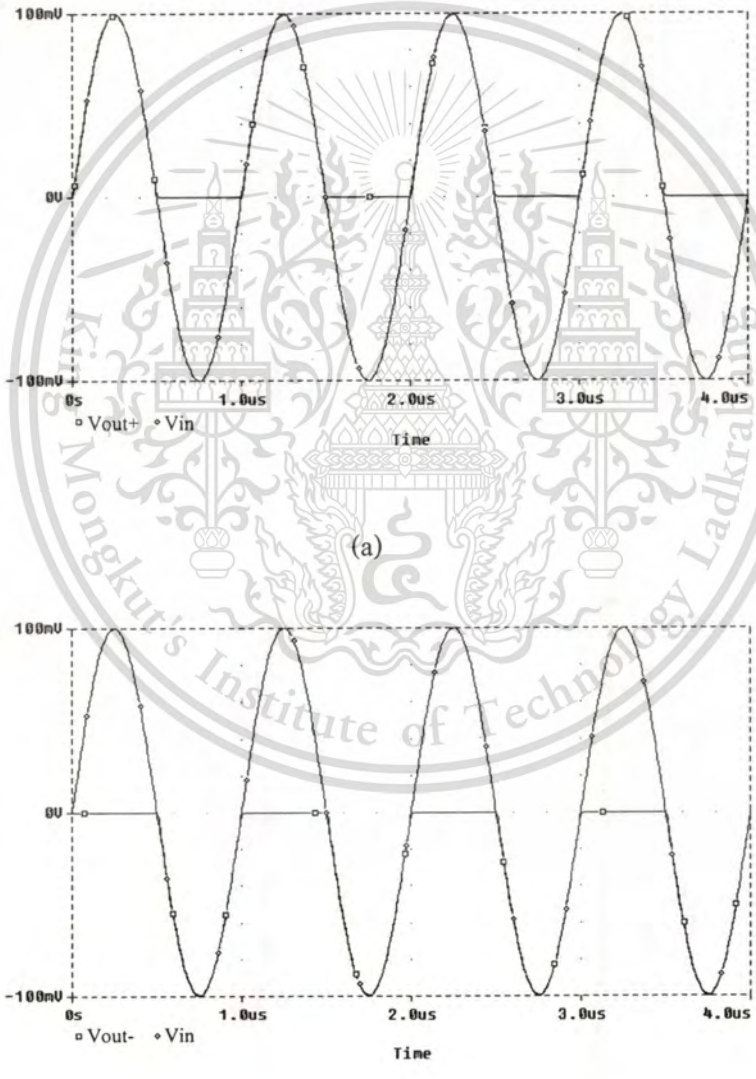

Figure 6.9 Operation of the proposed rectifier at a frequency of 1 MHz: (a) input and positive half-wave output; (b) input and negative half-wave output.

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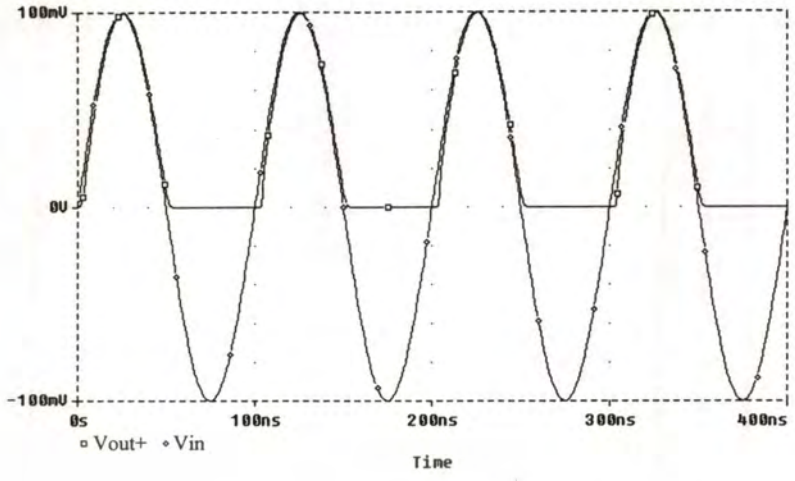
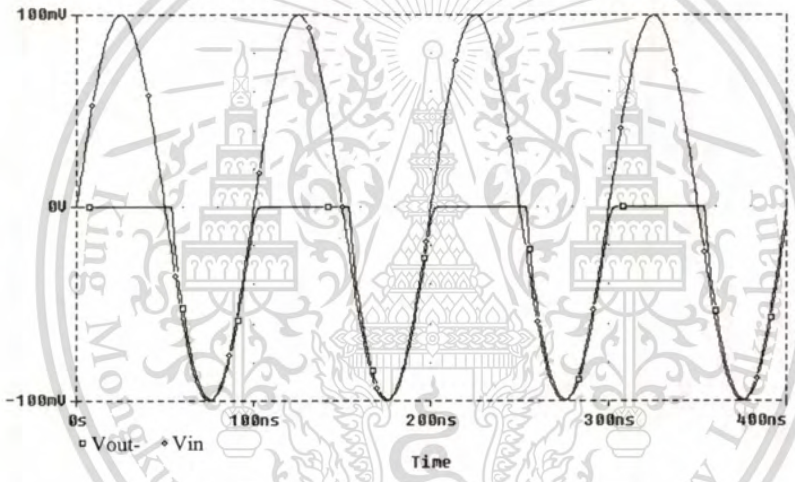


(a)



(b)

Figure 6.10 Operation of the proposed rectifier at a frequency of 10 MHz: (a) input and positive half-wave output; (b) input and negative half-wave output.

We again simulated the proposed rectifier at the frequency of 10 MHz without the diode bias voltage by adjusting $I_2 = I_3 = 0$ μA. The input and output signals in this case are shown in figure 6.12. Note that the output signals in figure 6.12 have errors by the time the voltages change from 0 V, which result from the non-conduction/conduction transition problem of MOS diodes. Comparing the output signals in figure 6.12 with those in figure 6.10, it is clearly seen that by using the MOS diode bias voltages the operating frequency of the proposed rectifier is increased.

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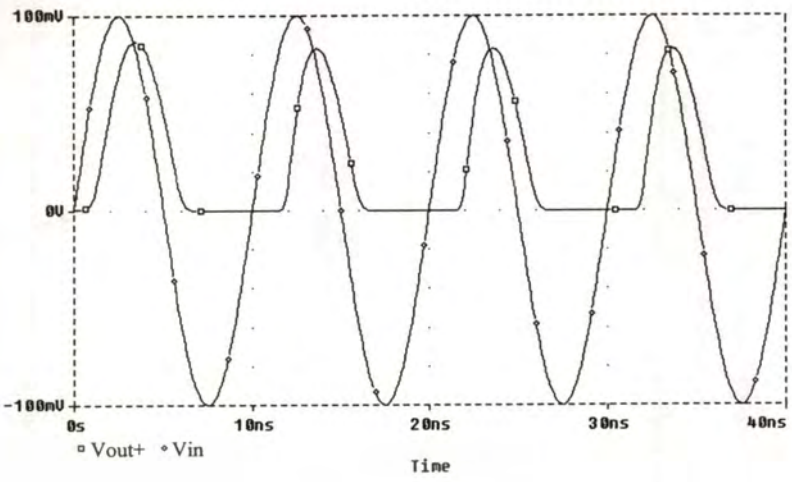
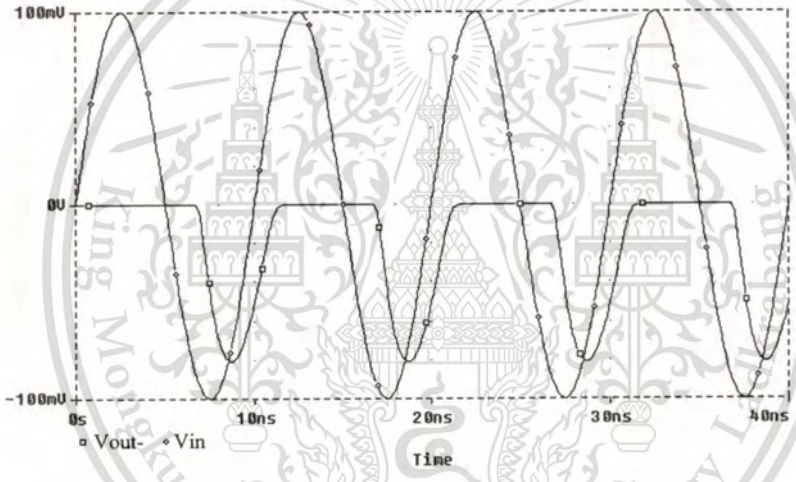


(a)



(b)

Figure 6.11 Operation of the proposed rectifier at a frequency of 100 MHz: (a) input and positive half-wave output; (b) input and negative half-wave output.

At the frequency of 1 MHz, we simulated the temperature performance of the proposed half-wave rectifier by changing temperatures from 0°C to 100°C. The minimum voltages of positive half-wave outputs at all temperatures being 0 V were observed.

Figure 6.13 shows the positive have-wave outputs at temperatures of 27°C, 50°C, and 70°C, choosing these temperatures to compare with the same temperatures results of [7]. At the zero crossings of signals in figure 6.13, it is evident that, for the proposed rectifier, the shifts in voltage

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between each temperature are much lower than those of the temperature independent current conveyor rectifier [7].

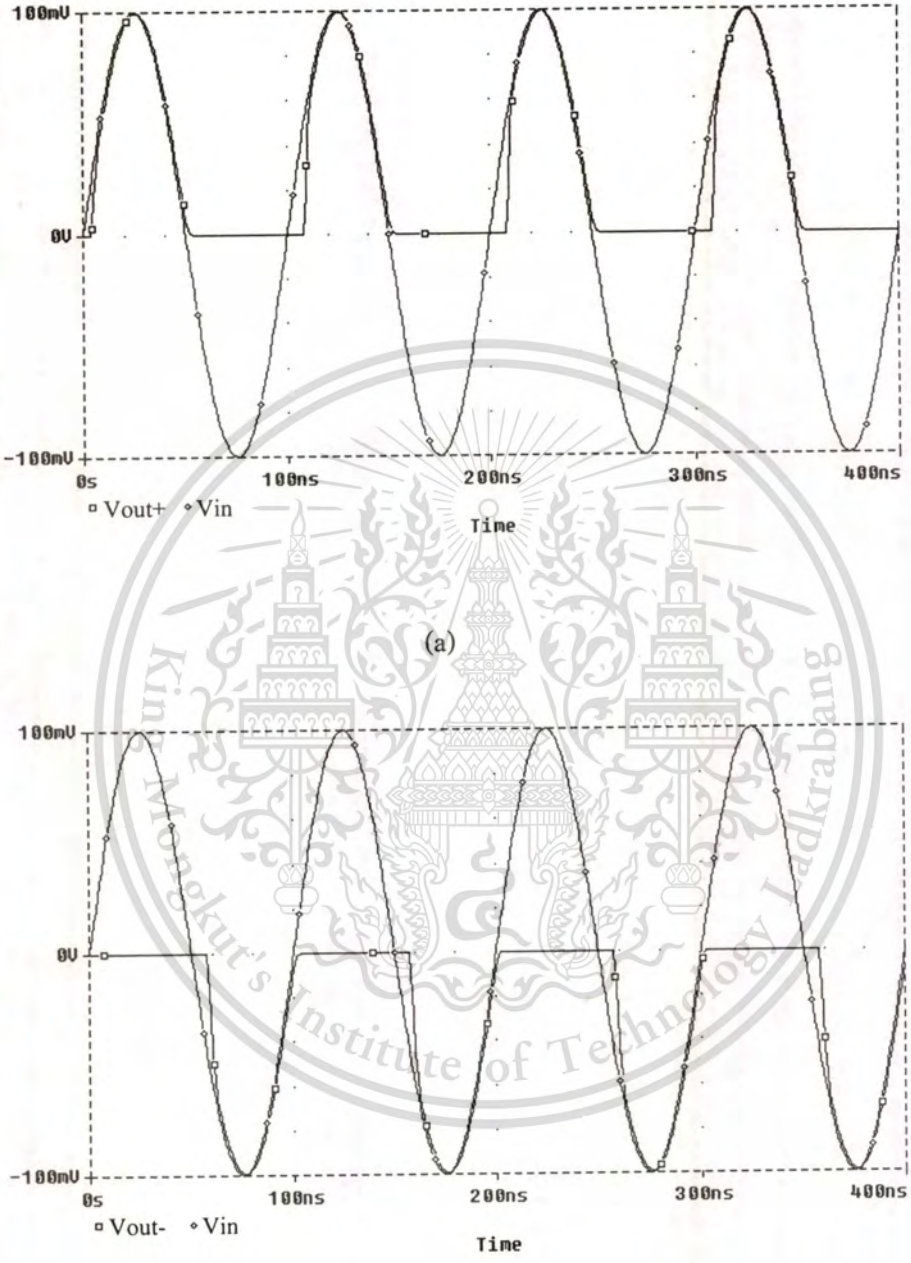

Figure 6.12 Operation of the proposed rectifier at a frequency of 10 MHz without the MOS diode bias voltages: (a) input and positive half-wave output; (b) input and negative half-wave output.

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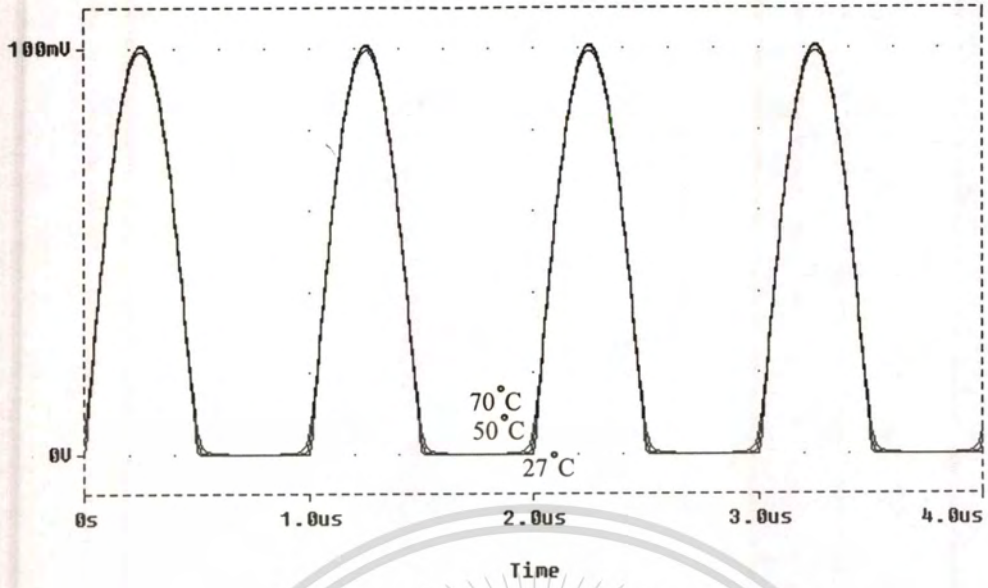

Figure 6.13 Positive half-wave outputs at different temperatures.

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Chapter 7

Conclusions

This thesis presents a bipolar full-wave rectifier using one current conveyor and four current mirrors and a CMOS dual output half-wave rectifier. Both proposed rectifiers are based upon the previous current conveyor rectifiers in [2], [6]-[8]. However, with the difference circuit structures, the proposed rectifiers yield the different performances as shown below.

The features of the proposed full-wave rectifier are as follows: i) it can rectify the small input signal, ii) it has low temperature sensitivity, and iii) it has the suitable structure for IC fabrication. For all solid-state structure, two MOS or bipolar resistors must substitute two resistors in the proposed full-wave rectifier. The proposed full-wave rectifier is suitable for driving the high input impedance load. If the load of the proposed full-wave rectifier has low input impedance, the proposed full-wave rectifier output needs a voltage buffer. Only one disadvantage of the proposed full-wave rectifier is the operation frequency which is lower than those of the previous rectifiers because of the on/off transition problems of diode-transistors (Q17 and Q18) in a current biasing circuit still remained.

The features of the proposed half-wave rectifier are in view of the employed voltage, the power consumption, the number of devices, the operating frequency, the temperature stability, and the simplicity for IC fabrication. For the operating frequency up to 100 MHz, however, this operating frequency obtained from only simulation, when the proposed half-wave rectifier is built as IC, this operating frequency will be lessened by the effect of parasitic capacitance in IC. The proposed half-wave rectifier uses the MOS-resistors, R_2 and R_3, to convert the output currents to the output voltages, which it is suitable for high impedance load. In fact, the MOS-resistors of the input V-I converter and output I-V one are based on the complementary source followers, loaded by parallel n-MOS and p-MOS transistors working in the triode region. The resultant resistors R_1, R_2, and R_3, are not quite linear, but the cascade of input V-I converter and output I-V one causes partial compensation of the non-linearity of these resistors. If the half-wave rectifier is loaded by low impedance load, the load may be connected directly instead of resistor R_2 or R_3 (it needs linear resistor R_1).

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The above compared performance is conclude to be simple for reader in table 7.1

Performances	Compared results	
	Proposed full-wave rectifier	Proposed half-wave rectifier
Simplicity for IC fabrication	Better (use all grounded resistors)	Better (use all MOS structure)
Minimum voltage rectification	Better (94 μV)	Better (0 V)
Temperature stability	Better (shift in minimum output voltage being 76 μV between 27 ° C and 70 ° C)	Better (shift in minimum output voltage being 0 V between 27 ° C and 70 ° C)
Operation frequency	Worse (1 kHz)	Better (100 MHz)

Table 7.1 Performances of the proposed rectifiers compared with the rectifiers in [2], [6]-[8].

For the future work, the proposed full-wave rectifier should be developed by designing a new biasing method that has no remaining on/off transition problem.

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References

[1] Lidgey F. J., Hayatleh K. and Toumazou C. "New current-mode precision rectifiers." Proc. IEEE ISCAS (Chicago), 1993. pp. 1322-1325.

[2] Toumazou C., Lidgey F. J. and Chattong S. "High frequency current conveyor precision full-wave rectifier." Electronics letters, vol. 30, 1994. pp. 745-746.

[3] Surakampontorn W., Jutaviriya S. and Apajinda T. "Dual translinear sinusoidal frequency doubler and full-wave rectifier." International Journal of Electronics, vol. 65, 1988. pp. 1203-1208.

[4] Ramirez-Angulo J. "High frequency low voltage CMOS diode." Electronics letters, vol. 28, 1992. pp. 298-300.

[5] Surakampontorn W., Riewruja V. "Integrable CMOS sinusoidal frequency doubler and full-wave rectifier." International Journal of Electronics, vol. 73, 1992. pp. 627-632.

[6] LTP Electronics Ltd. **CCII01 current-conveyor data sheet.** Oxford. 1993.

[7] Hayatleh K., Porta S. and Lidgey F. J. "Temperature independent current conveyor precision rectifier." Electronics letters, vol. 30, 1994. pp. 2091-2093.

[8] Khan A. A., Abou El-Ela M. and Al-Turaigi M. A. "Current-mode precision rectification." International Journal of Electronics, vol. 79, 1995. pp. 853-859.

[9] David J., Ken M. **Analog integrated circuit design.** USA : John Wiley & Sons, Inc. 1997.

[10] Sze S. M. **Physics of semiconductor devices.** New York : Wiley Interscience, Inc. 1981.

[11] Gray P. R., Meyer R. G. **Analysis and design of analog integrated circuits.** New York : John Wiley & Sons, Inc. 1993.

[12] Smith K. C., Sedra A. S. "The current conveyor—a new circuit building block." Proc. IEEE, vol. 56, 1968. pp. 1368-1369.

[13] Sedra A. S., Smith K. C. "A second generation current conveyor and its applications." IEEE Trans. Circuit Theory, vol. CT-17, 1970. pp. 132-134.

[14] Sedra A. S. "A new approach to active network synthesis." Ph.D. Thesis, University of Toronto, 1969.

[15] Wilson B. "Constant bandwidth voltage amplification using current conveyors." International Journal of Electronics, vol. 65, 1988. pp. 983-988.

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[16] Huijsing J. H., De Korte J. "Monolithic nullor – a universal active network element." IEEE Jounal of Solid State Circuits, vol. SC-12, 1977. pp. 59-64.

[17] Wilson B. "Universal conveyor instrumentation amplifier." Electronics letters, vol. 25, 1989. pp. 470-471.

[18] Toumazou C., Lidgey F. J. "Novel current mode instrumentation amplifier." Electronics letters, vol. 25, 1989. pp. 228-230.

[19] Bruton L. T. **RC active circuits.** New Jersey : Prentice-Hall, Inc. 1980.

[20] Svoboda J. A., McGory L. and Webb S. "Applications of a commercially available current conveyor." International Journal of Electronics, vol. 70, 1991. pp. 159-164.

[21] Fabre A., Saaid O., Wiest F. and Boucheron C. "High frequency applications based on a new current controlled conveyor." IEEE Trans. Circuits and Systems I, vol. 43, 1996. pp. 82-91.

[22] Toumazou C., Lidgey F. J. and Haigh D. G. **Analogue IC design: the current mode approach.** London : Peter Peregrinus Limited. 1990.

[23] Battersby N. C., Toumazou C. "Class AB switched-current memory for analogue sampled-data systems." Electronics letters, vol. 27, 1991. pp. 873-875.

[24] Wang Z. "2-MOSFET transistor with extremely low distortion for output reaching supply voltages." Electronics letters, vol. 26, 1990. pp. 951-952.

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Publications of the thesis

[1] K. Dejhan, A. Monpapassorn, F. Cheevasuvit, S. Wisetphanichkij and C. Soonyeekan, "A design of class AB current mirror," Proc. 1999 International Conference on Robotics, Vision and Parallel Processing for Automation, vol. 1, pp. 302-306, Ipoh, Malaysia.

[2] K. Dejhan, A. Monpapassorn, F. Cheevasuvit, C. Tanwongvarl, P. Moungnoul and C. Soonyeekan, "26 MHz CMOS RC oscillator circuit," Proc. 1999 International Conference on Robotics, Vision and Parallel Processing for Automation, vol. 2, pp. 667-672, Ipoh, Malaysia.

[3] A. Monpapassorn, K. Dejhan and F. Cheevasuvit, "A full-wave rectifier using a current conveyor and current mirrors," International Journal of Electronics, vol. 88, no.7, pp. 751-758, 2001.

[4] A. Monpapassorn, K. Dejhan and F. Cheevasuvit, "CMOS dual output current mode half-wave rectifier," International Journal of Electronics, vol. 88, no.10, pp. 1073-1084, 2001.

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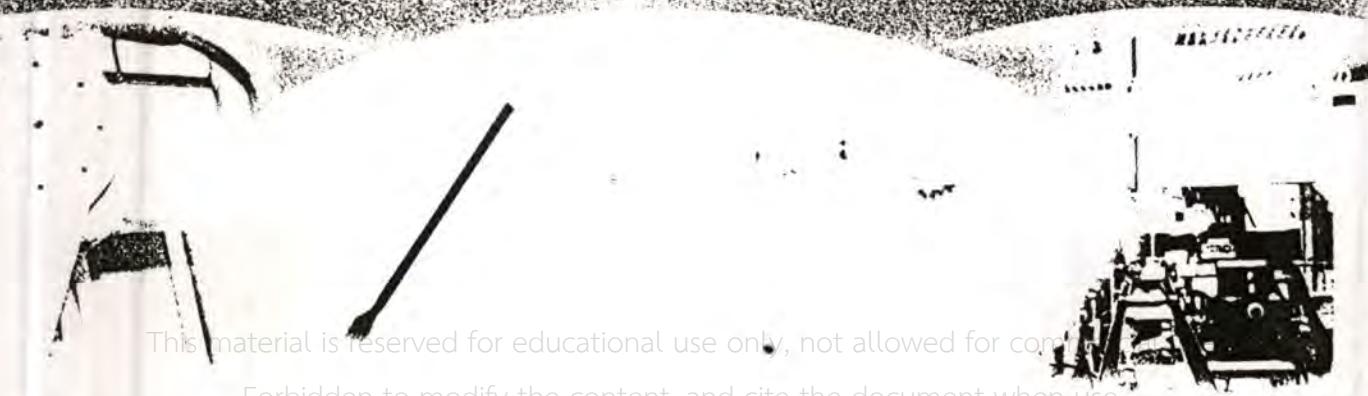

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A DESIGN OF CLASS AB CURRENT MIRROR

Kobchai Dejhan, Adisak Monpapassorn, Fusak Cheevasuvit, Sompong Wisetphanichkij

Faculty of Engineering and Research Center for Communications and Information Technology

King Mongkut's Institute of Technology Ladkrabang

Bangkok 10520, Thailand

Email : kobchai@telelan.telecom.eng.kmitl.ac.th

Tel : 66-2-3269967, 66-2-3269081

Fax : 66-2-3269086

Chatcharin Soonyeekan

Faculty of Engineering, Kasem Bundit University

Pattanakarn Road, Bangkok 10250, Thailand

Abstract

This paper presents a new circuit of class AB current mirror. The circuit has no needs to use the constant current source, it reduces the power dissipation and offset error from mismatching of devices. As there has not the input, it has not the flowing of current in the circuit; except only the leakage current. All results of the proposed circuit have been carried out by simulating based on PSpice. The results show that the input current is linearly with the output current.

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Introduction

The current mirror circuit are widely used to design the current mode analog integrated circuit and mixed-mode analog integrated circuit for signal processing such as filters, amplifiers, oscillators, data-converters and arithmetic unit. In general, the operation of the current mirror circuits are divided into class A and class AB, the difference between class A and class AB is one input direction for class A and two-input directions for class AB. The class AB uses both N and P channel MOS transistors to reduce the mismatch error of the devices [1].

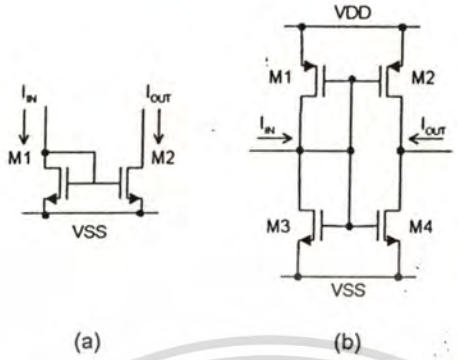

Fig. 1. (a) Class A, and (b) class AB.

Fig. 1(a) shows a class A current mirror circuit that uses all biased N-channel MOS transistors operating in saturation region. The disadvantage of this circuit is the use of input current direction. Fig.1 (b) shows a class AB current mirror without constant current source [2], the constant current has to be infected in the circuit for all-time according to the active load.

Theory

This paper proposes a design of low power dissipation class AB current mirror circuit as shown in Fig.2. Fig.2 (a) is a noninverting current mirror circuit. The proposed noninverting current mirror has no need for voltage supply. Both circuits in Fig.2(a) and Fig.2(b) have no current flow in the circuits as no input current feeding to the circuit, except the small leakage current of devices in the circuit [3]. Both proposed circuits are suitable for the lower power dissipation class AB current mirrors.

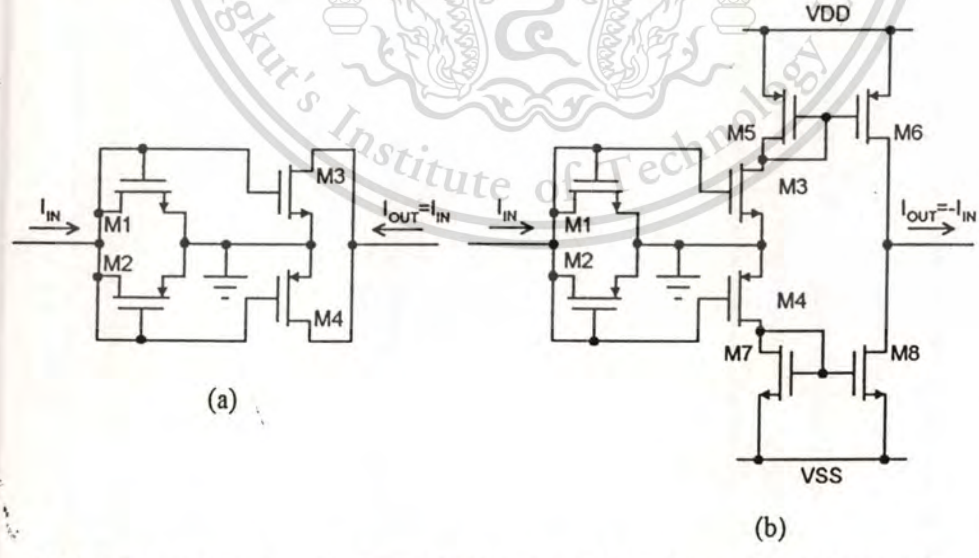

Fig.2 Two proposed class AB current mirror circuits (a) noninverting, (b) inverting.

Results

Both proposed circuits have been tested by simulating based on PSpice program. The transistor models of 2 μm CMOS technology of European Silicon Structure with worst case at 85° C are used. The supply voltages for V_{DD} and V_{SS} are +5 and -5 V, respectively. The W/L ratio for all CMOS transistors in Fig.2 (a) and 2(b) are equal to 200 μm /10 μm. The relation of the output current and input current for the proposed

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circuit in Fig.2(a) has been carried out as shown in Fig.3. It is obviously that the relation is linear. The relation is not linear until the input current is about 950 μA . The current tracking can be used within 1 mA.

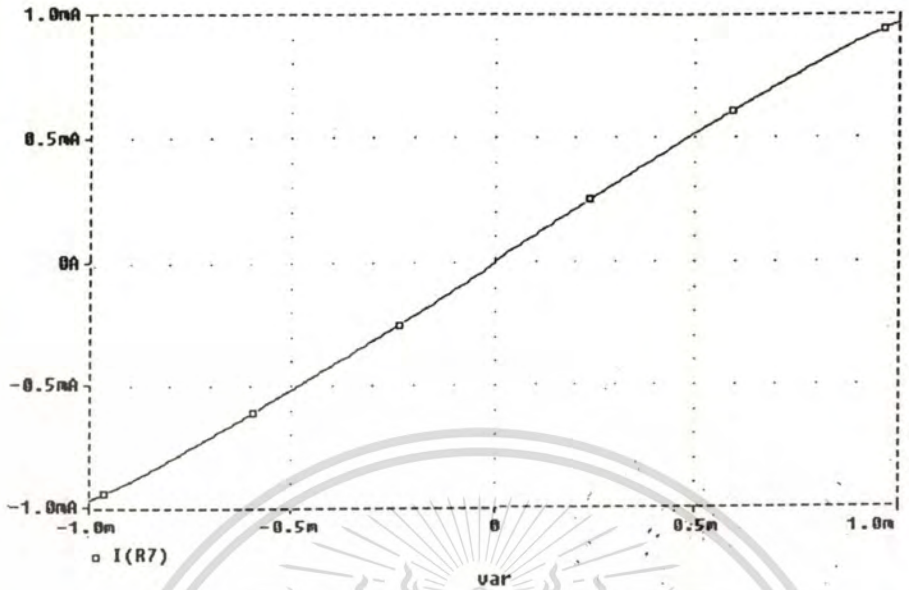

Fig. 3 Relation of input current and output current of proposed noninverting circuit as shown in Fig.2(a)

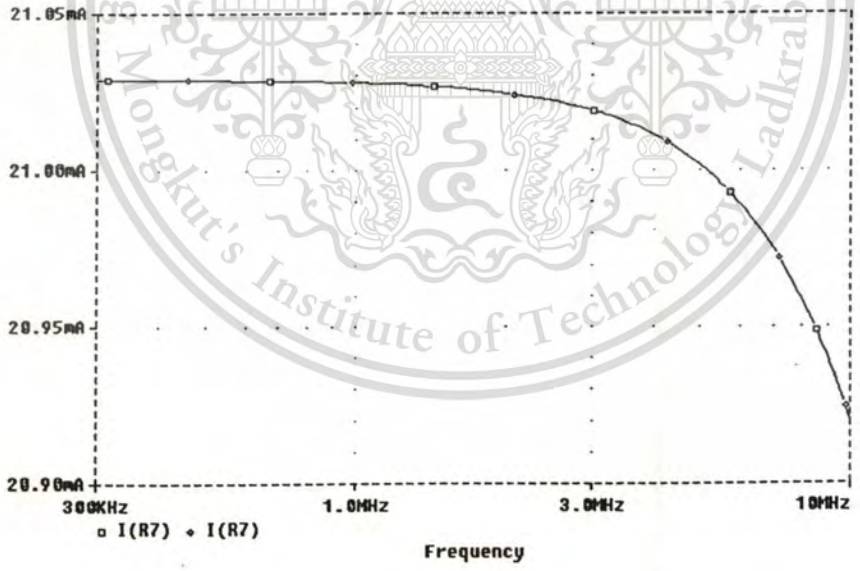

Fig. 4 Frequency response of noninverting circuit as shown in Fig.2(a)

The frequency response of proposed circuit in Fig.2 (a) has been carried out in order to investigate the operating frequency range. This proposed circuit can be used until 5 MHz.

Similarly, the relation of the output current and input current for the proposed circuit in Fig. 2(b) has also been carried out as shown in Fig. 5, which are linear until the higher current approximately 700 μA.

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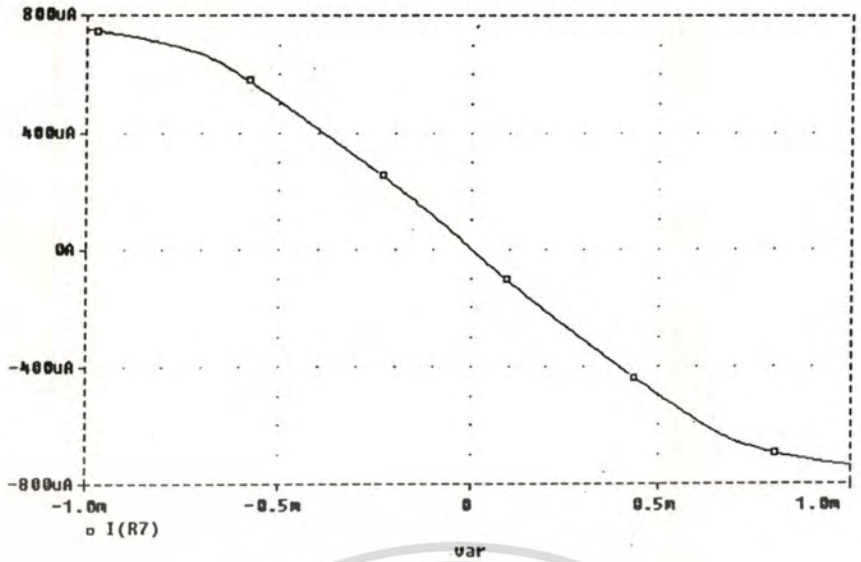

Fig.5 Relation of input current and output current of proposed inverting circuit as shown in Fig. 2 (b)

The frequency response of proposed circuit in Fig.2(b) has been shown in Fig.6 frequency range is about 5 MHz.

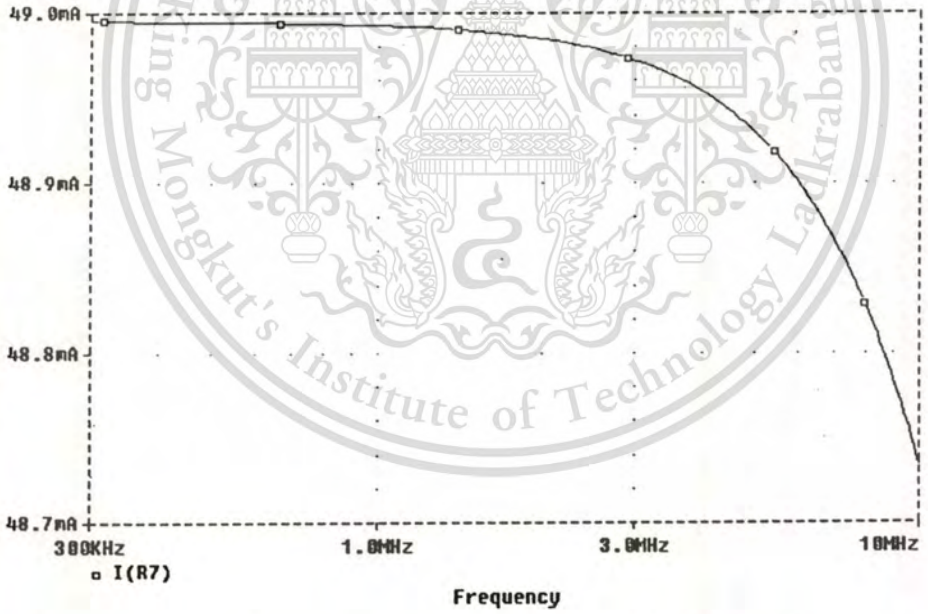

Fig.6 Frequency response of inverting circuit as shown in Fig. 2(b)

Conclusion

This paper proposes a low power class AB current mirrors for both non inverting and inverting current mirrors. The proposed circuits consume low power when compared with the previous paper [2]. The mismatch problem occurs and there is some error for the proposed inverting current mirror. The error can be neglected by using cascode circuit, but the number of transistors will be increased.

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References

[1] S. Kawahito and Y. Tadokoro, "CMOS Class-AB Current Mirror for Precision Current-Mode Analog-Signal-Processing Elements," IEEE Trans. Circuits Syst. II, vol. 43, pp.843-845, Dec. 1996.

[2] E.I. El-Masry and J. W. Gates, "A Novel Continuous-Time Current-Mode Differentiator and its Applications," IEEE Trans. Circuits Syst. II, vol. 43, pp.56-59, Jan. 1996.

[3] N.H.E Weste and K. Eshragian, Principles of CMOS VLSI Design - A System Perspective, 1st Edn., pp. 140, Reading, Massachuset : Addison - Wesley, 1985.

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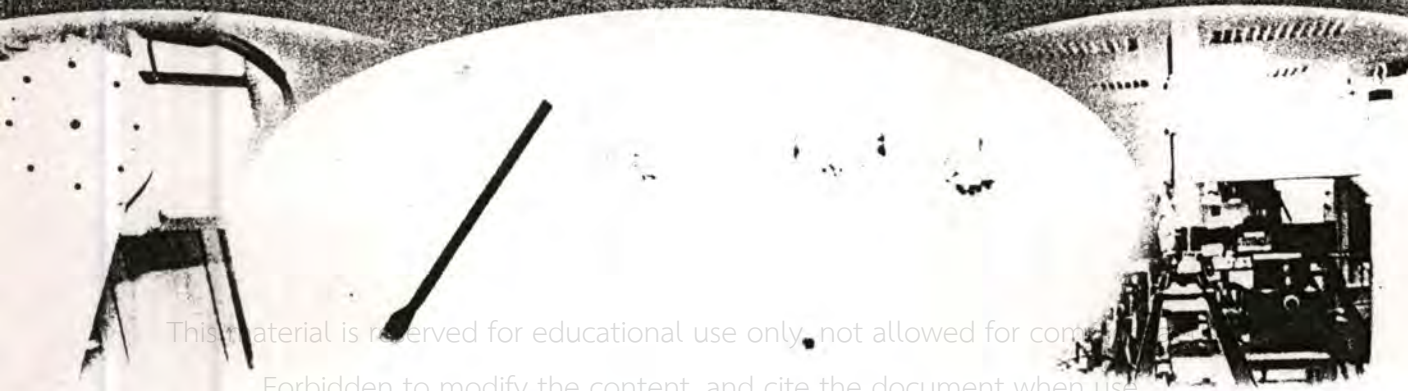

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26 MHz CMOS RC OSCILLATOR CIRCUIT

Kobchai Dejhan, Adisak Monpapassorn, Fusak Cheevasuvit, Chayaphon Tanwongvarl,

Phichet Moungnoul

Faculty of Engineering and Research Center for Communications and Information Technology

King Mongkut's Institute of Technology Ladkrabang

Bangkok 10520, Thailand

Email : kobchai@telelan.telecom.eng.kmitl.ac.th

Tel : 66-2-3269967, 66-2-3269081

Fax : 66-2-3269086

Chatcharin Soonyeekan

Faculty of Engineering, Kasem Bundit University

Pattanakarn Road, Bangkok 10250, Thailand

Abstract

This paper presents a circuit design of 26 MHz CMOS RC oscillator. The circuit technique is based on CMOS differential amplifier, four CMOS transistors, a constant current source and lead-lag network by using resistors and capacitors. The output of this proposed oscillator circuit is sinusoidal wave with low distortion. The oscillating frequency can be adjusted by varying the resistor or capacitor. This proposed circuit uses 0.6 μm technology. The results of this proposed circuit are simulated by using PSpice program.

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Introduction

The oscillators are widely used in electronics and communications. there are many types of oscillator. The paper concerns about RC oscillator. The previous paper[1] proposed to use voltage feedback operational amplifier (VFOA). the other previous papers [2-3] proposed to use current feedback operational amplifier (CFOA) and another previous paper [4] proposed to use the current mirrors to design RC oscillator. The disadvantages of VFOA, CFOA and current mirrors are a number of devices, high power consumption and low output oscillating frequency. This paper presents a design technique to overcome these disadvantages with small number of devices by using four MOS transistor, a constant current source, 5V DC supply with low power consumption. The oscillating frequency depends on the value of R and C.

Theory

The oscillator uses the principle of positive feedback without shifting the phase. The basic concept is shown in Fig.1. The feedback voltage is amplified, the sinusoidal output oscillating voltage will be obtained.

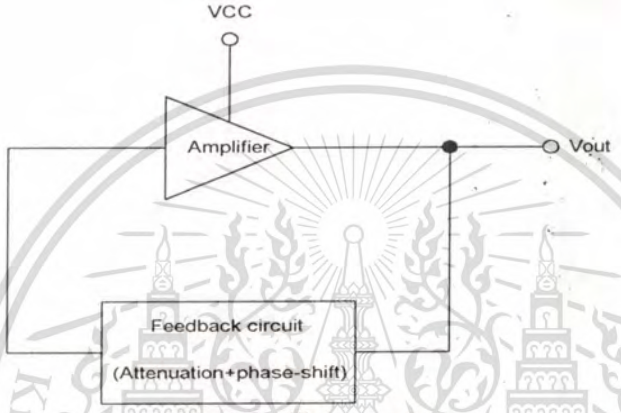

Fig. 1 Oscillator structure

The phenomenon of oscillation occurs. two conditions are required for a sustained state of oscillation: the phase shift around the feedback loop has to be 0° and the voltage gain of the closed loop is equal to 1 or more than 1.

The proposed circuit is shown in Fig.2. the lead-lag network consists of R_1 , R_2 , C_1 and C_2 . R_1 and C_1 are connected to form the lag portion of the network. Similarly for R_2 and C_2 are connected to form the lead portion. The circuit operation can be described as follows. In the low frequency range, the lead network dominates due to the high reactance of C_2 .

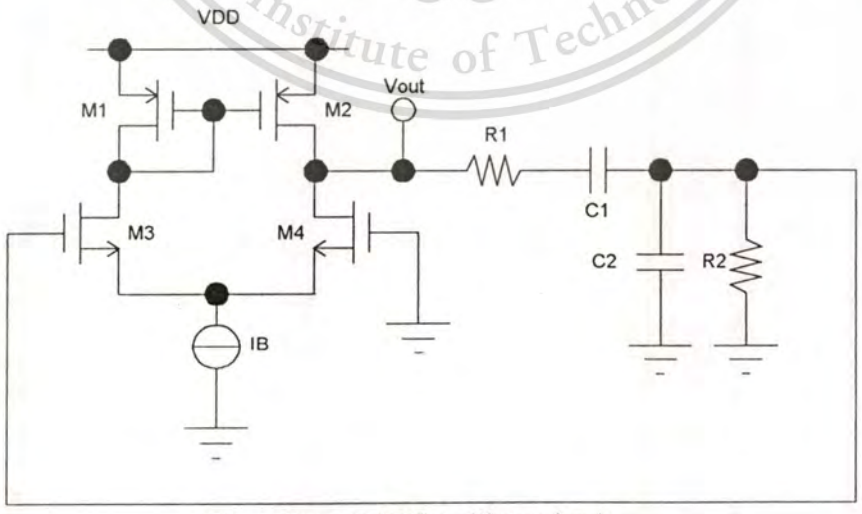

Fig. 2. Proposed RC oscillator circuit.

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As the frequency increases, the reactance of C_2 , X_{c2} decreases, then the output voltage will be increased. In some specific frequency range, the response of lag network will dominate and the X_{c1} is decreased, the output voltage is decreased. The voltage transfer function of lead-lag network is

$$\frac{V_{out}}{V_{oin}} = \frac{RX_C}{3RX_C + j\left(R^2 - X_C^2\right)} \tag{1}$$

whereas $R_1 = R_2 = R$ and $C_1 = C_2 = C$.

Consider at resonant frequency (f_r). $R = X_c$ and then.

$$\frac{V_{out}}{V_{in}} = \frac{1}{3} \tag{2}$$

and

$$f_r = \frac{1}{2\pi RC} \tag{3}$$

f_r is inverse proportional to the RC product. The amplifier circuit consists of transistors M1 to M4 with a constant current source (I_B). The amplification rate of the circuit is

$$A_v = g_{m1}\left(r_{ds2} // r_{ds4}\right) \tag{4}$$

g_{m1} : transconductance of MOS transistor: M1.

r_{ds2} and r_{ds4} : drain-to-source equivalent resistance of MOS transistor M2 and M4, respectively.

$$g_m = \mu_o C_{ox}\left(\frac{W}{L}\right)\left(V_{GS} - V_T\right)$$

μ_o = carrier mobility.
C_{ox} = oxide capacitance.
W = width of channel.
L = length of channel.
V_{GS} = gate-to-source voltage.
V_T = threshold voltage.

From the equation (2). $V_{in} = 3\ V_{out}$ or the amplification rate of the amplifier circuit must be equal to three times or more than 3. The oscillator circuit can oscillate, the ratio can be adjusted by using the ratio of W/L of MOS transistor M1.

Results

The proposed RC oscillator circuit has been tested by simulation. All simulation results have been carried out by using PSpice program. The proposed circuit uses 5V DC supply with 100 μA constant current source. The ratio of W/L for all MOS transistors are 15 μm / 0.6 μm by using 0.6 μm CMOS technology process. Let $R_1 = R_2 = 10k\Omega$, C1 = C2 = 100 pF. The start up oscillation is shown in Fig. 3. The oscillating signal of the proposed oscillator is shown in Fig.4.

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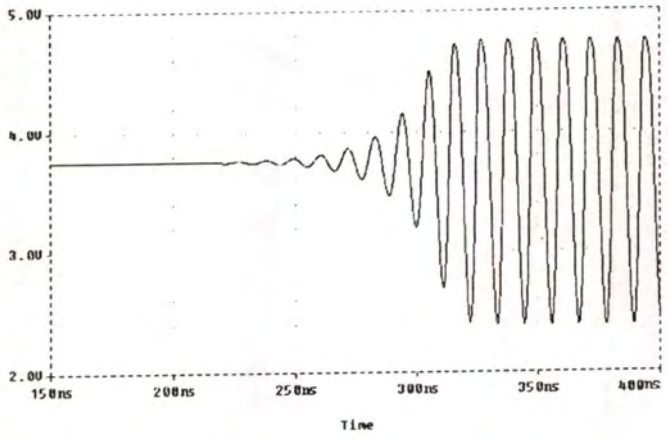

Fig.3. Start-up oscillating of oscillator.

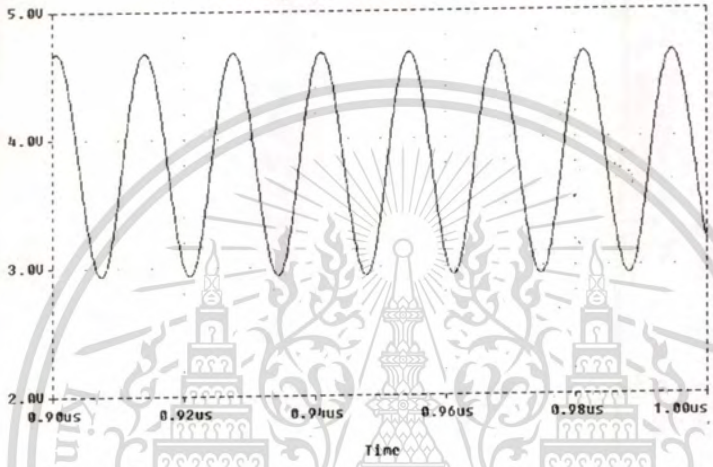

Fig.4. Oscillating waveform.

The spectrum of the oscillating signal is shown in Fig.5. Fig. 6, 7, 8 show the spectra of the oscillating signals for $C_1 = C_2 = 10$ pF, 1 pF and 0.1 pF, respectively.

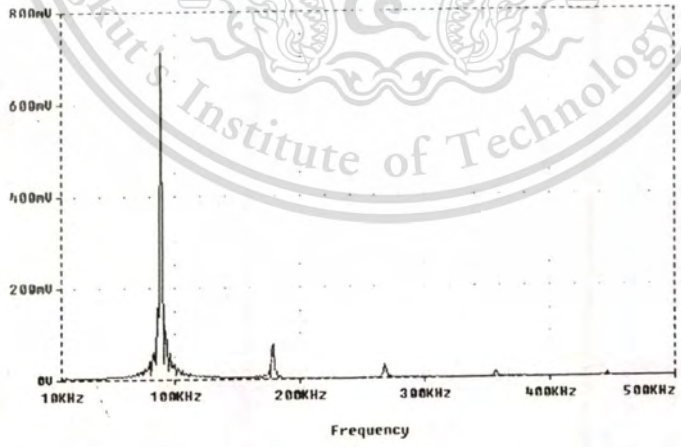

Fig. 5. Spectrum of oscillating signal for $C_1 = C_2 = 100$ pF.

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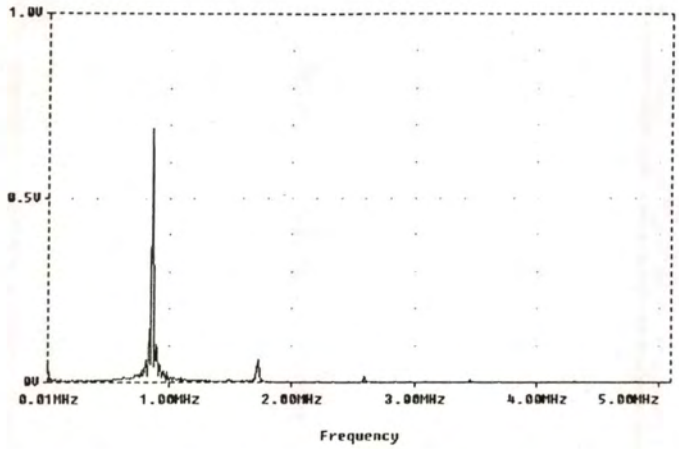

Fig. 6. Spectrum of oscillating signal for $C_1 = C_2 = 10$ pF.

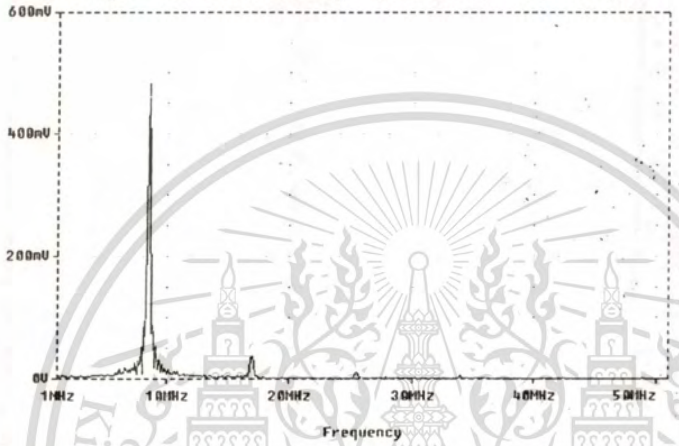

Fig. 7. Spectrum of oscillating signal for $C_1 = C_2 = 1$ pF.

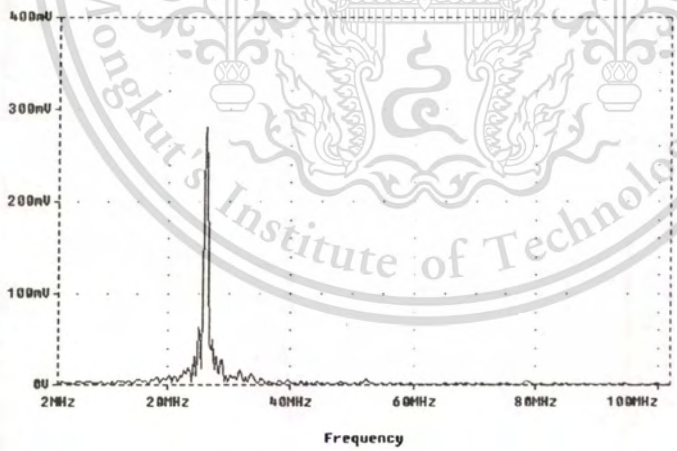

Fig. 8. Spectrum of oscillating signal for $C_1 = C_2 = 0.1$ pF.

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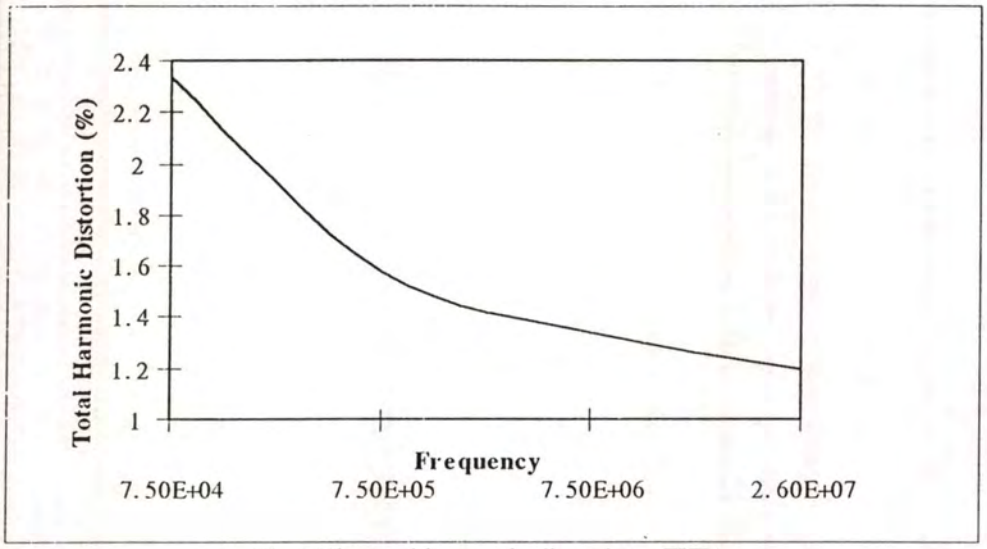

Fig.9 The total harmonic distortion (THD)

Conclusion

A simple CMOS RC oscillator circuit design is presented, it generates oscillation frequency from 10 kHz to 26 MHz by varying the values of R and C. The number of devices in the circuit is quite small, low power consumption at 5V DC supply, generate high oscillation frequency.

References

[1] S.J.G. Gift, "Multiphase Sinusoidal Oscillator System using Operational Amplifiers," Int. J. Electronics, vol. 83, pp.61-67, 1997.

[2] S.- I. Liu, " Single-Resistance-Controlled Sinusoidal Oscillator using Two FTFNs," Electron. Letts., vol. 33, pp.1185-1186, July 1997.

[3] M.T. Abuelma'atti and S.M. Al-shahrani, "New CFOA-based Sinusoidal Oscillator," Int. J. Electronics, vol. 82, pp.27-32, 1997.

[4] S. Pookaiyaudom, K. Samootrut and W. Kurutach, "Current mirrors RC oscillators," Int. J. Electronics, vol. 62, pp.803-303, 1987.

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A full-wave rectifier using a current conveyor and current mirrors

ADISAK MONPAPASSORN†‡, KOBCHAI DEJHAN† and FUSAK CHEEVASUVIT†

The realization of a full-wave rectifier using a current conveyor and current mirrors is presented. The proposed rectifier is composed of a voltage-to-current converter, a current mode full-wave rectifier, and a current-to-voltage converter. A voltage input signal is changed into a current signal by the voltage-to-current converter. The current mode full-wave rectifier rectifies this current signal resulting in the current full-wave output signal that is converted into a voltage full-wave output signal by one grounded-resistor. The theory of operation is described. The simulation and experiment results are used to verify the theoretical prediction. Simulated results show that the proposed rectifier yields the minimum voltage rectification to 94 μV. Experimental results demonstrate the performance of the proposed rectifier for 50 mV_{peak} signal rectification.

1. Introduction

Rectifiers are extensively used in wattmeters, AC voltmeters, RF demodulators, piecewise linear function generators, and various nonlinear analogue signal-processing circuits. The operation of diode-only rectifiers is limited by the threshold voltages of diodes, approximately 0.3 V for germanium diodes and 0.7 V for silicon diodes. Therefore diode-only rectifiers are used in only those applications in which the precision in the range of threshold voltage is insignificant, such as RF demodulators and DC voltage supply rectifiers. For applications requiring high accuracy, the diode rectifiers cannot be used: MOS or bipolar integrated circuit rectifier are used instead.

One advantage of the integrated circuit (IC) rectifiers designed using the simple devices such as opamps, current conveyors, transistors, diodes and resistors as components, is that they can be built in many countries. The classical problem with conventional precision rectifiers based on diodes and opamps is that during the non-conduction/conduction transition of the diodes the opamps must recover with a finite small-signal dV/dt resulting in significant distortion during the zero crossing of the input signal. The use of the high slew-rate opamps does not solve this fundamental drawback because it is a small-signal transient problem (Lidgey *et al.* 1993). Conventional rectifiers are thus limited to a frequency performance well below the gain-bandwidth product or f_T of the amplifier (Toumazou *et al.* 1994). This limitation is improved by designing the rectifier by the use of current mode techniques (Lidgey *et al.* 1993, LTP Electronics Ltd 1993, Hayatleh *et al.* 1994, Toumazou *et al.* 1994, Khan *et al.* 1995). Recently, the current mode full-wave rectifiers using current

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† Faculty of Engineering and Research Center for Communications and Information Technology (ReCCIT), King Mongkut's Institute of Technology Ladkrabang, Ladkrabang, Bangkok 10520, Thailand.

‡ Corresponding author. e-mail: aone_mon@hotmail.com

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conveyors as the voltage-to-current converter have received much attention. For example, LTP Electronics Ltd (1993) and Khan *et al.* (1995) proposed the same current conveyor full-wave rectifiers as shown in figure 1(*a*). This full-wave rectifier is developed to reduce the distortion due to the small-signal dV/dt limitation in the next time by Toumazou *et al.* (1994) with the addition of a DC voltage source as shown in figure 1(*b*). Hayatleh *et al.* (1994) further developed this full-wave rectifier to reduce the effect of temperature on the zero crossing performance by using a current source and a resistor in place of the voltage source, as shown in figure 1(*c*).

In this paper, the authors present the full-wave rectifier using the easy seen devices: the current conveyor, transistors, and resistors. The proposed rectifier yields the following advantages.

(i) The proposed rectifier using the number of solid-state devices is roughly equal to each of the rectifiers from LTP Electronics Ltd (1993), Hayatleh *et al.* (1994), Toumazou *et al.* (1994), and Khan *et al.* (1995). However, the proposed rectifier uses two grounded resistors whereas the previous rectifiers use one ungrounded resistor and one grounded resistor; therefore the proposed rectifier is more suitable for IC fabrication than some of the previous rectifiers.

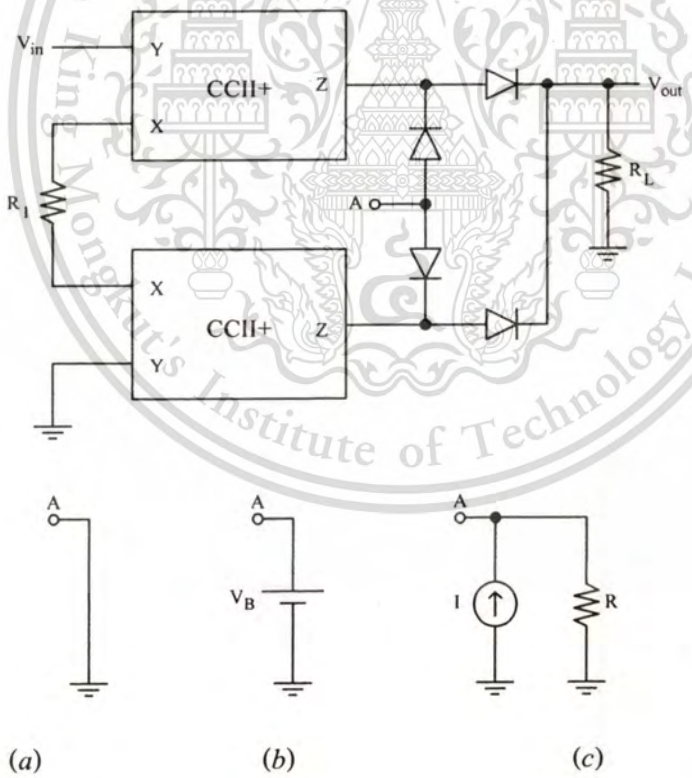

Figure 1. Current conveyor based precision full-wave rectifiers: (*a*) proposed by LTP Electronics Ltd (1993) and Khan *et al.* (1995), (*b*) voltage biasing technique proposed by Toumazou *et al.* (1994), and (*c*) current biasing technique proposed by Hayatleh *et al.* (1994).

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(ii) The proposed rectifier can rectify the minimum voltage of 94 μV.

(iii) The proposed rectifier provides good temperature stability.

2. Proposed full-wave rectifier

The second generation current conveyor CCII+ (Sedra and Smith 1970) shown in figure 2 is used as one component of the voltage-to-current converter in the proposed rectifier. The relations between the currents and voltages at the nodes (X, Y and Z) of this current conveyor are given by

$$i_y = 0 \qquad v_x = v_y \qquad i_z = i_x \tag{1}$$

Figure 3 shows the proposed full-wave rectifier. From (1), the output current of CCII+ (i_z) can be written as

$$i_z = \frac{V_{in}}{R_I} \tag{2}$$

This current is fed into the input of the current mode full-wave rectifier. In the proposed rectifier, the current mode full-wave rectifier consists of four Wilson bipolar current mirrors (CM1 (Q1 to Q4), CM2 (Q5 to Q8), CM3 (Q9 to Q12) and CM4 (Q13 to Q16)); two bipolar transistors (Q17 and Q18); and three constant current sources (I_1, I_2 and I_3). Q17 and Q18 operate as diodes to protect the short circuit between I_1 and I_2. The constant current sources, $I_1 = I_2 = I$, mean that the transistors in CM1 to CM4 are turned-on all the time, reducing the problem during the non-conduction/conduction transition of these transistors whereby both currents create the offset current ($2I$) through R_O. To eliminate this offset current at R_O, we exploit $I_3 = 2I$ at the output of the proposed rectifier.

The operation of the current mode full-wave rectifier is as follows. When $i_z > 0$, it is fed through Q17 and then is mirrored by CM1 to the collector of Q4 as $-i_z$, this $-i_z$ is again mirrored by CM3 to the collector of Q12 as $+i_z$. In addition, when $i_z < 0$, it is fed through Q18 and then is mirrored by CM2 to the collector of Q8 as $-i_z$, this $-i_z$ is second mirrored by CM4 to the collector of Q16 as $+i_z$, and this $+i_z$ is third mirrored by CM3 to the collector of Q12 as $-i_z$. From the operation of the current mode full-wave rectifier explained, the relations between the input current (i_z) and the output current at the collector of Q12 ($I_{C(Q12)}$) can be expressed as

$$\left.\begin{aligned} i_z > 0; \quad I_{C(Q12)} &= +i_z + 2I \\ i_z < 0; \quad I_{C(Q12)} &= -i_z + 2I \end{aligned}\right\} \tag{3}$$

The offset, $2I$, in (3) is compensated using I_3. Thus we can write the relations between i_z and the output current (I_{R_O}) as

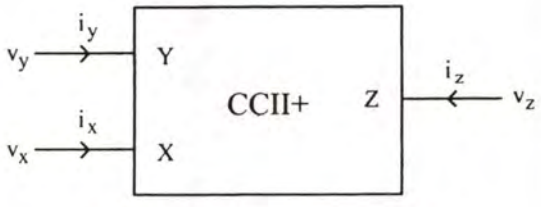

Figure 2. CCII+ current conveyor.

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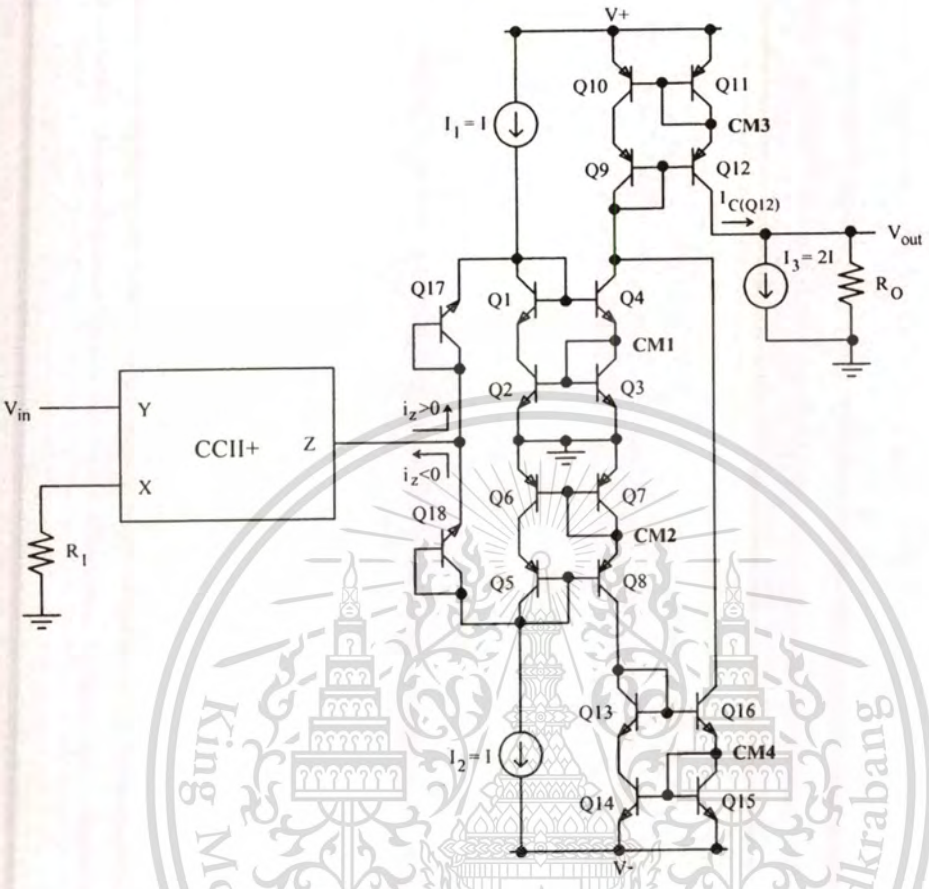

Figure 3. Proposed full-wave rectifier.

$$\left.\begin{aligned} i_z > 0; \quad I_{R_O} &= +i_z \\ i_z < 0; \quad I_{R_O} &= -i_z \end{aligned}\right\} \tag{4}$$

Using (2) and $R_O = R_I$, we get the relations between the input and the output voltages of the proposed rectifier as

$$\left.\begin{aligned} V_{in} > 0; \quad V_{out} &= +V_{in} \\ V_{in} < 0; \quad V_{out} &= -V_{in} \end{aligned}\right\} \tag{5}$$

This means that the proposed rectifier operates as the full-wave rectifier.

3. Simulation and experiment results

To verify the theoretical design, the proposed full-wave rectifier was simulated using the PSPICE program. We use the current conveyor CCII+ in the current feedback opamp AD844 (Svoboda *et al.* 1991) and we use the NPN and PNP transistors 2N3904 and 2N3906 respectively. All these device models are obtained from the PSPICE library. The supply voltage used is ±10 V. The constant current sources employed are $I_1 = I_2 = 100\,\mu A$ and $I_3 = 200\,\mu A$; in practice these current

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sources can be built using only one current source that supplies the current through the unity and double gain current mirrors. The $R_I = R_O = 100\,\Omega$ were chosen.

Figure 4 shows the sine wave input signals ($100\,mV_{peak}$) and output signals of the proposed full-wave rectifier at the frequencies of 1 kHz, 10 kHz and 100 kHz. Because the output current signal of CCII+ in the proposed rectifier is fed through more devices than those in the rectifiers of Toumazou *et al.* (1994) and Hayatleh *et*

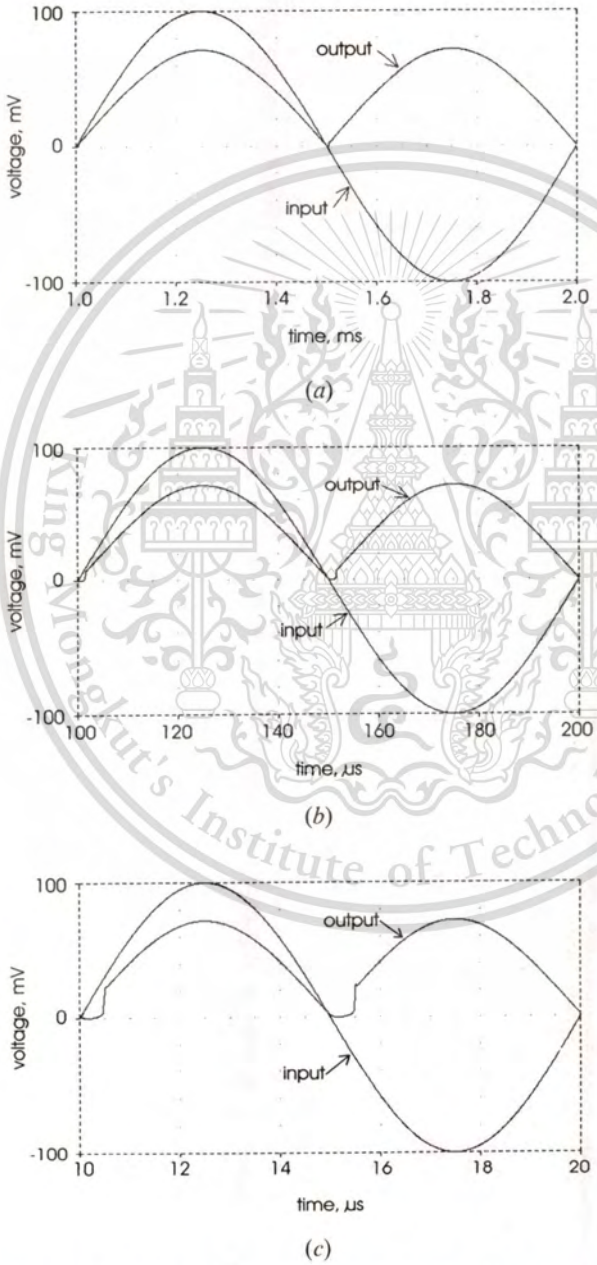

Figure 4. Input sine wave ($100\,mV_{peak}$) and output signals of the proposed rectifier from simulation at the frequencies of: (*a*) 1 kHz, (*b*) 10 kHz and (*c*) 100 kHz.

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al. (1994), the operation frequency of the proposed rectifier is lower than those of the rectifiers of these previous workers. Note that from the output signals in figure 4, the limit of the operation frequency of the proposed rectifier depends on the error at zero-crossing owing to the on/off transition problem of transistors Q17 and Q18. This error affects the small signals more than the large signals, so the operation frequency for large signals will higher than that for small signals.

At the 100 kHz output signal in figure 4(*c*), the minimum rectified output voltage of 94 μV was observed. Whereas the minimum rectified output voltages for the rectifiers of Toumazou *et al.* (1994) and Hayatleh *et al.* (1994) are 16 mV and 8 mV, respectively, as reported by Hayatleh *et al.* (1994). Additionally, at this 100 kHz frequency, the magnified zero crossing ranges of the output signals at temperatures 27°C, 50°C and 70°C are shown in figure 5. They show that the difference of the lowest output voltages between 27°C and 50°C is 40 μV and that between 50°C and 70°C is 36 μV. Whereas Hayatleh *et al.* (1994) reported that the difference of the lowest output voltages of the rectifier (Toumazou *et al.* 1994) between 27°C and 50°C is 32 mV and that between the 50°C and 70°C is 38 mV. Further Hayatleh *et al.* (1994) reported that the difference of the lowest output voltages of their rectifier between 27°C and 50°C is 8 mV and that between 50°C and 70°C is 12 mV. All the above in this section shows the better performance in minimum voltage rectification and temperature stability of the proposed rectifier.

The amplitude error of the output voltage signals in figure 4 results from three factors. The first factor is the non-ideal of the current conveyor, i.e. the input resistance at node X of the current conveyor in AD844 is 50 Ω (Svoboda *et al.* 1991), ideally, it must be 0 Ω. The error for this factor can be corrected by increasing the value of R_O. The second factor is the error of the Wilson bipolar current mirrors in the proposed rectifier, i.e. the input and output currents of Wilson bipolar current mirror (Gray and Meyer 1993) is given by

$$I_{out} = I_{in} - (2/\beta^2) \tag{6}$$

where β is the current gain of all the transistors in Wilson bipolar current mirrors. When $V_{in} > 0$, the output current of CCII+ is $i_z > 0$ that is mirrored by CM1 and CM3. Furthermore, when $V_{in} < 0$, the output current of CCII+ is $i_z < 0$ that is mirrored by CM2, CM4, and CM3. Hence, we can write the relations between the input and output voltages with the error from Wilson bipolar current mirrors as

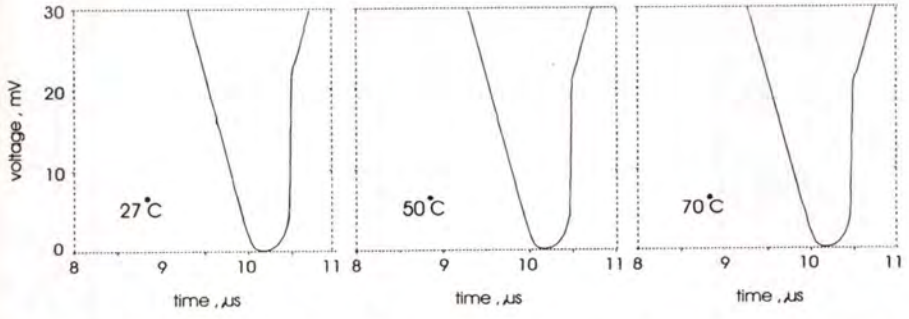

Figure 5. Efficiency of the proposed rectifier in zero crossing range at some temperatures.

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$$\left.\begin{aligned} V_{in} > 0; \quad V_{out} &= +V_{in} - (4/\beta^2)R_o \\ V_{in} < 0; \quad V_{out} &= -V_{in} - (6/\beta^2)R_o \end{aligned}\right\} \tag{7}$$

The third factor is the on/off transition problem of Q17 and Q18 as already mentioned.

We use the low value of R_1 to obtain the high value of i_z in order to reduce the error at zero crossing of the output signal from the conduction/non-conduction transition problem of Q17 and Q18. The operation voltage range of the proposed rectifier thus depends upon the operation range of the CCII+ in the voltage-to-current converter that is limited by the maximum current $i_{z(max)}$ of CCII+. This

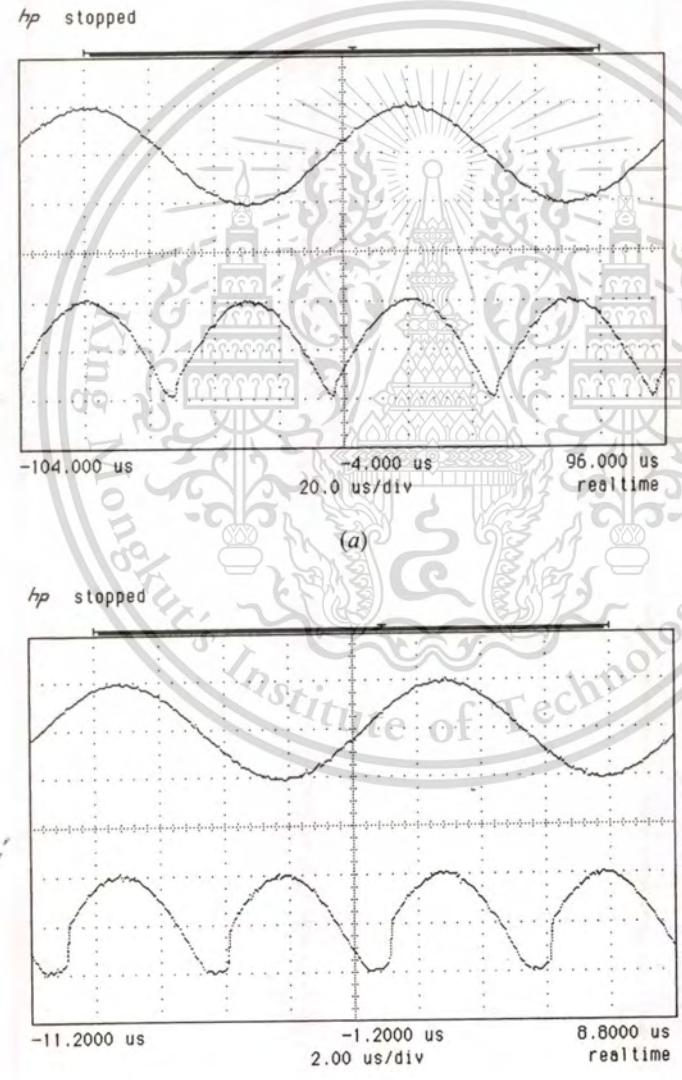

Figure 6. Input sine wave (50 mV_{peak}) and output waveforms of the proposed rectifier from experiment at the frequencies of (*a*) 10 kHz and (*b*) 100 kHz.

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$i_{z(\max)}$ depends on the supply voltage, that is if we use the high supply voltage, the operation range of CCII + will widen, resulting in the wide operation voltage range of the proposed rectifier; however, the maximum supply voltage of CCII + limits the increment of the supply voltage.

The simulated rectifier was also constructed. Figure 6(*a*) shows the upper input waveform ($50\,\text{mV}\,\text{div}^{-1}$) and the lower output waveform ($20\,\text{mV}\,\text{div}^{-1}$) of the proposed rectifier at the frequency of 10 kHz, and figure 6(*b*) shows the waveforms at the frequency of 100 kHz. These experimental results correspond to simulation results.

4. Conclusion

The full-wave rectifier using a current conveyor and current mirrors has been described. The features of the proposed rectifier are as follows: (i) it can rectify the small input signal, (ii) it has low temperature sensitivity and (iii) it has the suitable structure for IC fabrication. For all solid-state structure, two MOS or bipolar resistors must substitute two resistors in the proposed rectifier. The proposed rectifier is suitable for driving the high input impedance load. If the load of the proposed rectifier has low input impedance, the proposed rectifier output needs a voltage buffer.

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Our thanks go to K. Kumwachara for his CCIIs and suggestions. S. Maitreechit is also thanked for his assistance in the experiment. In addition, the authors would like to thank the editor and reviewers for all their suggestions.

References

GRAY, P. R. and MEYER, R. G., 1993, *Analysis and Design of Analog Integrated Circuits* (New York: John Wiley & Sons).

HAYATLEH, K., PORTA, S., and LIDGEY, F. J., 1994, Temperature independent current conveyor precision rectifier. *Electronics Letters*, **30**, 2091–2093.

KHAN, A. A., ABOU EL-ELA, M., and AL-TURAIGI, M. A., 1995, Current-mode precision rectification. *International Journal of Electronics*, **79**, 853–859.

LIDGEY, F. J., HAYATLEH, K., and TOUMAZOU, C., 1993, New current-mode precision rectifiers. *Proceeding of the IEEE International Symposium on Circuits and Systems (Chicago)*, 1322–1325.

LTP ELECTRONICS LTD., 1993, *CCII01 current-conveyor data sheet* (Oxford).

SEDRA, A., and SMITH, K. C., 1970, A second generation current conveyor and its applications. *IEEE Transactions on Circuit Theory*, **17**, 132–134.

SVOBODA, J. A., MCGORY,. L., and WEBB, S., 1991, Applications of a commercially available current conveyor. *International Journal of Electronics*, **70**, 159–164.

TOUMAZOU, C., LIDGEY, F. J., and CHATTONG, S., 1994, High frequency current conveyor precision full-wave rectifier. *Electronics Letters*, **30**, 745–746.

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CMOS dual output current mode half-wave rectifier

ADISAK MONPAPASSORN*†, KOBCHAI DEJHAN† and FUSAK CHEEVASUVIT†

A CMOS dual output current mode half-wave rectifier is presented. The proposed rectifier is composed of three main components: a dual output V–I converter, two half-wave current rectifiers and two I–V converters. A voltage input signal is changed into two current signals by the V–I converter. The current rectifiers rectify these current signals, resulting in positive and negative half-wave current signals that are converted to positive and negative half-wave voltage signals by the I–V converters. The theory of operation is described, and the simulated results obtained from the PSPICE program are used to verify the theoretical prediction. Simulated rectifier performance with a 0.5 μm MOSFET model using ±1.2 V supply voltage demonstrates good rectifier integrity at operating frequencies up to 100 MHz.

1. Introduction

Rectifiers are used extensively in wattmeters, AC voltmeters, RF demodulators, piecewise linear function generators, and various nonlinear analogue signal-processing circuits. The operation of the simple diode rectifier is limited by the threshold voltage of diodes, approximately 0.3 V for the germanium diode and 0.7 V for the silicon diode; thus the simple diode rectifier is used only in some applications in which the precision in the range of threshold voltage is insignificant, such as radio frequency demodulators and DC voltage supply rectifiers. However, for applications requiring accuracy in the range of threshold voltage, the simple diode rectifier cannot be used. This can be overcome by using integrated circuit rectifiers instead.

The classical problem with conventional precision rectifiers based on diodes and opamps is that during the non-conduction/conduction transition of the diodes the opamps must recover with a finite small-signal, dV/dt, resulting in significant distortion during the zero crossing of the input signal. The use of high slew-rate opamps does not solve this fundamental drawback because it is a small-signal transient problem (Lidgey *et al.* 1993). Conventional rectifiers are thus limited to a frequency performance well below the gain–bandwidth product or f_T of the amplifier (Toumazou *et al.* 1994). This limitation is improved by designing the rectifiers using the current mode techniques (Ramirez-Angulo 1992, Surakampontorn and Riewruja 1992, Lidgey *et al.* 1993, LTP Electronics Ltd. 1993, Toumazou *et al.* 1994, Hayatleh *et al.* 1994, Khan *et al.* 1995). Some of these current mode rectifiers use the CMOS class AB amplifiers (Ramirez-Angulo 1992, Surakampontorn and Riewruja 1992). Although they have the advantage in view of the use of few devices,

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* Corresponding author. e-mail: aone_mon@hotmail.com

† Faculty of Engineering and Research Center for Communications and Information Technology (ReCCIT), King Mongkut's Institute of Technology Ladkrabang, Ladkrabang, Bangkok 10520, Thailand.

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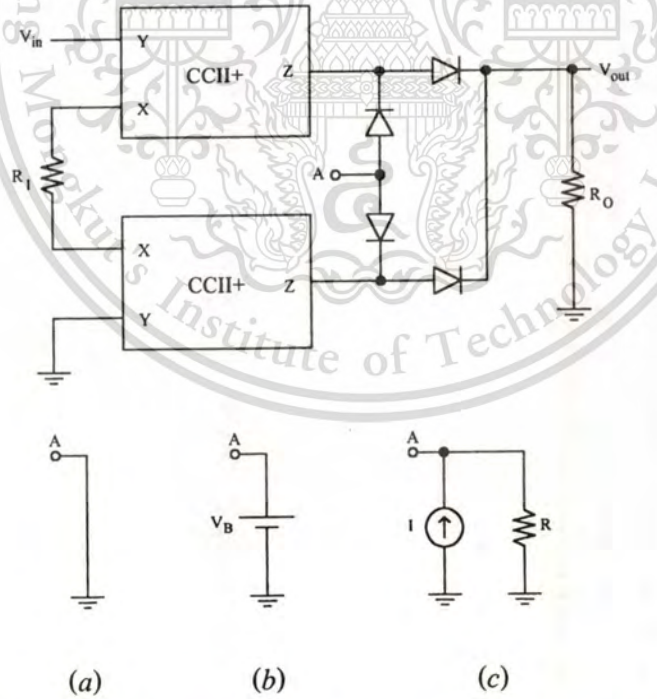
they also have the drawback that, while $-4I_B \leq I_{in} \leq 4I_B$, where I_{in} is the input current and I_B are two constant current sources used in the amplifier, the output current has an error with the square function of the input current. The use of current mode rectifiers employing current conveyors and diodes can avoid this square function problem.

Recently, rectifiers employing current conveyors and diodes have received wide attention. For example, LTP Electronics Ltd (1993) and Khan *et al.* (1995) proposed the same current conveyor full-wave rectifiers as shown in figure 1(*a*). This full-wave rectifier was developed to reduce the distortion due to the small-signal dV/dt limitation by Toumazou *et al.* (1994) with the addition of a DC voltage source as shown in figure 1(*b*). Hayatleh *et al.* (1994) developed this full-wave rectifier again to reduce the effect of temperature on the zero crossing performance by using a current source and a resistor in place of the voltage source, as shown in figure 1(*c*).

In this paper, we present a CMOS dual output current mode half-wave rectifier using similar techniques to the above current conveyor rectifiers. Namely, it uses the *V–I* converter to change the input voltage into currents, the diodes to rectify the currents, and the *I–V* converters to change the rectified currents into the output voltages. Moreover, it uses the diode bias voltages to clad the output voltage excursions during the zero crossings for operation at high frequency. However, the proposed rectifier has features superior to the above current conveyor rectifiers, as follows:



(*a*) (*b*) (*c*)

Figure 1. Current conveyor based precision full-wave rectifiers: (*a*) proposed by LTP Electronics Ltd (1993) and Khan *et al.* (1995); (*b*) voltage biasing technique proposed by Toumazou *et al.* (1994); (*c*) current biasing technique proposed by Hayatleh *et al.* (1994).

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(1) Each of the above current conveyor rectifiers uses a resistor and two current conveyors as devices in its *V–I* converter while the proposed rectifier uses the dual output all MOS *V–I* converter that is specially designed. Hence the number of devices used in the proposed rectifier is much fewer. Further, the proposed rectifier is more suitable for integrated circuit fabrication than the above current conveyor rectifiers (i.e. it needs no passive resistor).

(2) Each of the above current conveyor rectifiers employs a high supply voltage (needed by current conveyors) and has a low operating frequency (dependent on the operating frequencies of current conveyors). With the advantage of the specially designed *V–I* converter, the proposed rectifier employs only a ± 1.2 V supply voltage and provides an operating frequency up to 100 MHz (simulated result with 0.5 μm MOSFET model obtained through MIETEC).

(3) Each of the above current conveyor rectifiers uses the stable diode bias voltage to bias diodes in the rectifier in order to make the diodes turn-on all the time. This voltage is equal to approximately $2V_H$, where V_H is the threshold voltage of the diodes. Furthermore, this voltage must be the minimum voltage to obtain the minimum offset voltage at output. Unfortunately, V_H depends upon the temperature: when the temperature increases, it causes an offset voltage at the output; inversely, when the temperature decreases, it causes diodes not to turn-on all the time. The proposed rectifier uses the diode bias voltage at the series two diodes, $2V_H$. This voltage depends on the temperature of diodes being the same as the voltage $2V_H$ of the series two diodes in the bridge. Thus the proposed rectifier has much better temperature stability than either of above current conveyor rectifiers.

2. Proposed rectifier

The proposed rectifier is shown in figure 2(*a*). It consists of three main components: the dual output *V–I* converter, the current rectifiers, and the *I–V* converters. The *V–I* converter is composed of I_1, MI1 to MI5, M1 to M10, and MA and MB. The operation of the *V–I* converter is as follows. The constant current I_1 is mirrored by MI1, MI4, MI2 and MI3 to the drain of M1 and is mirrored by MI1 and MI5 to the drain of M3. Using MI1 to MI5 have the same characteristics; the drain currents of M1 and M3 are equal. Choosing M1 to M4, which are perfectly matched, the input voltage V_{in} is thus followed to node A (Bruun 1993). The voltage at node A creates the current I_{in} flowing through a MOS resistor R_1 (Wang 1990), the resistance of which is given by

$$R = \frac{1}{2KV_{DT}} \tag{1}$$

where MA and MB have the same characteristics; $K = \mu C_{ox} W/L$, μ is the carrier mobility, C_{ox} is the gate capacitance per unit area, W and L are the channel width and length respectively; $V_{DT} = V_{DD} - V_T = -(V_{SS} + V_T)$, $V_{DD} = -V_{SS}$, V_T is the threshold voltage. Consequently, I_{in} is given by

$$I_{in} = V_{in}(2KV_{DT}) \tag{2}$$

The current I_{in} is mirrored by M5, M6, M8 and M9 to node B and is mirrored by M5, M7, M8 and M10 to node C. The current rectifiers are the positive and negative

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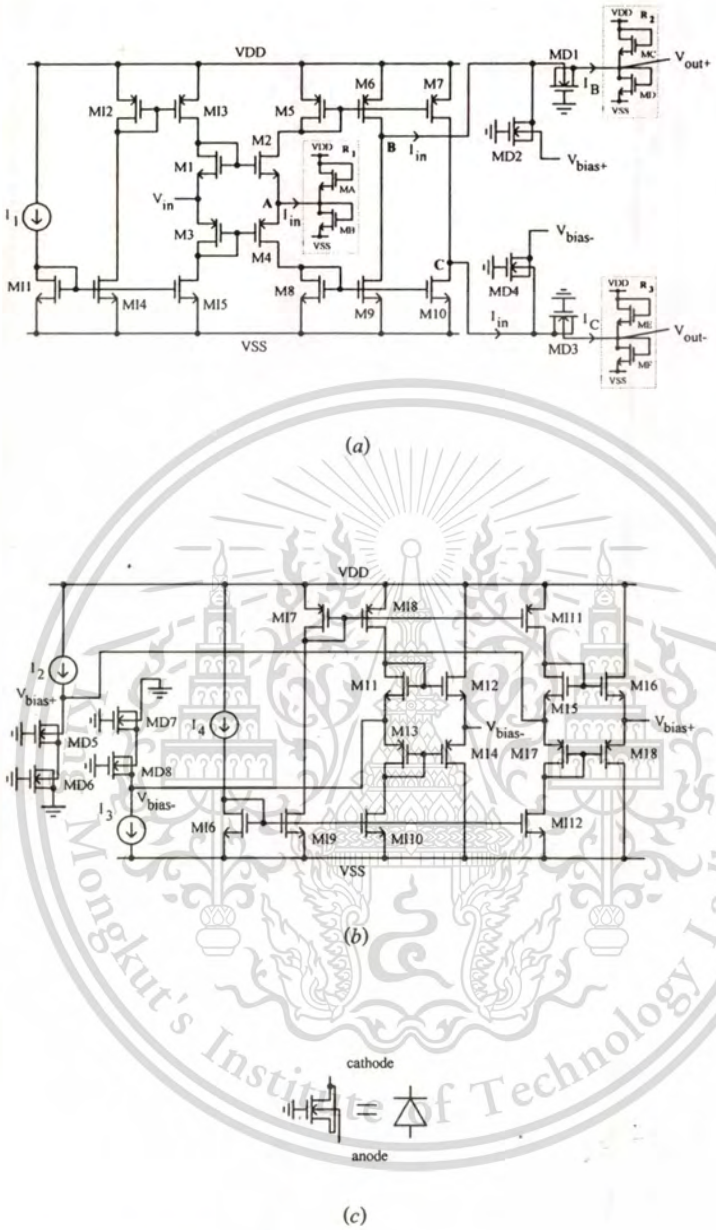

Figure 2. Proposed dual output current mode half-wave rectifier: (*a*) rectifier; (*b*) bias voltage source; (*c*) operation of MOSFET as diode.

half-wave rectifiers. The MOS diodes, MD1 and MD2 (see figure 2(*c*)), form as the positive half-wave rectifier. Its operation is as follows. When I_{in} is positive, MD1 is turned on and MD2 turned off; for this reason, I_{in} is equal to I_B. Conversely, when I_{in} is negative, MD1 is turned off and MD2 turned on, resulting in I_{in} being bypassed into V_{bias+}; as a result, there is no I_B. The current I_B is converted to the voltage V_{out+} by the MOS resistor R_2 (MC and MD). Setting $R_1 = R_2 = R_3$ with the use of the closely matched MA to MF, we can write the relation between V_{in} and V_{out+} as

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$$\left.\begin{aligned} V_{in} > 0;\ V_{out+} &= V_{in} \\ V_{in} < 0;\ V_{out+} &= 0 \end{aligned}\right\} \tag{3}$$

The negative half-wave rectifier consists of MD3 and MD4, which operate as follows. When I_{in} is positive, MD3 is turned off and MD4 turned on, causing I_{in} to be bypassed into V_{bias-}; thus there is no I_C. Inversely, when I_{in} is negative, MD3 is turned on and MD4 turned off, therefore, I_C is equal to I_{in}. This I_C is converted to the voltage V_{out-} by R_3 (ME and MF). The relation between V_{in} and V_{out-} can be expressed as

$$\left.\begin{aligned} V_{in} > 0;\ V_{out-} &= 0 \\ V_{in} < 0;\ V_{out-} &= V_{in} \end{aligned}\right\} \tag{4}$$

Figure 2(*b*) shows the bias voltage source. The bias voltages, V_{bias+} and V_{bias-}, are applied to make MOS diodes in the rectifiers MD1 to MD4 turn on all the time to clad the output voltage excursions during the zero crossings for operation at high frequency. The current I_2 flowing through MD5 and MD6 generates V_{bias+}, and the current I_3 flowing through MD7 and MD8 produces V_{bias-}. Both V_{bias+} and V_{bias-} must be the minimum and maximum voltages, respectively, that can make MD1 to MD4 turn on all the time to get the minimum offset voltages at the outputs; that is carried out by adjusting I_2 for V_{bias+} and I_3 for V_{bias-}. To protect the effects of loads and outputs of the V–I converter on the bias voltages, the voltage buffers, already mentioned above, are used. M11 to M14 are the buffer of V_{bias-}, the drain currents of M11 and M13 are made equal to I_4 by setting the same characteristics of MI6 to MI10. Similarly, M15 to M18 are the buffer of V_{bias+}; the drain currents of M15 and M17, and I_4, are made the same currents by using the same characteristics of MI6, MI7, MI9, MI11 and MI12.

3. Simulation results

To verify the theoretical design, the proposed rectifier was simulated by using a PSPICE program with the 0.5 μm MOSFET model obtained through MIETEC as listed in table 1. The W/L parameters of MOSs and the constant current sources in the proposed rectifier are listed in table 2. The supply voltage used is ±1.2 V. The DC transfer characteristics of the proposed rectifier are shown in figure 3, which displays the operating voltage range from −300 mV to 300 mV of the input voltage. In this range, a power consumption of approximately 1.8 mW was observed. The magnified zero crossings of figure 3 are shown in figure 4. In this figure, the blunting regions are found as $-3\,\text{mV} \le V_{in} \le 2\,\text{mV}$ for the positive half-wave output and $-2\,\text{mV} \le V_{in} \le 1\,\text{mV}$ for the negative half-wave output.

Applying the $100\,\text{mV}_{peak}$ sine wave at the input of the proposed rectifier, the input and output signals at frequencies of 1 MHz, 10 MHz and 100 MHz are shown in figures 5, 6 and 7, respectively. The amplitude errors between the input and output signals in figure 7 result from the decrease of the gain of the proposed rectifier for the operation at high frequency. There are two methods of compensating this problem. The first method is to increase the value of R_2 and R_3 by decreasing the W/L ratios of MC to MF. The second method is to increase the gain of the current mirrors in the proposed rectifier by increasing the W/L ratios of M6, M7, M9 and M10.

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```
.MODEL NM NMOS LEVEL = 3
+ UO = 460.5 TOX = 1.0E-8 TPG = 1 VTO = 0.62 JS = 1.08E-6
+ XJ = 0.15U RS = 417 RSH = 2.73 LD = 0.04U VMAX = 130E3
+ NSUB = 1.71E17 PB = 0.761 ETA = 0.00 THETA = 0.129 PHI = 0.905
+ GAMMA = 0.69 KAPPA = 0.10 CJ = 76.4E-5 MJ = 0.357 CJSW = 5.68E-10
+ MJSW = 0.302 CGSO = 1.38E-10 CGDO = 1.38E-10 CGBO = 3.45E-10
+ KF = 3.07E-28 AF = 1 WD = +0.11U DELTA = +0.42 NFS = 1.2E11
+ DELL = 0U LIS = 2 ISTMP = 10 TT = 0.1E-9

.MODEL PM PMOS LEVEL = 3
+ UO = 100 TOX = 1.0E-8 TPG = 1 VTO = -0.58 JS = 0.38E-6
+ XJ = 0.10U RS = 886 RSH = 1.81 LD = 0.03U VMAX = 113E3
+ NSUB = 2.08E17 PB = 0.911 ETA = 0.00 THETA = 0.120 PHI = 0.905
+ GAMMA = 0.76 KAPPA = 2 CJ = 85E-5 MJ = 0.429 CJSW = 4.67E-10
+ MJSW = 0.631 CGSO = 1.38E-10 CGDO = 1.38E-10 CGBO = 3.45E-10
+ KF = 1.08E-29 AF = 1 WD = +0.14U DELTA = 0.81 NFS = 0.52E11
+ DELL = 0U LIS = 2 ISTMP = 10 TT = 0.1E-9
```

Table 1. MOSFET model used in the simulation.

MI1–MI12, M1–M5, M8	20 μm/0.6 μm
M6, M9	26.7 μm/0.6 μm
M7, M10	26.3 μm/0.6 μm
MA–MF	2 μm/2 μm
MD1–MD8	2 μm/0.6 μm
MI1–M18	100 μm/0.6 μm
I_1	20 μA
I_2, I_3	250 μA
I_4	100 μA

Table 2. W/L parameters and constant current sources of the circuits in figure 2.

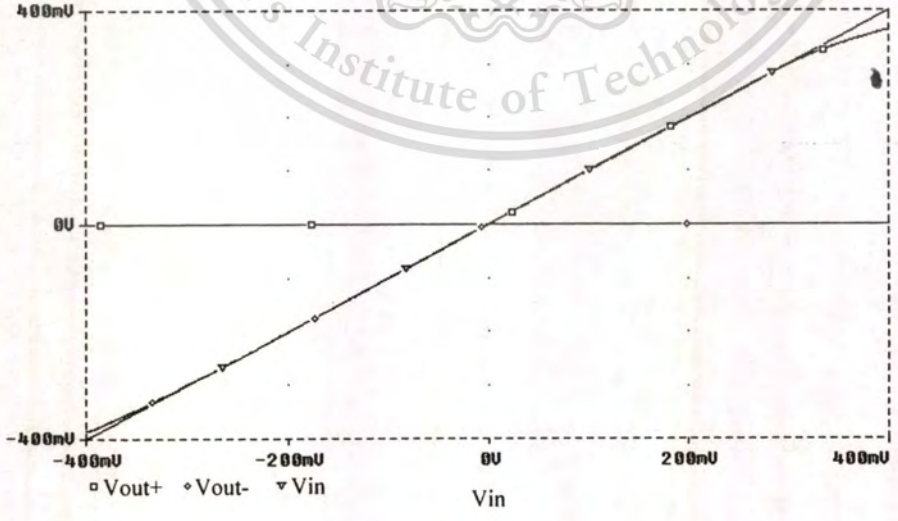

Figure 3. DC transfer characteristics of the proposed rectifier.

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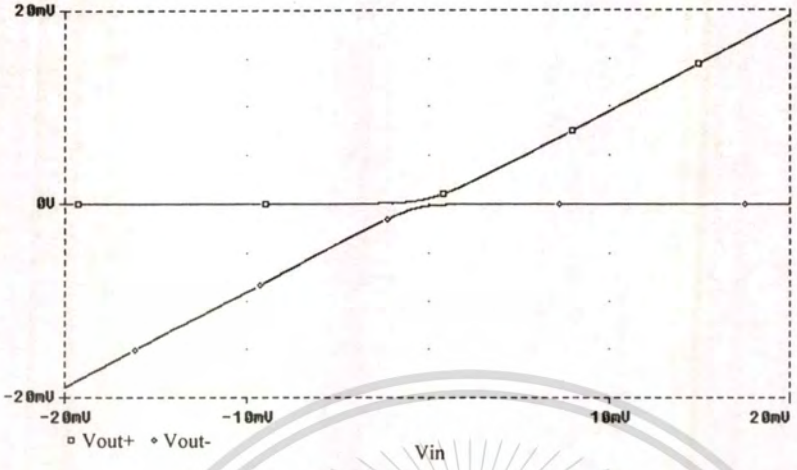
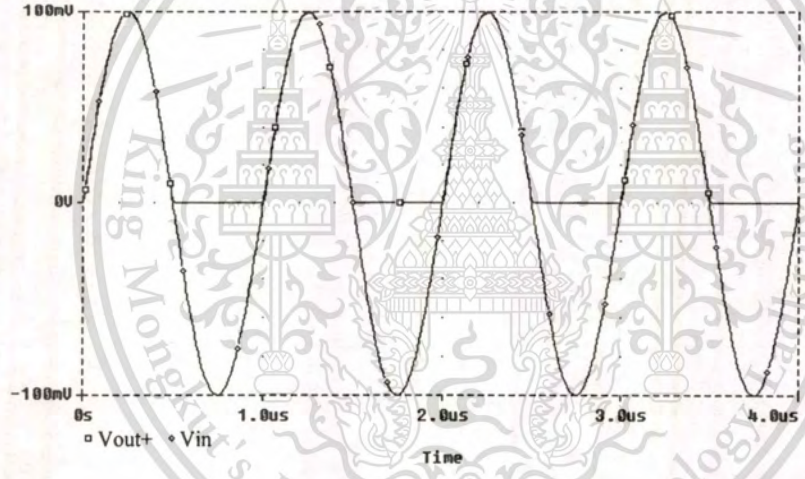


Figure 4. Magnified zero crossings of figure 3.

(*a*)



(*b*)

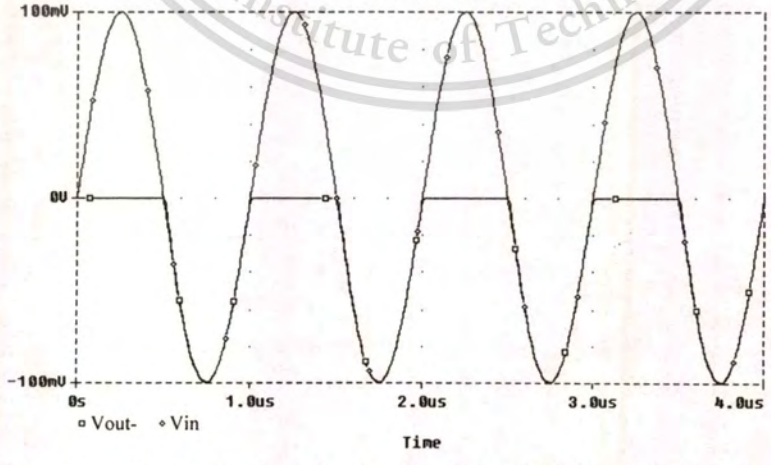


Figure 5. Operation of the proposed rectifier at a frequency of 1 MHz: (*a*) input and positive half-wave output; (*b*) input and negative half-wave output.

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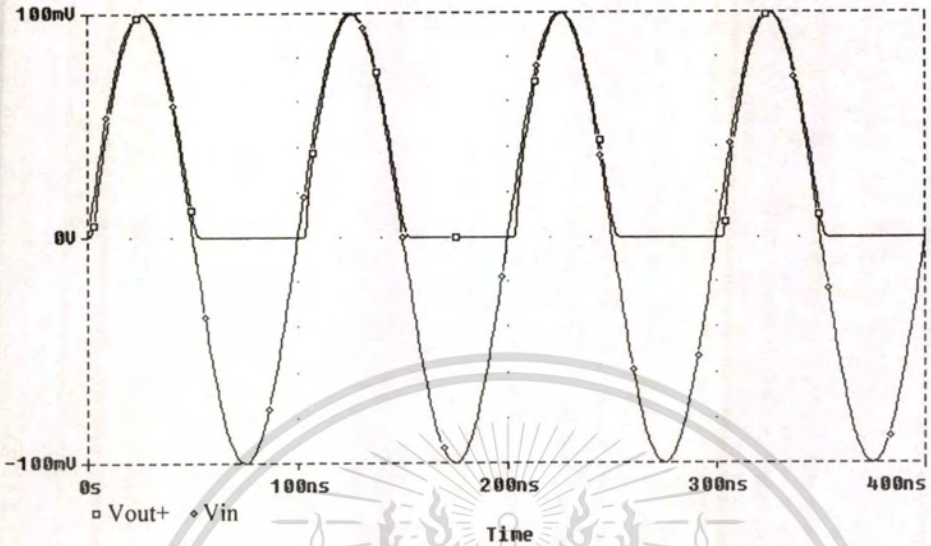
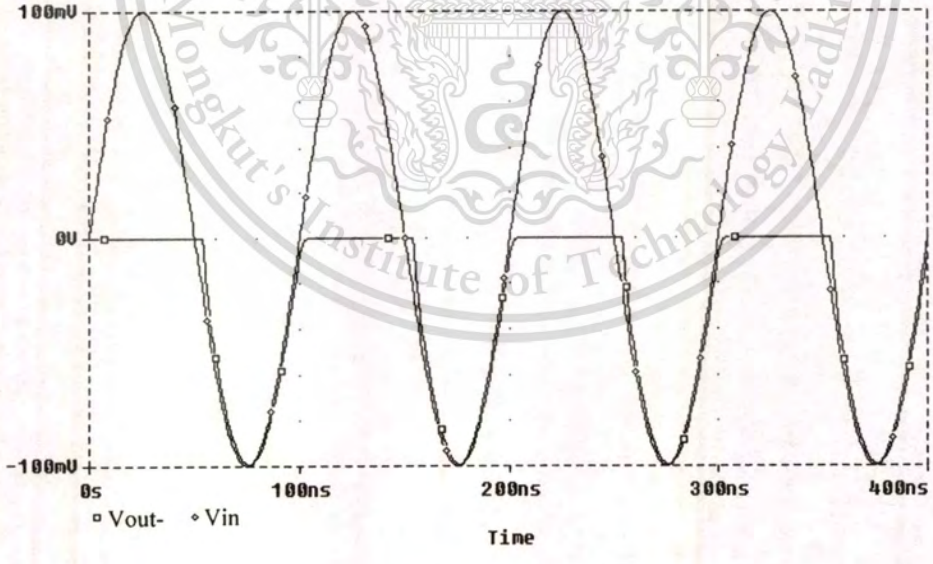


(*a*)



(*b*)

Figure 6. Operation of the proposed rectifier at a frequency of 10 MHz: (*a*) input and positive half-wave output; (*b*) input and negative half-wave output.

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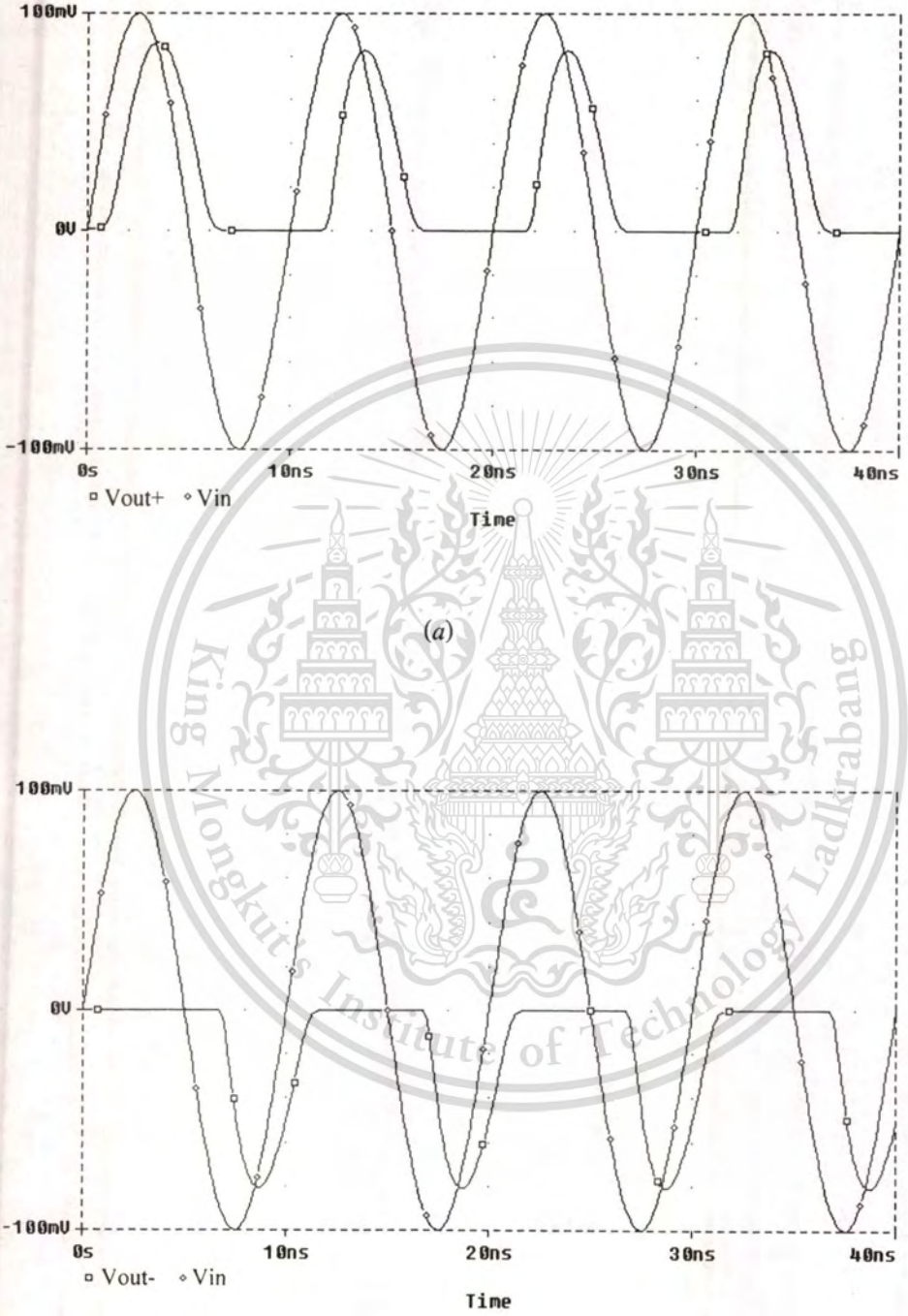

Figure 7. Operation of the proposed rectifier at a frequency of 100 MHz: (*a*) input and positive half-wave output; (*b*) input and negative half-wave output.

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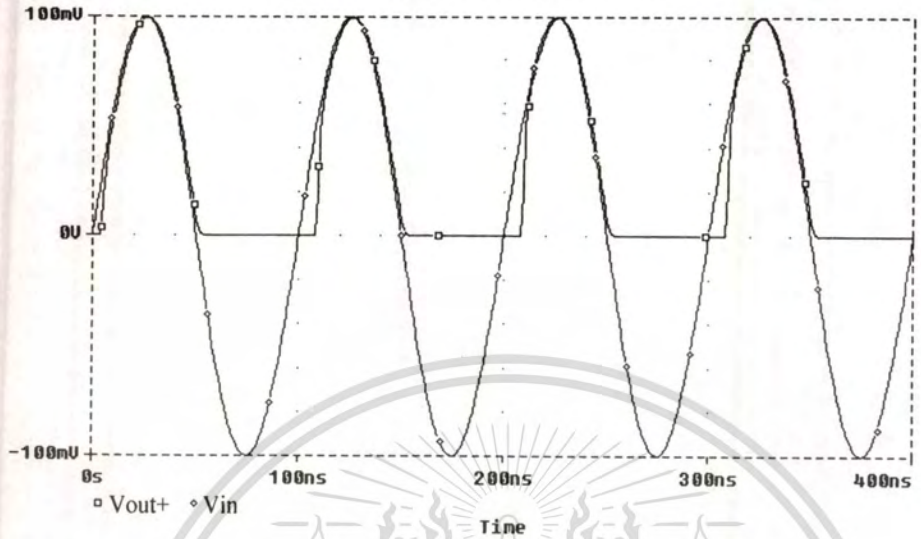
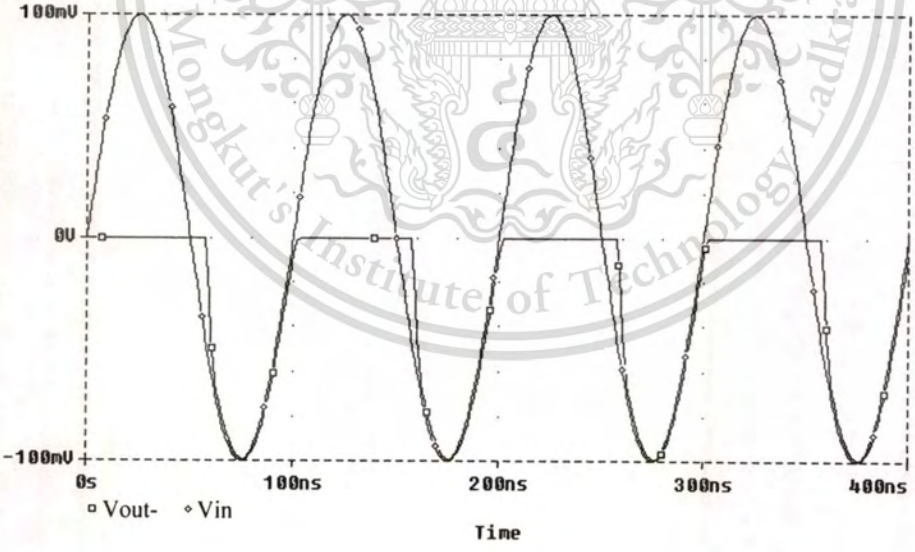


(*a*)



(*b*)

Figure 8. Operation of the proposed rectifier at 10 MHz without the MOS diode bias voltages: (*a*) input and positive half-wave output; (*b*) input and negative half-wave output.

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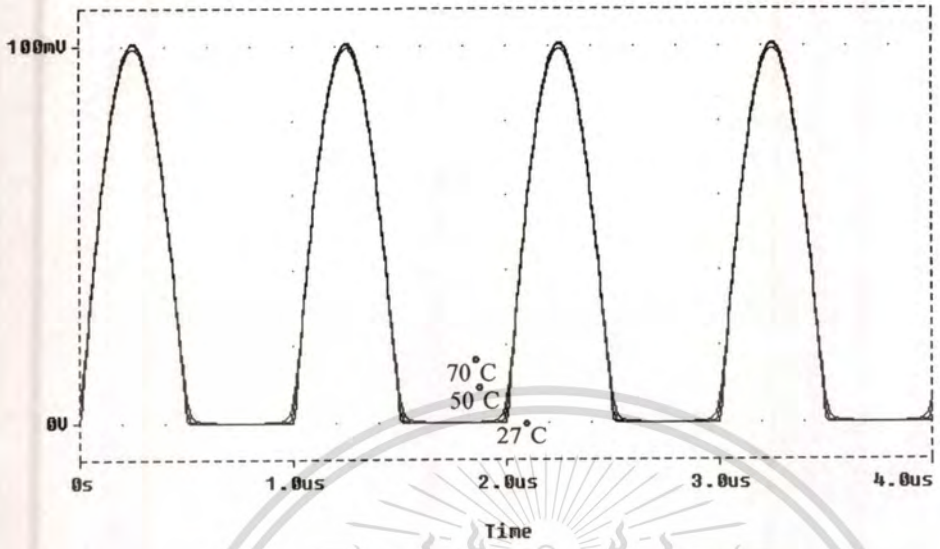

Figure 9. Positive half-wave outputs at different temperatures.

We again simulated the proposed rectifier at the frequency of 10 MHz without the diode bias voltage by adjusting $I_2 = I_3 = 0\,\mu A$. The input and output signals in this case are shown in figure 8. Note that the output signals in figure 8 have errors by the time the voltages change from 0 V, which result from the non-conduction/conduction transition problem of MOS diodes. Comparing the output signals in figure 8 with those in figure 6, it is clearly seen that by using the MOS diode bias voltages the operating frequency of the proposed rectifier is increased.

Figure 9 shows the positive half-wave outputs at temperatures of 27°C, 50°C and 70°C. At the zero crossings of signals in figure 9, it is evident that, for the proposed rectifier, the shifts in voltage between each temperature are much lower than those of the temperature independent current conveyor rectifier proposed by Hayatleh *et al.* (1994).

4. Conclusions

In this paper, we have reported the design of a CMOS dual output half-wave rectifier that rectifies the signal in the current mode. The proposed rectifier is based on previously reported current conveyer rectifiers. However, with the different circuit structure, the proposed rectifier yields features superior to the previously reported current conveyor rectifiers in view of the voltage employed, the power consumption, the number of devices, the operating frequency, the temperature stability, and simplicity for IC fabrication. The proposed rectifier uses a ± 1.2 V supply voltage and produces an input operating voltage range from -300 mV to 300 mV. In addition, it has an operating frequency up to 100 MHz. However, this operating frequency is obtained only from simulation, when the proposed rectifier is built as an IC, this operating frequency will be lessened by the effect of parasitic capacitance in the IC.

The proposed rectifier uses the MOS resistors R_2 and R_3 to convert the output currents to output voltages which are suitable for a high impedance load. In fact, the

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MOS resistors of the input V–I converter and the output I–V converter are based on complementary source followers loaded by parallel n-MOS and p-MOS transistors working in the triode region. The resultant resistors R_1, R_2 and R_3 are not quite linear, but the cascade of the input V–I converter and the output I–V converter causes partial compensation for the nonlinearity of these resistors. If the rectifier is loaded with a low impedance load, the load may be connected directly instead of resistor R_2 or R_3 (it needs the linear resistor R_1).

Acknowledgments

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References

BRUUN, E., 1993, CMOS high speed, high precision current conveyor and current feedback amplifier structures. *International Journal of Electronics*, **74**, 93–100.

HAYATLEH, K., PORTA, S., and LIDGEY, F. J., 1994, Temperature independent current conveyor precision rectifier. *Electronics Letters*, **30**, 2091–2093.

KHAN, A. A., ABOU EL-ELA, M., and AL-TURAIGI, M. A., 1995, Current-mode precision rectification. *International Journal of Electronics*, **79**, 853–859.

LIDGEY, F. J., HAYATLEH, K., and TOUMAZOU, C., 1993, New current-mode precision rectifiers. *Proceedings of the IEEE International Symposium on Circuits and Systems*, Chicago, pp. 1322–1325.

LTP ELECTRONICS LTD, 1993, *CCII01 current-conveyor data sheet* (Oxford).

RAMIREZ-ANGULO, J., 1992, High frequency low voltage CMOS diode. *Electronics Letters*, **28**, 298–300.

SURAKAMPONTORN, W., and RIEWRUJA, V., 1992, Integrable CMOS sinusoidal frequency doubler and full-wave rectifier. *International Journal of Electronics*, **73**, 627–632.

TOUMAZOU, C., LIDGEY, F. J., and CHATTONG, S., 1994, High frequency current conveyor precision full-wave rectifier. *Electronics Letters*, **30**, 745–746.

WANG, Z., 1990, 2-MOSFET transresistor with extremely low distortion for output reaching supply voltages. *Electronics Letters*, **26**, 951–952.

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About the author

Adisak Monpapassorn was born in Bangkok, Thailand, in 1971. He received the Bachelor's degree in electrical engineering in 1992 from Siam University, Bangkok, Thailand, and the Master's degree in electrical engineering in 1997 from King Mongkut's Institute of Technology Ladkrabang, Bangkok, Thailand. In 1992, he joined Department of Electronic Engineering, South-East Asia University, Bangkok, Thailand, as a lecturer.

Now, he is an assistant professor in electronic at South-East Asia University. His research interests include the designs of high-frequency current mode analog circuits, filters, oscillators, and analog signal processing circuits.

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