รายงานการวิจัย

เรื่อง วงจรรวมอนาลอกย่านความถี่วิทยุที่ใช้กำลังงานต่ำสำหรับระบบเซ็นเซอร์ไร้สาย

Low power radio frequency analog integrated circuit for wireless sensor

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สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง

รายงานการวิจัย

1. ชื่อโครงการวิจัย

(ไทย) วงจรรวมอนาลอกย่านความถี่วิทยุที่ใช้กำลังงานต่ำสำหรับระบบเซ็นเซอร์ไร้สาย

(อังกฤษ) Low power radio frequency analog integrated circuit for wireless sensor

2. บทคัดย่อ

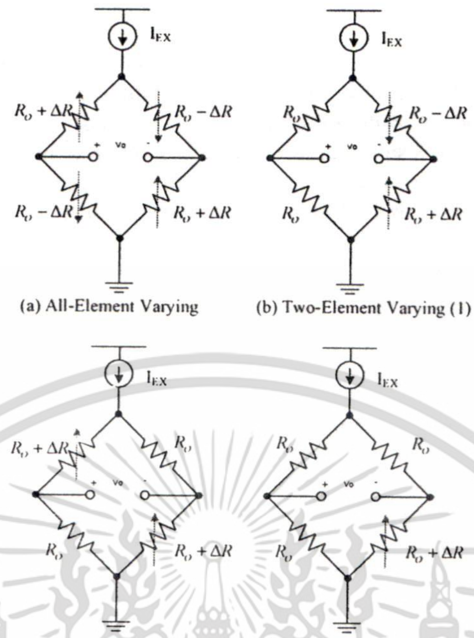
โครงการวิจัยนี้ได้ทำการออกแบบวงจรรวมอนาลอกสำหรับประยุกต์ใช้งานในระบบเซ็นเซอร์ไร้สายที่ใช้ความถี่วิทยุ (radio frequency wireless sensor) ที่ต้องการวงจรที่ใช้กำลังงานไฟฟ้าต่ำ โครงการนี้ได้ทำการออกแบบส่วนวงจรที่เชื่อต่อกับระบบเซ็นเซอร์แบบเปียร์โซรีซีสทีฟ (piezoresistive) สำหรับวัดความดัน โดยทำการออกแบบและจำลองการทำงานด้วยเทคโนโลยีซีมอสขนาด 0.35 ไมครอนและใช้แรงดันไฟเลี้ยง 1.5 โวลต์

This project is concerned with the design of low-power analog integrated circuits for radio frequency wireless sensor application. We have designed a low-power low-voltage CMOS interface circuit with digital output for piezoresistive sensor. An input current sensing configuration is used to detect change in piezoresistance due to applied pressure and allow low-voltage circuit application. The proposed interface circuit is realized in 0.35-μm CMOS technology and operates under a single 1.5-V power supply voltage.

3. บทนำ

Advance in CMOS processing and micromaching technologies have allowed various types of microsensor to be integrated with signal processing circuitry in a single chip, e.g. in [1]. With submicron CMOS technology, there is a need for instrumentation amplifier that interfaces with on-chip transducer and can operate under a low power supply voltage.

The aim of this work is to design and realize a low voltage interfacing circuit for an implantable blood pressure as [2]. The sensor is piezoresistive and its resistance is change when there is a pressure variation. The resistance change is traditionally detected by using the Wheatstone bridge circuit, whose sensitivity depends on the excitation voltage or current. For decent bridge sensitivity, high excitation voltage or current is needed, which may prevent low voltage and low power operation. Currently there is the need for the development of small and low cost conditioning circuitry of sensor interfacing circuit, capable of communication with a microprocessor. In order to facilitate communication with microcomputers is demanded to offer digital output. This makes the output signal noise immune and enables the sensor to be connected directly to a microcomputer without using an A/D converter [3],[4],[5]. In this project, a new low power low voltage instrumentation amplifier using a current-sensing topology is proposed



(a) All-Element Varying (b) Two-Element Varying (1)

(c) Two-Element Varying (2) (d) Single-Element Varying

Fig. 2. Current-driven Wheatstone bridge configurations

TABLE I
SUMMARY OF THE RESISTIVE READOUT INPUT CONFIGURATIONS

Input configuration	Output voltage or current	Linearity error (%/%)
Fig. 1(a)	$V_O = V_{EX}\left(\frac{\Delta R}{R_O}\right)$	0
Fig. 1(b)	$V_O = \frac{V_{EX}}{2}\left(\frac{\Delta R}{R_O}\right)$	0
Fig. 1(c)	$V_O = \left(\frac{\Delta R}{2R_O+\Delta R}\right)V_{EX} \approx \frac{1}{2}\left(\frac{\Delta R}{R_O}\right)V_{EX}$	0.5
Fig. 1(d)	$V_O = \frac{1}{2}\left(\frac{\Delta R}{2R_O+\Delta R}\right)V_{EX} \approx \frac{1}{4}\left(\frac{\Delta R}{R_O}\right)V_{EX}$	0.5
Fig. 2(a)	$V_O = (\Delta R)I_{EX}$	0
Fig. 2(b)&(c)	$V_O = \left(\frac{\Delta R}{2}\right)I_{EX}$	0
Fig. 2(d)	$V_O = \frac{R_O}{4}\left(\frac{\Delta R}{R_O+\frac{\Delta R}{4}}\right)I_{EX} \approx \frac{\Delta R}{4}I_{EX}$	0.25
Fig. 3(a)	$\Delta I = \frac{(V_{EX}-V_{CM})}{R_O}\cdot\frac{(\Delta R/R_O)}{(1+\Delta R/R_O)} \approx \frac{(V_{EX}-V_{CM})}{R_O}\cdot(\Delta R/R_O)$	1
Fig. 3(b)	$\Delta I = \frac{2(V_{EX}-V_X)}{R_O}\cdot\frac{(\Delta R/R_O)}{\left[1-(\Delta R/R_O)^2\right]} \approx \frac{2(V_{EX}-V_X)}{R_O}\cdot(\Delta R/R_O)$	0.01

B. Current-driven Wheatstone bridge

The Wheatstone bridges can also be driven by a constant current source, as shown in Fig. 2. All current-driven bridges are inherently linear, except for the single-element varying configuration in Fig. 2(d). The sensitivity of current-driven bridges is proportional to the excitation current, I_{EX}. Thus, a large I_{EX} is required to obtain high sensitivity, which increases the power consumption of the bridge.

The digital output pulse rate will be proportional to the applied pressure. The delta-sigma converter is a synchronized charge-balancing converter suitable for embedded smart sensor due to its simplicity.

The operation of the circuit can be described as follows. When no pressure is applied, I_S is zero and the capacitor will not be charged or discharged, and thus no digital output pulse. Assume that the output of the comparator is low, the switch SW will be open and the current I_S charges the capacitor. The voltage across the capacitor increases until it reaches the reference voltage V_r. At this instance, the output of the comparator goes to the negative saturation state and the output of the flip-flop will go LOW at the next rising edge of the clock. Then the switch SW is turned on, thus allowing the capacitor to be discharged with the current I_r-I_S, where I_r is the DC reference current. The capacitor voltage is discharged until it is less than V_r, at which the output of the comparator goes back to the positive saturation state. Then, at the next rising of the clock, the output of the flip-flop will go HIGH and turn off SW and I_r, thus the capacitor will be charged again with I_S.

It can be deduced that the number of digital output pulse, N, over a fixed measuring time interval, T_{int}, is proportional the value of I_S as described in eqn. (1). The output pulses during T_{int} are counted by a digital counter, and the total number of pulses is the digital representation of the applied pressure.

$$\frac{I_S}{I_r} = \frac{NT_{CLK}}{T_{int}} \qquad (1)$$

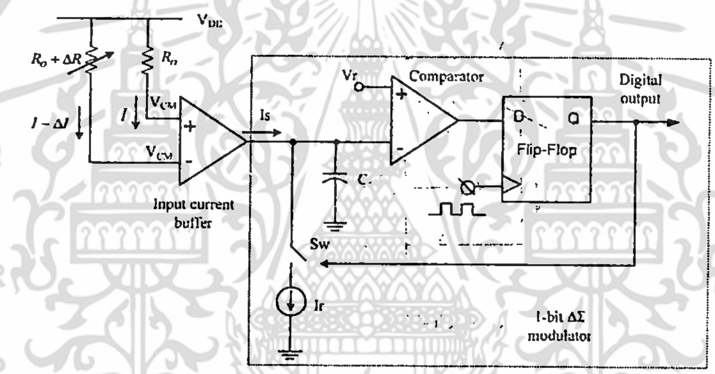


Fig. 4 Current-sensing resistive readout configuration

4.3 Circuit description

A. Input Current Buffer

Fig. 5 shows the circuit implementation of the input current buffer, which can be described as follows. The input section of the current buffer is realised by M1-M4 and DC biased current sources (M13-M20), which has be coined as the "flipped voltage follower". The circuit employs negative feedback to achieve small input resistance and fixed input common-mode voltage V_{CM}, as given by (2) where V_{B1} and I_A are DC bias voltage and current, and other parameters have their usual meanings. The input current buffer can be implementation in Fig. 5 the operation of the current buffer can be explained as follows. Low input resistance of the input current buffer is ensured by the flipped voltage follower circuit [6]. This fixes the input common-mode voltage of the input current buffer, rendering a constant voltage dropped across the resistors. Under a pressure variation, the resistance value of piezoresistor is changed and an input current (ΔI) flows into M_4, which is also mirrored to M_6. On the other hand, compensation resistor is fixed and does not vary with pressure, thus a constant common-mode current flows through M_3 and M_5. The accuracy of current mirroring is vital to the linearity and common-mode rejection ratio (CMRR) of the current buffer. This is achieved by using auxiliary amplifiers, A_1, and A_2 to match the drain-source voltages of M_3, M_5, and M_4, M_6. All auxiliary amplifiers are identical and are realized by using the conventional two-stage operational amplifier. Transistors M_9-M_{12} realizes cascode current mirrors that are used to eliminate DC common-mode current from the desired signal and the current mirror (M21- M24) are used fix the common-mode voltage in output of current buffer circuit and transmit output current (ΔI) to sigma-delta modulator circuit.

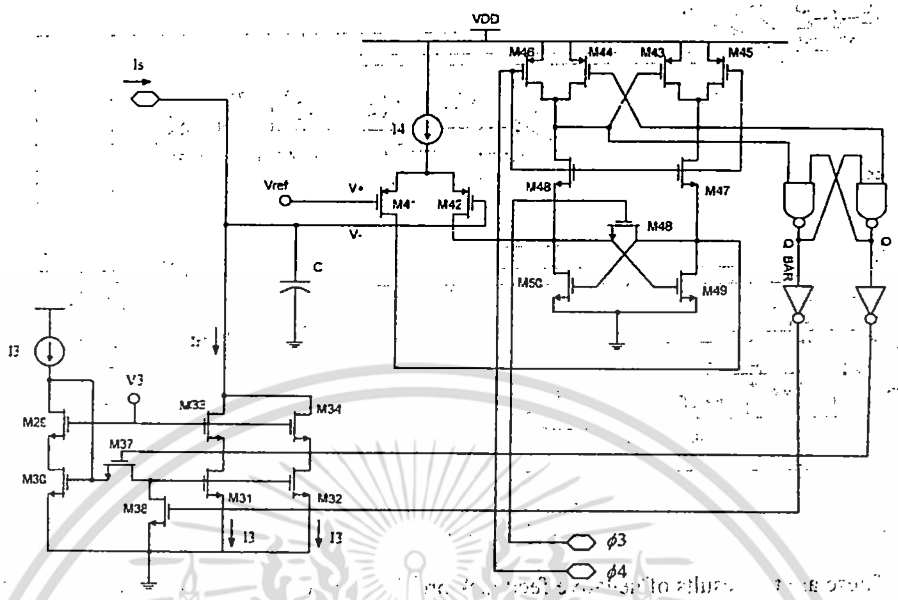


Fig. 6 First-order sigma-delta modulator

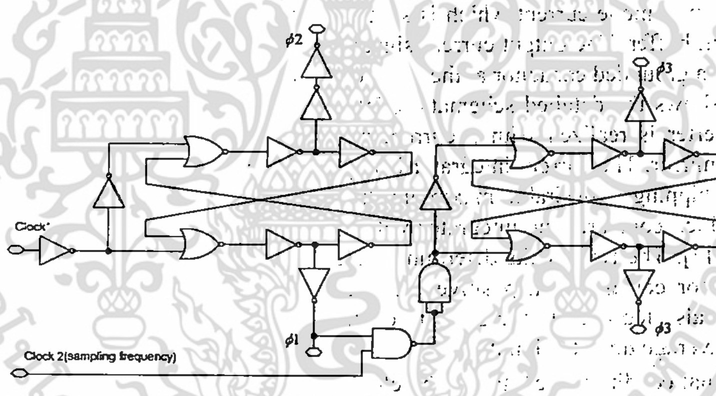


Fig. 7 Clock generator circuit

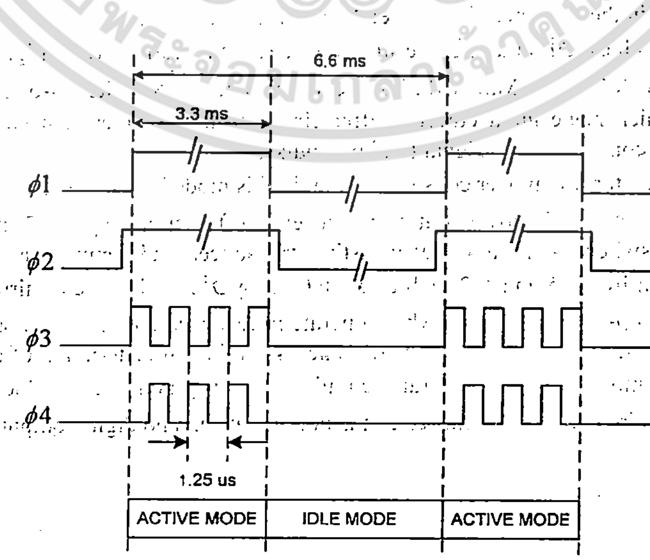


Fig. 8 Timing diagram of control signals

TABLE II
PERFORMANCE SUMMARY OF THE PROPOSED INTERFACE CIRCUIT

Parameter	Value
Supply voltage	1.5 V
Maximum Linearity error (±1% change in R_P)	0.23%
Resolution	9.17 bit
Conversation time	6.6 ms
Maximum Power dissipation (Active Mode)	298 μW
Power dissipation (Idle Mode)	78.8 μW

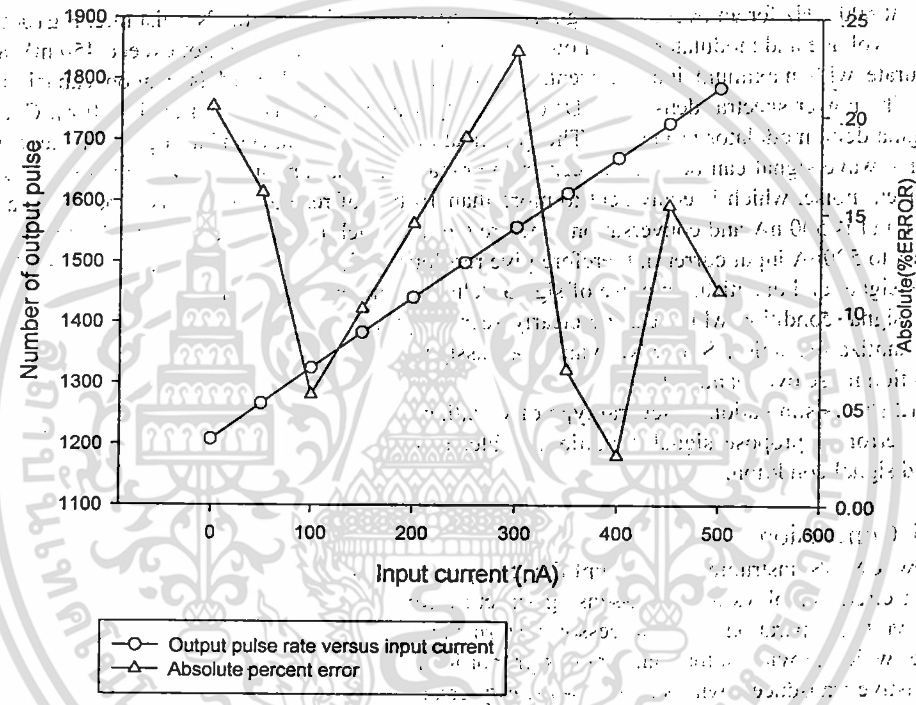
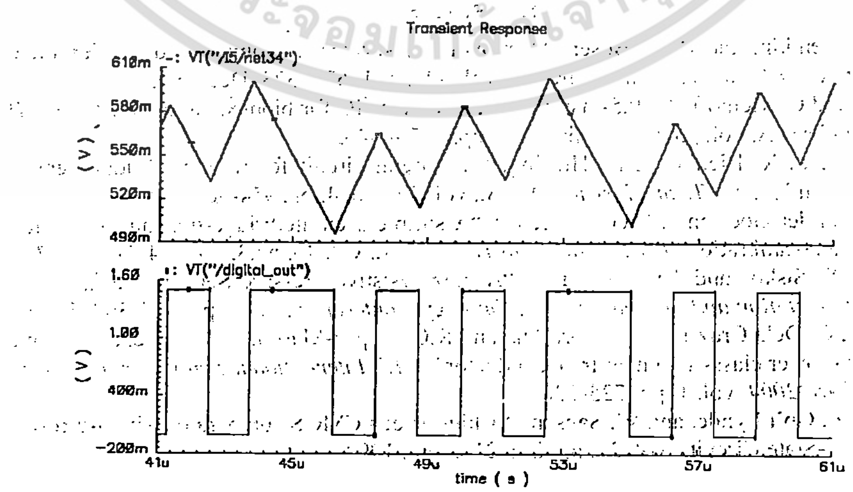
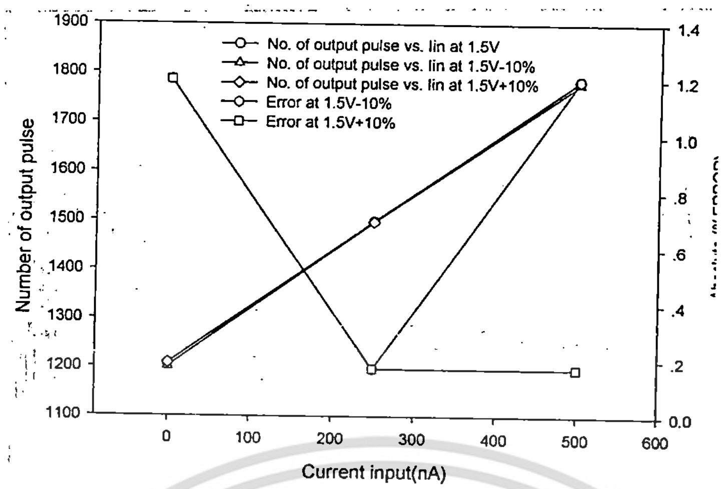


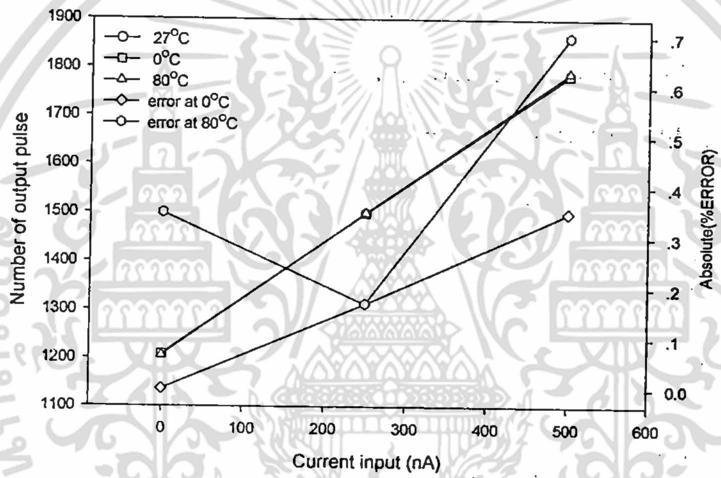
Fig. 9 Number of output pulse versus input current



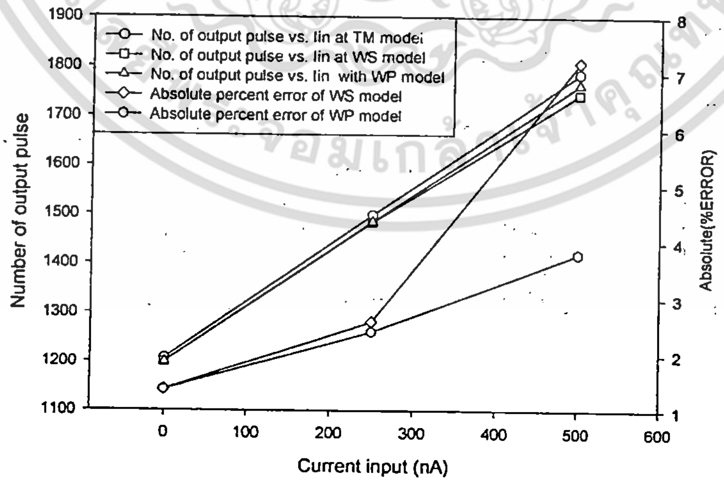
(a) Integrator output and output pulse.



(a) Simulation result of ±10% supply variation

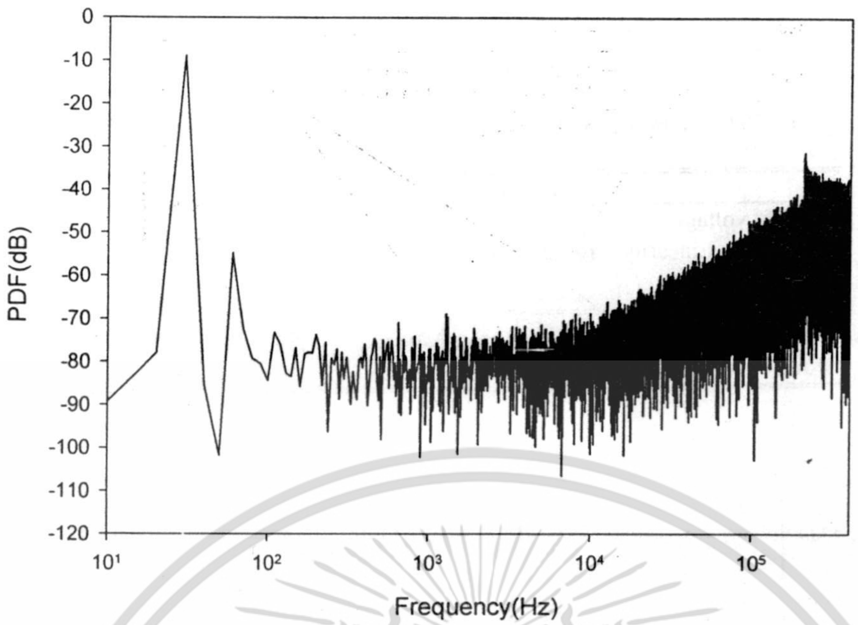


(b) Simulation result of temperature variation



(c) Simulation result of process variation

Fig. 12 Simulation of several variation of propose signal condition



(b) Power spectral density of 30 Hz sinusoidal input.

Fig. 10 First order sigma delta modulator simulation results.

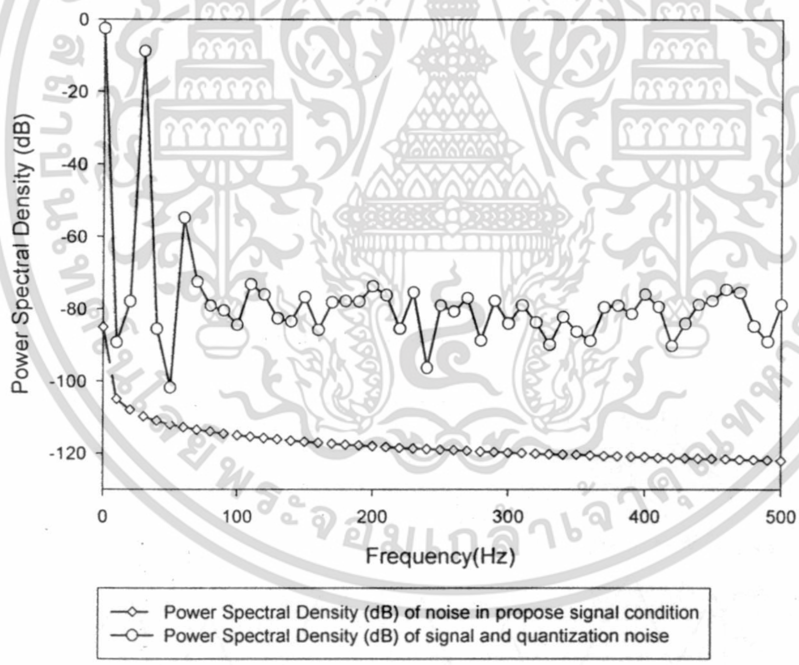


Fig. 11 PSD of signal and noise of propose signal condition

4.4 Simulation results

In this work, the proposed signal condition is targeted for an implantable pressure sensor [2] with the sensitivity of 5 μV/V/mmHg. The nominal resistance of piezoresistance (R_O) is 2.5 KΩ. The maximum change of ±1% from nominal value is expected from a typical blood pressure range (-500 to +500 mmHg). The signal condition was designed to operate with a single 1.5-V power supply voltage. The circuit was simulated using Spectre™ with process parameters from a 0.35-μm standard CMOS technology. The input common-mode voltage of the amplifier is set to 1.4 V to minimize the quiescent current flowing through R_O. Under the nominal value of pizoresistive transducer(2.5 KΩ), a typical simulation measurement set for proposed circuit and its linear regression are shown in Fig. 9. A linear dependence of number of pulse versus input current from 0nA to 500nA which enable to resistance variation 1% of nominal value is obtained. The nonlinearity measured using a best-fit line method for absolute maximum error is less than 1% (full scale output).

Fig. 10 shows simulation results with a 30 Hz 500 nA sinusoidal input. The comparator clock are running at 800 KHz for an over sampling ratio to estimate 13333 times the Niquist rate. Fig10(a) show integrator voltage and modulator digital output. The integrator voltage does not exceed 450 mV and did not saturate with maximum input current, indicating that the 20pF used is a good capacitor value choice. The power spectral density (PSD) of the output digital data is shown in fig. 10(b). Consistent with sigma delta modulator properties, The quantization noise is "bunched" at higher frequencies. The 30Hz sine wave signal can be clearly seen in the binary data stream and is approximate 60 dB above the adjacent noise, which is equivalent to more than 10 bits of resolution. In this paper the maximum current input is 500 nA and conversation time are 6.6 ms which in Fig. 10 different of output pulse are 578 (0nA to 500nA input current), therefore give resolution of propose signal condition is 9.17 bit. Fig 11 show signal and quantization noise of sigma-delta modulator are compared with generated noise by propose signal condition which can be clearly seen in generated noise by propose signal condition is lower quantization noise. Sine SNR value can assigned by total power of signal to total power of quantization noise over bandwidth.

Fig. 12 shows simulation of several type of variation(supply, temperature and process) and absolute percent error of propose signal condition. Table. II summarizes the simulated performance of the proposed signal condition.

4.5 Conclusion

A new CMOS instrumentation amplifier for piezoresistive transducer has been described. The proposed circuit employs a current-sensing structure for resistive readout, which enables low power and low voltage operation. The processor performs an A/D conversion with a first order sigma-delta converter which provide output pulse rate is proportional to the current input by resistance variation of piezoresistive transducer with small non-linearity error. The resolution could be as approximate 9.17 bit for conversion time of 6.6 ms. Preliminary simulation results suggest that the proposed interfacing circuit is suitable for implantable sensor applications.

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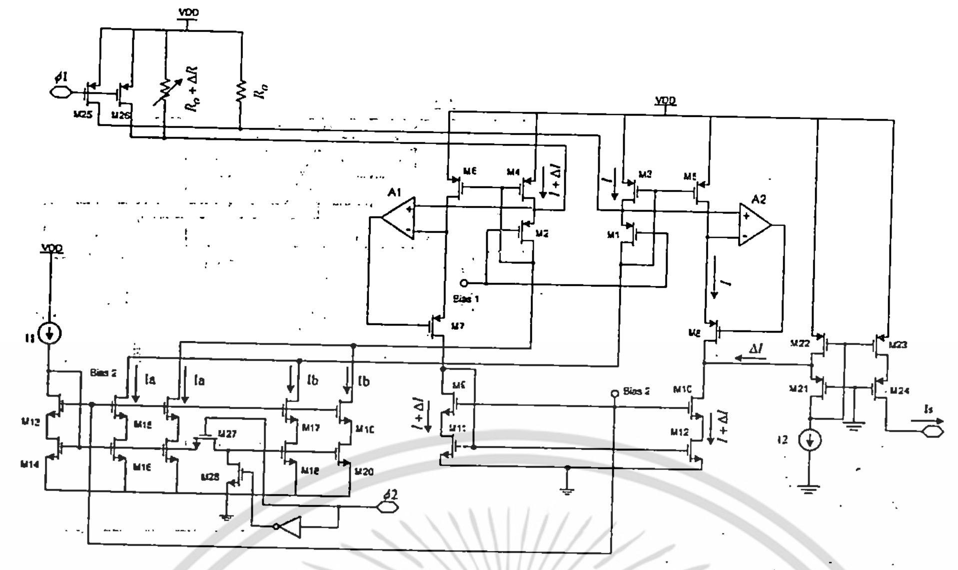

Fig. 5 Input current buffer

These are the results of negative feedback provided by M1 (M2), M3 (M4) and the DC current source Ibias. This ensures a fixed voltage dropped across both resistors. Under an applied presure variation, the piezoresistance is changed creating an input current into M3, which is mirrored to the output of the current buffer via M5. On the other side, Ro is fixed and does not vary with pressure; this creates a fixed common-mode current which is subtracted from the time-varying current signal at the output of the current buffer. The output current signal, Is, which is free of common-mode component, is applied to charge a grounded capacitor at the input of the following delta-sigma converter.

In Fig. 6 shows the detailed schematic of the first-order sigma-delta modulator circuit. The current DAC converter is realized with a current mirror and two switch transistors that enable or disable the current mirror. The current integrator is implemented with a capacitor whose value is set to prevent nonlinear chipping at desirable maximum input signal sizes and minimum operating speeds. The comparator, which compares the integrator voltage and a reference voltage, produces the one bit output data stream [7]. The two clocks determine the comparison time and the time at which data is valid. The comparator consists of a positive feedback differential amplifier and a data latch. The comparator outpt is also fed back to the DAC to control the DAC feedback current which makes the comparator output average track the input.

The proposed signal condition is controlled by clock $\phi 1$ and $\phi 2$ which generate by clock generator circuit in Fig. 7 and Timing diagram of clock show in Fig 8. Both clock $\phi 1$ and $\phi 2$ are enable the propose signal condition in the two operation mode: Active and Idle mode.

In Active mode ,both clock $\phi 1$ and $\phi 2$ are high and cause tail current I_b in Fig. 5 moved in to current buffer circuit by M27 and M28 (M27 switched-on and M28 switched-off) and transistor M25,M26 switch-off which make input current buffer circuit to measurement current signal ΔI and sigma-delta modulator is convert current signal to digital pulse.

In Idle mode is designed for low-power consumption by in this mode both clock $\phi 1$ and $\phi 2$ are low and cause tail current I_b in Fig 5 moved out from current buffer circuit by M27 and M28 (M27 switched-off and M28 switched-on) and piezoresistive transducer and temperature compensation resistor are shorted circuit by M25 and M26 which switch-on by $\phi 1$. Both current mirror M3,M5 and M4,M6 are switch-off by op-amp A1 and A2 which operate in feedback loop around both drain-source terminal of M3,M5 and M4,M6 ,make the voltage drop across drain-source terminal of these transistor are estimate zero. In Idle mode the clock generator circuit are not pay non-overlap clock $\phi 3$ and $\phi 4$ to sigma-delta modulator circuit and make this circuit is not operate and no digital output pulse.

C. *Proposed Current-sensing configuration*

In both voltage- and current-driven Wheatstone bridges, the DC common-mode voltage of the input amplifier is normally in the middle of the power supply voltage (assuming $V_{EX} = V_{DD}$), due to the voltage dropped across the resistors.

Under low power supply voltage (< 2 V) where the threshold voltage is a significant portion of V_{DD}, it is difficult to realize a high-CMRR amplifier with an input common-mode voltage in the middle of V_{DD}. This can be alleviated by using a current-sensing topology, as shown in Fig. 3. The current-sensing configuration uses two resistors that are connected between an excitation voltage (V_{EX}) and a fixed input common-mode voltage (V_{CM}) of a current buffer. Since the voltage across the resistors is fixed, change in resistance due to applied pressure generates an input current to flow into the current buffer. In this work, V_{EX} is equal to V_{DD} and V_{CM} is designed to be near V_{DD} to minimize the DC current flowing through the resistors.

There can be one or two piezoresistors in the current-sensing topology, as shown in Fig. 3(a) and Fig. 3(b) respectively. Both resistors in current sensing topology should have equal nominal resistance under no pressure variation. Under a pressure variation, the input current signal and the linearity error of both current-sensing configurations can be written as shown in Table I. The two-element varying current-sensing configuration has a much lower linearity error. However, as aforementioned, linearity error can be compensated easily; therefore the single-element varying arrangement is chosen in this work to save cost and area, and to mitigate resistance matching requirement. In addition, the fixed resistor can be used to compensate for temperature dependence of the piezoresistor.

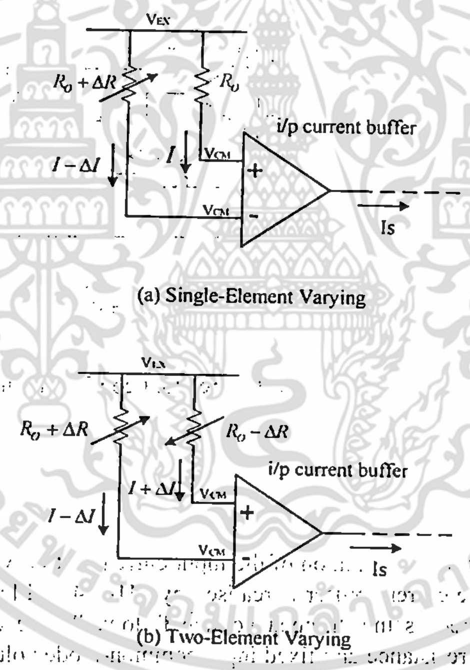

Fig. 3 Current-sensing resistive readout configuration

4.2 Architecture of the proposed interface circuit

Using the single-element varying current-sensing topology, Fig. 4 shows the simplified circuit diagram of the proposed interface circuit, which consists of an input current buffer and a 1-bit delta-sigma analog-to-digital converter. The piezoresistor and the reference resistor are connected between the power supply voltage and the input of the current buffer. The input common-mode voltage, V_{CM}, of the current buffer is kept constant due to the negative feedback within the circuit. Thus the voltages across the resistors are constant, and when the pressure is applied, it creates a current flow into the current buffer. The current buffer measures the diffential input current and gives a single-ended output current, I_S, to charge up a capacitor, which acts as an integrator, of the following delta-sigma converter.