รายงานผลการวิจัยในโครงการวิจัยโดยใช้เงินรายได้คณะวิศวกรรมศาสตร์ ประจำปีงบประมาณ 2551

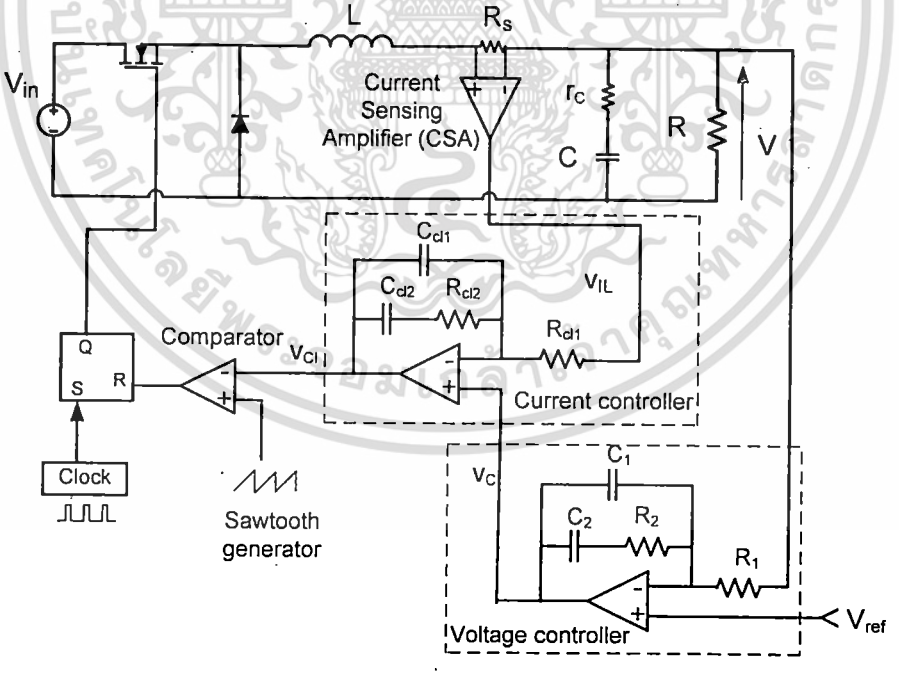
เรื่อง

เทคนิคการควบคุมแบบใหม่สำหรับแหล่งจ่ายกำลังไฟฟ้าในระบบอิเล็คทรอนิกส์ (Novel Control Technique for a Power Supply in Electrionic Systems)

ผู้รับผิดชอบโครงการวิจัย ดร. ชนินทร์ บุญลักษณานุสรณ์

ปัจจุบันระบบอิเล็คทรอนิกส์สมัยใหม่อาทิเช่น คอมพิวเตอร์ เครื่องถ่ายเอกสาร ระบบสื่อสาร เป็นต้น มีความสามารถในการทำงานได้หลายรูปแบบและมีฟังชั่นการทำงานที่หลากหลาย ซึ่ง ความสามารถดังกล่าวนี้เกิดจากความก้าวหน้าทางเทคโนโลยีของไอซีประมวลข้อมูล การทำงานของไอซีประมวลข้อมูลสมัยใหม่ต้องการแรงดันดีซีที่มีต่ำ (3.3V หรือ 2Vเป็นต้น) และกระแสที่มีการเปลี่ยนแปลงในช่วงกว้าง ในการเปลี่ยนสภาวะการทำงานของระบบจาก Idle mode ไปเป็น Active mode กระแสที่ไอซีต้องการจากแหล่งจ่ายกำลังไฟฟ้าจะเปลี่ยนจากค่าน้อยๆไปเป็นหลายสิบแอมแปร์ในระยะเวลาอันสั้น การเปลี่ยนแปลงกระแสอย่างฉับพลันนี้จะทำให้แรงดันของแหล่งจ่ายกำลังไฟฟ้าตกลงอย่างหลีกเลี่ยงไม่ได้ โดยแรงดันที่ตกลงนี้จะเกิดขึ้นเพียงชั่วขณะเพราะระบบควบคุมป้อนกลับในแหล่งจ่ายกำลังไฟฟ้าจะทำการปรับแรงดันให้กลับมายังค่าเดิมในที่สุด ภายในสภาวะดังกล่าวนี้แรงดันจะต้องไม่ตกต่ำเกินกว่าค่าที่กำหนดและไม่ควรใช้เวลานานเกินไปในการคืนตัว มิเช่นนั้นไอซีหรืออุปกรณ์อิเล็คทรอนิกส์ทั้งระบบอาจทำงานผิดพลาดได้ ขนาดของแรงดันที่ยอมให้ตกได้สูงสุด (Maximum allowable voltage drop) และระยะเวลาที่ใช้ในการคืนตัว (Settling time) จะถูกระบุอยู่ในข้อกำหนดทางไฟฟ้า (Electrical specifications) ของแหล่งจ่ายกำลังไฟฟ้าซึ่งมีค่าขึ้นอยู่กับชนิดของโหลด สำหรับระบบอิเล็คทรอนิกส์สมัยใหม่โดยส่วนใหญ่ แรงดันยอมให้เปลี่ยนแปลงได้ไม่เกิน ±1% ของค่าแรงดันปกติ นั่นคือในกรณีของแรงดัน 3.3V แรงดันจะต้องเปลี่ยนแปลงได้ไม่เกิน 33mV และระยะเวลาที่ใช้ในการคืนตัวจะอยู่ในหน่วยของไมโครวินาที

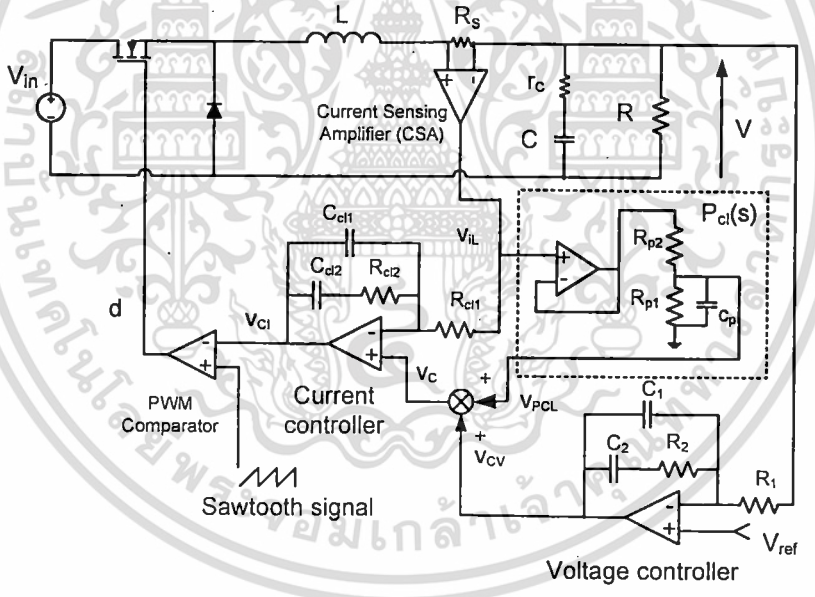
แหล่งจ่ายกำลังไฟฟ้าสำหรับระบบอิเล็คทรอนิกส์ส่วนใหญ่เป็นวงจรบัคคอนเวอร์เตอร์ที่ใช้วิธีการควบคุมแรงดันเอาพุทแบบกระแสเฉลี่ย (Average Current Mode Control, ACMC) แสดงดังรูปที่ 1



รูปที่ 1 วงจรบัคคอนเวอร์เตอร์ที่ใช้วิธีการควบคุมแรงดันเอาพุทแบบกระแสเฉลี่ย

การควบคุมแรงดันเอาพุทแบบกระแสเฉลี่ยสามารถอธิบายโดยสังเขปได้ดังนี้ แรงดันเอาพุท V ถูกป้อนกลับเพื่อมาเปรียบเทียบกับแรงดันอ้างอิง V_{ref} ค่าความแตกต่างระหว่าง V_{ref} กับ V จะถูกขยายโดยตัวควบคุมแรงดัน (Voltage controller) เพื่อสร้างสัญญาณควบคุม V_c โดย V_c นี้จะทำหน้าที่เป็นสัญญาณกระแสอ้างอิง (Reference current signal) ให้กับสัญญาณกระแสตัวเหนี่ยวนำ V_{iL} ที่ตรวจจับมาจากตัวต้านทาน R_S และวงจรขยาย CSA ค่าความแตกต่างระหว่าง V_c และ V_{iL} จะถูกขยายโดยตัวควบคุมกระแส (Current controller) สร้างสัญญาณควบคุมกระแส V_{ci} ตัวเปรียบเทียบ (Comparator) จะทำการเปรียบเทียบสัญญาณ V_{ci} กับสัญญาณฟันเลื่อย (Sawtooth signal) ให้เอาพุทเป็นสัญญาณพัลซ์สำหรับขับมอสเฟตสวิทซ์ (MOSFET switch) ในกรณีที่แรงดันเอาพุทลดลง V_c และ V_{ci} จะมีค่าเพิ่มขึ้น ความกว้างพัลซ์ของสัญญาณขับมอสเฟตสวิทซ์ก็จะเพิ่มขึ้นทำให้กระแสตัวเหนี่ยวนำ L มีค่าเพิ่มขึ้นเพื่อไปทำให้แรงดันเอาพุทเพิ่มขึ้น ในกรณีที่แรงดันเอาพุทเพิ่มขึ้น V_c และ V_{ci} จะมีค่าลดลง ความกว้างพัลซ์ของสัญญาณขับนกรณีที่แรงดันเอาพุทลดลง V_c และ V_{ci} จะมีค่าเพิ่มขึ้น ความกว้างพัลซ์ของสัญญาณขับก็จะลดลงทำให้กระแสตัวเหนี่ยวนำ L มีค่าลดลงเพื่อไปทำให้แรงดันเอาพุทลดลง จากการทำงานดังกล่าวแรงดันเอาพุทจะสามารถถูกรักษาให้มีค่าคงที่ได้

งานวิจัยนี้นำเสนอเทคนิคการควบคุมแรงดันเอาพุทแบบกระแสเฉลี่ยแบบใหม่ที่มีการเพิ่มส่วนการควบคุมป้อนไปข้างหน้า ($P_{cf}(s)$) ให้กลับการควบคุมแรงดันเอาพุทแบบกระแสเฉลี่ยแบบเดิมดังแสดงในรูปที่ 2



รูปที่ 1 วงจรบัคคอนเวอร์เตอร์ที่ใช้วิธีการควบคุมแรงดันเอาพุทกระแสเฉลี่ยแบบใหม่ที่มีการเพิ่มส่วนการควบคุมป้อนไปข้างหน้า

เนื้อหาที่นำเสนอในรายงานฉบับนี้จะเริ่มจากการอธิบายหลักการทำงานของเทคนิคการควบคุมแบบใหม่นี้ จากนั้นจะกล่าวถึงการแบบจำลอง การออกแบบระบบ และในตอนท้ายจะนำเสนอผลการทดสอบสมรรถนะการควบคุมโดยใช้วงจรต้นแบบที่ได้สร้างขึ้น

I. INTRODUCTION

Average Current Mode Control (ACMC) is a control technique commonly used in modern DC-DC converters to regulate the output voltage. The control structure comprises an output voltage and inductor current loops. In the current loop, a current amplifier is employed to force the inductor current to closely track the reference current, instead of directly comparing the two quantities using a comparator as in Peak Current Mode Control (PCMC). Because of this, ACMC has a better noise immunity, higher current loop gain, and no stability problem when the duty cycle is above 0.5. These good features have contributed to its widespread usage in today's DC-DC converters. In [1-2], modeling and control design of ACMC have been described. The modeling yielded a small-signal model, from which the transfer functions useful for control loop design can be derived. Based on these transfer functions, the controllers in the voltage and current loops are designed so that the converter exhibits the desired output performance, i.e. having good output regulation and fast dynamic response. However, even with the well designed controllers, the converter performance still may not meet the stringent requirements of modern electronic loads, which demands the tightly regulated voltage and wide current variations from the current variations from the converter. To enhance the performance of the conventional ACMC, a novel three-controller ACMC has recently been proposed [3]. The authors modified the voltage loop to include an auxiliary controller. The transfer function of the auxiliary controller was carefully selected and designed to increase the system robustness against variations in the input voltage, load current and *L-C* output filter. It was demonstrated experimentally that the three controller technique yields a faster output voltage response than the conventional ACMC. However, to implement the three-controller scheme, many additional circuit components are required. The increased cost and circuit complexity hence may not justify the practicality of the three-controller technique. This paper presents a novel Current Feedforward Average Current Mode Control (CFACMC) technique to improve output dynamic performance of DC-DC converters. The proposed technique makes use of the inductor current information readily available in the ACMC scheme as a feedforward signal to strengthen the corrective action of the output voltage loop. If properly designed, this current feedforward loop can lead to significant improvement in the output voltage

dynamic response of the converter. The feedforward path consists only of a low-pass filter circuit. Hence, the implementation of CFACMC is simple and requires just a minor modification to the standard ACMC circuit.

II. PRINCIPLE OF CFACMC

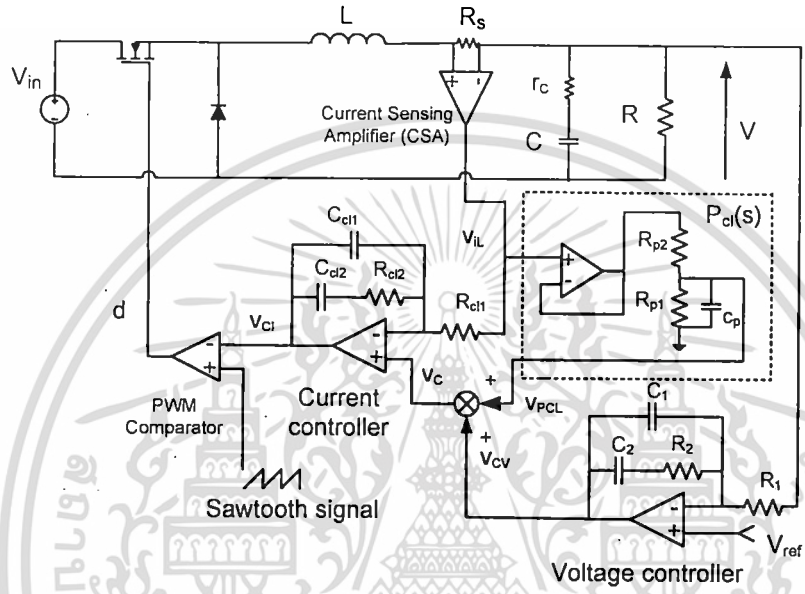


Fig. 1. Buck converter with CFACMC

A buck converter with CFACMC is shown in Fig. 1. The circuit block, $P_{cl}(s)$, consisting of a voltage buffer and low-pass filter (R_{p1}, R_{p2}, and C_p), is added into the conventional ACMC circuit. The inductor current is sensed by a resistor R_s and amplified by a current sensing amplifier (CSA) to give the sensed current signal v_{iL}. In the conventional ACMC, v_{iL} only serve as a feedback variable to the current controller. But, in the CFACMC proposed here, v_{iL} is also fed forward through $P_{cl}(s)$ to sum with the output signal from a voltage controller, v_{cv}, to form the control signal, v_c. The difference between v_c, which represents the desired current, and v_{iL}, which represents the actual inductor current, is amplified by the current controller. The resulting current error signal, v_{ci}, is then compared with the sawtooth signal to generate the duty cycle signal, d, to drive the MOSFET.

The proposed CFACMC can improve the output voltage response of the converter as follows. Assume that the output voltage drop is occurred due to a step load change, the

voltage controller will respond by increasing v_{cv}. The increase in v_{cv} will sequentially trigger the increase in v_c, v_{ci}, d, i_L, v_{iL}, and v_{PCL}. With the contribution from v_{PCL}, v_c, which is equal to $v_{cv} + V_{PCL}$, will increase more than that in the conventional ACMC, which relies on v_{cv} to act alone. In effect, CFACMC produces the stronger corrective action than the conventional ACMC. This paves the way to further improve the output voltage dynamic response of the converter. However, to achieve the improved dynamic performance, the feedforward signal, v_{PCL}, must be appropriate; otherwise a poor output voltage response or even instability can result. Hence, the gain and cut-off frequency of $P_{cl}(s)$ must be chosen such that the improved dynamic response of the converter is attained, while their impacts on system stability are kept to a minimum. .

III. Modeling of Buck Converter with CFACMC

A. Modeling of Power Stage

A buck converter's power stage is shown in Fig. 2, where r_c is the equivalent series resistance (ESR) of the capacitor C, R is the standing load, and the current source i_z represents the load current. In Continuous Conduction Mode (CCM), the converter exhibits the two circuit topologies within one switching period as shown in Fig. 3.

When the MOSFET is turned on (Fig. 3(a)), the state-space equation of the converter is

$$\begin{cases} \begin{bmatrix} i_L \\ v_c \end{bmatrix} = \begin{bmatrix} \dfrac{-R.r_c}{L(R+r_c)} & \dfrac{-R}{L(R+r_c)} \\ \dfrac{R}{C(R+r_c)} & \dfrac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} & \dfrac{R.r_c}{L(R+r_c)} \\ 0 & \dfrac{-R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_z \end{bmatrix} \\ v = \begin{bmatrix} \dfrac{R.r_c}{R+r_c} & \dfrac{R}{R+r_c} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & \dfrac{-R.r_c}{R+r_c} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_z \end{bmatrix} \end{cases} \quad (1)$$

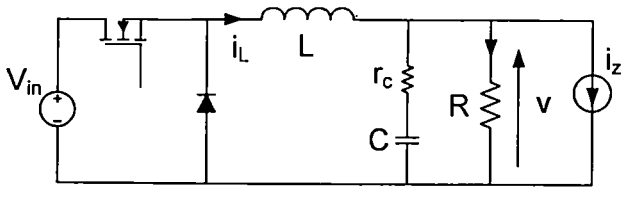
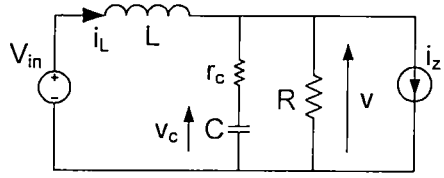
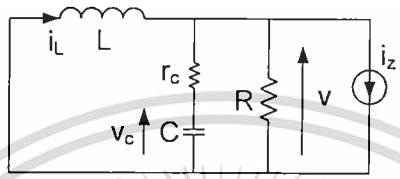


Fig. 2. DC-DC Buck Converter



(a) MOSFET on



(b) MOSFET off

Fig. 3. Buck converter circuit when (a) MOSFET turns on (b) MOSFET turns off

When the MOSFET is turned off (Fig. 3(b)), the state-space equation of the converter is

$$\begin{cases} \begin{bmatrix} i_L \\ v_c \end{bmatrix} = \begin{bmatrix} \dfrac{-R.r_c}{L(R+r_c)} & \dfrac{-R}{L(R+r_c)} \\ \dfrac{R}{C(R+r_c)} & \dfrac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & \dfrac{R.r_c}{L(R+r_c)} \\ 0 & \dfrac{-R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_z \end{bmatrix} \\ v = \begin{bmatrix} \dfrac{R.r_c}{R+r_c} & \dfrac{R}{R+r_c} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & \dfrac{-R.r_c}{R+r_c} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_z \end{bmatrix} \end{cases} \quad (2)$$

Equations (1) and (2) are weighed average by d and 1-d respectively. The result is state-space averaged equations:

$$\begin{cases} \begin{bmatrix} i_L \\ v_c \end{bmatrix} = \begin{bmatrix} \dfrac{-R.r_c}{L(R+r_c)} & \dfrac{-R}{L(R+r_c)} \\ \dfrac{R}{C(R+r_c)} & \dfrac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \dfrac{d}{L} & \dfrac{R.r_c}{L(R+r_c)} \\ 0 & \dfrac{-R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_z \end{bmatrix} \\ v = \begin{bmatrix} \dfrac{R.r_c}{R+r_c} & \dfrac{R}{R+r_c} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & \dfrac{-R.r_c}{R+r_c} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_z \end{bmatrix} \end{cases} \quad (3)$$

Equation (3) is a nonlinear equation because it contains the product dv_{in}, where d and v_{in} are both independent variables. Small-signal perturbation of (3) yields the small-signal state-space equation in (4).

$$\begin{cases} \begin{bmatrix} \hat{i}_L \\ \hat{v}_c \end{bmatrix} = \begin{bmatrix} \dfrac{-R.r_c}{L(R+r_c)} & \dfrac{-R}{L(R+r_c)} \\ \dfrac{R}{C(R+r_c)} & \dfrac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_c \end{bmatrix} + \begin{bmatrix} \dfrac{D}{L} & \dfrac{R.r_c}{L(R+r_c)} & \dfrac{V_{in}}{L} \\ 0 & \dfrac{-R}{C(R+r_c)} & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_z \\ \hat{d} \end{bmatrix} \\ \hat{v} = \begin{bmatrix} \dfrac{R.r_c}{R+r_c} & \dfrac{R}{R+r_c} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_c \end{bmatrix} + \begin{bmatrix} 0 & \dfrac{-R.r_c}{R+r_c} & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_z \\ \hat{d} \end{bmatrix} \end{cases} \tag{4}$$

By applying the Laplace transform to (4), transfer functions of the converter can be found in a matrix form

$$\begin{bmatrix} \hat{i}_L(s) \\ \hat{v}(s) \end{bmatrix} = \begin{bmatrix} G_{vi}(s) & G_{zi}(s) & G_{di}(s) \\ G_{vv}(s) & G_{zv}(s) & G_{dv}(s) \end{bmatrix} \begin{bmatrix} \hat{v}_{in}(s) \\ \hat{i}_z(s) \\ \hat{d}(s) \end{bmatrix} \tag{5}$$

Since only the duty cycle-to-inductor current and the duty cycle-to-output voltage transfer functions, $G_{di}(s)$ and $G_{dv}(s)$, are relevant in the control design, they have been derived and given in (6) and (7) respectively.

$$G_{di}(s) = \frac{\dfrac{V_{in}}{LCR}\left(1+s(R+r_c)C\right)}{s^2 + s\left(\dfrac{1}{RC}+\dfrac{r_c}{L}\right)+\dfrac{1}{LC}} \tag{6}$$

$$G_{dv}(s) = \frac{\dfrac{V_{in}}{LC}\left(1+sr_cC\right)}{s^2 + s\left(\dfrac{1}{RC}+\dfrac{r_c}{L}\right)+\dfrac{1}{LC}} \tag{7}$$

B. Modeling of Control Stage

Current Controller

As shown in Fig. 1, a function of the current controller is to force the inductor current to track its reference value, v_c. From Fig. 1, the current controller output, v_{ci}, is related to the control signal, v_c, and the sensed inductor current, v_{iL}, as:

$$v_{ci} = v_c(1+G_{cl}(s)) - G_{cl}(s)v_{iL} \tag{8}$$

where $G_{cl}(s) = \frac{Z_{cl2}}{Z_{cl1}}$, $z_{cl2} = \frac{1+sR_{cl2}C_{cl2}}{s(sR_{cl2}C_{cl2}C_{cl1}+C_{cl2}+C_{cl1})}$, and $z_{cl1} = R_{cl1}$. The signal v_{iL} is obtained from the Current Sensing Amplifier (CSA) which amplifies the inductor current sensed across R_S. If A_{CL} is the gain of the CSA, then v_{iL} is expressed by

$$v_{iL} = A_{CL}R_S i_L \tag{9}$$

By introducing the perturbed signals $v_{ci} = V_{ci} + \hat{v}_{ci}$, $v_c = V_c + \hat{v}_c$, and $v_{iL} = V_{iL} + \hat{v}_{iL}$ into (8) and collecting only the small signal terms, the small-signal model of the current controller is obtained

$$\hat{v}_{ci} = \hat{v}_c(1+G_{cl}(s)) - G_{cl}(s)\hat{v}_{iL} \tag{10}$$

Voltage Controller

A function of the voltage controller is to force the output voltage to track its reference value, V_{ref}. From Fig. 1, the control signal, v_c, is related to the reference voltage, V_{ref}, and the output voltage, v, as:

$$v_c = V_{ref}(1+G_c(s)) - G_c(s)v \tag{11}$$

where $G_c(s)=\frac{Z_{c2}}{Z_{c1}}$, $z_{c2}=\frac{1+sR_{c2}C_{c2}}{s(sR_{c2}C_{c2}C_{c1}+C_{c2}+C_{c1})}$, and $z_{c1}=R_{c1}$. By introducing the perturbed signal $v=V+\hat{v}$, $v_c=V_c+\hat{v}_c$ and V_{ref} being constant into (11) and collecting only the small signal terms, the small-signal model of the voltage controller is obtained.

$$\hat{v}_c=-\frac{z_{c2}}{z_{c1}}\hat{v}=-G_c(s)\hat{v} \tag{12}$$

Feedforward Block $P_{cl}(s)$

$P_{cl}(s)$ in Fig. 1 consists of the unity gain voltage buffer followed by the first-order low pass filter. Thus, the transfer function of $P_{cl}(s)$ is given by:

$$P_{cl}(s)=\frac{\hat{v}_{pcl}}{\hat{v}_{iL}}=\frac{k_p}{1+s/\omega_p} \tag{13}$$

where $K_p=\frac{R_{p1}}{R_{p1}+R_{p2}}$ and $\omega_p=\frac{R_{p1}+R_{p2}}{R_{p1}R_{p2}C_p}$.

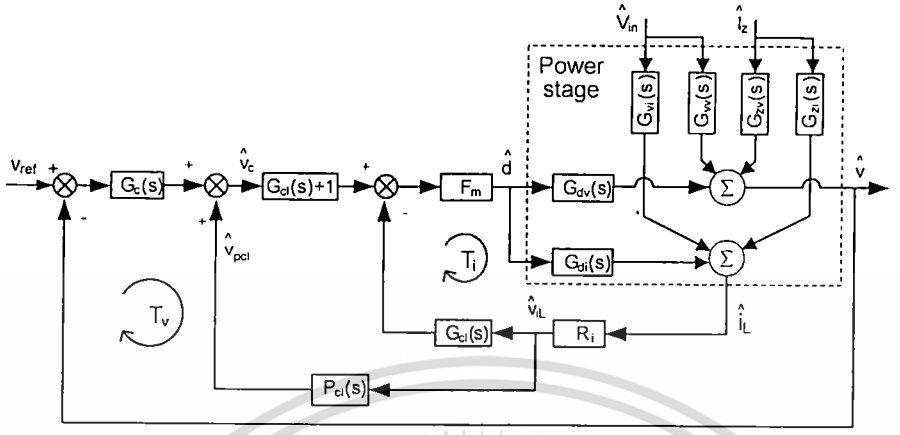
PWM Modulator

The transfer function of the PWM modulator is given by:

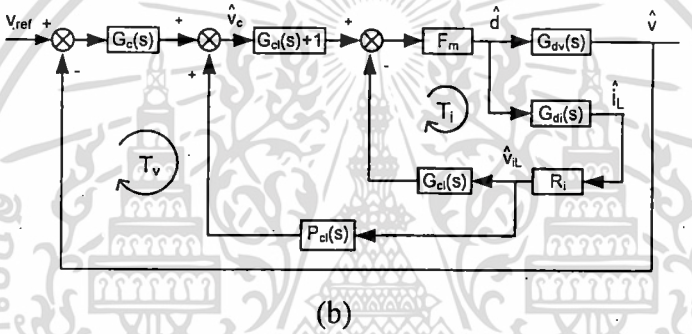
$$\frac{\hat{d}}{\hat{V}_{ci}}=F_m \tag{14}$$

where $F_m=\frac{1}{V_p}$ and V_p is the peak-to-peak sawtooth voltage.

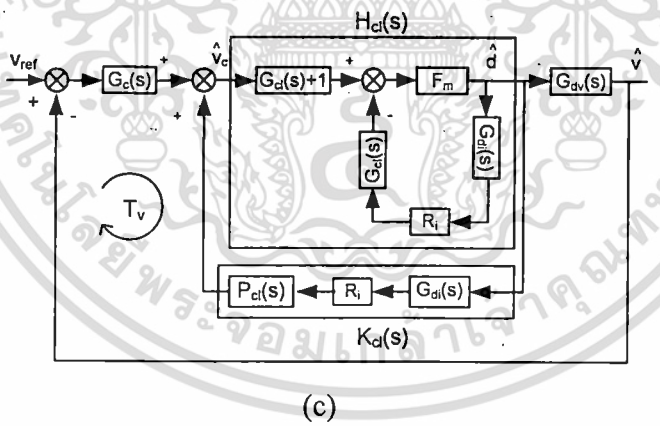
C. *Complete Small-signal Model of Buck Converter with CFACMC*



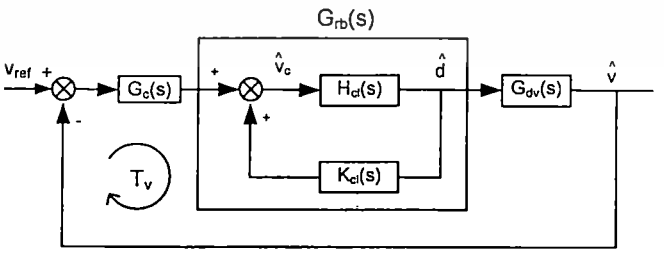
(a)



(b)



(c)



(d)

Fig. 4 Small-signal model of CFACMC

A small-signal model of the buck converter with CFACMC is illustrated in Fig. 4(a). The power stage is represented by the six transfer functions as given in (5), while the CFACMC control stage is formed by combining (10), (12), (13), and (14). Since $\hat{v}_{in}$ and $\hat{i}_z$ are independent input variables, they can be assumed to be zero for the control design purposes. The model in Fig. 4(a) can be simplified into that in Fig. 4(b). Note that if $P_{cl}(s)$ is zero, the model will be reduced to that of the conventional ACMC. This is logical because CFACMC is realised by only adding the feedforward block, $P_{cl}(s)$, into the existing ACMC-based converter. Hence, design of the voltage and current controllers in CFACMC can be carried out in the same way as in the conventional ACMC. The task in designing CFACMC, therefore, involves only selection of the gain and cut-off frequency of $P_{cl}(s)$ in (13).

For ease of analysis, the model in Fig. 4(b) is further manipulated into Figs. 4(c) and 4(d) respectively, where $H_{cl}(s)$, $K_{cl}(s)$ and $G_{rb}(s)$ are given by:

$$H_{cl}(s)=\frac{F_m(G_{cl}(s)+1)}{1+F_m R_i G_{cl}(s) G_{di}(s)} \tag{15}$$

$$K_{cl}(s)=R_i G_{di}(s) P_{cl}(s) \tag{16}$$

$$G_{rb}(s)=\frac{H_{cl}(s)}{1-K_{cl}(s)H_{cl}(s)} \tag{17}$$

In the conventional ACMC, $P_{cl}(s)$ is equal to zero, so is $K_{cl}(s)$, and $G_{rb}(s)$ equal to $H_{cl}(s)$. Hence, it can be seen from (17) that CFACMC has altered the transfer function of the conventional ACMC by a factor of $1/(1- K_{cl}(s)H_{cl}(s))$. From (16), $K_{cl}(s)$ is directly proportional to $P_{cl}(s)$. At low frequencies, $P_{cl}(s)$ should be high so that the product $K_{cl}(s)H_{cl}(s)$ in (17) approaches one and therefore $G_{rb}(s)$ as well as the voltage loop gain, $G_c(s)G_{rb}(s)G_{dv}(s)$, in Fig. 4(d) are increased. The increased voltage loop gain will lead to the faster output voltage dynamic response of the converter. Above the crossover frequency of the voltage loop, $P_{cl}(s)$ should be low so that the product $K_{cl}(s)H_{cl}(s)$ in (17) approaches zero and therefore $G_{rb}(s)$ is converged to $H_{cl}(s)$ to preserve the characteristic

of ACMC. From the preceding observation, it is concluded that the cut-off frequency of $P_{cl}(s)$ should be selected at the crossover frequency of the voltage loop gain of the conventional ACMC. In this way, $P_{cl}(s)$ will serve only to enhance the output voltage dynamic response, while having a minimum impact on the stability margin specified earlier during ACMC design stage.

At DC frequency (s = 0), $H_{cl}(s)$, $K_{cl}(s)$ and $G_{rb}(s)$ in (15) to (17) can be expressed as:

$$H_{cl}(0)=\frac{R}{V_{in}R_i} \tag{16}$$

$$K_{cl}(0)=k_p\frac{V_{in}R_i}{R} \tag{17}$$

$$G_{rb}(0)=\frac{H_{cl}(0)}{1-K_{cl}(0)H_{cl}(0)} \tag{18}$$

Substitution of (16) and (17) into (18) gives

$$G_{rb}(0)=\frac{H_{cl}(0)}{1-K_p} \tag{19}$$

It can be seen from (19) that $G_{rb}(0)$ is proportional to $H_{cl}(0)$ which, as seen in (16), is proportional to R and inversely proportional to V_{in}. In modern applications, the converter is normally located close to its electronic load and receives a constant input voltage from the central power supply unit. Therefore, V_{in} is assumed to be constant in this analysis. As a result, $G_{rb}(0)$ is only proportional to R and equation (19) can be rewritten as

$$G_{rb}(0)=\frac{kR}{1-K_p} \tag{20}$$

where $k = 1/V_{in}R_i$ is a constant of proportionality. Fig. 6 shows the plot of $G_{rb(0)}$ in (20) as a function of k_p for the two load resistor values, R_{max} and R_{min}. The curve is hyperbolic and the gain k_p can vary between zero and one. It can be seen that when the load current is changed from minimum to maximum, i.e. the load resistor is changed from R_{max} to R_{min}, $G_{rb(0)}$ is decreased. To prevent the effect of the load change on $G_{rb(0)}$, k_p has to be increased by the amount of k_1 as shown in Fig. 5. That is

$$\frac{kR_{min}}{1-k_1} = kR_{max} \tag{21}$$

Rearranging (21), the gain of the low-pass filter, k_p, is determined:

$$k_p = k_1 = \frac{R_{max} - R_{min}}{R_{max}} \tag{22}$$

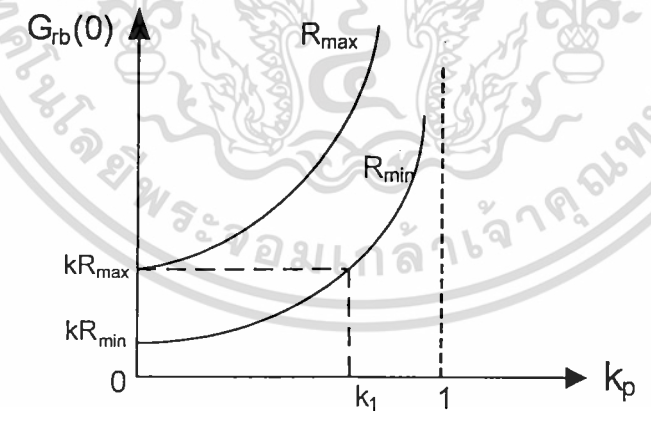


Fig. 5. Graph of $G_{rb}(0)$ as k_p varies

IV. PROTOTYPE CIRCUIT DESIGN

Circuit parameters of a buck converter are listed in Table I.

TABLE I

PARAMETERS OF PROTOTYPE BUCK CONVERTER

V_{in}	V	L	C	r_C	R
5V	2V	45.2H	1230uF	0.015Ω	0.4-2Ω

The peak-to-peak voltage of the sawtooth signal is V_p=1.8V. The value of a sensing resistor is R_S=0.01Ω and the current sensing amplifier's gain is A_{cl}=7.5. The switching frequency is f_s=100 kHz. From the parameters listed in Table I, the transfer functions in (6), (7), and (14) can be calculated:

$$G_{di}(s)=4.5\times10^{7}\frac{2.5\times10^{-3}s+1}{s^{2}+738.6s+1.8\times10^{7}} \tag{23}$$

$$G_{dv}(s)=8.99\times10^{7}\frac{1.84\times10^{-5}s+1}{s^{2}+738.6s+1.8\times10^{7}} \tag{24}$$

$$F_m=1/V_p=0.55 \tag{25}$$

The current controller and voltage controller are designed in the same way as in the conventional ACMC. For the current controller design, the crossover frequency of the current loop is selected at 10kHz. The first pole of $G_{cl}(s)$ is at the origin, the zero is placed at w_{clz} = 4.482×10^{3}rad/sec, and the second pole is placed at one-third of the switching frequency or w_{clp}= 188×10^{3}rad/sec. The design yields C_{cl1}=500pF, C_{cl2}=22nF R_{cl1}=560Ω, and R_{cl2}=10kΩ. Substitution of these component values into (10) results in

$$G_{cl}(s)=\frac{7.93\times10^{4}}{s}\frac{1+2.2\times10^{-4}s}{1+4.89\times10^{-6}s} \tag{26}$$

For the voltage controller design, the crossover frequency of the voltage controller is selected at 5kHz. The first pole of $G_c(s)$ is at the origin, the zero is place at $w_{cz}=4.3\times10^{3}$rad/sec, and the second pole is placed at one-third of the switching frequency or $w_{cp}=188\times10^{3}$rad/sec. The design yields C_1=500pF, C_2=22nF, R_1=3.9kΩ, and R_2=10kΩ. Substitution of these component values into (12) results in

$$G_{c}(s)=\frac{1.12\times10^{4}}{s}\frac{1+2.2\times10^{-4}s}{1+4.89\times10^{-6}s} \tag{27}$$

As shown in the Table I, the maximum and minimum load resistances are 2Ω and 0.4Ω, respectively. From (22), k_p can be calculated:

$$k_p=0.8 \tag{28}$$

The cut-off frequency of $P_{cl}(s)$ is selected to be equal to the crossover frequency of the voltage loop gain of the conventional ACMC, which was set at 5kHz. Thus, the cut-off frequency of $P_{cl}(s)$ is $w_p=31.4\times10^{3}$rad/s. From the values of k_p and w_p, the low-pass filter's component are calculated, yielding R_{p1}=4kΩ, R_{p2}=1kΩ, and C_p=38nF. Substitution of these component values into (13) results in

$$P_{cl}(s)=\frac{0.8}{1+3.04\times10^{-5}s} \tag{29}$$

The open loop transfer function of the CFACMC in Fig. 4(d) is given by:

$$T_v(s) = G_c(s) G_{rb}(s) G_{dv}(s) \tag{30}$$

Bode plot of (20) is shown by the solid lines in Fig. 6.

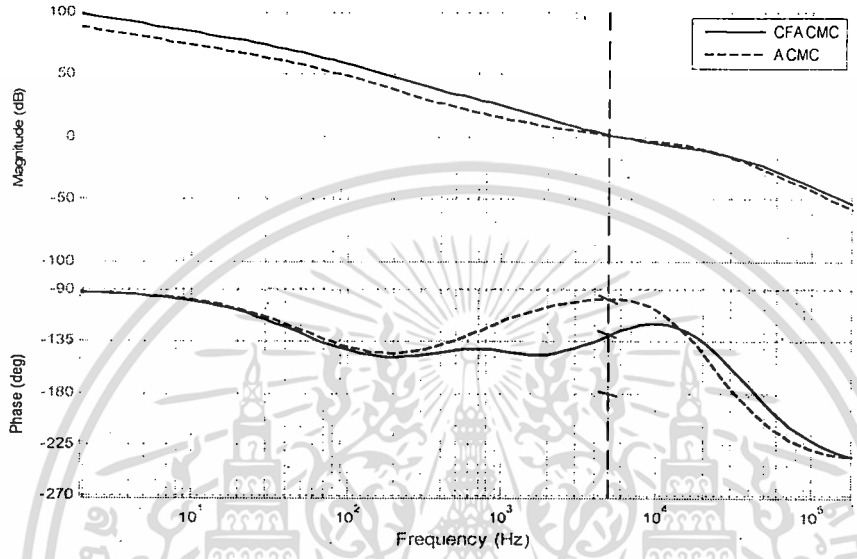


Fig. 6. Open loop frequency responses of CFACMC versus ACMC

In Fig 4(c), if $P_{cl}(s) = 0$, the model will become that of conventional ACMC, whose open loop transfer function is given by:

$$T_v(s) = G_c(s) H_{cl}(s) G_{dv}(s) \tag{31}$$

Bode plot of (31) is also shown in Fig. 6 by the dashed lines. It can be seen that the loop gain of CFACMC is greater than the loop gain of the conventional ACMC up to the crossover frequency. Above the crossover frequency, the two plots are converged. This result confirms that the designed $P_{cl}(s)$ only serves to improve the dynamic response of the converter, while keeping its impact on system stability at the minimum.

V. RESULTS

The prototype converter circuit was built in order to verify the performance of CFACMC against the conventional ACMC. In the prototype circuit board (Fig. 11), selection between the conventional ACMC (i.e. $P_{cf}(s) = 0$) and CFACMC was made by a jumper. The converter was subjected to a step load current change and an output voltage response of the converter recorded. Figs. 7 and 8 show the simulated and measured output voltage responses of the converter with the conventional ACMC and CFACMC respectively. In Fig. 7, the maximum voltage drop/raise is about 65mV and the settling time is about 750μs. In Fig. 8, they are about 60mV and 200μs respectively. It can be seen that while the maximum voltage drop/raise given by the two control methods is roughly the same, the settling time given by CFACMC is faster than the conventional ACMC by 450μs. This represents a significant improvement in the dynamic response time of the converter. Fig. 9 compares the results in Fig. 7 and 8 on the same scale, where the improvement yielded by CFACMC is evident.

Moreover, in Figs. 7 to 9, the simulated results are seen to be in good agreement with their experimental counterparts. These simulated results were produced by the SIMULINK models shown in Fig. 10. Good correspondence between the simulated and experimental results indicates the accuracy and validity of the models in predicting the converter's dynamic response.

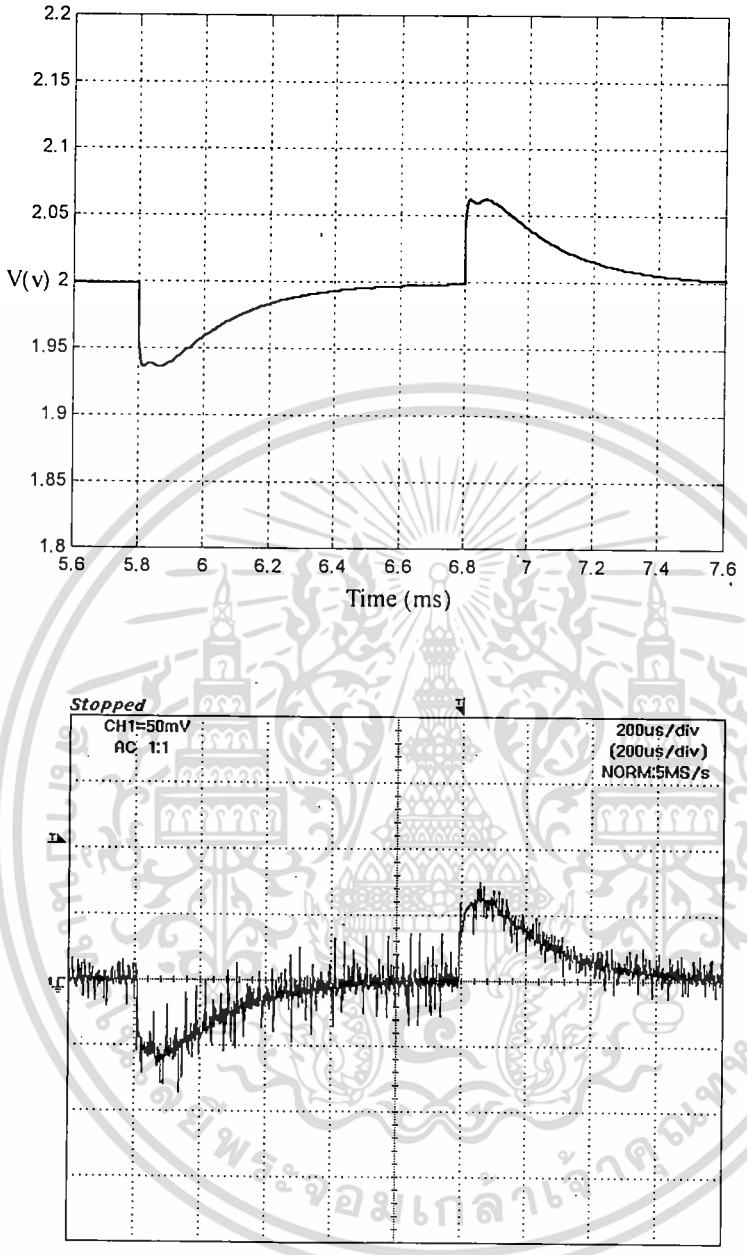


Fig. 7. Output voltage response of the buck converter with ACMC as the load current is stepped back and forth between 1A and 4A.

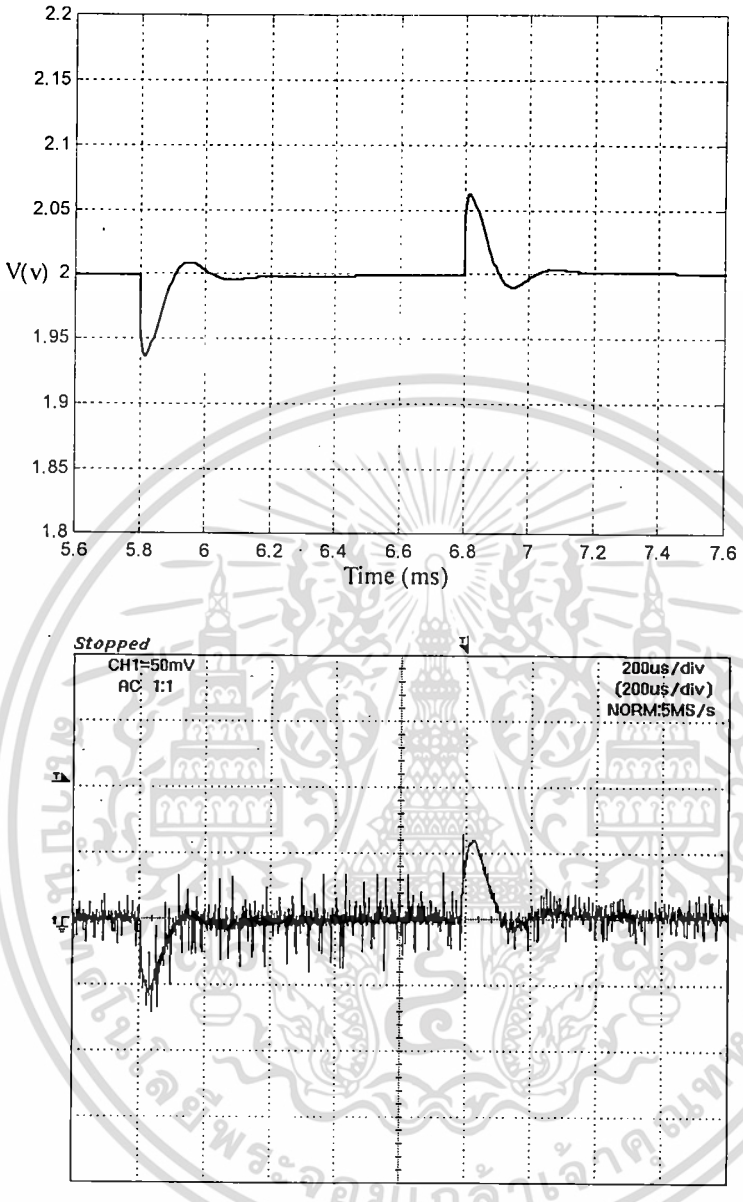
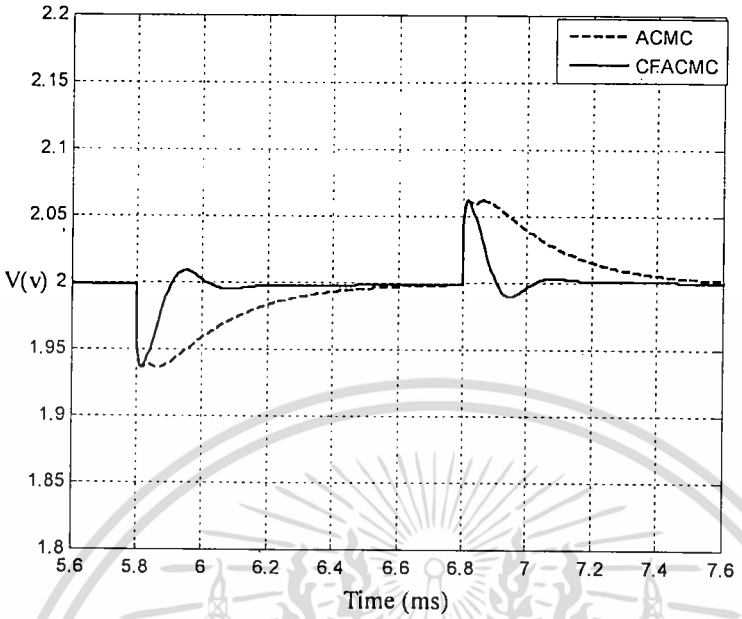


Fig. 8. Output voltage response of the buck converter with CFACMC as the load current is stepped back and forth between 1A and 4A.



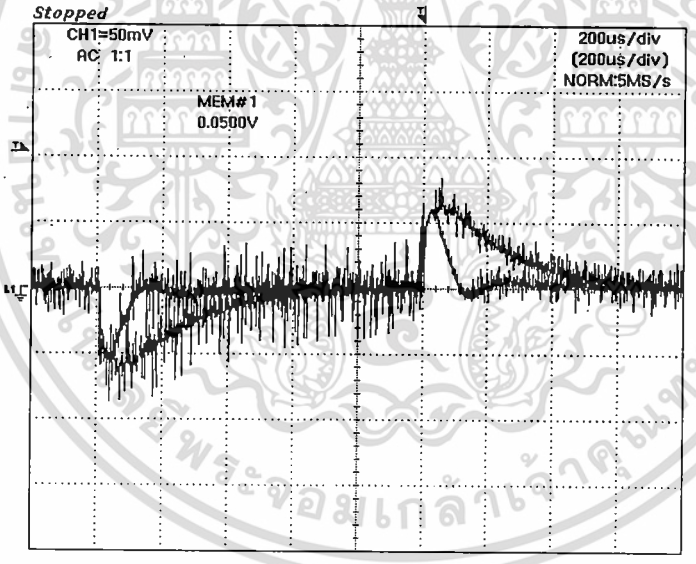


Fig. 9. Comparison between output voltage responses of buck converter with conventional ACMC and CFACMC

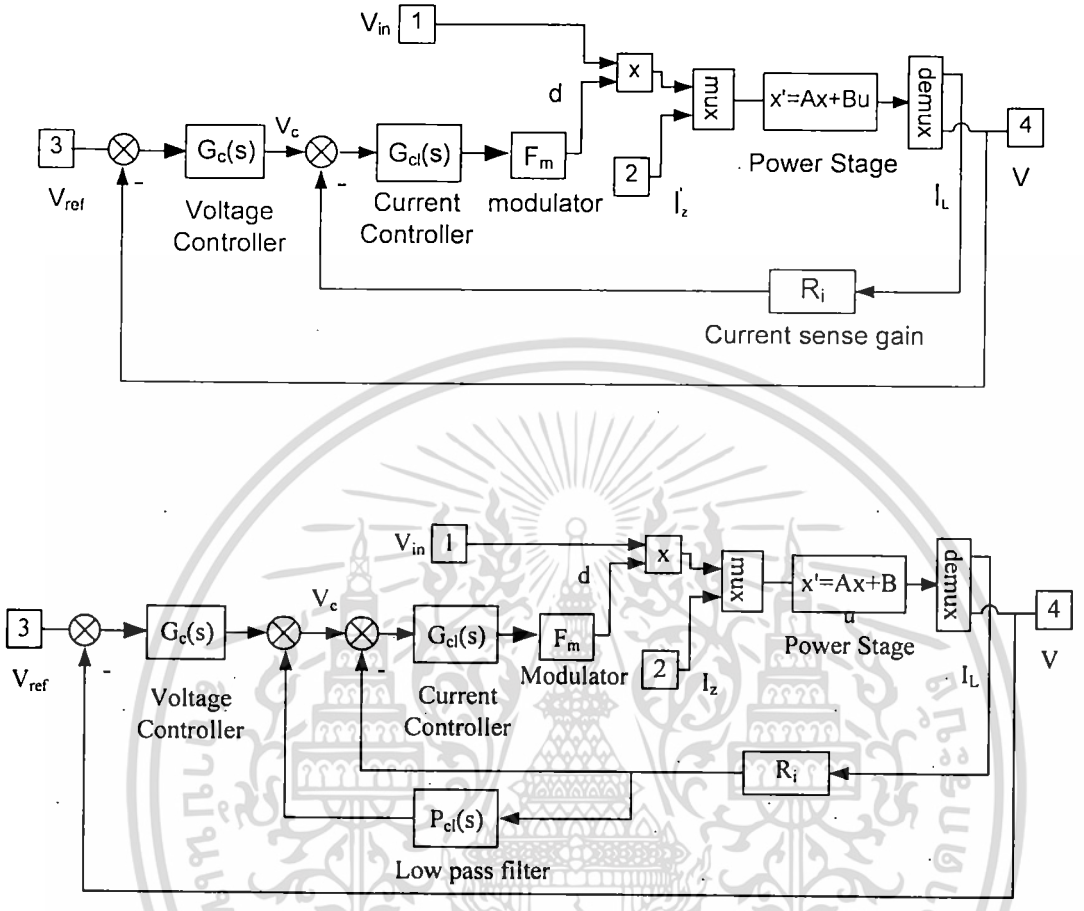


Fig. 10. Simulink model of buck converter with (a) ACMC (b) CFACMC

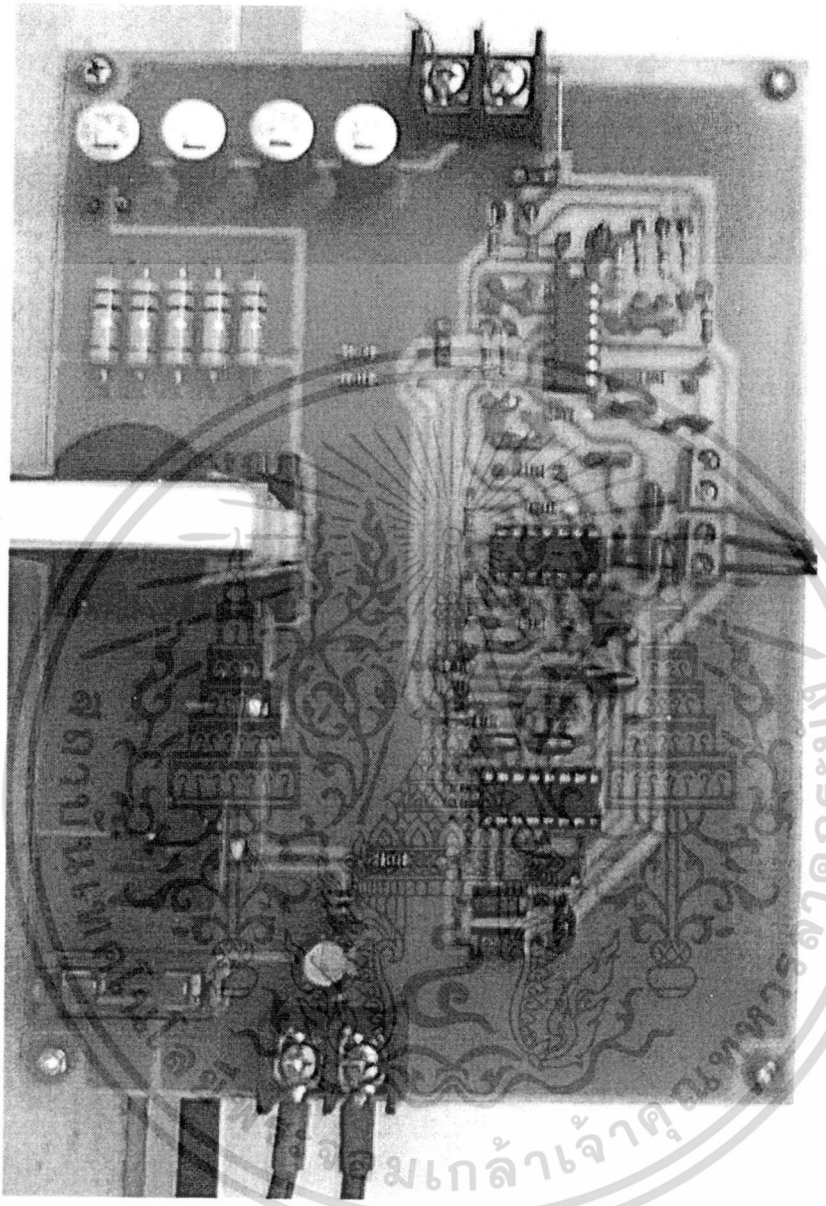


Fig. 11. Protoype buck converter circuit board (selection of ACMC or CFACMC are done by a jumper on the board) .

VI. CONCLUSION

The novel Current Feedforward Average Current Mode (CFACMC) technique to improve output dynamic performance of DC-DC converters has been proposed in this paper. It is based on feedforward of the sensed inductor current, through the low-pass filter circuit, $P_{cf}(s)$, to sum with the output signal from the voltage controller to produce the control signal. The feedforward signal helps strengthen the corrective action of the voltage loop, hence making it possible for the converter's dynamic response to be further improved from the conventional ACMC. To achieve the improved output dynamic performance, the gain and cut-off frequency of $P_{cf}(s)$ must be appropriately chosen. The equation for selecting the low-pass filter gain was derived in (22) and the low pass filter's cut-off frequency must be set equal to the crossover frequency of the voltage loop of the conventional ACMC. The capability of CFACMC in enhancing the converter's output dynamic performance was confirmed by the simulated and experimental results. Due to its simplicity and capability to significantly improve the converter's output dynamic response, the proposed CFACMC technique has a good potential for practical usage.

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PUBLICATION

[1] P. Chrin, C. Bunlaksananusorn, "Novel Current Feedforward Average Current Mode Control Technique to Improve Output Dynamic Performance of DC-DC Converters", Proceeding 7th International Conference on Power Electronics and Drive Systems, pp. 1416-1421, Bangkok, Thailand.

Novel Current Feedforward Average Current Mode Control Technique to Improve Output Dynamic Performance of DC-DC Converters

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Abstract--This paper proposes a novel Current Feedforward Average Current Mode Control (CFACMC) technique to improve output dynamic performance of DC-DC converters. In this new control scheme, besides its usual role as a feedback variable to a current controller, the sensed inductor current is fed forward, through a low-pass filter circuit, to sum with an output signal from a voltage controller to form the control signal. In the paper, the operating principle of CFACMC and its small signal model are described. From the small-signal model, the expression for selecting the gain of the low-pass filter to yield the improved output voltage response is derived. Both simulated and experimental results are provided to show that significant improvement in output dynamic response is achieved with CFACMC.

Index Terms—Average current mode control, DC-DC converters.

I. Introduction

Average Current Mode Control (ACMC) is a control technique commonly used in modern DC-DC to regulate the output voltage. The control structure comprises of an output voltage and inductor current loops. In ACMC, a current amplifier is employed in the current loop to force the inductor current to closely track the reference current, instead of directly comparing the two quantities using a comparator as in Peak Current Mode Control (PCMC). Because of this, ACMC has a better noise immunity, higher current loop gain, no stability problem when the duty cycle is above 0.5. These appealing features have contributed to its popularity in today's DC-DC converters. In [1-3], operating principle, modeling and control design of ACMC have been described. The small-signal model of ACMC [2,3], together with the small-signal model of the converter's power stage [4], form a complete converter system, from which transfer functions for the control design can be derived. Based on these transfer functions, the controllers in the voltage and current loops are designed so that the converter exhibits the desired output performance, i.e. having good output regulation and fast dynamic response. However, even with the well designed controllers, the converter's performance still may not meet the stringent requirements of modern electronic loads, which demands the tightly regulated voltage and wide current variations from the converter. To enhance the performance of the conventional ACMC, the novel three-controller ACMC has recently been proposed [5]. The authors modified the voltage loop to include an auxiliary controller. The transfer function of the auxiliary controller was carefully selected and designed to increase the system robustness against variations in the input voltage, load current and *L-C* output filter. It was demonstrated experimentally that the three controller technique yields a faster output voltage response than the conventional ACMC.

This paper presents a novel Current Feedforward Average Current Mode (CFACMC) technique to improve output dynamic performance of DC-DC converters. The sensed inductor current signal, which is readily available in the conventional ACMC, is used as a feedforward signal to enhance a corrective action of the voltage loop. The feedforward path consists only of a low-pass filter circuit. Hence, the implementation of CFACMC is simple, which requires just a minor modification to the standard ACMC circuit.

II. Current Feedforward Average Current Mode Control

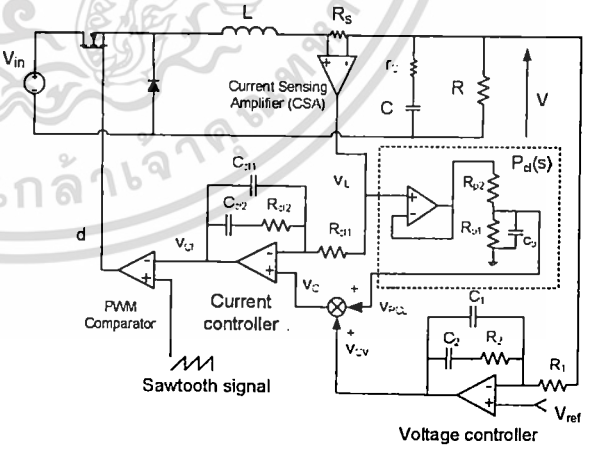

Fig. 1. Buck converter with CFACMC

A buck converter with CFACMC is shown in Fig. 1. To implement CFACMC, a low-pass filter circuit, $P_{cl}(s)$, is added to the conventional ACMC circuit to provide a feedforward path to the voltage loop. The inductor current is sensed by a resistor R_S and amplified by a current sensing amplifier (CSA) to give the sensed

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current signal V_{iL}. Besides being fed back to a current controller, V_{iL} is also fed forward through $P_{cl}(s)$ to sum with the output signal from a voltage controller, V_{CV}, to form the control signal, V_C. The difference between V_C, which represents the desired current, and V_{iL}, which represents the actual inductor current, is amplified by the current controller. The resulting current error signal, V_{CI}, is then compared with the sawtooth voltage, V_p, to generate the duty cycle signal, d, to drive the MOSFET.

The proposed CFACMC can improve the output voltage response of the converter as follows. Assume that the output voltage drop is occurred due to a step load change, the voltage controller will respond by increasing V_{CV}. The increase in V_{CV} will trigger the increase in V_C, V_{CI}, d, i_L, V_{iL}, and V_{PCL}, respectively. With the contribution from V_{PCL}, V_C, which is equal to $V_{CV} + V_{PCL}$, will increase more than that in the conventional ACMC, which relies on V_{CV} alone to act. In effect, CFACMC produces the stronger corrective action than the conventional ACMC, and enables the possibility to further improve the converter's dynamic response. To achieve the improved performance, the amplitude and phase of the feedforward signal, V_{PCL}, must be appropriate as the wrong signal can lead to a poor response or even instability. The amplitude and phase of V_{PCL} are dependent on the low-pass filter $P_{cl}(s)$. Therefore, the gain and cut-off frequency of $P_{cl}(s)$ must be chosen such that the improved dynamic response of the converter is attained, while their impacts on system stability are kept to a minimum.

III. Modeling of Buck Converter with CFACMC

A. Modeling of Power Stage

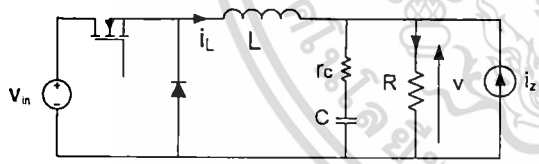
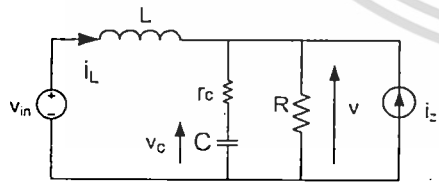
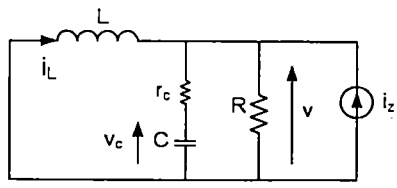


Fig. 2. Buck DC-DC Converter



(a) transistor on



(b) transistor off

Fig. 3. Circuit configurations of the CCM buck converter in one switching period

A buck converter's power stage is shown in Fig. 2. In the figure, r_c is the equivalent series resistance (ESR) of the capacitor C, R is the standing load, and the current source i_z models the load current. In Continuous Conduction Mode (CCM) where the inductor current flows continuously over one switching period, the converter exhibits two circuit states as shown in Fig. 3. During the MOSFET turn-on interval (Fig. 3(a)) the inductor is charged and its current increases linearly. During the MOSFET turn-off interval (Fig. 3(b)), the inductor is discharged and its current decreases linearly.

From Fig. 3, the state-space equation for each circuit configuration can be written as given by (1) and (2).

$$\begin{cases} \begin{bmatrix} \dot{\mathbf{i}}_L \\ \dot{\mathbf{v}}_c \end{bmatrix} = \begin{bmatrix} \frac{-R.r_c}{L(R+r_c)} & \frac{-R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & \frac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} \mathbf{i}_L \\ \mathbf{v}_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{-R.r_c}{L(R+r_c)} \\ 0 & \frac{R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} \mathbf{v}_{in} \\ \mathbf{i}_z \end{bmatrix} \\ \mathbf{v} = \begin{bmatrix} \frac{R.r_c}{R+r_c} & \frac{R}{R+r_c} \end{bmatrix} \begin{bmatrix} \mathbf{i}_L \\ \mathbf{v}_c \end{bmatrix} + \begin{bmatrix} 0 & \frac{R.r_c}{R+r_c} \end{bmatrix} \begin{bmatrix} \mathbf{v}_{in} \\ \mathbf{i}_z \end{bmatrix} \end{cases} \quad (1)$$

$$\begin{cases} \begin{bmatrix} \dot{\mathbf{i}}_L \\ \dot{\mathbf{v}}_c \end{bmatrix} = \begin{bmatrix} \frac{-R.r_c}{L(R+r_c)} & \frac{-R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & \frac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} \mathbf{i}_L \\ \mathbf{v}_c \end{bmatrix} + \begin{bmatrix} 0 & \frac{-R.r_c}{L(R+r_c)} \\ 0 & \frac{R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} \mathbf{v}_{in} \\ \mathbf{i}_z \end{bmatrix} \\ \mathbf{v} = \begin{bmatrix} \frac{R.r_c}{R+r_c} & \frac{R}{R+r_c} \end{bmatrix} \begin{bmatrix} \mathbf{i}_L \\ \mathbf{v}_c \end{bmatrix} + \begin{bmatrix} 0 & \frac{R.r_c}{R+r_c} \end{bmatrix} \begin{bmatrix} \mathbf{v}_{in} \\ \mathbf{i}_z \end{bmatrix} \end{cases} \quad (2)$$

The averaged state-space equation of the buck converter is obtained by weight average of (1) and (2) in accordance with [4], which gives:

$$\begin{cases} \begin{bmatrix} \dot{\mathbf{i}}_L \\ \dot{\mathbf{v}}_c \end{bmatrix} = \begin{bmatrix} \frac{-R.r_c}{L(R+r_c)} & \frac{-R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & \frac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} \mathbf{i}_L \\ \mathbf{v}_c \end{bmatrix} + \begin{bmatrix} \frac{d}{L} & \frac{-R.r_c}{L(R+r_c)} \\ 0 & \frac{R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} \mathbf{v}_{in} \\ \mathbf{i}_z \end{bmatrix} \\ \mathbf{v} = \begin{bmatrix} \frac{R.r_c}{R+r_c} & \frac{R}{R+r_c} \end{bmatrix} \begin{bmatrix} \mathbf{i}_L \\ \mathbf{v}_c \end{bmatrix} + \begin{bmatrix} 0 & \frac{R.r_c}{R+r_c} \end{bmatrix} \begin{bmatrix} \mathbf{v}_{in} \\ \mathbf{i}_z \end{bmatrix} \end{cases} \quad (3)$$

Linearization of (3) yields the small-signal state-space equation in (4).

$$\begin{cases} \begin{bmatrix} \dot{\hat{\mathbf{i}}}_L \\ \dot{\hat{\mathbf{v}}}_c \end{bmatrix} = \begin{bmatrix} \frac{-R.r_c}{L(R+r_c)} & \frac{-R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & \frac{-1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} \hat{\mathbf{i}}_L \\ \hat{\mathbf{v}}_c \end{bmatrix} + \begin{bmatrix} \frac{D}{L} & \frac{-R.r_c}{L(R+r_c)} & \frac{V_{in}}{L} \\ 0 & \frac{R}{C(R+r_c)} & 0 \end{bmatrix} \begin{bmatrix} \hat{\mathbf{v}}_{in} \\ \hat{\mathbf{i}}_z \\ \hat{\mathbf{d}} \end{bmatrix} \\ \hat{\mathbf{v}} = \begin{bmatrix} r_c & 1 \end{bmatrix} \begin{bmatrix} \hat{\mathbf{i}}_L \\ \hat{\mathbf{v}}_c \end{bmatrix} + r_c \, \hat{\mathbf{i}}_z \end{cases} \quad (4)$$

By applying the Laplace transform to (4), the converter's transfer functions can be found in matrix form:

$$\begin{bmatrix} \hat{\mathbf{i}}_L(s) \\ \hat{\mathbf{v}}(s) \end{bmatrix} = \begin{bmatrix} G_{vi}(s) & G_{zi}(s) & G_{di}(s) \\ G_{vv}(s) & G_{zv}(s) & G_{dv}(s) \end{bmatrix} \begin{bmatrix} \hat{\mathbf{v}}_{in}(s) \\ \hat{\mathbf{i}}_z(s) \\ \hat{\mathbf{d}}(s) \end{bmatrix} \quad (5)$$

Since only the duty cycle-to-inductor current and the duty cycle-to-output voltage transfer functions, $G_{di}(s)$ and

$G_{dv}(s)$, are required in the control design, they are determined as expressed by (6) and (7) respectively.

$$G_{di}(s)=\frac{V_{in}}{LCR}\frac{1+s(R+r_c)C}{s^2+s(\frac{1}{RC}+\frac{r_c}{L})+\frac{1}{LC}} \quad (6)$$

$$G_{dv}(s)=\frac{V_{in}}{LC}\frac{1+sr_cC}{s^2+s(\frac{1}{RC}+\frac{r_c}{L})+\frac{1}{LC}} \quad (7)$$

B. Modeling of Control Stage

Transfer functions of the current controller, $G_{cl}(s)$, and voltage controller, $G_c(s)$, in Fig. 1 are expressed by (8) and (9), respectively.

$$G_{cl}(s)=\frac{w_{cl}}{s}\frac{1+s/w_{clz}}{1+s/w_{clp}} \quad (8)$$

where $w_{cl}=1/R_{cl1}(C_{cl1}+C_{cl2})$, $w_{clp}=(C_{cl1}+C_{cl2})/R_{cl2}C_{cl1}C_{cl2}$ and $w_{clz}=1/R_{cl2}C_{cl2}$.

$$G_c(s)=\frac{w_c}{s}\frac{1+s/w_{cz}}{1+s/w_{cp}} \quad (9)$$

where $w_c=1/R_1(C_1+C_2)$, $w_{cz}=1/R_2C_2$, and $w_{cp}=(C_1+C_2)/R_2C_1C_2$

A transfer function of the PWM comparator is well known and given by:

$$F_m=1/V_p \quad (10)$$

where V_p is peak to peak sawtooth voltage.

The inductor current is sensed by R_S and then multiplied by A_{cl}, which is the gain of the current sensing amplifier (CSA). Hence, the sensed inductor current signal is:

$$V_{iL}=R_i i_{iL} \quad (11)$$

where $R_i=A_{cl}.R_S$

A transfer function of $P_{cl}(s)$ is given by:

$$P_{cl}(s)=\frac{k_p}{1+s/w_p} \quad (12)$$

where $k_p=R_{p1}/(R_{p1}+R_{p2})$ and $w_p=(R_{p1}+R_{p2})/R_{p1}R_{p2}C_p$.

C. Small-signal Model of Buck Converter with CFACMC

The small-signal model of the buck converter with CFACMC in Fig. 1 is shown in Fig. 4(a). It is manipulated into Fig. 4(b) which is then simplified into Fig. 4(c). The transfer functions $H_{cl}(s)$, $K_{cl}(s)$ and $G_{rh}(s)$ are given by:

$$H_{cl}(s)=\frac{F_m(G_{cl}(s)+1)}{1+F_mR_iG_{cl}(s)G_{di}(s)} \quad (13)$$

$$K_{cl}(s)=R_iP_{cl}(s)G_{di}(s) \quad (14)$$

$$G_{rh}(s)=\frac{H_{cl}(s)}{1-K_{cl}(s)H_{cl}(s)} \quad (15)$$

If $P_{cl}(s)$ = 0, then $K_{cl}(s)$ = 0, $G_{rh}(s)$ = $H_{cl}(s)$, and the small-signal model in Fig. 4 will beome the small-signal model of the conventional ACMC [3]. It can be observed from (15) that CFACMC has altered the transfer function of the conventional ACMC by a factor of $1/(1-K_{cl}(s)H_{cl}(s))$. Note that from (14) $K_{cl}(s)$ is dependent on $P_{cl}(s)$. At low frequencies, $K_{cl}(s)$ should be high so that the product $K_{cl}(s)H_{cl}(s)$ approaches one. As a result, $G_{rh}(s)$ in (15) is increased as well as the loop gain $G_c(s)G_{rh}(s)G_{dv}(s)$ in Fig. 4(c). The increased loop gain will lead to the improved dynamic response of the converter. At high frequencies, $K_{cl}(s)$ should be low so that the product $K_{cl}(s)H_{cl}(s)$ approaches zero. As a result, $G_{rh}(s)$ in (15) is converged to $H_{cl}(s)$. Therefore, if the cut-off frequency of $P_{cl}(s)$ is set equal to the crossover frequency of the voltage loop gain of the conventional ACMC, $G_c(s)H_{cl}(s)G_{dv}(s)$, then $G_{rh}(s)$ will be increased only up to the crossover frequency and converged to $H_{cl}(s)$ above the crossover frequency. In this way, the inclusion of the circuit block $P_{cl}(s)$ in Fig. 1 will only serve to enhance the converter's dynamic response and not affect the system stability.

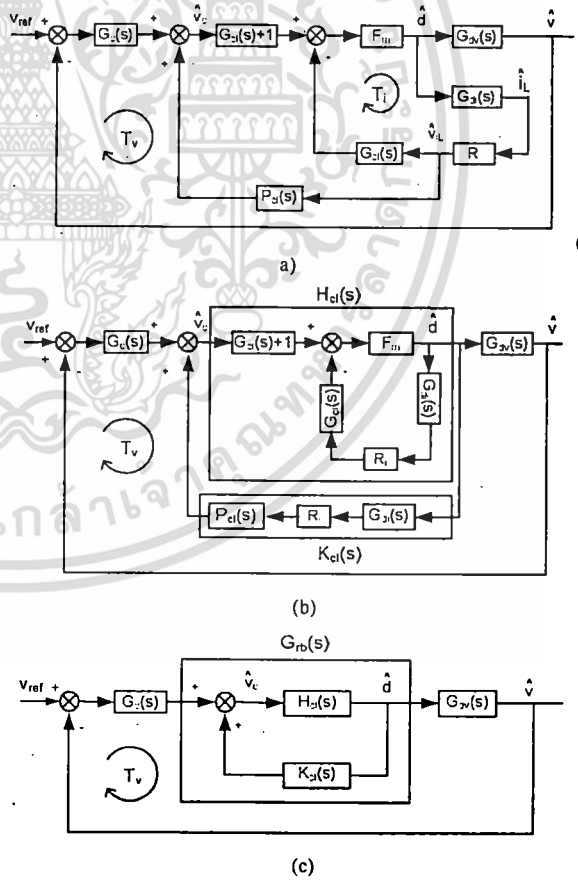


Fig. 4. Small-signal model of CFACMC

At DC frequency (s≈0), $H_{cl}(0)$, $K_{cl}(0)$ and $G_{rh}(0)$ can be expressed as:

$$H_{cl}(0)=\frac{R}{V_{in}R_t} \tag{16}$$

$$K_{cl}(0)=k_p\frac{V_{in}R_t}{R} \tag{17}$$

$$G_{rh}(0)=\frac{H_{cl}(0)}{1-k_p} \tag{18}$$

Assume that the input voltage V_{in} is constant. From (16) $H_{cl}(0)$ is proportional to the load resistor R and from (18) $G_{rh}(0)$ is proportional to $H_{cl}(0)$. Thus, $G_{rh}(0)$ is proportional to R. Fig. 5 shows the plot of $G_{rh}(0)$ in (18) as a function of k_p at the two load resistor values, R_{max} and R_{min}. When the load current is changed from minimum to maximum (i.e. the load resistor changed from R_{max} to R_{min}), $G_{rh}(0)$ will be reduced (Fig. 5). To prevent the effect of load change on $G_{rh}(0)$, from (18) k_p has to be increased, in this case, by the amount of k_1, which can be found by solving

$$G_{rh}(0)\big|_{R_{\min}}=\frac{H_{cl}(0)\big|_{R_{\min}}}{1-k_1}=H_{cl}(0)\big|_{R_{\max}} \tag{19}$$

From (19), the gain of the low-pass filter can be found:

$$k_p=k_1=\frac{R_{\max}-R_{\min}}{R_{\max}} \tag{20}$$

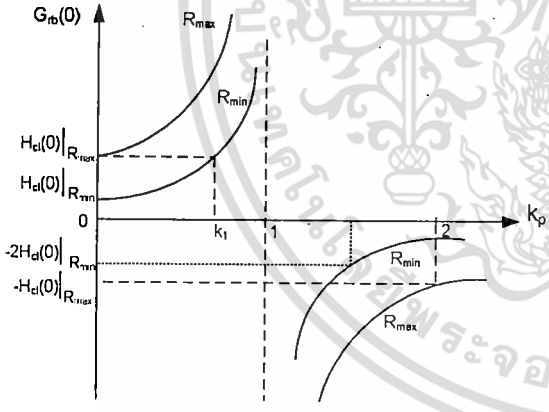


Fig. 5. Graph of $G_{rh}(0)$ versus k_p

IV. Design Example

TABLE I
PARAMETERS OF PROTOTYPE BUCK CONVERTER

V_{in}	V	L	C	r_C	R
5V	2V	45.2uH	1230uF	0.015Ω	0.4-2Ω

Circuit parameters of a buck converter are listed in Table I. The peak-to-peak voltage of the sawtooth signal is V_p=1.8V. The value of a sensing resistor is R_S=0.01Ω and the current sensing amplifier's gain is A_{cl}=7.5. The switching frequency is f_s=100 kHz.

From the parameters listed in Table I, the transfer functions in (6), (7), (10) and (11) can be calculated:

$$G_{di}(s)=4.5\times10^7\frac{2.5\times10^{-3}s+1}{s^2+738.6s+1.8\times10^7} \tag{21}$$

$$G_{dv}(s)=8.99\times10^7\frac{1.84\times10^{-5}s+1}{s^2+738.6s+1.8\times10^7} \tag{22}$$

$$F_m=1/V_p=0.55 \tag{23}$$

$$R_t=R_S A_{cl}=0.075 \tag{24}$$

A. Frequency Responses

The current controller and voltage controller are designed in the same way as do in the conventional ACMC. Hence, the design procedure outlined in [2,3] can be adopted. For the current controller design, the crossover frequency of the current loop is selected at 10kHz. The first pole of $G_{cl}(s)$ is at the origin, the zero is placed at w_{clz} = 4.482×10^{3}rad/sec, and the second pole is placed at one-third of the switching frequency or w_{clp}= 188×10^{3}rad/sec. The design yields C_{cl1}=500pF, C_{cl2}=22nF R_{cl1}=560Ω, and R_{cl2}=10kΩ. Substitution of these component values into (8) results in

$$G_{cl}(s)=\frac{7.93\times10^4}{s}\frac{1+2.2\times10^{-4}s}{1+4.89\times10^{-6}s} \tag{25}$$

For the voltage controller design, the crossover frequency of the voltage controller is selected at 5kHz. The first pole of $G_c(s)$ is at the origin, the zero is place at w_{cz}=4.3×10^{3}rad/sec, and the second pole is placed at one-third of the switching frequency or w_{cp}=188×10^{3}rad/sec. The design yields C_1=500pF, C_2=22nF, R_1=3.9kΩ, and R_2=10kΩ. Substitution of these component values into (9) results in

$$G_c(s)=\frac{1.12\times10^4}{s}\frac{1+2.2\times10^{-4}s}{1+4.89\times10^{-6}s} \tag{26}$$

As shown in the Table I, the maximum and minimum load resistances are 2Ω and 0.4Ω, respectively. From (20), k_p can be calculated:

$$k_p=0.8 \tag{27}$$

The cut-off frequency of $P_{cl}(s)$ is selected to be equal to the crossover frequency of the voltage loop gain of the conventional ACMC, which was set at 5kHz. Thus, the cut-off frequency of $P_{cl}(s)$ is w_p=31.4×10^{3}rad/s. From the values of k_p and w_p, the low-pass filter's component are calculated, yielding R_{p1}=4kΩ, R_{p2}=1kΩ, and C_p=38nF. Substitution of these component values into (12) results in

$$P_{cl}(s)=\frac{0.8}{1+3.04\times10^{-5}s} \tag{28}$$

The open loop transfer function of the CFACMC in Fig. 4(c) is given by:

$$T_v(s) = G_c(s)G_{rb}(s)G_{dv}(s) \quad (29)$$

Bode plot of (29) is shown by the solid lines in Fig. 6. In Fig 4(b), if $P_{cl}(s) = 0$, the model will become that of conventional ACMC, whose open loop transfer function is given by:

$$T_v(s) = G_c(s)H_{cl}(s)G_{dv}(s) \quad (30)$$

Bode plot of (30) is shown by the dashed lines in Fig. 6. It can be seen that the loop gain of CFACMC is greater than the loop gain of the conventional ACMC up to the crossover frequency. Above the crossover frequency, the two plots are converged. This result confirms that the designed $P_{cl}(s)$ only serves to improve the dynamic response of the converter, while keeping its impact on system stability at the minimum.

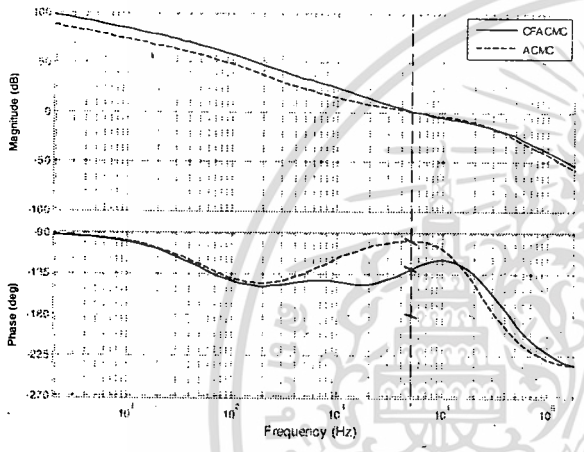
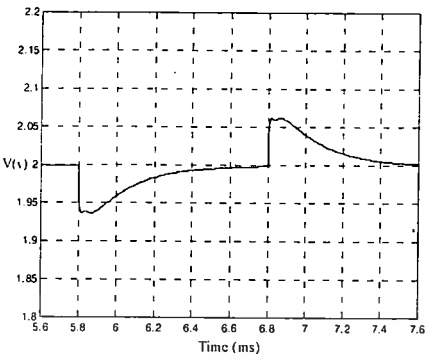


Fig. 6. Open loop frequency responses of CFACMC versus ACMC

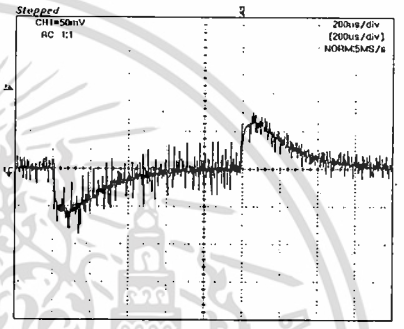
B. Time Response

The prototype converter circuit was built in order to verify the performance of CFACMC against the conventional ACMC. In the prototype circuit board, selection between the conventional ACMC (i.e. $P_{cl}(s) = 0$) and CFACMC was made by a selecting switch. The converter was subjected to a step load current change and an output voltage response of the converter recorded. Figs. 7 and 8 show the simulated and measured output voltage responses of the converter with the conventional ACMC and CFACMC respectively. In Fig. 7, the maximum voltage drop/raise is about 65mV and the settling time is about 750μs. In Fig. 8, they are about 60mV and 200μs respectively. It can be seen that while the maximum voltage drop/raise given by the two control methods is roughly the same, the settling time given by CFACMC is faster than the conventional ACMC by 450μs. This represents a significant improvement in the dynamic response time of the converter. Fig. 9 compares the results in Fig. 7 and 8 on the same scale, where the improvement yielded by CFACMC is evident.

In Figs. 7-9, the simulated results are seen to be in good agreement with their experimental counterparts. These simulated results were produced by the SIMULINK models developed in [6]. Good correspondence between the simulated and experimental results indicates the accuracy and validity of the models in predicting the converter's dynamic response.

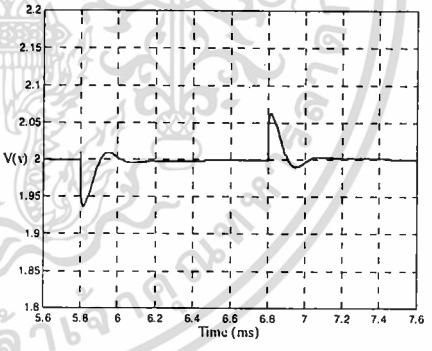


(a) Simulated

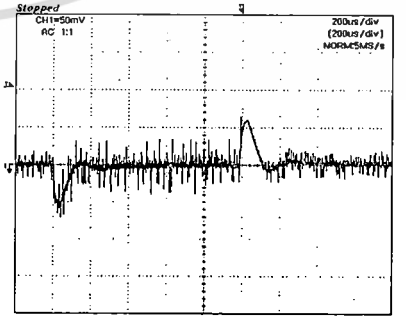


(b) Experimental

Fig. 7. Output voltage response of the buck converter with ACMC as the load current is stepped back and forth between 1 A and 4 A.

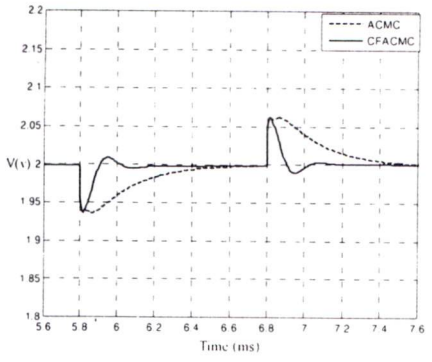


(a) Simulated

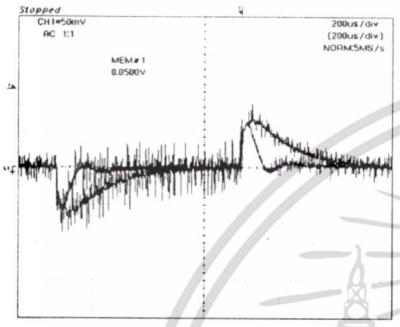


(b) Experimental

Fig. 8. Output voltage response of the buck converter with CFACMC subjected to the same loading condition as in Fig. 7



(a) Simulated



(b) Experimental

Fig. 9. Comparison between the output voltage responses of the buck converter with ACMC and CFACMC

V. Conclusions

The novel Current Feedforward Average Current Mode (CFACMC) technique to improve output dynamic performance of DC-DC converters has been proposed in this paper. It is based on feedforward of the sensed inductor current, through the low-pass filter circuit, $P_{cf}(s)$, to sum with the output signal from the voltage controller to produce the control signal. The feedforward signal helps strengthen the corrective action of the voltage loop, hence making it possible for the converter's dynamic response to be further improved from the conventional ACMC. To achieve the improved output dynamic performance, the gain and cut-off frequency of $P_{cf}(s)$ must be appropriately chosen. The equation for selecting the low-pass filter gain was derived in (20) and the low pass filter's cut-off frequency must be set equal to the crossover frequency of the voltage loop of the conventional ACMC. The capability of CFACMC in enhancing the converter's output dynamic performance was confirmed by the simulated and experimental results. Due to its simplicity and capability to significantly improve the converter's output dynamic response, the proposed CFACMC technique has a good potential for practical usage.

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